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Connection to Line

Transformer Selection

The major criterion for the selection of a transformer is that it should not significantly attenuate or distort the signals travelling between MT8971B/72B's. A transformer with the following specifications may be used:

Primary Inductance	30mH min.
Primary Leakage Inductance	200µH max.
Primary Resistance	2.25Ω max.
Secondary Resistance	1.0Ω max.
Turns Ratio	Primary 4 Secondary1:1 Secondary2:1
Longitudinal Balance	70dB @ 200Hz 60dB @ 1kHz 46dB @ 100kHz
DC Current without saturation	100mA max.

A center-tap to ground on the secondary will probably be necessary to ensure good longitudinal balance. The effect of the variations from the specification can be checked with a spectrum analyzer.

Protection Circuit for the LIN Pin

In a typical application, the LIN pin of the MT8971B/72B will be connected to a line through a transformer. This means that voltage spikes on the line could cause the voltage at LIN to exceed its Absolute Maximum Rating and damage the device. The circuit shown in Figure 1 is designed to prevent this.

The diodes, D1 and D2 clamp the voltage received from the line. Further protection is provided by R1 which limits the current at LIN. The diodes will handle several amps of current from the line before the Absolute Maximum Ratings on LIN are exceeded.

Generation of ST-BUS Timing Signals for MT8971B/72B in Master Mode

The circuit shown in Figure 2 generates the ST-BUS framing and clock signals for the MT8971B/72B in Master Mode.

The basic clock source is a 16.384 MHz oscillator. This is used as an input to the MT8940 which generates all the ST-BUS timing signals except C10. C10 is generated by the phase-locked loop formed by the remaining components. The C10 clock is the output of the 74LS624 Voltage Controlled Oscillator. This is input to the 74LS163 counter which is

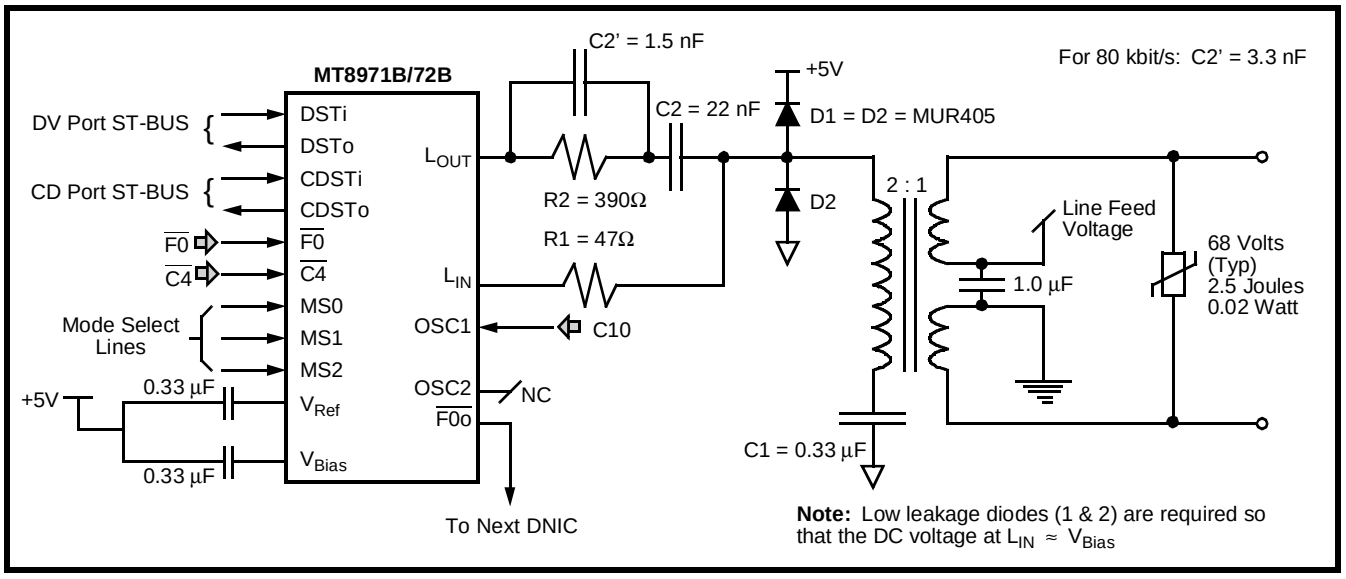


Figure 1 - Connection to Line

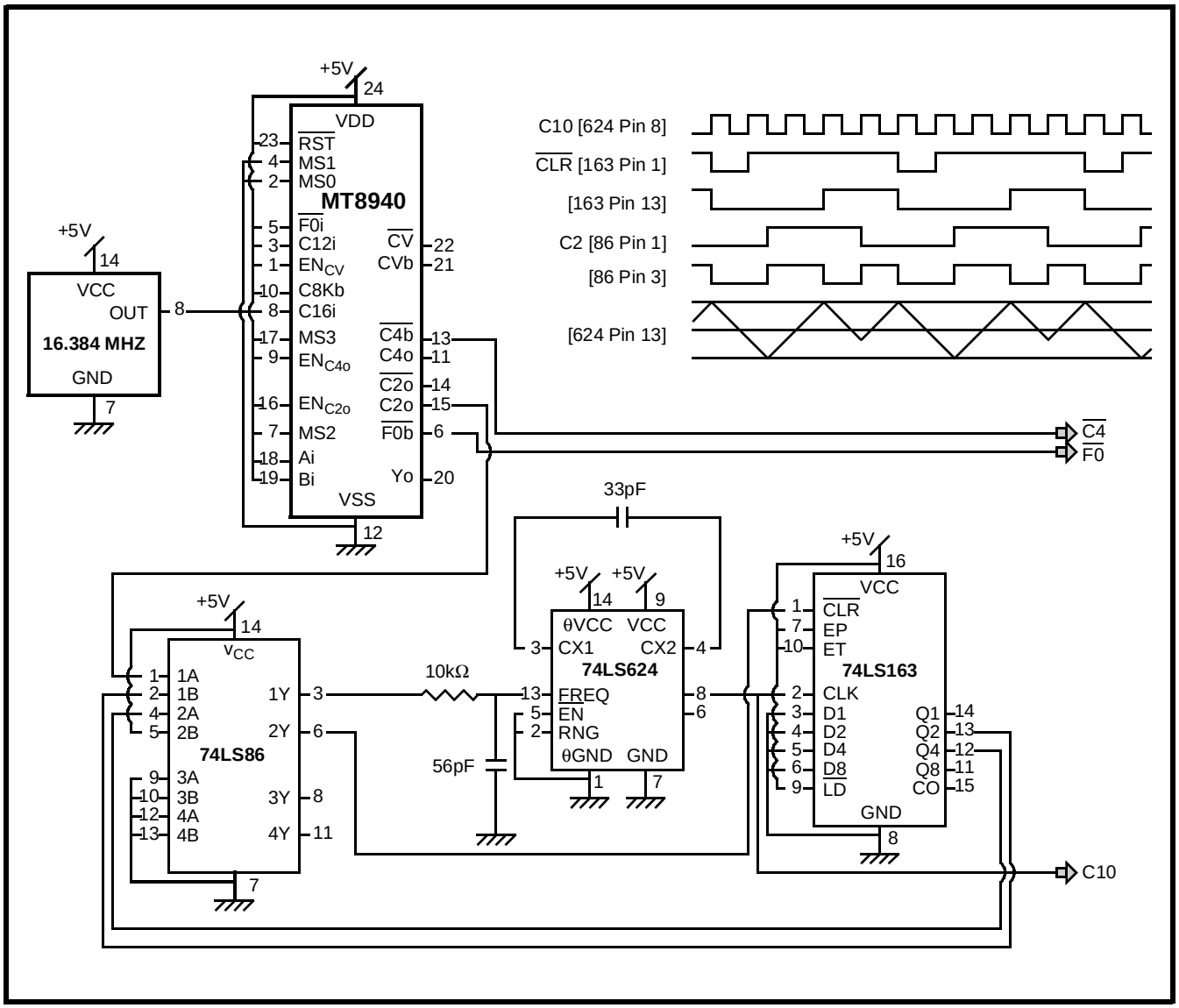


Figure 2 - Generation of ST-BUS Timing Signals for MT8971B/72B in Master Mode

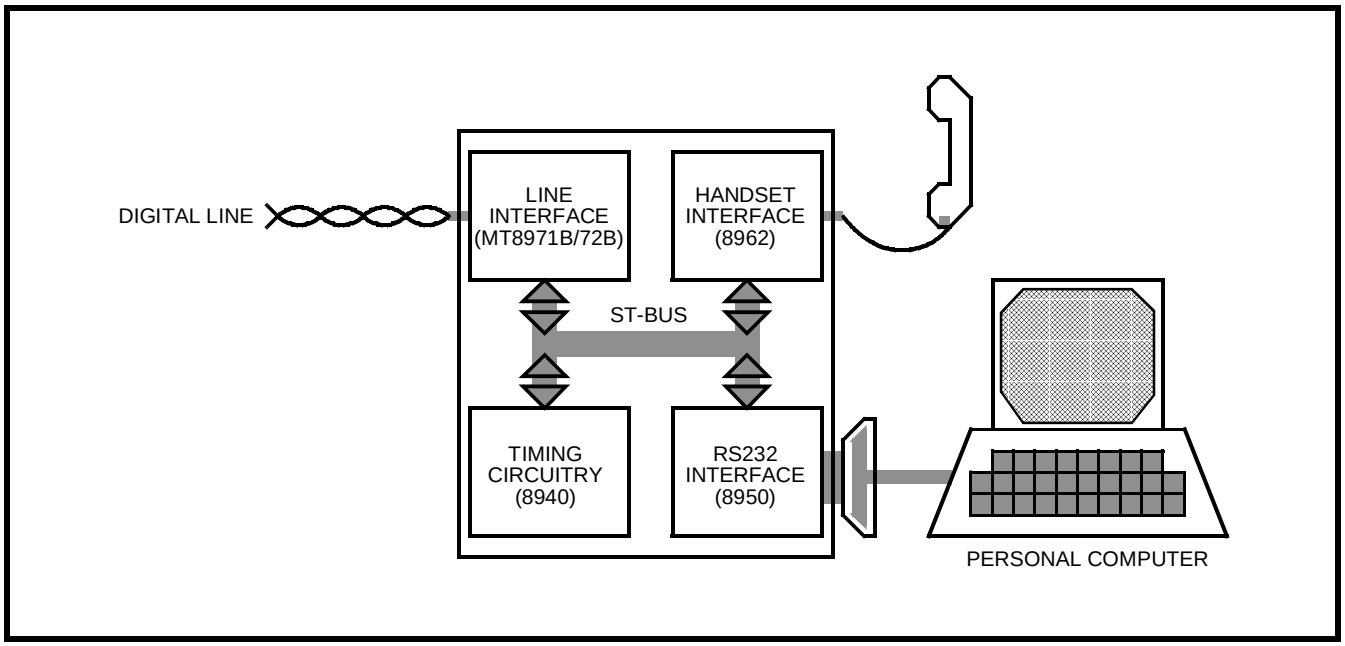


Figure 3 - Integrated Voice and RS232 Data Capability for a Personal Computer

synchronously reset to 0 after it reaches a count of 4, giving an output which is the 10.24 MHz input divided by 5. This 2.048 MHz output is compared to the C2 clock generated by the MT8940 using the 74LS86 exclusive-or chip.

As C2 slows down, the overlap between the two signals increases causing the output of the exclusive-or to spend more time low. This reduces the input voltage on the 74LS624 and so causes C10 to slow down. The phase-locked loop was found to lock when the period of C2 was between 400 ns and 600 ns.

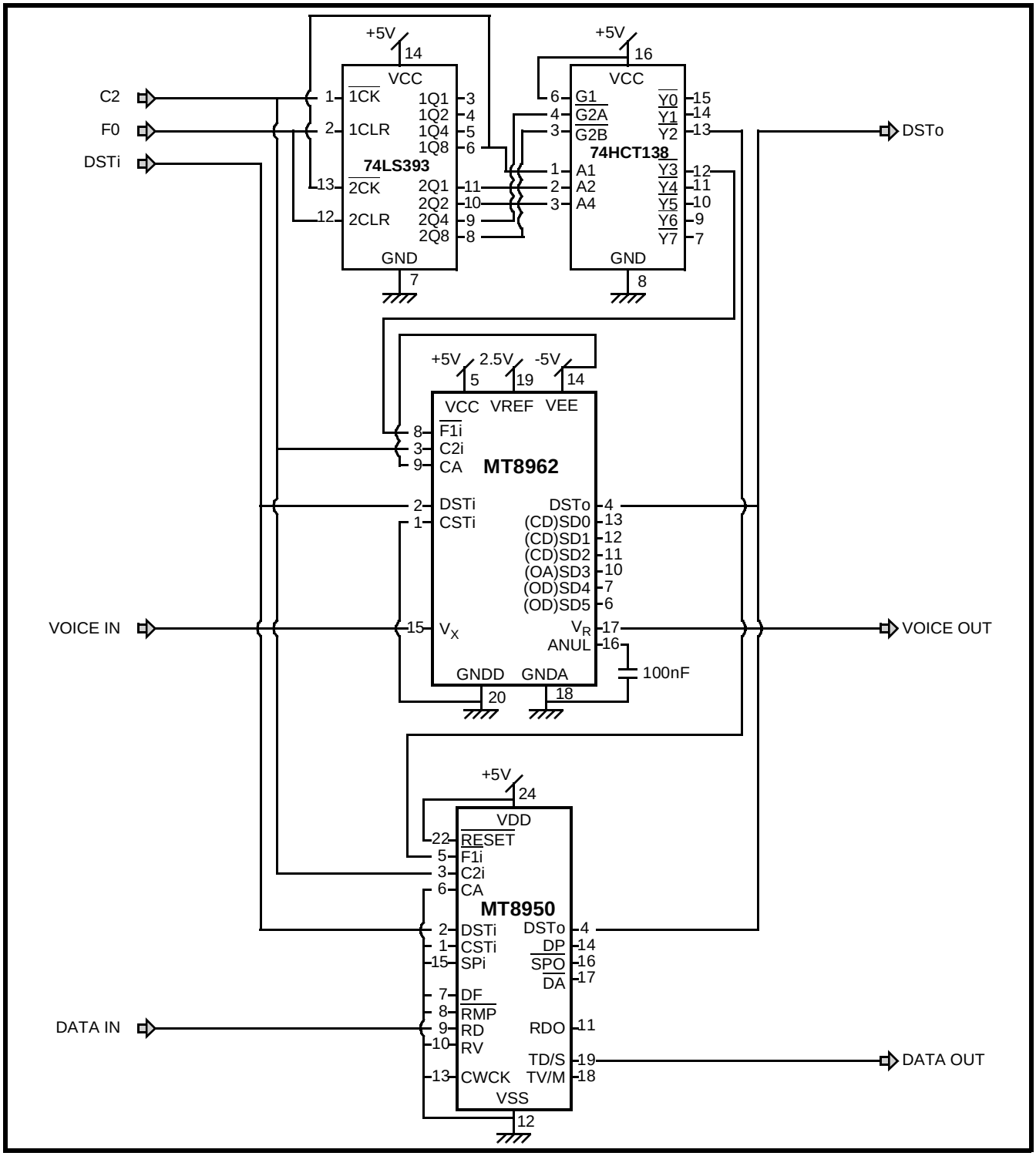


Figure 4 - Handset and RS232 Interface Circuit

Integrated Voice and RS232 Data Capability for a Personal Computer

Figure 3 shows how an integrated voice and data capability can be added to a Personal Computer.

Data is transmitted and received on the ISDN - compatible digital line using an MT8971B/72B. If the MT8971B/72B acts as master on the line then timing is provided by an MT8940. If the MT8971B/72B acts as a slave then it extracts timing from the line and passes it on to the rest of the circuit.

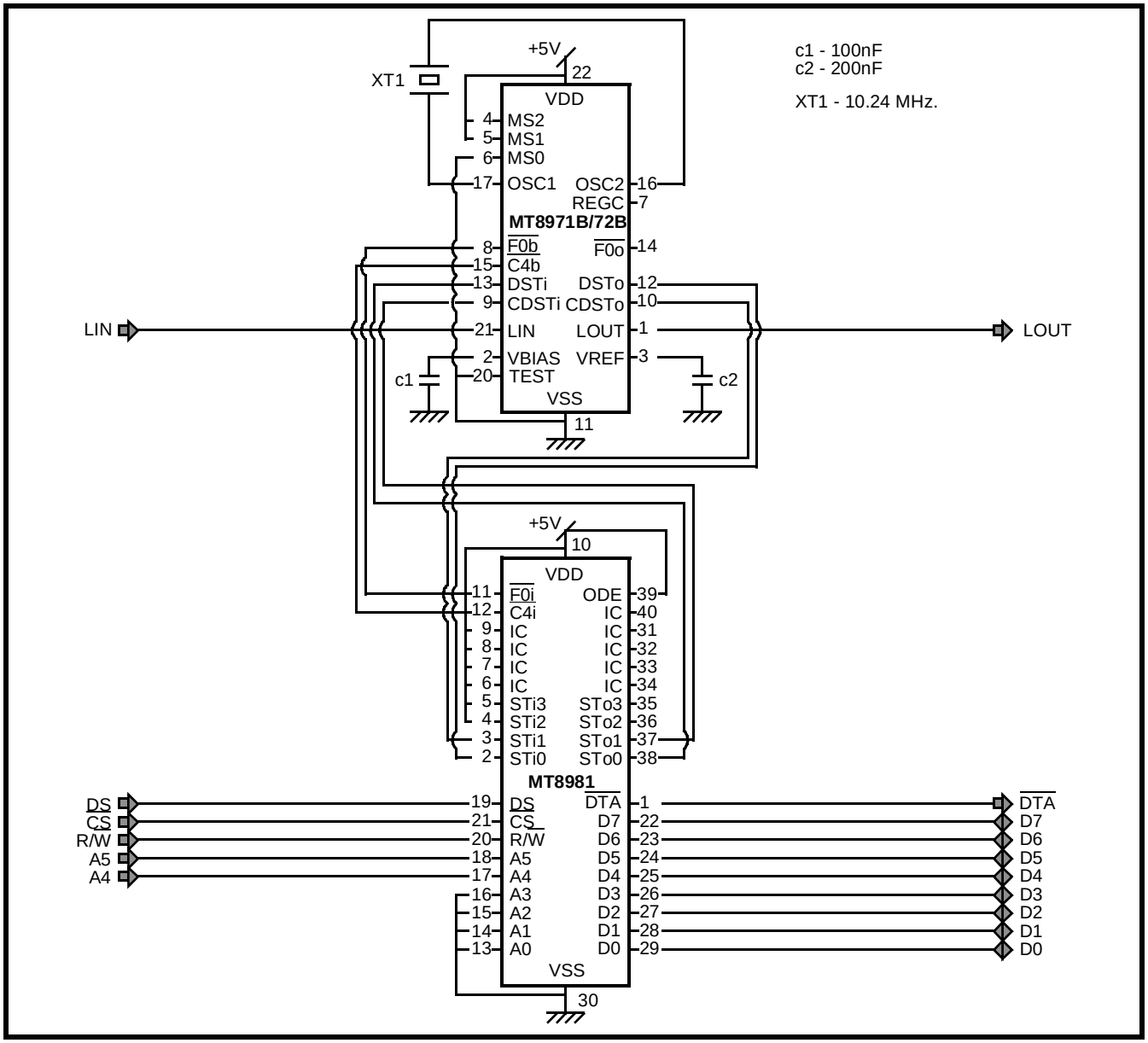
The basic schematic diagram for the handset and RS232 interface is shown in Figure 4. Level shifters (typically an MC1488 and an MC1489) for the RS232 interface and a suitable transducer interface for the handset complete the design.

This particular approach could be used with any Personal Computer which can handle an RS232 link. No additional software is required and there is no microprocessor to be programmed.

Microprocessor Interface to MT8971B/72B

Figure 5 shows a simple microprocessor interface to a MT8971B/72B in Slave Mode. A similar approach can be used for Master Mode.

The MT8971B/72B in Slave Mode generates the ST-BUS frame and clock signals needed for the MT8981. As only channels 0 and 16 are used on the ST-BUS streams in this configuration, the A0 to A3 address lines on the MT8981 can be strapped to



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ground. This reduces the number of address lines needed for the microprocessor interface.

The status of the MT8971B/72B and data received from the line can be read through the MT8981 by selecting the appropriate input stream and reading the appropriate channel. The MT8971B/72B can be controlled and data transmitted on LOUT by selecting the appropriate memory on the MT8981 and writing to the appropriate channel. The MT8981 is used in its Message Mode here.

Digital Line Card

A digital line card can be built by chaining MT8971B/72B's together (see Figure 6).

The first MT8971B/72B in the chain receives a framing signal from the system and generates a delayed framing signal for the second MT8971B/72B. Each subsequent MT8971B/72B in the chain accepts the framing signal output by the previous MT8971B/72B and generates a delayed signal from it. This eliminates the need for a timeslot assignment circuit for the MT8971B/72B's on the digital line card.

In this example data is transmitted down the lines from channels on the DSTi input stream and data from the lines is output on channels on the DSTo output stream. The MT8971B/72B's are controlled and monitored on the channels on the CSTi and CSTo streams.

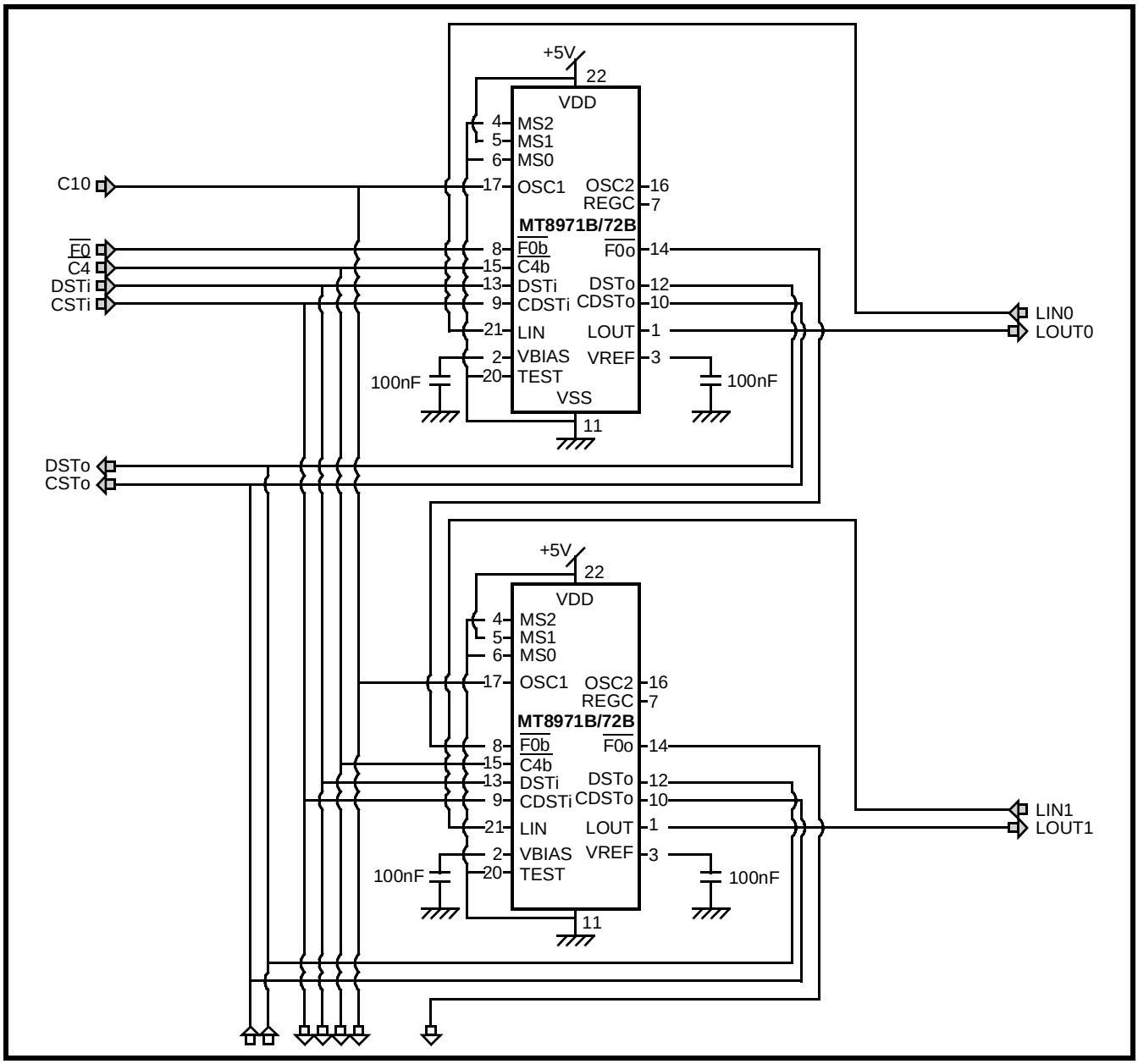

Figure 6 - Digital Line Card

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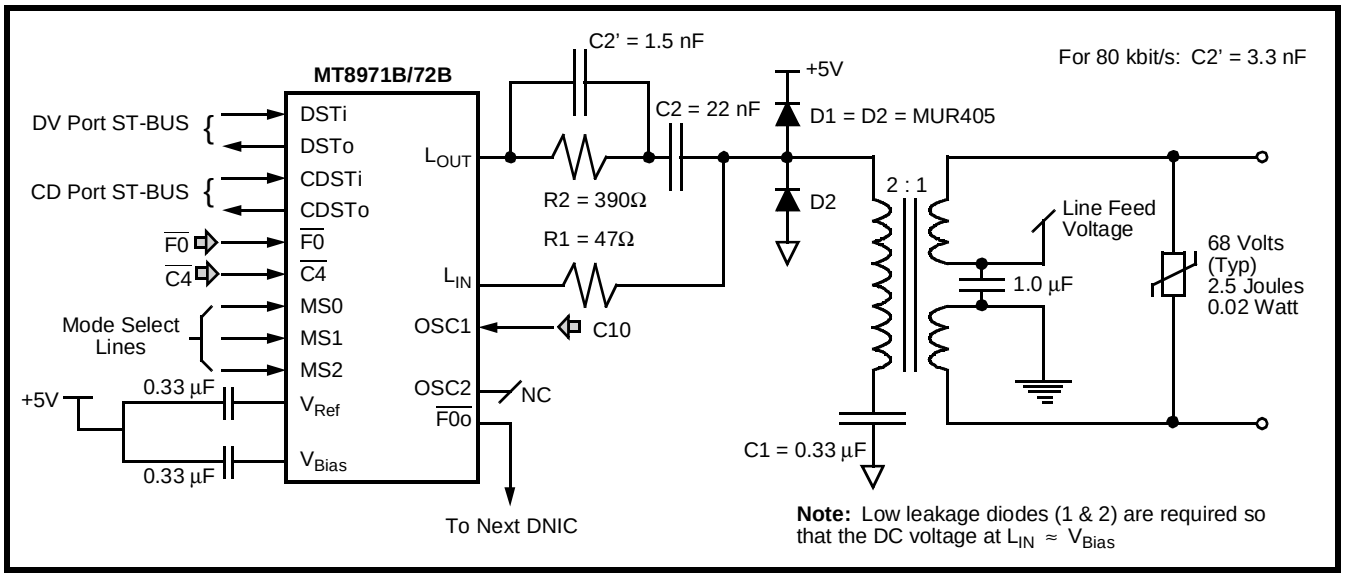

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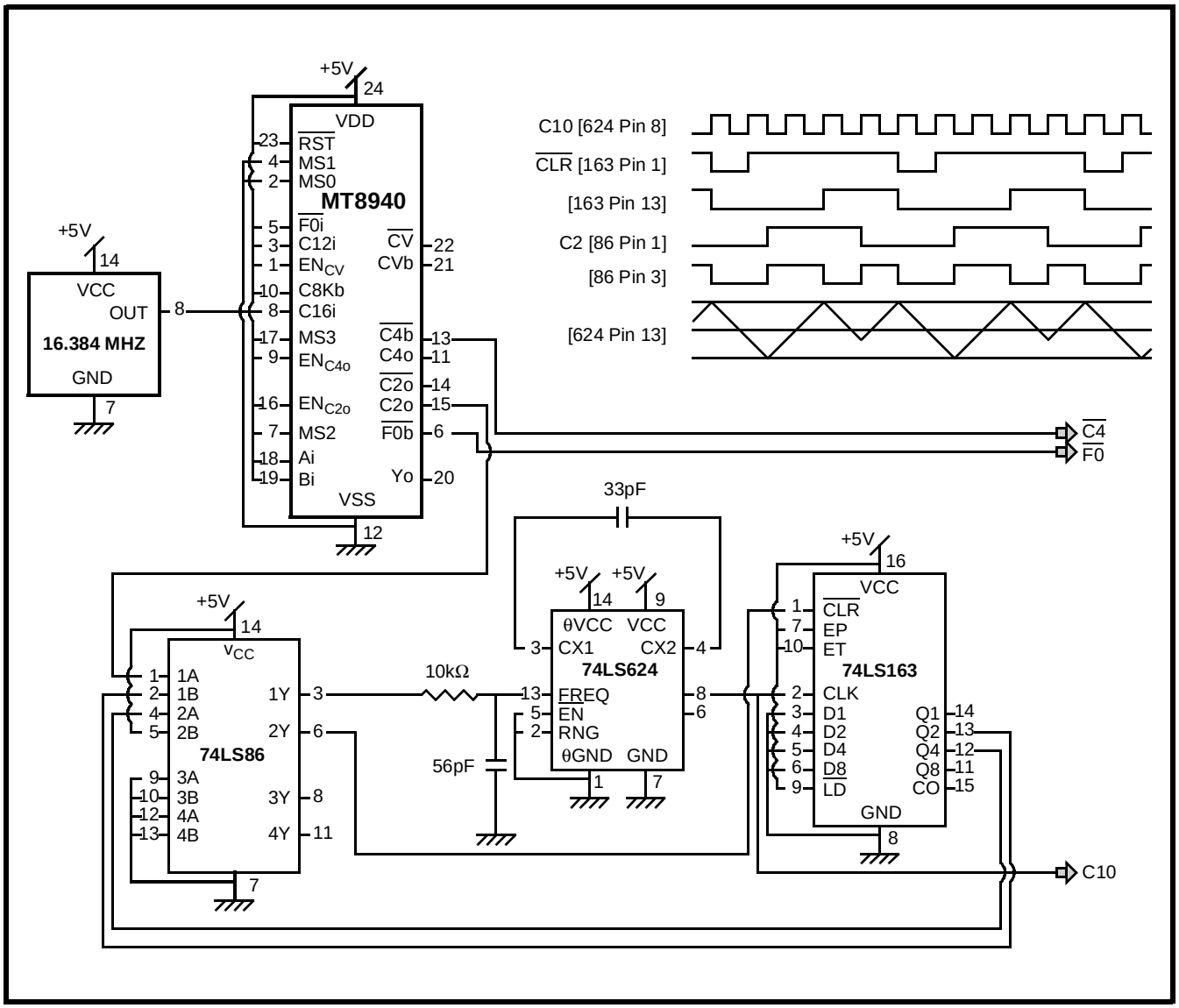

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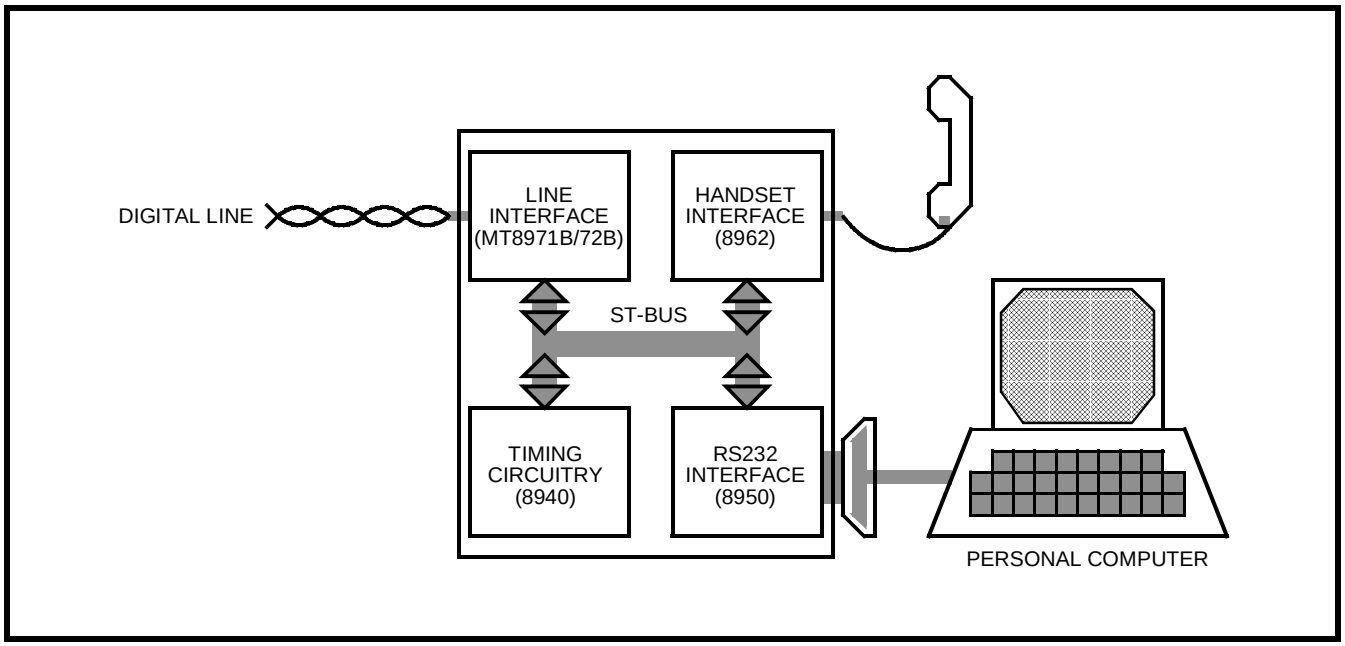

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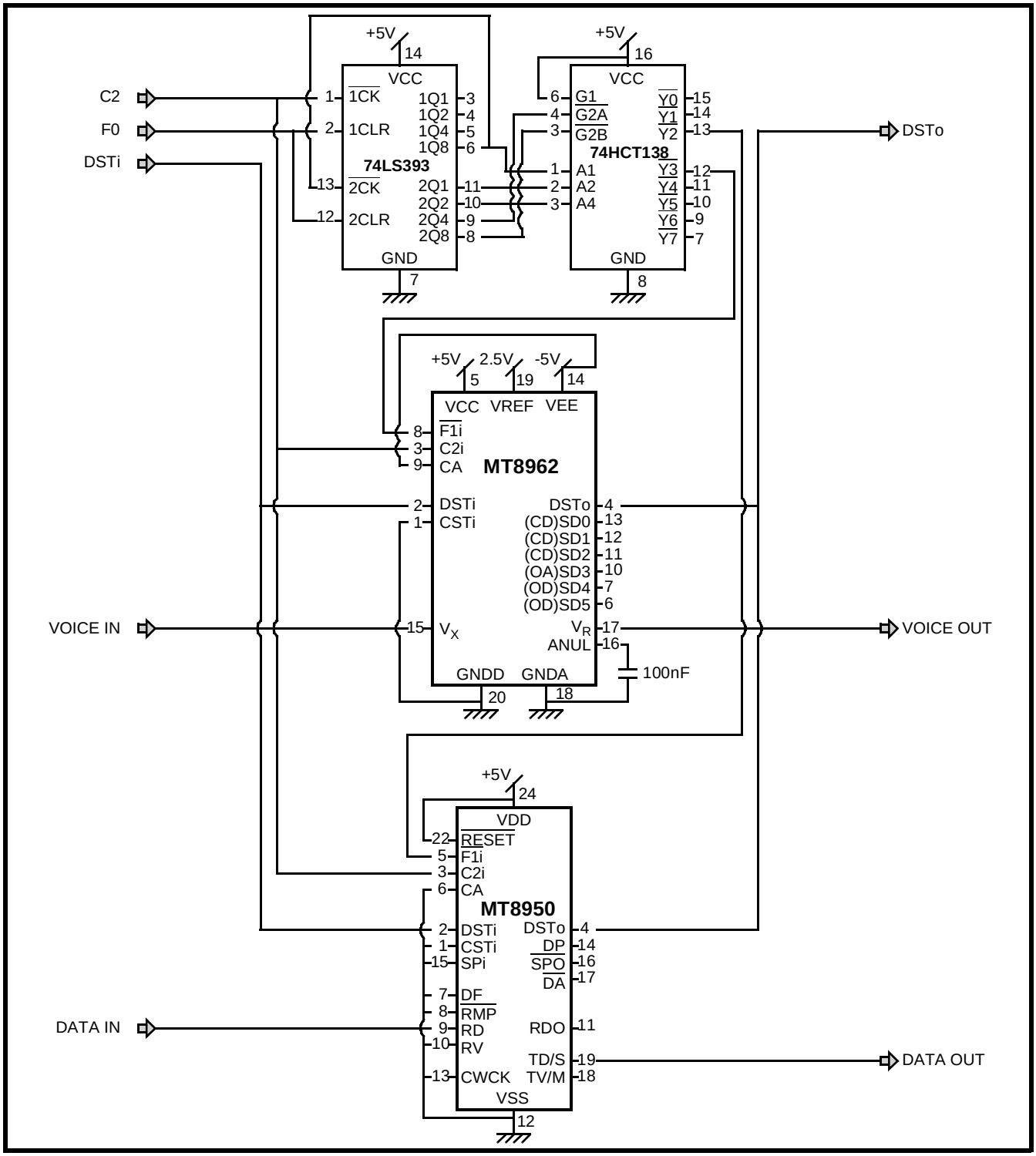

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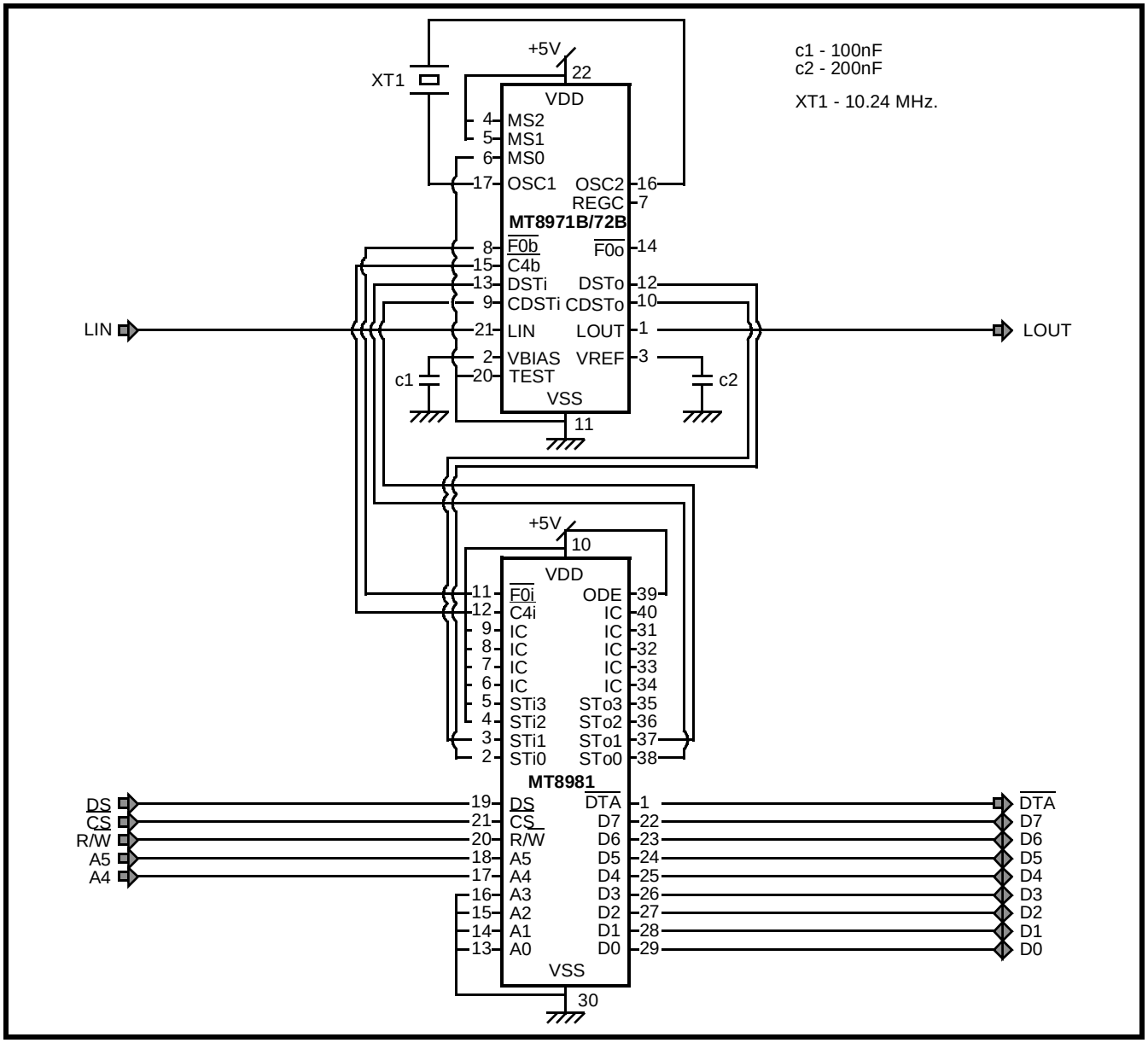

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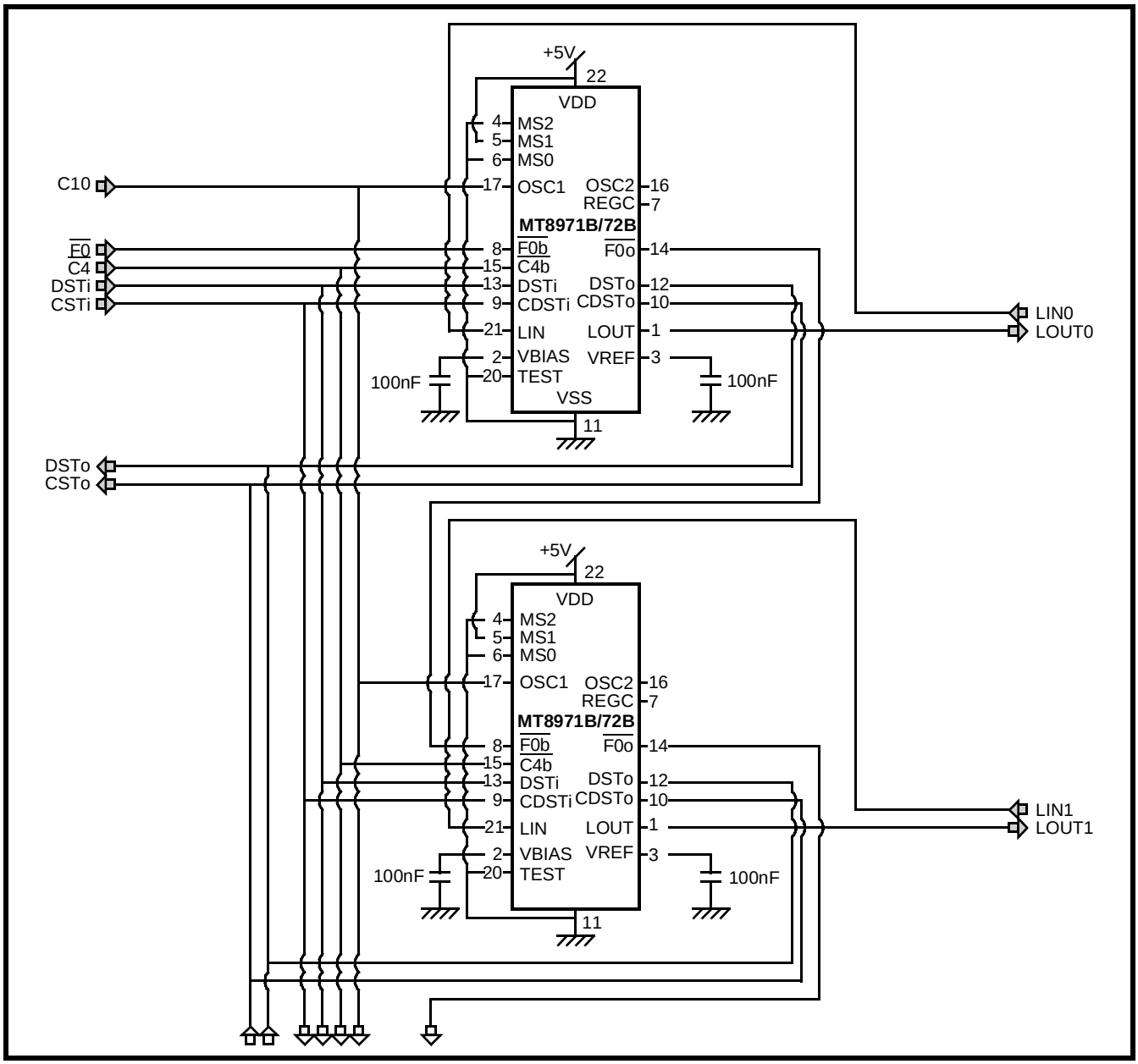

Figure 6 - Digital Line Card

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