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1.0 Introduction

The switching matrix is generally one of the most important elements in any digital communication system. Traditional implementations of switch matrices, with channel capacity in excess of 2048 channels, have been typically based on discrete memory components; with numerous counters, latches and decode logic to generate addresses, timing signals, and, provide a processor interface. Commercially available digital switch devices have in the past been either too inflexible in terms of the input/output timing requirements or their use has not been practical due to the excessively large number of components required to implement the matrix. The Mitel MT9080 Switch Matrix Module (SMX) and MT9085 Parallel Access Circuit (PAC) address these shortcomings to provide a cost effective and optimized solution for large matrix implementation.

The MT9080 (SMX) is a flexible memory component which has been optimized for use in the construction of large switch matrices. The device has separate 16 bit input and output ports. A 16 bit address bus and a full microprocessor interface is also provided. An internal counter generates sequential addresses for the memory. Depending on the specific application, the addresses generated by the counter can be used to clock data in or out of the device. A 2048 channel, non-blocking, switch with 16 bit input/output ports can be constructed using three SMXs. The maximum input/output data rate that the SMX can support is 16.384 Mb/s. There is no restriction on the lower data rate limit other than bandwidth requirements imposed by the type of signal to be switched through the device. Serial interface to the switch, if necessary, can be provided by the MT9085 (PAC). The PAC can be configured to perform serial-to-parallel or parallel-to-serial conversion. It supports the standard 2.048 Mb/s Mitel ST-BUS format and also a 4.096 Mb/s serial data rate format.

This application note presents details on how the MT9085 and MT9080 can be used to construct switch matrices. Details on implementation of 1024, 2048, 4096 and 8192 channel switch matrices are presented following an introduction to digital switching basics. The discussion includes detailed timing information and throughput delay considerations for the various configurations. Information presented in this note is intended to

supplement the PAC and SMX data sheets. It is assumed that the reader has a basic understanding of the functional features of the two devices. Please refer to the MT9080 and MT9085 data sheets for a detailed pin and functional description.

2.0 Digital Switching Basics

In most digital voice and data communication switching systems, the signals are multiplexed in a fixed manner to establish time division multiplexed (TDM) busses. The multiplexed bus can be parallel or serial. Switching of channels in a parallel time division multiplexed bus is accomplished by changing the timeslot occupied by the channel in a frame. The switch is referred to as a timeslot interchange circuit. For switching pulse coded modulated voice signals, the frame rate is fixed at 8 kHz. The data rate depends on the total number of channels to be handled by the switch. For example, to handle 256 parallel channels, the data rate has to be 2.048 Mb/s. Similarly, to handle 1024 channels,

the data rate has to be 8.192 Mb/s. An example of a parallel TDM bus and a timeslot interchange circuit is illustrated schematically in Figure 1.

Serial time division multiplexed switches generally employ more than one link; each link being made up of a number of channels per frame. Once again, the frame rate for voice switching applications is fixed at 8 kHz. The number of channels per frame is dictated by the architecture of the system. Mitel's ST-BUS architecture, for example, has 32 channels per frame. The ST-BUS aggregate data rate is 2.048 Mbit/s with each channel being made up of 8 bits. In most system level applications, it is necessary to be able to switch between timeslots on a specific link and also between other links.

A circuit switch matrix implementation typically requires two blocks of memory. Data to be switched is clocked into the "Data Memory" block and is stored in sequentially addressed locations. It is read out of the Data Memory according to the address supplied

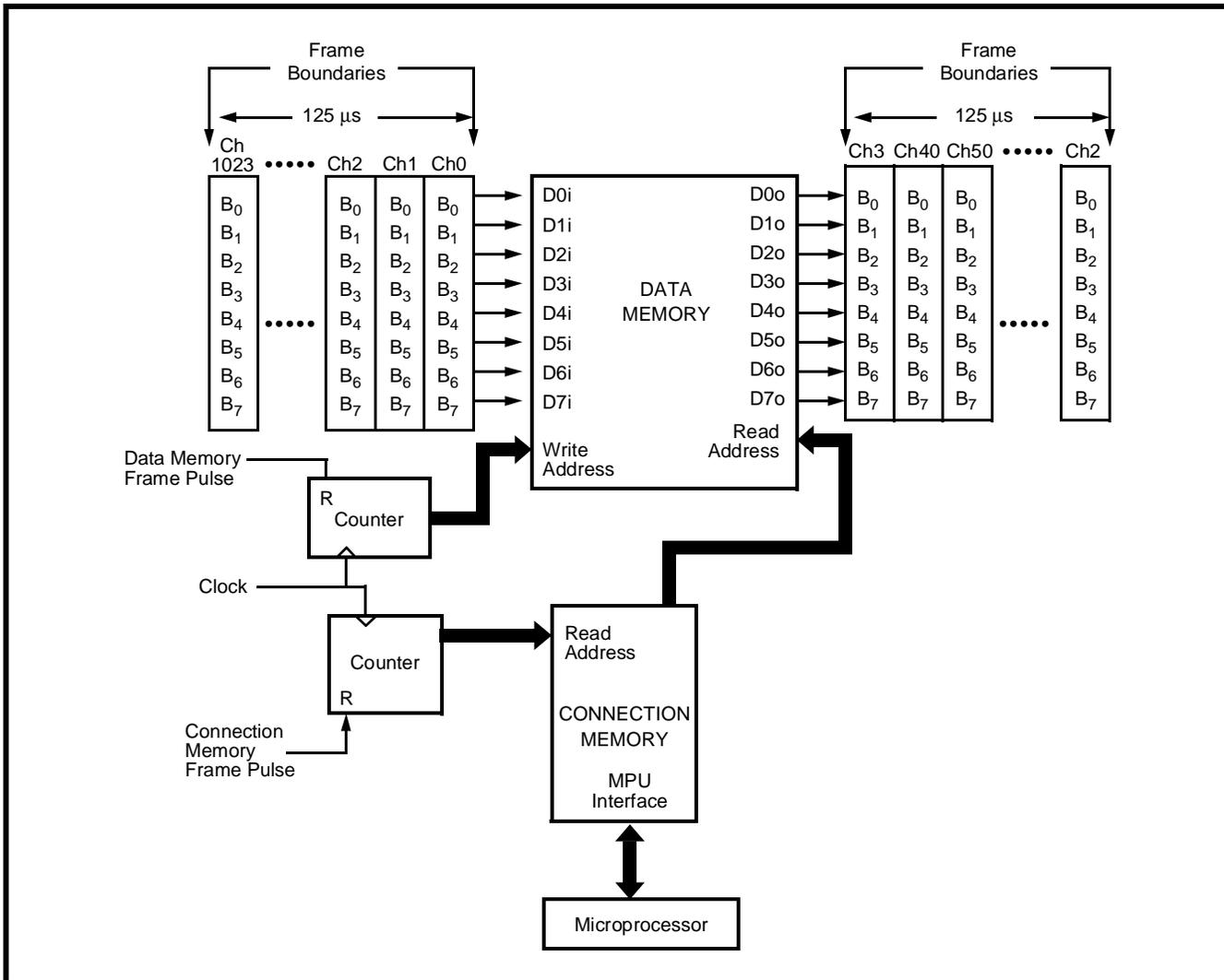


Figure 1 - Example Parallel Timeslot Interchange Circuit

by the "Connection Memory" block. The data memory is accessed twice during each timeslot; first for the read operation, and the second time for the write operation. The maximum number of channels that can be supported by a single memory is given by the following simple relationship:

$$C = \frac{T_f}{2t_c}$$

where T_f is the frame rate in microseconds and t_c is the minimum memory access time in microseconds. For voice switching applications, T_f is equal to 125 microseconds (to accommodate 8 kHz sampling employed by PCM codecs). The time constant, t_c , depends on the technology used to implement the memory. In the SMX, t_c is equal to 60 ns; implying that the maximum switch size that can be constructed with one SMX data memory block is 1024 channels. Larger switch matrices can be created by using more than one SMX for the data memory. Details presented in sections 4 and 5 illustrate how this can be accomplished. The MT9085 Parallel Access Circuit is used to interface the SMX to serial TDM busses.

3.0 Design of 1024 Channel Switch

3.1 Parallel Timeslot Switch

A 1024 (1K) channel, non-blocking, timeslot interchange switch can be constructed using two SMX devices. One SMX serves as the Data Memory while the second one operates as the Connection Memory.

3.1.1 Circuit Description

A circuit diagram is shown in Figure 2. Data to be switched is clocked into SMX-1, the Data Memory, via the 16 bit input data bus and stored sequentially in memory locations addressed by the internal 11 bit counter. Data is read out of the memory according to the address supplied by the connection memory (SMX-2). The connection memory clocks out its contents according to the addresses supplied by the internal 11 bit counter. SMX-1 is operated in either Data Memory mode-1 (DM-1) or Data Memory mode-2 (DM-2) depending on the application requirements (see sec. 3.1.2). SMX-2 is operated in Connect Memory mode-1 (CM-1).

In order to address 1K of memory, only ten address lines are required. Output lines D0 to D9 from the connection memory are connected to address lines A0 to A9 on the data memory. The remaining data

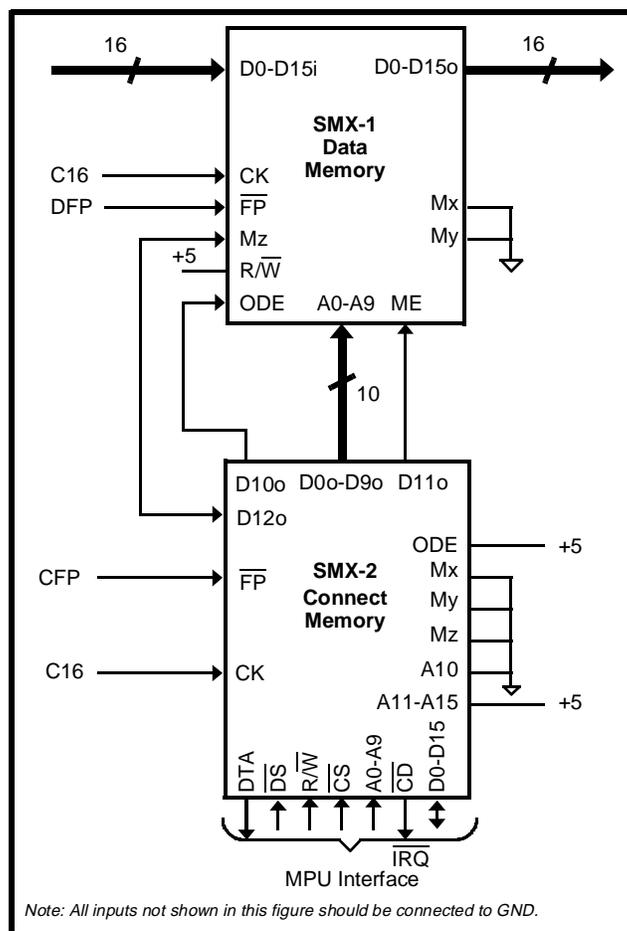


Fig. 2 - 1024 Channel Parallel Timeslot Interchange Circuit

lines from the connection memory can be used to control other features. In the example illustrated, D10 is used to enable the output drivers via ODE. D11 is used to control the Message Enable function, while D12 is used to select between Data Memory modes 1 and 2. Using these interconnections, Data Memory address and control functions can be mapped onto specific bits of the Connect Memory to form a 16 bit control word as shown in Figure 3.

The clock supplied at the CK input of both the devices has a frequency of 16.384 MHz. A framing signal with a frequency of 8 kHz is used to delineate frames with 1024 channels each. The data rate on the parallel bus is 8.192 Mb/s. Each timeslot is made up of two clock periods of the C16 clock. A detailed timing diagram is shown in Figure 4. Note that the Data Memory Frame Pulse (DFP) occurs seven clock periods after the Connection Memory Frame Pulse (CFP). This phase delay synchronizes the internal counters of the two SMXs such that the connection memory clocks out the addresses and the control bits (for ODE, ME and Mz) on D0-D12o one channel ahead of the affected output data memory timeslot. The address and other control signals are latched into the data memory with a

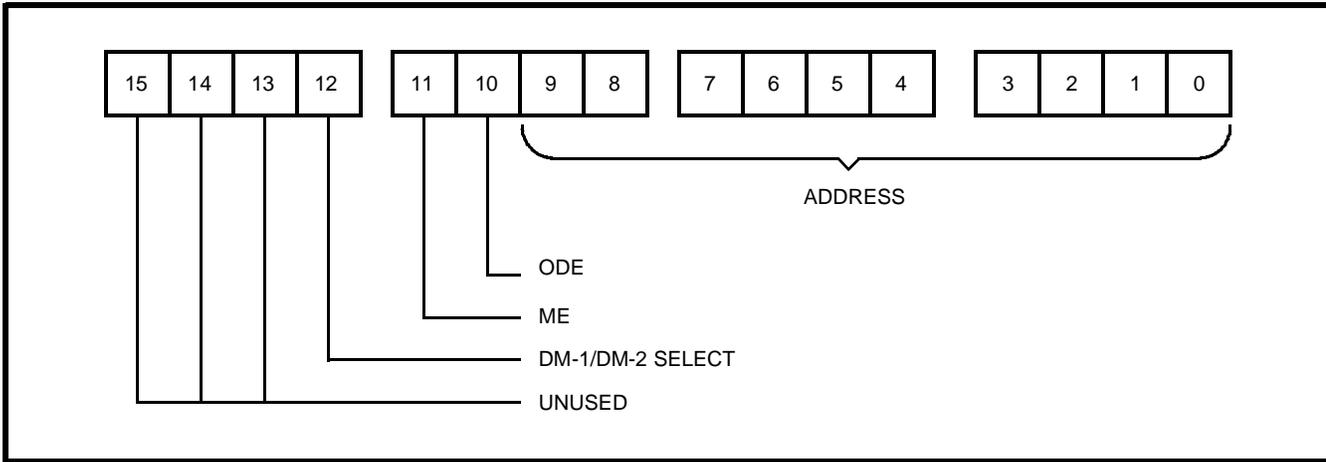


Fig. 3 - Mapping of Data Memory Address and Control Functions onto Connection Memory Data Bits

positive edge of the clock. In this example, the phase delay between the connection memory frame pulse and the data memory frame pulse results in the input and output data frames having a specific phase relationship. It is possible to time the two frame pulses such that the input and output frames are offset by any number of clock periods. The Data Memory frame pulse determines the channel timeslot boundaries and the input frame boundary. The Connection Memory Frame pulse indirectly defines output frame boundaries.

The Change Detect output of the connection memory is used to interrupt the MPU. As described in the MT9080 data sheet, \overline{CD} will go low when the internal Cyclic Redundancy Check (CRC) performed by the device indicates a change in memory contents from one frame to the next. The CD output will go low only if the change in memory contents occurs due to some event other than a direct processor access of the device. This could be due to power supply spikes or static discharges, etc. The feature acts to

provide an extra margin of security and is particularly useful in systems such as Digital Crossconnects where the connection memory is configured once and not modified for long periods of time. The CRC check uses an X+1 polynomial per bit (for a total number of bits equal to 16).

3.1.2 Throughput Delay Considerations

The delay through the SMX for any switching configuration is determined by the mode of operation.

When the SMX is operated in Data Memory mode-1, the throughput delay depends on the difference between the input and output channel timeslots. If the difference between the input and output channel is less than two timeslots, then data clocked into the device in the current frame will be clocked out in the next frame. On the other hand, if the difference between the input and output timeslots is greater

Data Memory Mode -1			Data Memory Mode - 2		
Input Timeslot	Output Timeslot	Throughput Delay	Input Timeslot	Output Timeslot	Throughput Delay
n	n	1 Fr.	n	n+L	1 Fr.+ L Ch.
n	n+1	1 Fr. + 1 Ch.	n	n- k	1 Fr. - k Ch.
n	n+m	m Ch.	n	0	2 Fr. - n*
n	n- k	1 Fr. - k Ch.	n	1	2 Fr. -(1+n)Ch.*

$n = 0, 1, 2 \dots 1023$
 $m = 2, 3 \dots 1023$
 $m+n \leq 1023$
 $k \leq n$

$n = 0, 1, 2 \dots 1023$
 $L = 0, 1, 2 \dots 1023$
 $n+L \leq 1023$
 $n+L \neq 0$ or 1 when input/output data frames are aligned.
 $k \leq n$
 *Applies only to the cases where input/output frames are aligned.

Table 1. Summary of Throughput Delay for 1024 Channel Parallel Switch Circuit

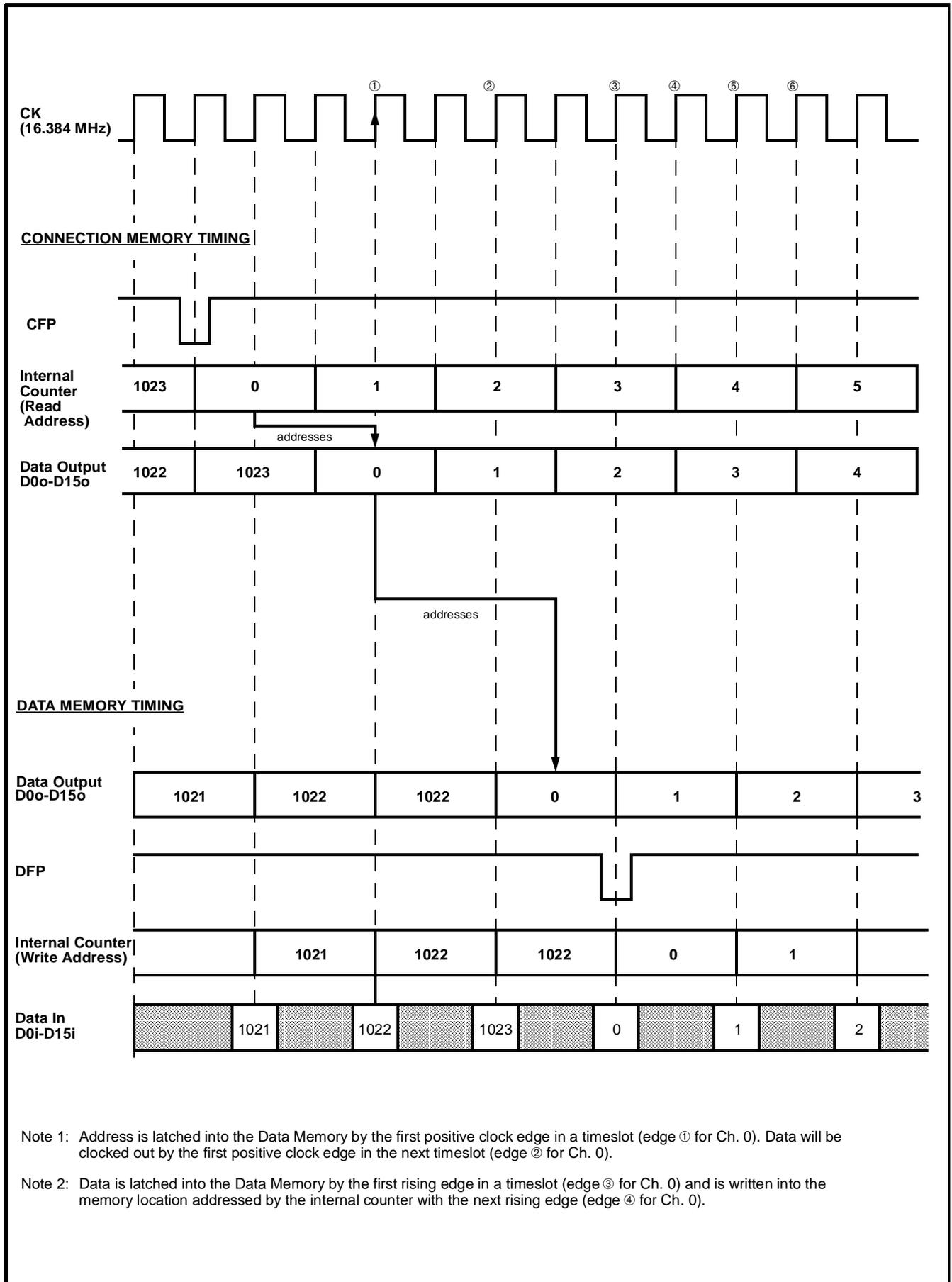


Figure 4 - 1024 Parallel Timeslot Interchange Circuit Timing

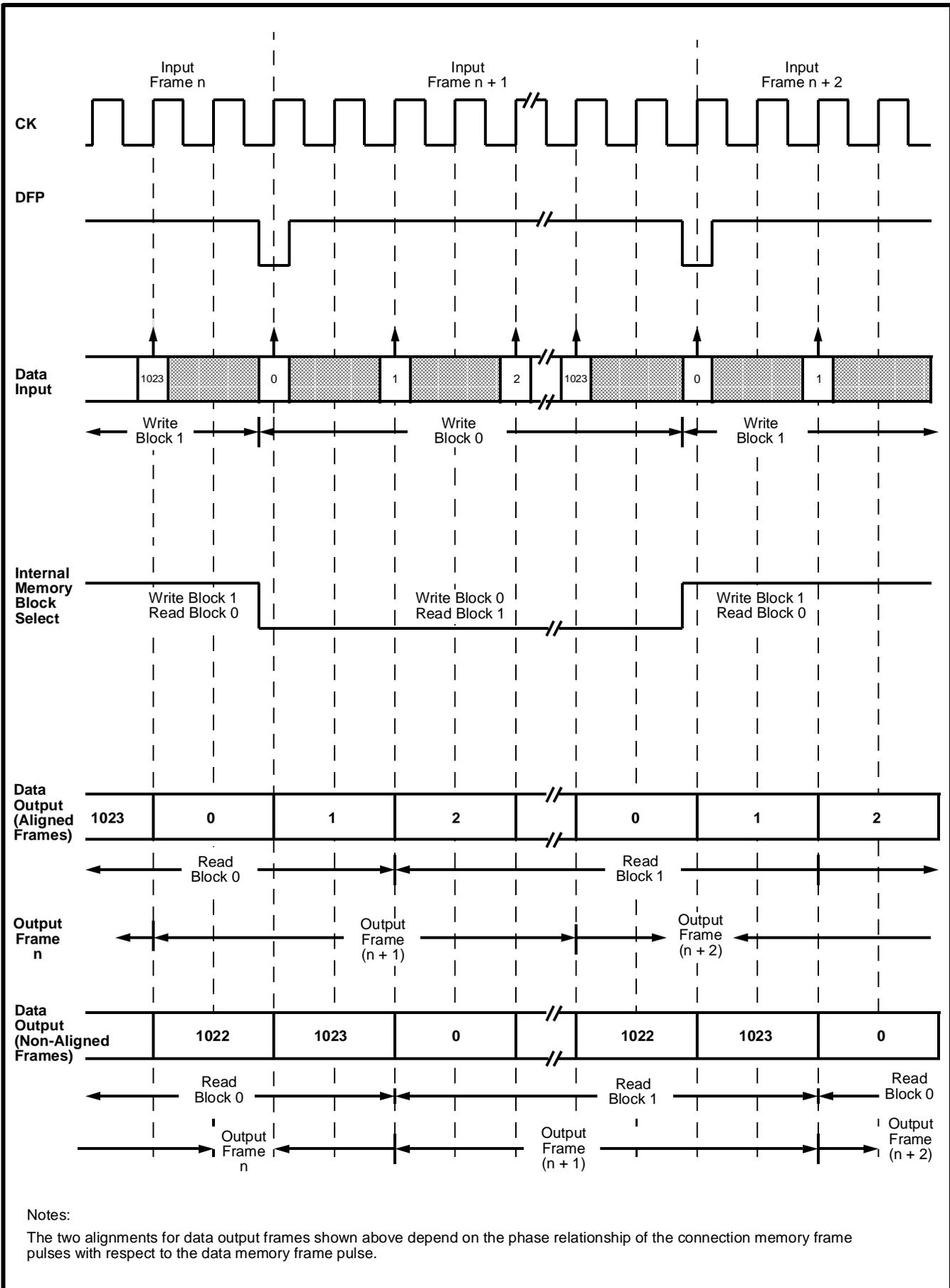


Figure 5 - Data Memory Mode-2 Functional Timing

than or equal to two timeslots, data clocked in the current frame will be clocked out in the same frame. For example, if the contents of input timeslot 1 are to be switched to output timeslot 2, data clocked in frame "n" will be clocked out in frame "n+1". However, if timeslot 1 is switched to timeslot 3, data will be clocked out in the same frame (frame n). The reason why this happens can be understood if the timing diagram in Figure 4 is examined. Note that input channel 1 is latched into the device with the CK clock edge marked 5. The data in channel 1 will subsequently be stored in the memory with the next clock edge (marked 6). Data for channel 2 is clocked out with the edge marked 5. Because this event occurs before the data is actually stored in the memory, data clocked out during channel 2 cannot originate from channel 1 in the current frame. The contents output during channel 2 timeslot will have been clocked in the previous frame. A summary of the delays for different switching combinations is presented in Table 1.

In Data Memory Mode-2 (DM-2), data clocked into the device in the current frame will be clocked out in the next frame. DM-2 is primarily designed for applications where a group of channels is to be switched together and timeslot sequence integrity is to be maintained. To illustrate the advantages consider a case where input channels 1, 4, 5 and 8 are to be switched to output channels 3, 4, 5 and 6 respectively. In this case, if the switch is operating in single buffer mode, the throughput delay for input channels 4, 5 and 8 will be different than that for channel 1. If the SMX-1 is operated in Data Memory Mode-2 (double buffer mode), the throughput delay for all connections will be the same. Double buffering is achieved by dividing the internal memory into two equal 1024 channel blocks. In any specific frame, data is written to one block and read from the other. In the subsequent frame, data is read from the block which was written to in the previous frame (see Figure 5). The internal block select signal is synchronous with the frame pulse input to the data memory (SMX-1). Data clocked in any specific frame will always be clocked out in the next frame; irrespective of which input and output timeslot is being switched. Timeslot sequence integrity is therefore maintained for any switching combination. It is important to note, however, that alignment of the input and output frames will effect the throughput delay. In Figure 5 two data output frames are illustrated. If the first phase is used, then switching any input channel to channels 0 or 1 will result in greater than one frame delay. For example if channel 1022 is switched to channel 0, data clocked in frame n will be clocked out of the switch in frame n+2, not frame n+1 as would be expected. Note that in frame n+1 channels 0 and 1 are output from internal block 0 while all the other channels are output from block

1. Switching channel 1022 to any other channel will result in the data being clocked out in frame n+1. If the second frame alignment shown is selected, all channels will be double buffered in the same way. As shown in Figure 5, in frame n+1 channels 0 to 1023 will be sourced from block 1. Therefore, any channel input in frame n will be clocked out in frame n+1.

A summary of the throughput delay in Data Memory Mode-2 for different switching configurations is presented in Table 1.

The undesirable effect of double buffering each frame is that the delay through the switch can be as high as two frames (250 microseconds). In some voice switching applications this may not be acceptable. The SMX allows switching between DM-1 and DM-2 on a per timeslot basis. Consequently, a single switch matrix can be optimized both for voice and data switching.

3.1.3 Programming for Switching

The contents of the connection memory are clocked out onto the data bus and are latched into the address bus of the Data Memory. The address is used to specify the data memory location to be read during a particular output timeslot. The connection memory is programmed in a manner that permits specific addresses to be output in certain timeslots. Switching any input channel to an output channel timeslot is accomplished by merely writing the address of the input channel in the connection memory location corresponding to the output channel timeslot. For example, to switch input channel 5 to output channel 10, the connection memory location corresponding to channel 10 is loaded with the address for channel 5. As discussed in section 3.2, the state of the remaining bits, which are used to control other features, can be programmed at the same time (see also Figure 3 for the address/control function mapping). Writing binary XX11 0100 0000 0101 (where X = don't care) in the connection memory location corresponding to channel 10 will cause the output drivers to be enabled, select Data Memory mode-2 operation, disable messaging and switch channel 5 to channel 10. These features can be enabled or disabled on a per-timeslot basis.

3.2 Serial Crosspoint Switch Matrix

A 1024 channel serial time-space digital switch can be constructed using the parallel timeslot interchange circuit described previously (sec. 3.1) in conjunction with two MT9085 Parallel Access Circuits (PAC).

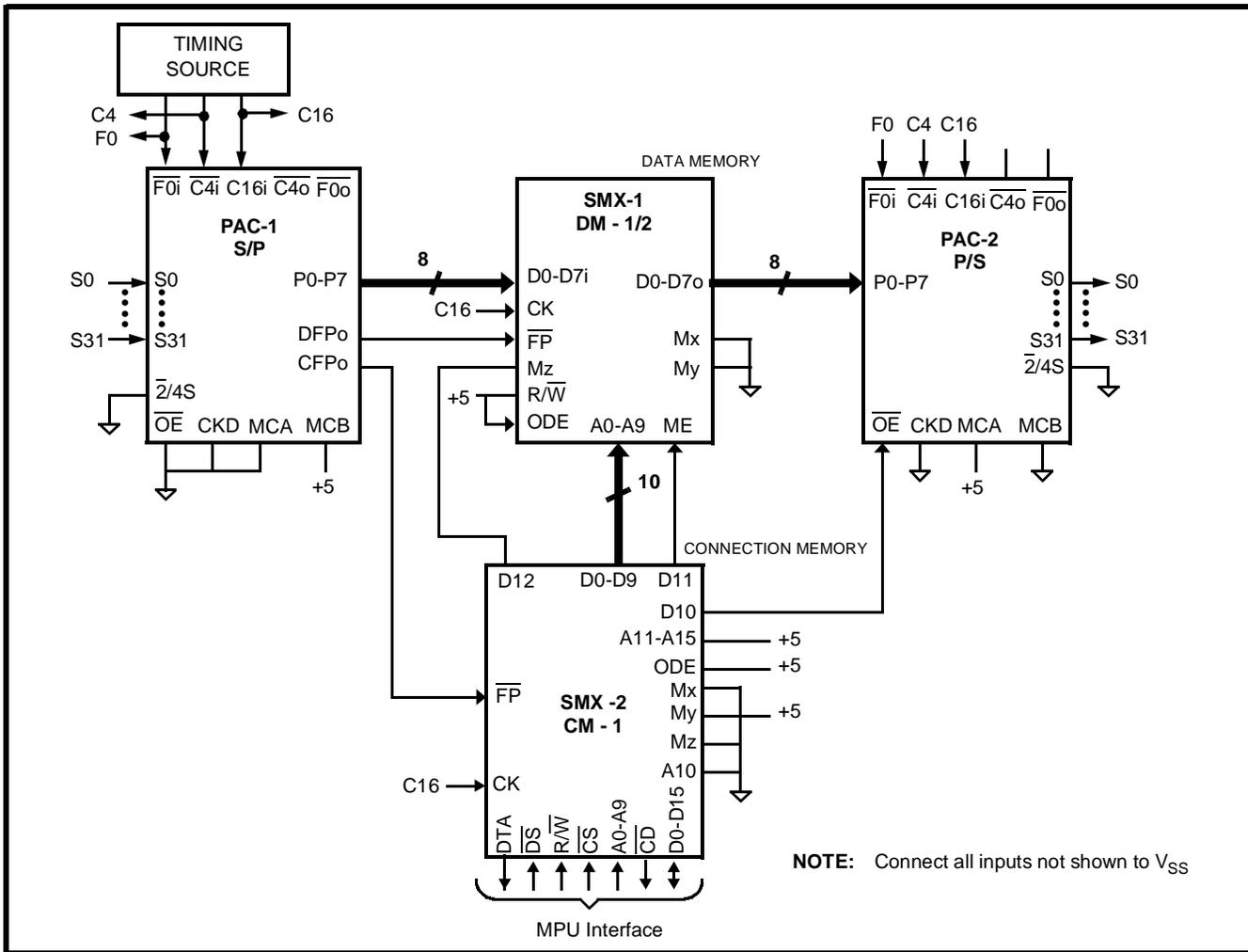


Figure 6 - 1024 Channel Switch Matrix

3.2.1 Circuit Description

Implementation of a 1024 channel time-space crosspoint switch requires two PACs. One PAC performs serial-to-parallel conversion; the second is used to perform parallel-to-serial conversion. The complete circuit is illustrated in Figure 6.

The main switching function is accomplished by the timeslot interchange circuit made up of two SMXs. The complete description for the SMX part of the circuit is presented in section 3.1.

PAC-1 is configured for serial-to-parallel conversion (MCA is tied low). Note that because the PAC has a 8 bit wide data bus, only eight of the sixteen data inputs on the SMX are used. The unused SMX data inputs should be tied high or low.

The MCB input on the PAC controls the state of the parallel bus drivers. When the PAC is used with the SMX in the 1024 channel configuration, MCB is tied high to enable output drivers for the full duration of

the parallel timeslot (two C16 clock periods). The CKD input affects the relative input and output timing on the PAC. When the CKD is tied high, all device timing is delayed by one C16 clock period with respect to the boundary established by the system frame pulse ($F0i$). The phase of the Connection Memory Frame pulse generated by the PAC is also affected by this input. For the 1024 channel configuration, CKD should be tied low.

The data rate on the serial inputs is selected to be 2.048 Mb/s by tying $\bar{2}/4S$ low. The data rate can be selected to be 4.096 Mb/s by tying $\bar{2}/4S$ high. If the data rate is selected to be 4.096 Mb/s, only the first 16 serial streams are utilized. The remaining serial inputs should be tied low.

PAC-2 is configured for parallel-to-serial conversion (MCA is tied high). Once again CKD is tied low in this device to make the PAC's input timing compatible with the SMX's output timing. The output drivers on the PAC are controlled via bit 10 in the connection memory. The serial output drivers can be disabled or

enabled on a per-channel basis by asserting the appropriate level on the OE pin.

In parallel-to-serial mode, the MCB pin determines whether a positive or negative clock edge latches data into the PAC. MCB is tied low for the 1K configuration to permit data to be clocked into the PAC with the last falling edge in the timeslot. Clocking data in with the last falling edge in the bit allows for more delay between the SMX output and PAC input.

The main timing source generates a 16.384 MHz clock phase-locked to a 4.096 MHz clock. In most system applications, the 4.096 MHz clock can be divided down from a 16.384 MHz master clock. In cases where only a 4.096 MHz clock is available, the C16 clock should be derived by phase locking to the 4.096 MHz signal.

The framing signal input to PAC-1 at \overline{FOi} should meet the requirements specified in the PAC data sheet to ensure correct alignment with C4. The frame pulse, C4 and C16 clocks input to PAC-2 are also supplied by the timing source. PAC-1 generates the Data Memory and Connect Memory frame pulses.

3.2.2 Timing Description - 1024 Channel PAC/ SMX Configuration

The SMX and PAC are synchronized by the Data Memory Frame Pulse (DFPo) and the Connect Memory Frame Pulse (CFPo) issued by the PAC.

3.2.2.1 Serial-to-Parallel Conversion Timing

The timing diagram shown in Figure 7 illustrates the PAC and SMX serial-to-parallel conversion timing. The serial bus frame boundary is established by the \overline{FOi} signal supplied to PAC-1. The first serial channel that is clocked into the PAC is channel 0. The data on the parallel bus corresponding to this channel will be output after channel 0 has been clocked in (which occurs 64 C16 clock cycles after the serial bus frame boundary). The first timeslot on the parallel bus carries data from channel 0, stream 0 (C_0S_0); the next timeslot carries data from channel 0, stream 1 (C_0S_1) and so on. Timeslot 0 output on the parallel PAC bus is clocked into SMX-1 and stored in memory location 0. This alignment is ensured by providing a Data Memory Frame Pulse exactly 64 - C16 clock cycles after the frame boundary. The data memory counter is reset with the next positive clock edge. The data output by the PAC on the parallel bus corresponding to channel 0, Stream 0 is latched into the SMX with this same clock edge (marked TS0 on the timing diagram). It is stored in the memory

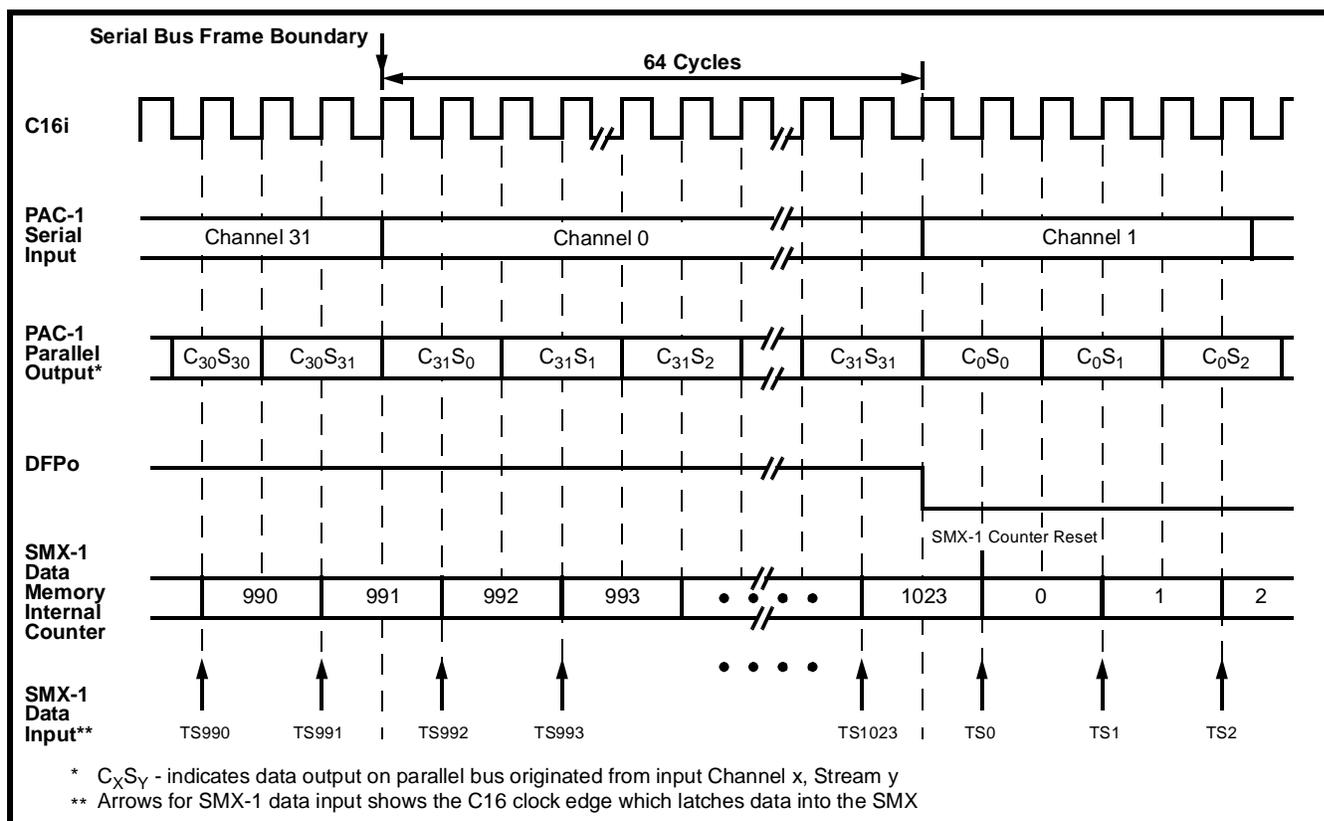


Figure 7 - SMX/PAC 1024 Channel Configuration - Serial-to-Parallel Conversion Timing

location addressed by the internal counter with the next positive clock edge.

3.2.2.2 Parallel-to-Serial Conversion Timing

Data is clocked out of the Data Memory (SMX-1) according to the addresses asserted on its address bus. The connection memory is synchronized with the PAC's serial input/output timing with the Connect Memory Frame Pulse issued by PAC-1. This frame pulse goes low exactly 71 clock cycles before the serial frame boundary. The rationale behind this specific timing becomes clear when the timing constraints for parallel-to-serial conversion are considered. As mentioned earlier, there are 32 serial output streams on the PAC. Channel 0 of each stream is aligned with respect to the frame boundary. Consequently, data corresponding to channel 0 for all 32 serial streams must be latched into the parallel bus of the PAC before the beginning of channel 0 on the serial side. This requires 32 timeslots each occupying two C16 clock cycles to be clocked out of the SMX before channel 0 is clocked out by the PAC on the serial bus. To simplify programming the switch, it is desirable to have data destined for channel 0 on stream 0 stored in SMX memory

location corresponding to parallel timeslot 0. With these constraints in place, and, the requirements imposed by the SMX data and connection memory timing, it is necessary to have the Connection Memory internal counters reset exactly 70 - C16 clock cycles before the frame boundary (see Fig. 8 for specific details). By having the CFPo go low 71 clock cycles before the frame boundary, all of these constraints can be met.

3.2.3 Throughput Delay Considerations

The 1024 channel SMX/PAC configuration described in section 3.2.2 provides for selectable double or single buffering.

When the SMX is operated in Data Memory Mode-1 (DM-1), the switch does not double buffer any of the channels. Data clocked into the device in one frame may be clocked out in the same frame or in the next frame, depending on the difference between the input and output channels on the serial streams. A summary of the delays is presented in Table 2.

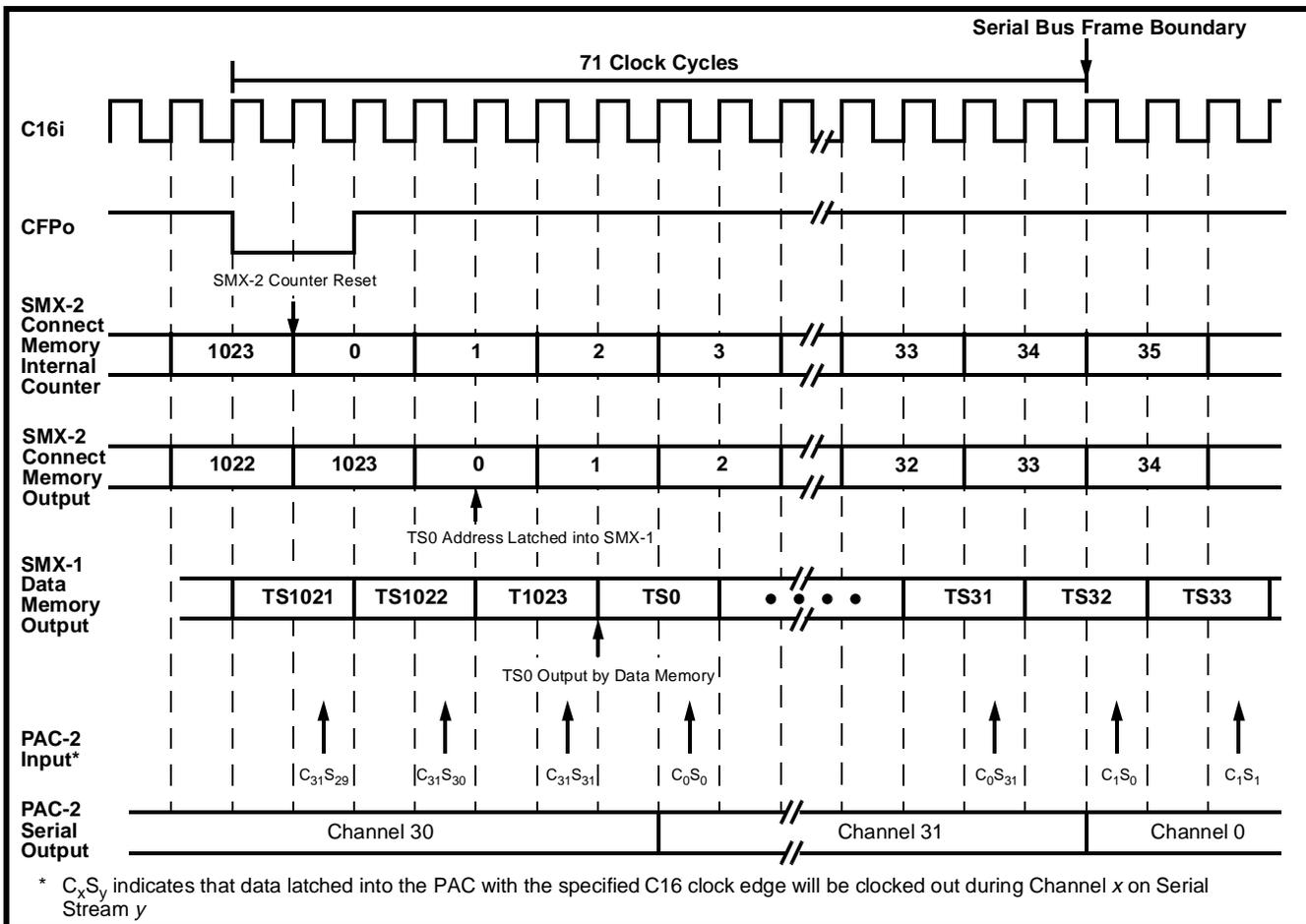


Figure 8 - SMX/PAC Parallel-to-Serial Conversion Timing

Single Buffered Mode			Double Buffered Mode		
Input Channel	Output Channel	Throughput Delay	Input Channel	Output Channel	Throughput Delay
N	N	1 Fr.	N	N + M	1 Fr. + M Ch
N	N + 1	1 Fr. + 1 Ch.	N	N - M	1 Fr. - M Ch
N	N + 2	See Note**	N	0	2 Fr. - N
N	N + M	M Ch.	N	1	2 Fr. - (1 + N) Ch.
N	N - k	1 Fr. - k Ch.	N	2	2 Fr. - (2 + N) Ch.*

N = 0, 1, 2 ...31

M = 3, 4, 5 ...31

N + M ≤ 31

K is any integer less than N

** The delay is determined by the input/output stream combination as shown in Table 3.

N = 2, 3, 4, ...31

M = 0, 1, 2 ...31

N + M ≤ 31

N + M ≥ 0

* Applies only to output 0

Table 2. Throughput Delay for 1024 Channel SMX/PAC Configuration

Data will be clocked out in the next frame if the difference between the input channel and output channels is less than two, i.e., if the data is input to the switch in frame n, it will be clocked out in frame n+1. For example, if serial channel 1 is switched to output channel 1 or 2, data clocked in the current frame will be clocked out of the switch in the next frame during the channel 1 or 2 timeslot. When the difference between the input and output channels is greater than two channels, the data is always clocked out in the same frame. If, for example, channel 2 is switched to output channel 5, data

clocked into the device in frame n will be output in frame n.

On the other hand, if the difference between the input and output is exactly two channels, the output data may be clocked out in the same frame or the next depending on which input and output stream the two channels are located. Table 3 is a summary of input/output stream combinations which will result in minimum throughput delay. Note that if the output stream number is at least two times higher than the input stream number, the throughput delay will be

Input Stream	Output Stream																														
0	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
1	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
2	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
3	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31				
4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31					
5	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31						
6	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31							
7	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31								
8	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
9	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31										
10	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31											
11	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31												
12	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31													
13	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31														
14	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31															
15	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31																
16	18	19	20	21	22	23	24	25	26	27	28	29	30	31																	
17	19	20	21	22	23	24	25	26	27	28	29	30	31																		
18	20	21	22	23	24	25	26	27	28	29	30	31																			
19	21	22	23	24	25	26	27	28	29	30	31																				
20	22	23	24	25	26	27	28	29	30	31																					
21	23	24	25	26	27	28	29	30	31																						
22	24	25	26	27	28	29	30	31																							
23	25	26	27	28	29	30	31																								
24	26	27	28	29	30	31																									
25	27	28	29	30	31																										
26	28	29	30	31																											
27	29	30	31																												
28	30	31																													
29	31																														

Table 3. Input/Output Stream Combinations which will result in less than one Frame Delay when Δ =2 Ch.

less than one frame. The use of the table can be best illustrated with a specific example. Consider the case where channel 0 is to be switched to channel 2. If the input channel is located on stream 0 and the output channel is located on stream 1 data clocked in frame n will be clocked out in the next frame (n+1). However, if the output channel was located on stream 2, then the contents of the channel would be clocked out in the same frame (n).

For most voice switching applications this differential delay is not of any significance. In data switching applications where concatenated channels are being transported through the switch, the variable delay can pose some problems. To illustrate, consider the case where concatenated channels 3, 4, and 5 are to be switched to output channels 4, 5, and 8. Contents of input channels 3 and 4 will be output in the next frame while the contents of input channel 5 will be clocked out in the current frame. If the channels were carrying packetized information, the sequence of bits in the packet would be altered thereby destroying the packet.

In Data Memory Mode-2 all channels are double buffered. Except where channels 0, 1 and 2 (only on stream 0) are involved, data clocked in a specific frame will always be clocked out in the next frame (see Table 2). If the concatenated channel example discussed above is considered in this mode, all channels switched through the device will be output in the next frame. The bit sequence in the packet would be preserved.

The only exception to the rule described above is seen when output channels 0, 1 and 2 (on stream 0 only) make up the group of concatenated channels (see boxed area for an explanation). Input data channels switched to channels 0 or 1 in frame n will be output in frame n+2. For example, if the circuit is programmed to switch any input channel to output channel 0, data clocked into the switch in frame n will be clocked out in the frame after next (i.e., frame n+2). In contrast, when any input channel is switched

to output channel 3, the data will be output in the next frame (i.e., n+1). If channels 0 and 1 are used as part of a concatenated hyper-channel and all channels are operated in double buffered mode (DM-2), timeslot integrity will not be maintained. However, because the SMX/PAC switch in the 1K configuration is capable of selectively double buffering specific channels while single buffering others, timeslot sequence integrity can be ensured for all switching configurations if the device is programmed as follows:

- Operate output channels 0 and 1 (on all streams) and channel 2 (on stream 0) in single buffer mode (DM-1)
- Operate all other channels in double buffer mode (DM-2)

3.2.4 Programming the 1024 Channel Serial Switch

The principles involved in switching any incoming serial channel to a serial output channel timeslot are identical to those presented in the parallel switching section. The address of the source channel is stored in the connection memory location corresponding to the destination channel. Since the actual switching function is accomplished in parallel by the SMX, it is necessary to determine the parallel timeslot addresses corresponding to the serial channels. The mapping of the PAC serial channels onto SMX parallel timeslots can be accomplished by directly coding the serial channel and stream number in binary as shown in Figure 9. The SMX timeslot corresponding to a specific serial channel is also given by the following simple algebraic expression:

$$T = (C * 32) + S$$

where

- T is the SMX timeslot
- C is the serial channel number (0,1, 2,.....31)
- S is the serial stream number (0, 1, 2,.....31)

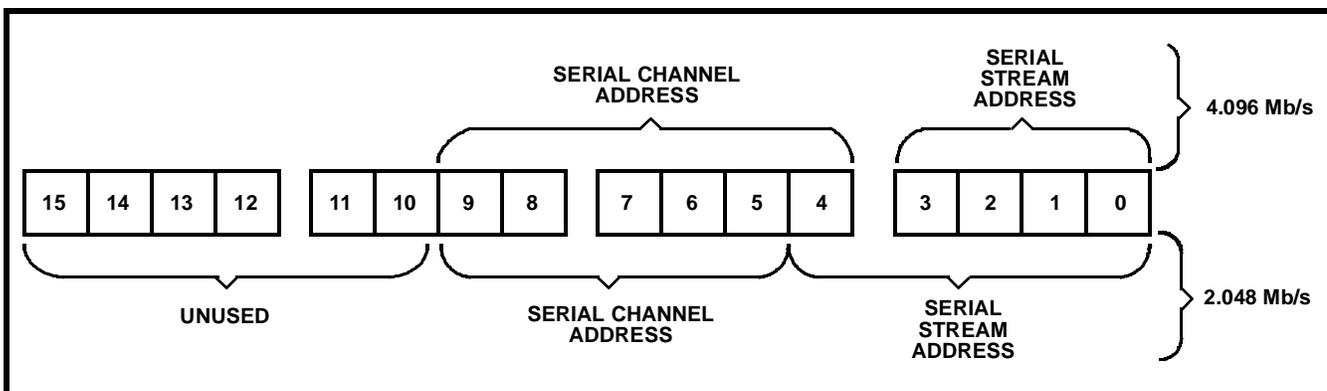


Figure 9 - SMX Address Corresponding to Serial Stream and Channel Numbers

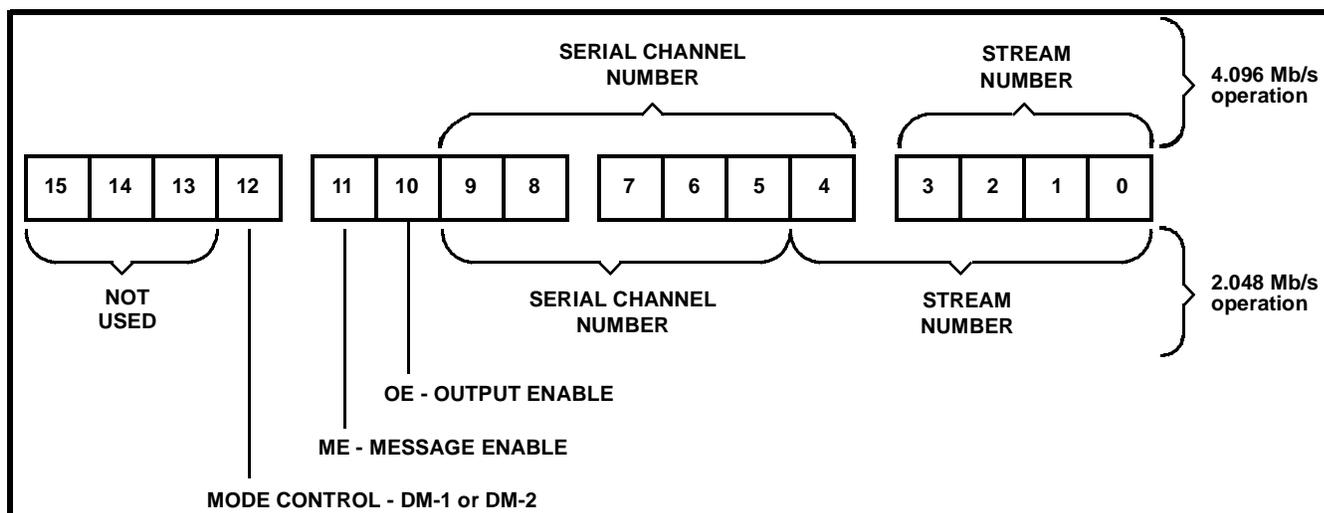


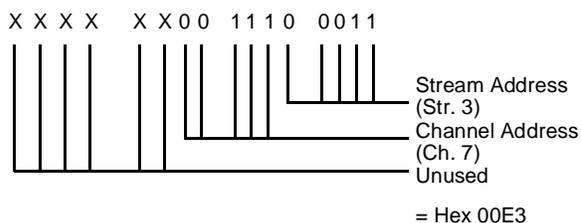
Fig. 10 - Mapping of Data Memory Address and PAC Control Functions on Connection Memory Data Bits

When switching a specific input channel to an output channel, the SMX timeslot address corresponding to the serial channel is stored in the connection memory location corresponding to the output channel. The other control bits (OE and ME) are also stored along with the address of the source channel. The mapping of the control functions for the circuit described above is shown in Figure 10.

To illustrate the basic programming principles consider the example where channel 4 on stream 5 is switched to channel 7 on stream 3. The example discussed below assumes that the PACs are configured for 2.048 Mb/s operation. The circuit is programmed using the following steps:

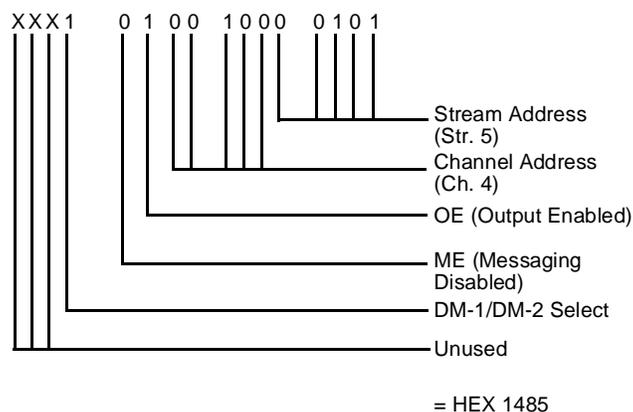
1. Determine the SMX parallel timeslot address corresponding to the output channel.

The SMX memory corresponding to the output channel, Ch. 7, Str. 3 in binary is shown below:



2. Store the address of the input channel along with the state of the three control bits in the output channel timeslot.

The SMX address corresponding to the input channel timeslot and the position of the control bits is decoded as follows:



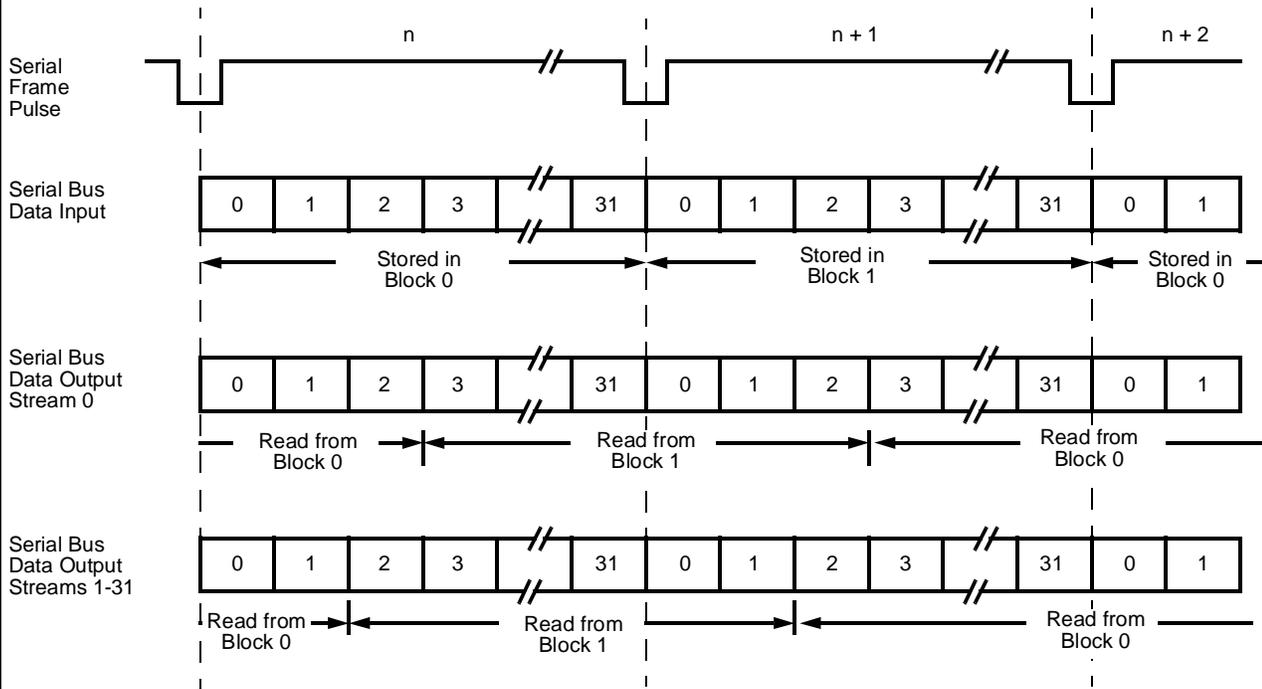
Storing Hex 1485 in Connection Memory location Hex 00E3 will switch channel 4, stream 5 to channel 7, stream 3. It will also put the device in Data Memory mode 2, disable the messaging feature and enable output drivers.

When the PAC is operated in the 4.096 MHz mode, only 16 of the 32 serial streams are used. Each stream carries 64 channels. Translating the serial channel and stream number to binary is accomplished by specifying the stream address with the first four bits in the word. The next six bits are used to specify channel address. Decimal conversion of the channel addresses is given directly by the following algebraic relationship:

$$T = (C * 16) + S$$

where

- T is the SMX timeslot
- C is the serial channel number (0,1, 2,.....63)
- S is the serial stream number (0, 1, 2,.....15)



Throughput Delay In Serial Bus Applications

The throughput delay in the SMX/PAC serial switch, when the SMX is configured for double buffer mode operation, is affected by the choice of the output channel timeslot. In the double buffered mode, data clocked into the SMX/PAC on the serial bus in any specific frame will be stored in block-0 or block-1. All 32 channels in the frame will be stored in the same block. However, all channels clocked out on the serial bus do not originate from the same block of memory. As shown above, on stream 0, channels 0, 1 and 2 in frame n originate from block 0, while all the other channels in the frame originate from block 1. Similarly, in frame n+1, channels 0, 1, and 2 originate from block 1, while all the other channels are sourced from block 0. If data from any input channel is switched to channel 0, 1 or 2 (on stream 0), it will be clocked out two frames later. For example, if channel 3 is switched to channel 0, data clocked into the PAC in frame n will be clocked out in frame n+2. If the same channel is switched to timeslot 4 (or for that matter any timeslot other than 0, 1 or 2), the data will be clocked out in Frame n+1. Note that by operating channels 0, 1 or 2 in single buffer mode, the extra frame delay can be eliminated.

Note that channel 2 on streams other than stream 0, is not affected by the extra frame delay experienced by channel 2 on stream 0. Therefore, switching any input channel to channel 2 on streams 1 to 31 will result in data being clocked out in the next frame.

The specific block select alignment results because the input and output serial frames have to be aligned.

In the 2048 channel configuration, the data on the serial bus is stored in the two SMXs alternatively. The two SMXs act as separate blocks of memory. The alignment of the serial channels with the blocks of memory is the same as described above. The 2048 channel switch always double buffers all channels. It is not possible to selectively disable double buffering on a per-channel basis.

4.0 Design of a 2048 Channel Switch

The 2048 channel parallel switch is one of the main building blocks used in construction of larger switch matrices. The switch is constructed using three SMXs. Interface to serial time division multiplexed busses is possible using PACs.

4.1 Parallel Timeslot Interchange Circuit

Implementation of a 2048 channel parallel timeslot interchange circuit requires three SMXs. Two SMXs operating alternatively in Counter and External modes make up the data memory. The third is used as the connection memory and is operated in Connect Memory Mode-2. The circuit shown in Figure 11 illustrates the interconnections between the three devices.

two Data Memory SMXs is operated in Counter mode while the other is operated in External mode. In the subsequent frame, the device operating in Counter mode will be reconfigured to operate in External mode. The device operating in Counter mode accepts data on its input parallel bus at the clock rate. This data is stored in memory locations addressed by the internal 11 bit counter. The second device, which is configured to operate in External Mode, clocks out data onto its parallel output bus according to the levels asserted on A0-A10 by the connection memory. Consequently, data is written into the first SMX in one frame and read from it in the next resulting - effectively double buffering the data.

4.1.1 Circuit Operation

A circuit diagram showing the interconnections between SMXs is shown in Figure 11.

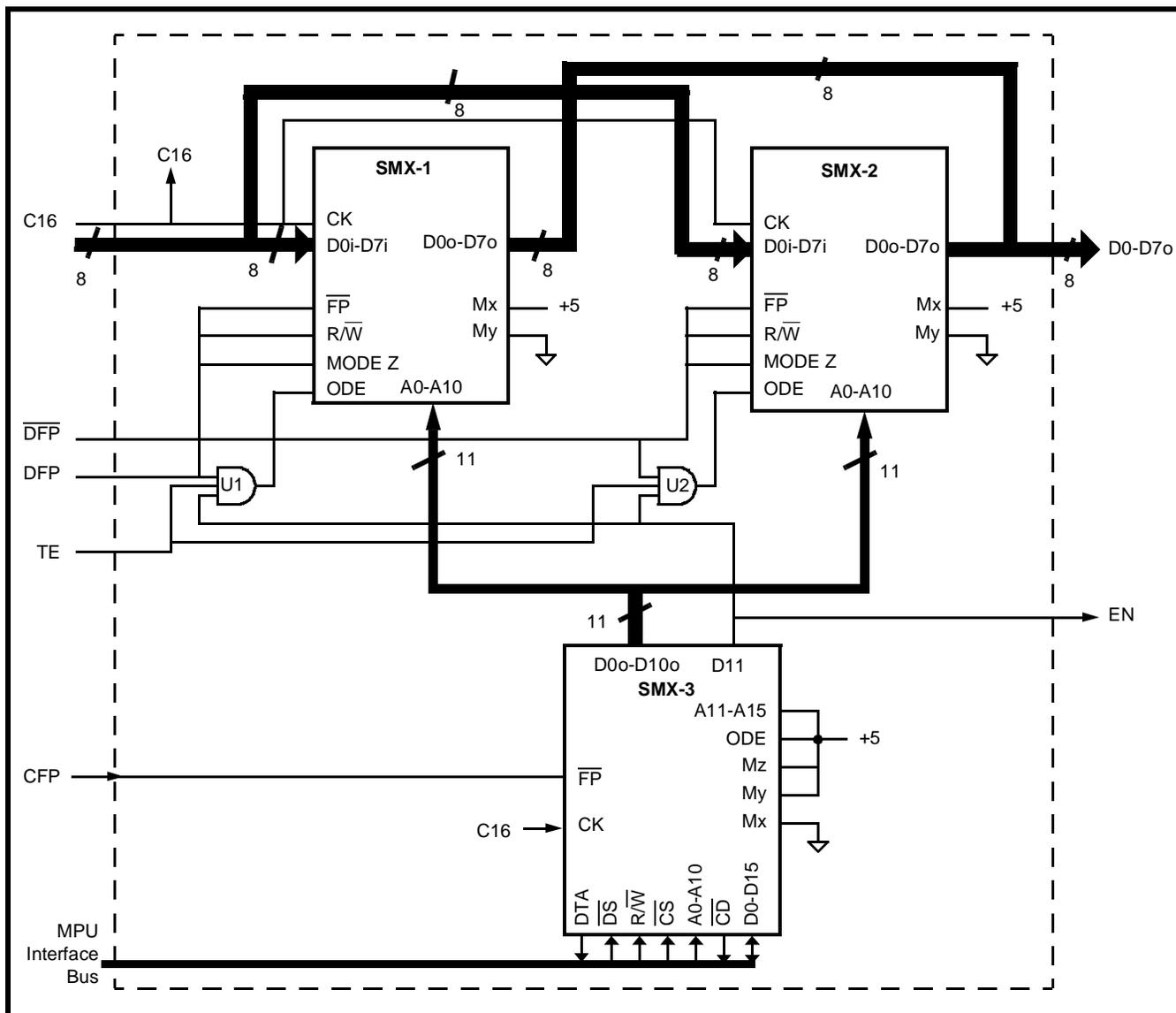


Figure 11 - 2048 Parallel Switch Block (PSB)

Timing for the three SMXs making up the 2048 channel switch is derived from a single 16.384 MHz clock. The DFP signal, sourced by an external timing generator block, functions as the Data Memory frame pulse and also as a mode select for SMX-1. It is also used to assert the proper level on R/W and the Output Drive Enable (ODE) inputs of the same device. The complementary signal $\overline{\text{DFP}}$ is used to control the corresponding inputs in SMX-2. DFP and $\overline{\text{DFP}}$ change state once per frame. By asserting the proper level on the Mz input, one of the two SMXs is operated in External mode while the other is operated in Counter mode. In the subsequent frame the mode of operation of the two devices will interchange. The level asserted on R/W and ODE will ensure that the device operating in Counter mode has its write enabled and its output drivers disabled. The SMX operating in External mode will have its output drivers and read function enabled (both R/W and ODE are high).

In Counter mode, with the write enabled, input data is clocked into the SMX and stored in sequential memory locations addressed by the internal 11 bit counter. The counter is reset with the rising edge of CK after DFP goes low. It is also reset after counting up to 2047. In External mode, with read enabled, data is clocked out of the device according to the addresses asserted on the Address bus (A0 - A11). These addresses are provided by SMX-3 which operates in Connect Memory mode (CM-2). The SMX in CM-2 mode is capable of generating 2048 addresses. The connection memory timing is synchronized with the data memory timing using the Connection Memory Frame pulse (CFP) sourced by the external timing generator. The phase difference between CFP and DFP determines the offset between the input and output frames. The offset selected affects the delay through the switch. SMX-3 is the only device which is directly accessed by a processor.

The parallel input busses of SMX-1 and SMX-2 are interconnected. However, due to the level asserted on the R/W pin only one device is configured to clock data in. The parallel output busses of the two devices are also interconnected. Only one of the devices will have its output drivers enabled. The AND gates U1 and U2 allow ODE to be disabled on a per-timeslot basis via D11 of the Connection Memory and also via an external Timed Enable (TE) control input. In applications where more than one 2K block is to be interconnected, the TE control input can be used to disable the output drivers on power up.

4.1.2 Timing Description

The following is the description of the timing signals for the 2048 switch configuration described above. The relative phase difference between the data memory frame pulse and the connection memory frame pulse determines the alignment of the input and output channel timeslots. The alignment desired depends on system level requirements of the user. An example of phase relationship between the Connect Memory frame pulse and the Data Memory frame pulse is shown in Figure 12. Note that the timing described is an example only. Depending on specific application requirements, other phase relationships between the Connect Memory and Data Memory frame pulse may be used.

The input channel timing is controlled by the signal applied at the frame pulse input of the data memory. As mentioned earlier, one of the SMXs which makes up the data memory is operated in counter mode to allow data to be clocked into the device. A low going signal (DFP) applied at the $\overline{\text{FP}}$ input resets the internal counter of the device. Data clocked into the device at this time will be stored in memory location addressed as zero.

The output channel timing depends on the frame pulse input to the connection memory. The internal counter of the connection memory is reset with the first rising edge of the CK clock after $\overline{\text{FP}}$ goes low. The connection memory will clock out an address from an internal memory location corresponding to channel zero after the counter has been reset. This data will be clocked into the address bus of the data memory SMX operating in External mode. Subsequently, data from the addressed location in the data memory will be clocked out by the SMX in the next timeslot.

Note that although, the level on the R/W pin is latched into the device with the first rising edge after the signal changes state, the actual change in operation is not implemented until the beginning of the next timeslot. Consequently, in the timing example illustrated in Figure 12, output channel 2047 is sourced from SMX-1 while channel 0 is clocked out of SMX-2. On the input side channel 0 is stored in SMX-1

4.1.3 Throughput Delay Considerations

In the example input/output phase relationship described above, all channels are double buffered. Any output channel in any specific frame will always be sourced from the previous frame. For example, if channel 2047 is switched to output channel 0, the

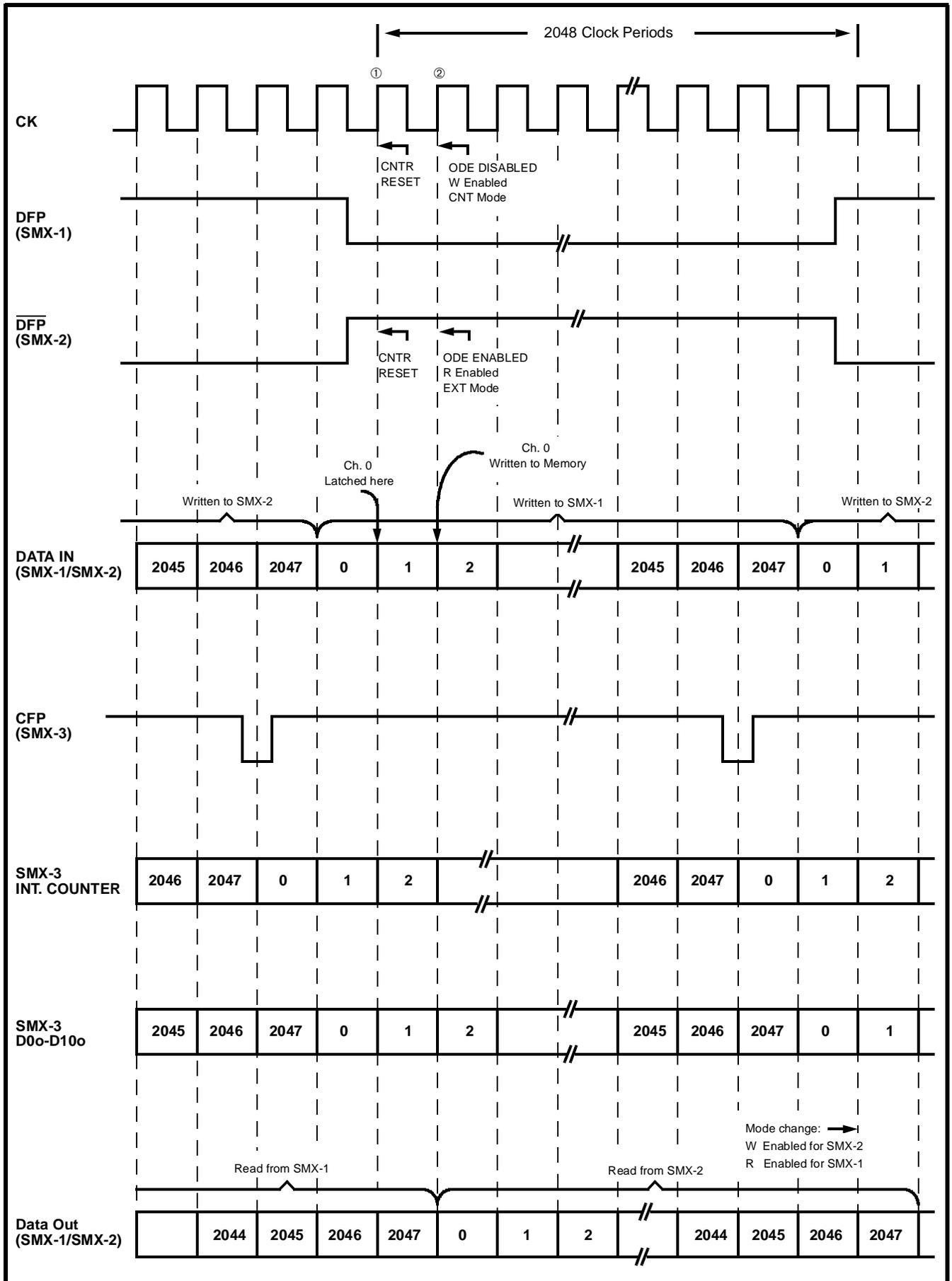


Figure 12 - 2048 Parallel Channel Switch Timing - Non-aligned Input/Output Frames

data input in channel 2047 during frame "n" will be clocked out in frame "n+1".

If the phase relationship between the data memory and connect memory frame pulses is such that the input and output data frames are aligned, the throughput delay when switching channel 2047 to channel 0 will be greater than the delay for any other configuration. In this case it is very important that the correct level is asserted the on R/W, mode select (Mz) and ODE signal to ensure that the correct memory block is enabled for input and output.

4.1.4 Programming For Switching

Programming the 2K switch is very similar to programming the 1K switch described earlier. The address of the source channel is stored in the

connection memory location corresponding to the destination channel. As discussed in the 1K mode description, the state of other control pins can be set or reset at this time using spare data bits from the connection memory. The controlled features on the SMX can be enabled or disabled on a per-timeslot basis. In the example configuration discussed above, the output drive enable is controlled by the unused data bit - D11. Message Enable is controlled by D12. Recall that when the ME pin of the SMX is pulled high, data clocked in on the address bus is output directly onto the data bus of the device. This feature can be enabled on a per timeslot basis. Selected individual channels can be placed in message mode while the others are kept in switch mode.

On initial power up it is advisable to reset all connection memory contents by writing hex 0000 in

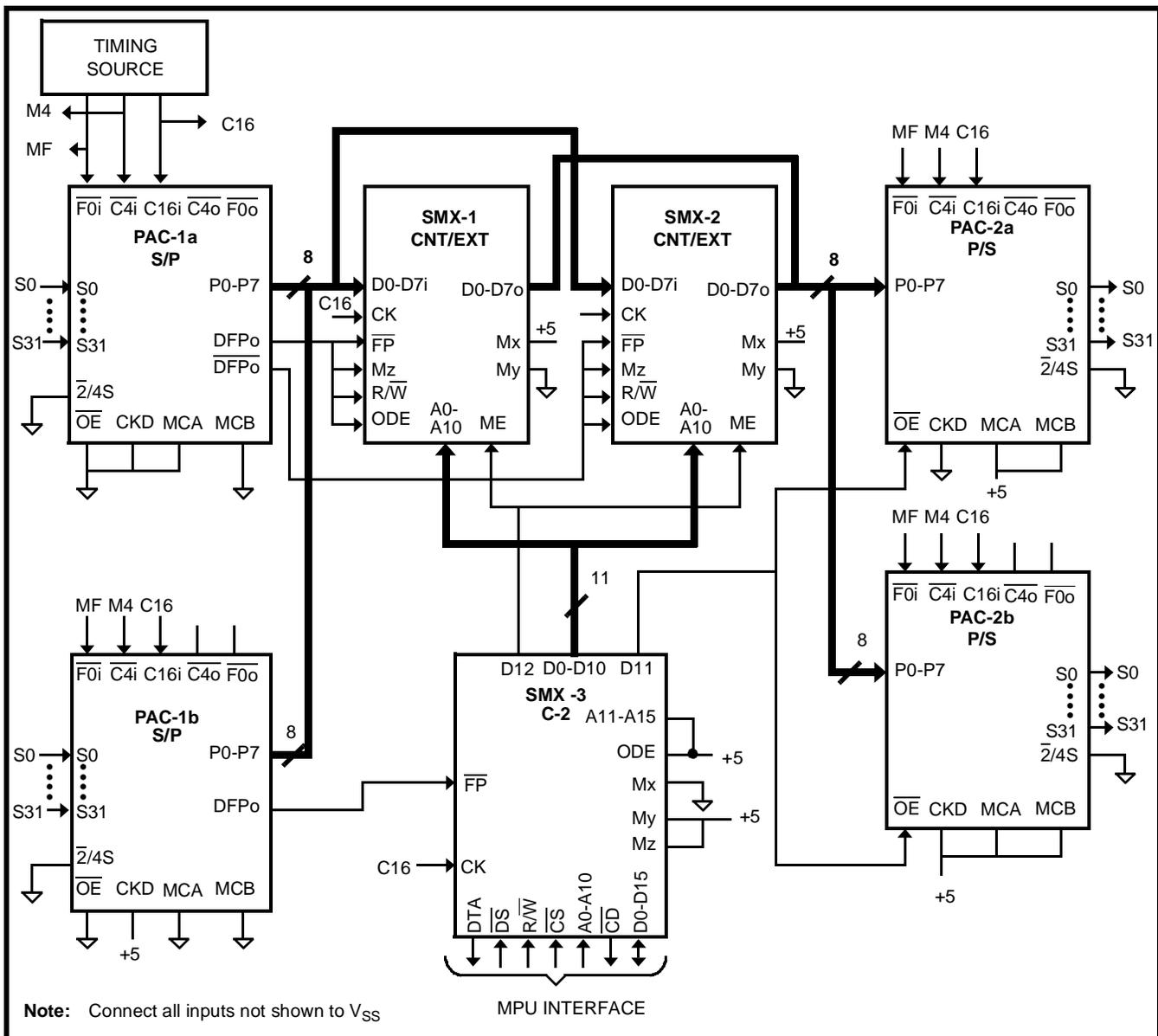


Figure 13 - 2048 Channel Switch Matrix Using the PAC and SMX

all locations. This will ensure that the output drivers are disabled. Subsequently, as the connections are made, the output drivers can be selectively enabled.

4.2 Serial Interface to SMX

The SMX can be interfaced to a 2.048 or 4.096 Mb/s serial time division multiplexed bus with the MT9085 (PAC). A total of four devices are required for a complete interface. Two devices perform serial to parallel conversion while the other two are configured for parallel-to-serial conversion.

4.2.1 Circuit Description

Figure 13 shows how the MT9085s and the parallel timeslot interchange switch (SMXs 1, 2 and 3) are interconnected.

Serial to parallel conversion is performed by PACs 1a and 1b. The MCA pin is tied low to configure the devices for serial to parallel conversion. The parallel bus of the two PACs both drive the input SMX bus. Bus contention is prevented by having only one device drive the bus at anytime. When MCB is tied low in the PAC, the parallel bus on the device will be actively driven for one parallel channel timeslot (i.e., one C16 clock period). The CKD pin in one of the two PACs is tied high while it is tied low in the other. This will offset the timing of the two PACs by one C16 clock period, thus ensuring that only one of the two PACs drives the SMX data bus during a specific timeslot.

Note that only 8 of the 16 input data lines on the SMX are connected to both the PACs. The other 8 inputs on the SMX bus can be tied low if they are not being used for anything.

The main timing source generates a 16.384 MHz clock phase locked to a 4.096 MHz clock. The system framing signal input at $\overline{F0i}$ must meet the requirements specified in the PAC data sheet to ensure correct bit alignment on the serial interface. The C4, C16 and $\overline{F0i}$ inputs to all other PACs in the system should be provided directly from the master timing source.

PAC's 1a and 1b generate all framing signals for the data memory and the connection memory. PAC-1a generates the frame pulse for the data memory SMXs (SMX-1 and SMX-2) which are configured to operate in Counter mode and External mode. The same signal is used to control the state of the Mz, R/W, and ODE pins. PAC-1b sources the Connect Memory Frame pulse for SMX-3 which serves as the connection memory.

The data rate on the serial input streams can be selected to be 2.048 Mb/s or 4.096 Mb/s by asserting the appropriate level on the $\overline{2/4S}$ pin on the PAC.

The parallel-to-serial conversion is performed with two PACs. In Figure 13, PAC's 2a and 2b are configured for parallel-to-serial conversion (MCA is tied high). Data is output by the SMX and clocked into one PAC or the other in alternative timeslots. Note that the CKD pin of one of the PACs is tied high while it is tied low in the other. As mentioned earlier, this results in the internal timing of the two PACs being off-set by one clock period. Consecutive channels output by the SMX data memory are latched into PAC-2a and PAC-2b alternatively. The MCB pin is tied high for both devices. The MCB pin controls the clock edge which latches data into the device on the parallel bus. Tying MCB high programs the PAC to clock in data on its parallel input bus with rising clock edge. This ensures that the PAC's interface timing is compatible with the SMX timing.

The serial output drivers can be disabled or enabled by asserting the proper level on the OE pin of the PACs. In the example circuit illustration, the D11 output on the connection memory (SMX-3) is used to control the state of the \overline{OE} pin. The output drivers on the serial bus can be selectively enabled or disabled during any specific channel timeslot by merely writing to the connection memory location corresponding to the serial channel. Examples are provided in Sec. 4.2.4.

4.2.2 PAC/SMX Timing Description

The input and output timing for the PAC interface with the SMX is shown in Figure 14.

4.2.2.1 Serial-to-Parallel Conversion

The frame boundary for the serial time division multiplexed streams is defined by the $\overline{F0i}$ signal. Each channel on the serial bus is made up of 8 bits with a data rate of 2.048 or 4.096 Mb/s. Data is clocked into the serial interface on the PAC three quarters of the way down in a bit cell. Data on the parallel bus of the PAC will be clocked out after all 8 bits have been clocked into the device; 64 C16 clock cycles after the serial frame boundary. The delay is necessary to clock in all 8 bits of the channel on the serial bus before data is clocked out on the parallel bus.

Note that because MCB is tied low, the data on the parallel bus is clocked out with the falling edge of the C16 clock. The second PAC has its timing offset by one C16 clock period. It will output data onto the

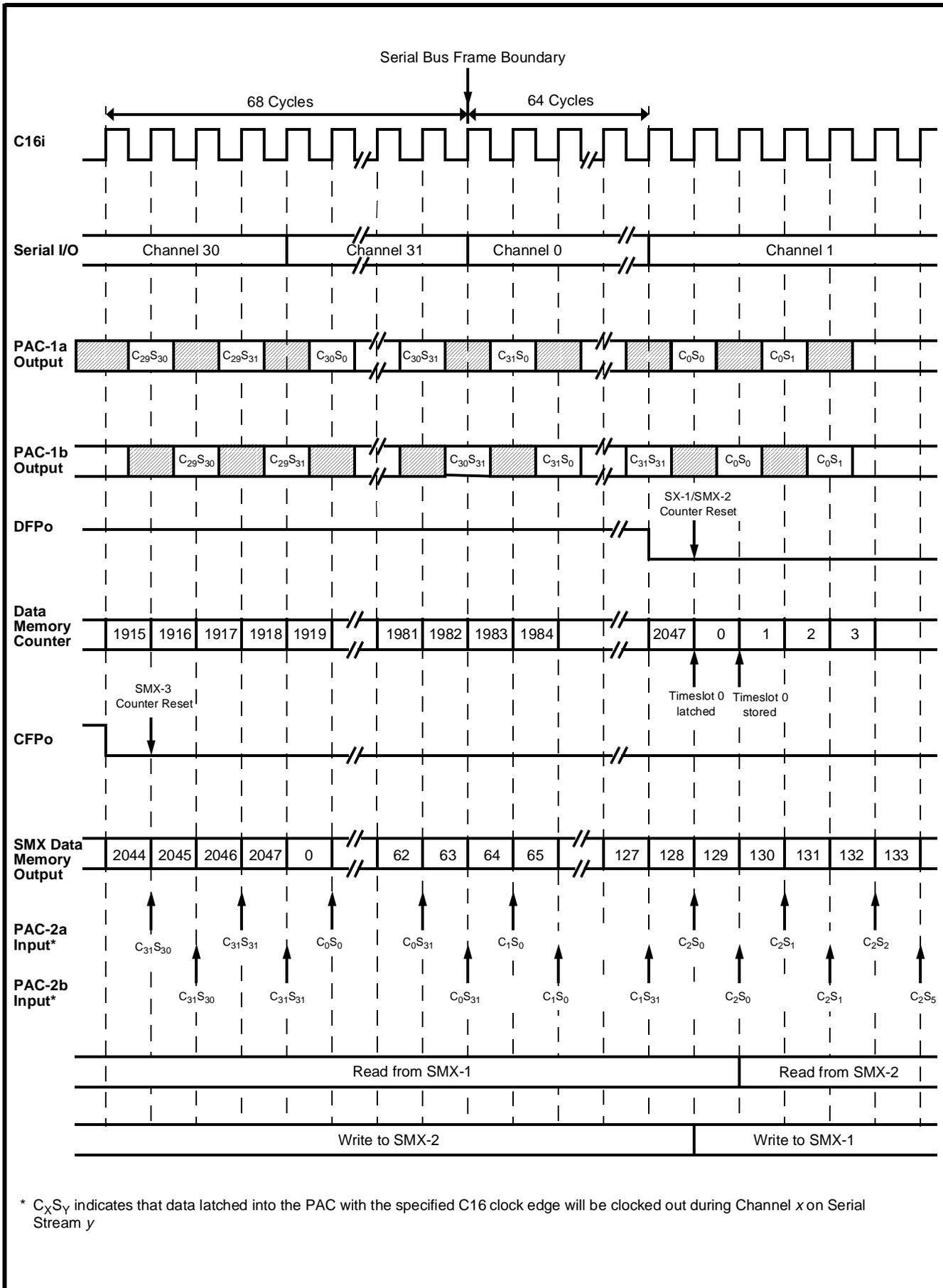


Figure 14 - SMX/PAC Interface Timing - 2048 Channel Configuration

parallel bus with the next falling edge of C16. The first channel output by PAC-1a corresponds to serial channel 0 originating from stream 0 (abbreviated as C₀S₀). The first channel output by PAC-1b is sourced from channel 0, Stream 0 located on PAC-1b.

The DFPO and \overline{DFPO} signals generated by PAC-1a are used by the SMX-1 and SMX-2 as frame pulses. DFPO and \overline{DFPO} change state 64 C16 clock cycles from the serial frame boundary - synchronous with the end of serial channel 0. The internal counters of the SMX-1 or SMX-2 will be reset with the next C16 clock edge when DFPO goes low as indicated in Figure 14. The SMX counters will also be reset on reaching terminal count (2047).

Channel 0 data clocked out by PAC-1a will be latched into the SMX, operating in Counter mode, with the first rising edge of C16 and stored in memory location corresponding to timeslot 0 with the next rising edge. Channel 0 data output by PAC-1b will be clocked into the SMX and stored in timeslot 1. Similarly, the next parallel channel clocked out by PAC-1b will be stored in SMX memory location corresponding to timeslot 2.

As mentioned earlier, input data is stored alternatively in SMX-1 and SMX-2 in consecutive frames. The timing relationship between the input channel number and the SMX accessed is shown at the bottom of Figure 14. Note that in any specific frame, channels 0 to 2047 are all written into the same SMX. This also implies that in any specific frame all serial channels on both PACs are stored in one or the other SMX.

4.2.2.2 Parallel-to-Serial Conversion

Data is clocked out on the parallel bus by the data memory SMX (SMX-1 or SMX-2) according to the addresses asserted by the connection memory during a specific channel timeslot. The Connect Memory Frame pulse (CFPO) is used to synchronize the connection memory timing with the data memory and the output PAC timing. CFPO is a 4 kHz signal which changes state 68 clock cycles before the serial frame boundary. The internal counter in SMX-3 is reset with the first rising clock edge after CFPO goes low and subsequently on reaching terminal count.

The rationale behind the specific phase relationship between the system frame boundary (F0i) and the Connect Memory frame pulse (CFPO) is best understood if the path followed by a timeslot output by the SMX is traced. The connection memory counter is reset with the first C16 clock edge after

CFPO goes low. The contents of connection memory addressed by this counter will be clocked out in the next timeslot and placed on the data bus. Subsequently, this data will be clocked into SMX-1 or SMX-2 (which ever is operating in External mode) address bus. The contents of the addressed data memory location will be clocked out of SMX-1 or SMX-2 in the next timeslot and clocked into PAC-2a. The MCB pin is tied high. Data is latched into the PAC with the rising C16 clock edge. This data will be output on Channel 0 on serial stream 0 (S0) in PAC-2a. The data output during the next parallel timeslot corresponds to channel 0 on serial stream 0 in PAC-2b. Note that since, PAC-2b has its CKD pin tied low, its timing is delayed by one C16 clock period. Consecutive data timeslots output by the SMX are clocked into PAC-2a and PAC-2b alternatively. The relationship between the parallel timeslots and the serial channel timeslots is illustrated in Table 4. Before PAC-2a or PAC-2b clocks data out channel 0 on the serial bus, parallel data corresponding to all channel 0s on the serial bus has to be clocked in. This requires 64 parallel timeslots to be clocked out of the SMX before the PAC outputs channel 0 on the serial bus. Allowing for the delay in clocking out the address from the connection memory, and subsequent latching of the address into the data memory, the connection memory frame pulse must occur 68 cycles before the serial bus frame pulse.

Parallel Timeslot	Serial Channel	Serial Stream	PAC
0	0	0	2a
1	0	0	2b
2	0	1	2a
3	0	1	2b
4	0	2	2a
5	0	2	2b
•	•	•	•
•	•	•	•
•	•	•	•
62	0	31	2a
63	0	31	2b
64	1	0	2a
65	1	0	2b
•	•	•	•
•	•	•	•
•	•	•	•
2047	31	31	2b

Table 4. Relationship between PAC-Serial Bus Channels and SMX Timeslots (2048 Mb/s Mode)

4.2.3 Throughput Delay Considerations

The 2048 channel configuration double buffers all channels. Timeslot sequence integrity will be maintained for all switching configurations except in cases where channels 0, 1 or 2 (on stream 0 of both PACs) are involved. For all other output channels, data clocked into the switch on any of the serial inputs in any specific frame (n) will be clocked out in the next frame (n+1). If data from any input channel is switched to channels 0, 1 or 2 (channel 2 on S0 only of both PACs), it will be clocked out one frame later (n+2).

It is not important to understand the reasoning behind the differential delay (see boxed area, "Throughput Delay in Serial Bus Applications", for explanation). However, it is important to realize the implications this has on switching packetized data over hyper-channels through the switch. To illustrate the implications, consider the case where channels 0, 1, 2 and 3 on serial stream 0 (S0) form a hyper-channel generated by an HDLC device and are all clocked into the PAC in frame 1 (numbered arbitrarily). If these channels are switched through the SMX/PAC to output channels 0, 1, 2 and 3 respectively on stream 0, the contents of channels 0, 1 and 2 will be output in frame 3 while channel 3 will be output in frame 2. Timeslot integrity would not be maintained and the packet would be corrupted. On the other hand, consider the case where input channels 3, 4, 5 and 6 are clocked into the switch in frame 1 and switched to output channels 3, 4, 5 and 6. In this instance, contents of the input channels will be clocked out in frame 2. Timeslot sequence integrity will be maintained. The advantages of double buffering are realized when the differences between input and output channels are not constant for the various channels as may be the case if channels 3, 5, 8 and 10 are switched to channels 5, 6, 7 and 8. In this case if the input channels are clocked into the SMX in frame 1, the contents of the channels will be clocked out in frame 2. Timeslot integrity will once again be maintained and the throughput delay will be constant.

In conclusion, if it is necessary to switch hyper-channels through the SMX/PAC circuit described above, channels 0 and 1 on any of the output streams should not be included as part of the hyper-channel. Channel 2 on stream 0 (for both PAC 2a and 2b) should also not be used as part of the hyper channel. The throughput delay for switching channels 0 to 0, 1 to 1, 2 to 2 will be two frames. The delay for switching channel 3 to 3, 4 to 4, etc., is only one frame. It is possible to double buffer all channels by offsetting the serial input and output frames. To implement the offsets, it is necessary to

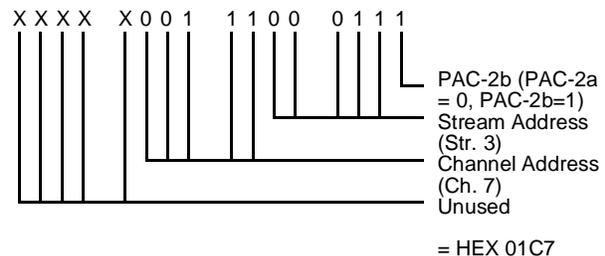
generate the connection memory and data memory frame pulses externally.

4.2.4 Programming the 2048 Channel Switch

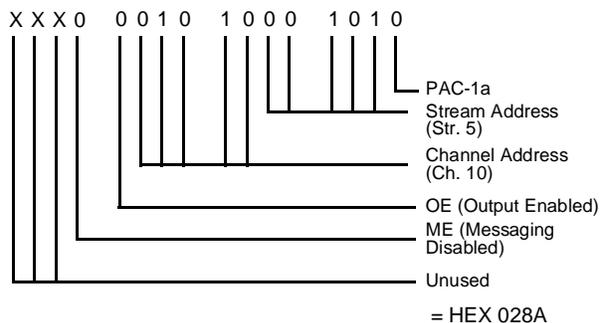
The principles involved in switching any incoming serial channel to a serial output channel timeslot are identical to those presented in the parallel switching section (see Section 4.1.4). The address of the source channel is stored in the connection memory location corresponding to the destination channel. Since the actual switching function is accomplished in parallel by the SMX, it is necessary to determine the parallel timeslot addresses corresponding to the serial channels. As discussed in the 1K switching section, the mapping of the PAC serial channels onto SMX parallel timeslots can be accomplished by directly coding the serial channel and stream number in binary as shown in Figure 3. In the 2K configuration, consecutive channels clocked out by the SMX are latched into PAC-2a and PAC-2b alternatively. If the numbering of the serial streams on the two PACs is kept distinct (i.e., 0 to 31 for PAC-2a and 0 to 31 for PAC-2b) the LSB in the binary coding can be used to point to the PAC on which the serial stream is located. This is explained in the following paragraph with an example.

To illustrate the basic switching principles, consider the example where channel 10 on stream 5 of PAC-1a is switched to channel 7 on stream 3 on PAC-2b. The example discussed below assumes that the PACs are configured for 2.048 Mb/s operation. The following is an outline of the steps to be followed.

1. Determine the SMX memory address corresponding to the output channel. Ch. 7, Str. 3 on PAC-2b in binary is shown below:



2. Store the address of the source channel in the address decoded above (Hex 01C7). The state of the control bits for D11 and D12 (OE and ME) is also stored into the addressed location at this time. The SMX address corresponding to the input channel timeslot and the position of the control bits is decoded below as follows:



The SMX timeslot address can be derived directly from the serial channel and stream address using the following algebraic relationship:

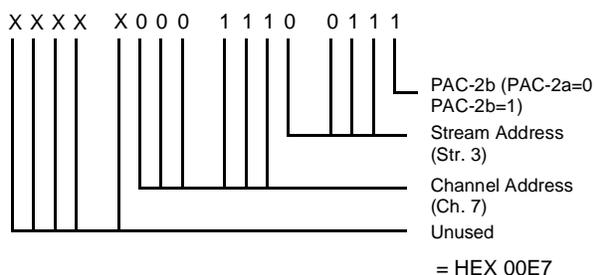
$$SMX\ Timeslot\ \# = (C * 64) + 2S + P$$

where

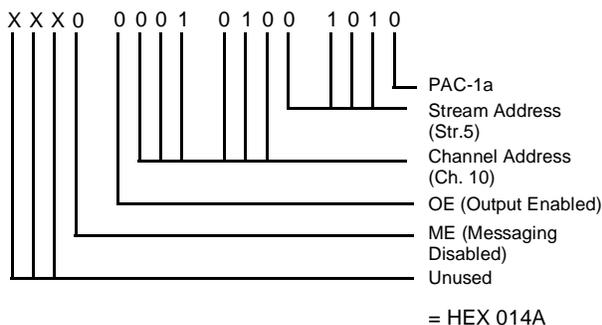
- C = Channel number 0, 1, 2, ...,31
- S = Stream number 0, 1, 2, ...,31
- P = PAC 0 for PAC-2a
1 for PAC-2b

Decoding the timeslot addresses from the serial channel and stream address when the PACs are operated in 4.096 Mb/s mode can be accomplished in a similar manner. The only difference is that the channel address is coded with six bits while the stream address is coded with four bits. Considering the same example presented above:

The SMX timeslot corresponding to output Channel 7 Stream 3 on PAC-2b is decoded as follows:



The SMX timeslot corresponding to input Channel 10 Stream 5 on PAC-2a is decoded as follows:



In this configuration the algebraic relationship for 4.096 Mb/s serial streams is:

$$T = (C * 32) + 2S + P$$

where

- T= SMX Timeslot #
- C = Channel number 0, 1, 2, ...,63
- S = Stream number 0, 1, 2,15
- P = PAC 0 for PAC-2a
1 for PAC-2b

5.0 Design of 4096 Channel Switch Matrix

The most efficient implementation of a 4096 (4K) channel matrix using the SMX/PAC is to use the 2K parallel building block described in sec. 4. A total of four 2K building blocks are required to construct a 4K timeslot interchange circuit. A block diagram showing the interconnections between the various components is presented in Figure 15. Eight PACs provide access to serial busses if necessary. The timing interface between the PACs and the SMX is identical to that described in the 2K configuration.

5.1 Circuit Operation

Figure 15 illustrates the interconnections between the various devices. Each block marked Parallel Switch Block (PSB) is a 2K switching block made up of three SMXs. Refer to Section 4 (Figure 11) for details on the PSB. The parallel input bus of each PSB is connected to the PSB of one other PSB. Similarly, the output bus of each PSB is connected to the output bus of one other PSB as follows:

Input Busses	PSB-1 and PSB-2 PSB-3 and PSB-4
Output Busses	PSB-1 and PSB-3 PSB-2 and PSB-4

Note that only one PSB in an interconnected pair should be programmed to drive the bus. The ODE control line on the Data Memory SMX should be enabled for only one PSB in a pair. In Figure 11 the state of the ODE line is controlled by D11 on the Connection memory and the Timed Enable (TE) input. During power up, the TE input should be pulled low to ensure that the output drivers of the PSB are disabled - until the controlling processor has programmed the state of the ODE pin. See the next section for information on how the ODE pin is controlled by the processor.

The serial interface to the main 4K switch block is provided by four PACs. Each PAC is configured for interfacing to the SMX in the 2K mode. All framing

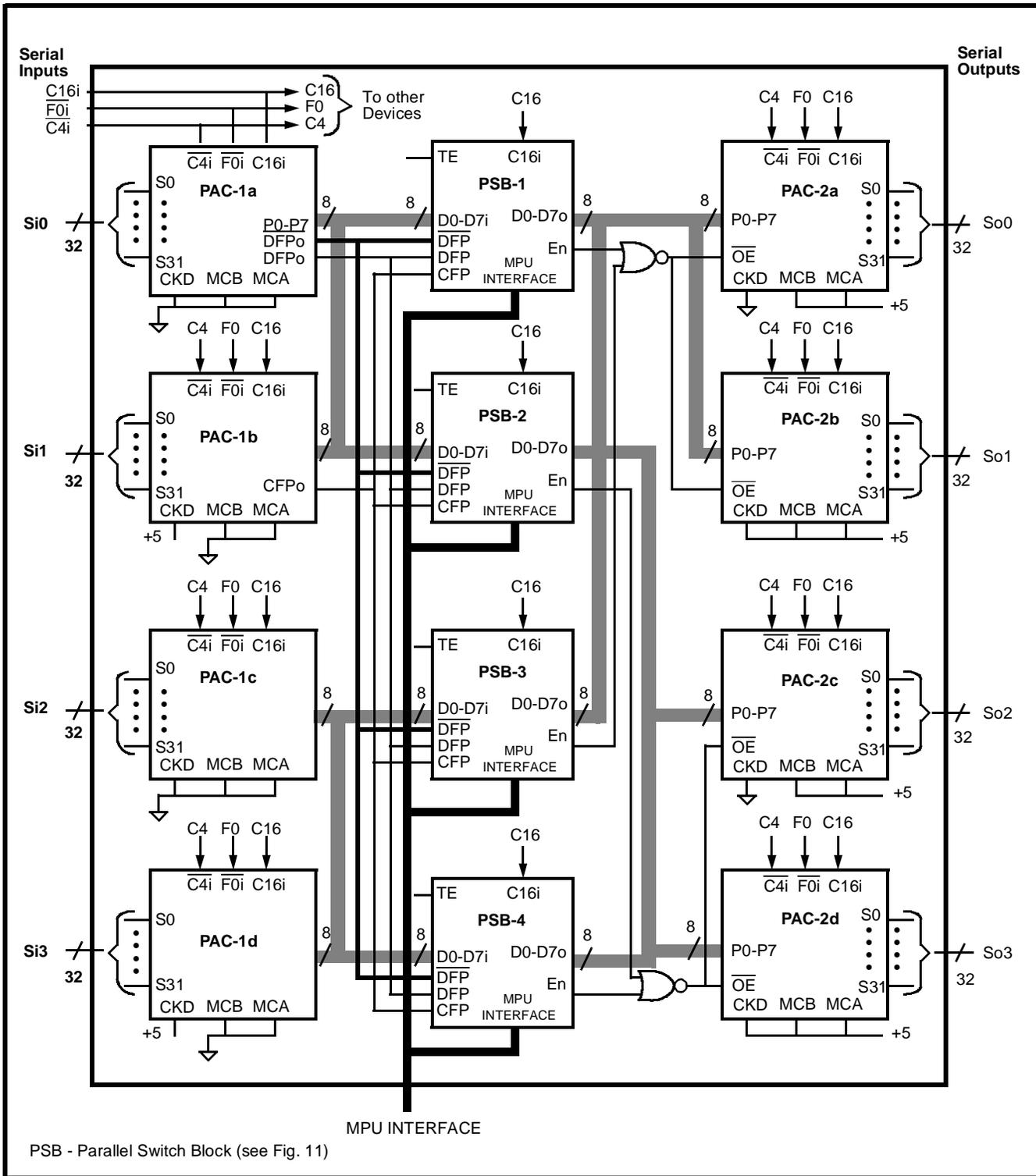


Figure 15 - 4096 Channel Serial Switch Block (SB)

signals for the PSBs are generated by PAC-1a and PAC-1b.

5.2 Programming the 4K Switch Matrix

The steps in programming the 4K switch are very similar to those used for the 2K switch. The only extra factor included here is the requirement to

ensure that the output drivers of only one SMX in an interconnected pair are enabled. As mentioned earlier, D11 controls the state of the ODE pin of the Data Memory SMXs. Once it is determined which SMX is going to be driving the bus, the ODE of that SMX would be enabled by writing a 1 to B11 in the connection memory corresponding to the output channel. On initial power up, a timer should be used

to pull the TE pin low. This will ensure that there is no contention on the output bus of the SMX. The processor controlling the switch should be programmed to load the connection memory contents with Hex 0000 before the TE input is set high.

As discussed in the 2K configuration programming example, it is necessary to translate the serial channel and stream address to the corresponding SMX addresses. To illustrate consider the following specific switching examples:

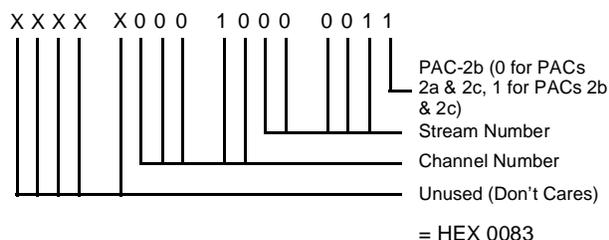
Example 1

Switch input channel 1 on stream 0, PAC-1a to output channel 2 on stream 1, PAC- 2b.

Input: Channel 1 on Stream 0, PAC-1a
Output: Channel 2 on Stream 1, PAC-2b

To program the switch the following steps should be followed:

1. Determine the SMX address corresponding to output channel in binary:

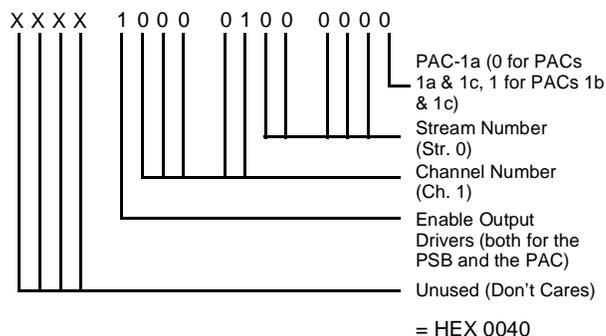


2. Determine the path from the input PAC to the output PAC.

Note from Figure 15, the only path from PAC-1a to PAC-2d is via PSB-2. Because the output busses of PSB-2 and PSB-4 are interconnected, it is necessary to disable the drivers of PSB-4 during the specific output timeslot. This is achieved by writing Hex 0000 to connection memory address Hex 0083 in PSB-4. However, this step may not be necessary, if all connection memory addresses were reset during power up initialization.

3. Store the address of the source channel in the memory location decoded in 1 for the PSB specified in 2. The required state of the other control bits should be stored at the same time.

Storing the following binary word in connection memory address Hex 0083 in PSB-2 will complete the connection:



Writing Hex 0000 into the output timeslot memory location will tear down the connection.

Example 2

Input: Channel 10 on Stream 4, PAC-1d
Output: Channel 4 on Stream 3, PAC-2a

SMX output timeslot address corresponding to output serial channel is:

XXXX X001 0000 0110 = Hex 0106

The only path connecting PAC-1d to PAC-2a is via PSB-3. Therefore, to make the connection, the address of the source channel is written to the Connection Memory location corresponding to the output timeslot on PSB-3. It is assumed that the output drivers on PSB-1 will be disabled during this time. Writing the following binary word to memory address Hex 0106 in PSB-3 will complete the connection:

XXXX X010 1000 1001 = Hex 0289

Once again, writing Hex 0000 to this memory location will tear down the connection.

6.0 Design of Switch Matrices Larger than 4K

Implementation of an 8192 (8K) channel parallel timeslot interchange circuit using the SMX requires connection of the outputs of each SMX serving as the data memory to eight other SMXs. The resulting large capacitive load may limit applications where this matrix can be used - largely due to excessive delay introduced by the capacitive loading. A possible solution is to use high speed drivers on the output bus.

Serial matrices with 8K channel capacity can be easily implemented. The input/output timing on the

serial busses of the PAC is not as critical as on the SMX parallel bus. Figure 16 illustrates an example configuration. Each of the blocks shown in the diagram is a 4K serial matrix block.

It is possible to construct an 8K parallel timeslot interchange circuit using the SMX with external buffers to handle the large capacitive load.

7.0 Conclusions

The SMX and PAC have been designed to provide a flexible and optimized solution for digital switch implementation. As has been illustrated with the examples discussed in the application note, matrices from 1K and up can be constructed very efficiently to meet all switching requirements.

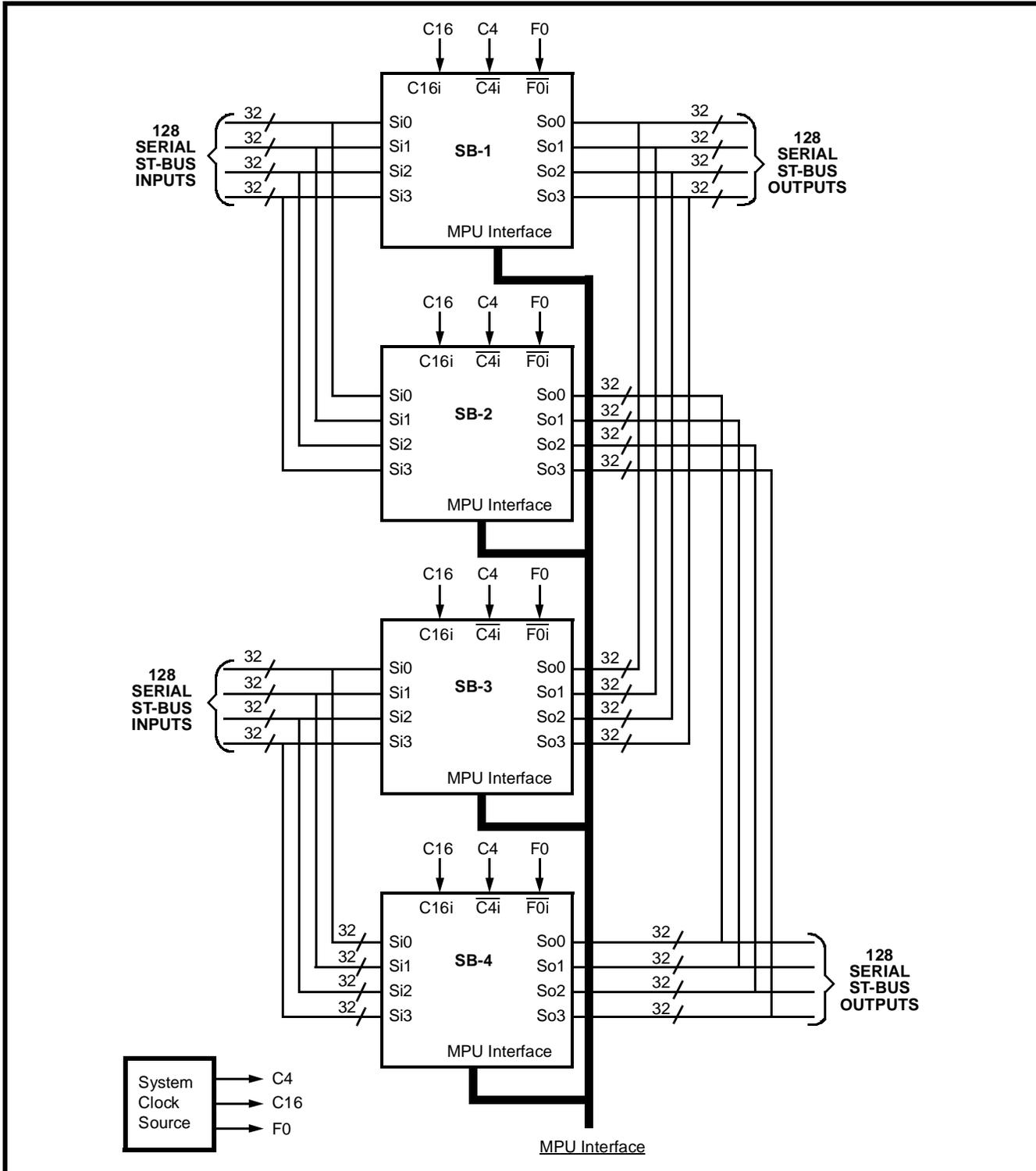


Figure 16 - 8192 Switching Matrix Block

Note: SB-1 to SB-4 Serial Switching Blocks (see Fig. 15)