MSAS-68

Guidelines on a Printed Circuit Board Layout for the MT8910

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1.0 Introduction

The MT8910 Digital Subscriber Line Interface Circuit (DSLIC) is one of the most complex integrated circuits ever developed for telecommunication applications. The performance of this complex device incorporating both analog and digital circuitry can be maximized by proper design of the printed circuit board. This application sheet provides guidelines on how to design PCBs holding the DSLICs.

2.0 DSLIC's Internal Layout and Pin Configuration

The semiconductor process used for the DSLIC does not permit a full isolation of analog and digital circuitry on the same silicon die. As shown in Fig. 1, the analog and digital ground pins, AV_{SS} and V_{SS} can remain isolated as long as the differential voltage between them does not exceed 0.4V. But the +5V supply pins AV_{DD} and V_{DD} are internally connected through the substrate, and the connection between them behaves as a low resistive short. This has a direct bearing on the decoupling circuit because it does not allow the use of two fully independent power supplies. If two separate power supplies are used, then the differential voltage between the supplies at the power-up may damage the internal structure of the DSLIC.

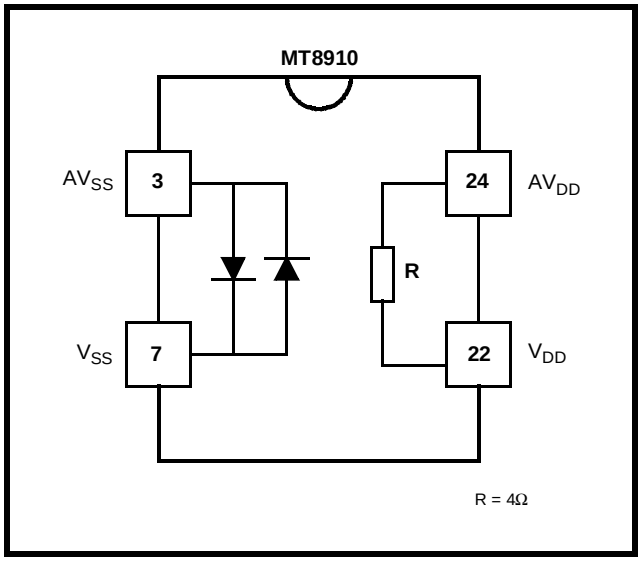

Figure 1 - Internal Arrangement of Power Supply Distribution

The DSLIC's internal circuit layout is carefully done so as to minimize the interference between the analog and digital sections. The pin configuration is also selected accordingly, to reduce the cross-coupling effects between the two sections.

3.0 Suggested Ground and Supply Connections

Proper grounding, power supply distribution and decoupling techniques on a printed circuit board have a big impact on the total performance of the system associated with the DSLIC. It is suggested that the external components, PCB tracks and circuits on the board (see Fig. 2) follow a similar separation between the digital and analog sections (as inside the DSLIC) to reduce the effect of interference on one another. Grounding and power supply distribution depends upon the number of metallic layers in a printed circuit board. In the case of two-layer boards, it is recommended to run two separate power distribution networks, one for analog and the other for digital circuitry. Both distribution networks MUST BE CONNECTED TOGETHER at a single place on the board (usually at the edge connector) to protect the DSLIC from being damaged.

Two-layer PCBs will perform well in a low density application, but in the case of compact design, four-layer PCBs with separate "GROUND" and "+5V" layers are highly recommended. Experiments show that solid power and ground planes provide very good performance. It is useful to go even further and split the "GROUND" plane into "ANALOG GROUND" and "DIGITAL GROUND" within the same physical plane. A similar split can also be planned for a "+5V" supply plane.

Recommended decoupling is shown in the Applications section of the MT8910 data sheet. Both figures show that the V_{Ref} (pin 26) and V_{Bias} (pin 25) pins should be decoupled to AV_{SS} with 1µF capacitors. Special considerations should be given when selecting decoupling capacitors because not all capacitors are good for decoupling. The most common mistake is the use of high quality capacitors with very low losses. Unfortunately, this type of capacitor, instead of suppressing the high frequency interference, resonates in conjunction with the

inductance of the tracks. We recommend 1 µF decoupling capacitors with high dielectric losses like the ones based on Z5U dielectric. If this value is not available then the alternative choice can be 2.2 µF electrolytic or tantalum capacitor in parallel with 0.1µF ceramic capacitors (with Z5U dielectric).

In case of line cards where many DSLICs are on the same board, each of them should have its own decoupling capacitors for AV_{DD} (+5V) and V_{DD} (+5V). These capacitors should be placed very close to the power supply pins to be effective.

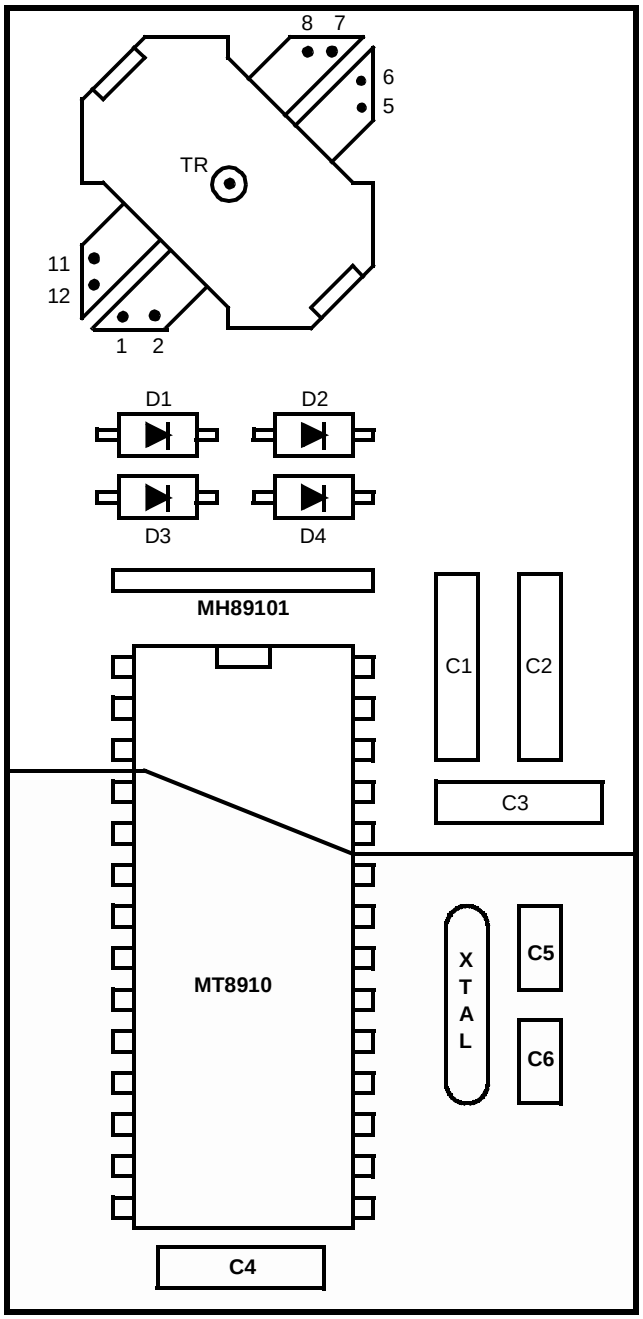

Figure 2 - Example of Components Layout on the Board

ANALOG CIRCUIT AREA

DIGITAL CIRCUIT AREA

Components List:

TR	=	Transformer TPW4671
D1-D4	=	Protection Diodes MUR105
C1	=	V_{Ref} Decoupling Capacitor 1µF
C2	=	V_{Bias} Decoupling Capacitor 1µF
C3	=	AV_{DD} Decoupling Capacitor 1µF
C4	=	V_{DD} Decoupling Capacitor 1µF
Xtal	=	10.24 MHz Crystal