MT90732
E2/E3 Framer (E2/E3F)

Preliminary Information

ISSUE 1 October 1995

Features

- Framer for ITU-T Recommendations:
  - G.742 (8448 kbit/s)
  - G.745 (8448 kbit/s)
  - G.751 (34368 kbit/s)
  - G.753 (34368 kbit/s)
- Line side interface:
  - Dual Rail or NRZ
- HDB3 codec for dual rail I/O
- Terminal side interface:
  - Nibble-parallel
  - Bit-serial
- Transmit reference generator for serial I/O
- Microprocessor or control leads
- Service bit I/O port

Applications

- Line terminals
- Wideband data or video transport
- Test equipment
- Multiplexer systems

Ordering Information

MT90732AP 68 Pin PLCC

-40°C to +85°C

Description

The MT90732 E2/E3 Framer (E2/E3F) is a CMOS VLSI device that provides the functions needed to frame a wideband payload to one of four ITU-T Recommendations: G.742, G.745, G.751, or G.753. The E2/E3 Framer interfaces to line circuitry with either dual rail or NRZ signals. On the terminal side, the interface can be either nibble-parallel or bit-serial.

The MT90732 can be operated with or without a microprocessor. When interfaced with a microprocessor, the E2/E3 Framer provides an 8-byte memory map for controlling the device and reporting performance and alarm status. The MT90732 provides a transmit and receive interface port for accessing the overhead bits as defined in the ITU-T recommendations.

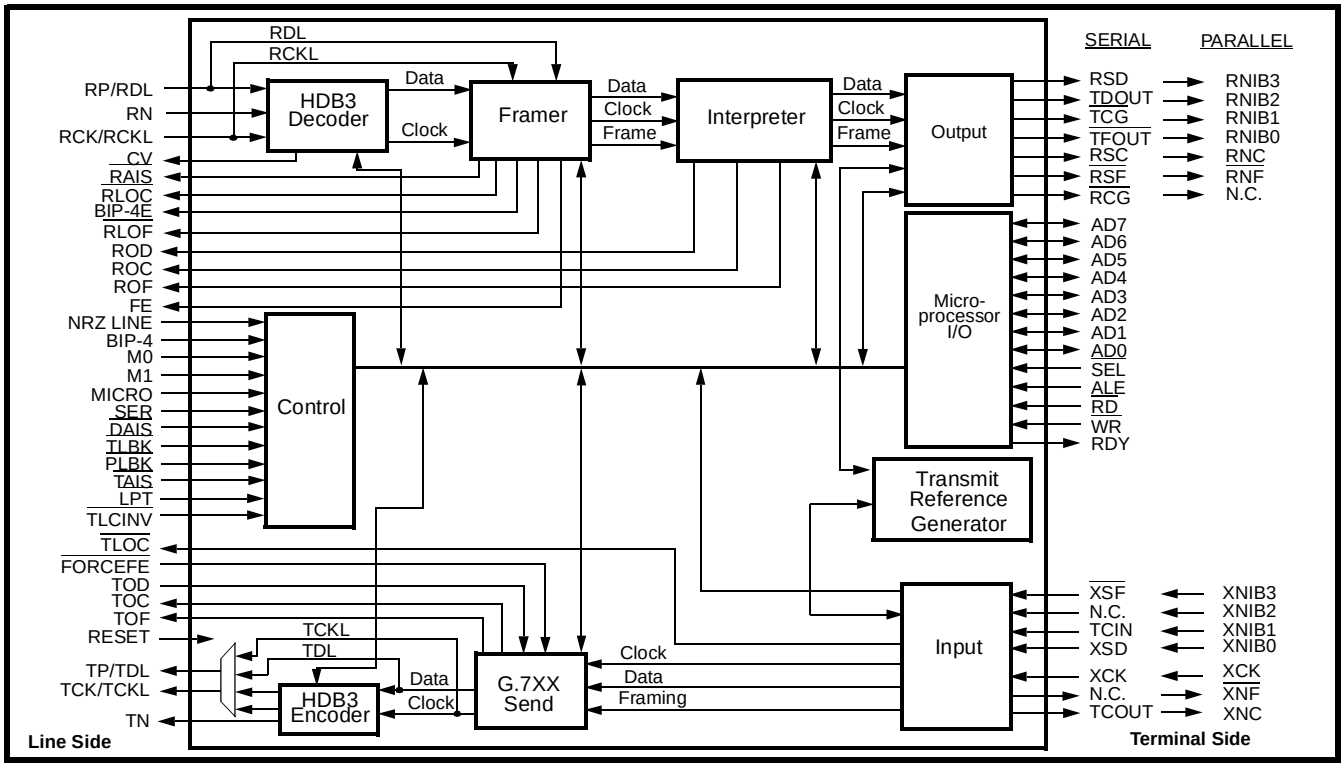


Figure 1 - Functional Block Diagram

U.S. Patent Number 5040170

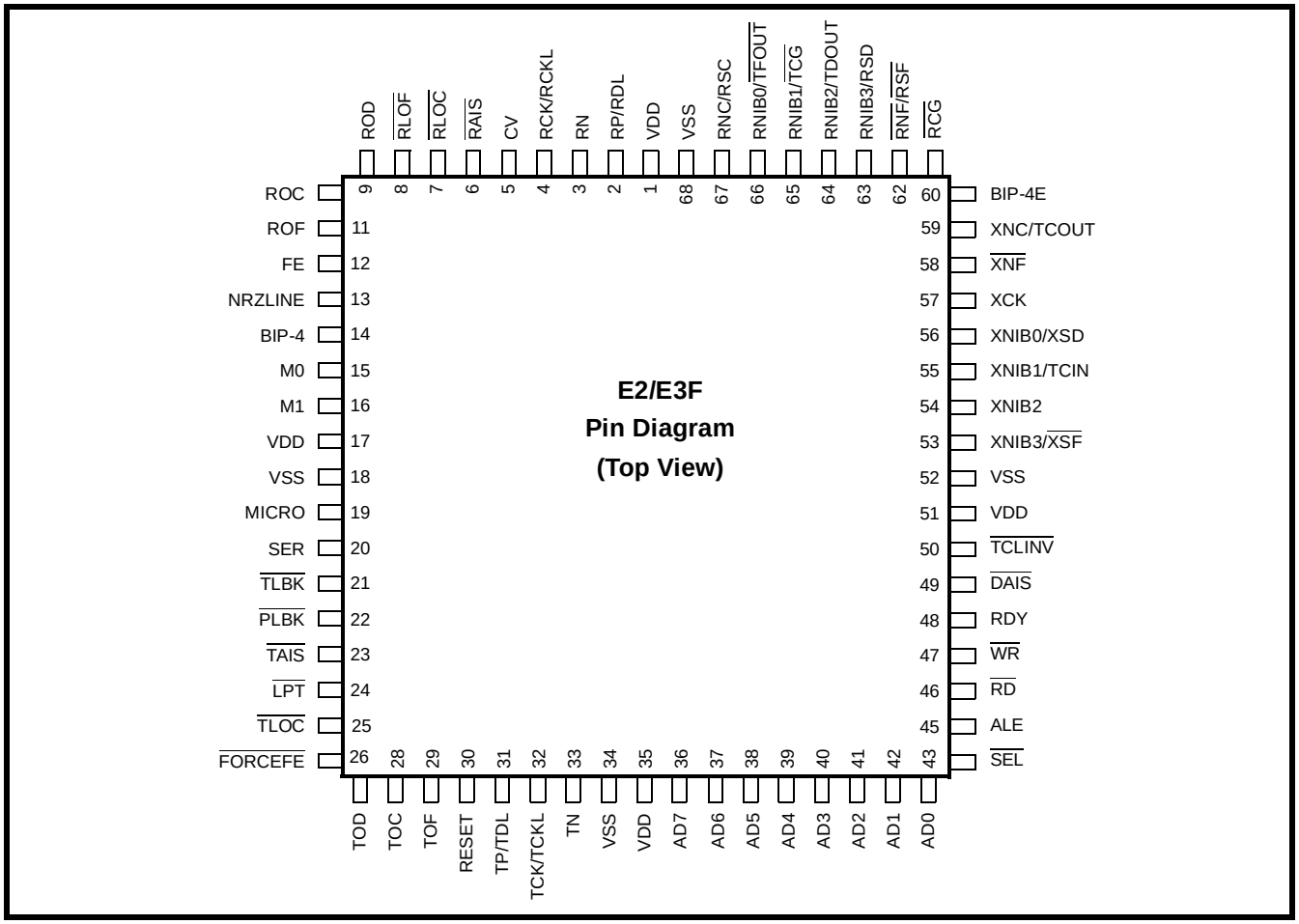


Figure 2 - Pin Connections

Pin Description

Power Supply and Ground

Pin #	Name	I/O/P*	Description
1,17,35,51	VDD	P	**Power Supply.** 5-volt supply voltage, +/- 5%
18,34,52,68	VSS	P	**Ground.**

*Note: I = Input; O = Output; P = Power

Line Side Receive

Pin #	Name	I/O/P*	Description
2	RP/RDL	I	**Receive Positive Rail/Receive NRZ Data.** Positive rail input data is clocked into the E2/E3F on negative transitions of the clock signal RCK/RCKL. The HDB3 codec for dual rail operation is enabled by applying a low to the NRZLINE(pin 13). Receive NRZ data is clocked into the E2/E3F on positive transitions of the clock signal RCK/RCKL. The NRZ mode is enabled by applying a high to the NRZLINE.
3	RN	I	**Receive Negative Rail Data.** Negative rail input data is clocked into the E2/E3F on negative transitions of the clock signal RCK/RCKL. The HDB3 codec for dual rail operation is enabled by applying a low to the NRZLINE signal lead.
4	RCK/ RCKL	I	**Receive Clock Rail/Receive Clock NRZ.** The receive clock is used for clocking in the dual rail/NRZ data signals and is used as the time base for receiver operation.

*Note: I = Input; O = Output; P = Power

Line Side Transmit

Pin #	Name	I/O/P*	Description
31	TP/TDL	O	**Transmit Positive Rail/Transmit NRZ Data.** Positive rail data is clocked out of the E2/E3F on positive transitions of the clock signal TCK/TCKL when TLCINV is high and on negative transition of the clock when TLCINV is low. The HDB3 codec for dual rail operation is enabled by applying a low to the NRZLINE (pin 13). Transmit NRZ data is clocked out of theE2/E3F on negative transitions of the clock signal TCK/TCKL. The NRZ mode is enabled by applying a high to the NRZLINE.
32	TCK/TCKL	O	**Transmit Clock Rail/Transmit Clock NRZ.** The transmit clock is used for clocking out the dual rail/NRZ data signals. The TCK/TCKL clock signal is derived from the XCK clock. Note: When XCK is removed, the framer uses TCIN to generate TCK/TCKL (in bit-serial mode only). If both XCK and TCIN are removed, TCK/TCKL is derived from RCK/RCKL. This clock may be inverted by using control input $\overline{\text{TLCINV}}$ (pin 50)
33	TN	O	**Transmit Negative Rail Data.** Negative rail output data is clocked out of the E2/E3F on positive transitions of the clock signal TCK/TCKLwhen $\overline{\text{TLCINV}}$ (pin 50) is high and on negative transitions of the clock when $\overline{\text{TLCINV}}$ is low. The HDB3 codec for dual rail operation is enabled by applying a low to the NRZLINE.

*Note: I = Input; O = Output; P = Power

Terminal Interface

Pin #	Name	I/O/P*	Description
61	$\overline{\text{RCG}}$	O	**Receive Clock Gapped.** An active low signal which indicates the receive framing and service bit locations. The $\overline{\text{RCG}}$ signal is provided in the bit- serial mode only.
62	$\overline{\text{RNF}}$/$\overline{\text{RSF}}$	O	**Receive Framing Pulse.** This active low framing pulse is synchronous with the last nibble (RNBn) for the terminal side nibble-parallel interface, and with the first bit in the frame for the bit-serial interface.
63	RNIB3/ RSD	O	**Receive Nibble Bit 3/Receive Serial Data.** Bit 3 is the most significant bit in the nibble and corresponds to the first bit of the nibble received on the line side. The framing pattern, service bits, and BIP-4 nibble are not output as parallel data. In the bit-serial mode, the Receive Serial Data consists of all bits, including the framing pattern and service bits.
64	RNIB2/ TDOUT	O	**Receive Nibble Bit 2/Transmit Reference Generator Data Output.** In the nibble-parallel mode, it is Bit 2 of the received nibble. The reference generator is enabled in the bit-serial mode. The output data signal (TDOUT) contains of all ones in place of the framing bits and zeros elsewhere in the frame. The TDOUT signal is generated from the input clock (TCIN).
65	RNIB1/ $\overline{\text{TCG}}$	O	**Receive Nibble Bit 1/Transmit Reference Generator Clock Gap Signal.** In the nibble-parallel mode, it is Bit 1 of the received nibble. The reference generator is enabled in the bit-serial mode. The active low $\overline{\text{TCG}}$ signal indicates the location of the framing pattern and the service bits in the frame. The $\overline{\text{TCG}}$ signal is generated from the input clock (TCIN).
66	RNIB0/ $\overline{\text{TFOUT}}$	O	**Receive Nibble Bit 0/Transmit Reference Generator Framing Pulse.** Bit 0 is the least significant bit in the nibble and is the last bit received. The reference generator is enabled in the bit-serial mode. The active low $\overline{\text{TFOUT}}$ signal is one clock cycle (TCOUT) wide, and is synchronous with the first bit in the frame. The $\overline{\text{TFOUT}}$ signal is generated from the input clock (TCIN).

Terminal Interface (Continued)

Pin #	Name	I/O/P*	Description
67	RNC/RSC	O	**Receive Nibble Clock/Receive Serial Clock.** The nibble and serial clocks are derived from the line side dual rail/NRZ clock signal (RCK/RCKL). A received nibble is clocked out on positive transitions of RNC. The RNC is gapped during framing pattern, service bit and BIP-4 bit times, if BIP-4 option is selected. Serial data is clocked out on positive transitions of RSC.
53	XNIB3/ $\overline{\text{XSF}}$	I	**Transmit Nibble Bit 3/Transmit Serial Framing Pulse.** For the terminal side nibble-parallel interface, bit 3 is the most significant bit in the nibble and corresponds to the first bit transmitted. When the terminal interface is bit-serial, the negative framing pulse is synchronous with the first bit in the frame. For the bit-serial interface, the $\overline{\text{XSF}}$ may be derived from transmit reference generator framing pulse ($\overline{\text{TFOUT}}$).
54	XNIB2	I	**Transmit Nibble Bit 2.** Bit 2 in the 4-bit nibble.
55	XNIB1/ TCIN	I	**Transmit Nibble Bit 1/Transmit Reference Generator Clock In.** Bit 1 in the transmit nibble. For a bit-serial interface, the reference clock TCIN is used to derive the clock out (TCOUT), data signal (TDOUT), framing pulse ($\overline{\text{TFOUT}}$), and gapped clock signal ($\overline{\text{TCG}}$). These Transmit Reference Generator signals are provided for multiplexing the external payload data into the serial frame. The E2/E3F requires a transmit clock having a frequency of 8448 kHz with a stability of +/- 30 ppm to meet the clock tolerance specified in ITU-T Recommendations G.742 and G.745. For Recommendations G.751 and G.753, the required clock frequency is 34368 kHz with a stability of +/- 20 ppm.
56	XNIB0/ XSD	I	**Transmit Nibble Bit 0/Transmit Serial Data.** For the terminal side nibble-parallel interface, bit 0 is the least significant bit in the nibble and the last bit from the nibble that is transmitted. For a bit-serial interface, the input (XSD) must consist of all the bits in the frame. It is recommended that the signals generated by the Transmit Reference Generator be used for multiplexing the data into the frame. The E2/E3F inserts a new framing pattern and the service bits (from the external interface or the memory map) into the transmit data stream determined by the location of the framing pulse ($\overline{\text{XSF}}$).
57	XCK	I	**Transmit Clock.** For the terminal side nibble-parallel interface, the transmit clock is used for all transmit timing functions, including deriving the nibble output clock (XNC) and framing pulse ($\overline{\text{XNF}}$). The E2/E3F requires a transmit clock having a frequency of 8448 kHz with a stability of +/- 30 ppm to meet the clock tolerance specified in ITU-T Recommendations G.742 and G.745. For Recommendations G.751 and G.753, the required clock frequency is 34368 kHz with a stability of +/- 20 ppm. For the bit-serial interface, this clock may be derived from the transmit reference generator clock output (TCOUT). The duty cycle must be 50 +/-5%.
58	$\overline{\text{XNF}}$	O	**Transmit Nibble Framing Pulse.** The nibble framing pulse and clock signal (XNC) are provided for loading nibble data into the E2/E3F from external circuitry. The negative framing pulse identifies the first bit in the frame.
59	XNC/ TCOUT	O	**Transmit Nibble Clock/Transmit Reference Generator Clock Out.** The nibble clock is derived from the transmit clock (XCK) and is used as a time base for clocking data out of the external circuitry and into the E2/E3F. XNC is gapped during the framing pattern, service bit and BIP-4 bit times, if BIP-4 option is selected. Data is clocked in on positive transitions. TCOUT is derived from the input clock (TCIN), and has the same duty cycle.

*Note: I = Input; O = Output; P = Power

Service Bit Interface

Pin No.	Symbol	I/O/P*	Name/Function
9	ROD	O	**Receive Service Data Bits.** The service bits for the G.742 and G.751 recommendations are defined as bits 11 and 12. For the G.745 and G.753 recommendations, the service bits are defined as 5 through 8 in Sets II and III. The service bits for all four recommendations are given in Figure 3.
10	ROC	O	**Receive Service Bits Clock.** A gapped clock that clocks out the service bits on positive transitions.
11	ROF	O	**Receive Service Bits Framing Pulse.** A positive framing pulse that is synchronous with the first bit in the frame.
27	TOD	I	**Transmit Service Data Bits.** The service bits for G.742 and G.751 are bits 11 and 12. For G.745 and G.753, the service bits are 5 through 8 in Sets II and III. When the E2/E3F is configured to work with a microprocessor, bit 0 (OHI/O) in location 00H selects service bit interface. A one enables external service bit interface (TOD). A zero disables external service bit interface and the service bits are transmitted from internal memory map.
28	TOC	O	**Transmit Service Bits Clock.** A gapped clock that clocks in the service bits on positive transitions.
29	TOF	O	**Transmit Service Bits Framing Pulse.** A positive framing pulse that is synchronous with the first bit in the frame.

*Note: I = Input; O = Output; P = Power

Microprocessor Interface

Pin No.	Symbol	I/O/P*	Name/Function
36-43	AD(7-0)	I/O	**Address/Data Bus.** These leads constitute the time-multiplexed address and data bus for accessing the registers which reside in the E2/E3F.
44	$\overline{\text{SEL}}$	I	**Select.** A low enables the microprocessor to access the E2/E3F memory map for control, status, and alarm information.
45	ALE	I	**Address Latch Enable.** An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle.
46	$\overline{\text{RD}}$	I	**Read.** An active low signal generated by the microprocessor for reading the registers which reside in the memory map. The E2/E3F memory map is selected by placing a low on the select pin.
47	$\overline{\text{WR}}$	I	**Write.** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The E2/E3F memory map is selected by placing a low on the select pin.
48	RDY	O	**Ready.** An active high signal indicating an E2/E3F acknowledgment to the microprocessor that the addressed memory map location can complete the data transfer.

*Note: I = Input; O = Output; P = Power

Control Interface

<table>
<tr><th>Pin #</th><th>Name</th><th>I/O/P</th><th>Description</th></tr>
<tr><td>13</td><td>NRZLINE</td><td>I</td><td>Non-Return to Zero Line Selection. A high on this pin configures the line side I/O in NRZ format (RP and TP) and bypasses the HDB3 Encoder/Decoder. When low, the dual rail format (RP/RN and TP/TN) is selected and the HDB3 Encoder/Decoder is enabled.</td></tr>
<tr><td>14</td><td>BIP-4</td><td>I</td><td>Bit Interleaved Parity - 4. A high enables the BIP-4 function. In the transmit direction, the BIP-4 is calculated for data nibbles only, and is sent as the last nibble in the frame. In the receive direction, the BIP-4 is calculated for the data bits only and compared against the received value which is present in the last four bits of the frame. An output indication (BIP-4E) occurs when one or more columns do not match. A BIP-4 error mask is provided in the memory map which permits transmit BIP-4 values to be inverted. At the terminal interface, the transmit and receive nibble clocks are gapped to accommodate the time that corresponds to the BIP-4 nibble.</td></tr>
<tr><td>15
16</td><td>M0
M1</td><td>I</td><td>Mode Control. The two controls select the operating rate of the E2/E3F according to the table given below:
<table>
<tr><th>M1</th><th>M0</th><th>Recommendation</th><th>Rate (kbit/s)</th></tr>
<tr><td>low</td><td>low</td><td>G.745</td><td>8448</td></tr>
<tr><td>low</td><td>high</td><td>G.742</td><td>8448</td></tr>
<tr><td>high</td><td>low</td><td>G.753</td><td>34368</td></tr>
<tr><td>high</td><td>high</td><td>G.751</td><td>34368</td></tr>
</table></td></tr>
<tr><td>19</td><td>MICRO</td><td>I</td><td>Microprocessor Mode. A high enables the microprocessor interface. When the microprocessor is enabled, the following hardware control leads are disabled: BIP-4, Mode Control (M0 and M1), Serial Interface (SER), and Transmit Alarm Indication Signal ($\overline{\text{TAIS}}$). Bits are provided in the memory map for implementing these functions.</td></tr>
<tr><td>20</td><td>SER</td><td>I</td><td>Serial Interface. This control lead determines the type of terminal side interface. A high selects the bit-serial interface. A low selects the nibble-parallel interface.</td></tr>
<tr><td>21</td><td>$\overline{\text{TLBK}}$</td><td>I</td><td>Terminal Loopback. A low enables the transmit- to- receive loopback at the line side. The receive line input is ignored. When this lead is active then it dominates over memory map control bit (TLBK).</td></tr>
<tr><td>22</td><td>$\overline{\text{PLBK}}$</td><td>I</td><td>Payload Loopback: A low enables the receive- to- transmit loopback at the terminal side in the bit-serial mode of operation only. When this lead is active then it dominates over memory map control bit (PLBK).</td></tr>
<tr><td>23</td><td>$\overline{\text{TAIS}}$</td><td>I</td><td>Transmit Alarm Indication Signal. A low causes an all ones unframed signal (AIS) to be sent in place of a G.7XX frame on the line side.</td></tr>
<tr><td>24</td><td>$\overline{\text{LPT}}$</td><td>I</td><td>Loop Timing. A low enables the loop timing feature. Loop timing ignores the transmit clock (XCK) and enables the receive clock to be used as the transmit clock.</td></tr>
<tr><td>26</td><td>$\overline{\text{FORCEFE}}$</td><td>I</td><td>Force Framing Error. An errored framing bit is inserted into the transmit framing pattern upon a high to low transition of this input.</td></tr>
<tr><td>30</td><td>RESET</td><td>I</td><td>Reset. A positive pulse having a duration of at least 10 transmit clock cycles (XCK) applied to this pin resets the internal counters, logic circuits, and the performance counters and control bits in the memory map to zero. The reset pulse is applied after the power becomes stable.</td></tr>
<tr><td>49</td><td>$\overline{\text{DAIS}}$</td><td>I</td><td>Disable AIS. A low disables the automatic insertion of AIS into the terminal side receive nibble-parallel/bit-serial bit stream. Data is provided regardless of the line side content.</td></tr>
</table>

Control Interface (Continued)

Pin #	Name	I/O/P	Description
50	$\overline{\text{TLCINV}}$	I	**Transmit Line Clock Invert**. A low inverts the output clock (TCK) when operating in dual rail mode.
5	CV	O	**Coding Violation.** A positive pulse, one clock cycle wide, is generated when an illegal coding violation is detected. A coding violation is not part of the HDB3 zero-substitution code. A CV can occur because of noise or other impairments on the line. The output of this pin should be disregarded in the NRZ mode.
6	$\overline{\text{RAIS}}$	O	**Receive Alarm Indication Signal.** An active low alarm occurs within one millisecond after the E2/E3F detects an all unframed ones condition, even in the presence of a 10^{-5} error rate. An incoming signal with a framing pattern and all ones in the data field is not mistaken as an AIS.
7	$\overline{\text{RLOC}}$	O	**Receive Loss of Clock.** An active low alarm occurs when there are no transitions in the received clock (RCK/RCKL) for 10 clock cycles. Recovery occurs on the first clock transition.
8	$\overline{\text{RLOF}}$	O	**Receive Loss of Frame.** An active low alarm occurs when frame cannot be detected in the following modes and conditions: **G.742:** Four consecutive frames lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 1111010000 (10-bit pattern). **G.745:** Five consecutive frames lost. Recovery occurs when two consecutive frames are detected. The framing pattern is 11100110 (8-bit pattern). **G.751:** Four consecutive frames lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 1111010000 (10-bit pattern). **G.753:** Three consecutive frames lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 111110100000 (12-bit pattern).
12	FE	O	**Framing Error.** An active high alarm occurs when one or more framing bits are in error. The framing error alarm occurs at the end of the framing pattern and remains high until an error-free framing pattern is received or a loss of frame occurs.
25	$\overline{\text{TLOC}}$	O	**Transmit Loss of Clock.** An active low alarm occurs when there are no transitions in the transmit clock (XCK) for 10 clock cycles. Recovery occurs on the first clock transition.
60	BIP-4E	O	**BIP-4E.** A positive pulse occurs when the comparison between the received BIP-4 value and the calculated value does not match in a column.

*Note: I = Input; O = Output; P = Power

Functional Description

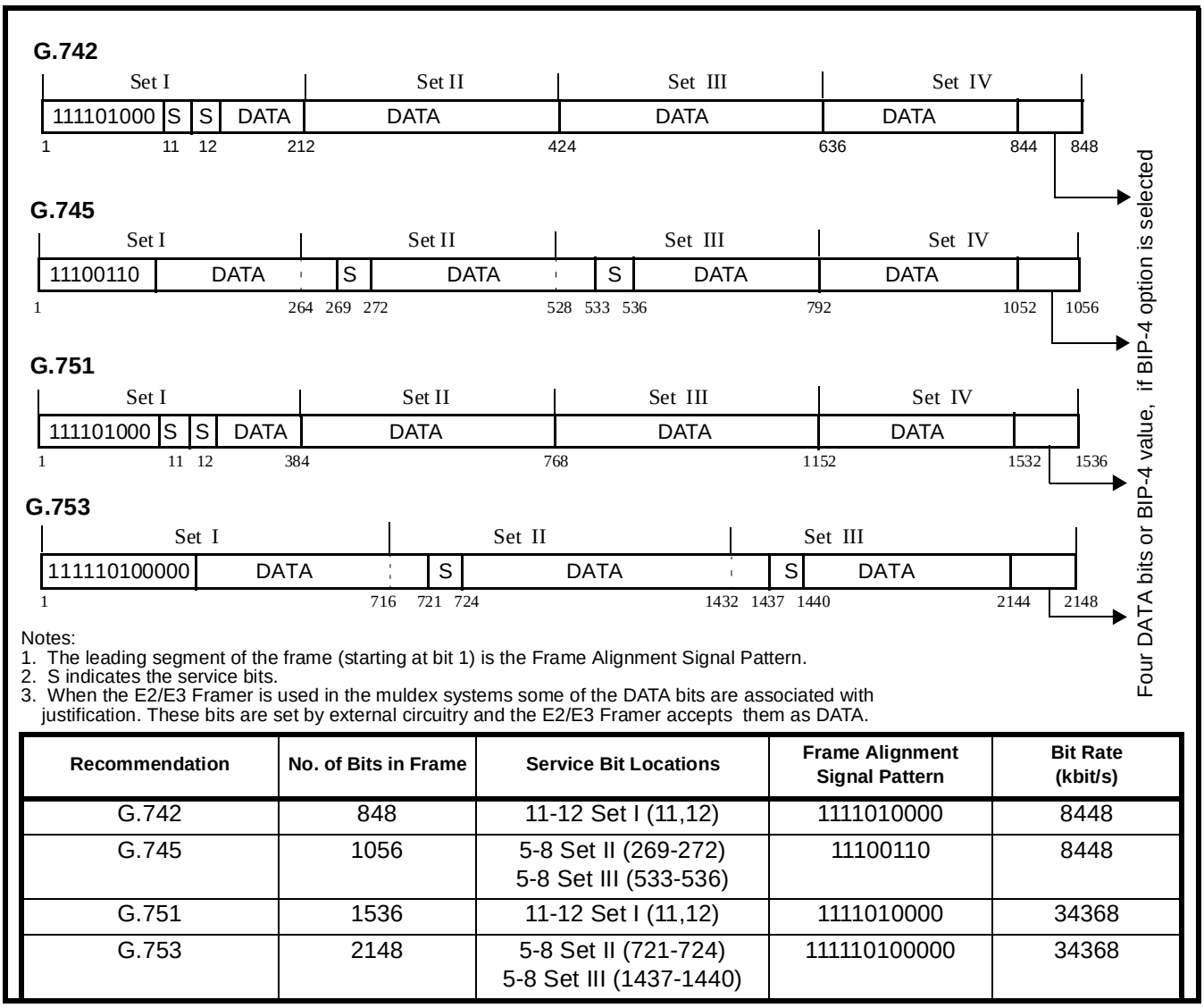
The MT90732 is a multi-mode framing device that frames the user data in E2/E3 format accordingly to ITU-T recommendations G.742, G.745, G.751 and G.753. In receive direction, the MT90732 synchronizes to the received E2/E3 frame, monitors and reports all performance and status reports, while providing the user data in nibble-parallel or bit-serial format. The block diagram of the E2/E3 Framer is shown in Figure 1.

The selection of the framing format (G.742, G.745, G.751 or G.753) is determined by control leads M1 and M0, or states written into the memory map by the microprocessor.

The clock extracted from receive line signal by a line interface circuit is used for receive operation. The external reference clock source is required for transmit operation unless loop timing feature ($\overline{\text{LPT}}$) is selected. When the loop timing feature is selected, the receive clock becomes the transmitted clock.

Line Side Interface

The selection of the signal format on the line side, dual rail or NRZ, is done by the NRZLINE input. When NRZLINE is tied low, the HDB3 Encoder/ Decoder is bypassed and the line side I/O signals have NRZ format. When HDB3 Encoder/Decoder is enabled by applying a high to NRZLINE input, the line side I/O are configured in dual rail format.



Notes:
1. The leading segment of the frame (starting at bit 1) is the Frame Alignment Signal Pattern.
2. S indicates the service bits.
3. When the E2/E3 Framer is used in the muldex systems some of the DATA bits are associated with justification. These bits are set by external circuitry and the E2/E3 Framer accepts them as DATA.

Recommendation	No. of Bits in Frame	Service Bit Locations	Frame Alignment Signal Pattern	Bit Rate (kbit/s)
G.742	848	11-12 Set I (11,12)	1111010000	8448
G.745	1056	5-8 Set II (269-272) 5-8 Set III (533-536)	11100110	8448
G.751	1536	11-12 Set I (11,12)	1111010000	34368
G.753	2148	5-8 Set II (721-724) 5-8 Set III (1437-1440)	111110100000	34368

Figure 3 - G.7xx Frame Contents Summary

The E2/E3 Framer receives data signal, dual rail (RP and RN) or NRZ (RDL), and clock signal (RCK/ RCKL), from the line interface circuit as shown in Figure 4.

The Framer Block performs frame alignment and alarm detection including Loss of Frame ($\overline{\text{RLOF}}$), Loss of receive Clock ($\overline{\text{RLOC}}$), AIS detection ($\overline{\text{RAIS}}$) and BIP-4 (Bit Interleaved Parity-4) detection (BIP-4E) when this feature is enabled in the nibble-parallel mode. Loss of clock is detected whether the clock is stuck high or low. A framing error (FE) output is also provided to indicate when any of the framing bits in the selected G. 7xx frame are in error.

Loss of receive Clock or Frame normally causes AIS to be inserted into the terminal side receive data stream. However, for some applications, receive data is required on the terminal side regardless of frame alignment. The disable AIS ($\overline{\text{DAIS}}$) control lead permits the E2/E3 Framer to provide receive data in the presence of Loss of Frame. The insertion of Alarm Indication Signal into the line side transmit data stream is controlled by $\overline{\text{TAIS}}$ input or control bit (TAIS) in the memory map.

In the dual rail mode, the HDB3 coding violation errors are detected in the HDB3 Decoder Block and are indicated on the signal lead CV as pulses. Coding violation errors are also counted in an 8-bit saturating counter accessed by the microprocessor through the memory map. A coding violation is not part of the standard HDB3 zero-substitution code, and can occur because of noise or other impairments on the line.

In the transmit direction, the line side interface consists of a data signal, dual rail (TP and TN) or NRZ (TDL), and a clock signal (TCK/TCKL). In the dual rail mode, the TCK clock may be inverted by setting $\overline{\text{TCLINV}}$ low.

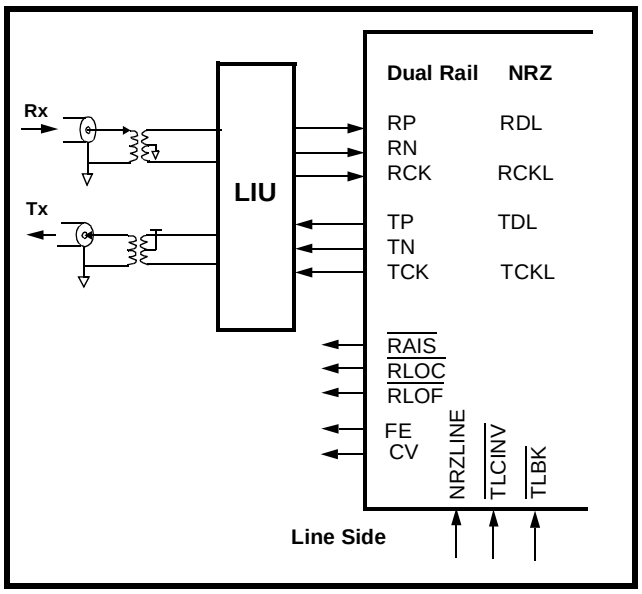


Figure 4 - Line Side Interface

When terminal loopback is enabled (TLBK), line output is internally looped to line input while line side receive signal is ignored.

Terminal Side Interface

The E2/E3 Framer terminal side provides either a bit-serial or a nibble-parallel interface. The interface is selected by an SER input or by a control bit in the memory map.

Bit-Serial Interface

In the receive direction, the bit-serial interface consists of the following signals: a data output signal (RSD), a clock output signal (RSC), a receive clock gapped output signal (RCG), and a framing pulse (RSF). The data signal consists of the all bits in the frame, including framing and service bits. The receive clock gapped signal (RCG) is low during the framing and service bit times and high during the rest of the period in a frame. This clock together with RSC and RSF can be used by external circuitry for extracting user data from RSD.

In the transmit direction, the bit-serial interface consists of: a data input signal (XSD), a clock input signal (XCK), and a framing pulse (XSF). The data input signal must consist of all bits in the frame, including bits in the framing and service bit locations.

To facilitate transmit side multiplexing while operating in the bit-serial mode, the E2/E3 Framer provides a Transmit Reference Generator. The Transmit Reference Generator accepts an external 8.448 or 34.368 MHz clock signal (TCIN) and produces a clock out signal (TCOUT), a framing pulse (TFOUT), a clock gap signal (TCG), and a data signal (TDOUT). The data signal consists of all ones in place of framing bits and zeros elsewhere. The purpose of the transmit reference signals is to provide time-base necessary for external circuitry to insert user data into frame format acceptable for XSD input, as shown by Figure 5. It is recommended that XCK and XSF be derived from TCOUT and TFOUT.

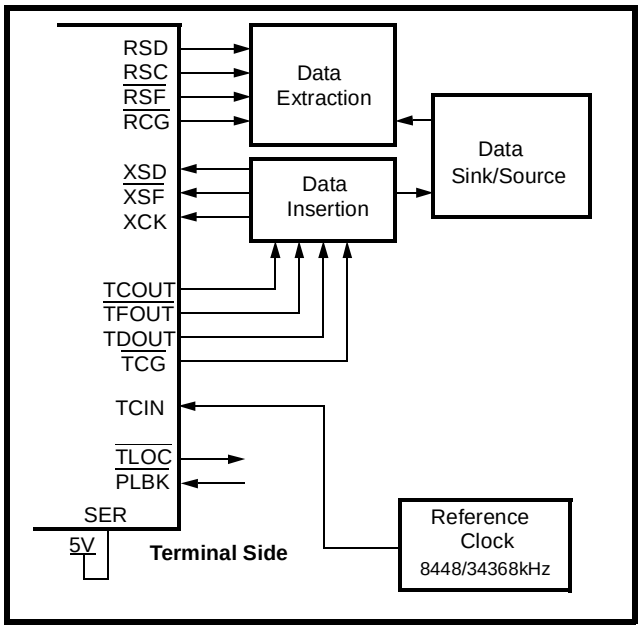


Figure 5 - Bit-Serial Interface

A low applied to PLBK enables a receive to transmit loopback on the terminal side in bit-serial mode only.

Nibble-Parallel Interface

In the receive direction, the nibble-parallel interface consists of the following signals: a data output signal having a nibble format (RNIB3 through RNIB0), a clock output signal (RNC), and a framing pulse (RNF). The RNIB3 bit corresponds to the first bit received in a four-bit bit-serial stream segment on the line side. The data output signal contains only the user data. The framing pattern, service bits and BIP-4 nibble are not provided at the interface. The receive nibble clock (RNC) is gapped during framing pattern, service bit and BIP-4 times, when BIP-4 option is selected.

In the transmit direction, the Input Block accepts the external reference clock through XCK input and produces a nibble output clock signal (XNC) and a framing output pulse (XNF). The data input signal has a nibble format (XNIB3 - XNIB0) and contains only the user data. The XNIB3 bit corresponds to the

first bit transmitted in a four-bit bit-serial stream segment. The transmit nibble clock (XNC) is stretched to accommodate the framing pattern, service bit and BIP-4 times, if BIP-4 option is selected. The XNC and XNF can be used for loading nibble data into the E2/E3 Framer directly from the Data Sink/Source, as shown by Figure 6.

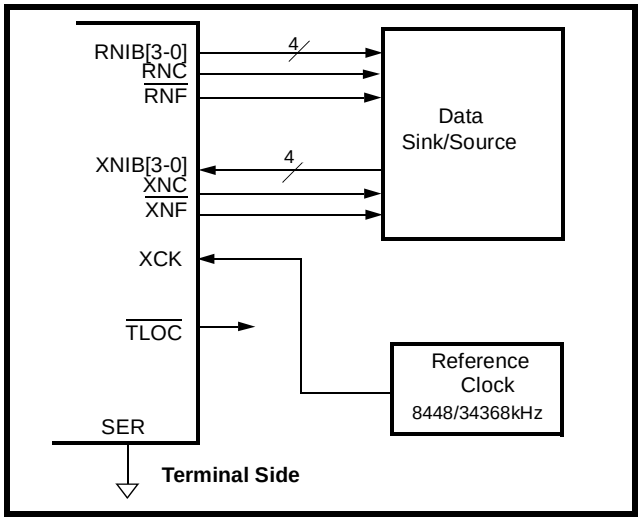


Figure 6 - Nibble-Parallel Interface

In the nibble-parallel mode the E2/E3 Framer provides BIP-4 as an additional method of error monitoring. The Bit Interleaved Parity check (BIP-4) can be activated either by control input BIP-4 or control bit in the memory map. When the BIP-4 option is selected, the nibble that contains calculated BIP-4 value is transmitted as the last four bits in the transmit frame format, as shown in Figure 3. The BIP-4 option makes data transport more reliable but reduces bandwidth available for user data, as shown by Table 1.

In the bit-serial and the nibble-parallel mode, the E2/E3 Framer detects loss of clock and TLOC goes low whenever the input clock is stuck high or low for 10 or more clock cycles.

Service Bit Interface

The service bits are listed in Figure 3. The receive service bit interface consists of the following signals: data output signal (ROD), clock output signal (ROC), and framing pulse (ROF). The clock signal (ROC) is gapped and is provided for clocking out the service bits. The service bit states are also written into E2/E3 Framer memory locations by the Interpreter Block. Memory locations can be read by the microprocessor.

The service bits to be transmitted are inserted into the frame format from either an external service bit interface or from memory map locations. The transmit service bit interface consists of the following signals: a data in signal (TOD), a clock output signal (TOC), and a framing pulse (TOF) output. The gapped clock TOC is used for clocking the transmit service data bits (TOD) in the E2/E3 Framer.

Microprocessor Interface

When the operation of E2/E3 Framer is managed by microprocessor the 8-byte memory map is used for control and performance monitoring. The microprocessor access the memory map through microprocessor interface.

The microprocessor interface consists of eight bidirectional data and address leads (AD7 - AD0), along with other microprocessor control leads, including a ready (RDY) output signal. The ready signal is used to resolve contention between microprocessor access and the internal read/write done by the E2/E3 Framer.

A high placed on the microprocessor control lead (MICRO) activates the microprocessor interface.When the microprocessor interface is selected, all the external control leads are disabled, except the loop timing (LPT), receive AIS disable (DAIS), force framing error (FORCEFE), transmit line clock invert (TLCINV), terminal loopback (TLBK), payload loopback (PLBK) and the line interface control leads (NRZLINE). The E2/E3 Framer provides pull-up resistors for the active low control leads.

The external alarm indications RLOF, RLOC, RAIS and TLOC are provided in the memory map, latched and unlatched.

Recommendation	BIP-4 On Number of Nibbles	BIP-4 On Nibble Rate k nibbles/s	BIP-4 Off Number of Nibbles	BIP-4 Off Nibble Rate k nibbles/s
G.742	208	2072.15	209	2082.11
G.745	259	2072.00	260	2080.00
G.751	380	8502.50	381	8524.80
G.753	531	8496.00	532	8512.00

Table 1 - Nibble Rates

Power Supply Distribution

The E2/E3 Framer has four supply pins that provide internal power distribution. A V_{DD} pin must be connected to a single +5 volt power supply, as shown in Figure 7.

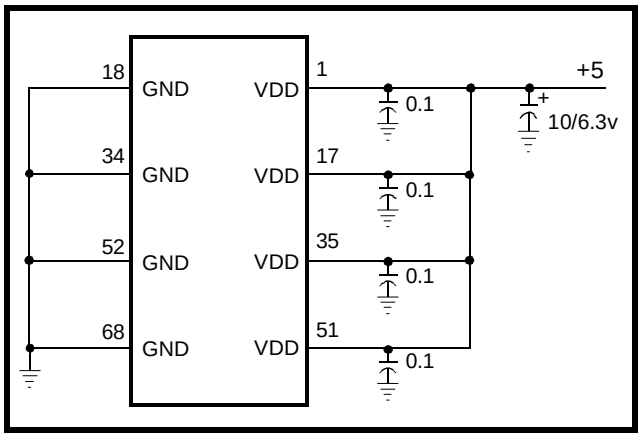


Figure 7 - E2/E3F Power Supply Connections

It is recommended that 0.1 microfarad ceramic disk capacitors be used for decoupling each of the supply pins, and that the decoupling capacitors be connected in close proximity to the E2/E3F. In addition, a 10 microfarad 6.3v tantalum capacitor should be connected between +5 volt and ground

Applications

Today's high capacity transmission networks are based on a hierarchy of digital multiplexed signals. At each level in the hierarchy, several bit streams, known as tributaries, are combined or separated by a multiplex/demultiplex equipment called a muldex. Muldex sites are connected by digital line systems making network.

The levels in the CEPT hierarchy are given in Table 2.

Level	Bit Rate [kbit/s]	Number of Voice Channels
E1	2048	30
E2	8448	120
E3	34368	480
E4	139264	1920

Table 2 - CEPT Hierarchy

The E2/E3 Framer frames user data either in E2 or E3 framing format. Framed E2/E3 data signal can be multiplexed with other tributaries into higher level digital signal (E3 or E4) and correctly reconstructed (demultiplexed) at the receive side of transmission system, as shown in Figure 8. The service bits, which are not utilized by the ITU-T recommendations, can be used for end-to-end monitoring of the transmission system.

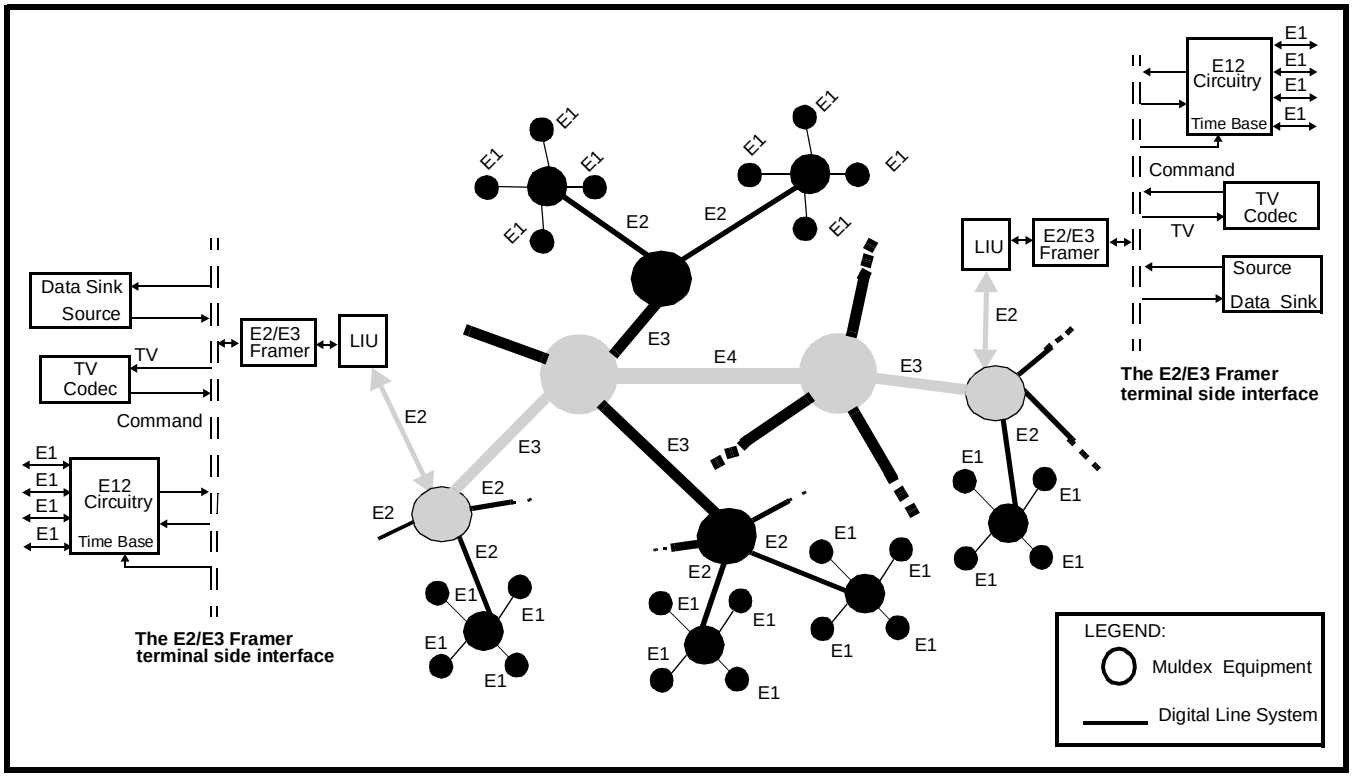


Figure 8 - The E2/E3 Framer Interfacing European High Capacity Network at 8.048 Mbit/s

One of the new services that requires wide band for transmission is video on demand. Although 70Mbit/s is needed for high quality PAL video signals, there is a variety of compression schemes which allow them to be carried over E3 system at 34 Mbit/s. The bandwidth required for Command channel is very low. The rate of 8 Mbit/s (E2) is enough for video telephone quality.

When it is used for wideband data or video transport applications the MT90732 can be used either in bit-serial or nibble-parallel mode. Nibble-parallel mode is recommended because it requires no glue logic for user data.

The E2/E3 Framer can also be used in more conventional role of building E12, E23 or E13 muldex systems. The E13 Muldex system, shown by Figure 9, multiplexes and demultiplexes sixteen independent E1 signals to and from an E3 signal. In this application the MT90732 operates in bit-serial mode. The Framer provides a time base (TCOUT) for multiplexing operation and allows comfortable access to E3 frame service bits.

The E13 muldex circuitry uses the timing signals, generated by Transmit Reference Generator, to identify the frame start (TFOUT) and determine the locations of framing and service bits (TDOUT, TCG) within the G.7XX frame.

The transmit E3 signal from the E13 circuitry consists of the entire frame. The Framer overwrites overhead bits, inserts valid framing pattern and provides access to all service bits.This data signal is then encoded by HDB-3 coder and sent out to the Line Interface Unit. The built in HDB3 codec allows E2/E3 Framer to be connected to variety of LIUs (with or without built-in HDB3 codec).

Receive E3 data signal along with clock, that is recovered by LIU, is connected to Framer on the line side. The E2/E3 Framer terminal side receive signal consists of all bits (RSD), including framing and service bits. The receive clock (RCK) is used for demultiplex functions while other timing signals (RCG, RSF) give information about frame start and overhead bit positions to E13 multiplexer circuitry. The received service bits can be read either by microprocessor through the memory map or external service bit interface.

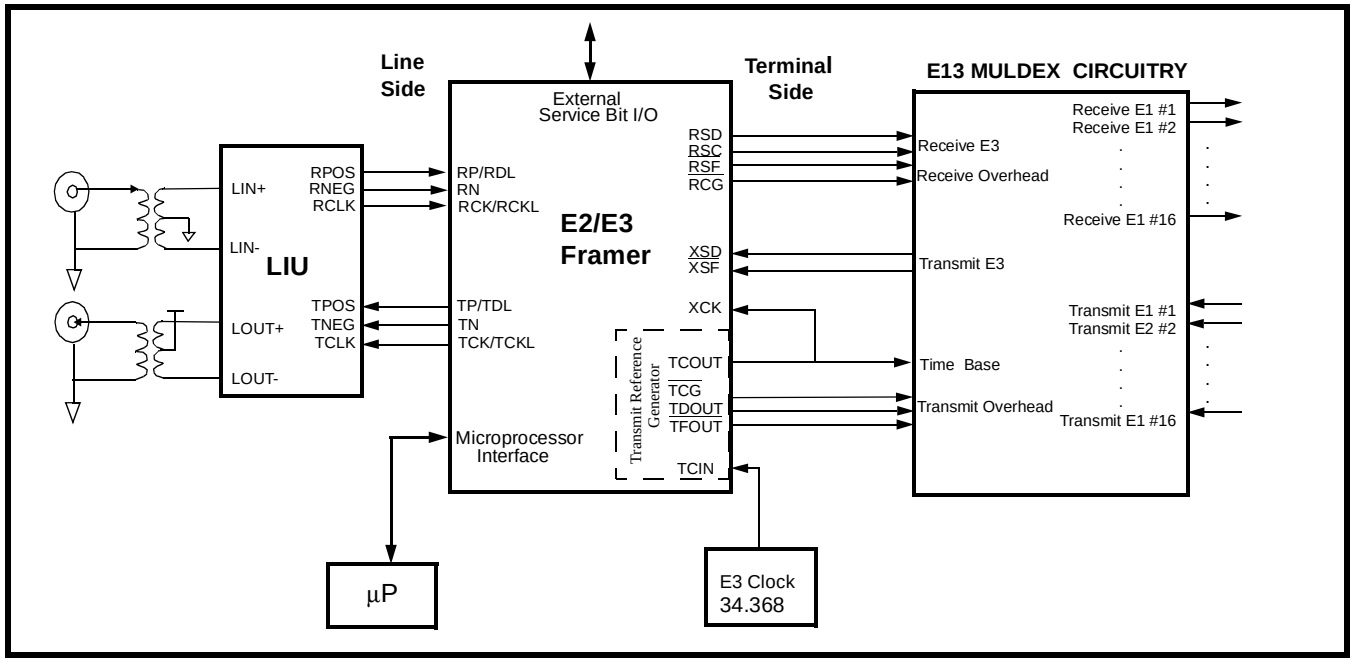


Figure 9 - E13 Muldex System

E2/E3 Framer Register Bit Map

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R/W	M1	M0	SER	TAIS	BIP-4	TLBK	PLBK	OHI/O
01	R	CODING VIOLATION COUNTER							
02	R	RLOF	RLOC	RAIS	TLOC	--	--	--	--
03	R	BIP-4 ERROR COUNTER							
04	R/W	BIP-4 ERROR MASK				--	--	--	FRSRCH
05	R	ROH5/11	ROH6/12	ROH7	ROH8	ROH5	ROH6	ROH7	ROH8
06	R/W	TOH5/11	TOH6/12	TOH7	TOH8	TOH5	TOH6	TOH7	TOH8
07	R(L)	RLOF	RLOC	RAIS	TLOC	--	--	--	--

*R/W: Read/write; R: Read only; R(L): Read only - latched register. Unused bit positions in R/W addresses should be written to "0".

E2/E3 FRAMER REGISTER MEMORY MAP DESCRIPTIONS

Control Registers

Address	Bit	Symbol	Description
00	6 7	M0 M1	**Mode Control:** The two controls select the operating rate of the E2/E3F according to the table given below: M1 M0 Recommendation Rate (kbit/s) 0 0 G.745 8448 0 1 G.742 8448 1 0 G.753 34368 1 1 G.751 34368
	5	SER	**Serial Interface:** A one written into this bit location selects the bit-serial interface for the terminal side I/O. A zero selects the terminal side nibble-parallel interface.
	4	TAIS	**Transmit Alarm Indication Signal:** A one written into this bit location causes an all ones unframed signal (AIS) to be sent in place of a G.7XX frame format on the line side.
	3	BIP-4	**Bit Interleaved Parity-4 Alarm:** A one written into this location enables the BIP-4 function. In the transmit direction, the BIP-4 is calculated for data nibbles only, and is sent as the last four bits in the transmitted frame format. In the receive direction, the BIP-4 is calculated for the data bits only and compared against the last four bits of the frame (BIP-4). An output indication (BIP-4E) occurs when one or more columns do not match. At the terminal interface, the transmit and receive nibble clocks are gapped during the BIP-4 time.
	2	TLBK	**Terminal Loopback:** A one written into this location disables the receive line side input and causes the transmit line output to be looped back as the receive input. To avoid contention between the loopback control lead, which is not disabled in the microprocessor mode, and the memory map control bit, the following truth table is used. $\overline{\text{TLBK}}$ Control Lead — TLBK Microprocessor — Terminal Loopback Low — Don't Care — On High — 1 — On High — 0 — Off

Address	Bit	Symbol	Description
	1	PLBK	**Payload Loopback:** PLBK is valid only in the serial mode. A one written into this location disables the terminal side transmit data input, and causes the terminal receive data to be looped back as the transmit terminal data in the serial mode only. To avoid contention between the loopback control lead which is not disabled in the microprocessor mode, and the memory map control bit, the following truth table is used. $\overline{\text{PLBK}}$ Control Lead / PLBK Microprocessor / Payload Loopback Low / Don't Care / On High / 1 / On High / 0 / Off
00H	0	OHI/O	**Service (Overhead) Bit I/O Selection:** A one written into this location enables the external service bit interface (TOD). A zero written into this location disables the external service bit interface, and enables bits written into Address 06H to be inserted into transmit E2/E3 frame as a service bits.
01H	7-0		**Coding Violation Counter:** This saturating counter counts the number of illegal coding violations. Bit 7 is the most significant bit. The counter resets to zero upon completion of a microprocessor read cycle.
02H	7	RLOF	**Receive Loss of Frame (Unlatched):** An one occurs when frame cannot be detected in the following modes and conditions: **G.742:** RLOF occurs when four consecutive frames are lost. Recovery occurs when three consecutive frames are detected. The framing pattern is: 1111010000. **G.745**: RLOF occurs when five consecutive frames are lost. Recovery occurs when two consecutive frames are detected. The framing pattern is 11100110. **G.751** RLOF occurs when four consecutive frames are lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 1111010000. **G.753**: RLOF occurs when three consecutive frames are lost. Recovery occurs when three consecutive frames are detected. The framing pattern is: 111110100000.
	6	RLOC	**Receive Loss of Clock (Unlatched):** An one occurs when no transitions are detected in the received clock (RCK/RCKL) for 10 clock cycles. Recovery occurs on the first clock transition.
	5	RAIS	**Receive Alarm Indication Signal (Unlatched):** An one occurs when an all unframed ones (AIS) condition is detected in the receive data, including in the presence of a 10^{-5} error rate.
	4	TLOC	**Transmit Loss of Clock (Unlatched):** An one occurs when no transitions are detected in the transmit clock (XCK) for 10 clock cycles. Recovery occurs on the first clock transition.
	3-0		Not used.
03H	7-0		**BIP-4 Error Counter:** This saturating counter counts the number of BIP-4 errors that have occurred in the comparison between the received BIP-4 value and the calculated value. Bit 7 is the most significant bit. The counter resets to zero upon completion of a microprocessor read cycle. The count is valid in dual rail mode only.

Address	Bit	Symbol	Description
04H	7-4		**BIP-4 Error Mask:** A one written to one or more bits causes those BIP-4 values to be inverted from their calculated value, and transmitted continuously. Bit 7 represents the first BIP-4 value transmitted in the frame, while bit 4 represents the last BIP-4 value transmitted in the nibble in the frame. To stop the transmission of errors, the microprocessor must write zeros to the appropriate mask positions again.
	3-1		Not used.
	0	FRSRCH	**Frame Search:** A one written to this control bit causes one clock slip in the framer detection circuit, which forces framer out of frame intentionally and forces the frame to search for new valid frame. A zero must be written to this location before a subsequent frame search is issued.
05H	7-0	ROHn	**Receive Overhead (Service Bits):** ROH5/11 and ROH6/12 in bits 7 and 6 are the received bits which correspond to bits 11 and 12 in received G.742 and G.751 frame formats. ROH5/11 - ROH8 in bits 7-4 correspond to bits 5-8 in Set II in the G.745 and G.753 frame formats. ROH5-ROH8 in bits 3-0 correspond to bits 5-8 in Set III in the G.745 and G.753 frame formats.
06H	7-0	TOHn	**Transmit Overhead (Service Bits):** TOH5/11 and TOH6/12 in bits 7 and 6 correspond to bits 11 and 12 in the G.742 and G.751 frame formats. TOH5/11-TOH8 in bits 7-4 correspond to bits 5-8 in Set II in the G.745 and G.753 frame formats. TOH5-TOH8 in bits 3-0 correspond to bits 5-8 in Set III in the G.745 and G.753 frame formats. The transmission of the service bits in this location is enabled by writing a zero to bit 0 (OHI/O) in Adress 00H.
07H	7-4		**Latched Alarm Bits:** The bits in this location correspond to the bits in location 02H, except that the bits are latched on with an alarm. A microprocessor read cycle clears the latched bit positions. If an alarm remains active during a read cycle, the bit re-latches.
	3-0		Not used.

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Unit
1	Supply voltage	V_{DD}	-0.3	7.0	V
2	DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
3	Continuous power dissipation	P_C		1	Watts
4	Storage Temperature	T_S	-55	150	^oC

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Symbol	Min	Typ	Max	Unit
1	Supply Voltage	V_{DD}	4.75	5	5.25	V
2	Supply Current	I_{DD}			125	mA
3	Operating Temperature	T_A	-40		85	^oC

DC Electrical Characteristics

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	All Inputs. $4.75 \le V_{DD} \le 5.25$.
2	Input Low Voltage	V_{IL}			0.8	V	All Inputs. $4.75 \le V_{DD} \le 5.25$.
3	Input leakage current	I_{IL}		-70.0		µA	All Inputs.
4	Input capacitance	C_{IN}		4.0		pF	All Inputs except 36 to 43.
				7.1		pF	Inputs 36 to 43.
5	Output High Voltage	V_{OH}	2.4			V	All Outputs except 48*. V_{DD} = 4.75; I_{OH}.
6	Output Low Voltage	V_{OL}			0.5	V	All Outputs. V_{DD} = 4.75; I_{OL}.
7	Output Low Current	I_{OL}			-8.0	mA	All Outputs except 61 to 67 & 58.
					-4.0	mA	Outputs 61 to 67 and 58.
8	Output High Current	I_{OH}			8.0	mA	All Outputs except 61 to 67 & 58.
					4.0	mA	Outputs 61 to 67 and 58.
9	Rise Time	t_{RISE}		2.0		ns	Outputs 5 to 12, 25, 28 to 29, 31 to 33 and 59 to 60 . C_{LOAD}=15 pF.
				3.3		ns	Outputs 36 to 43. C_{LOAD}=15 pF.
				1.2		ns	Outputs 61 to 67 and 58. C_{LOAD}=15 pF.
10	Fall Time	t_{FALL}		1.9		ns	Outputs 5 to 12, 25, 28 to 29, 31 to 33 and 59 to 60. C_{LOAD}=15 pF.
				7.9		ns	Outputs 36 to 43. C_{LOAD}=15 pF.
				1.7		ns	Outputs 61 to 67 and 58. C_{LOAD}=15 pF.

Note: All Inputs have a 72K (nominal) internal pull-up resistor.
Note*: Pin 48 (RDY) is an open drain output.

AC Electrical Characteristics - Detailed timing diagrams for the MT90732 are illustrated in Figures 10 through 25, with values of the timing intervals preceding each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$ as applicable.

E2/E3 Line Side Receive NRZ Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	RCKL clock period	t_{CYC}	116.0/29.0			ns	
2	RCKL high time	t_{PWH}	46.0/12.1	59.2/14.6		ns	
3	RCKL low time	t_{PWL}	46.0/12.1	59.2/14.6		ns	
4	RDL set-up time to RCKL↑	t_{SU}	4.0/4.0			ns	
5	RDL hold time after RCKL↑	t_H	4.0/4.0			ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

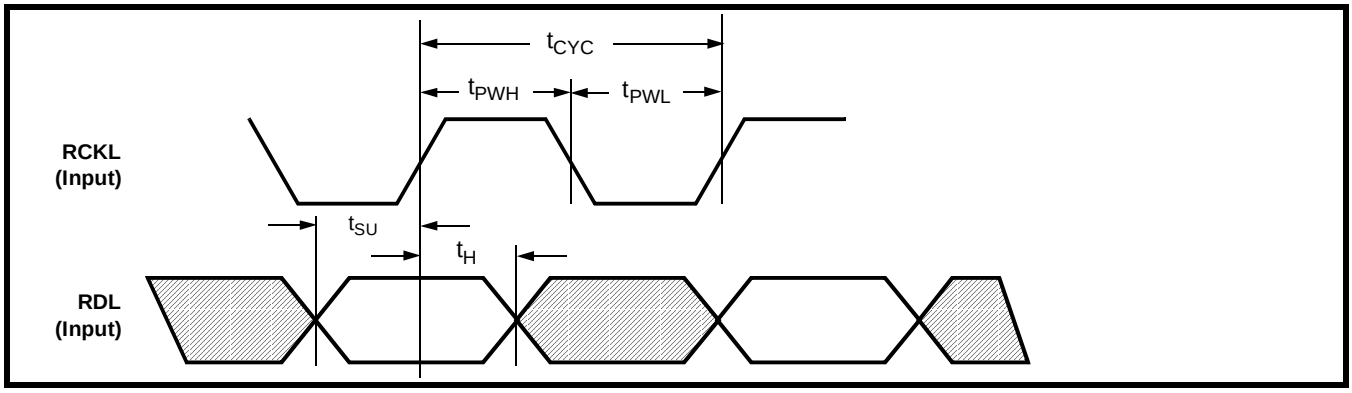


Figure 10 - Line Side Receive NRZ Timing

E2/E3 Line Side Transmit NRZ Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	TCKL clock period	t_{CYC}	118.4/29.1	118.4/29.1		ns	
2	TCKL high time	t_{PWH}	53.3/13.1			ns	
3	TCKL low time	t_{PWL}	53.3/13.1			ns	
4	TDL delay after TCKL ↓	t_D			7.0/7.0	ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

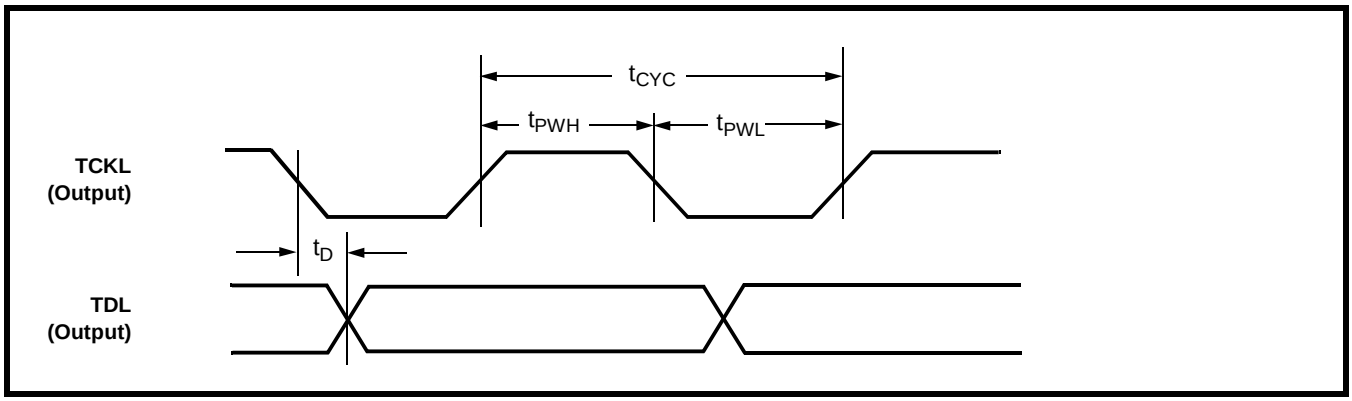


Figure 11 - Line Side Transmit NRZ Timing

E2/E3 Line Side Receive Dual Rail Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	RCK clock period	t_{CYC}	116.0/29.0			ns	
2	RCK high time	t_{PWH}	46.0/12.1	59.2/14.6		ns	
3	RCK low time	t_{PWL}	46.0/12.1	59.2/14.6		ns	
4	RP/RN set-up time to RCK↓	t_{SU}	4.0/4.0			ns	
5	RP/RN hold time after RCK↓	t_H	4.0/4.0			ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

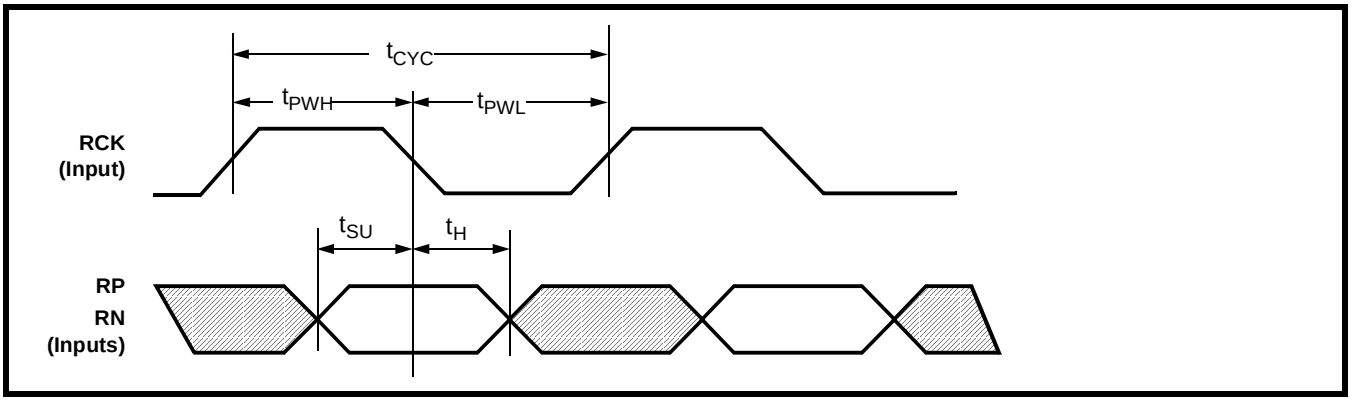


Figure 12 - Line Side Receive Dual Rail Timing

E2/E3 Line Side Transmit Dual Rail Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	TCK clock period	t_{CYC}	118.4/29.1	118.4/29.1		ns	
2	TCK high time	t_{PWH}	53.3/13.1			ns	
3	TCK low time	t_{PWL}	53.3/13.1			ns	
4	TP/TN delay after TCK↑	t_D			7.0/7.0	ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

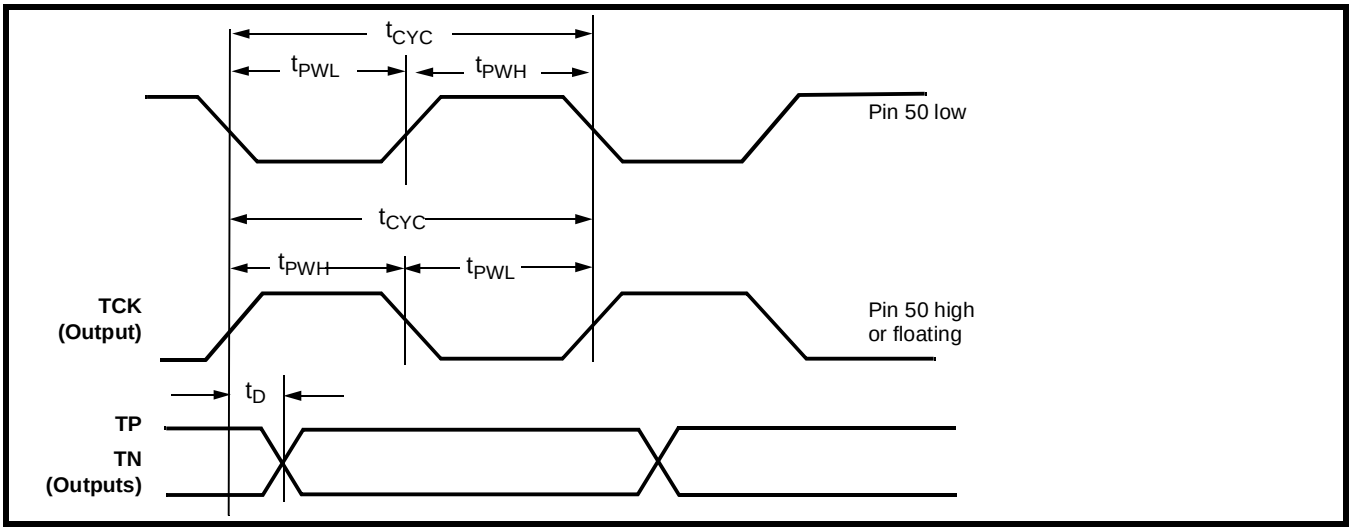


Figure 13 - Line Side Transmit Dual Rail Timing

E2/E3 Transmit Reference Generator Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	TCIN clock period	$t_{CYC(1)}$	118.4/29.1			ns	
2	TCIN high time	$t_{PWH(1)}$	53.3/13.1			ns	
3	TCIN low time	$t_{PWL(1)}$	53.3/13.1			ns	
4	TCOUT clock period	$t_{CYC(2)}$	118.4/29.1			ns	
5	TCOUT high time	$t_{PWH(2)}$	53.3/13.1			ns	
6	TCIN delay after TCOUT↑	$t_{D(1)}$			15.0/15.0	ns	
7	TDOUT, $\overline{\text{TFOUT}}$, $\overline{\text{TCG}}$ delay after TCOUT↑	$t_{D(2)}$			7.0/7.0	ns	
8	$\overline{\text{TFOUT}}$ pulse width	t_{PW}		$t_{CYC(1)}$		ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

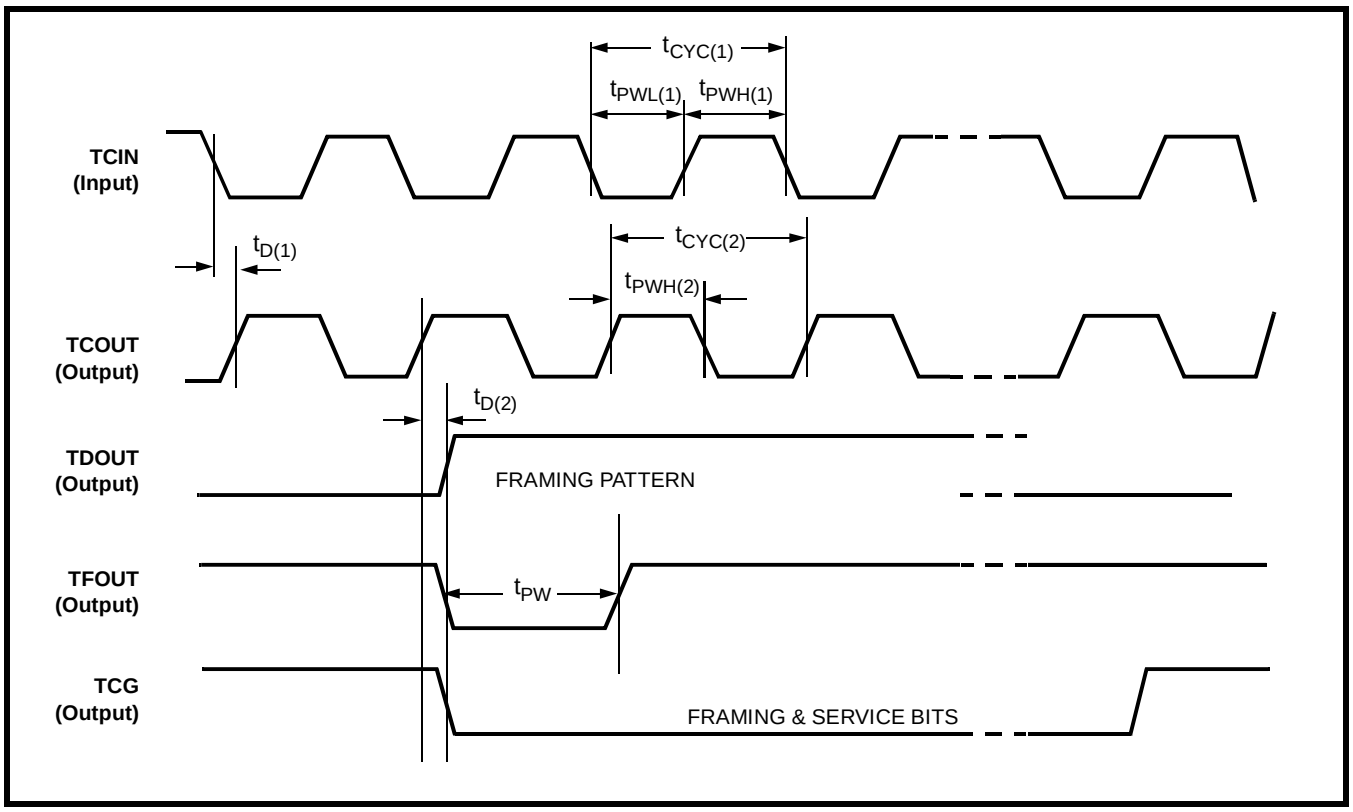
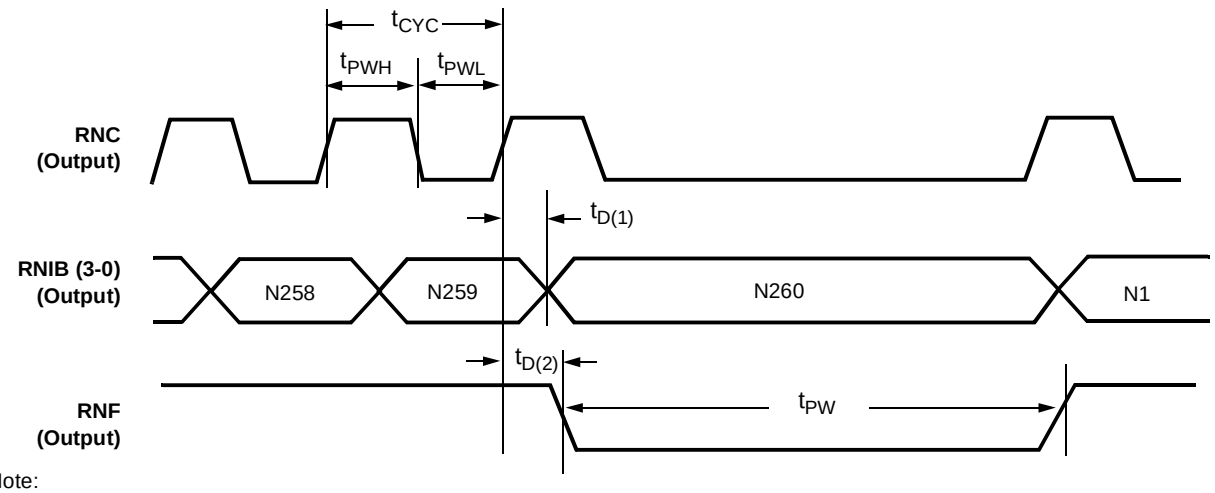


Figure 14 - Transmit Reference Generator Timing

E2/E3 Terminal Side Receive Nibble-Parallel Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	RNC clock period	t_{CYC}	473.0/116.4			ns	
2	RNC high time	t_{PWH}	213.0/52.4			ns	
3	RNC low time	t_{PWL}	213.0/52.4			ns	
4	RNIB delay after RNC↑	$t_{D(1)}$			7.0/7.0	ns	
5	$\overline{\text{RNF}}$ delay after RNC↑	$t_{D(2)}$			7.0/7.0	ns	
6	$\overline{\text{RNF}}$ pulse width	t_{PW}	947/291			ns	BIP-4 OFF

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).



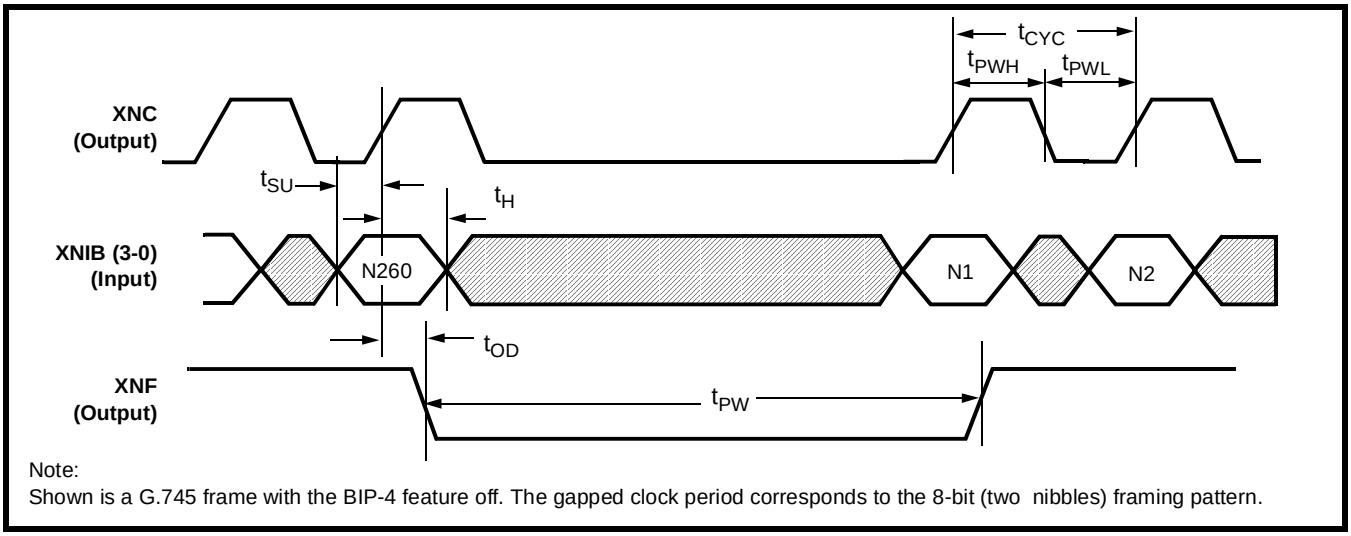
Note:
This waveform diagram shows a G.745 frame with the BIP-4 feature off. The gapped clock period corresponds to the 8-bit (two nibbles) framing pattern.

Figure 15 - Terminal Side Receive Nibble-Parallel Timing

E2/E3 Terminal Side Transmit Nibble-Parallel Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	XNC clock period	t_{CYC}	473.0/116.4			ns	
2	XNC high time	t_{PWH}	213.0/52.4			ns	
3	XNC low time	t_{PWL}	213.0/52.4			ns	
4	XNIB set-up time to XNC↑	t_{SU}	4.0/4.0			ns	
5	XNIB hold time after XNC↑	t_{H}	4.0/4.0			ns	
6	$\overline{\text{XNF}}$ output delay after XNC↑	t_{OD}	4.0/4.0			ns	
7	$\overline{\text{XNF}}$ pulse width	t_{PW}	947/291			ns	BIP-4 OFF

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).



Note:
Shown is a G.745 frame with the BIP-4 feature off. The gapped clock period corresponds to the 8-bit (two nibbles) framing pattern.

Figure 16. Terminal Side Transmit Nibble-Parallel Timing

E2/E3 Terminal Side Receive Bit-Serial Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	RSC clock period	t_{CYC}	116.0/29.0	118.4/29.1		ns	
2	RSC high time	t_{PWH}	46.0/11.5			ns	
3	RSC low time	t_{PWL}	46.0/11.5			ns	
4	RSD, $\overline{RCG}$, $\overline{RSF}$ delay after RSC↑	t_D			7.0/7.0	ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

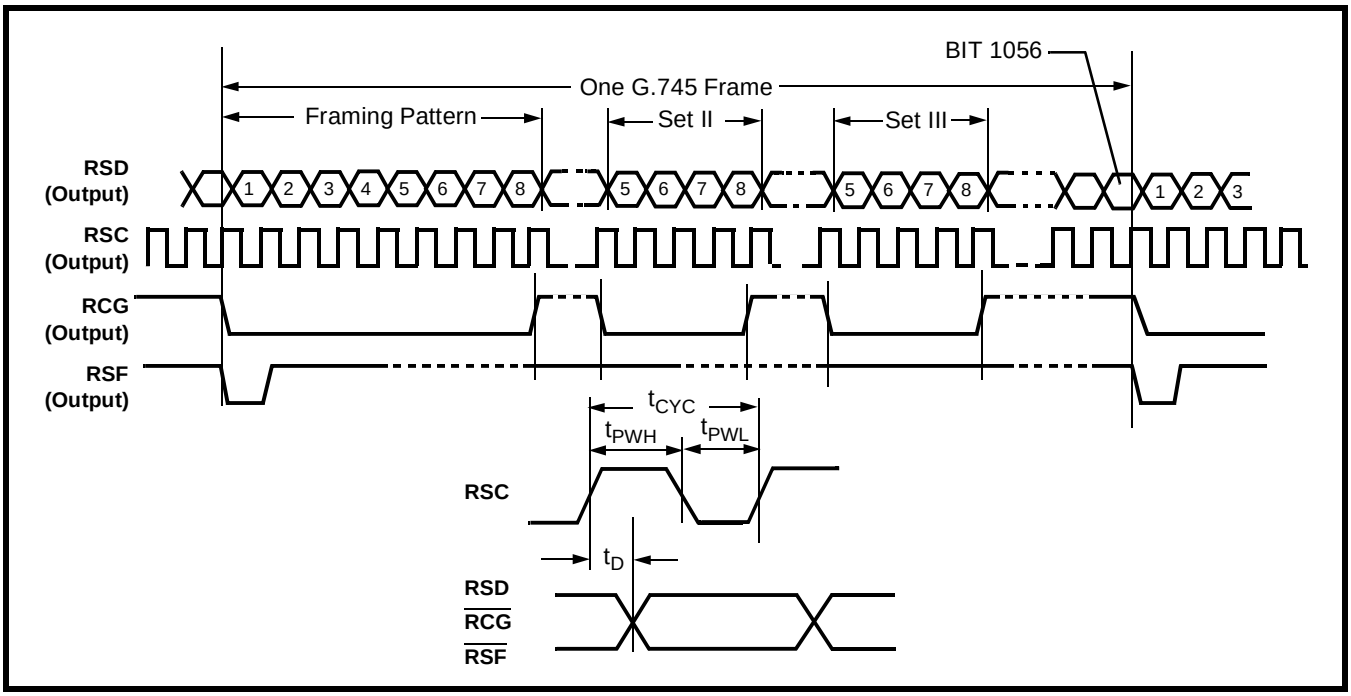


Figure 17- Terminal Side Receive Bit-Serial Timing

E2/E3 Terminal Side Transmit Bit-Serial Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	XCK clock period	t_{CYC}	118.4/29.1			ns	
2	XCK high time	t_{PWH}	53.3/13.1			ns	
3	XCK low time	t_{PWL}	53.3/13.1			ns	
4	XSD, $\overline{XSF}$ set-up time to XCK↓	t_{SU}	4.0/4.0			ns	
5	XSD, $\overline{XSF}$ hold time after XCK↓	t_H	4.0/4.0			ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

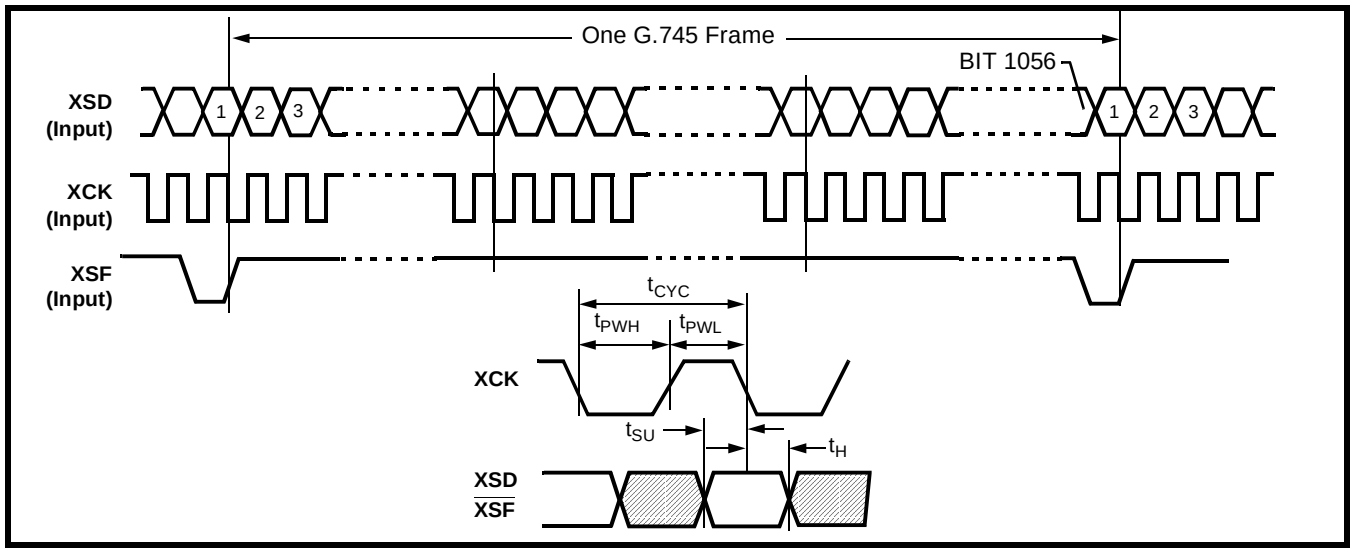


Figure 18 - Terminal Side Transmit Bit-Serial Timing

G.742 (E2)/G.751(E3) Service Bit Receive Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	ROC clock period	t_{CYC}	116.0/29.0	118.4/29.1		ns	
2	ROC high time	t_{PWH}	46.0/11.0			ns	
3	ROC low time	t_{PWL}	46.0/11.0			ns	
4	ROF pulse width	t_{PW}	46.0/11.0			ns	
5	ROD delay after ROC↑	t_D			7.0/7.0	ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

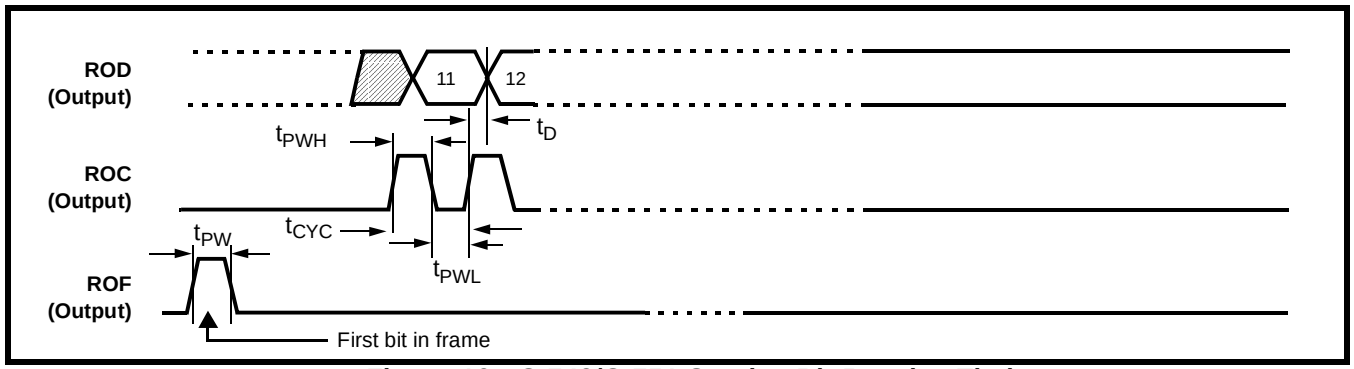


Figure 19 - G.742/G.751 Service Bit Receive Timing

G.745 (E2)/G.753 (E3) Service Bit Receive Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	ROC clock period	t_{CYC}	116.0/29.0	118.4/29.1		ns	
2	ROC high time	t_{PWH}	46.0/11.0			ns	
3	ROC low time	t_{PWL}	46.0/11.0			ns	
4	ROF pulse width	t_{PW}	46.0/11.0			ns	
5	ROD delay after ROC↑	t_D			7.0/7.0	ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

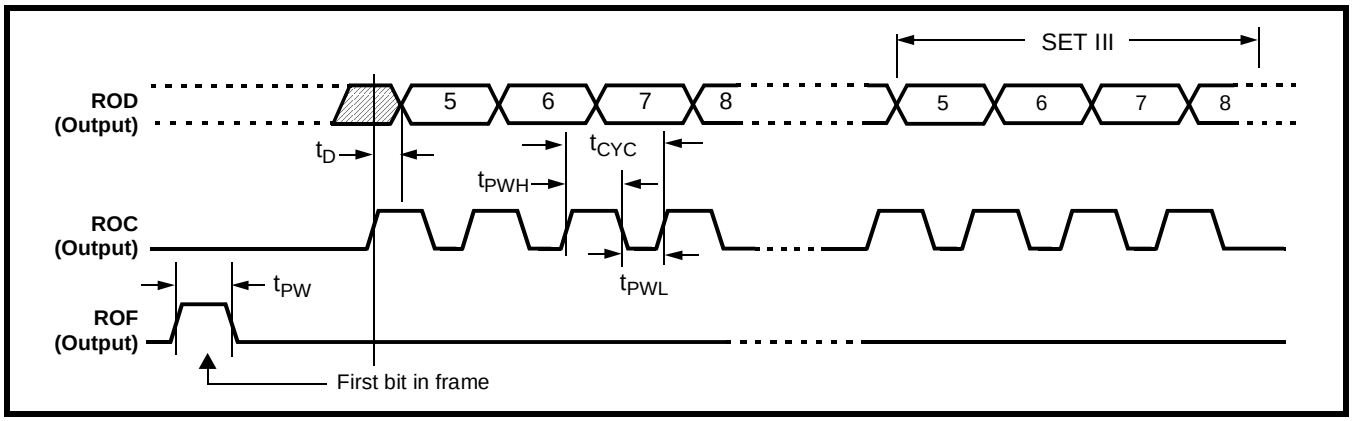


Figure 20 - G.745/G.753 Service Bit Receive Timing

G.742(E2)/G.751(E3) Service Bit Transmit Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	TOC clock period	t_{CYC}	118.4/29.1			ns	
2	TOC high time	t_{PWH}	53.3/13.1			ns	
3	TOC low time	t_{PWL}	53.3/13.1			ns	
4	TOF pulse width	t_{PW}	46.0/11.0			ns	
5	TOD set-up time to TOC↑	t_{SU}	4.0/4.0			ns	
6	TOD hold time after TOC↑	t_H	4.0/4.0			ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

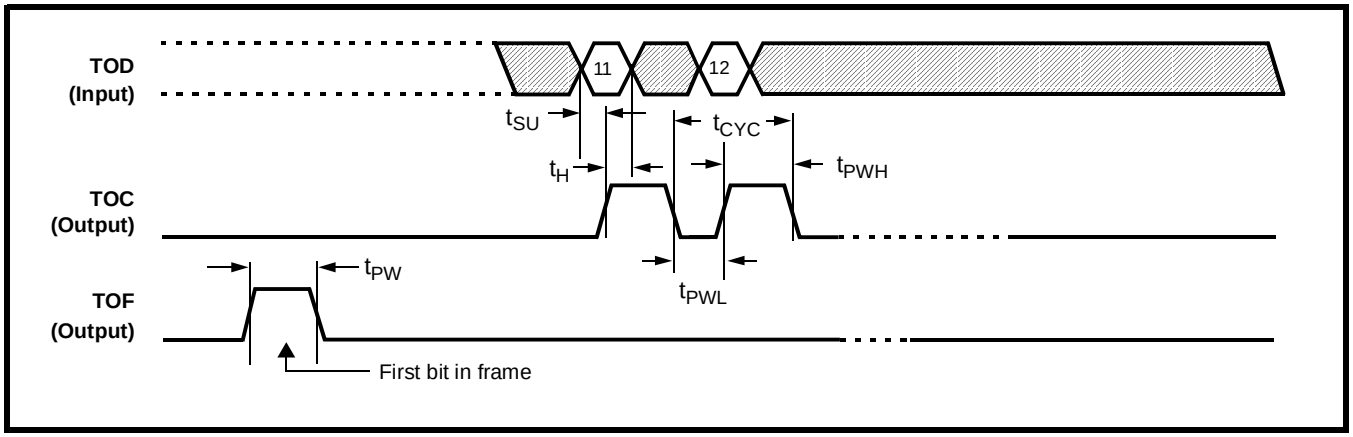


Figure 21 - G.742/G.751 Service Bit Transmit Timing

G.745(E2)/G.753(E3) Service Bit Transmit Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	TOC clock period	t_{CYC}	118.4/29.1			ns	
2	TOC high time	t_{PWH}	53.3/13.1			ns	
3	TOC low time	t_{PWL}	53.3/13.1			ns	
4	TOF pulse width	t_{PW}	46.0/11.0			ns	
5	TOD set-up time to TOC↑	t_{SU}	4.0/4.0			ns	
6	TOD hold time after TOC↑	t_H	4.0/4.0			ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

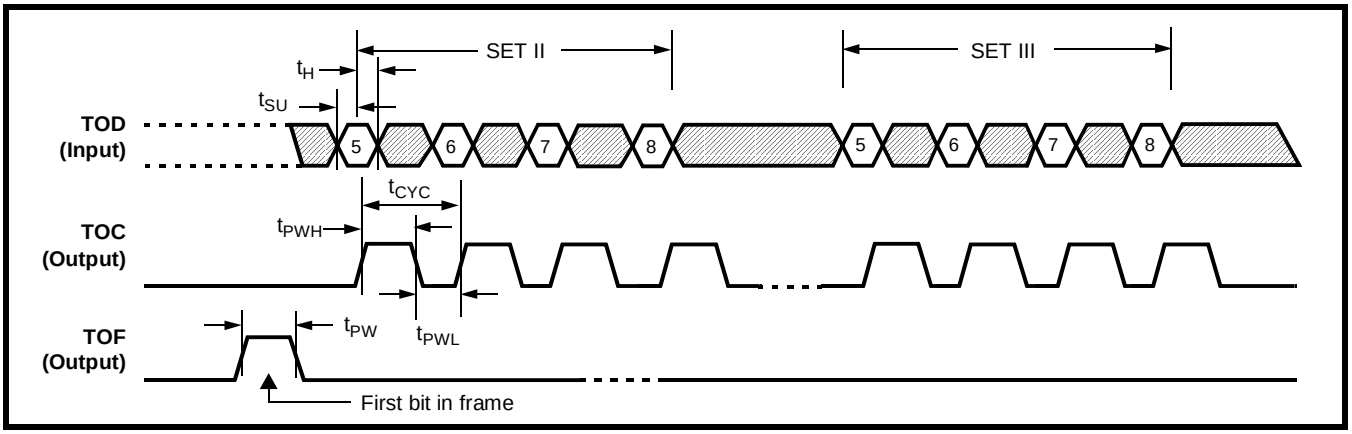


Figure 22 - G.745/G.753 Service Bit Transmit Timing

E2/E3 BIP-4 Error Timing

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	RCK/RCKL high time	$t_{PWH(1)}$	46.0/12.1	59.2/14.6		ns	
2	RCK/RCKL low time	t_{PWL}	46.0/12.1	59.2/14.6		ns	
3	BIP-4E delay after RCK/RCKL↓	t_D			7.0/7.0	ns	
4	BIP-4E high time	$t_{PWH(2)}$	46.0/11.0			ns	

Note: the above table contains timing values for both bit rates, 8448 kbit/s (E2) and 34368 kbit/s (E3), separated by a slash (/).

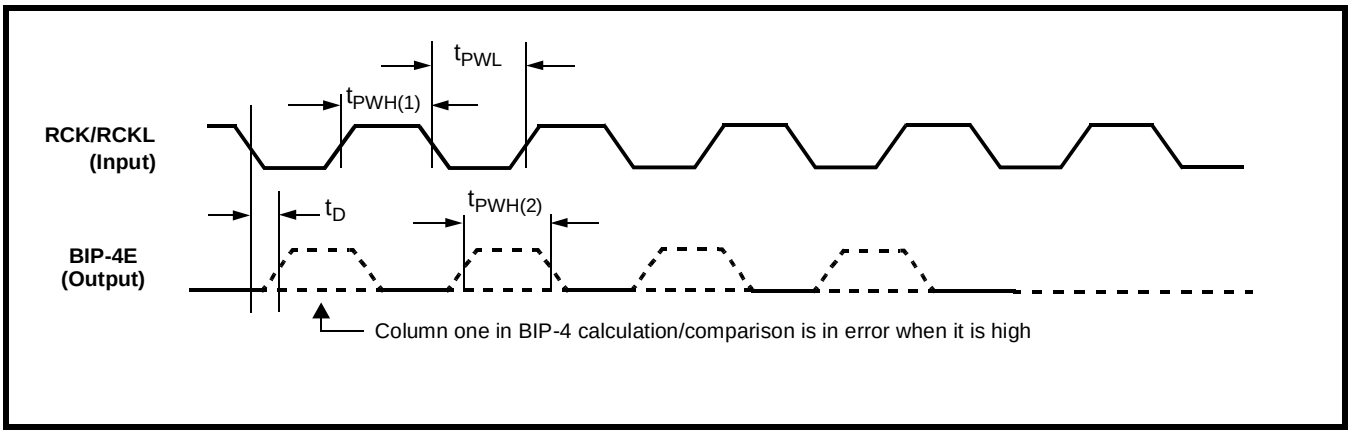


Figure 23 - BIP-4 Error Timing

Microprocessor Read Cycle

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	ALE pulse width	$t_{PW(1)}$	20.0			ns	
2	ALE wait time after $\overline{RD}\uparrow$	$t_{W(1)}$	25.0			ns	
3	Address set-up time to ALE$\downarrow$	$t_{SU(1)}$	10.0			ns	
4	Address hold time after ALE$\downarrow$	$t_{H(1)}$	10.0			ns	
5	Address hold time after $\overline{RD}\downarrow$	$t_{H(2)}$	0.0			ns	
6	Data output delay (to tristate) after $\overline{RD}\uparrow$	$t_{OD(1)}$	10.0		90.0	ns	
7	Data output delay after $\overline{RD}\downarrow$	$t_{OD(2)}$			$2 * t_{CYC} + 20$	ns	(Notes 2 & 4)
8	$\overline{SEL}$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	20.0			ns	
9	$\overline{RD}$ pulse width	$t_{PW(2)}$	$2 * t_{CYC} + 3.0$			ns	(Notes 2 & 3)
10	$\overline{RD}$ wait time after ALE$\downarrow$	$t_{W(2)}$	20.0			ns	
11	$\overline{SEL}$ wait time after $\overline{RD}\uparrow$	$t_{W(3)}$	5.0			ns	
12	RDY delay after $\overline{RD}\downarrow$	t_D	3.0		t_{CYC} +12	ns	(Note 2)
13	RDY pulse width	$t_{PW(3)}$	t_{CYC}		$3 * t_{CYC}$	ns	(Notes 2 & 4)
14	$\overline{RD}$ wait time after RDY$\uparrow$	$t_{W(4)}$	0.0			ns	
15	$\overline{SEL}$ wait time after ALE$\downarrow$	$t_{W(5)}$	10.0			ns	

Note 1: Open drain rise time is dependent upon external load resistance (R) and capacitance (C).
Note 2: t_{CYC} is period of the line interface clock used (E2 or E3).
Note 3: At least 10 clock cycles of XCK must occur after Reset before a Read cycle is valid.
Note 4: Output data is valid when RDY is released from low level at the end of $t_{PW(3)}$.

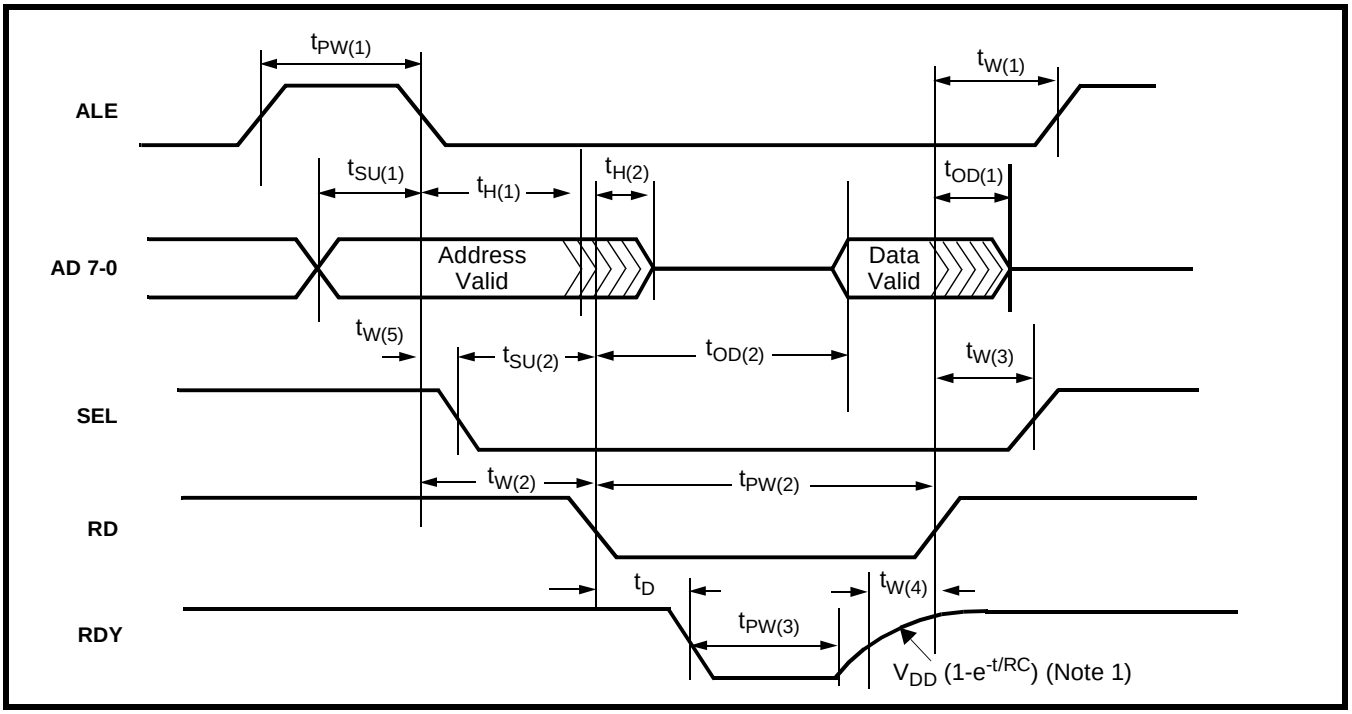


Figure 24 - Microprocessor Read Cycle

Microprocessor Write Cycle

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	ALE pulse width	$t_{PW(1)}$	20.0			ns	
2	ALE wait time after $\overline{WR}\uparrow$	$t_{W(1)}$	25.0			ns	
3	Address set-up time to ALE$\downarrow$	$t_{SU(1)}$	10.0			ns	
4	Address hold time after ALE$\downarrow$	$t_{H(1)}$	10.0			ns	
5	Data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	10.0			ns	
6	Data set-up time to $\overline{WR}\uparrow$	$t_{SU(2)}$	10.0			ns	
7	$\overline{WR}$ pulse width	$t_{PW(2)}$	$2 * t_{CYC} + 3.0$			ns	(Notes 2 & 3)
8	$\overline{WR}$ wait time after ALE$\downarrow$	$t_{W(2)}$	20.0			ns	
9	$\overline{SEL}$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	20.00			ns	
10	$\overline{SEL}$ wait time after $\overline{WR}\uparrow$	$t_{W(3)}$	5.0			ns	
11	RDY delay time after $\overline{WR}\downarrow$	t_D	3.0		t_{CYC} +12	ns	(Note 2)
12	RDY pulse width	$t_{PW(3)}$	$2 * t_{CYC}$		$3 * t_{CYC}$	ns	(Note 2)
13	$\overline{WR}$ wait time after RDY$\uparrow$	$t_{W(4)}$	0.0			ns	
14	$\overline{SEL}$ wait time after ALE$\downarrow$	$t_{W(5)}$	10.0			ns	

Note 1: Open drain rise time is dependent upon external load resistance (R) and capacitance(C).
Note 2: t_{CYC} is period of the line interface clock used (E2 or E3).
Note 3: At least 10 clock cycles of XCK must occur after Reset before a Write cycle is valid.

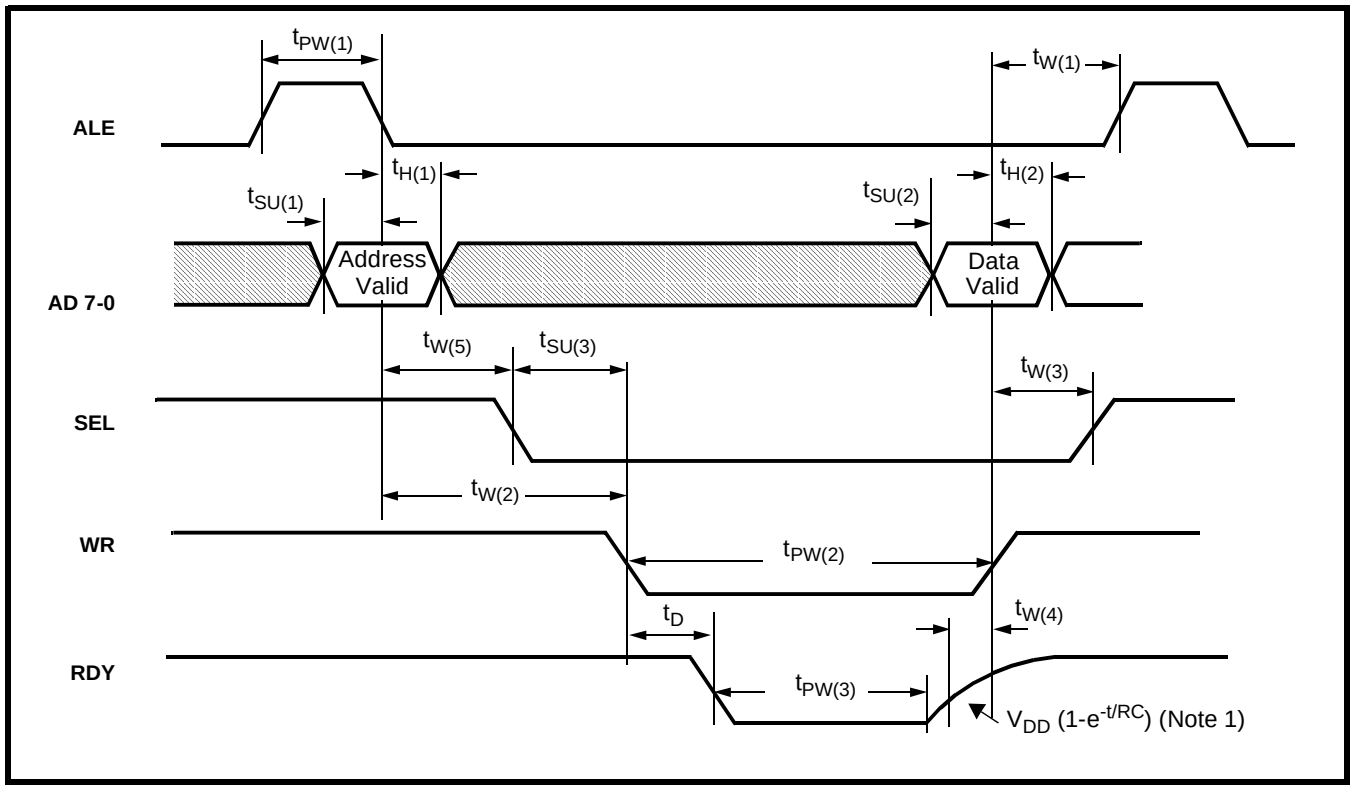
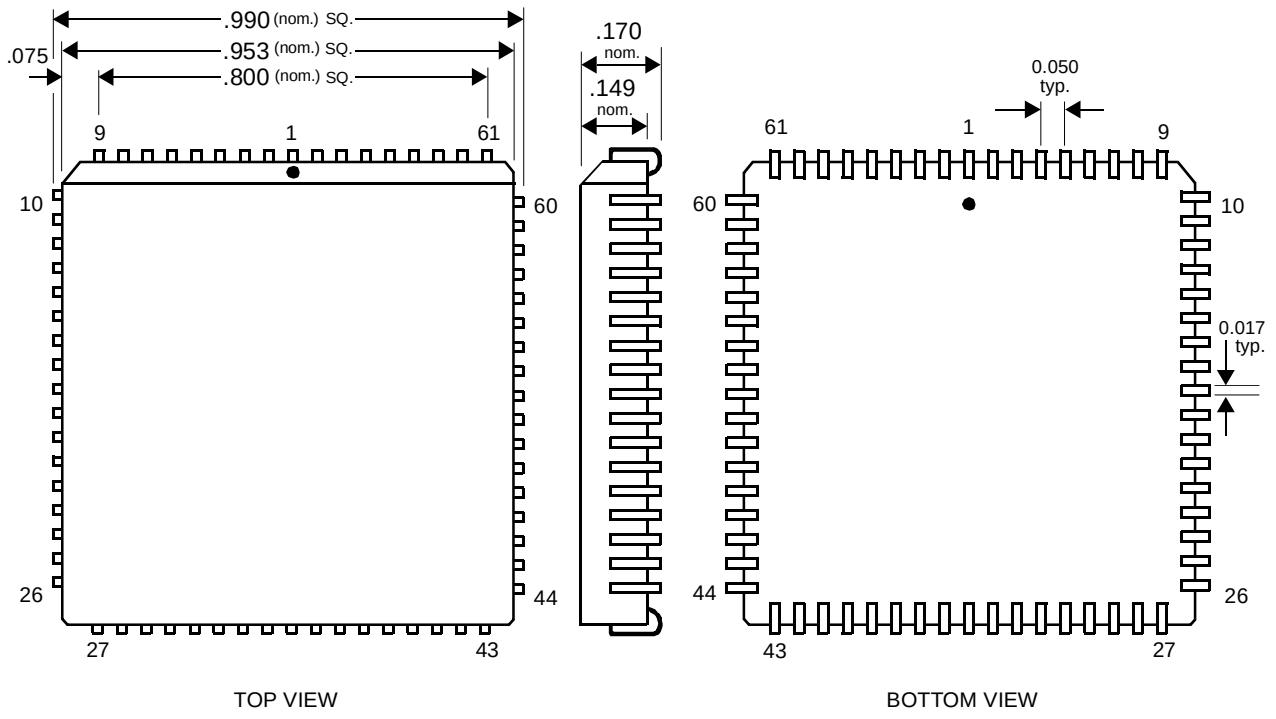


Figure 25 - Microprocessor Write Cycle



(JEDEC Outline MO-047AE)

Note: All dimensions shown are in inches. All dimensions and notes for the specified JEDEC outline apply.

Figure 26 - Mechanical Drawing

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