MT9075
E1 Single Chip Transceiver
Advance Information

ISSUE 1 June 1996

Features

- Combined PCM 30 framer, Line Interface Unit (LIU) and link controller in a 68 pin PLCC or 100 pin MQFP package
- Selectable rate data link access with optional S_a bits HDLC controller (HDLC0) and channel 16 HDLC controller (HDLC1)
- Enhanced performance monitoring and programmable error insertion functions
- Low jitter DPLL clock generation for master, slave or free-run mode
- Two-frame receive elastic buffer with controlled slip direction indication and 26 channel hysteresis
- Selectable transmit or receive jitter attenuator
- Intel or Motorola non-multiplexed parallel microprocessor interface
- CRC-4 updating algorithm for intermediate path points of a message-based data link application
- ST-BUS/GCI 2.048 Mbit/s backplane bus for both data and signalling

Applications

- E1 add/drop multiplexers and channel banks
- CO and PBX equipment interfaces
- Primary Rate ISDN nodes
- Digital Cross-connect Systems (DCS)

Ordering Information

MT9075AP	68 Pin	PLCC
MT9075AL	100 Pin	MQFP

0^o to 70^oC

Description

The MT9075 is a single chip device which integrates an advanced PCM 30 framer with on-board Line Interface Unit (LIU).

The framer interfaces to a 2.048 Mbit/s backplane and provides selectable rate data link access with optional HDLC controllers for S_a bits and channel 16. The LIU interfaces the frame functions to the PCM 30 transformer-isolated four wire line.

The MT9075 meets or supports the latest ITU-T Recommendations including G.704, G.706, G.732, G.775, G.796, G.823 for PCM 30, and I.431 for ISDN primary rate. It also meets or supports ETSI ETS 300 011 and ETS 300 233 as well as BS 6450.

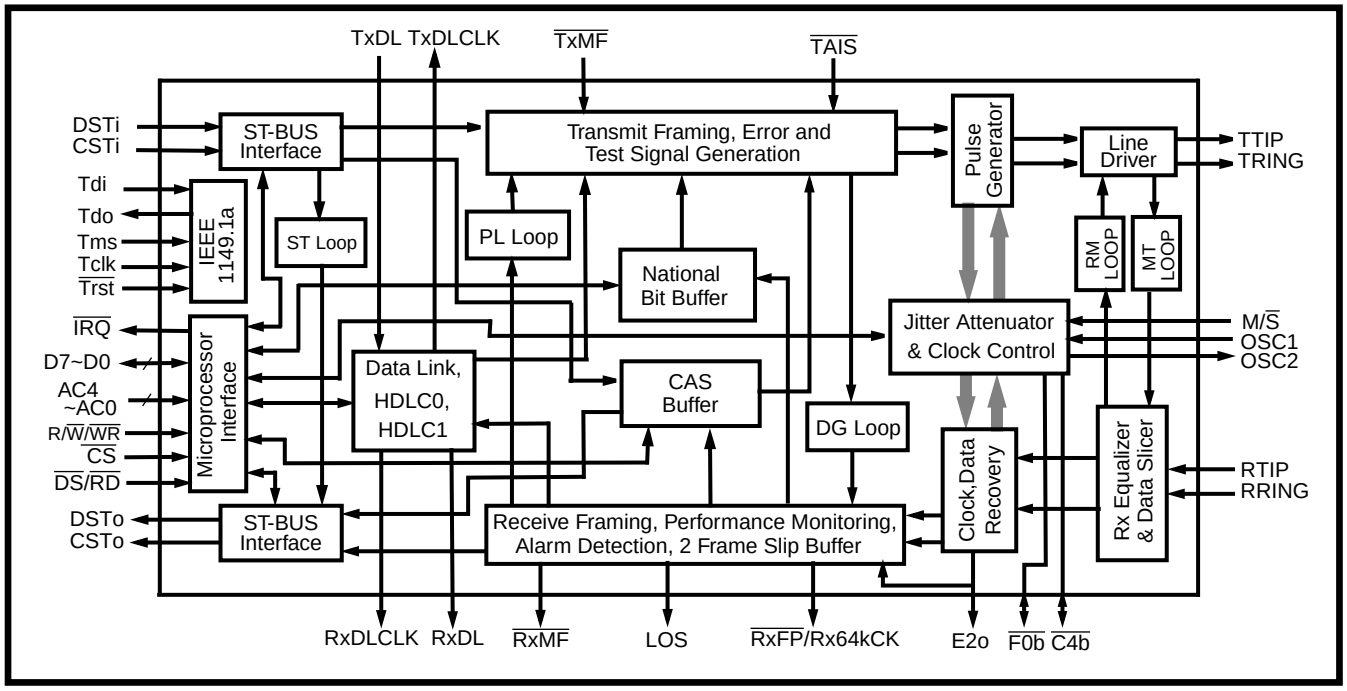
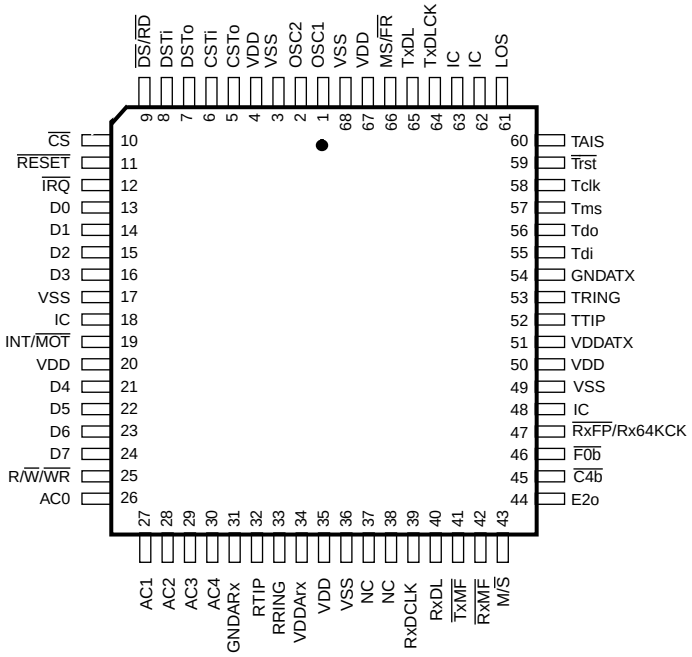
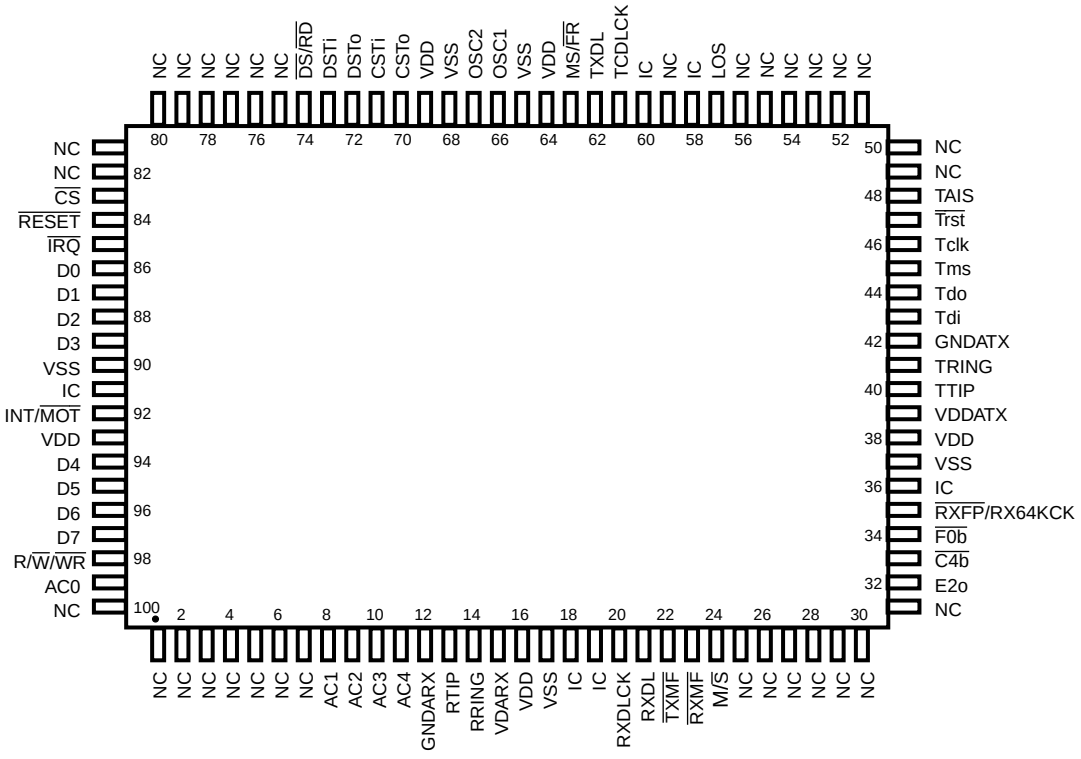


Figure 1 - Functional Block Diagram



68 PIN PLCC



100 PIN MQFP (JEDEC MO-112)

Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
PLCC	MQFP		
1	66	OSC1	**Oscillator Input.** Connect a 20.0 MHz crystal between OSC1 and OSC2. Not suitable for TTL compatible oscillator.
2	67	OSC2	**Oscillator Output.** Connect a 20.0 MHz crystal between OSC1 and OSC2. Not suitable for driving other devices.
3	68	V_{SS}	**Negative Power Supply (Input).** Digital ground.
4	69	V_{DD}	**Positive Power Supply (Input).** Digital supply (+5V ± 10%).
5	70	CSTo	**Control ST-BUS Output (Output).** CSTo carries one of the following two serial streams for CAS and CCS respectively: (i) A 2.048 Mbit/s ST-BUS status stream which contains the 30 receive signaling nibbles (ABCDZZZZ or ZZZZABCD). The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are tristated when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and tristated nibbles are reversed. (ii) A 64 kbit/s output when 64 Khz clear channel option is selected (page 01H, address 1AH, bit 0, 64KCCS =1) for channel 16.
6	71	CSTi	**Control ST-BUS Input (Input).** CSTi carries one of the following two serial streams for CAS and CCS respectively: (i) A 2.048 Mbit/s ST-BUS control stream which contains the 30 transmit signaling nibbles (ABCDXXXX or XXXXABCD) when RPSIG=0. When RPSIG=1 this pin has no function. The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are ignored when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and ignored nibbles is reversed. (ii) A 64 kbit/s input when 64 Khz clear channel option is selected (page 01H, address 1AH, bit 0, 64KCCS =1) for channel 16.
7	72	DSTo	**Data ST-BUS Output (Output).** A 2.048 Mbit/s serial stream which contains the 30 PCM or data channels received on the PCM 30 line.
8	73	DSTi	**Data ST-BUS Input (Input).** A 2.048 Mbit/s serial stream which contains the 30 PCM or data channels to be transmitted on the PCM 30 line.
9	74	$\overline{DS}/\overline{RD}$	**Data/Read Strobe (Input)**. In Motorola mode ($\overline{DS}$), this input is the active low data strobe of the processor interface. In Intel mode ($\overline{RD}$), this input is the active low read strobe of the processor interface.
10	83	$\overline{CS}$	**Chip Select (Input)**. This active low input enables the non-multiplexed parallel microprocessor interface of the MT9075. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
11	84	$\overline{RESET}$	**RESET (Input).** This active low input puts the MT9075 in a reset condition. $\overline{RESET}$ should be set to high for normal operation. The MT9075 should be reset after power-up, and the $\overline{RESET}$ pin must be held low for a minimum of 1000 nsec. to reset the device properly.

Pin Description (continued)

Pin #		Name	Description
PLCC	MQFP		
12	85	$\overline{\text{IRQ}}$	**Interrupt Request (Output).** A low on this output pin indicates that an interrupt request is presented. $\overline{\text{IRQ}}$ is an open drain output that should be connected to V_{DD} through a pull-up resistor. An active $\overline{\text{CS}}$ signal is not required for this pin to function.
13 - 16	86-89	D0 - D3	**Data 0 to Data 3 (Three-state I/O).** These signals with D4-D7 form the bidirectional data bus of the parallel processor interface (D0 is the least significant bit).
17	90	VSS	**Negative Power Supply (Input).** Digital ground.
18	91	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
19	92	INT/$\overline{\text{MOT}}$	**Intel / Motorola Mode Selection (Input).** A high on this pin configures the processor interface for Intel parallel non-multiplexed processors. A low configures the processor interface for Motorola parallel non-multiplexed processors.
20	93	VDD	**Positive Power Supply (Input).** Digital supply (+5V ± 10%).
21 - 24	94-97	D4 - D7	**Data 4 to Data 7 (Three-state I/O).** These signals with D0-D3 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit).
25	98	R/$\overline{\text{W}}$/$\overline{\text{WR}}$	**Read/Write / Write Strobe (Input).** For Motorola mode (R/$\overline{\text{W}}$), this input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{\text{W}}$ is high, the parallel processor is reading data from the MT9075. When low, the parallel processor is writing data to the MT9075. For Intel mode ($\overline{\text{WR}}$), this active low write strobe configures the data bus lines as output.
26 - 30	99, 8-11	AC0 - AC4	**Address/Control 0 to 4 (Inputs).** Address and control inputs for the non-multiplexed parallel processor interface. AC0 is the least significant input.
31	12	GNDARx	**Receive Analog Ground (Input).** Analog ground for the LIU receiver.
32	13	RTIP	**Receive TIP (Input).** Receive input for the PCM 30 AMI signal - must be transformer coupled.
33	14	RRING	**Receive RING (Input).** Receive input for the PCM 30 AMI signal - must be transformer coupled.
34	15	VDDARx	**Receive Analog Power Supply (Input).** Analog supply for the LIU receiver (+5V ± 10%).
35	16	VDD	**Positive Power Supply (Input).** Digital supply (+5V ± 10%).
36	17	VSS	**Negative Power Supply (Input).** Digital ground.
37	18	IC	**Internal Connection.** Must be left open for normal operation.
38	19	IC	**Internal Connection.** Must be left open for normal operation.
39	20	RxDLCLK	**Data Link Clock (Output)**. A gapped clock signal derived from a 2.048 Mbit/s clock, available for an external device to clock in DL data (RxDL) (at 4, 8, 12, 16 or 20 kHz) on the rising edge.
40	21	RxDL	**Receive Data Link (Output)**. A 2.048 Mbit/s data stream containing received line data after HDB3 decoding. This data is clocked out with the rising edge of E2o.
41	22	$\overline{\text{TxMF}}$	**Transmit Multiframe Boundary (Input)**. This active low input is used to set the transmit multiframe boundary (CAS or CRC multiframe). The MT9075 will generate its own multiframe if this pin is held high. This input is usually pulled high in most applications.

Pin Description (continued)

Pin #		Name	Description
PLCC	MQFP		
42	23	$\overline{\text{RxMF}}$	**Receive Multiframe Boundary (Output).** An output pulse delimiting the received multiframe boundary. The next frame output on the data stream (DSTo) is basic frame zero on the PCM 30 link. This receive multiframe signal can be related to either the receive CRC multiframe (page 01H, address 10H, bit 6, MFSEL=1) or the receive signalling multiframe (MFSEL=0).
43	24	M/$\overline{\text{S}}$	**Master / Slave Mode Selection (Input)**. If high, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be inputs; if low, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be outputs.
44	32	E2o	**2.048 MHz Extracted Clock (Output).** This clock is extracted from the received signal and it is used internally to clock in data received on RTIP and RRING.
45	33	$\overline{\text{C4b}}$	**4.096 MHz System Clock (Input/Output)**. $\overline{\text{C4b}}$ is the clock for the ST-BUS sections and transmit serial PCM data of the MT9075. When M/$\overline{\text{S}}$ is low this signal is an output, and when M/$\overline{\text{S}}$ is high this signal is an input clock phase locked to the extracted clock (E2o).
46	34	$\overline{\text{F0b}}$	**Frame Pulse (Input/Output).** This is the ST-BUS or GCI frame synchronization signal, which delimits the 32 channel frame of CSTi, CSTo, DSTi, DSTo and the PCM30 link. When M/$\overline{\text{S}}$ is low this signal is an output, and when M/$\overline{\text{S}}$ is high this signal is an input. The GCI/STBUS selection is made under software control.
47	35	$\overline{\text{RxFP}}$/ Rx64KCK	**Receive Frame Pulse /Receive CCS Clock (Output).** An 8KHz pulse signal, which is low for one extracted clock period. This signal is synchronized to the receive PCM 30 basic frame boundary. When 64KCCS (page 01H, address 1AH, bit 0) is set to 1, this pin outputs a 64 KHz clock derived from dividing down the extracted 2.048 MHz clock. This clock is used to clock CCS data out of pin CSTo in the CCS mode.
48	36	IC	**Internal Connection.** Must be left open for normal operation.
49	37	V_{SS}	**Negative Power Supply (Input).** Digital ground.
50	38	V_{DD}	**Positive Power Supply (Input).** Digital supply (+5V ± 10%).
51	39	VDD_{ATx}	**Transmit Analog Power Supply (Input).** Analog supply for the LIU transmitter (+5V ± 10%).
52	40	TTIP	**Transmit TIP (Output).** Transmit output for the PCM 30 AMI signal - must be transformer coupled.
53	41	TRING	**Transmit RING (Output).** Transmit output for the PCM 30 AMI signal - must be transformer coupled.
54	42	GND_{ATx}	**Transmit Analog Ground (Input).** Analog ground for the LIU transmitter.
55	43	Tdi	**IEEE 1149.1a Test Data Input.** If not used, this pin should be pulled high.
56	44	Tdo	**IEEE 1149.1a Test Data Output.** If not used, this pin should be left unconnected.
57	45	Tms	**IEEE 1149.1a Test Mode Selection (Input)**. If not used, this pin should be pulled high.
58	46	Tclk	**IEEE 1149.1a Test Clock Signal (Input).** If not used, this pin should be pulled high.
59	47	$\overline{\text{Trst}}$	**IEEE 1149.1a Reset Signal (Input).** If not used, this pin should be held low.
60	48	$\overline{\text{TAIS}}$	**Transmit Alarm Indication Signal (Input).** An active low on this input causes the MT9075 to transmit an AIS (all ones signal) on TTIP and TRING pins. $\overline{\text{TAIS}}$ should be set to high for normal data transmission.

Pin Description (continued)

Pin #		Name	Description
PLCC	MQFP		
61	57	LOS	**Loss of Signal or Synchronization (Output).** When high, and page 02H address 13H bit 2, LOS/LOF = 0, this signal indicates that the receive portion of the MT9075 is either not detecting an incoming signal (bit LLOS on page 03H address 18H is one) or is detecting a loss of basic frame alignment condition (bit $\overline{\text{SYNC}}$ on page 03H address 10H is one). If LOS/LOF=1, a high on this pin indicates a loss of signal condition.
62	58	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
	59	NC	**No Connection.** Leave open for normal operation.
63	60	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
64	61	TxDLCLK	**Transmit Data Link Clock (Output).** A gapped clock signal derived from a gated 2.048 Mbit/s clock for transmit data link at 4, 8, 12, 16 or 20 kHz. The transmit data link data (TxDL) is clocked in on the rising edge of TxDLCLK. TxDLCLK can also be used to clock DL data out of an external serial controller.
65	62	TxDL	**Transmit Data Link (Input)**. An input serial stream of transmit data link data at 4, 8, 12, 16 or 20 kbit/s composed of 488ns-wide bit cells which are multiplexed into selected national bits of the PCM 30 transmit signal.
66	63	MS/FR	**Master-Slave/Freerun (Input).** If this pin is set to high, the MT9075 is in the Master or Slave mode depending on the M/$\overline{\text{S}}$ pin. If low, the MT9075 is in the free run mode.
67	64	VDD	**Positive Power Supply (Input).** Digital supply (+5V ± 10%).
68	65	VSS	**Negative Power Supply (Input).** Digital ground.
	1-7, 25-31, 49-56, 75-82, 100	NC	**No Connection.** Leave open for normal operation.

Functional Description

The MT9075 is an advanced PCM 30 framer with on-chip Line Interface Unit (LIU) that meets or supports the latest ITU-T Recommendations for PCM 30 and ISDN primary rate including G.703, G.704, G.706, G.775, G.796, G.732, G.823 and I.431. It also meets or supports the layer 1 requirements of ETSI ETS 300 011, ETS 300 233 and BS6450.

The Line Interface Unit (LIU) of the MT9075 interfaces the frame functions to the PCM 30 transformer-isolated four wire line. The transmit portion of the LIU consists of a digital buffer, high speed digital-to-analog converter, pre-emphasis amplifier and complementary line drivers. The receiver portion of the LIU consists of an input signal peak detector, an optional equalizer with two separate high pass sections, a smoothing filter, data and clock slicers and a clock extractor. The optional equalizer allows for error free reception of data with a line attenuation of up to 20 dB.

The MT9075 LIU also contains a Jitter Attenuator (JA), which can be configured to either the transmit or receive path. The JA will attenuate jitter from 2.5 Hz and roll-off at a rate of 20 dB/decade. Its intrinsic jitter is less than 0.02 UI.

The digital portion of the MT9075 connects an incoming stream of time multiplexed PCM channels (at 2.048 Mbit/s) to the transmit payload of the E1 trunk, while the receive payload is connected to the ST-BUS or GCI 2.048 Mbit/s backplane bus for both data and signalling. Control, reporting and conditioning of the line is implemented via a parallel microprocessor interface. The MT9075 framing algorithm allows automatic interworking between CRC-4 and non-CRC-4 interfaces.

The S_a bits of the MT9075 can be accessed in the following four ways:

- Single byte registers;
- Five byte transmit and receive national bit buffers;
- Data link pins TxDL, RxDL, RxDLCLK and TxDLCLK;
- HDLC Controller with a 128 byte FIFO.

The MT9075 operates in either termination or transparent modes selectable via software control. In the termination mode the CRC-4 calculation is performed as part of the framing algorithm. In the transmit transparent mode, no framing or signalling is imposed on the data transmit from DSTi on the line. In particular, the MT9075 optionally allows the data link maintenance channel to be modified and updates the CRC-4 remainder bits to reflect the modification. All channel, framing and signalling data passes through the device unaltered. This is useful for intermediate point applications of a PCM 30 link where the data link data is modified, but the error information transported by the CRC-4 bits must be passed to the terminating end. In the receive transparent mode, the received line data is channelled to DSTo with framing operations disabled, consequently, the data passes through the slip buffer and drives DSTo with an arbitrary alignment.

The MT9075 has a comprehensive suite of status, alarm, performance monitoring and reporting features. These include counters for BPVs, CRC errors, E-bit errors, errored frame alignment signals, BERT, and RAI and continuous CRC errors. Also, included are transmission error insertion for BPVs, CRC-4 errors, frame and non-frame alignment signal errors, payload errors and loss of signal errors.

A complete set of loopback functions is provided, which includes digital, remote, ST-BUS, payload, metallic, local and remote time slot.

The MT9075 also contains a comprehensive set of maskable interrupts and an interrupt vector function. Interrupt sources consist of synchronization status, alarm status, counter indication and overflow, timer status, slip indication, maintenance functions and receive channel associated signalling bit changes. A special set of maskable interrupts have been included for change of the state of national use bits and nibbles, in order to enable compliance to the emerging ETS requirements.

The MT9075 system timing may be slaved to the line, operated in free-run mode or controlled by an external timing source.

Notes: