

Features

- Time-slot interchange function between eight pairs of ST-BUS/GCI/MVIP™ streams (512 channels) and a Parallel Data Port (PDP)
- Parallel port data rates up to 19.44 Mbyte/s
- Programmable data rates on the serial port side (2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s)
- Supports star, point-to-point connections and unidirectional or bidirectional ring topologies for distributed systems
- Input-to-output bypass function on the parallel data port for add/drop functions
- Provides a 125µs elastic store on the receive direction
- Provides byte switching for up to 2430 channels
- Per-channel direction control on the serial port side
- Per-channel message mode and high-impedance control on both parallel and serial port sides
- 8-bit multiplexed port compatible with Intel and Motorola microcontrollers
- Guarantees frame integrity when switching wideband channels such as ISDN H0 channel
- Provides external control lines allowing the fast parallel interface to be shared with other devices

ISSUE 1

August 1995

Ordering Information

MT90840AL	100 Pin PQFP
MT90840AP	84 Pin PLCC
-40°C to 85°C	

- Special diagnostic alarm functions for statistical analysis
- JTAG boundary scan

Applications

- Bridging ST-BUS/MVIP buses to high speed Time Division Multiplex backplanes at SONET rates (STS-1/3)
- High speed isochronous backbones for distributed PBX and Local Area Network systems
- Switch platforms of up to 2430 channels with guaranteed frame integrity for wideband channels
- Serial bus control and monitoring
- Data multiplexer
- High speed communications interface
- Isochronous switching/multiplexing to support IEEE 802.9 standards

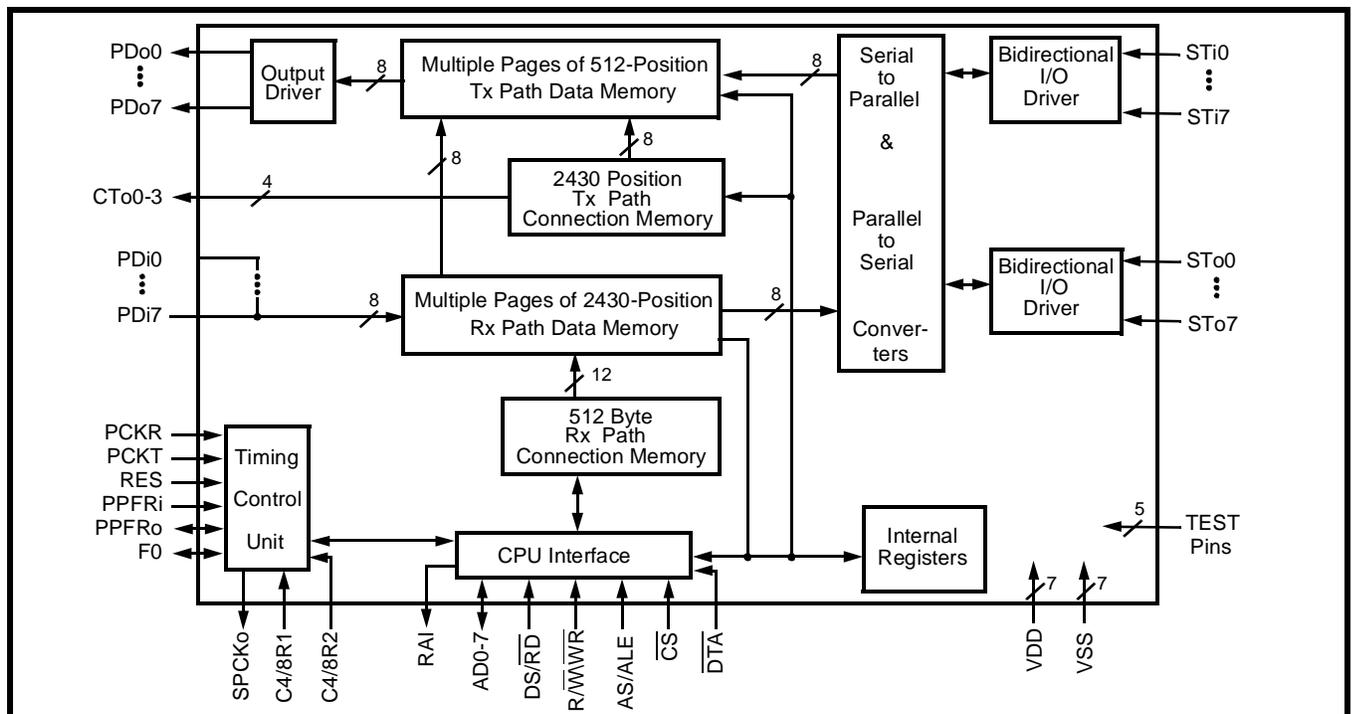


Figure 1 - Functional Block Diagram

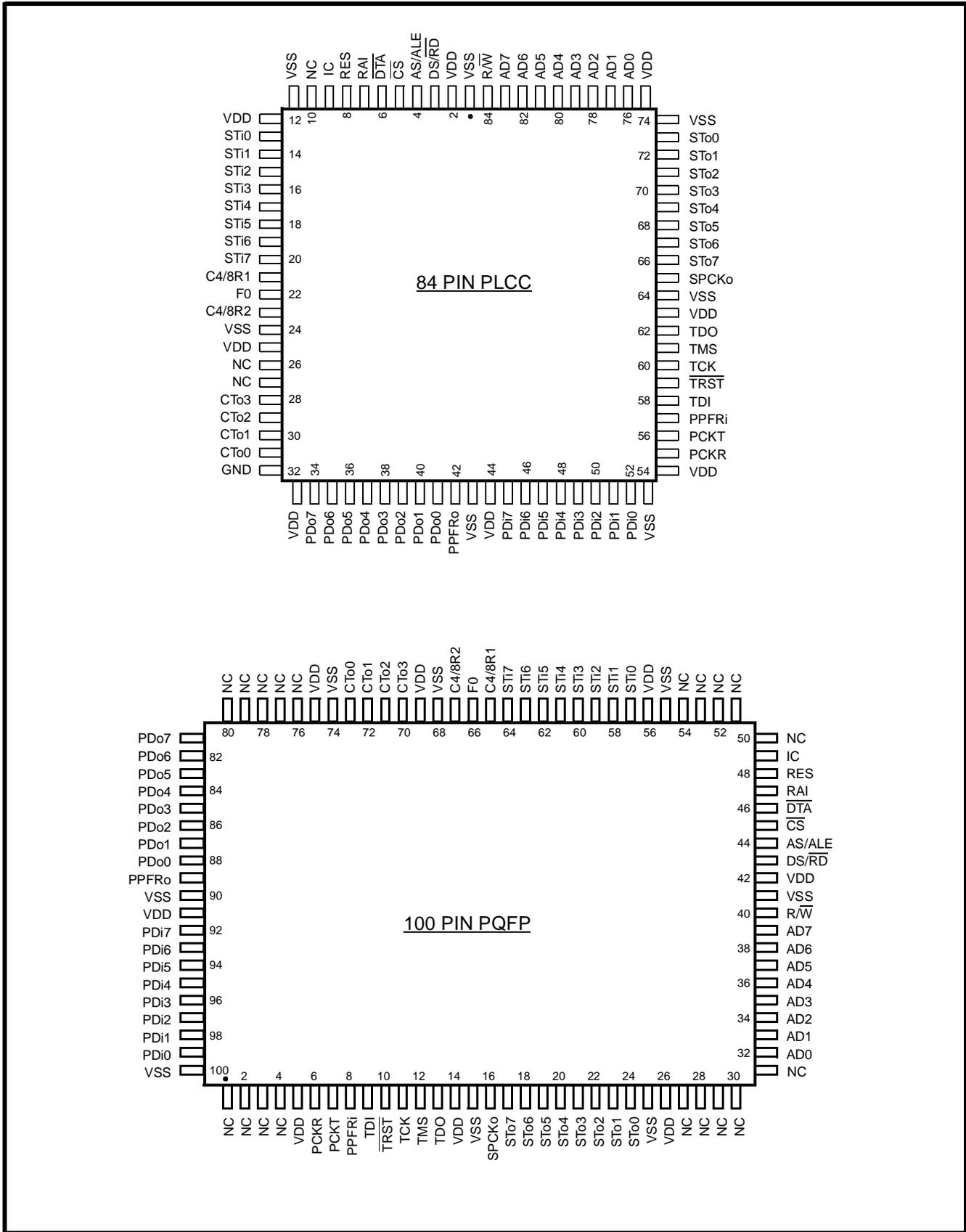


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
84	100		
3	43	DS/RD	Data Strobe/Read (Input). In MOTOROLA Multiplexed bus mode this input is DS. This active high input works in conjunction with \overline{CS} to enable the internal read and write generation. In Intel/National multiplexed bus mode this input is RD. This active low input configures the data bus lines (AD0/AD7) as outputs.
4	44	AS/ALE	Address Strobe / Address Latch Enable (Input). The falling edge of this signal is used to sample the address into the Address Latch circuit.
5	45	\overline{CS}	Chip Select (Input). Active low input enabling a microprocessor read or write of control or status registers.
6	46	\overline{DTA}	Data Acknowledgement (Open Drain Output). This active low output indicates that a data bus transfer is complete.
7	47	RAI	Receive Alarm Interrupt (Active High Output). This output indicates that the MT90840 has detected an alarm condition. The indication of the specific condition can be read in the ALS (Alarm Status) register. The CPU should read ALS, identify the source for the interrupt and then set the appropriate mask bit to cause the RAI signal to go LOW again.
8	48	RES	RESET (Input). A HIGH pulse should be given to this input during system initialization to configure the MT90840 internal registers into a specific power up functional mode (STo0-7, STi0-7, PDo0-7 are placed into high impedance condition). During normal operation this input should be held LOW.
9	49	IC	Internal Connection. The user must connect this pin to Ground.
10, 26, 27	1-4, 27-31, 50-54, 76-80	NC	No Connection.
11-20	57-64	STi0-STi7	Serial Inputs 0 to 7 (Bidirectional). Serial data input streams. These may be composed of 32, 64 or 128 channels at data rates of 2.048, 4.096 or 8.192 Mbit/s, respectively. For 2.048 and 4.096 Mb/s applications, streams STi0-STi7 can be used while for 8.192 Mb/s, only streams STi0-STi3 (512 channel limit) are used. These eight bidirectional lines can be programmed as inputs or outputs in a channel basis (64 kb/s).
21	65	C4/8R1	Serial Clock Reference Input 1. When enabled by the C4/8R bit (high) in the TIM register, this input receives the 4.096 or 8.192 MHz reference that is used by the MT90840 in TM1 to shift data in and out of the serial port. In TM2 if this input is enabled by the C4/8R bit (high), it receives a 4.096 or 8.192 MHz clock from an external source (DPLL locked to the system 8 kHz reference) that are used to regenerate the serial port SPCKo and F0 outputs. If the C4/8R bit is set LOW or if INTCLK bit is set HIGH, this input is ignored by the MT90840. For more details on the utilization of this signal, see Timing Modes 1 and 2 description. In TM3 and TM4 this input is not used.
22	66	F0	Serial Port Frame Synchronization (Bidirectional). This signal determines the frame boundaries at the serial data port interface. In TM1 or TM2 (with SFDI bit=1), this signal is an input and its pulse polarity can be either ST-BUS or GCI formatted. The MT90840 automatically identifies the polarity of the pulse and adapts the serial data transmit and receive timing to an adequate format without CPU interaction. In TM2 (with SFDI bit=0) and TM3, this signal is an output generated by the internal timing unit and it is synchronized to the SPCKo output signal. The polarity of the active F0 pulse can be selected at bit SPFP in the GPM register.

Pin Description

Pin #		Name	Description
84	100		
23	67	C4/8R2	<p>C4/8R2 Serial Clock Reference Input 2. In TM1, this pin behaves like the C4/8R1 input; i.e, when enabled by the C4/8R bit (low), it receives the 4.096 or 8.192 MHz reference that is used by the MT90840 in TM1 to shift data in and out of the serial port.</p> <p>In TM2 if this input is enabled by the C4/8R bit (low), it receives a 4.096 or 8.192 MHz clock from an external source (DPLL locked to the system 8 kHz reference) that is used to regenerate the serial port SPCKo and F0 outputs. If either C4/8R and INTCLK bits are set HIGH, this input is ignored by the MT90840.</p> <p>In TM3 and TM4 this input is not used.</p>
28-31	70-73	CTo3-CTo0	<p>External Control Lines 0-3. These four output signals are generated by the MT90840's internal Transmit Path Connection Memory (TPCM) circuitry. The four serial CTo output lines represent the contents of the four CT bits in the TPCM and are clocked at the parallel port rate (up to 19.44 Mb/s). See Per Channel Functions section.</p>
34-41	81-88	PDo7-PDo0	<p>Parallel Data Output Port 0 to 7. These eight outputs carry the parallel port data bytes in the transmit direction and operates at data rates up to 19.44 Mbyte/s.</p>
42	89	PPFRo	<p>Parallel Port Frame Pulse (Bidirectional). This signal delineates the start of a new data frame at the PDo0-7 lines on the transmit side of the MT90840 parallel port. When the PFDI bit at the TIM register is set High, PPFRo becomes an input and it receives the output frame reference from the main frame alignment source (e.g., another MT90840). This output is used in all timing modes except TM3.</p>
45-52	92-97	PDi7-0	<p>Parallel Data Input Port 0 to 7. These eight inputs carry the parallel port data bytes in the receive direction and operates at data rates up to 19.44 Mbyte/s.</p>
55	6	PCKR	<p>Parallel Port Clock Receive (Input). This could be either a 19.44, 16.384 or 6.48 MHz clock input and it determines the byte rate on the receive and transmit parallel ports. This signal is typically provided by the high speed framers. In TM1 the PCKR input is used by the MT90840 to clock in data bytes from the Parallel Data Port. In timing modes 2, 3 and 4, this input controls the byte transmit and receive operations on the parallel port.</p>
56	7	PCKT	<p>Parallel Port Clock Transmit (Input). This could be either a 19.44, 16.384 or 6.48 MHz clock input. It is typically provided by the high speed framers. The PCKT input is used by the MT90840 to clock out data bytes on the Parallel Data Port when the device is operating in TM1. In TM2,3 & 4 this input is ignored.</p>
57	8	PPFRi	<p>Parallel Port Frame Pulse Input. This input determines the start of a new frame at the PDi0-7 lines on the receive side of the MT90840 parallel port. It is typically connected to the 8 kHz frame pulse output signal provided by high speed framers. In TM3, PPFRi is the only frame sync reference for both transmit and receive parallel interface.</p>
58	9	TDI	<p>(Test Data Input). JTAG Serial test instructions and data are shifted-in on this pin. This pin is pulled high when not driven.</p>
59	10	TRST	<p>(Test Reset Input). Asynchronously initializes the JTAG TAP controller by putting it in the <i>Test-Logic-Reset</i> state. This pin is pulled high when not driven.</p>
60	11	TCK	<p>(Test Clock Input). Provides the clock to the JTAG test logic.</p>
61	12	TMS	<p>(Test Mode Select Input). JTAG Signal that controls the state transitions of the TAP controller. This pin is pulled high when not driven.</p>
62	13	TDO	<p>(Test Data Output). JTAG Serial data is output on this pin on the falling edge of TCK.</p>

Pin Description

Pin #		Name	Description
84	100		
65	16	SPCKo	<p>Serial Port Clock Output: In TM2 and TM3 this is a 4.096 MHz clock output derived from the system 4.096 MHz reference (received at the C4/8R input pins or from the internal 16.384 or 19.44 MHz clocks. See bit INTCLK in the TIM register). In TM2 and TM3 this output is used to shift data in and out of the Serial Port.</p> <p>In TM1 and TM4, this output is automatically placed in high impedance.</p> <p>For applications with the serial port running at 8.192 Mb/s, this output is not used. For those applications, the user should supply the MT90840 (at C4/8R1 or C4/8R2 input pins) and other devices connected to the serial port with a main 8.192 MHz clock source.</p>
66-73	17-24	STo7-STo0	<p>Serial Output Streams 0 to 7 (Bidirectional). These may be composed of 32, 64 or 128 channels at data rates of 2.048, 4.096 or 8.192 Mbit/s, respectively. For 2.048 and 4.096 Mb/s applications, streams STo0/STo7 can be used while for 8.192 Mb/s, only streams STo0/STo3 (512 channel limit) are used. These eight bidirectional lines can be programmed as inputs or outputs in a channel basis.</p>
76-83	32-39	AD0-AD7	<p>Multiplexed Address/Data (Bidirectional bus). These I/O lines provide eight input address lines to the Address Latch circuit as well as the eight I/O data lines to be connected to the Bus Direction Control circuit.</p>
84	40	R/W \ WR	<p>Read/Write \ Write (Input). In MOTOROLA Multiplexed bus mode this input is R/W. This input controls the direction of the data bus lines (AD0/AD7) during a microprocessor access. In INTEL/NAT multiplexed timing mode this input is WR. This active low signal configures the data bus lines (AD0/AD7) as inputs.</p>
1,11 24,32, 43,53, 64,74	15,25, 41,55, 68,74, 90,100	V _{SS}	<p>Ground.</p>
2, 12, 25,33 44,54, 63,75	5, 14, 26,42 56,69, 75,91	V _{DD}	<p>+5 Volt Power Supply.</p>

Functional Description

Real time multimedia applications require the transmission of mixed voice and data transmission into the same integrated network and transmission media. The network must simultaneously ensure that data at N x 64 kbit/s rates maintain time slot sequence integrity by providing constant delay through the switch.

The MT90840 device bridges existing Mitel ST-BUS components into a new networking environment whereby mixed data, voice and video signals can be time-interchanged or multiplexed from serial PCM streams onto a serial high speed Time Division Multiplex (TDM) isochronous backbones operating at SONET rates such as 51 (STS-1) or 155 Mb/s (STS-3). Figure 1 shows the MT90840 functional block diagram.

The MT90840 device is designed to switch 64 kbit/s or wideband N x 64 kb/s channels from a Serial Data Port (SDP) to/from the Parallel Data Port to be connected to off-the-shelf high speed Serial-to-Parallel (S to P) and Parallel-to-Serial (P to S) devices. The MT90840 Parallel Data Port is designed to accept data rates up to 19.44 Mbyte/s and the Serial Data Port can be programmed to connect to PCM serial streams at 2.048, 4.096 and 8.192 Mb/s.

Since the parallel and serial ports of the MT90840 device operate at different rates, an internal rate converter circuit associated with a multiple buffer time interchange block is employed to achieve the rate adaptation between the two ports.

The internal time interchange block allows the switching of 512 64 kb/s channels on the serial interface in a flexible connection scheme. This is accomplished by a feature called "per channel

direction control" on the 16 serial streams. For example, in some applications all 512 channels from the serial port can be time interchanged to the parallel port side. In the opposite direction, 512 channels coming from the parallel port can be dropped or time interchanged to the serial port side.

Two main clock synchronization schemes are provided by the MT90840. In master mode, the serial port interface provides the clock and frame reference signals to the parallel port while in slave mode, the serial port clock and frame reference signals are derived from the parallel port interface.

When the MT90840 device operates in applications whereby a ring architecture is employed, a special mode called Data Bypass is provided to allow the input data at the parallel port to be bypassed to the output port feeding the ring back with the data which is not destined to the local station. The data destined for the local station can be dropped through CPU programming. In this mode, the CPU has the full control on managing the outgoing bandwidth (from the serial interface to the high speed link) so that it does not contend with the bypassed data.

For CPU access to the serial channels, the MT90840 device can be programmed message mode with fast memory access times. By using the Mitel message mode, the microprocessor can access serial input and output TDM data on a per channel basis.

Device Operation

User Serial Data Port

The serial port is composed of 16 bidirectional serial data lines (STo0-7, STi0-7), two reference input clocks (C4/8R1, C4/8R2), one serial clock output (SPCKo) and a bidirectional frame synchronization signal (F0). Different data rates can be handled by the MT90840 device on the serial interface side: 2.048, 4.096 and 8.192 Mb/s. The MT90840 data rates on the serial port are selected for the complete group of input and output stream; i.e., when a specific data rate is selected, all input and output streams are affected.

During system initialization, the CPU should select the Input and Output data rates through the programming of bits DR1-0 at the Interface Mode Selection (IMS) register. For applications at 2.048, 4.096 and 8.192 Mb/s, all 16 serial data streams have their direction (input or output) defined by the CPU on a per channel basis. The per-channel direction control feature can be enabled by the DC

bit in the Receive Path Connect Memory High. This is ideal for applications in Computer Telephony Integration (CTI) whereby per-channel direction control is required within telephony servers.

When 2.048 Mb/s data rate is selected, a typical configuration would be 8 input x 8 output data streams each with 32 channels of 64 kbit/s. This mode allows a 256 channel Switch Matrix configuration. The interface clock for this mode is 4.096 MHz. Another possible connection available is the 16 stream bidirectional mode selected by the FDC bit in the IMS register. This operation allows up to 512 channels to be handled by the internal switch matrix. When per-channel direction control is used in this mode all 512 channel available at the serial port can be turned into one single direction.

For 4.096 Mb/s applications, the MT90840 provides a 8 input x 8 output data stream configuration with 64 channels of 64 Kb/s each per stream. In this mode, a 512 channel switch matrix can be built and the interface clock is also 4.096 MHz. The channel direction control is also provided in this mode, however, if one time slot in an input stream (e.g., STi0) is programmed as an output, the correspondent time slot on the equivalent output stream (STo0) is automatically set as an input.

In 8.192 Mb/s applications, a 4 input x 4 output stream configuration provides 128 channels per stream, allowing a 512 channel switch matrix to be built. The interface clock for this mode should be 8.192 MHz. The capabilities of per channel direction control in 8.192 Mb/s mode are similar to the ones explained for 4.096 Mb/s mode.

For each of the 32, 64 or 128 time slots on each serial output stream, the MT90840 can be programmed to provide per-channel high impedance control. Figure 3 shows the different configurations for the MT90840 serial port. When the MT90840 drives the serial port frame reference different frame pulse polarities can be selected for the F0 signal by accessing bit SPFP in the GPM register. This flexibility allows the MT90840 to be employed with different serial digital interface formats. In this case, depending on the polarity specified, the serial bit transmit and receive edges will automatically adapt to the specified interface (ST-BUS or GCI). When the MT90840 receives the frame reference (F0) from an external source with ST-BUS or GCI format an internal frame pulse identifier adapts the device to either a positive or negative polarity frame pulse without CPU interaction.

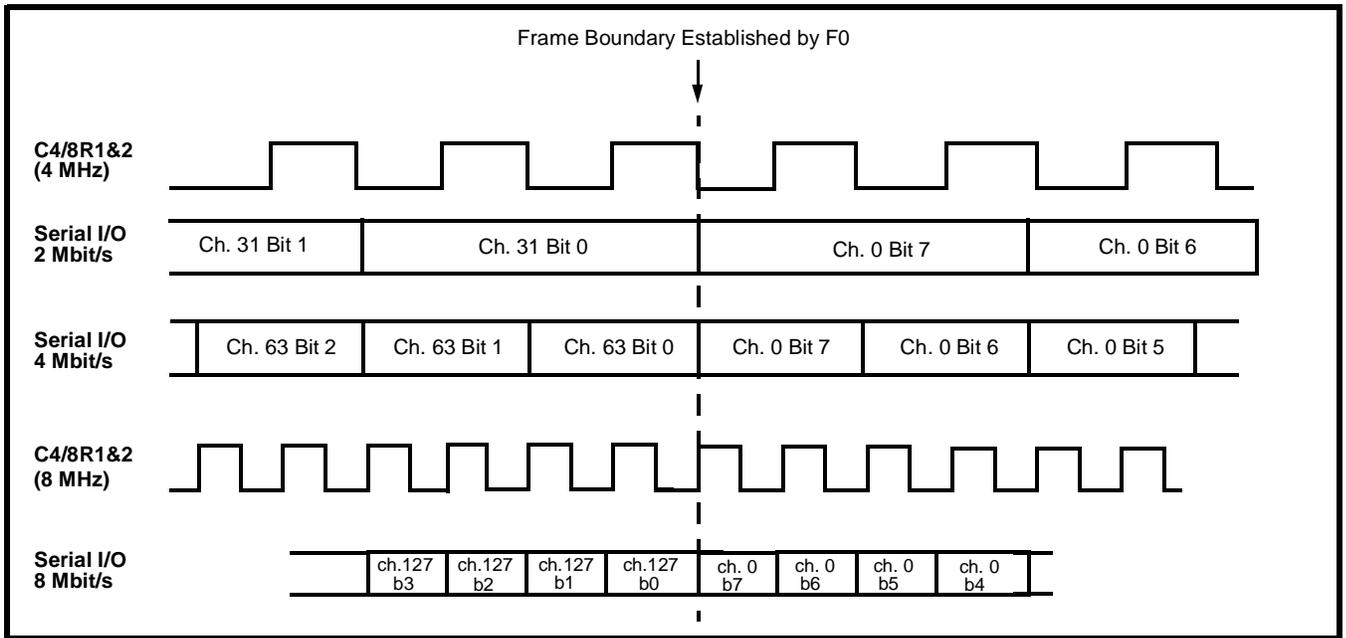


Figure 3 - Serial Port Interface Functional Timing

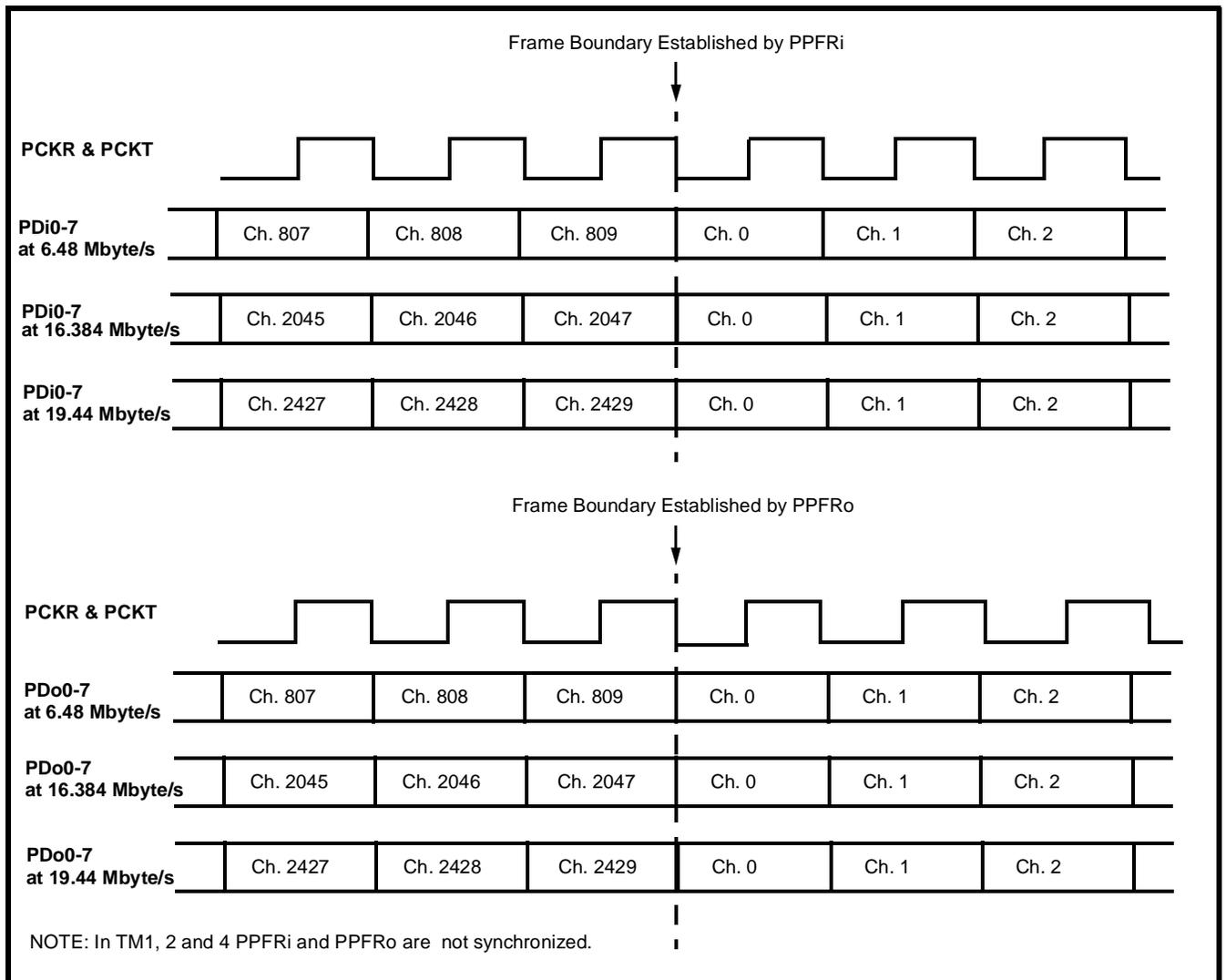


Figure 4 - Parallel Data Port Functional Timing

Serial Port Clock Signals

Depending on the Timing Mode selected, the MT90840 device can either accept the serial port 4.096 or 8.192 MHz as input references or drive the ST-BUS clocks from an internal divider. See section on TIMING CONTROL for more details. When the device accepts the clock reference, input pins C4/8R1 and C4/8R2 are used. Since only one reference can be taken at a time, the CPU has to define which of the two input pins will be used to acquire that clock reference. The bit C4/8R of the Timing Mode register should be used to select which pin will carry the reference. When the device drives the serial port clock, SPCKo output is provided.

Parallel Data Port

The MT90840 parallel port is composed of six functional lines: two separate 8 bit wide Parallel Data Output Port (PDo0-7) and Parallel Data Input Port (PDi0-7), an Input (PPFRi) and Output (PPFRo) Frame Synchronization signals, an Input Transmit (PCKT) and Receive Data Clocks (PCKR). The byte transmit edge of the parallel port can be selected to be at the rising or falling edges of the PCKT or PCKR clocks. The bit TCP (Transmit Clock Polarity) of the TIM register can be used for this selection. The parallel port of the MT90840 device is designed to interface to a variety of existing high speed S to P and P to S converter devices used when implementing serial transport backbones of up to 155 Mb/s.

The most popular S to P and P to S converter and framer devices available in the market provide a parallel synchronous backplane on the local system side that operates respectively at 6.48 or 19.44 Mbyte/s (which correspond respectively to the serial rate of 51.8 or 155.52 Mb/s divided by 8). The MT90840, together with the converter devices, provide the user with capabilities of designing a "backbone access switch" or "add/drop" function which allows the time interchange of the data from the serial port to/from the frame payload of the high speed serial backbone.

The MT90840 device allows three different speeds to be accommodated on the parallel port: 6.480, 16.384 and 19.44 Mbyte/s. The selection of the speeds has to be done by the local CPU through the setting of the PPS2-0 bits in the IMS register.

The MT90840's parallel port frame pulse input (PPFRi) and output (PPFRo) signals synchronize the MT90840 internal time interchange circuit to the payload of the high speed frame allowing data from

the serial port side to be inserted to or received from the high speed parallel data interface (PDP port). Upon the selection of the parallel port data rate, the MT90840's internal memory control circuitry determines what is the internal amount of memory required to store the incoming frame. For example, if the clock rate is 19.44 MHz, all 2430 locations of the Receive Path Data Memory and Transmit Path Connect Memory will be used. If the clock rate is 6.48 MHz, only 810 locations of the RPDm and TPCM will be used by the device. In case of 52 and 155 Mb/s interfaces, 810 and 2430 time slots can be assigned, respectively, in 125 μ s. See Figure 4 for functional timing.

Because the major application of the MT90840 device is to switch information from the Serial Data Port to the Parallel Data Port and vice versa, the total device's data throughput per direction is 512 channels. For example, if 155 Mb/s interface is used from the 2430 time slots available in the payload, 512 channels will be assigned for transmission (from serial to high speed backbone) and additional 512 on the receive (from high speed backbone to serial).

The MT90840 device also provides a per channel tristate selection on the Parallel Port interface, allowing several MT90840s (switch matrix applications) or other devices (for example, an ATM formatter device) to share the same parallel backplane and the high speed TDM backbone.

Different frame pulse polarity can be selected for the PPFRo signal by accessing bit PPFP in the GPM register. This flexibility allows the MT90840 to be employed with different framer devices.

Time Slot Interchange Operation

The MT90840 was created to provide access and time interchange functions between the serial and parallel user data ports. Time interchange functions are provided in two directions: Transmit and Receive Paths. The Transmit Path is defined to be from the serial to parallel data ports. The Receive Path is defined from the parallel to serial data ports. Therefore, switching functions between serial data streams is not provided.

Since the MT90840 device provides serial and parallel ports operating at different rates, the internal rate converter circuit has to accommodate the differences in speed between serial incoming/parallel outgoing and parallel incoming/serial outgoing data. This is done by incorporating a "Multiple Port RAM" circuitry working at different speeds. This approach requires "pages" of memory working so that while some pages are being

accessed at one rate, another ones are being handled at a different rate.

The multiple port RAM approach also allows for the implementation of an architecture which guarantees wideband or Hyper-channel integrity through the switch. Analogous to any of the Mitel digital switches, user data on both serial and parallel ports is written to data memory buffers, one for each alternate frame period. To perform the time interchange functions, an internal Connection memory is provided whereby the address for the data memory is read. The address provided to the data memory represents the source channel address and originates from the connection memory location corresponding to the desired output channel.

Transmit Path

On the Transmit Path, user data entering the MT90840 device at the serial port is converted into parallel format (8 bits per channel) and written to consecutive locations of the 512-byte page of the TX path data memory (TPDM). While one page is being written by the serial to parallel converters (at rates defined by bits DR1-0 in the IMS register), the other pages are read and used as source buffer for information to be transmitted on to the parallel port (at rates defined in bits PPS1-0).

To allow for applications running at transmission rates up to 155 Mb/s or 2430 DS0 channels, the switching procedure is achieved through a 2430 position deep Transmit Path Connection Memory (TPCM). The 16-bit wide TPCM is clocked synchronously at the parallel port clock and it will provide connection source information to one page of the Transmit Path Data Memory (TPDM). This connection memory is composed of two sub memories; high and low. The connection memory Low is used to provide the output address of the source channel and the connection memory High provides access to per-channel functions such as output driver enable. As an example, the TPCM LOW provides the local CPU with the ability to program connections from the incoming 512 channels on the serial port to any of the 2430 channels available in the high speed frame. Once the connection is established, the CPU can set all unused channels in tristate condition, allowing other devices to share the same bandwidth on the parallel output.

For transport backbone applications at 52 Mb/s (parallel port rate at 6.48 Mb/s), only 810 channels of the TPCM are available for connection between the

512 ST-BUS channels and the parallel output port. In applications whereby two or more MT90840s share the 810 channels on the parallel output port side, the per-channel tristate control bits in the TPCM HIGH can be used to avoid data contention. Additional per-channel functions available on the parallel data port side are message mode, channel bypass for ring applications and external output control line activation.

Receive Path

In the Receive direction, 8 bit wide parallel data entering the MT90840 device is written to consecutive locations of a 2430-byte deep Receive Path Data Memory (RPDM). While one page is being accessed by the parallel port circuitry at the rate defined at PPS bits, another page is being accessed by the parallel to serial converters on the serial port interface at rates defined by bits DR1-0.

Switching is done through a 512 position deep Receive Path Connection Memory (RPCM). The RPCM is a 15-bit wide memory clocked synchronously at the serial output rate and it will provide the source channel address to the Receive Path Data Memory (RPDM). The RPCM allows the programming of connections of up to 2430 source channels (stored in the RPDM) to any 512 output channels of the serial port. The RPCM is composed of two sub memories: Connection memory high and low. See Register Description section for more details.

In 52 Mb/s interface applications, the RPCM allows for the connection of any of the 810 incoming channels to any of the 512 output channels available on the serial interface. The per channel tri-state and message channel enable functions are available on the serial port and it is programmed by the CPU in the RPCM HIGH bits.

Parallel Port Switching

The MT90840 provides an operation called Parallel Port switching whereby the Serial Port, Receive Path Connection Memories (RPCM) low and high, are not used. Only the RPDM and TPCM memory group is available to allow for unidirectional switching of up to 2430 DS0 channels. To switch channels from the parallel input port to the parallel output port, only the TPCM high and low bits are required. In this operation mode, 12-bit wide channel address (AB0-11) bits in the TPCM high and low locations are used by the CPU to specify the source channel address for the switching. See Timing Control section for more details.

Output Drivers Enable Control Capability

The MT90840 device provides a bit (ODE) in the IMS register that places all data outputs of the device (parallel and serial) in high impedance condition. The ODE bit (Output Drive Enable) is automatically set LOW by the reset input pulse applied to the device during system power up. When LOW, the ODE bit disables all outputs of the MT90840 device while internal connection initialization is performed by the CPU. This function is useful to avoid data collision on the output when several MT90840s have their transmit ports connected together to the same output lines.

Timing Control

Four timing synchronization modes are available in the MT90840 device. Bits TM1-0 in the TIM register are used to select the timing modes. In all MT90840 timing operations, the throughput delay when performing time interchange functions of grouped channel data is constant maintaining the frame integrity of the input and output.

Timing Mode 1 (TM1) - Asynchronous Parallel Port With ST-BUS Clock Master

See Figure 5 for a connection example. TM1 allows the MT90840 to operate with simultaneous serial and parallel port input clock references. In TM1 the MT90840 receives the serial port frame pulse (F0) and serial data clock (at the C4/8R1 & 2 inputs) from the serial port side and generates the parallel port output frame pulse (PPFRo) synchronized to the F0. Due to internal serial to parallel conversion and time interchange functions, an internal fixed offset exists between the F0 and PPFRo output at the parallel port. Signals PCKT (Parallel Port Clock Transmit) and PCKR (Parallel Port Clock Receive) as well as

PPFRo and PPFRi are asynchronous in TM1. Since the serial port interface is always synchronized to a common C4/8R and F0 signals, an internal elastic store is required on the parallel port receive side to compensate for differences in phase between the parallel and serial ports. The internal elastic store can accumulate up to 125 μs of delay on the parallel receive direction.

The transmit path does not provide frame phase alignment and therefore the parallel port Tx clock (PCKT) must be tightly locked (in frequency) to the serial port clock C4/8R1 input. In TM1, the MT90840's SPCKo clock output is not used. For applications where multiple MT90840 share the same parallel output data lines (PDo0-7), one of the MT90840s must provide the parallel port transmit frame reference to both the framers and the other MT90840 on the bus. The one providing the reference must have the PFDi bit in the TIM register set Low. All other MT90840s will have PFDi set High (forcing PPFRo to be an input).

Timing Mode 2 (TM2) - Asynchronous Parallel Port With ST-BUS Clock Slave

See Figure 6 for a connection example. In TM2, the MT90840 internal serial (C4/8R1 and 2, F0) and parallel port timing references are derived from the parallel interface signals PCKR and PPFRi. In TM2, PCKT input is not used. Since the transmit and receive parallel data ports are synchronized to PCKR, the internal elastic store is not required.

In applications with the serial data port operating at 2.048 or 4.096 Mb/s, the receive parallel port 8 kHz reference (PPFRi) can be connected to an external PLL (e.g; MT9041/2) for the generation of the 4.096 MHz clocks. The 4.096 MHz output of the PLL is then fed back to the MT90840's C4/8R1 & 2 inputs for the generation of the SPCKo and F0 output signals which drive the serial data streams.

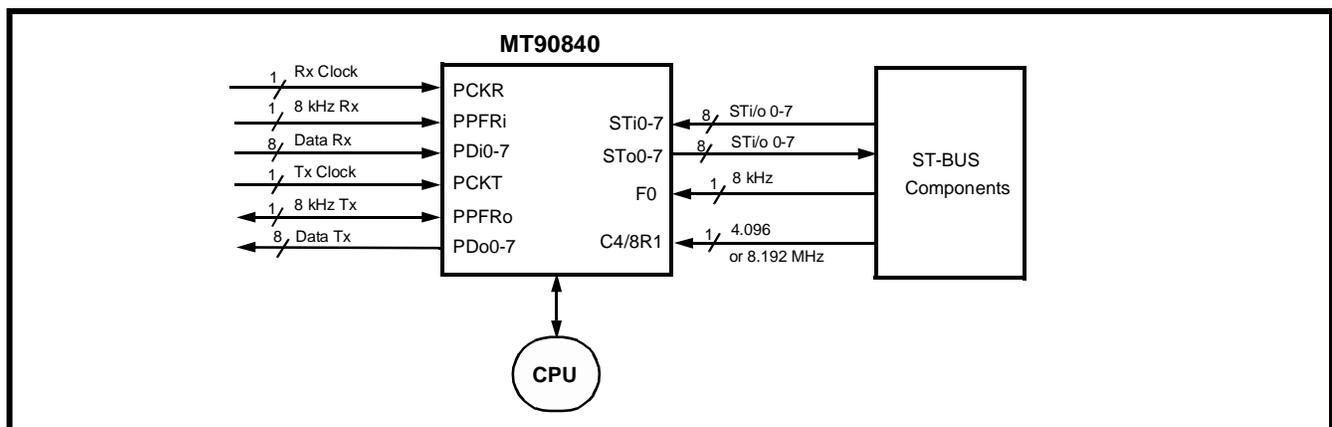


Figure 5 - Timing Mode 1 Configuration

In case of 8.192 MHz applications, a similar approach is required so that the 8.192 MHz output of the PLL is connected to the MT90840's C4/8R1 & 2 inputs. The MT90840 then utilizes the C4/8R1 input signal as the transmit and receive clock for the serial port. Therefore, the MT90840's SPCKo output is not used and the 8.192 MHz clock reference coming out of the PLL should be used as the main clock to drive serial port.

Internal 4.096 MHz clock Generator

For applications utilizing 19.44 and 16.384 MHz rates at the parallel interface of the MT90840, an optional method to generate the serial port 4.096 MHz clock is provided. An internal divider can be enabled to generate 4.096 MHz (at SPCKo output pin) from the 19.44 or 16.384 MHz clock applied at the PCKR input. The internal divider can not be used in applications where the parallel port operates at 6.480 MByte/s rates. The INTCLK bit in the TIM register determines which source is used to generate the serial port 4.096 MHz clock.

In timing mode 2, the received data on the parallel port will be switched to the serial port after certain delay required to perform time interchange and parallel to serial conversion. Due to this internal delay, the serial port output frame pulse (F0) is offset from the parallel port input frame sync signal (PPFRi). From the serial to the parallel port sides, another offset is generated due to serial to parallel

and rate conversion operations. An offset of two serial channels (2.048 Mb/s channels) is provided between parallel and serial port frames.

The offset between the Parallel Port Frame Pulse input (PPFRi) and output (PPFRo) signals are not higher than 4, 2Mb/s serial channels providing low latency when performing parallel data bypass function. For applications where multiple MT90840s share the same PPFRi and PCKR inputs on the parallel port side, and have the serial port clock derived from the C4/8R1 & 2 input pins an extra feature is provided to allow the serial port of all MT90840s to be synchronized so that it can be shared among multiple MT90840s. In this application, the SFDi bit at the TIM register of the TM2 device has to be set High. When SFDi bit = 1, the serial port F0 signal becomes an input and the main serial interface 8 kHz frame source can be applied to all MT90840s.

Timing Mode 3 (TM3) - Synchronous Parallel Port With ST-BUS Clock Slave

The connection of timing mode 3 is shown in Figure 7. TM3 is mode is similar to TM2 with two main differences: per channel bypass function is internally disabled and the parallel port Input and Output buses are synchronized and aligned with PPFRi input. In timing mode 3, the main 8 kHz reference on the parallel port is received at the PPFRi input pin and the PPFRo is not used.

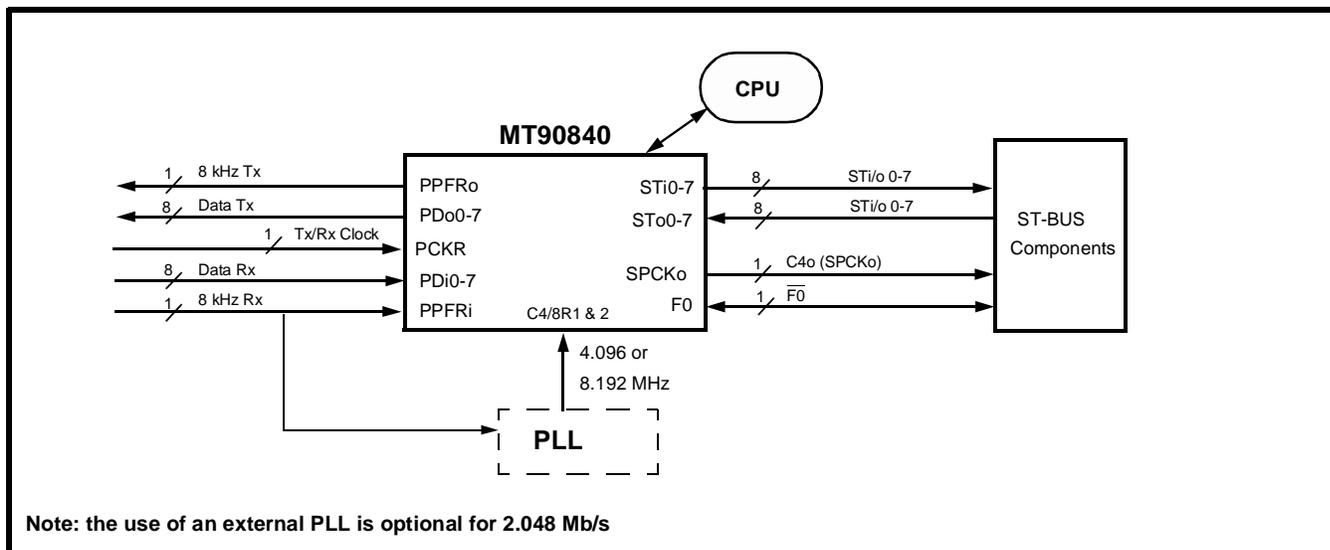


Figure 6 - Timing Mode 2 Configuration

In TM3, the generation of the serial port timing signals by the MT90840 is restricted to the internal divider mode (i.e., the C4/8R12 inputs are not required and ignored). In addition, TM3 mode is limited to 19.44 and 16.384 MHz rates on the parallel port side and 2.048 and 4.096 Mb/s data rates on the serial port side.

In TM3, an offset between the parallel and serial data ports frame pulse signals (PPFRi and F0) is provided. This offset corresponds to 30 PCM serial channels in 2 Mb/s, 60 channels in 4 Mb/s and 120 channels in 8 Mb/s.

Timing Mode 4. Parallel Data Switching Mode

Refer to Figure 8 for connection details. In TM4, the MT90840 device provides time interchange capabilities at the parallel data port only (PDi0-7 & PDo0-7) and the serial data streams STi0-7 and STo0-7 are not used. User data is received on PDi0-7 lines synchronized to the PPFRi input and clocked in with PCKR. Data clocked in at PDi0-7 is switched to PDo0-7 output lines.

On the parallel port output side, the MT90840 generates an output frame with parallel data at PDo0-7 lines clocked with PCKR and synchronized

to an internally generated PPFRo output. In TM4, PPFRo is offset (non-aligned) by a maximum of 4 clock cycles from the input frame sync PPFRi. This mode is only available for 19.44 and 16.384 Mbyte/s rates. In TM4, PCKT and all serial data port data and timing signals are not used.

MT90840 Throughput Delay

The MT90840 is designed to perform constant throughput delay on a per frame basis in all timing mode configurations. Although minimum and maximum values vary depending upon the input and output channel chosen for time-interchange, frame integrity is guaranteed for all switching configurations. Grouped channels at serial input streams or at the parallel port input are switched through the device to the same output frame.

Figure 9 summarizes the minimum and maximum throughput delay values for all timing modes.

MT90840 Per-channel Functions

The MT90840 provides per-channel functions that are available at the serial and parallel data ports. Per-channel functions on the parallel port side can

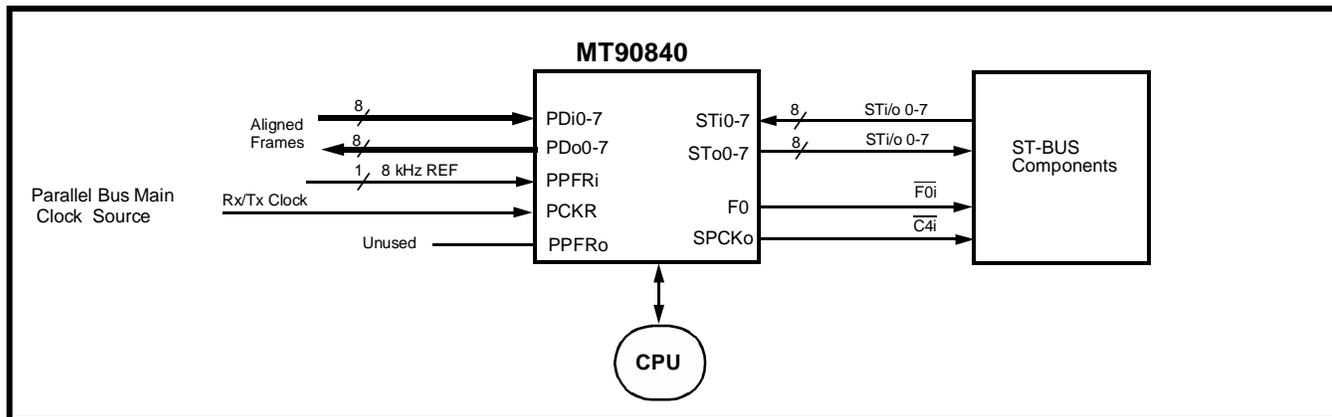


Figure 7 - Timing Mode 3 Configuration

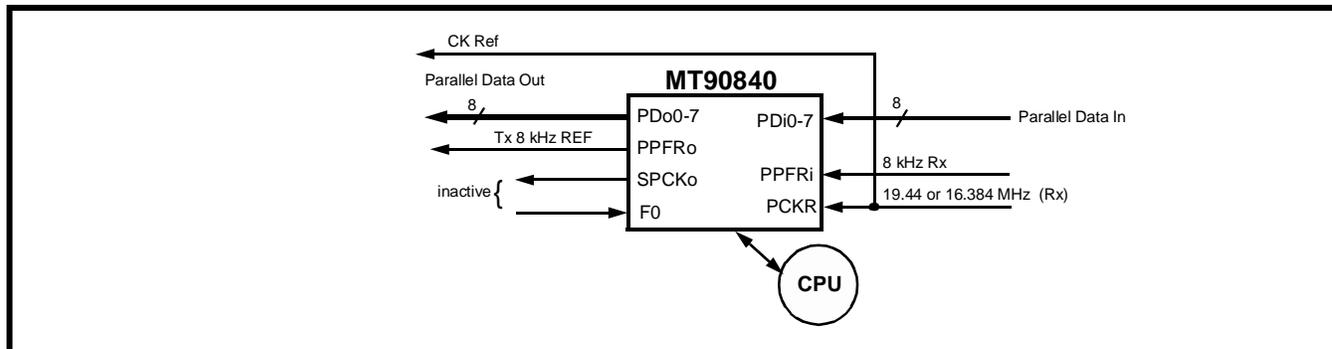


Figure 8 - Timing 4 Configuration

Timing Mode	Serial Data Rate	Minimum Delay (μs)	Total Throughput Delay (μs)
TM1, 2, 3	2.048 Mb/s	$D_{min}=[2+(32-S_{in})] * 3.9$	$T= D_{min} + [125-(125- P_{out1}/10e3)]$
	4.096 Mb/s	$D_{min}=[4+(64-S_{in})] * 1.75$	$T= D_{min} + [125-(125- P_{out1}/10e3)]$
	8.192 Mb/s	$D_{min}=[8+(128-S_{in})] * 0.975$	$T= D_{min} + [125-(125- P_{out1}/10e3)]$

Throughput Delay for TM1, 2, 3 - For the Transmit Path (Serial-to-Parallel Interface)

Timing Mode	Serial Data Rate	Minimum Delay (μs)	Total Throughput Delay (μs)
TM1	2.048 Mb/s	$D_{min}=4.8\mu s$	$T= D_{min} + ELD + \{ [32-(32-S_{out})] * 3.9\}$
	4.096 Mb/s		$T= D_{min} + ELD + \{ [64-(64-S_{out})] * 1.75\}$
	8.192 Mb/s		$T= D_{min} + ELD + \{ [128-(128-S_{out})] * 0.975\}$
TM2	2.048 Mb/s	$D_{min}=4.3\mu s$	$T= D_{min} + \{ [32-(32-S_{out})] * 3.9\}$
	4.096 Mb/s		$T= D_{min} + \{ [64-(64-S_{out})] * 1.75\}$
	8.192 Mb/s		$T= D_{min} + \{ [128-(128-S_{out})] * 0.975\}$
TM3	2.048 Mb/s	$D_{min}=117\mu s$	$T= D_{min} + \{ [32-(32-S_{out})] * 3.9\}$
	4.096 Mb/s		$T= D_{min} + \{ [64-(64-S_{out})] * 1.75\}$

Throughput Delay for TM1, 2, 3 - For the Receive Path (Parallel-to-Serial Interface)

Timing Mode	Minimum Delay (μs)	Total Throughput Delay (μs)	Units
TM4	$D_{min}=3.5$ (TCP bit =0) $D_{min}=4$ (TCP bit=1)	$T = D_{in} + [PPF - (PPF - OUT.CH)]$	PCKR cycles

Throughput Delay for TM4

Figure 9 - MT90840 Throughput Delay Summary

Notes: Naming rules

Sin: Serial Input Channel / Sout: Serial Output Channel
(1 to 32 in 2.048 Mb/s, 1 to 64 in 4.096 Mb/s, 1 to 128 in 8.192 Mb/s)

Pout1: Time in nanoseconds of Output Channel at the parallel port
52 x OUT.CH in 19.44 MHz mode
61 x OUT.CH in 16.384 MHz mode
154 x OUT.CH in 6.48 MHz mode

OUT.CH.: Output Channel on PDo0-7 outputs (up to 2430)
PPF : Total number of bytes at the parallel port frame
ELD : Elastic Store fixed delay (0 or 62.5 μs)

be activated in the Transmit Path Connect Memory High bits (TPCM High) and per-channel functions on the serial port interface can be enabled through Receive Path Connect Memory High bits (RPCM High). On the parallel port interface these per-channel features include: Output Enable, Message Mode, Data Bypass (or loopback) and External Control Lines.

On the serial port interface side the per-channel features include Output Enable, Message Mode and Direction Control.

Per-channel bypass on the parallel port side

A feature called per-channel Bypass is incorporated in the MT90840 parallel data interface (PDi0-7 & PDo0-7) to allow applications requiring data loopback from PDi0-7 inputs to PDo0-7 outputs. This mode is suitable for ring applications whereby received data at the parallel port can be either time-interchanged to the serial port or bypassed back to the transmit parallel port. This feature is only provided in Timing modes 1 and 2.

The per-channel bypass function allows all incoming data at PDi0-7 to be bypassed to the parallel output lines PDo0-7. The data from the serial port interface can be inserted (time-interchanged) in the parallel port output channels not being used in bypass mode.

The programming of the per-channel bypass feature is defined in the PPBY bit of the Transmit Path Connect Memory High locations as explained in the register section. If PPBY bit is High at a certain TPCM high location, the corresponding parallel input channel for that location will be bypassed. Depending on the parallel port data rate selected, up to 2430 channels can be bypassed from the parallel input to the parallel output. When PPBY bit is LOW at a certain TPCM High location, the corresponding output channel for that location can be used for data

insert function from the serial interface side. Since up to 512 channels can be inserted from the serial port side to the parallel port side, usually, only 512 PPBY bits from the 2430 are set Low in a given application. The Transmit Path Connect Memory Low contents used to determine source address of the inserted channel should coincide with the locations in the TPCM High with PPBY Low. Channels being bypassed can be monitored at the Receive Path Data Memory.

The MT90840 per-channel tri-state control and message channel bits in the TPCM High location have higher priority than the PPBY bits.

Per-channel External Control Lines on the Parallel Port Side

The MT90840 provides four output control signals (CTo0-CTo3) which are synchronized to the parallel port output timing. Each of the CTo output lines behaves as a mirror of the CTo-3 bits of the TX Path Connection memory high (TPCM high) bits. The contents of the CTo bit of each Connection Memory High location is output on the corresponding CTo pin once every frame. Typically this feature can be used to allow other devices to share the parallel data port bandwidth.

The CTo0-3 outputs are synchronized to the 19.44 MHz carrying 2430 bits per 125 μs frame. If CTo bit is set HIGH, the corresponding bit on CTo output is transmitted in HIGH. If CTo bit is LOW, the corresponding bit on the CTo output is transmitted in LOW. The contents of the 2430 CTo bits of the TPCM High are transmitted sequentially on to the CTo output pins and are synchronous to the PDo0-7 lines. Any HIGH or LOW levels written into position 0 of the TPCM high will be transmitted during the output frame pulse PPFRO as per Figure 10. The following bits are sequentially transmitted.

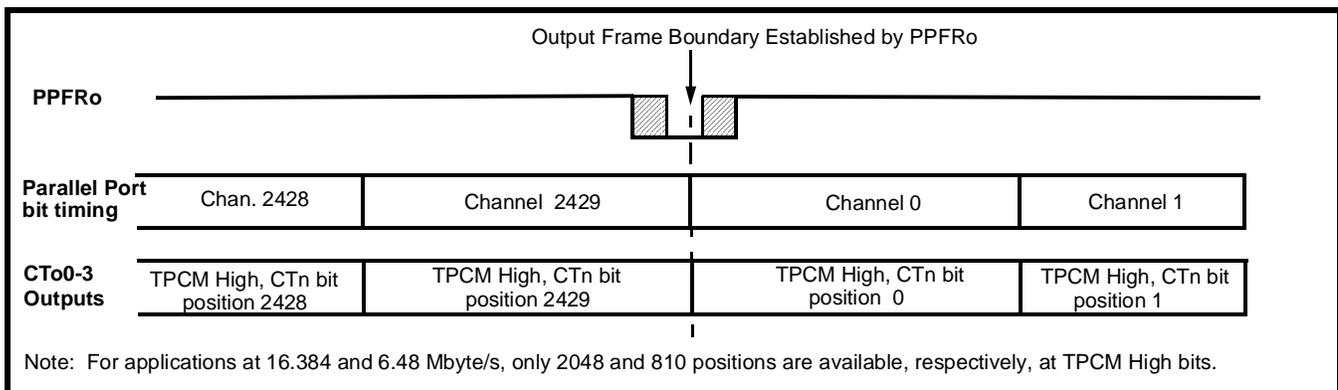


Figure 10 - External Control Line Outputs

Per-channel Direction Control on the Serial Port

The per-channel direction control feature of MT90840 can be activated in two different ways, symmetrical (or balanced) and full direction control operations. The symmetrical operation is available for 4 and 8 Mb/s rates at the serial port. The full direction control is only available for 2 Mb/s rates at the serial port.

- Symmetrical Operation

This operation is enabled when FDC bit at IMS register is LOW. The direction control performed by these bits will work in a manner where if a channel on any of the 8 serial output streams (STo0-7) is defined as an input (associated DC bit = 0, 4.096 and 8.192 Mb/s), the symmetrical channel on the equivalent input stream (STi0-7) will be configured as an output. For example, if channel 0 on STo7 is programmed as an input (DC=0), then channel 0 on STi7 is configured as an output. Therefore, the RPCM High DC bits will each correspond to every individual output channel available on the serial output stream STo0 to STo7.

- Full Direction Control Operation (2.048 Mb/s)

This operation is activated when FDC bit at the IMS register is HIGH. In full direction control mode all 16 serial streams can be controlled on a per-channel basis so that up to 512 channels can be either transmit or receive. As an example, if all DC bit locations of RPCM HIGH are set HIGH, then all 512 channels on STo0-7 and STi0-7 will be configured as outputs. If the same operation is done with DC bit LOW, then all 512 channels will be configured as inputs.

As an example, Figure 11 illustrates how two MT90840s are addressed when controlling up to 512 channels each in a single direction.

For more details on per-channel control functions for the serial and parallel data ports, see the TPCM and RPCM High bits definition in the Register Description section.

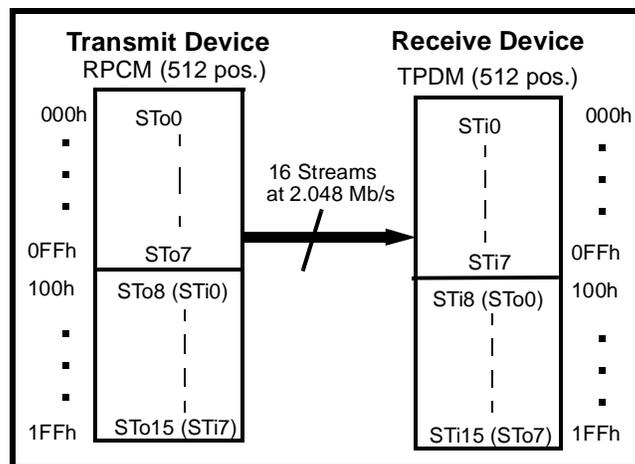


Figure 11- RPCM/TPCM Addressing FDC bit = 1

Microprocessor Port

A Multiplexed Parallel Microprocessor Port is provided by the MT90840 device to allow the local CPU to configure and read internal registers and memories. The MT90840 CPU interface is compatible to Motorola, National and Intel Multiplexed Bus CPUs and it adapts itself to the appropriate CPU's control signal timing without any mode selection.

The MT90840 CPU interface signals are AD0-7 (Data and Address), ALE/AS, DS/RD, R/W, CS and DTA. The parallel microprocessor interface provides the CPU with the access to five internal configuration registers and two Connection and Data Memories for transmit and receive paths. All locations are read/write except for the data memory which is read only. Accesses from the microport to the connection memory and the data memory are multiplexed with accesses from the input and output TDM ports. This can cause variable Data Acknowledge delays which are determined by the DTA output signal. Note that if the parallel port clocks PCKR & PCKT or serial port clocks C4/8R1 & 2 are not present during an internal memory access, the DTA output signal will be held HIGH until the clocks are applied again.

For complete details on the Microprocessor Interface timing signals, refer to the AC Electrical Characteristics section.

A7	A6	A5	A4	A3	A2	A1	A0	LOCATION	Power-on-reset Value (Hex)
0	0	0	0	0	0	0	0	IMS Register	00
0	0	0	0	0	0	0	1	Control register	n.a.
0	0	0	0	0	0	1	0	TIM register	00
0	0	0	0	0	0	1	1	GPM register	00
0	0	0	0	0	1	0	0	ALS register	00

Table 1 - MT90840 Register Address Mapping

Address Mapping of the internal registers

The MT90840 provides five internal registers which are used by the local CPU to configure the device in different operation modes. The IMS, TIM, GPM and ALS registers should be initialized by the local CPU on every system power-up to place the MT90840 device in the required operation mode before any internal memory access is performed. In the MT90840, the A7 input line must be kept LOW when accessing the internal registers as depicted in Table 1.

When input line A7 is HIGH, input signals A0-A6 are used together with bits HA7-HA11 in the Control register to form a 12-bit address stream to access the MT90840 internal Transmit and Receive Path memories. See section Internal Memory Description for memory address mapping.

RAI Interrupt

The MT90840 provides an external output line called RAI (Receive Alarm Interrupt Indication) which is active HIGH and indicates the occurrence of one or more erroneous conditions detected in the MT90840 internal timing operation. The occurrences are indicated by bits PPCE, RXPAA, TXPAA and FSA at the ALS register.

Except for cases where the indications are masked by the MSK3-0 bits in the ALS register, the occurrence of any indication cause an RAI interrupt to be generated to the CPU. When any interrupt is masked by MSK3-0 bits the RAI output will not be activated. However, the interrupt indication will still be provided in the ALS bits.

To cause the RAI output signal or the indication bits to return to low again the CPU should write any value to ALS register.

Memory Block Programming Feature

The MT90840 device provides the user with the capability of programming the TPCM and RPCM high blocks. By using this feature, the four most significant bits of the TPCM and RPCM high

memories can be automatically programmed in all of their positions with a pattern defined by the CPU. This eases the system initialization routines by saving the CPU memory access time and extra write instructions. The procedure works as follows:

- a) The SEL2-0 bits in the Control register are used to select from either TPCM and RPCM high blocks.
- b) With a single write instruction, the user sets the Block Programming Data (BPD7-4) bits in the GPM register with the appropriate values to be loaded in the four most significant bits of the chosen memory (TPCM or RPCM high) and Block Programming Enable (BPE) bit to High. That action causes the contents of the BPD7-4 bits to be loaded into the four most significant bits of TPCM or RPCM.
- c) The user waits 250 μs to allow the TPCM (2430 positions) or RPCM (512) to be entirely loaded with the new pattern.
- d) After 250 μs timer expires, the user should write BPE bit = 0 (maintaining BPD7-4 and the other bits of the GPM register with desired values) and the process ends.

Procedures a, b, c, d have to be done twice if both TPCM and RPCM have to be initialized.

Timing Mode Initialization

On system power-up, the user should set the MT90840 IMS and TIM register to establish the data rates at the serial and parallel ports as well as the Timing Mode (1,2,3,4) that the device will operate. After this setting, the device will adjust its internal rate conversion and time interchange circuits to accommodate the different rates set at both data ports.

To perform the rate conversion functions between the serial and the parallel ports, the MT90840 device provides a phase alignment circuit that has to be initialized by the user before establishing any

connection. To initialize the internal timing, after the parallel and serial port reference clocks (PCKT/PCKR and C4/8R1/C4/8R2) are stable the DIN bit in the GPM register has to be set HIGH. The DIN bit will auto-reset itself returning to LOW. Once DIN returns to LOW, the access to internal memories and memory block programming features can be done. The Din bit procedure should be performed whenever C4/8R1 & 2 inputs are used.

JTAG PORT

The JTAG boundary-scan circuitry was designed according to the IEEE 1149.1a-1993 standard. The standard defines the test logic that should be included in an IC to verify interconnections between IC's at the board level. In addition, JTAG procedures can test the IC itself without interfering with the internal operation. Full details can be obtained in the IEEE 1149.1a-1993 standard.

Test Access Port

The test access port (TAP) has five signal and it provides access to the test logic defined by the JTAG standard. The TAP has the following connections:

- TCK: (Test clock input) Provides the clock to the test logic.
- TDI: (Test data input) Serial test instructions and data are shifted-in on this pin. This pin is pulled high when not driven.
- TDO: (Test data output) Serial data is output on this pin on the falling edge of TCK.
- TMS: (Test mode select input) Signal that controls the state transitions of the TAP controller. This pin is pulled high when not driven.
- $\overline{\text{TRST}}$: (Test reset input) Asynchronously initializes the TAP controller by putting it in the *Test-Logic-Reset* state. This pin is pulled high when not driven.

REGISTER DESCRIPTION

Interface Mode Selection Register (IMS) - READ/WRITE

DR1	DR0	PPS1	PPS0	ODE	-	-	FDC
7	6	5	4	3	2	1	0

DR1-0 Serial Port Data Rate Selection. These two bits select three different data rates at the serial inputs and outputs of the MT90840.

DR1	DR0	Data Rate
0	0	2.048 Mb/s
0	1	4.096 Mb/s
1	0	8.192 Mb/s
1	1	reserved

PPS1-0 Parallel Port Data Rate Selection. These two bits select three different data rates for the parallel port of the MT90840.

PPS1	PPS0	Data Rate
0	0	reserved
0	1	6.480 Mbyte/s. A 6.480 MHz clock should be applied at the parallel port clock input.
1	0	19.44 Mbyte/s. A 19.44 MHz clock should be applied at the parallel port clock input.
1	1	16.384 Mbyte/s. A 16.384 MHz clock should be applied at the parallel port clock input.

ODE Output Drive Enable. This bit controls the high impedance capabilities of the MT90840's output buffers on the serial and parallel data port sides (STo0/STo7, STi0/STi7 serial and PDo0-7 parallel outputs). If this bit is LOW, all serial streams and PDo0-7 are placed in high impedance. If this output is HIGH, all channels have their output drive enable control dictated by the per-channel OE feature operated in the OE bit locations of Transmit and Receive Connection memory high bits.

FDC Full Direction Control Enable. This mode can only be enabled if the serial port is running at 2.048 Mb/s data rate. When this bit is set HIGH, all the 16 ST-BUS lines can be configured as inputs or outputs streams with 64 Kb/s channel granularity. That implies that up to 512 channels can be received from the serial interface and transferred to the parallel port to perform an "insert function" or up to 512 channels can be dropped from the parallel port and transmitted to the serial interface. The definition of the channel direction is performed at the DC bit located in the Receive Path Connect Memory High bits. For applications at 4.096 and 8.192 Mb/s, the user should set this bit to LOW.

Timing Mode Register (TIM) - READ/WRITE

0	TM1	TM0	C4/8R	TCP	INTCLK	SFDi	PFDi
7	6	5	4	3	2	1	0

TM1-0 Timing Operation Modes. These 2 bits define four different timing modes described in the TIMING CONTROL section.

0	0	Timing Mode 1
0	1	Timing Mode 2
1	0	Timing Mode 3
1	1	Timing Mode 4

C4/8R C4/8R Input Reference Enable. If set HIGH, this bit enables the 4.096 or 8.192 MHz serial port reference clock to be taken from input pin C4/8R1. If LOW, the reference is taken from input pin C4/8R2 (default).

TCP Parallel Port Transmit Clock Polarity. To allow the MT90840 Parallel Port Transmit clock to comply with different 155 Mb/s framer backplanes, the TCP bit is provided to control the transmit edge of the clock (PCKT in TM1 or PCKR in TM2,3,4,5). This bit allows the rising (TCP=0) or the falling (TCP=1) edges of the transmit clock to be selected.

INTCLK Internal 4.096 MHz Clock Reference. For applications utilizing 19.44 or 16.384 MHz at the parallel port and requiring the automatic generation of the serial port 4.096 MHz clock (at the SPCKo output), the INTCLK bit can be used by the CPU to select if the 4.096 MHz clock is derived from the internal divider (INTCLK=1) or from the C4/8R1 input pin (INTCLK=0). When TM3 is enabled, the device automatically sets itself in the internal divider mode and the state of INTCLK has no effect. In TM1 and TM4, this bit is ignored.

SFDi F0 Direction Control. This bit is used in Timing Mode 2. When set HIGH, the F0 line becomes an input and the device is limited to receiving 4.096 and 8.192 MHz references as inputs. When the SFDi bit is set HIGH, INTCLK and SPCKo outputs are unused.

PFDi PPFRO Direction Control. This bit is used in Timing Mode 1. When HIGH, the PPFRO line becomes an input. When PFDi bit is LOW, PPFRO becomes an output.

Note: Bit 7 has to be always set to 0 by the CPU.

General Purpose Mode Register (GPM) - READ/WRITE

BPD7	BPD6	BPD5	BPD4	PPFP	DIN	SPFP	BPE
7	6	5	4	3	2	1	0

- BPD7-4** Block Programming Data bits 7-4. These bits carry the value to be loaded into the TPCM or RPCM high blocks whenever the Memory Block Programming feature is activated. Whenever BPE bit is set HIGH, the contents of bits BPD7-4 are loaded into the four most significant bits of TPCM or RPCM and the four least significant bits of TPCM and RPCM are zeroed.
- PPFP** Parallel Port Output Frame Pulse Polarity. This bit is used by the CPU to program the active polarity of the output PPFRO frame pulse. If set HIGH, the frame boundaries at the Parallel Port output will occur when PPFRO pulse signal is HIGH. If this bit is set LOW, the PPFRO output will indicate frame boundaries with a LOW active pulse. The transmit edge for the generation of PPFRO is determined by the TCP bit in the TIM register.
- DIN** Device Initialization. This bit should be set HIGH by the local CPU on every system power up as soon as the serial and parallel port rates are established by the CPU in the IMS register. If the MT90840 internal divider is utilized (INTCLK bit = 1) in TM2 or if TM4 and TM3 are selected, this bit is not used.
- SPFP** Serial Port Frame Pulse. In TM2 and TM3 this bit defines the polarity of the output frame pulse (F0) at the serial port. If high, the frame boundary is set as a positive going frame pulse. If low, the frame boundary it is set as a negative going pulse. Whenever this bit is changed by the local CPU, the associated bit transmit and sampling edges will adapt to the interface timing specifications provided at the end of this document.
- BPE** Block Programming Enable. This bit activates the memory block programming feature. It should be set HIGH after the SEL0-2 bits in the Control register select the memory block section to be affected. The BPE and BPD7-4 bits in this register have to be defined in the same write operation. Once the BPE bit is set HIGH, the user should wait at least 250 μ s and then write BPE=0 to finish the operation.
- Note:** Whenever the CPU writes BPE=1 (to start) and then BPE=0 (to finish), the previous logical value of the other 7 bits in the GPM register have to be maintained to avoid any change in the device's settings.

Alarm Status Register (ALS) - READ/WRITE

MSK3	MSK2	MSK1	MSK0	PPCE	RXPAA	TXPAA	FSA
7	6	5	4	3	2	1	0

- MSK3-0** Mask Alarm Bits 3-0. The MSK3-0 bits will mask the interrupt output signal. MSK3 masks PPCE, MSK2 masks RXPAA, MSK1 masks TXPAA and MSK0 masks FSA. If MSKx is set HIGH, the corresponding interrupt is enabled. If set LOW, the corresponding interrupt is masked. On system power-up all interrupts are masked.
- PPCE** Parallel Port Frame Counter Error bit. This indication is only used in TM2 and TM4. This bit is set HIGH whenever there is a wrong number of clock pulses between frame synchronization signals on the parallel port side. Under normal operation, different number of clock pulses are expected depending on the parallel port data rate selected in the IMS register (2430, 2048 or 810). In TM1 and TM3 this bit should be ignored and the MSK3 bit should be high.
- RXPAA** RX Phase Alignment Alarm. Used in TM2 operation. This bit goes HIGH whenever the C4/8R1 or C4/8R2 input references go out of phase in relation to the parallel port transmit/receive clock (PCKR). Note that a CPU write access to the RPCM memory as RXPAA goes HIGH is not valid. Upon the RXPAA indication, the previous write generation at RPCM should be repeated.
- TXPAA** TX Phase Alignment Alarm. Used in TM1 operation. This bit goes HIGH whenever the PCRT input reference goes out of phase in relation to the C4/C8R1&2 inputs. When HIGH, TXPAA indicates that the MT90840 has moved the position of the active PPFRO and a slip at the parallel data port output has occurred.
- FSA** Frame Slip on Elastic Buffer. This condition occurs when either an overflow or underun conditions on the parallel port's elastic buffer have been detected. NOTE: In TM2,3, and 4 the user has to mask this bit.

Control Register (CR) - READ/WRITE

SEL2	SEL1	SEL0	HA11	HA10	HA9	HA8	HA7
7	6	5	4	3	2	1	0

SEL2-0 Memory Select bits. These bits are used by the CPU to select the internal memories of the device for read or write operations. SEL2-0 bits have to be accessed before any READ/WRITE operation is performed in the internal memories.

SEL2	SEL1	SEL0	Memory Selected for RD/WR operation
0	0	0	Receive Path Connect Memory Low (RPCM low)
0	0	1	Receive Path Connect Memory High (RPCM high)
0	1	0	Receive Path Data Memory
0	1	1	Enable Memory Block Programming feature for RPCM high bits
1	0	0	Transmit Path Connect Memory Low (TPCM low)
1	0	1	Transmit Path Connect Memory High (TPCM high)
1	1	0	Transmit Path Data Memory
1	1	1	Enable Memory Block Programming feature for TPCM high bits

HA11-7 High Address Bits 11-7. These bits are used along with A0-A6 input lines to address the MT90840 internal memories. See RPCM, TPCM, RPDM and TPDM Address Mapping section for more details.

For the Transmit Path Memories:

Serial Port Interface Speed	Number of Serial Port Input and Output Streams	STA bits and input address lines used to select the 2430-position deep Transmit Path Connection Memory (12 addr lines needed).	STA bits and Address input lines used to select the 512-position Transmit Path Data Memory (9 addr lines needed).
2 Mb/s	16 i/o (512 channels)	HA11 to HA7 + A6 to A0	HA8 to HA7 + A6 to A0
4 Mb/s	8i x 8o (512 channels)	HA11 to HA7 + A6 to A0	HA8 to HA7 + A6 to A0
8 Mb/s	4i x 4o (512 channels)	HA11 to HA7 + A6 to A0	HA8 to HA7 + A6 to A0

For the Receive Path Memories:

Serial Port Interface speed	Number of Serial Port Input and Output Streams	STA bits and input address lines used to select the 2430-position deep Receive Path Data Memory (12 addr lines needed).	STA bits and Address input lines used to select the 512-position Receive Path Connect Memory (9 addr lines needed).
2 Mb/s	16 i/o (512 channels)	HA11 to HA7 + A6 to A0	HA8 to HA7 + A6 to A0
4 Mb/s	8i x 8o (512 channels)	HA11 to HA7 + A6 to A0	HA8 to HA7 + A6 to A0
8 Mb/s	4i x 4o (512 channels)	HA11 to HA7 + A6 to A0	HA8 to HA7 + A6 to A0

INTERNAL MEMORY DESCRIPTION

Transmit Path Connect Memory High (TPCM High) - This is an 8-bit wide x 2430 position deep memory.

OE/ CTo0	PPBY	MC	CTo1	CTo2/ AB11	CTo3/ AB10	AB9	AB8	(Tx Path CM High Bits)
7	6	5	4	3	2	1	0	

- OE/CTo0** Output Enable. This bit provides per channel tri-state control on the parallel port side. It controls the MT90840 parallel output drivers to disable (tri-state, when LOW) or enable (when HIGH) the transmission of data from the device. The contents of this bit will be clocked to the CTo0 output pin at the parallel port rate.
- PPBY** Parallel Port Bypass enable. This bit identifies which channels are going to be bypassed (PPBY=HIGH) from the parallel input to parallel output ports of the MT90840. The use of this bit is only allowed in Timing Modes 1 and 2. The channels that are not bypassed (PPBY=LOW) can be used for insertion of data from the serial port side. In TM3 and 4 this bit is ignored.
- MC** Message Channel. The message channel contents is provided by the CPU in bits AB0-7 in the TP Connection Memory low. If MC=1 the contents of the corresponding location of TPCM LOW is output on the corresponding channel at the parallel data port interface. If MC=0 the contents of the programmed location in TPCM LOW act as an address for the Data Memory and so it determines the source channel for the connection. Depending on the timing mode selected the source of the connection can be an input channel from either serial (TM1, 2, or 3) or parallel (TM4) data ports.
- CTo1-3** External Control lines 1-3. These three lines are used by the CPU to program (along with CTo0) three additional external control lines that can be used externally. Like CTo0, the contents of these lines will be transmitted to pins CTo1-3 at the parallel port rate. Note: bits CTo2 and CTo3 cannot be used in Timing Mode 4.
- AB8-11** Source Channel Address bits 8-11. In **Timing Mode 4**, these bits are used along with bits AB0-7 in the TPCM low to select up to 2430 source channels from the parallel port input to be connected to any of the 2430 available on the parallel port output side.

In all Timing Modes except TM 4, only bit AB8 is used along with bits AB0-7 in the TPCM low memory to select 512 serial source channels from the serial port side to be connected to any 512 output parallel channels of the 2430 available on the parallel port side.

Transmit Path Connect Memory Low (TPCM Low) - This is an 8-bit wide x 2430 position deep memory. The contents of each position is shown below.

AB6	AB6	AB5	AB4	AB3	AB2	AB1	AB0	(Tx Path CM Low Bits)
7	6	5	4	3	2	1	0	

AB7-0 Source Channel Address bits. In timing modes 1, 2 and 3 these 8 bits are used along with bit AB8 in the TPCM high memory to select up to 512 serial source channels from the serial port side to be connected to any 512 (out of 2430) output channels available on the parallel port side. See table for details.

In Timing Mode 4, these 8 bits are used along with bits AB8-11 in the TPCM high memory to select up to 2430 source channels from the parallel port input to be connected to any of the 2430 available on the parallel port output side.

If Message mode is selected at TPCM HIGH bits then the contents of the AB0-7 bits in the TPCM low locations are transmitted on to the corresponding channels at the PDo0-7 lines until it is changed by the CPU.

UTILIZATION OF THE TPCM HIGH AND LOW BITS WHEN PROGRAMMING SOURCE CHANNEL IN THE SERIAL PORT			
SERIAL STREAM and CHANNEL ALLOCATION		SOURCE STREAM ADDRESSING	SOURCE CHANNEL ADDRESSING
2 Mb/s	16 i/o (512 channels)	AB5,AB6,AB7,AB8 (up to 16 streams)	AB0 to AB4 used to select up to 32 channels per stream
4 Mb/s	8i x 8o (512 channels)	AB6, AB7, AB8 used to select up to 8 streams	AB0 to AB5 used to select up to 64 channels per stream
8 Mb/s	4i x 4o (512 channels)	AB7, AB8 used to select up to 4 streams	AB0 to AB6 used to select up to 128 channels per stream

SOURCE CHANNEL ADDRESSING IN TM4 AT THE PARALLEL PORT INPUT	
16.384 Mb/s	AB0 - AB10 (up to 2048 channels)
19.44 Mb/s	AB0 - AB11 (up to 2430 channels)

Receive Path Connect Memory High (RPCM High) - This is a 7 bit x 512 position deep memory. Used only in TM1, 2 & 3.

-	MC	DC	OE	AB11	AB10	AB9	AB8	(Rx Path CM High Bits)
7	6	5	4	3	2	1	0	

MC Message Channel on the serial data port. The message channel contents is provided by the CPU in bits AB0-7 in the RP Connection Memory low. If MC=1 the contents of the corresponding location of RPCM LOW is output on the corresponding channel at the serial data port interface. If MC=0 the contents of the programmed location in RPCM LOW act as an address for the RP Data Memory and so it determines the source of the connection (input channels from the PDI0-7 port).

DC Direction Control bit. Used to enable per channel direction control on the serial data port. This bit assumes a different operation depending on the state of FDC bit at the IMS register. If FDC= LOW with data rates at 4.096 or 8.192 Mb/s, the 512 DC bits will define the direction of each of the 512 channels available at the ST0-7 lines. If DC bit is LOW, then the corresponding output channel on ST0-7 lines becomes an input and the corresponding input channel on ST10-7 becomes an output.

If FDC bit = HIGH (serial port at 2.048 Mb/s), then this 512-bit memory can be used to control the direction of each individual 64 Kb/s time-slot present on the 16 serial I/O lines in a non-symmetrical basis; i.e, all 512 channels can be configured as outputs or inputs or any mix combination. Note that the CPU still has to set the OE bit to enable the output buffers on all channels defined as outputs. If DC bit=0 in a specific location of RPCM High, the corresponding channel is defined as input. If DC=1 a channel is defined as output.

OE Output Enable. Per channel tri-state control for up to 512 channels on the serial port side. If FDC bit is HIGH, the 512 OE bit locations enable the driver for current ST channel on any of the 16 serial streams, unless the channel is defined as an input by the DC bit.

In 4.096 and 8.192 Mb/s modes, the 512 OE bit locations are active and enable the output buffers for the corresponding channel on ST0-7 lines.

AB8-11 Source Channel Address bits. These 4 bits are used along with AB0-7 to select any of the 2430 parallel incoming channels from the Parallel Port and determine the switch connection to the 512 possible destination channels on the serial port.

Receive Path Connect Memory Low (RPCM Low) - This is a 8 bit x 512 position deep memory. Used only in TM1, 2 & 3.

AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0	(Rx Path CM Low Bits)
7	6	5	4	3	2	1	0	

AB0-7 Source Channel Address bits. In switching mode (MC bit=0), these 8 bits are used along with AB8-11 to select any of the 2430 incoming channels from the Parallel Port and determines the switch connection to the 512 possible destination on the serial port. In message mode (MC bit=1), these 8 bits are used by the local CPU to program per channel message pattern on the serial port interface output channels.

UTILIZATION OF THE RPCM HIGH AND LOW BITS WHEN PROGRAMMING SOURCE CHANNELS IN THE PARALLEL PORT								
AB11-7	AB6	AB5	AB4	AB3	AB2	AB1	AB0	SOURCE
0 0 0 0 0	0	0	0	0	0	0	0	Channel 0
.
0 0 0 0 0	1	1	1	1	1	1	1	Channel 127
0 0 0 0 1	0	0	0	0	0	0	0	Channel 128
.
0 0 0 0 1	1	1	1	1	1	1	1	Channel 255
.	0	0	0	0	0	0	0	.
(from 00010 to 01111)								(Channels 256 to 2047)
.	1	1	1	1	1	1	1	.
1 0 0 0 0	0	0	0	0	0	0	0	Channel 2048
.
.
1 0 0 1 0	1	1	1	1	1	0	1	Channel 2429

Address Mapping of the Internal RPCM and TPDM (both have 512 positions)

Note: To access the internal Receive Path Connection memory, the bit A7 has to be maintained HIGH; i.e, only bits A0 to A6 and HA8,HA7 in the control register will be used for addressing the internal memories.

Address to be provided to MT90840									Channel
HA8	HA7	A6	A5	A4	A3	A2	A1	A0	LOCATION
0	0	0	0	0	0	0	0	0	Channel 0
0	0	0	0	0	0	0	0	1	Channel 1
.	.	.	0
.	.	.	0
.	.	.	0
.	.	.	0
0	0	0	0	1	1	1	1	1	Channel 31
0	0	0	1	0	0	0	0	0	Channel 32
.
0	0	0	1	1	1	1	1	1	Channel 63
0	0	1	0	0	0	0	0	0	Channel 64
.
0	0	1	1	1	1	1	1	1	Channel 127
0	1	0	0	0	0	0	0	0	Channel 128
.
0	1	1	1	1	1	1	1	1	Channel 256
1	0	0	0	0	0	0	0	0	Channel 256
.
1	1	1	1	1	1	1	1	1	Channel 512

Selection between Serial Stream and Channel

Serial Stream and Channel Allocation		Stream Addressing	Channel Addressing
2 Mb/s	16 i/o (512 channels)	HA8,HA7,A6,A5 (up to 16 streams)	A0 to A4 used to select up to 32 channels per stream
4 Mb/s	8i x 8o (512 channels)	HA8, HA7,A6 used to select up to 8 streams	A0 to A5 used to select up to 64 channels per stream
8 Mb/s	4i x 4o (512 channels)	HA8, HA7 used to select up to 4 streams	A0 to A6 used to select up to 128 channels per stream

Address Mapping of the Internal TPCM and RPDM (both have 2430 positions)

Note: To access the internal Transmit Path Connection memory and the Receive Path Data memory, the bit A7 has to be maintained HIGH; i.e., only bits A0 to A6 and HA7-11 in the control register will be used for addressing the internal memories.

HA11-7	A6	A5	A4	A3	A2	A1	A0	LOCATION
0 0 0 0 0	0	0	0	0	0	0	0	Channel 0
. 0 0 0 0 0	. 1	. Channel 127						
0 0 0 0 1	0	0	0	0	0	0	0	Channel 128
. 0 0 0 0 1	. 1	. Channel 255						
. (from 00010 to 01111) .	0 1	 (chann 256 to 2047)						
1 0 0 0 0	0	0	0	0	0	0	0	Channel 2048
. . 1 0 0 1 0	. . 1	. . 1	. . 1	. . 1	. . 1	. . 0	. . 1	. . Channel 2429

Applications

Distributed Isochronous Network

Low latency isochronous backbones provide capabilities necessary for the deployment of systems that require cost effective implementation, high bandwidth, predictable data transfer delays and direct synchronization with the wide area network.

Some applications in Computer Telephony Integration (CTI) require a large amount of bandwidth to be transported between multiple chassis within the same location, or between locations separated from each other. The MT90840 is ideal for implementing physically distributed transport and switching systems for multi-chassis or inter-shelf communications.

The MT90840 device bridges existing Mitel ST-BUS components into a new networking environment whereby mixed data, voice and video signals can be time-interchanged or multiplexed from serial PCM

streams onto a serial high speed Time Division Multiplex (TDM) isochronous backbones operating at SONET rates such as 51 (STS-1) or 155 Mb/s (STS-3).

Today, transmission links operating at SONET rates utilize serial-to-parallel and parallel-to-serial converter devices (or framers) which perform embedded framing functions and give the user the access to the payload of the high speed frame. The MT90840 device provides an 8-bit bidirectional parallel data port (PDP) which directly interfaces to those high speed framer's user data interface, allowing designers to build distributed networking systems with interconnection speeds up to 155 Mb/s. Figure 12 depicts an example of distributed networking application in Computer Telephony Integration (CTI) systems.

The device's clock synchronization and reference options allow many applications and topologies when isochronous TDM backbones are required. Two major clock synchronization schemes provided by the MT90840 allow the serial port interface (ST-

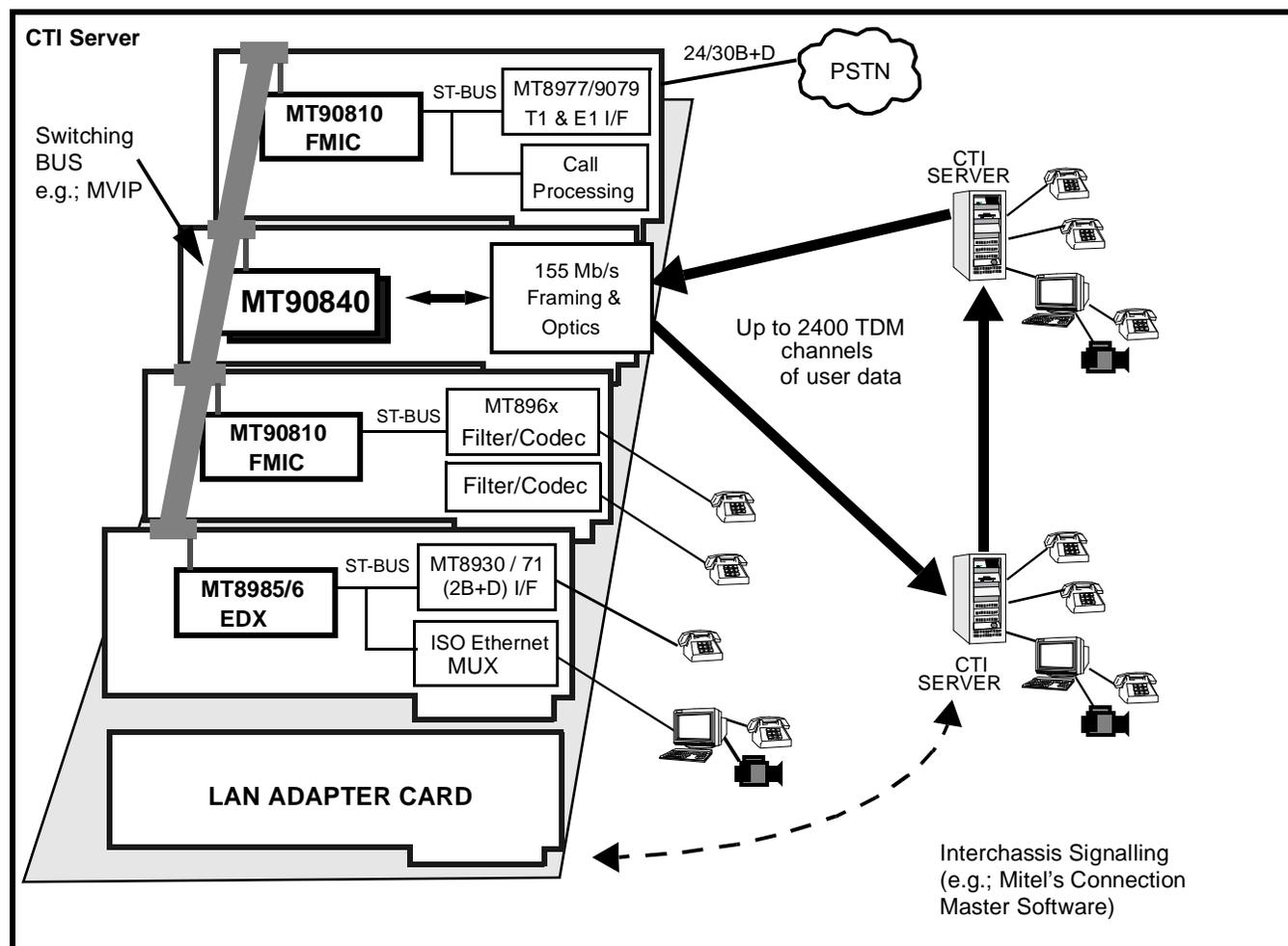


Figure 12 - CTI Distributed Architecture Implemented with the MT90840

BUS) to provide the master clock and frame reference signals for the distributed high speed backbone (master operation) or to derive the entire ST-BUS clock and frame reference signals from the high speed backbone (slave operation).

This type of synchronization scheme may be used in applications such as the proposed MVIP multi-chassis level 3 interface (MC-3 system) utilizing point-to-point or point-to-multipoint switching connections.

When the MT90840 device operates in a ring type of application the Parallel Data Bypass mode is provided to allow all or part of the received input parallel data to be bypassed to the output parallel port feeding the ring back with the data which is not destined (to be dropped) to the local station. The data destined for the local station can be dropped through CPU programming. In this mode, the CPU has the full control on managing the outgoing bandwidth (from the serial interface to the high speed link) so that it does not contend with the bypassed data.

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	$V_{DD} - V_{SS}$		0	6	V
2	Voltage on Digital Inputs	V_I	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Voltage on Digital Outputs	V_O	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40	25	+85	°C	
2	Positive Supply	V_{DD}	4.75	5.0	5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
I N P U T S	Supply Current	I_{DD}			200	mA	Outputs unloaded
	Input High Voltage	V_{IH}	2.0			V	
	Input Low Voltage	V_{IL}			0.8	V	
	Input Leakage (input pins) Input Leakage (I/O pins)	I_{IL}		34	5 100	μ A	V_I between V_{SS} and V_{DD}
	Input Pin Capacitance	C_I		8		pF	
O U T P U T S	Output High Voltage	V_{OH}	2.4			V	$I_{OH} = 10$ mA
	Output High Current	I_{OH}	10	15		mA	Sourcing. $V_{OH}=2.4$ V
	Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 5$ mA
	Output Low Current	I_{OL}	5	10		mA	Sinking. $V_{OL} = 0.4$ V
	High Impedance Leakage	I_{OZ}			5	μ A	V_O between V_{SS} and V_{DD}
	Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

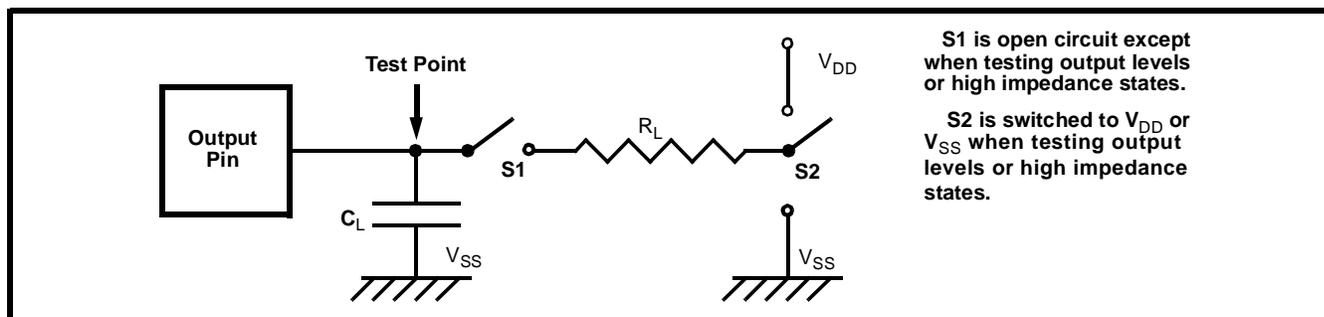


Figure 13 - Output Test Load

AC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	CLK Period at C4/8R1 input 2.048 Mb/s & 4.096 Mb/s 8.192 Mb/s	t_{clk}	200 100	244 122		ns ns	
	CLK Period 2.048 Mb/s & 4.096 Mb/s SPCKo generated internally		200			ns	
	2.048 Mb/s and 4.096 Mb/s SPCKo generated from C4/8R1 input reference (external source)		220			ns	considering C4/8R1 input with 220 ns cycle
	8.192 Mb/s (expected at C4/8R1 input - only external source operation)		100			ns	
2	CLK Period Width HIGH at C4/8R1 input 2.048 Mb/s & 4.096 Mb/s 8.192 Mb/s	t_{clkh}	85 50	122 61		ns ns	
	CLK Period 2.048 Mb/s & 4.096 Mb/s SPCKo generated internally		97			ns	PCKR with 45/55% duty cycle
	2.048 Mb/s and 4.096 Mb/s SPCKo generated from C4/8R1 input reference (external source)		110	122		ns	considering C4/8R1 input with min. 115ns semi-cycle
	8.192 Mb/s (expected at C4/8R1 input - only external source operation)		50			ns	
3	CLK Period Width LOW at C4/8R1 input 2.048 Mb/s & 4.096 Mb/s 8.192 Mb/s	t_{clkl}	85 50	122 61		ns ns	
	CLK Period (TM2,3,5) 2.048 Mb/s & 4.096 Mb/s SPCKo generated internally		110			ns	PCKR with 45/55% duty cycle
	2.048 Mb/s and 4.096 Mb/s SPCKo generated from C4/8R1 input reference (external source)		110			ns	considering C4/8R1 input with min. 115ns semi-cycle
	8.192 Mb/s (expected at C4/8R1 input - only external source operation)		50			ns	
4	CLK rise/fall time	t_t		5		ns	
5	F0 output delay in 2.048 , 4.096 and 8.192 Mb/s	t_{df}	20			ns	
6	Frame Pulse Setup from CLK input reference 2.048 , 4.096 and 8.192 Mb/s	t_{frs}	10			ns	
7	Frame Pulse Hold Time from CLK input reference 2.048, 4.096 and 8.192 Mb/s	t_{frh}	20			ns	
8	Frame pulse width 2.048, 4.096, 8.192 Mb/s	t_{frw}	35			ns	$C_L=150pF$ $R_L=1K$
9	STo delay - active to High-Z, 2.048 and 4.096 Mb/s 8.192 Mb/s	t_{az}			80 45	ns ns	$C_L=150pF$ for 2, 4 & 8 Mb/s, $R_L=1K$

AC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
10	STo delay from High-Z to active 2.048 and 4.096 Mb/s 8.192 Mb/s	t_{za}			80 45	ns ns	$C_L=150\text{pF}$ for 2, 4 & 8Mb/s, $R_L=1\text{K}$
11	STo Delay from CLK ref. transmit edge 2.048 and 4.096 Mb/s 8.192 Mb/s	t_{sod}			80 45	ns ns	$C_L=150\text{pF}$ for 2, 4 & 8 Mb/s, $R_L=1\text{K}$
12	STi Set-up Time from CLK sampling edge 2.048 Mb/s 4.096 Mb/s and 8.192 Mb/s	t_{stis}	20 5			ns ns	
13	STi Hold Time from CLK sampling edge 2.048 Mb/s 4.096 Mb/s and 8.192 Mb/s	t_{stih}	20 10			ns ns	

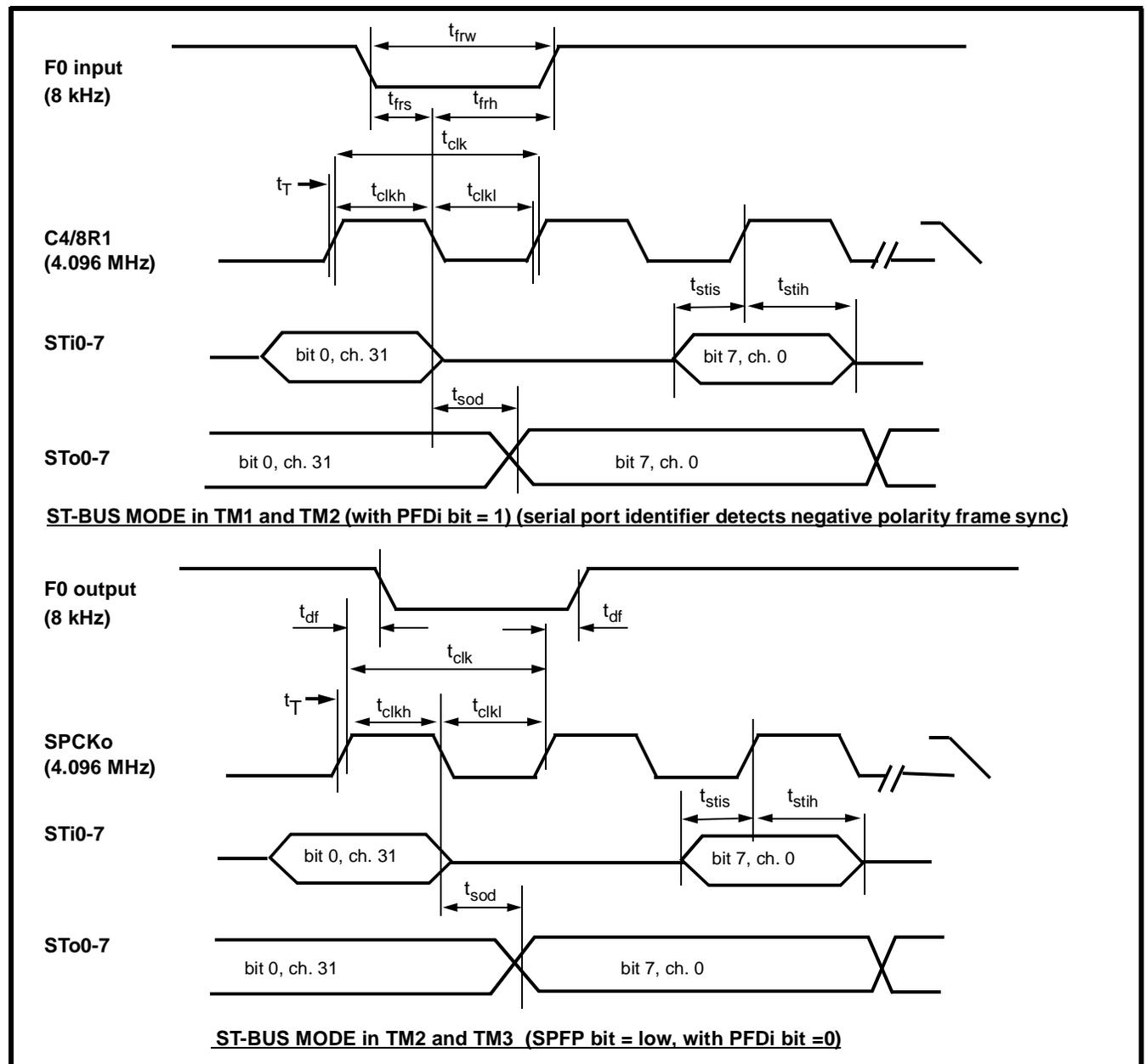


Figure 14 - Serial Port Timing for 2.048 Mb/s Operation (ST-BUS Mode)

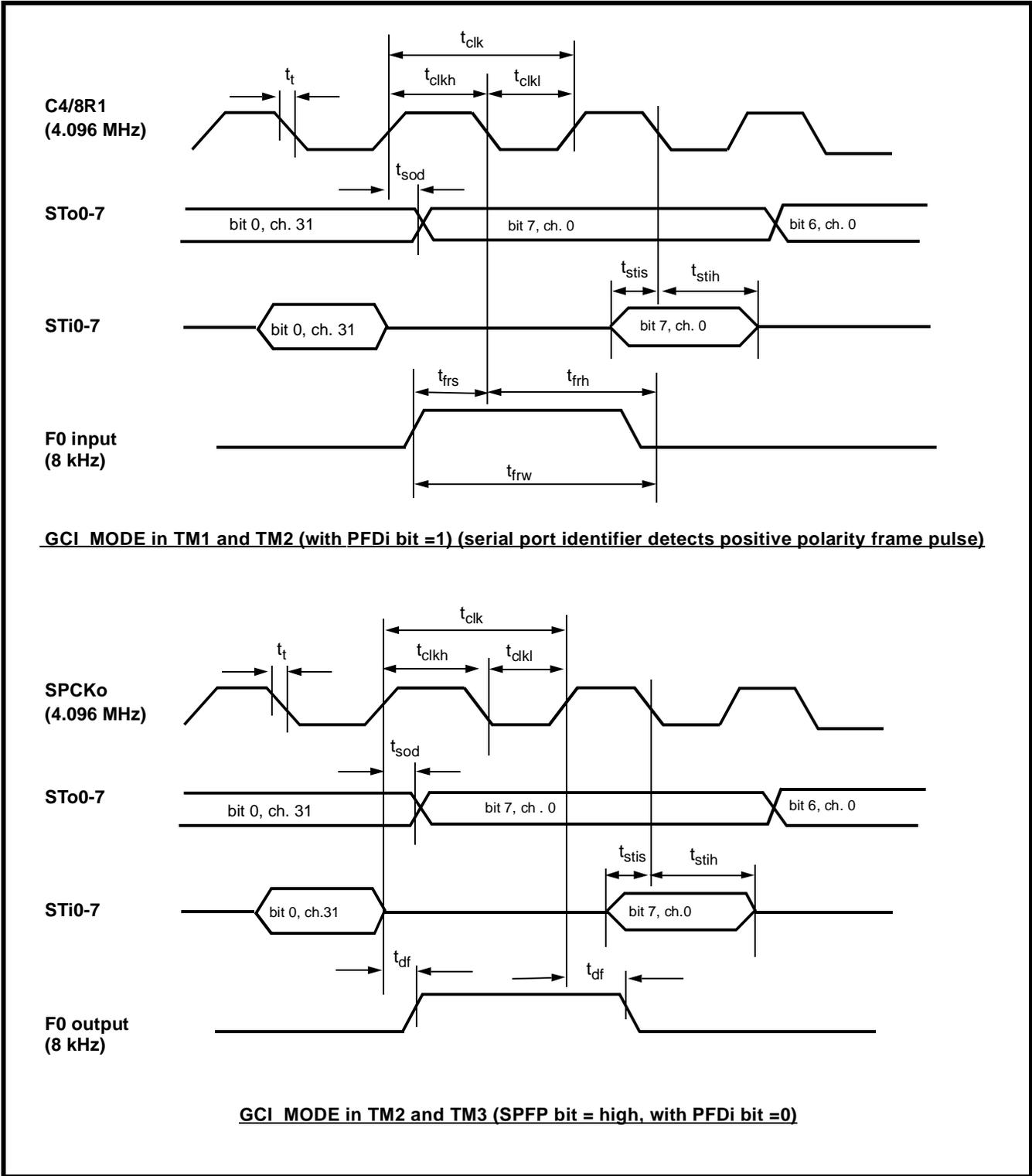


Figure 15 - Serial Port Timing for 2.048 Mb/s in GCI Interface Mode

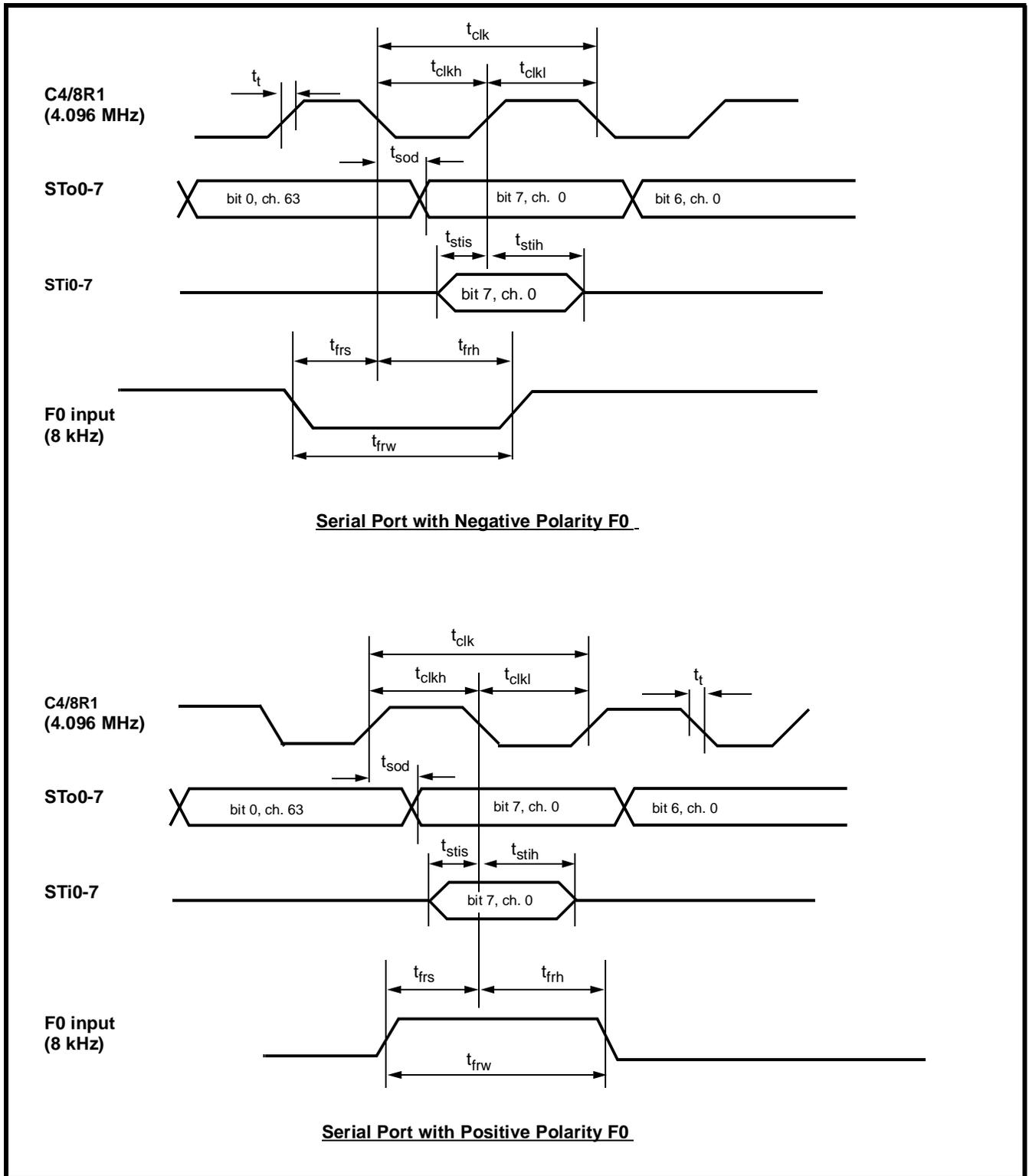


Figure 16 - Serial Port Timing for 4.096 Mb/s Operation - TM1 and TM2 (with PFDi bit = 1)

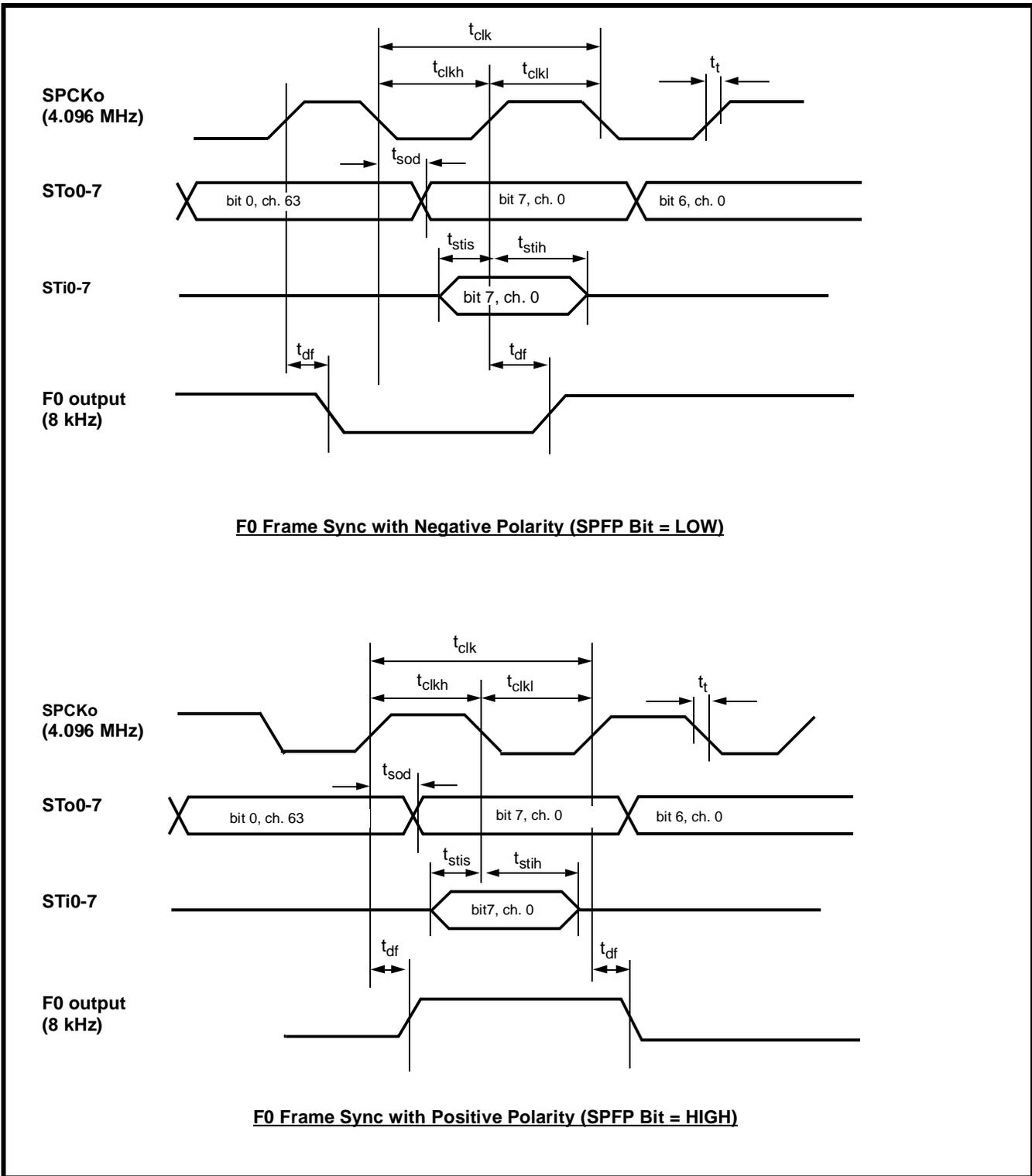


Figure 17 - Serial Port Timing for 4.096 Mb/s Operation - TM2 and TM3 (with PFDi bit = 0)

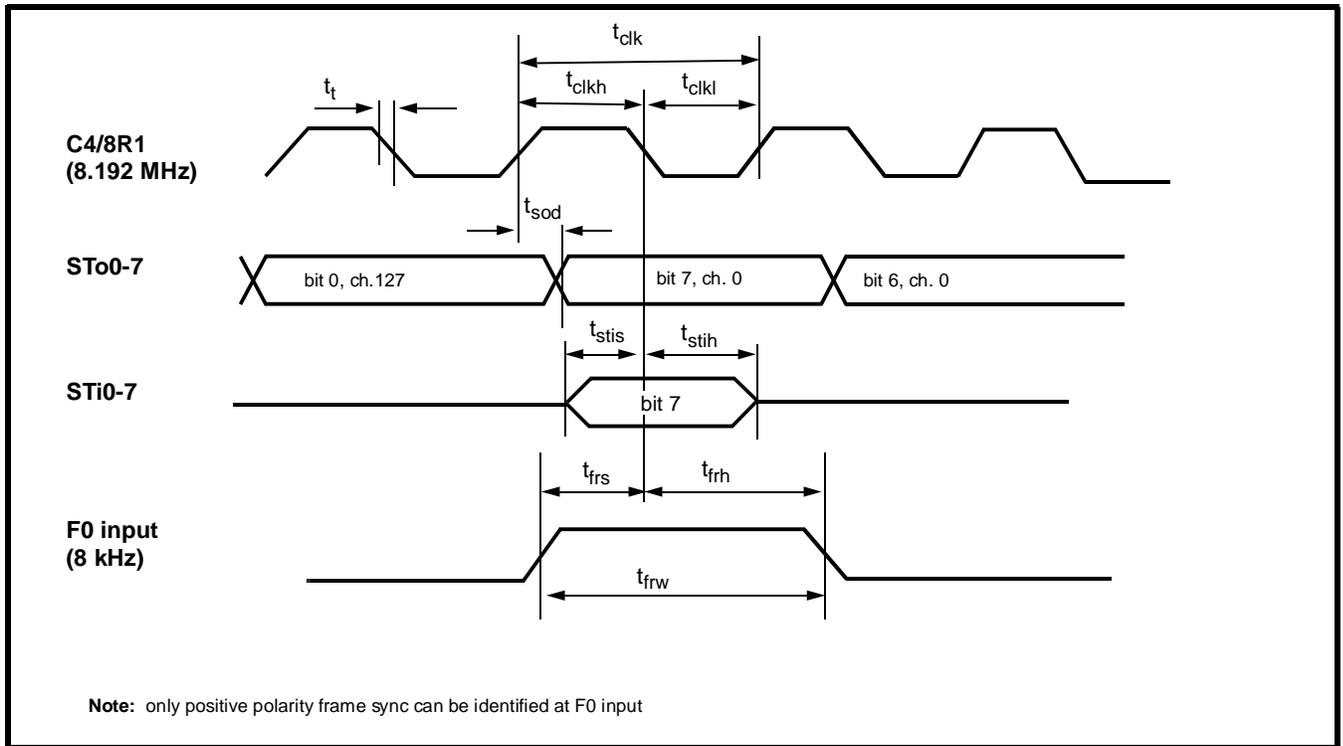


Figure 18 - Serial Port Timing for 8.192 Mb/s - TM1 and TM2 (with PFDi bit = 1)

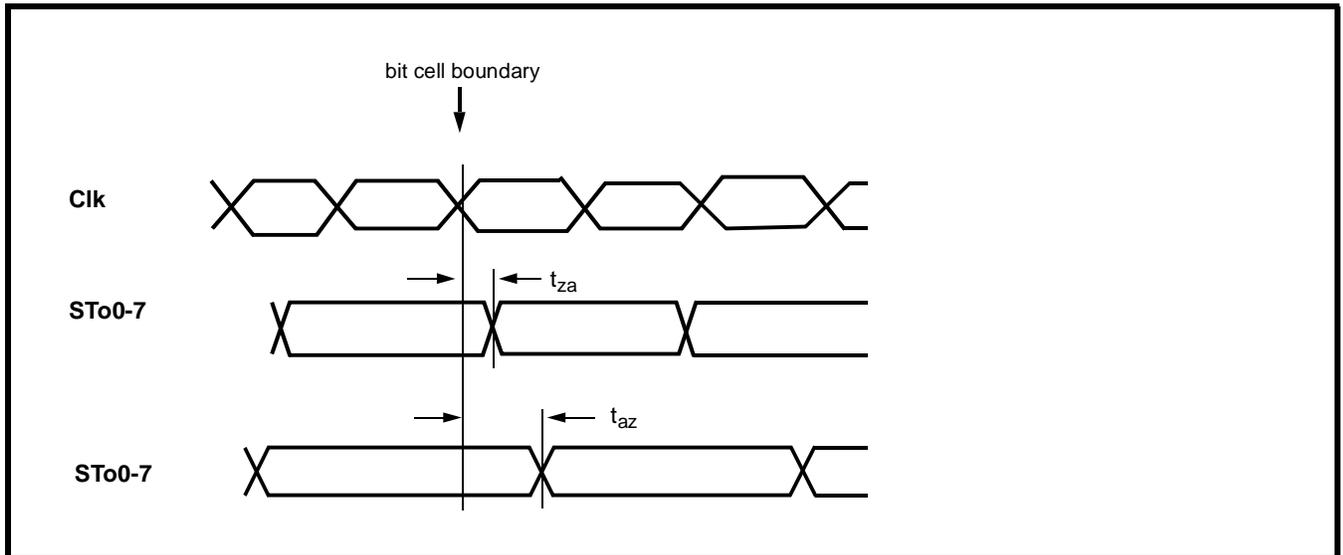


Figure 19 - Per-Channel Tri-State Characteristics in all Data Rates

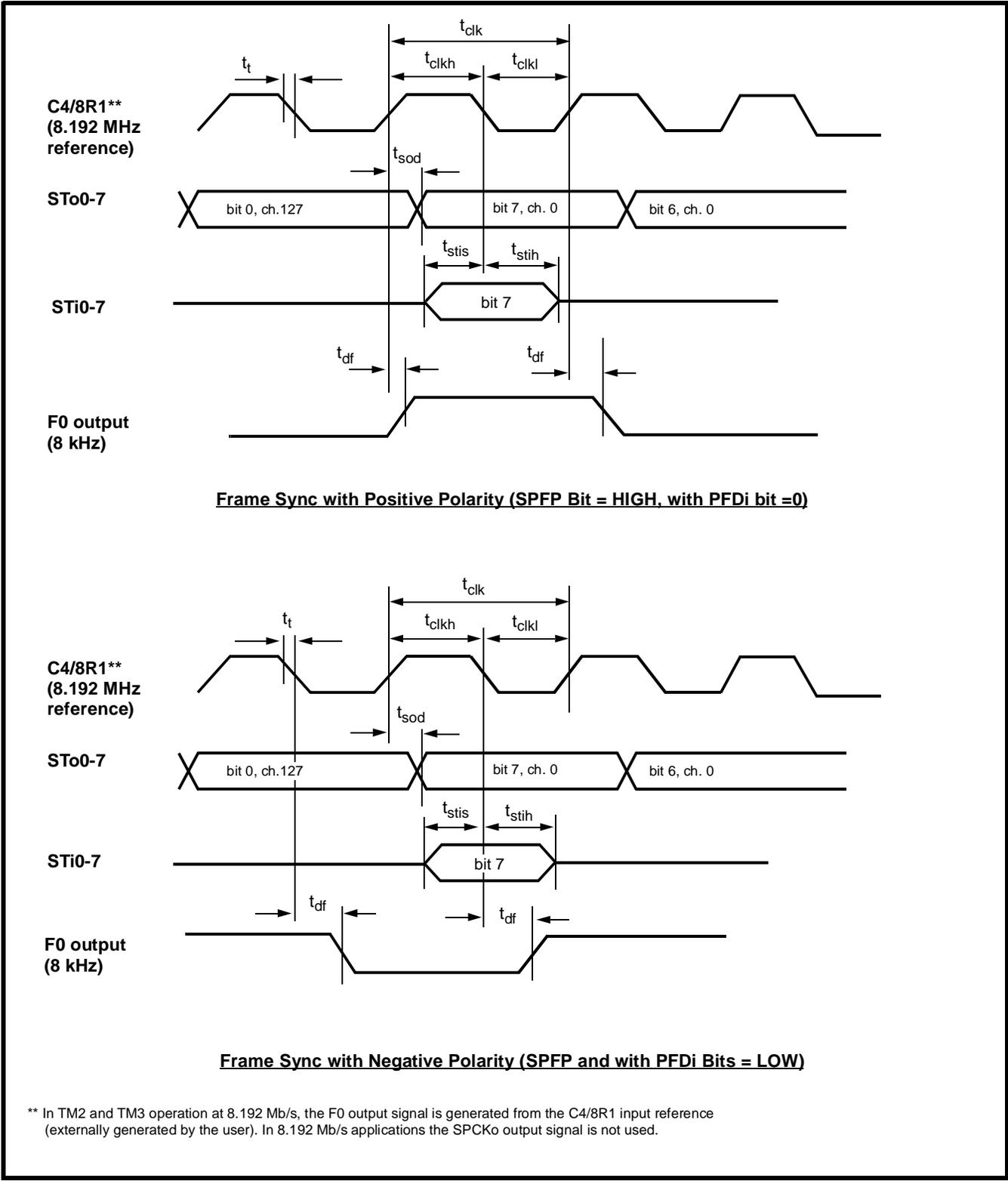


Figure 20 - Serial Port Timing for 8.192 Mb/s - Timing Modes 2 and 3

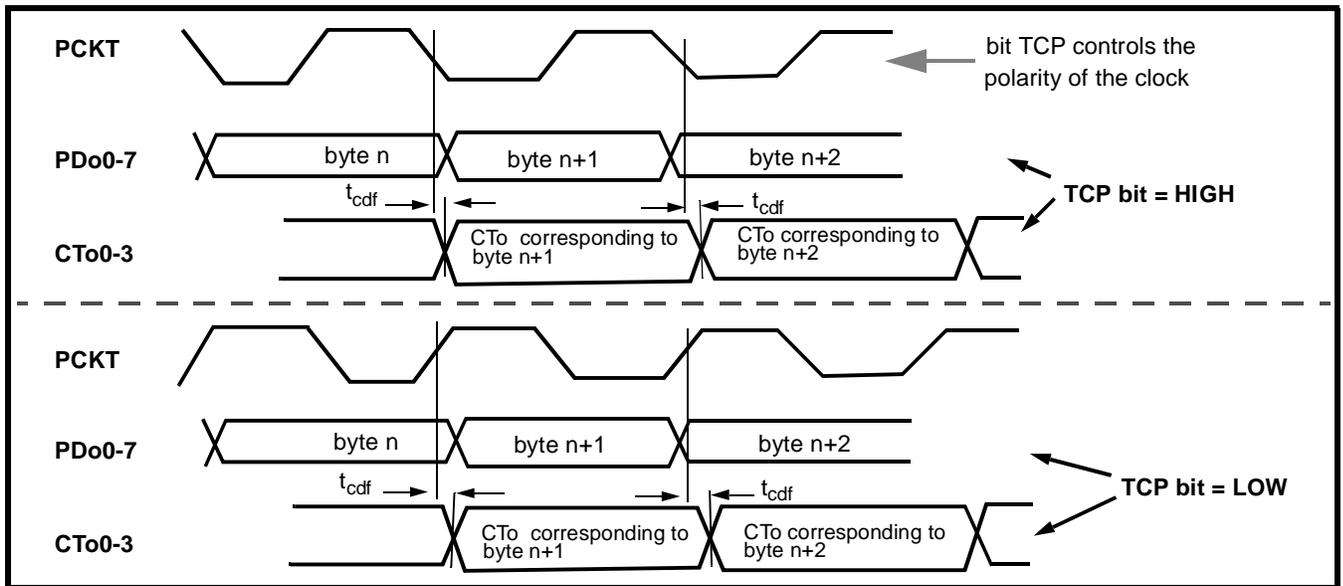


Figure 21 - Timing for the Parallel Port External Control Lines CTo0-3

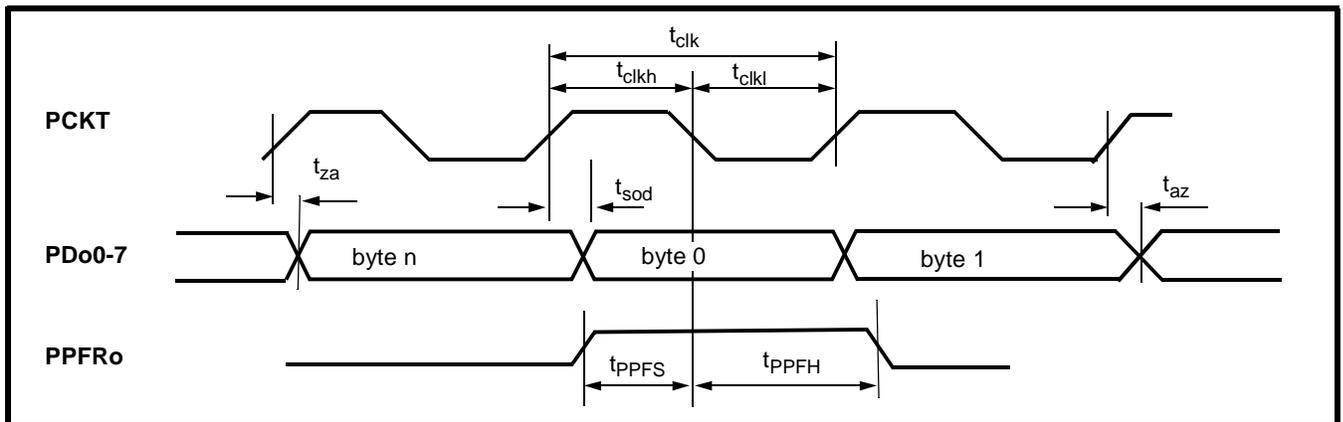
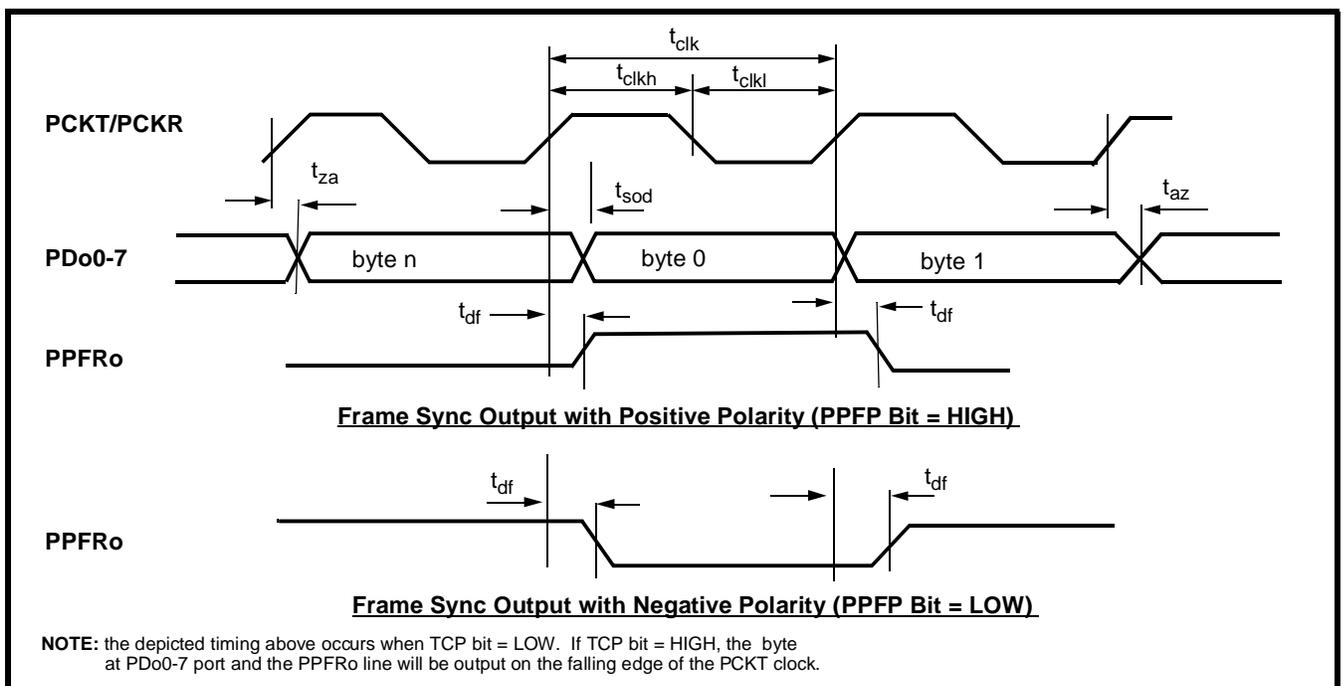


Figure 22 - TM1 Parallel Port Transmit Timing (PFDi bit = 1)



NOTE: the depicted timing above occurs when TCP bit = LOW. If TCP bit = HIGH, the byte at PDo0-7 port and the PPFRO line will be output on the falling edge of the PCKT clock.

Figure 23 - Parallel Port Transmit Timing (with PFDi bit = 0)

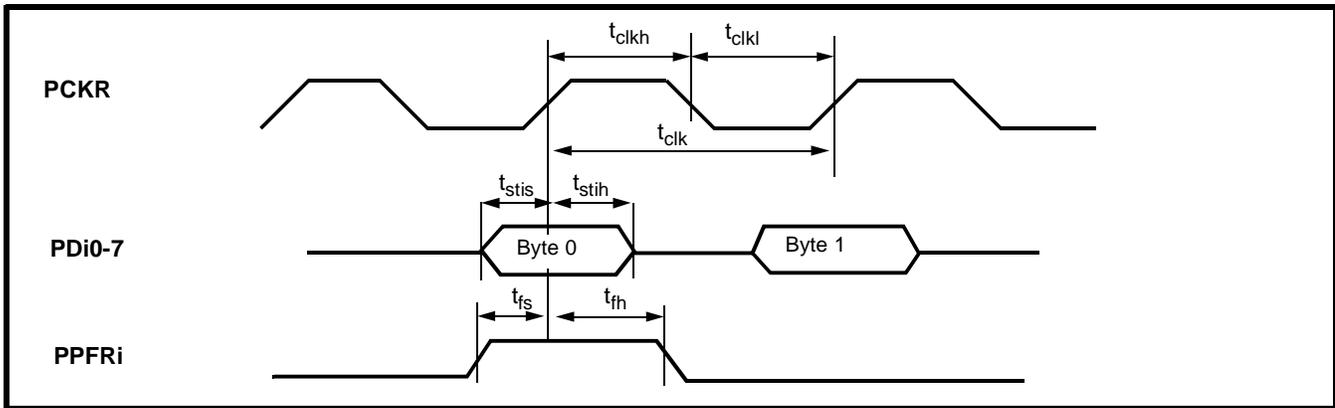


Figure 24 - Parallel Port Receive Timing

AC Electrical Characteristics - Parallel Data Port

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
1	PCKT clock period	t_{clk}		51.4		ns	
2	PCKT high time	t_{clkh}	20			ns	
3	PCKT low time	t_{clkl}	20			ns	
4	PCKT rise/fall time	t_t		2		ns	
5	PPFRo output delay	t_{df}			35	ns	$C_L=50pF, R_L=1K$
6	CTo0-3 output delay	t_{cdf}			35	ns	$C_L=50pF, R_L=1K$
7	Frame Pulse Setup from PCKR input reference	t_{frs}	5			ns	
8	Frame Pulse Hold Time from PCKR input reference	t_{frh}	5			ns	
9	Frame pulse width	t_{frw}	35			ns	$C_L=50pF, R_L=1K$
10	PDo delay from active to High-Z	t_{za}			35	ns	$C_L=50pF, R_L=1K$
11	PDo delay from High-Z to active	t_{az}			35	ns	$C_L=50pF, R_L=1K$
12	PDo delay from PCKR/PCKT transmit edge	t_{sod}			35	ns	$C_L=50pF, R_L=1K$
13	PDi Set-up Time from PCKR sampling edge	t_{stis}	5			ns	
14	PDi Hold Time from PCKR sampling edge	t_{stih}	5			ns	
15	Phase Variation between PCKT and C4/8R1 & 2 inputs	t_{pv}	100		- 100	ns	C4/8R1 & 2 at 4.096 MHz with 50% duty cycle
16	PPFRo Setup time (PFDi bit = 1)	t_{ppfs}	5			ns	
17	PPFRo Hold time (PFDi bit = 1)	t_{ppfh}	5			ns	

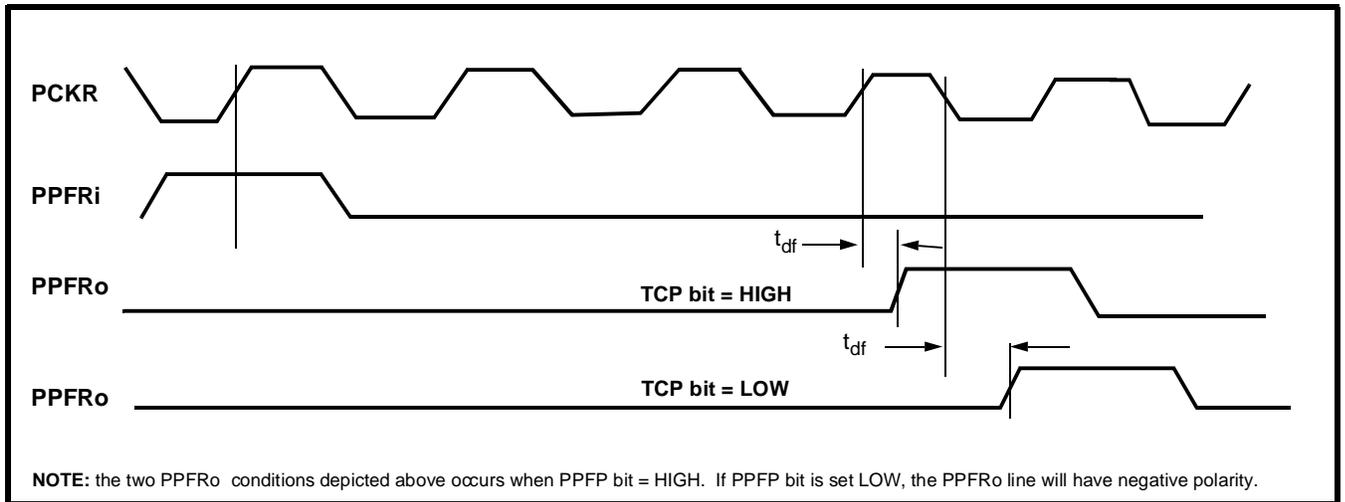


Figure 25 - Parallel Port in Timing Mode 4

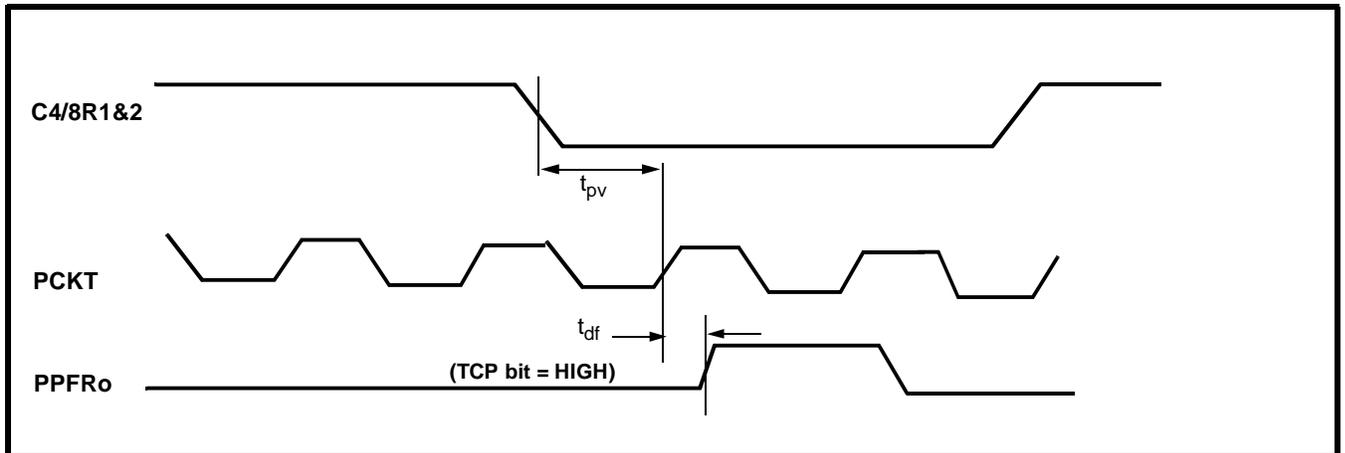


Figure 26 - Phase Variation Between C4/8R1 & 2 and PCKT Inputs for TM1 Operation

AC Electrical Characteristics† - Intel/National- HPC Multiplexed Bus Mode

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ALE pulse width	t_{alw}	20			ns	
2	Address setup from ALE falling	t_{ads}	5			ns	
3	Address hold from ALE falling	t_{adh}	9			ns	
4	\overline{RD} active after ALE falling	t_{alrd}	9			ns	
5	Data setup from \overline{DTA} Low on Read	t_{ddr}	0			ns	$C_L=150$ pF
6	\overline{CS} hold after $\overline{RD}/\overline{WR}$	t_{csw}	0			ns	
7	\overline{CS} setup from \overline{RD}	t_{csr}	0			ns	
8	Data hold after \overline{RD}	t_{dhr}	0			ns	$C_L=150$ pF, $R_L=1K\Omega^*$
9	\overline{WR} delay after ALE falling	t_{alwr}	0			ns	
10	\overline{CS} setup from \overline{WR}	t_{csw}	0			ns	
11	Data setup from \overline{WR}	t_{dsw}	30			ns	
12	Data hold after \overline{WR} inactive	t_{dhw}	8			ns	
13	Acknowledgement Delay: Reading Data Memory Reading/Writing Conn. Memories Reading/Writing to Control & Mode Reg.	t_{akd}			900 500 50	ns ns ns	$C_L=150$ pF
14	$\overline{RD}/\overline{WR}$ inactive to ALE active	t_{rst}	0			ns	$C_L=150$ pF, $R_L=1K\Omega^*$
15	Acknowledgement Hold Time	t_{akh}	0			ns	

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

High Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .

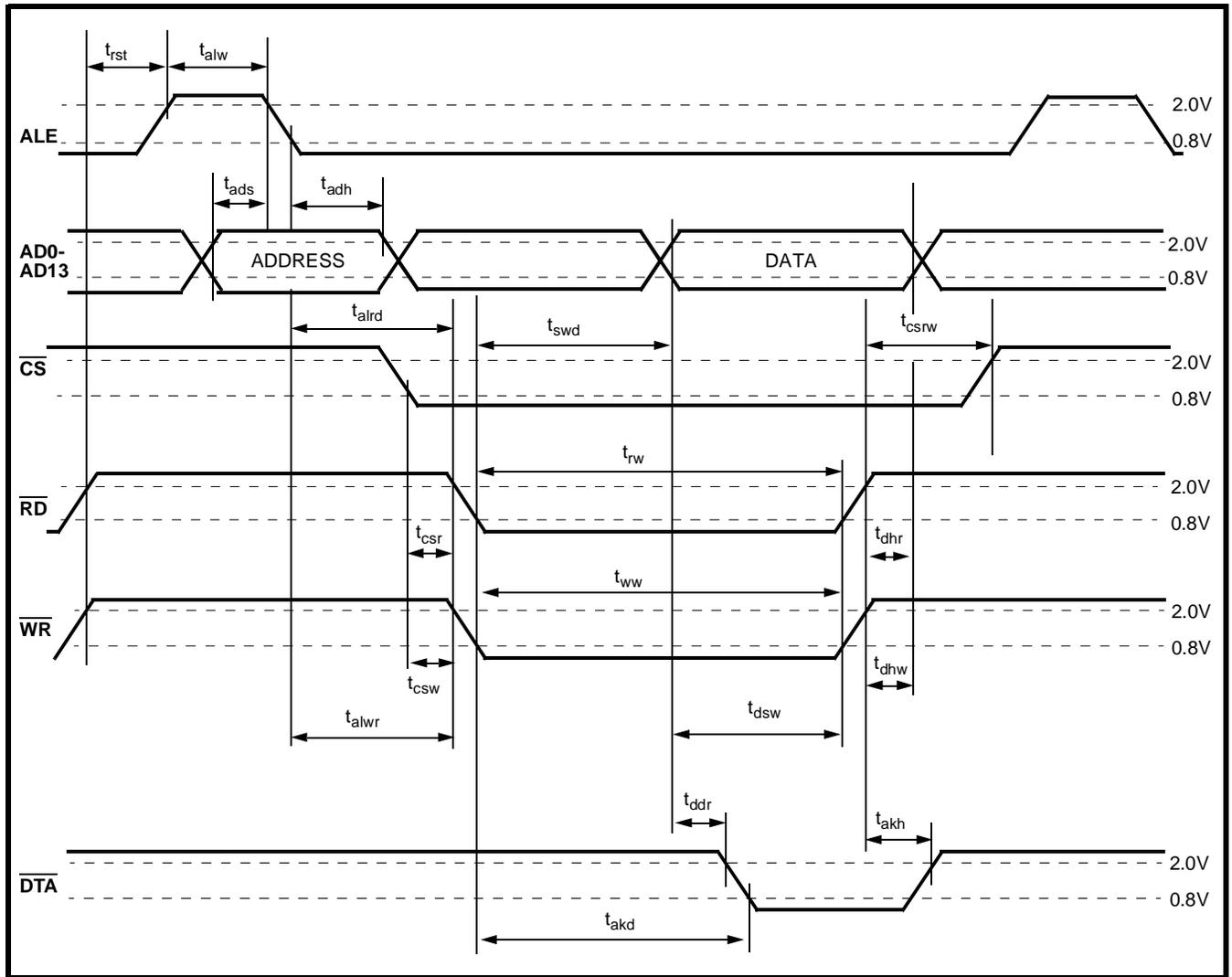


Figure 27 - Intel/National Multiplexed Bus Timing

AC Electrical Characteristics† - Motorola Multiplexed Bus Mode

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Unis	Test Conditions
1	AS pulse width	t_{asw}	80			ns	
2	Address setup from AS falling	t_{ads}	8			ns	
3	Address hold from AS falling	t_{adh}	9			ns	
4	Data setup from \overline{DTA} Low on Read	t_{ddr}	0			ns	$C_L=150$ pF
5	\overline{CS} hold after DS falling	t_{csh}	0			ns	
6	\overline{CS} setup from DS rising	t_{css}	0			ns	
7	Data hold after write	t_{dhw}	8			ns	
8	DS inactive to AS active	t_{dss}	40			ns	
9	R/\overline{W} setup from DS rising	t_{rws}	60			ns	
10	R/\overline{W} hold after DS falling	t_{rwh}	9			ns	
11	Data hold after read	t_{dhr}	0			ns	$C_L=150$ pF, $R_L=1K\Omega^*$
12	DS delay after AS falling	t_{dsh}	10			ns	
13	Acknowledgement Delay: Reading Data Memory Reading/Writing Conn. Memories Reading/Writing to Control & Mode Regs.	t_{akd}			900 500 50	ns ns ns	$C_L=150$ pF
14	Acknowledgement Hold Time	t_{akh}	0			ns	$C_L=150$ pF, $R_L=1K\Omega^*$

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

High Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .

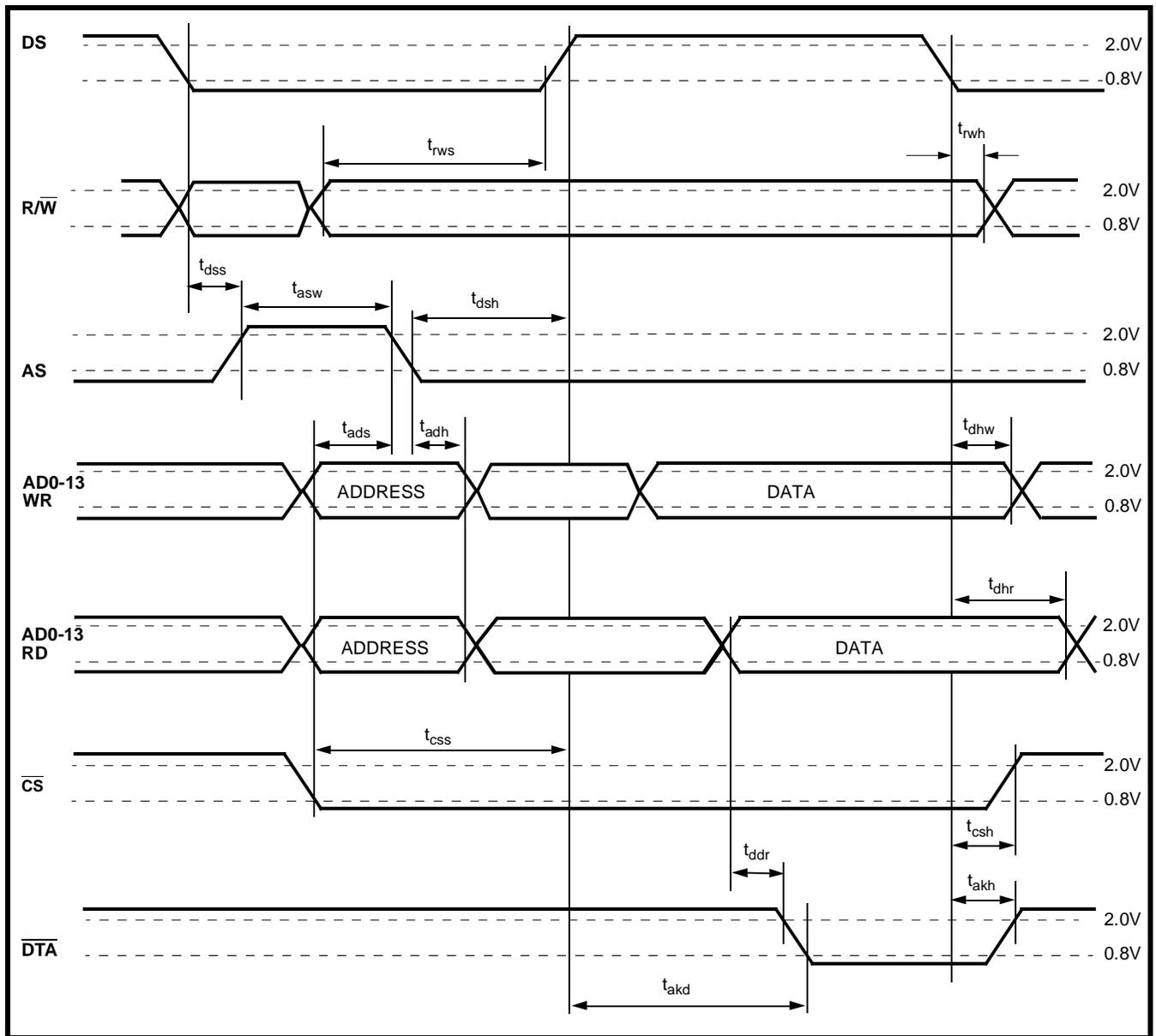


Figure 28 - Motorola Multiplexed Bus Timing

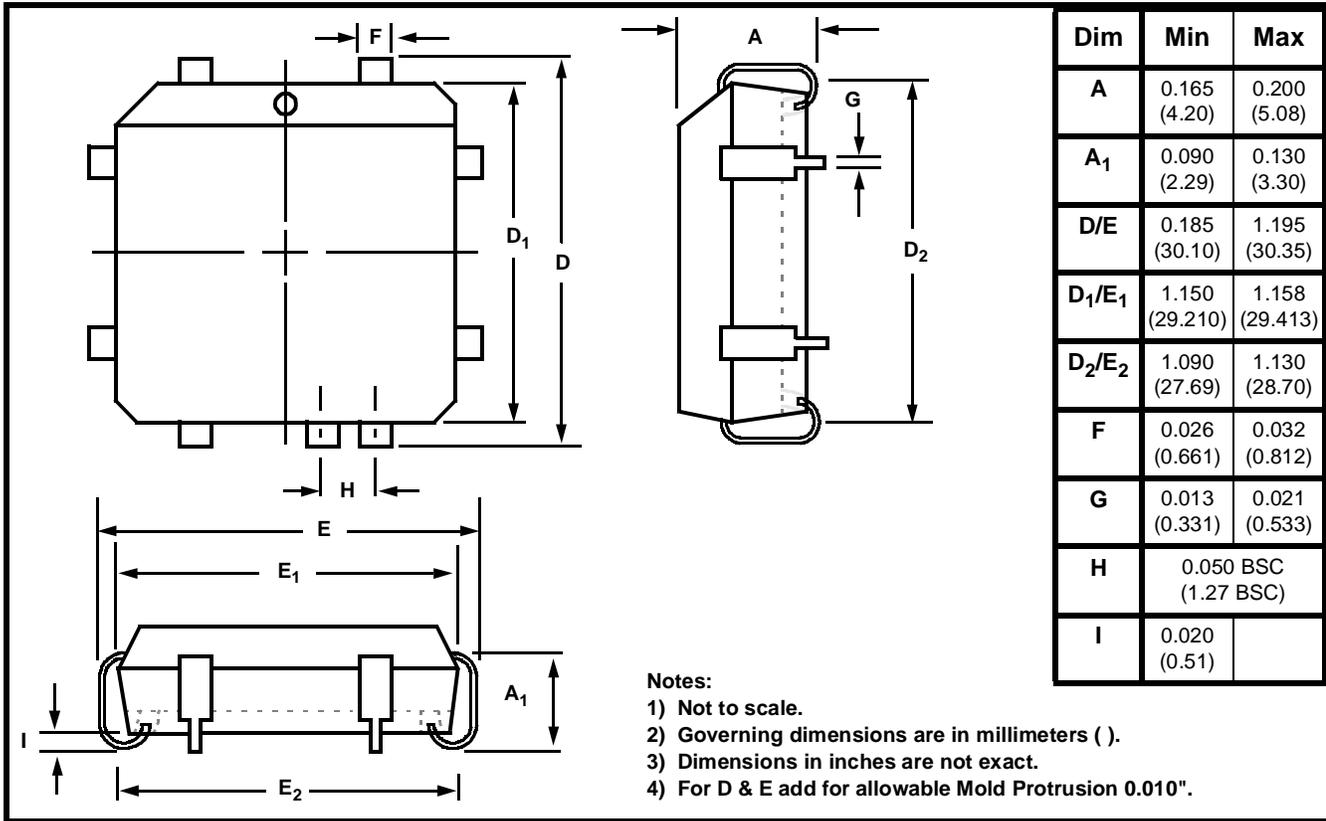


Figure 29 - 84 PLCC Mechanical Drawing

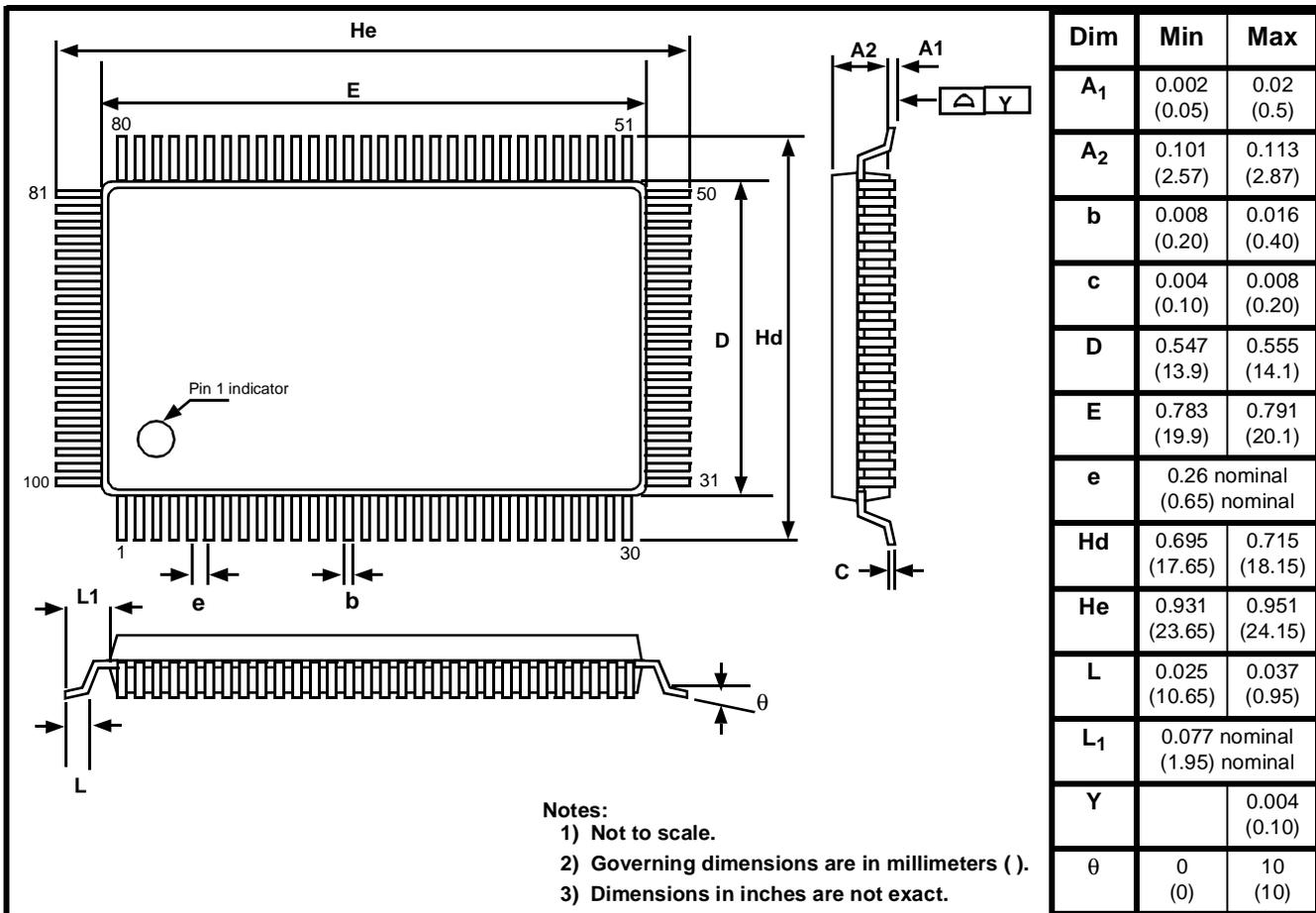


Figure 30 - 100 Pin PQF Mechanical Drawing

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