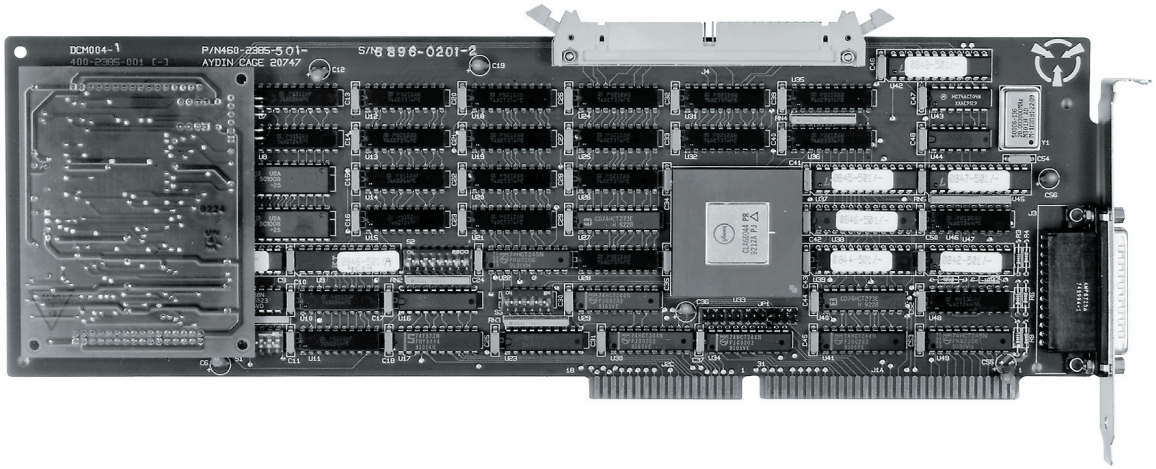
Technical Bulletin

PC 440

PC-Compatible Format Synchronizer/Decommutator

Ground Products



FEATURES

- 1 bps to 20 Mbps
- 16 to 1048576 bits-per-frame
- 2 to 4095 frames-per-subframe
- 1 to 32 bits-per-word
- Full support for IRIG Class I formats
- Time tags each minor frame
- Dual-port memory
- On-board simulator (option)

DESCRIPTION

The PC 440 Format Synchronizer and Decommutator module provides synchronization to serial PCM data stream at rates from 1 bps to 20 Mbps. The synchronization pattern is from 3 to 64 bits in length and is fully maskable and supported by software-selectable optimum synchronization strategy. Subframe synchronization is achieved on an incrementing or decrementing ID field in the data stream, the CFS frame sync pattern, or a Unique Recycle Code (URC) that occurs once each subframe.

Data decommutation includes serial-to-parallel conversion with word size and orientation, parity check and strip control. Data, status and time (from an external time code translator) are output to the ISAbus of a personal computer (PC).

Parallel data and strobes are also available for external interface on a 40-pin connector mounted in the front edge panel of the module. The memory can be configured as a time history buffer or a current value table. At the end-of-block, an interrupt is asserted.

As an option, an on-board simulator can be provided to generate test formats. Up to 2k data values may be inserted into the data stream. Data rates of 10 Mbps, 5 Mbps, 2.5 Mbps and 1.25 Mbps are selectable. An external clock source may also be used.

L3 communications

OPERATION

Setup and programming of the PC 440 module is accomplished via ISAbus read and write transfers to individual setup registers for the programmable parameters. Registers are organized to accommodate quick and easy programming of all setup parameters via a 16-bit slave-only interface.

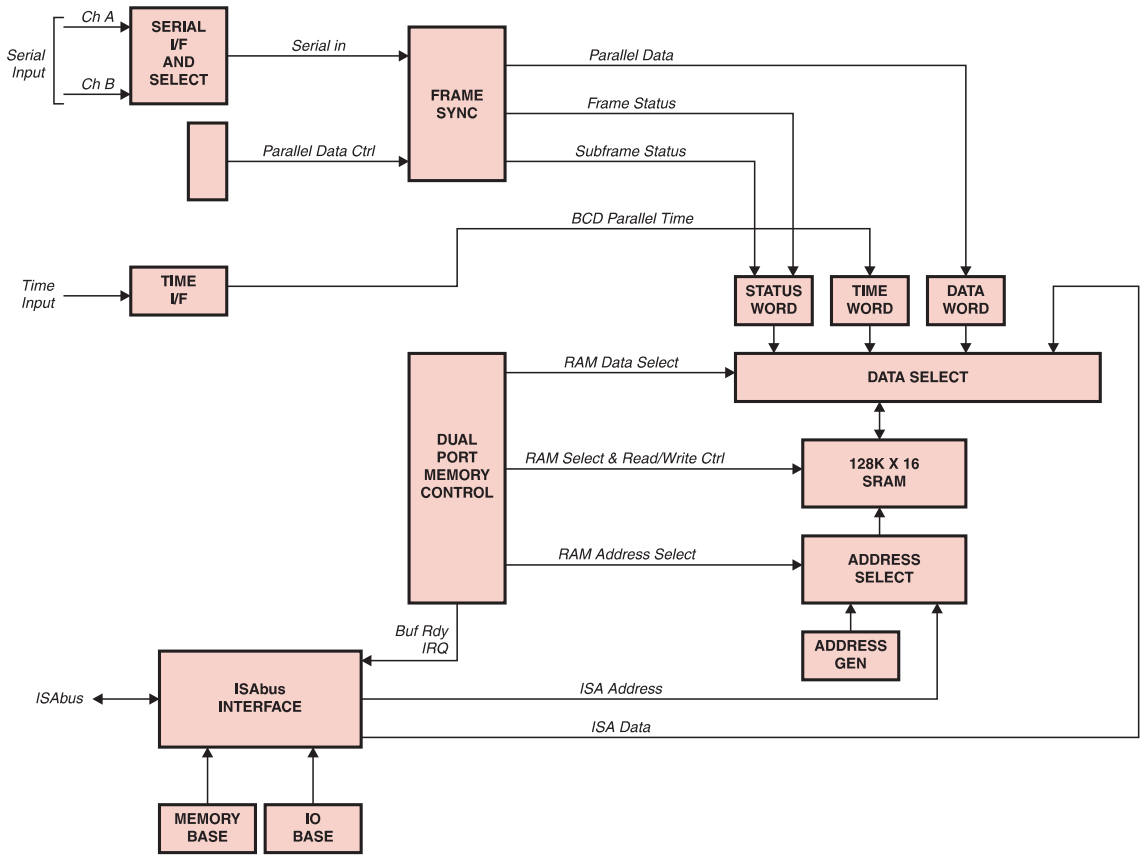
Buffer building on the PC 400 is supported by a 64k by 16-bit dual-port memory approach. A unique implementation has been adopted to allow the building of buffers of various types and sizes, depending upon the application requirements. Typical buffer types include Current Value Tables (CVTs) and Time History Buffers (THBs).

CVTs are most frequently used for quick-look data display applications, where a group of measurements is to be captured from the incoming PCM stream and transferred to a real-time display. In the CVT, a memory location is assigned to each individual input value. The display task may read the CVT at any given time, and find the most recent value for a given measurement for updating the real-time data display.

THBs, occasionally referred to as sequential buffers, are most frequently used in applications that require archiving data to a mass storage device. In a THB, data is sequentially written to the dual-port memory and an interrupt is generated to the ISAbus host CPU at the input minor frame or major frame rate. At the selected interrupt time, a register resident on the DCM004 is updated with the address of the last buffer updated in the dual-port memory. The CPU can access this information and access the appropriate THB. At the same time, the next THB is being built in the next sequential memory location.

In applications which require both CVTs for display and THBs for data archiving, a sequential buffer approach may be taken. The sequential buffer could then be accessed by an acquisition task which generates both the CVT and THB. This approach is most useful where further processing is to be performed on the data for display (i.e., EU conversions, limit checking), and where information such as time, headers, and trailers are to be merged with the archived data.

PC 440 Block Diagram



SPECIFICATIONS

Functional	Characteristics
SERIAL INPUT (J3)	
Rate	20 Mbits/sec (max)
Inputs	2 (active input is selectable)
Data	NRZ-L
Clock	0 degree
Levels	TTL with 130-ohm Thevenin termination
FRAME SYNCHRONIZER	
Input Polarity	Normal, APC
Strategy	Norm, Quick, Burst
Frame Length	8 to 1048576 bits
Minimum Error Detect	On, Off
Bit Slip Window	0, ±1, ±2, ±3 bits
Frame Sync Location	First, Last
Frame Sync Pattern	4 to 64 contiguous bits with mask
Pattern Types	Normal, AFS, CFS
Search/Check/Lock Errors	0 to 15 bit errors
Check/Flywheel Frames	0 to 15 frames
Sync States	Search, Check, Lock, Flywheel
SUBFRAME SYNCHRONIZER	
Sync Mode	ID, ID-JAM, CFS, URC
Subframe Length	2 to 4095 frames
Frame ID Counter	Up, Down
Frame Count	0 or 1 (min); 4095 (max)
ID Counter Synchronizer (ID)	
Location	Any word in the frame
Pattern	1 to 12 bits
Orientation	MSB, LSB first
ID Mode	Normal, JAM
Frame Pattern Complement Synchronizer (CFS)	Complement of FS pattern
Unique Recycle Code Synchronizer (URC)	4 to 32 bits
Sync Strategy	
Check/Lock/Flywheel Errors	0 to 7 bit errors
Check/Flywheel Frames	0 to 15 frames
Sync States	Search, Check, Lock, Flywheel
FIXED DECOMMUTATION	
Word Length	4 to 32 bits
Word Orientation	LSB, MSB first
Parity Check/Strip	Yes, No
DATA INTERFACES	
Transfer Criteria	Off, always, frame in lock, frame not in search, subframe in lock, subframe not in search, frame and subframe in lock, frame and subframe not in search.
Start Transfer	Frame boundary, subframe boundary.
ISAbus Output	
Buffer Types	2 (active buffer is selectable)
Type 1/2	Time History/Current Value Table
Size	64k deep by 16 bits wide
Interrupt	End-of-frame
TIME INPUT INTERFACE (J4)	
Resolution	Units of microseconds
Format	54 bits binary coded decimal (BCD)
Time Merging	No, Yes at start-of-frame
Levels	TTL

SPECIFICATIONS *(continued)*

Functional	Characteristics
OPTION	
PGN004	Simulator Module
ELECTRICAL AND PHYSICAL	
Input DC	+5VDC; 2.5A
Temperature	Operating: 0° to +45°C
Non-operating	-5°C to +50°C
Relative Humidity	Up to 95% without condensation
Dimensions	Full form factor PC-AT type board
Mounting	1 PC-AT bus slot (rear panel bracket and hardware included)
Weight	2 lbs.

L-3 Communications Telemetry-East
1515 Grundy's Lane, P.O. Box 729 • Bristol, PA 19007
Telephone: (267) 545-7000 • Fax: (267) 545-0100
E-Mail: sales/mktg@L-3com.com • www.L-3com.com/te

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