Technical Bulletin

PCI 3362

Dual Channel/QPSK PCM Bit Synchronizer

Ground Products

FEATURES

- Up to 2 independent bit sync channels
- Bit Rates to 20 Mbps NRZ codes, 10 Mbps all other codes
- Performance within 1 dB of theory
- Loop Bandwidth Adjustable form 0.01% to 1.60%
- Accepts NRZ-L/M/S. BiØ-L/M/S, DBiØ-/LM/S, DM-M/D, MDM-M/D codes
- Two single-ended and one differential input
- Selectable PCM outputs at TTL, RS-422, or Bipolar levels.
- Selectable Output Clock (0°, 90°, 180°, 270°)
- PN Randomizer/Derandomizer per IRIG STD 106-96
- Optional Viterbi Decoding with constraint length k=7 and rate R=1/2 & 1/3
- Optional Convolutional De-interleaving per NASA 530 SNUG REV 7
- Optional resequencer for QPSK/OQPSK Mode
- Plug-N-Play Technology

DESCRIPTION

The PCI 3362 is a full function 20 Mbps tunable Dual Channel QPSK PCM Bit Synchronizer. It is ideally suited for reconstructing a noisy input PCM data stream and providing a clean PCM signal with a coherent clock. The card can be operated as a single channel. Dual channel is available as an option. By providing Dual Channels on a single card, I and Q outputs from a QPSK receiver demodulator may be processed and recombined into a single output. This PCI compatible card offers the performance of many box level Bit Synchronizers.

Each channel of the PCI 3362 is tunable over the bit rate range of 10 bps to 20 Mbps for NRZ codes and up to 10 Mbps for all other codes. The standard NRZ-L/M/S, BiØ-L/M/S, DBiØ-M/S, DM-M/S, MDM-M/S codes are accepted from one of three input sources. The Bit Sync produces an output data stream with a bit error rate within 1 dB of theory. The bit synchronizer excels in BER performance, offering enhanced sync maintenance and acquisition capabilities. It maintains effective synchronization down to an Eb/No of -3 dB and acquisition time is less than 20 transitions in noise. The loop bandwidth can be set anywhere in the range from 0.01% to 1.60% without losing phase lock.

Programmable randomizer and derandomizer are included for generation of a randomized serial data output and derandomizing of the data on playback from an external tape recorder.

L3 communications

DESCRIPTION *(continued)*

Two single-ended inputs and one differential input per channel are standard interfaces. The single-ended input impedance is selectable between 75 ohms or 10k ohms through the PCI interface. The selected noisy input is gain-controlled and corrected for dc offset. It is then supplied to a matched filter. The peaks of the filtered signals are detected to reconstruct the PCM data streams. The internal clock is locked to the input signal through a phase-locked loop circuit. Differences between the selected clock rate and input signal rate develop loop correction voltages that synchronize the clock with the data. The loop deviation and lock status can be read through the PCI interface.

An abundance of outputs provide for flexibility in integrating the PCI 3362 into your system. A selectable PCM output and a programmable clock (0°, 90°, 180° and 270°) are available at TTL and RS-422 levels for each channel. A bipolar PCM output is also provided. For systems requiring forward error corrections, 3-bit soft decision outputs are fed to the internal Viterbi decoder (option).

Several decoder and resequencer modes of operation are supported - BPSK, QPSK, and OQPSK. In the BPSK mode, the card may act as a single channel Viterbi decoder (option). The input channel may be processed by Rate 1/2 or 1/3 Viterbi decoding with constraint length K=7 and the decoded data is presented to the serial output of the single channel. For the QPSK mode, (dual channel option), the inputs may be processed by separate Viterbi decoders prior to resequencing or a single decoder processes both inputs and produces a single output. Various differential decoding schemes are supported. The two inputs may run through a QPSK Permutation decoder where any one of 24 possible permutations may be selected to resolve ambiguities before recombining into a single stream. For offset QPSK, NRZ-M to NRZ-L decoders may be enabled prior to resequencing (option). The resequencer can be programmed for AB swapping and polarity control.

The PCI 3362 operates under software control via the PCI bus. The driver software computes all the control parameters from basic information such as the expected bit rate and the desired loop bandwidth.

SETUP, CONTROL AND STATUS

The PCI 3362 bit synchronizer uses Plug-N-Play over the PCI Bus thus eliminating the need of setting the base address of the board as is normally required for ISA based systems.

The PCI control interface of the PCI 3362 is simple but sufficiently flexible to allow the experienced user to tailor the performance to suit the characteristics of the input data. The setup and control parameters include input source selection, input impedance, input PCM code, output PCM codes, polarity, bit rate, loop bandwidth, de-interleaving enable/disable, resequencing, and Viterbi decoder parameters. Parameter updating, such as loop bandwidth and polarity does not affect normal operation of the board. Register readback capability is also included.

Status registers provide fault indications on the received signal, 12 bits of loop deviation and the synchronization state. The fault indications include loss of input signal, excessive offset, and input signal overload. These fault indications along with the sync lock status are returned to the controller for display.

SPECIFICATIONS

FUNCTION	***CHARACTERISTICS***
Bit Rate:	10 bps to 20 Mbps for NRZ codes, 10 Mbps for all other codes.
Input Source	Selectable: Two single-ended, one differential channel
PCM Codes	Accepts NRZ-L/M/S, BiØ-/L/M/S, DBiØ-L/M/S, DM-M/S, Randomized,derandomizer per IRIG STD 106-96
S/N Performance	Reconstructs data to within 1 dB of ideal bit error probability curves to Eb/No of 0 dB
INPUT SIGNAL	
Amplitude	0.1V to 10V p-p single-ended; built-in AGC and offset compensation
Baseline Shift	No degradation in baseline shifts of up to 100% p-p signal amplitude
Baseline Variations	No degradation in performance for a superimposed waveform whose amplitude is equal to the peak-to-peak amplitude of the PCM input signal and whose frequency is up to 0.1% of the bit rate
Polarity	Normal or Inverted
Direction	Program selectable forward or reverse for BiØ-L code
Impedance	75 ohms (50 optional) or 10k ohms
SYNCHRONIZATION	
Acquisition	Acquires synchronization reliably on input signals with Eb/No to 0 dB with 50% transition density
Acquisition Range	Within ± 5% of selected bit rate and Eb/No to 15 dB
Tracking	Tracks to bit rate variations up to ± 20% of selected bit rate after acquisition
Phase Ambiguity	Resolves phase in BiØ codes having 100 random bit periods; maintains phase up to 2000 constant logic 1 or 0 bits for Eb/No to 15 dB
Retention	Retains synchronization with gaps up to 128 bit periods once every 512 random bits for Eb/No to 3dB.
Phase Locked Loop Bandwidth	Loop Bandwidth is tunable from 0.1% to 1.60% without causing loss of synchronization.
DIFFERENTIAL DECODER	Type 1: BPSK (Single NRZ-M to L) Type 2: SQPSK (Dual NRZ-M to L) Type 3: QPSK (Permi Select) Permutatation Select: 1 of 24
REMOTE PROGRAMMING	External controller via the PCI bus.
OUTPUT SIGNALS	
Data PCM Channel 1 (Single Channel)	Code: Selectable (NRZ-L/M/S, RNRZ-L or BiØ-L/M/S) Levels: TTL compatible, +3V into 50 ohms and RS-422 differential or Bi-polar 2Vp-p into 50 ohms
Data PCM Channel 2 (Dual Channel)	Code: Selectable (NRZ-L/M/S, RNRZ-L or BiØ-L/M/S) Levels: TTL compatible, +3V into 50 ohms and RS422 differential or Bi-polar 2Vp-p into 50 ohms

SPECIFICATIONS *(continued)*

FUNCTION	CHARACTERISTICS
OUTPUT SIGNALS (continued)	
Clock CLK Channel 1 (Single Channel) Clock CLK Channel 2 (Dual Channel)	Phase: Selectable 0, 90, 180, 270 degrees Levels: TTL compatible, +3V into 50 ohms and RS 422 compatible Phase: Selectable 0, 90, 180, 270 degrees Levels: TTL compatible, +3V into 50 ohms
Synchronization status	Sync status is provided at TTL compatible and RS422 compatible levels. Logic “0” a indicates unit maintaining sync; logic “1” indicates unit out of sync
3 Bit Soft Decision	Direct connection to the Viterbi decoder
Symbol clock	Phase 0 direct connection to Viterbi decoder
OPTIONS	
Optional Viterbi Decoder	Constraint length k=7, 1/2 rate with option of G1 or G2 first and G1 or G2 inverted plus 1/3 rate Viterbi Polynomials 1/2 rate $G_1 = 171_8$ and $G_2 = 133_8$ 1/3 rate $G_1 = 171_8$, $G_2 = 133_8$ and $G_3 = 165_8$
Optional Convolutional De-interleaving	Compliant with the NASA Space Network Users Guide (530-SNUG) Revision 7, Appendix F
Optional Resequencer	Modulation: BPSK, QPSK, OQPSK Order: AB/BA Polarity: Invert A or Invert B
ELECTRICAL AND PHYSICAL	
Input DC Voltage and current	+12 VDC; 0.65 A -12 VDC; 0.20 A +5 VDC; 1.00 A +3.3 VDC; 1.00A
Temperature	Operating: 0° to 45°C Non-operating -5° to 50°C
Relative Humidity	Up to 95% without condensation
Dimensions	Half Length PCI interface card

ORDERING INFORMATION

PCI 3362 Dual Channel/QPSK PCM Bit Synchronizer
- 10 Single Channel only
- 11 Dual Channel

- 20 No Viterbi Decoder + De-interleaver
- 21 Viterbi Decoder + De-interleaver

- 30 No Resequencer
- 31 Resequencer

L3 communications

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