Understanding the Power Supply Requirements of PCI Bus Standard-How to Protect the Digital Components

National Semiconductor
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Until recently, PCI systems primarily used 5V components. But as submicron process technology advances, the trend is to support mixed voltage components in the newer PCI systems. As a result, power supply requirements on mixed voltage PCI systems are getting increasing attention from the design community. Understanding and designing to these requirements will prevent any power supply variations from damaging PCI components. These requirements are defined in the analog portion of the PCI Specification Revision 2.1. They specifically deal with 5V and 3.3V mixed-voltage environment.

This article provides a guide to the PCI system designers. The analog portion of the PCI 2.1 is scattered in various sections of the document. This article compiles all the analog requirements in *Table 1* and explains the requirements in detail.

Inside a typical computer, there are ±12V, ±5V and +3.3V power supplies. The analog portion of PCI Specification Revision 2.1 focuses on the +5V and +3.3V power supply requirements, because the PCI local bus and add-in cards may run on either or both voltages. The requirements outline what actions must be taken when the supply voltages are out of tolerance, as in Section 4.3.2 of PCI 2.1. It also describes possible behaviors of supply voltages that may destroy PCI components. Real danger exists if these requirements are ignored. Therefore, building a robust PCI system demands a solution to address the issues discussed above. This responsibility falls on the PCI system architecture designers and system design engineers.

Table 1 lists the sections in the PCI Specification Revision 2.1 that cover the analog requirements. Specs I and II establish the ±5% initial tolerance for 5V supply. Specs III and IV establish ±9% initial tolerance for 3.3V supply.

TABLE 1. Analog Requirements Found in PCI Specification Revision 2.1

	PCI Local Bus Specification Revision 2.1	Where to Find Spec	Page #
I	Maximum for 5V Supply Voltage 5.25V *see Spec V	Section 4.2.1.1 Table 4.1	123
II	Minimum for 5V Supply Voltage 4.75V *see Spec V	Section 4.2.1.1 Table 4.1	123
III	Maximum for 3.3V Supply Voltage 3.6V *see Spec V	Section 4.2.2.1 Table 4.3	128
IV	Minimum for 3.3V Supply Voltage 3.0V *see Spec V	Section 4.2.2.1 Table 4.3	128
V	The value of T_{fail} is the minimum of 500 ns (maximum) from either power rail going out of specifications *(exceeding specified tolerances by more than 500 mV). 100 ns (maximum) from the 5V rail failing below 3.3V rail by more than 500 mV.	Section 4.3.2 Reset Section	139
VI	Anytime $\overline{RST}$ is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated.	Section 2.2.1 $\overline{RST}$ Section	9
VII	Clamping directly to the 3.3V rail with a simple diode must never be used in the 5V signaling environment. When dual power rails are used, parasitic diode paths can exist from one supply to another. These diode paths can become significantly forward biased (conducting) if one of the power rails goes out of spec momentarily. Diode clamps to a power rails as well as to output pull-up devices, must be able to wthstand short circuit current until drivers can be tri-stated. Refer to Section 4.3.2 for more information.	Section 4.2.1.2 (refer to the article for more information)	126

TABLE 1. Analog Requirements Found in PCI Specification Revision 2.1 (Continued)

	PCI Local Bus Specification Revision 2.1	Where to Find Spec	Page #
VIII	There is no specified sequence in which the four power rails (12V, -12V, 5V and 3.3V) are activated or deactivated. They may come up and go down in any order. The system must assert $\overline{RST}$ both at power up and whenever either the 5V or 3.3V rails go out of spec (per Section 4.3.2). During reset, all PCI signals are driven to a "safe" state, as described in Section 4.3.2.	Section 4.3.4.2 (refer to the article for more information)	142

Spec V establishes an additional ±500 mV on both of the 5V and 3.3V supplies for noise margin consideration. Moreover, Spec V states that if either the 5V supply or the 3.3V supply is out of limit, a $\overline{RST}$ signal has to be asserted within 500 ns. For example, if 5V supply is over 5.75V, $\overline{RST}$ has to be asserted within 500 ns. The worst case in Spec V, and a potentially destructive case, is if 5V supply falls below 3.3V supply by more than 300 mV. $\overline{RST}$ signal has to be asserted within 100 ns when this occurs.

Spec VI requires that all PCI output signals be tri-stated once $\overline{RST}$ is asserted. Tri-stating the PCI devices will prevent any current flowing from the PCI devices to damage other PCI devices connected to the PCI bus.

Spec VII describes possible dangers of protection diodes being turned on in mixed voltage environment. In the event that a protection diode is clamped directly to 3.3V supply in an 3.3V I/O device, it will be forwarded biased when the input of the I/O is coming from 5V devices. This is shown in *Figure 1*. Possibly, a large amount of current will flow from 5V outputs into the 3.3V device through the protection diode, damaging the 3.3V device. Consequently, Spec VII advises never to clamp a diode directly to 3.3V supply in 5V signaling environment.

Specs VII describes another situation where the current flow is from 3.3V supply to 5V supply. In the case when 5V supply is accidently crowbarred to ground, a current path exists between 3.3V supply and 5V supply (now ground), shown in *Figure 2*. The current flows from the 3.3V device through the PCI bus into the 5V device. Since the 5V supply is now ground, the input protection diode inside the 5V device becomes forward biased, allowing the large current to pass through, possibly damaging the 5V device. Spec V and VI protect the 5V device by asserting $\overline{RST}$ in 100 ns when the 5V falls below 3.3V by more than 300 mV. Upon $\overline{RST}$ assertion, all PCI output signals will be tri-stated.

The 5V and the 3.3V devices in *Figure 2* can be part of a discrete logic, chipset, or ASIC.

Spec VIII points out another threat that mixed voltage supplies have on PCI components. PCI 2.1 does not guarantee power-up and power-down sequences. As as example of Spec VIII, consider the instance where 3.3V supply comes up before 5V supply. If 5V rises slowly, staying under 3.3V, there can be a current path from 3.3V supply to 5V supply through the protection diode inside the 5V logic. Destruction can happen. The same principle applies when 3.3V power supply goes to ground slower than 5V. Spec V prevents disasters by asserting $\overline{RST}$ until supplies are within their limits.

A second example on Spec VIII is the case where 5V and 3.3V supplies are independently regulated from the main power supply. If the 5V supply momentarily fails, 5V devices can suffer from electrical overstress resulting from current flowing from 3.3V to 5V through the 5V device input protection diodes. Again, Spec V saves the situation by asserting $\overline{RST}$ when 5V is out of limit.

A third example of Spec VIII is the case where 3.3V is generated from 5V via a linear regulator either in the main power supply or add-in cards. Some regulators do not provide current limiting on 3.3V output. Electrical overstress can damage the pass transistor inside the regulator, allowing the 3.3V to rise to 5V. This would exceed the operating voltage range on the 3.3V devices. PCI 2.1 provides over-voltage protection by asserting $\overline{RST}$ to tri-state outputs in this situation.

Mixed voltage environment presents a new challenge to the PCI system architecture designers. With so many different power supply sources using various implementations, it is very difficult to ensure that a power supply complies with PCI 2.1 at all times. Many believe that PCI voltage monitoring is the responsibility of the power supply section. Today, this is not the case. A PCI system designer has no control of power supplies and add-in cards. However, he does have control of the motherboard. Therefore, it is far better to design the protection function that will monitor all types of power supplies and add-in cards on the motherboard. As a reference, *Table 2* shows some safe and unsafe conditions in mixed voltage PCI systems.

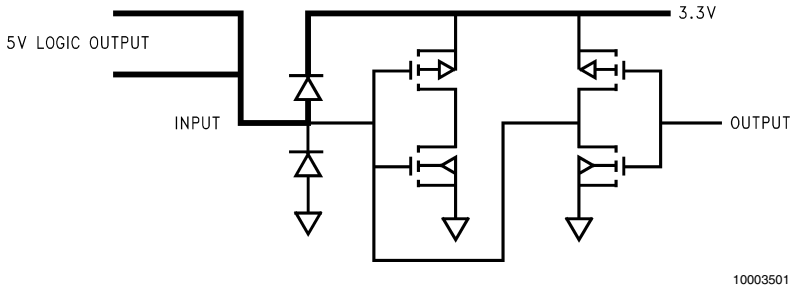

FIGURE 1. Possible Current Diode Path from 5V to 3.3V via 3.3V Clamp Diode

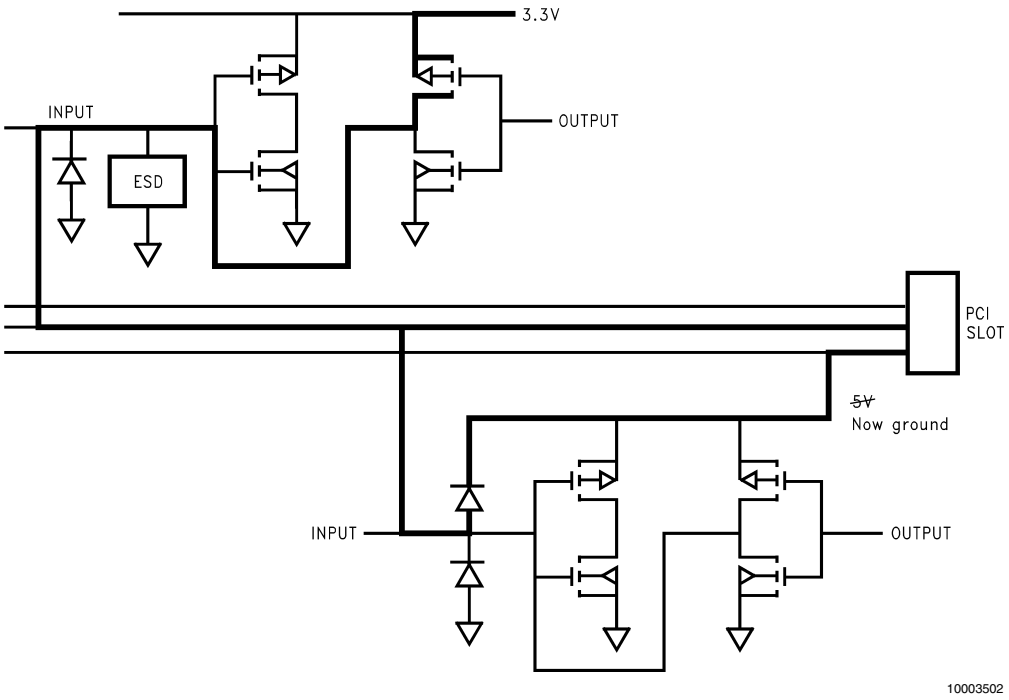

FIGURE 2. Possible Current Diode Path from 3.3V to 5V when 5V is Crowbarred

TABLE 2. Safe and Unsafe Conditions in Mixed Voltage PCI Systems

UNSAFE CONDITIONS:
3.3V supply coming up before 5V supply.
5V and 3.3V power supplies are independently regulated from the main power supply.
3.3V is generated from 5V via linear regulator.
Any 3.3V logic IC that is not 5V tolerant and does not use buffers that are 5V tolerant to drive directly on the PCI bus.
SAFE CONDITIONS:
PCI bus is 5V only or 3.3V only. This includes PCI add-in cards.
3.3V logic is 5V tolerant. This includes any I/O being directly connected to the PCI bus. Mixed 5V and 3.3V have compatible logic levels.
Any 3.3V logic IC's that are not 5V tolerant use buffers that are 5V tolerant to drive directly on the PCI bus. This applies to motherboard as well as add-in cards.

National Semiconductor recognizes the need for monitoring power supplies in PCI environment to ensure system integrity and safety. The LMC6953 PCI power supply monitor IC is designed to comply with PCI 2.1, meeting all the analog requirements. It fully addresses all the specs discussed.

There are five comparators inside the LMC6953. Two of them monitor over-voltage and under-voltage on the 5V supply; two other monitor the over-voltage and under-voltage on the 3.3V supply. The fifth one is a differential comparator monitoring for power failure - 5V going 300 mV below 3.3V. The LMC6953 also has a 5V/3.3V logic compatible interrupt pin. During power-up, the LMC6953 holds $\overline{RST}$ low for 100 ms (as required by Section 4.3.2, Figure 4.12 on page 140 of PCI 2.1) after both 5V and 3.3V supplies are within their specified windows. It asserts $\overline{RST}$ within 490 ns when an over-voltage or an under-voltage is detected. In case of power failure or momentary fault where the 5V supply falls below 3.3V supply by 300 mV maximum, $\overline{RST}$ is asserted within 90 ns.

$\overline{RST}$ also can be instantly asserted by sending a CMOS logic low to the manual interrupt pin. Each time $\overline{RST}$ is asserted, it holds low for 100 ms after all fault conditions are recovered. The 100 ms delay is generated by the 0.01 µF C_{EXT} capacitor, and can be adjusted by changing the value of C_{EXT}.

The LMC6953 is designed for desktop PC motherboards or add-in cards. *Figure 3* shows the LMC6953 monitoring the 5V and 3.3V power supplies from the power supplies and asserting $\overline{RST}$ to the system controllers in case of a fault condition. $\overline{RST}$ from the LMC6953 has an open-drain output and can be ORed to different system controllers. If monitoring a third voltage is desired, for example, 12V, it can be achieved by voltage dividing the 12V down to 2.5V and connecting it to the manual reset input. Furthermore, the manual reset input can, at the same time, accept a logic output and the divided-down 12V, as shown in *Figure 4*.

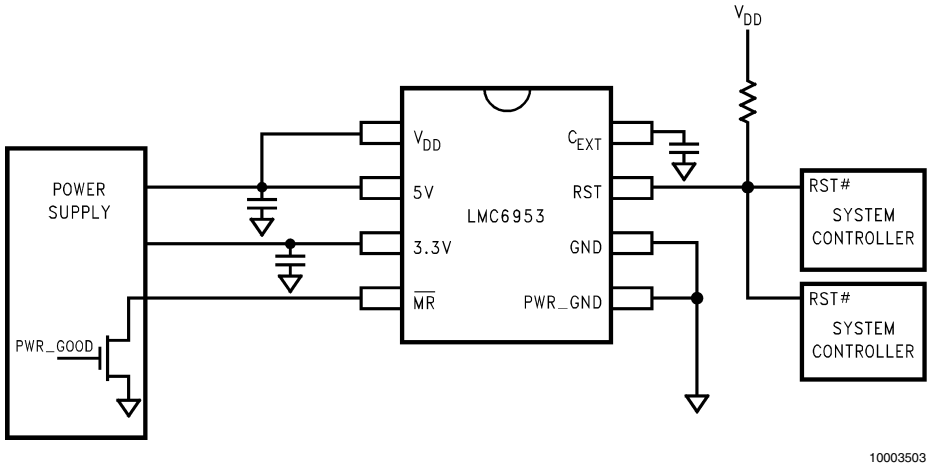

FIGURE 3. Typical Application Circuit using the LMC6953 on a Motherboard

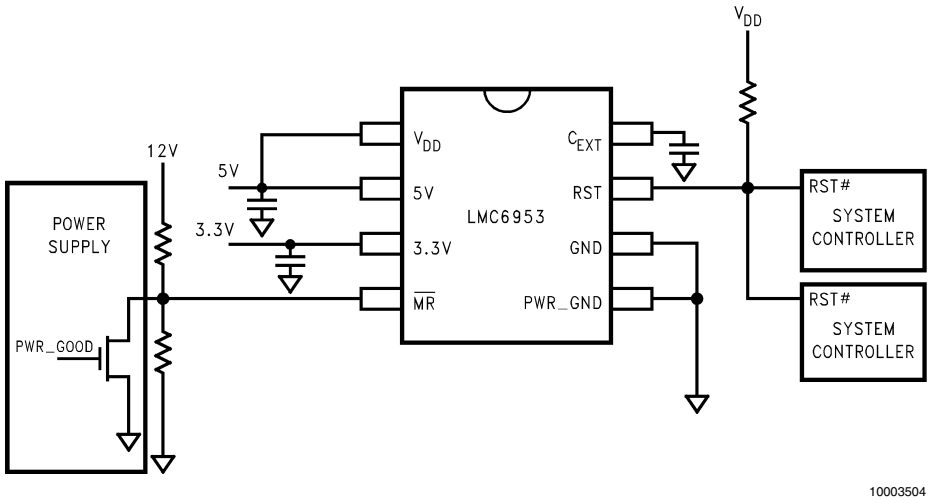

FIGURE 4. Using LMC6953 to Monitor Three Different Voltages

Power supplies do not provide any functions defined in PCI 2.1. In fact, power supplies have such diverse designs that the only sure way to design a PCI-compliant system is to include the power supply monitoring functions on the motherboard. The LMC6953 is designed for that purpose. It offers an integrated solution that completely covers the power supply requirements in PCI 2.1. Designing the LMC6953 into a mixed voltage PCI system will protect the digital components in that system. The LMC6953 asserts $\overline{RST}$ to the system controllers when there is a fault condition on the supply voltages. The $\overline{RST}$ in turn drives all PCI output signals to their benign state, preventing destructive events due to any of the conditions listed in *Table 1*.

There are datasheets, demonstration boards and powerpoint presentation to aid designers and the sales force to learn more about the LMC6953 as well as gaining further insight into this subject.

Notes

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