LM3477 Evaluation Board

National Semiconductor
Application Note 1193
Mark Hartman
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Introduction

The LM3477 is a current mode, high-side N channel FET controller. It is most commonly used in buck configurations, as shown in *Figure 1*. All the power conducting components of the circuit are external to the LM3477, so a large variety of inputs, outputs, and loads can be accommodated by the LM3477.

The LM3477 evaluation board comes ready to operate at the following conditions:

$4.5V \le V_{IN} \le 15V$

$V_{OUT} = 3.3V$

$0A \le I_{OUT} \le 1.6A$

The circuit and BOM for this application are given below:

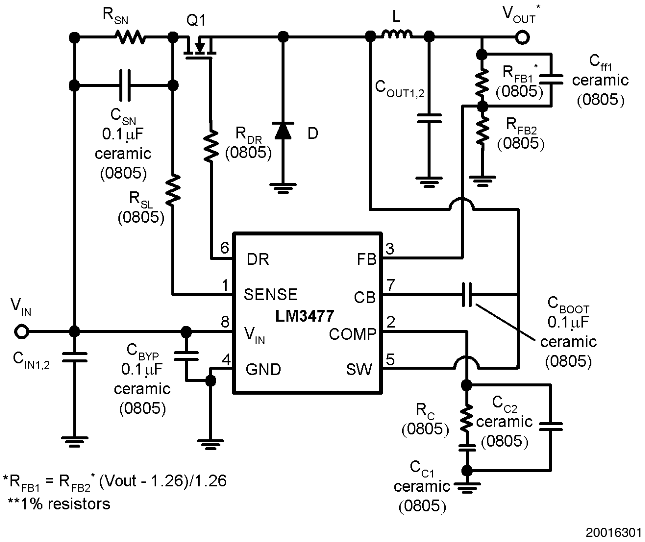

FIGURE 1. LM3477 Buck Converter

TABLE 1. Bill of Materials

Component	Value	Part Number
C_{IN1}	120µF/20V	594D127X0020R2
C_{IN2}	No connect	
C_{OUT1}	22µF/10V	LMK432BJ226MM (Taiyo Yuden)
C_{OUT2}	22µF/10V	LMK432BJ226MM (Taiyo Yuden)
L	10µH, 3.8A	DO3316P-103 (Coilcraft)
R_C	1.8kΩ	CRCW08051821FRT1 (Vitramon)
C_{C1}	12nF/50V	VJ0805Y123KXAAT (Vitramon)
C_{C2}	No connect	
Q1	5A, 30V	IRLMS2002 (IRF)
D	100V, 3A	MBRS340T3 (Motorola)
R_{DR}	20Ω	CRCW080520R0FRT1 (Vitramon)
R_{SL}	1kΩ	CRCW08051001FRT1 (Vitramon)
R_{FB1}	16.2kΩ	CRCW08051622FRT1 (Vitramon)
R_{FB2}	10.0kΩ	CRCW08051002FRT1 (Vitramon)
C_{FF}	470pF	VJ0805Y471KXAAT (Vitramony)
R_{SN}	0.03Ω	WSL 2512 0.03Ω ±1% (Dale)

Performance

Following are some benchmark data taken from the circuit above on the LM3477 evaluation board. This evaluation board may also be used to evaluate a buck regulator circuit optimized for a different operating point, or to evaluate a trade-off between cost and some performance parameter. For example, the conversion efficiency may be increased by using a lower $R_{DS(ON)}$ MOSFET, ripple voltage may be lowered with lower ESR output capacitors, and the hysteretic threshold may be changed as a function of the R_{SN} and R_{SL} resistors.

The conversion efficiency may be increased by using a lower $R_{DS(ON)}$ MOSFET, however it drops as input voltage increases. The efficiency reduces because of increased diode conduction time and increased switching losses. Switching losses are due to the Vds*Id transition losses and to the gate charge losses, both of which may be lowered by using a FET with low gate capacitance. At low duty cycles, where most of the power loss in the FET is from the switching losses, trading off higher $R_{DS(ON)}$ for lower gate capacitance will increase efficiency.

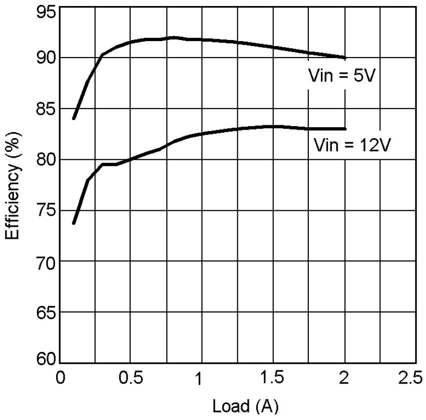

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FIGURE 2. Efficiency vs Load
V_{OUT} = 3.3V

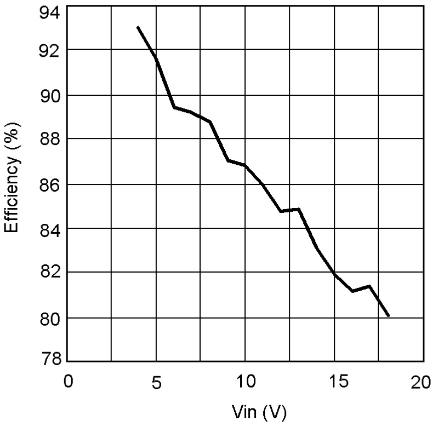

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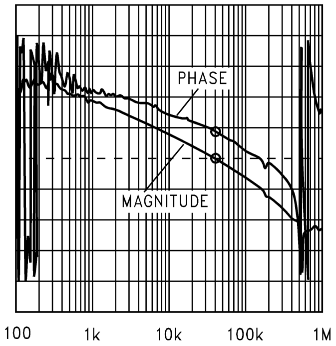
FIGURE 3. Efficiency vs V_{IN}
V_{OUT} = 3.3V, I_{OUT} = 2A

Given below is a bode plot of LM3477 open loop frequency response using the external components listed in *Table 1*.



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Magnitude = 20 dB/Decade
Bandwidth = 39.8kHz
Phase = 45˚/Decade
Phase Margin = 41˚

FIGURE 4. Open Loop Frequency Response
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1.5A

Hysteretic Mode

As the load current is decreased, the LM3477 will eventually enter a 'hysteretic' mode of operation. When the load current drops below the hysteretic mode threshold, the output voltage rises slightly. The over voltage protection (OVP) comparator senses this rise and causes the power MOSFET to shut off. As the load pulls current out of the output capacitor, the output voltage drops until it hits the low threshold of the OVP comparator and the part begins switching again. This behavior results in a lower frequency, higher peak-to-peak output voltage ripple than with the normal pulse width modulation scheme. The magnitude of the output voltage ripple is determined by the OVP threshold levels, which are referred to the feedback voltage and are typically 1.25V to 1.31V (see Electrical Characteristics table in the LM3477 datasheet). In the case of a 3.3V output, this translates to a regulated output voltage between 3.27V and 3.43V. The hysteretic mode threshold point is a function of R_{SN} and R_{SL}. *Figure 5* shows the Hysteretic Threshold vs. V_{IN} for the LM3477 evaluation board with and without R_{SL}.

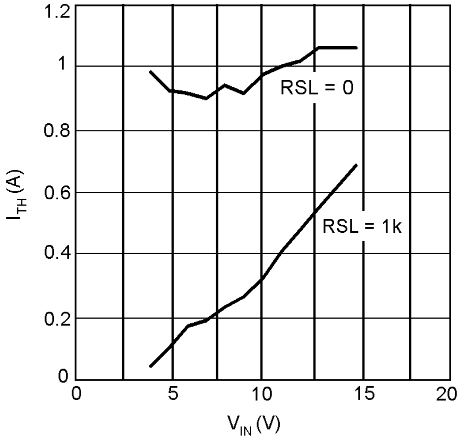

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FIGURE 5. I_{TH} vs V_{IN}

Increasing Current Limit

The R_{SL} resistor offers flexibility in choosing the ramp of the slope compensation. Slope compensation affects the minimum inductance for stability (see the Slope Compensation section in the LM3477 datasheet), but also helps determine the current limit and hysteretic threshold. As an example, R_{SL} can be disconnected and replaced by a 0 ohm resistor so that no extra slope compensation is added to the current sense waveform to increase the current limit. A more conventional way to adjust the current limit is to change R_{SN}. R_{SL} is used here to change current limit for the sake of simplicity and to demonstrate the dependence of current limit to R_{SL}. By changing R_{SL} to 0 ohm, the following conditions may be met:

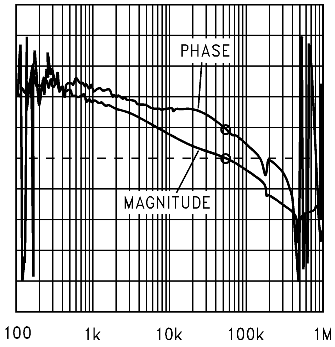
$4.5V \leq V_{IN} \leq 15V$

$V_{OUT} = 3.3V$

$0A \leq I_{OUT} \leq 3A$

The current limit is a weak function of slope compensation and a strong function of the sense resistor. By decreasing R_{SL}, slope compensation is decreased, and as a result the current limit increases. The hysteretic mode threshold will also increase to about 1A (see *Figure 5*).

Given below is a bode plot of LM3477 open loop frequency response using the modified ($R_{SL} = 0\Omega$) components to achieve higher output current capability.



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Magnitude = 20 dB/Decade Bandwidth = 55.3kHz

Phase = 45˚/Decade Phase Margin = 42˚

FIGURE 6. Open Loop Frequency Response
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 3A

Layout Fundamentals

Good layout for DC-DC converters can be implemented by following a few simple design guidelines:

1. Place the power components (catch diode, inductor, and filter capacitors) close together. Make the traces between them short.
2. Use wide traces between the power components and for power connections to the DC-DC converter circuit.
3. Connect the ground pins of the input and output filter capacitors and catch diode as close as possible using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane with several vias.
4. Arrange the power components so that the switching current loops curl in the same direction.
5. Route high-frequency power and ground return as direct continuous parallel paths.
6. Separate noise sensitive traces, such as the voltage feedback path, from noisy traces associated with the power components.
7. Ensure a good low-impedance ground for the converter IC.
8. Place the supporting components for the converter IC, such as compensation, frequency selection and charge-pump components, as close to the converter IC as possible but away from noisy traces and the power components. Make their connections to the Converter IC and it's pseudo-ground plane as short as possible.
9. Place noise sensitive circuitry, such as radio-modem IF blocks, away from the DC-DC converter, CMOS digital blocks, and other noisy circuitry.

Layout Fundamentals (Continued)

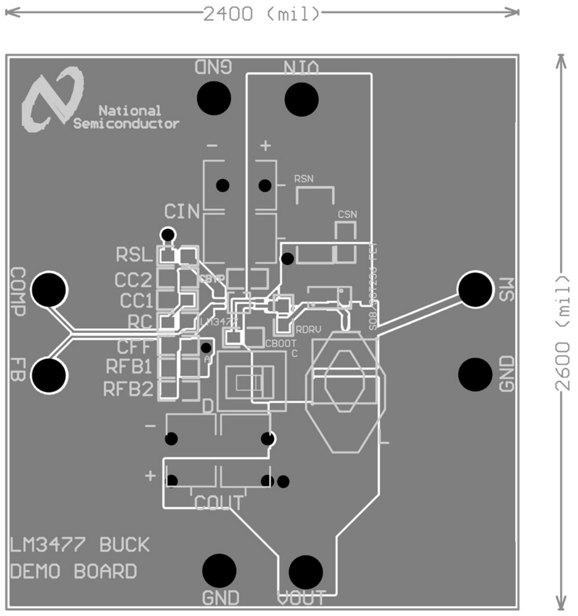

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FIGURE 7. LM3477 Evaluation Board PCB Layout (Top Side)

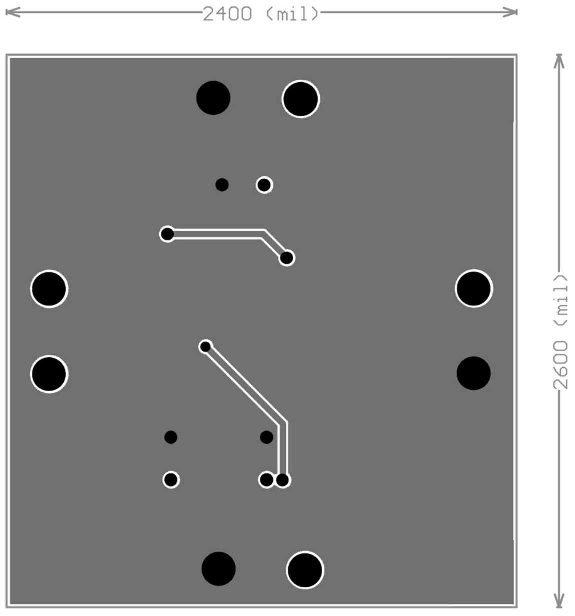

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FIGURE 8. LM3477 Evaluation Board PCB Layout (Bottom Side)

Notes

National Semiconductor
Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor
Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507