LM2642 Evaluation Board

National Semiconductor
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Introduction

The LM2642 evaluation board has been developed to aid in the design and evaluation of dc/dc converters based on the LM2642 controller IC. The board is intended to be a reusable tool on which several different circuit configurations meeting the requirements of different applications can be built. As shown in Figure 1, the evaluation board is configured to provide two outputs of 5V/3A and 3.3V/3A from an input range of 6V to 30V. The corresponding bill of materials is given in *Table 1*. *Figure 2*, *Figure 9* and *Figure 10* show the full evaluation board schematic and layout.

Board Configuration

The LM2642 Eval. Board can be easily configured for different current sensing schemes, as well as for parallel operation. *Table 1* gives the jumper and part settings for the current sensing. *Table 2* gives the jumper and circuit configurations for parallel and two-channel operation. The evaluation board also includes several optional component pads for reducing switch node ringing and current sense noise, and for low input voltage applicatons.

TABLE 1. Jumper Settings for Current Sensing

Jumper/Part#	Connects To	Current Sense
KSx	VIN	Sense Resistor
RSNx	RSx	
KSx	DSx	$R_{DS(ON)}$ Sense
RSNx	SWx	
C28, 29, 30, 31	Installed	Sense Resistor
C5, 32, 17, 33	Open	
C28, 29, 30, 31	Open	$R_{DS(ON)}$ Sense
C5, 32, 17, 33	Installed	

Board Configuration (Continued)

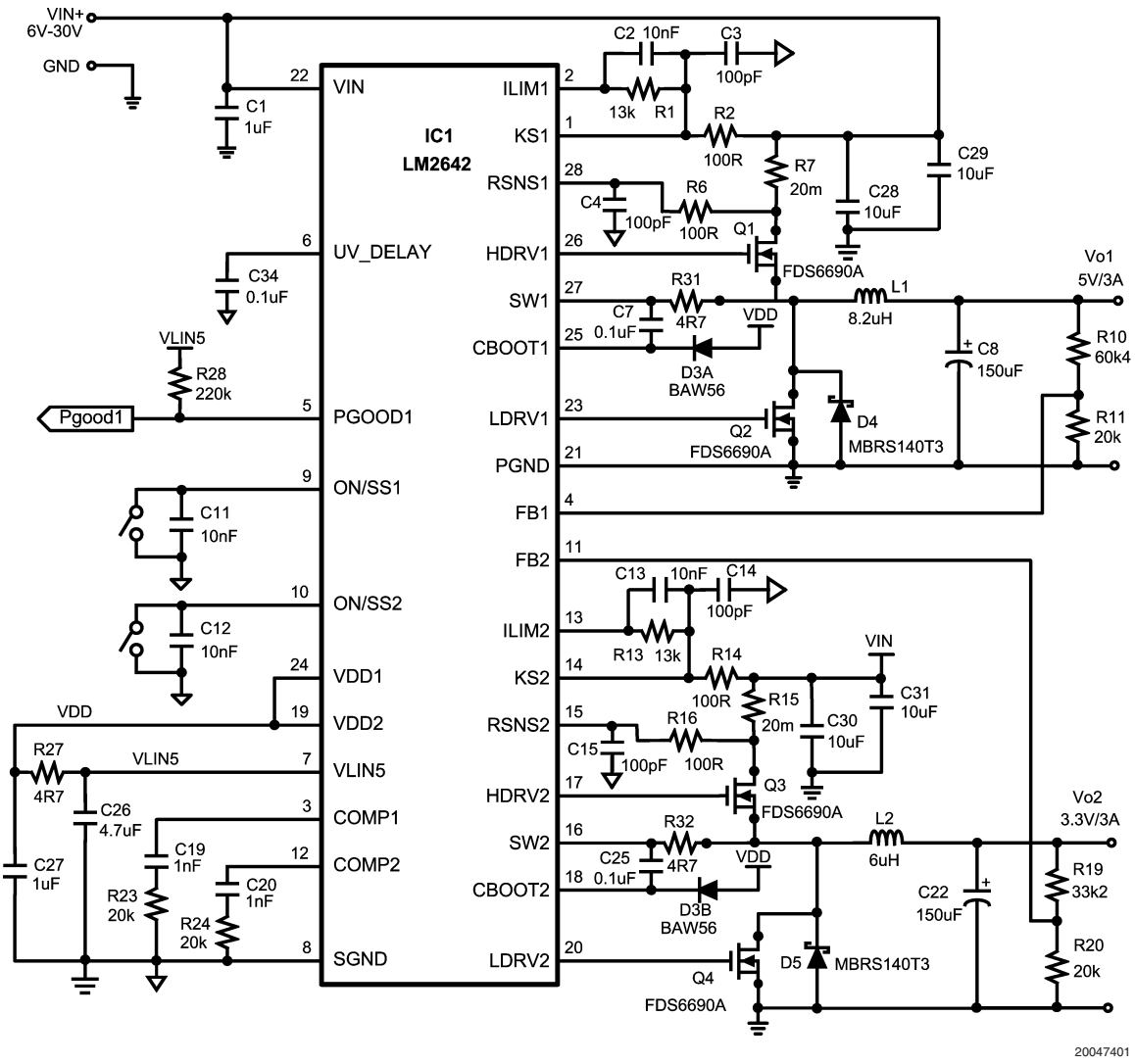


FIGURE 1. Example Circuit

Parallel Operation

In applications with high output current demand, the two switching channels can be configured to operate as a two-180˚ out of phase converter to provide a single output voltage with current sharing between the two switching channels. This approach greatly reduces the stress and heat on the output stage components while lowering input ripple current. The sum of inductor ripple current is also reduced which results in lowering output ripple voltage. Because precision current sense is the primary design criteria to ensure accurate current sharing between the two channels, both channels must use external sense resistors for current sensing. To minimize the error between the error amplifiers of the two channels, tie the feedback pins FB1 and FB2 together using **J1** and **J2** and connect to one voltage divider for output voltage sensing. Also, tie pins COMP1 and COMP2 together with **R30** and connect to a single compensation network. ON/SS1 and ON/SS2 must be tied together with **R29** to enable and disable both channels simultaneously. Also, both output nodes must be connected.

TABLE 2. Parallel Configuration Settings

Jumper/Part#	2-Ch. Setting	Parallel Setting
J1	Open	Short
J2	Open	Short
R29	Open	Short
R30	Open	Short
R24	Installed	Open
R19	Installed	Open
R20	Installed	open

Optional Components

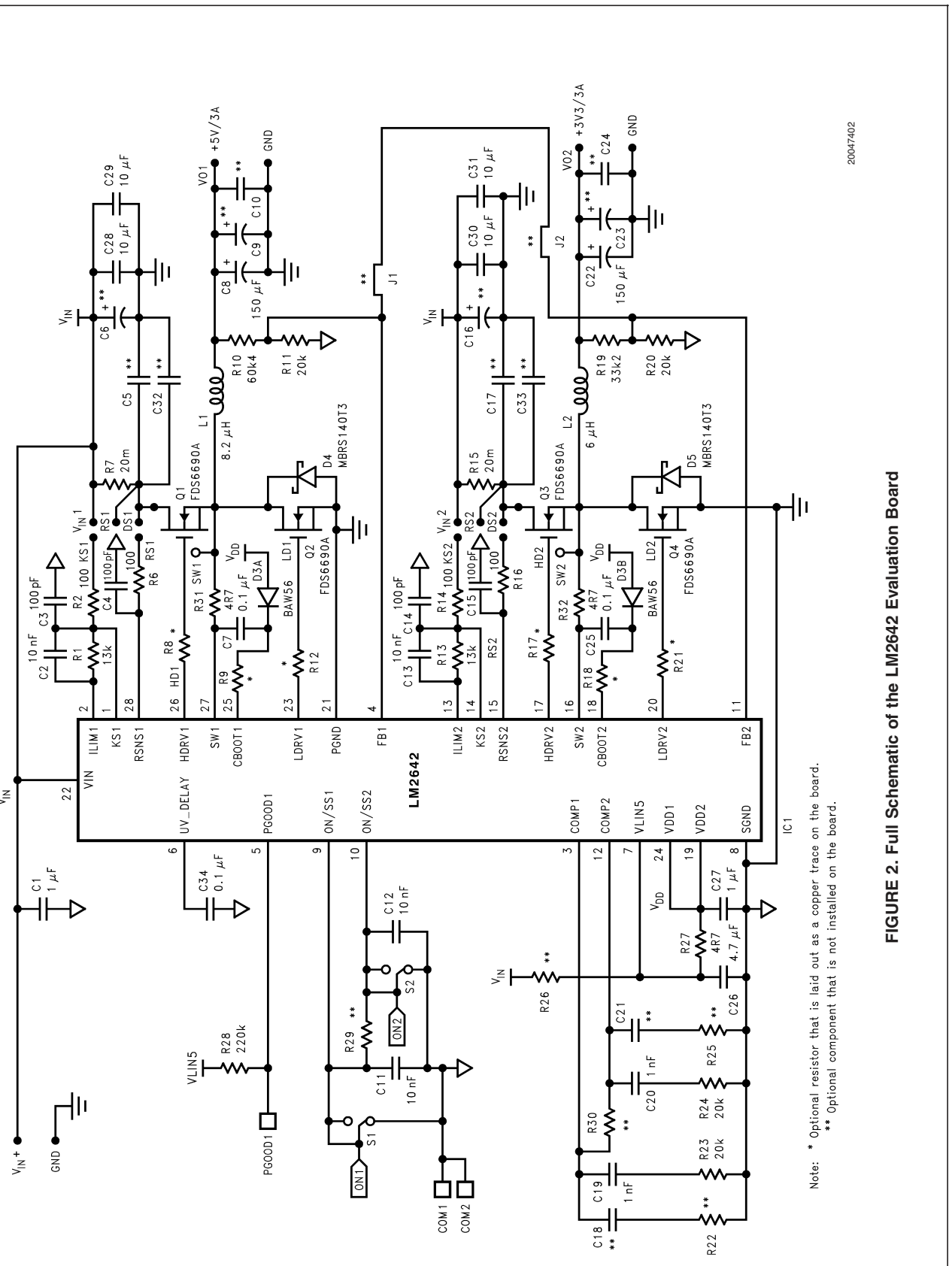
Optional resistor **R26**, must be installed with a 4.7ohm resistor when the input voltage is below 5.5V. This will ensure that VLIN5 does not fall below the UVLO threshold.

Power MOSFETs are very fast switching devices. In synchronous rectifier converters, the rapid increase of drain current in the top FET coupled with parasitic inductance will generate unwanted Ldi/dt noise spikes at the source node of the FET (SWx node) and also at the VIN node. The magnitude of this noise will increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. The LM2642 evaluation board provides several options for suppressing this noise.

R-C filters can be added to the current sense amplifier inputs as shown in *Figure 7*. These filters are comprised of **R2, C3, C4, R6,** and R**14, C14, R16, C15,** and are included in the example circuit. These filters will reduce the susceptibility to switching noise, especially during heavy load transients and short on-time conditions. Note that these filters should only be used when a current sense resistor is used.

The resistor in series with the SWx pin **(R31, R32)** slows down the gate drive (HDRVx), thus slowing the rise and fall time of the top FET, yielding a longer drain current transition time and reducing switch node ringing. Top FET switching losses will increase with higher resistance values. Small resistors (1-5 ohms) can also be placed in series with the HDRVx pin **(R8, R17)** or the CBOOTx pin **(R9, R18)** to effectively reduce switch node ringing. A CBOOT resistor will slow the rise time of the FET, whereas a resistor at HDRV will reduce both rise and fall times.

To maintain stable regulation, the FBx pins should remain free of noise. The LM2642 evaluation board provides pads for **C10** and **C24**, which can be used to suppress noise that may be picked up by the FBx traces. Notice that both of these capacitors are placed close to the FBx nodes.



Note: * Optional resistor that is laid out as a copper trace on the board.
** Optional component that is not installed on the board.

FIGURE 2. Full Schematic of the LM2642 Evaluation Board

TABLE 3. Bill Of Materials

Code	Description	Manufacturer
C1	Cap-MLCC 1uF 50V UMK212F10560ZG	TaiyoYuden
C11	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C12	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C13	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C18, C21	Cap-MLCC 470pF 50V VJ0805Y471KXAMT	Vishay
C19	Cap-MLCC 1nF 25V VJ0805Y102KXA	Vishay
C2	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C20	Cap-MLCC 1nF 50V VJ0805Y102KXA	Vishay
C22	CAP-SP 150uF 6.3V +/-20% EEFUE0J151R	Panasonic
C25	Cap-MLCC 0.1uF 50V VJ0805Y104KXA	Vishay
C26	Cap-MLCC 4.7uF 10V LMK316475JML	TaiyoYuden
C27	Cap-MLCC 1uF 10V LMK212105FML	TaiyoYuden
C28, C29, C30, C31	Cap-MLCC 10uF 35V GMK 325 F106ZH-B	TaiyoYuden
C3, C4, C14, C15	Cap-MLCC 100pF 50V VJ0805Y101KXA	Vishay
C34	Cap-MLCC 0.1uF 50V VJ0805Y104KXA	Vishay
C7	Cap-MLCC 0.1uF 50V VJ0805Y104KXA	Vishay
C8	CAP-SP 150uF 6.3V +/-20% EEFUE0J151R	Panasonic
COM1&2, PGOOD1	Terminal Silver 0.094" Dia 40F6004	Newark
D3	Switching Diode-Dual 70V 200mA BAW56F	Fairchild
D4	Schottky Diode 40V MBRS140T31A	ON Semiconductor
D5	Schottky Diode 40V MBRS140T31A	ON Semiconductor
IC1	IC controller LM2642	National
L1	Inductor 8u2H CEP125-8R2MC	Sumida
L2	Inductor 6uH CEP125-6R0MC	Sumida
P1	HEADER- BREAKAWAY 2 POST PITCH = 0.156" 26-48-1025	Molex
P2	HEADER- BREAKAWAY 2 POST PITCH = 0.156" 26-48-1025	Molex
P3	HEADER- BREAKAWAY 2 POST PITCH = 0.156" 26-48-1025	Molex
Q1	N-MOSFET FDS6690A	Fairchild
Q2	N-MOSFET FDS6690A	Fairchild
Q3	N-MOSFET FDS6690A	Fairchild
Q4	N-MOSFET FDS6690A	Fairchild
R1	Resistor Chip 13K 0.1W 0.05 CRCW0805*J	Vishay
R10	Resistor Chip 60K4 0.1W 0.01 CRCW08056042F	Vishay
R11	Resistor Chip 20K 0.1W 0.01 CRCW08052002F	Vishay
R13	Resistor Chip 13K 0.1W 0.05 CRCW0805*J	Vishay
R15	Resistor Thick Film 20m 0.5W 0.01 WSL20100.020.01	Vishay
R19	Resistor Chip 33K2 0.1W 0.01 CRCW08053322F	Vishay
R2, R6, R14, R16	Resistor Chip 100R 0.1W 0.05 CRCW08051000J	Vishay
R20	Resistor Chip 20K 0.1W 0.01 CRCW08052002F	Vishay
R22, R25	Resistor Chip 0R0 0.1W ±5% CRCW08050RJ	Vishay
R23	Resistor Chip 20K 0.1W 0.05 CRCW0805203J	Vishay
R24	Resistor Chip 20K 0.1W 0.05 CRCW0805203J	Vishay
R27	Resistor Chip 4R7 0.1W 0.05 CRCW08054R7J	Vishay
R28	Resistor Chip 220K 0.1W 0.05 CRCW0805*J	Vishay
R31, R32	Resistor Chip 4R7 0.1W 0.05 CRCW08054R7J	Vishay
R7	Resistor Thick Film 20m 0.5W 0.01 WSL20100.020.01	Vishay
SW1, SW2	Switch SPST 0.4VA 28V AC/DC A12AB	NKK

TABLE 3. Bill Of Materials (Continued)

Code	Description	Manufacturer
KS1, RS1, KS2, RS2	Jumper Tinned Copper Wire AWG26 L=0.5" x 4pcs.	

Output Voltage Setting

The output voltage for each channel is set by the ratio of a voltage divider as shown in (**R10, R11** and **R19, R20**)*Figure 3*. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{nom}}{V_{fb}} - 1\right)} \quad (1)$$

Where Vfb=1.238V. Although increasing the value of R1 and R2 will increase efficiency, this will also decrease accuracy. Therefore, a maximum value is recommended for R2 in order to keep the output within .3% of Vnom. This maximum R2 value should be calculated first with the following equation:

$$R_{2\ max} = \frac{.3\% \cdot V_{nom}}{200\ nA} \quad (2)$$

Where 200nA is the maximum current drawn by FBx pin.

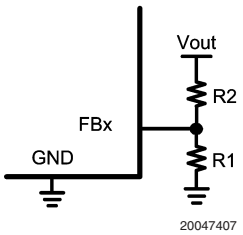


FIGURE 3. Output Voltage Setting

Example: Vnom=5V, Vfb=1.238V, Ifbmax=200nA.

$$R_{2\ max} = \frac{.003 \cdot 5V}{200\ nA} = 75\ k\Omega \quad (3)$$

Choose 60K

$$R_1 = \frac{60k}{\left(\frac{5V}{1.238V} - 1\right)} = 19.75\ k\Omega \cong 20\ k\Omega \quad (4)$$

The output voltage is limited by the maximum duty cycle as well as the minimum on time. *Figure 4* shows the limits for input and output voltages. The recommended maximum output voltage is approximately 1V less than the nominal input voltage. At 30V input, the minimum output is approximately 2.3V, and the maximum is approximately 27V.

For input voltages below 5.5V, VLIN5 must be connected to Vin through resistor **R26** (approximately 4.7 ohm).

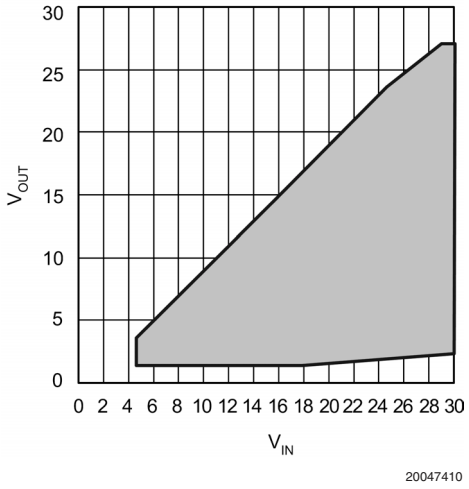


FIGURE 4. Available Output Voltage Range

Current Sensing and Limiting

As shown in *Figure 5*, the KSx and RSNSx pins are the inputs of the current sense amplifier. Current sensing is accomplished either by sensing the Vds of the top FET or by sensing the voltage across a current sense resistor (**R7** and **R15**) connected from VIN to the drain of the top FET. The advantage of sensing current across the top FET are reduced parts count, cost and power loss, whereas using a current sense resistor improves the current sense accuracy. Keeping the differential current-sense voltage below 200mV ensures linear operation of the current sense amplifier. Therefore, the Rdson of the top FET or the current sense resistor must be small enough so that the current sense voltage does not exceed 200mV when the top FET is on. There is a leading edge blanking circuit that forces the top FET on for at least 166ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. Additionally, a minimum voltage of at least 50mV across Rsns is recommended to ensure a high SNR at the current sense amplifier.

Assuming a maximum of 200mV across Rsns, the current sense resistor can be calculated as follows:

$$R_{sns\ max} = \frac{200\ mV}{I_{max} + \frac{1}{2} I_{rip}} \quad (5)$$

where Imax is the maximum expected load current, including overload multiplier (ie:120%), and Irip is the inductor ripple current (see *Equation (14)*). The above equation gives the maximum allowable value for Rsns. Switching losses will increase with Rsns, thus lowering efficiency.

The peak current limit is set by an external resistor (**R1** and **R13**) connected between the ILIMx pin and the KSx pin. An internal 10µA current sink on the ILIMx pin produces a voltage across the resistor to set the current limit threshold which is compared to the current sense voltage. A 10nF

Current Sensing and Limiting

(Continued)

capacitor across this resistor is required to filter unwanted noise that could improperly trip the current limit comparator.

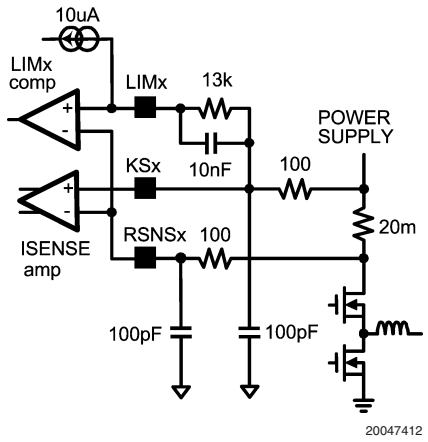


FIGURE 5. Current Sense and Current Limit

Current limit is activated when the inductor current is high enough to cause the voltage at the RSNSx pin to be lower than that of the ILIMx pin. This toggles the comparator, thus turning off the top FET immediately. The comparator is disabled either when the top FET is turned off or during the leading edge blanking time. The equation for current limit resistor, R_{lim}, is as follows:

$$R_{lim} = \frac{(I_{lim} + \frac{1}{2} I_{rip}) R_{sns}}{10\ \mu A} \quad (6)$$

Where Ilim is the load current at which the current limit comparator will be tripped.

When sensing current across the top FET, replace Rsns with the Rdson of the FET. This calculated Rlim value guarantees that the minimum current limit will not be less than Imax. It is recommended that a 1% tolerance resistor be used.

When sensing across the top FET, Rdson will show more variation than a current sense resistor, largely due to temperature. Rdson will increase proportional to temperature according to a specific temperature coefficient. Refer to the manufacturer's datasheet to determine the range of Rdson values over operating temperature or see the *COMPONENT SELECTION* section for a calculation of maximum Rdson. This will prevent Rdson variations from prematurely setting off the current limit comparator as the operating temperature increases.

Output Capacitor Selection (C8, C9, C22 and C23)

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple will often result in fewer design iterations.

ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient (ΔVc_s) is:

$$\Delta V_{c\_s} = (\delta\% - \varepsilon\%) \cdot V_{nom} - \frac{1}{2} V_{rip}. \quad (7)$$

Where $\pm\delta\%$ is the output voltage regulation window and $\pm\epsilon\%$ is the output voltage initial accuracy.

Example: Vnom = 5V, $\delta\%$ = 7%, $\epsilon\%$ = 3.4%, Vrip = 40mV peak to peak.

$$\Delta V_{c\_s} = (7\% - 3.4\%) \times 5V - \frac{40\ mV}{2}$$
$$= 160\ mV. \quad (8)$$

Since the ripple voltage is included in the calculation of ΔVc_s, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, ΔIc_s.

MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (Re) is too high, the load transient requirement will not be met, no matter how large the capacitance.

The maximum allowed total combined ESR is:

$$R_{e\_max} = \frac{\Delta V_{c\_s}}{\Delta I_{c\_s}} \quad (9)$$

Example: ΔVc_s = 160mV, ΔIc_s = 3A. Then Re_max = 53.3mΩ.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \cdot \left[\Delta V_{c\_s} - \sqrt{(\Delta V_{c\_s})^2 - (\Delta I_{c\_s} \cdot R_e)^2} \right]}{V_{nom} \cdot R_e^2} \quad (10)$$

Notice it is already assumed the total ESR, Re, is no greater than Re_max, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be

Output Capacitor Selection (C8, C9, C22 and C23) (Continued)

calculated before Cmin and after Re (see Inductor Selection below). Example: Re = 20mΩ, Vnom = 5V, ΔVc_s = 160mV, ΔIc_s = 3A, L = 8µH

$$C_{min} = \frac{8\,\mu H \cdot \left[160\,mV - \sqrt{(160\,mV)^2 - (3A \times 20\,m\Omega)^2}\right]}{5 \times (20\,m\Omega)^2}$$

$$= 47\,\mu F.$$

(11)

Generally speaking, Cmin decreases with decreasing Re, ΔIc_s, and L, but with increasing Vnom and ΔVc_s.

Inductor Selection

The size of the output inductor (**L1** and **L2**) can be determined from the desired output ripple voltage, Vrip, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in} - V_{nom}}{f \cdot V_{in}} \cdot \frac{V_{nom} \cdot R_e}{V_{rip}}$$

(12)

In the above equation, Re is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to Re. In the case of ceramic capacitors, replace Re with the true impedance.

Example: Vin (max)= 30V, Vnom = 5.0V, Vrip = 40mV, Re =20mΩ, f = 300kHz

$$L_{min} = \frac{30V - 5.0V}{300\,kHz \cdot 30V} \cdot \frac{5.0V \cdot 20\,m\Omega}{40\,mV}$$

$$L_{min} = 7\,\mu H$$

(13)

Lmin = 7µH

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than Lmin is selected, make sure that the Cmin requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$I_{rip} = \frac{(V_{in} - V_{nom})}{f \cdot L} \cdot D$$

(14)

Also important is the ripple content, which is defined by Irip /Inom. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content will cause too much loss in the inductor.

Example: Vin = 12V, Vnom = 5.0V, f = 300kHz, L = 8µH

$$I_{rip} = \frac{12V - 5.0V}{300\,kHz \cdot 8\,\mu H} \cdot \frac{5.0V}{12V} = 1.22A$$

(15)

Given a maximum load current of 3A, the ripple content is 1.2A / 3A = 40%.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

Input Capacitor Selection

The LM2642 eval. board provides 5 input capacitor options for each channel (**C5, C6, C28, C29, C32** and **C16, C17, C30, C31, C33**). Referring to *Table 2*, two capacitors are used on each channel and their placement depends on the method of current sensing. C6 and C16 can be installed when higher input capacitances are necessary.

The fact that the two switching channels of the LM2642 are 180˚ out of phase will reduce the RMS value of the ripple current seen by the input capacitors. This will help extend input capacitor life span and result in a more efficient system. Input capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. In applications in which output voltages are less than half of the input voltage, the corresponding duty cycles will be less than 50%. This means there will be no overlap between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current for duty cycles under 50% is:

$$I_{irrm} = \sqrt{I_1^2 D_1 (1 - D_1) + I_2^2 D_2 (1 - D_2) - 2 I_1 I_2 D_1 D_2}$$

(16)

where I1 is maximum load current of Channel 1, I2 is the maximum load current of Channel 2, D1 is the duty cycle of Channel 1, and D2 is the duty cycle of Channel 2.

Example: Imax_1 = 3.6A, Imax_2 = 3.6A, D1 = 0.42, and D2 = 0.275

$$I_{irrm} = \left[(3.6A)^2 \cdot 0.42 \cdot (1 - 0.42) + (3.6A)^2 \cdot 0.275 \cdot (1 - 0.275) - 2 \cdot 3.6A \cdot 3.6A \cdot 0.42 \cdot 0.275\right]^{.5}$$

$$= 2.75A.$$

(17)

Choose input capacitors that can handle 2.75A ripple RMS current at highest ambient temperature. In applications where output voltages are greater than half the input voltage, the corresponding duty cycles will be greater than 50%, and there will be overlapping input current pulses. Input ripple current will be highest under these circumstances. The input RMS current in this case is given by:

$$I_{irrm} = \left[\begin{array}{l}\left[I_1(1 - D_1) + I_2(1 - D_2)\right]^2 (D_1 + D_2 - 1) \\ + \left[I_1(1 - D_1) - I_2(D_2)\right]^2 (1 - D_2) + \\ \left[I_2(1 - D_2) - I_1(D_1)\right]^2 (1 - D_1)\end{array}\right]^{.5}$$

(18)

Where, again, I1 and I2 are the maximum load currents of channel 1 and 2, and D1 and D2 are the duty cycles. This equation should be used when both duty cycles are expected to be higher than 50%.

Input Capacitor Selection (Continued)

Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. The input capacitor should always be placed as close as possible to the current sense resistor or the drain of the top FET.

MOSFET Selection

BOTTOM FET SELECTION (Q2 AND Q4)

During normal operation, the bottom FET is switching on and off at almost zero voltage. Therefore, only conduction losses are present in the bottom FET. The most important parameter when selecting the bottom FET is the on resistance (Rdson). The lower the on resistance, the lower the power loss. The bottom FET power loss peaks at maximum input voltage and load current. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$R_{dson\_max} = \frac{1}{I_{max}^2 \cdot \left(1 - \frac{V_{nom}}{V_{in\_max}}\right)} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25^{\circ}C/W)\right] \cdot R_{\theta ja}} \quad (19)$$

where Tj_max is the maximum allowed junction temperature in the FET, Ta_max is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/˚C.

If the calculated Rdson_max is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the Imax term in the above equation, thus reducing Rdson. When using two FETs in parallel, multiply the calculated Rdson_max by 4 to obtain the Rdson_max for each FET. In the case of three FETs, multiply by 9.

$$R_{ds\_max} = \frac{1}{(3.6A)^2 \cdot \left(1 - \frac{5V}{30V}\right)} \times \frac{100^{\circ}C - 60^{\circ}C}{\left[1 + 0.01/^{\circ}C \cdot (100^{\circ}C - 25^{\circ}C)\right] \cdot 60^{\circ}C/W} = 35.3\,m\Omega \quad (20)$$

If the selected FET has an Rds value higher than 35.3Ω, then two FETs with an Rdson less than 141mΩ (4 x 35.3mΩ) can be used in parallel. In this case, the temperature rise on each FET will not go to Tj_max because each FET is now dissipating only half of the total power.

TOP FET SELECTION (Q1 AND Q3)

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

$$R_{ds\_max} = \frac{V_{in\_min} \cdot .4}{I_{max}^2 \cdot V_{nom}} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25^{\circ}C/W)\right] \cdot R_{\theta ja}} \quad (21)$$

Example: Tj_max = 100˚C, Ta_max = 60˚C, Rqja = 60˚C/W, Vin_min = 4.5V, Vnom = 5V, and Iload_max = 3.6A.

$$R_{ds\_max} = \frac{5.5V \times .4}{(3.6A)^2 \times 5V} \times \frac{100^{\circ}C - 60^{\circ}C}{\left[1 + 0.01/^{\circ}C \cdot (100^{\circ}C - 25^{\circ}C)\right] \cdot 60^{\circ}C/W} = 13\,m\Omega \quad (22)$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

Loop Compensation

The general purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked to determine small-signal performance. Loop gain is equal to the product of control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking it is a good idea to have a loop gain slope that is -20dB /decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60kHz in the case of LM2642. The higher the bandwidth is, the faster the load transient response speed will potentially be. However, if the duty cycle saturates during a load transient, further increasing the small signal bandwidth will not help. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain will be relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot.

Loop Compensation (Continued)

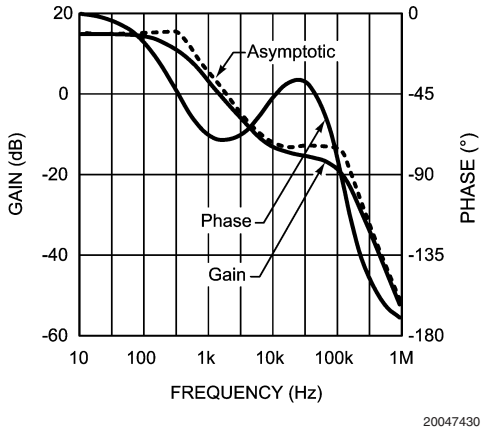


FIGURE 6. Control-Output Transfer Function

As shown in *Figure 6*, the control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency). The following can be done to create a -20dB /decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at fp, the second pole at fz, and the second zero at fn. The resulting output-control transfer function is shown in *Figure 7*.

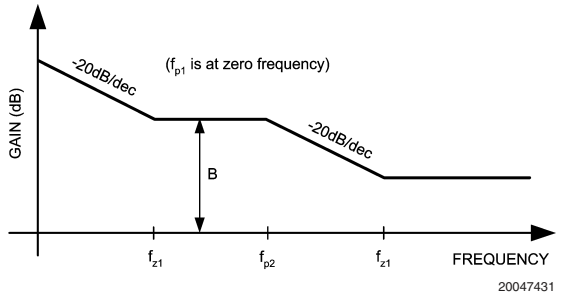


FIGURE 7. Output-Control Transfer Function

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_z = \frac{1}{2\pi R_e C_o} \quad (23)$$

$$f_p = \frac{1}{2\pi R_o C_o} + \frac{.5}{2\pi L f C_o} \quad (24)$$

Since fp is determined by the output network, it will shift with loading (Ro). It is best to use a minimum Iout value of approximately 100mA when determining the maximum Ro value.

Example: Re=20mΩ, Co=100uF, Romax=5V/100mA=50Ω:

$$f_z = \frac{1}{2\pi \cdot 20\,m\Omega \cdot 100\,\mu F} = 80\,kHz \quad (25)$$

$$f_{p\,min} = \frac{1}{2\pi \cdot 50\Omega \cdot 100\,\mu F} + \frac{.5}{2\pi \cdot 300k \cdot 8\mu \cdot 100\,\mu F} = 363\,Hz \quad (26)$$

First determine the minimum frequency (fpmin) of the pole across the expected load range, then place the first compensation zero at or below that value. Once fpmin is determined, Rc1 (**R23** and **R24**) should be calculated using:

$$R_{c1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right) \quad (27)$$

Where B is the desired gain in V/V at fp (fz1), gm is the transconductance of the error amplifier, and R1 and R2 are the feedback resistors. A gain value around 10dB (3.3v/v) is generally a good starting point.

Example: B=3.3v/v, gm=650m, R1=20KΩ, R2=60.4KΩ:

$$R_{c1} = \frac{3.3}{650\mu}\left(\frac{20k + 60.4k}{20k}\right) = 20.4\,k\Omega \cong 20\,k\Omega \quad (28)$$

Bandwidth will vary proportional to the value of Rc1. Next, Cc1 (**C19** and **C20**) can be determined with the following equation:

$$C_{c1} = \frac{1}{2\pi \cdot f_{p\,min} \cdot R_{c1}} \quad (29)$$

Example: fpmin=363Hz, Rc1=20KΩ:

$$C_{c1} = \frac{1}{2\pi \cdot 363\,Hz \cdot 20\,k\Omega} \cong 22\,nF \quad (30)$$

The compensation network (*Figure 8*) will also introduce a low frequency pole which will be close to 0Hz.

A second pole should also be placed at fz. This pole can be created with a single capacitor Cc2 (**C18** and **C21**) and a shorted Rc2 (see *Figure 8*). The minimum value for this capacitor can be calculated by:

$$C_{c2\,min} = \frac{1}{2\pi \cdot f_z \cdot R_{c1}} \quad (31)$$

Cc2 may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

Example: fz=80kHz, Rc1= 20KΩ:

$$C_{c2\,min} = \frac{1}{2\pi \cdot 80\,kHz \cdot 20\,k\Omega} \cong 100\,pF \quad (32)$$

A second zero can also be added with a resistor in series with Cc2 (**R22** and **R25**). If used, this zero should be placed at fn, where the control to output gain rolls off at -40dB/dec. Generally, fn will be well below the 0dB level and thus will have little effect on stability. Rc2 can be calculated with the following equation:

Loop Compensation (Continued)

$$R_{c2} = \frac{1}{2\pi \cdot f_n \cdot C_{c2}} \quad (33)$$

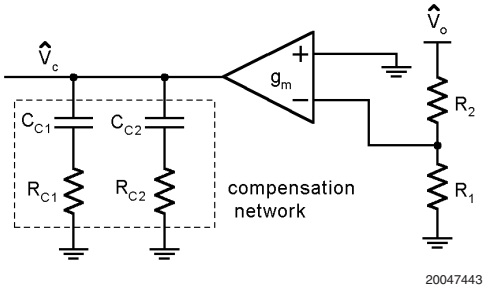
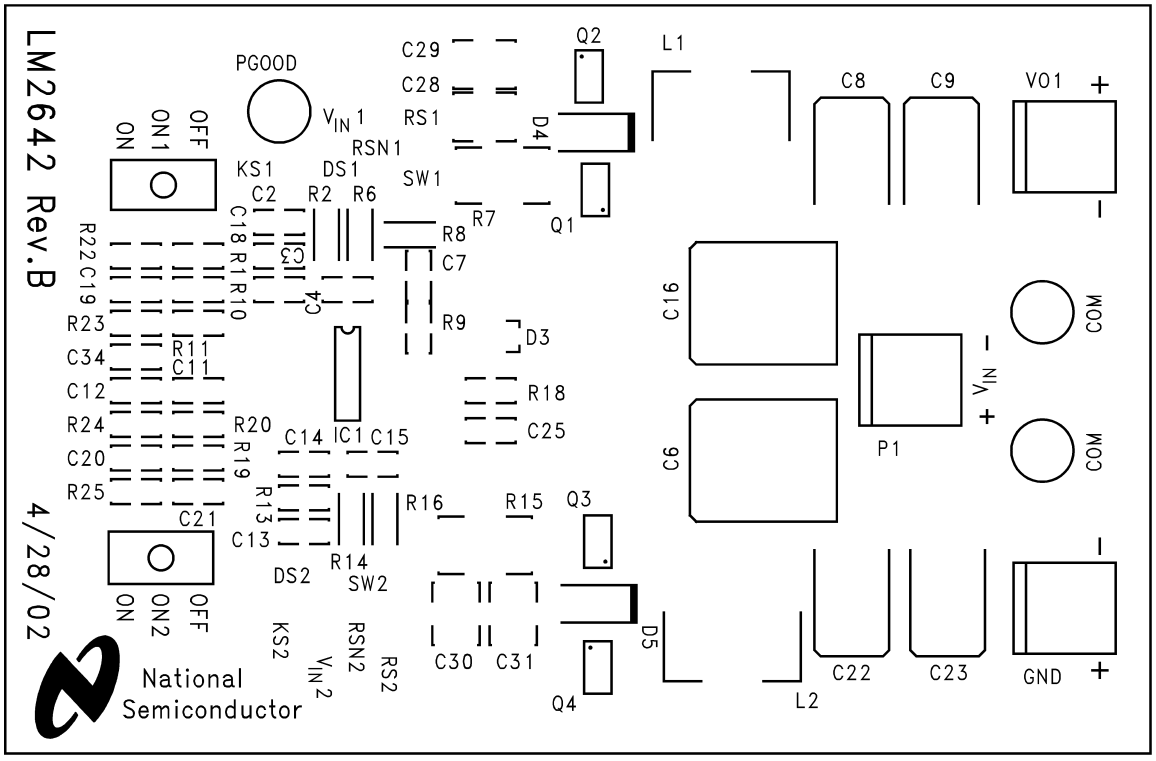


FIGURE 8. Compensation Network



Top Layer

FIGURE 9.

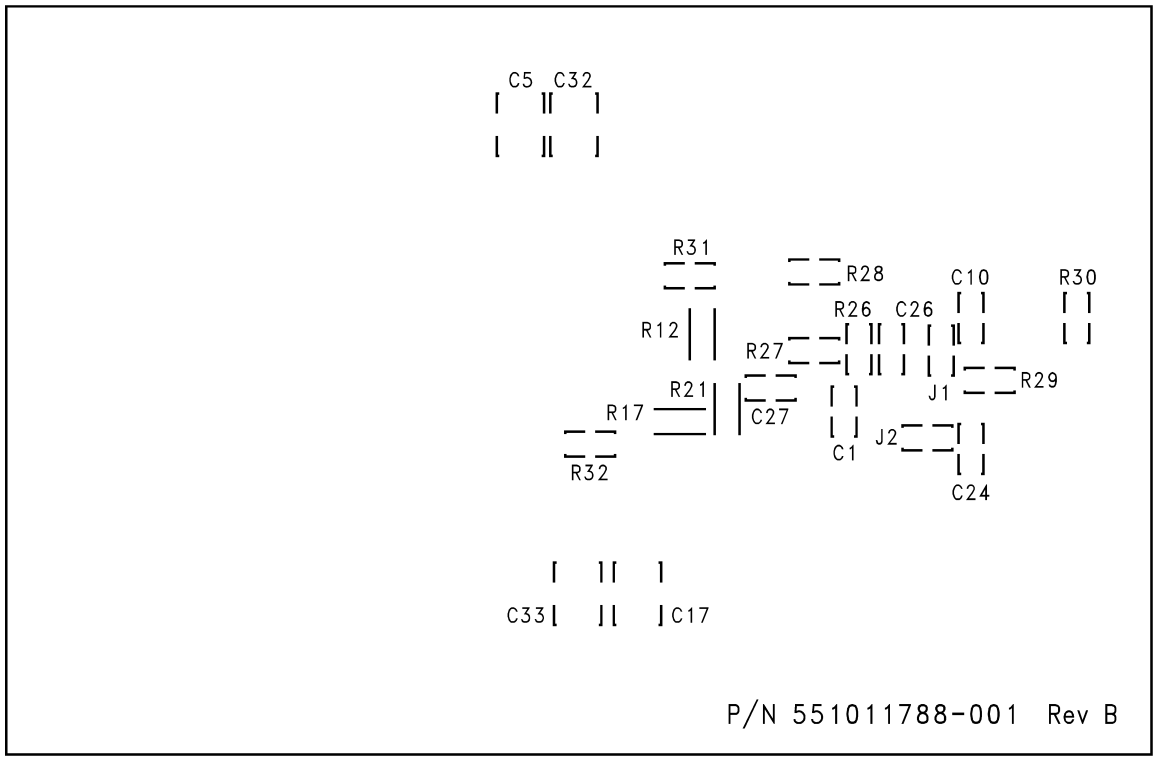


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FIGURE 10.

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