SCANSTA112 Designers Reference

National Semiconductor
Application Note 1259
April 2003

Introduction

The SCANSTA112 is the third device in a series that enable multi-drop address and multiplexing of IEEE-1149.1 scan chains. The 'STA112 is a superset of its predecessors - the SCANPSC110 and the SCANSTA111. The 'STA112 has all features and functionality of these two previous devices.

The 'STA112 is essentially a support device for the IEEE 1149.1 standard. It is primarily used to partition scan chains into managable sizes, or to isolate specific devices onto a seperate chain. The benefits of multiple scan chains are improved fault isolation, faster test times, faster programming times, and smaller vector sets.

In addition to scan chain partitioning, the device is also addressable for use in a multidrop backplane environment. In this configuration, multiple IEEE-1149.1 accessible cards with a 'STA112 on board can utilize the same backplane test bus for system-level IEEE-1149.1 access. This approach facilitates a system-wide commitment to structural test and programming throughout the entire system life cycle.

Operating Modes

ScanBridge Mode - ScanBridge mode refers to functionality and protocol that has been used by National since the introduction of the SCANPSC110 in 1993. This functionality consists of a multidrop, addressable, IEEE1149.1 switch. This enables one or more devices to be selected from many that are connected to a parallel IEEE1149.1 bus or backplane. The second function that ScanBridge mode accomplishes is to act as a mux for multiple IEEE1149.1 local scan chains. The Local Scan Ports (LSP) of the device creates a connection between one or more of the local scan chains to the backplane bus.

To accomplish this functionality the ScanBridge has two levels of protocol and an operational mode. Level 1 protocol refers to the required actions to address/select the desired ScanBridge.

Level 2 protocol is required to configure the multiplexing function and enable the connection (UNPARK) between the local scan chain and the backplane bus via an LSP.

Upon completion of Level 1 and 2 protocols the ScanBridge is prepared for its operational mode. This is where scan vectors are moved from the backplane bus to the desired local scan chain(s).

ScanBridge mode is the typical mode of operation. All overhead (protocol, register and pad-bit) is dealt with by most commercially available Automatic Test Pattern Generation (ATPG) tools. This is the same functionality that is contained in the SCANPSC110 and the SCANSTA111. Pertaining to the 'STA112, all forms of reset are effective if not disabled via the IgnoreReset bit in the Control Register. Level 1 and 2 protocols are required. The scan chains will contain ScanBridge registers and pad-bits. If the devices that are connected to the LSP do not have the $\overline{TRST}$ pin available, the preamble needs to select and configure the ScanBridge and then do a 5 high TMS reset and then re-select and configure the ScanBridge. This insures that all of the TAPs on the LSPs are in a reset mode.

Transparent Mode - Transparent mode refers to a condition of operation in which there are no pad-bits or 'STA112 registers in the scan chain. The Transparent mode of operation is available in both ScanBridge and Stitcher modes. Only the activation method differs. Once transparent mode has been activated there is no difference in operation. Transparent mode allows for the use of vectors that have been generated for a chain where these bits were not accounted. When in transparent mode the chain may take on the following configuration:

$TDI_B \rightarrow LSP_{B1} \rightarrow LSP_{01} \rightarrow LSP_n \rightarrow TDO_B$

Conversely, when not in transparent mode the chain may take on the following configuration:

Instruction: $TDI_B \rightarrow$ IR 8-bit $\rightarrow LSP_a \rightarrow$ PAD $\rightarrow LSP_n \rightarrow$ PAD $\rightarrow TDO_B$

Data Shift: $TDI_B \rightarrow$ DR 8-bit $\rightarrow LSP_a \rightarrow$ PAD $\rightarrow LSP_n \rightarrow$ PAD $\rightarrow TDO_B$

Transparent mode is controlled by two completely different mechanisms depending on the mode of operation. In ScanBridge mode the active instruction enables transparent mode. (e.g. *TRANSPARENT4* or *TRANSPARENTENABLE*). The TRANS bit in the Control Register and TRANS pin are ignored. When the 'STA112 is in Stitcher mode, the TRANS bit in the Control Register (initialized by the TRANS pin) is used to control the activation of transparent mode.

Transparent LSP Mode - This mode is enabled by programming mode-1 bit-7 to a "1". In this mode no pad bits will be placed between unparked lsp's, but the scanbridge register and the last pad bit are part of the chain. In transparent-lsp mode the chain may take on the following configuration:

Instruction: $TDI_B \rightarrow$ IR 8-bit $\rightarrow LSP_a \rightarrow LSP_n \rightarrow$ PAD $\rightarrow TDO_B$

Data Shift: $TDI_B \rightarrow$ DR 8-bit $\rightarrow LSP_a \rightarrow LSP_n \rightarrow$ PAD $\rightarrow TDO_B$

This mode offers two advantages to full transparent mode. It is capable of higher speeds than full transparent mode due to the trailing sync bit, and the tester does not lose software control of the 'STA112 in this mode. The bridge register and the trailing pad bit can be specified by the HIR, HDR, TIR, and TDR instructions in SVF.

ScanBridge in Transparent Mode - This mode of operation was first introduced into the ScanBridge family of devices with the 'STA111. The intent of this feature is to allow the use of tools (e.g. FPGA programming tools) that are not able to deal with the insertion of ScanBridge registers and pad-bits into the scan chain. The user is required to insert a preamble into the series of scan vectors that performs Level 1 and 2 protocol. This selects a specific 'STA112 and one LSP. Once the selection is completed, the LSP signals become a buffer version of the backplane signals. In this mode the TAPs on the LSPs can be reset by way of the 5 high TMS reset without the ScanBridge responding to it.

Operating Modes (Continued)

With the addition of the IgnoreReset bit in the Control Register, the TAPs on the LSPs can also be reset by way of the $\overline{TRST}_B$ reset without the ScanBridge responding to it. It is possible to lose software control of the device in this mode where the only method of recovery is to toggle the $\overline{RESET}$ pin or to cycle the power. Therefore, for applications that expect the 'STA112 to behave in the same manner as the SCANSTA111 it is suggested the $\overline{TRST}_B$ and the $\overline{RESET}$ pins be connected together.

Stitcher Mode - Stitcher Mode is a method of skipping Level 1 and 2 protocol of the ScanBridge mode of operation. This is accomplished via external pins. When in stitcher mode the 'STA112 will go directly to the operational mode.

The Stitcher mode is intended to provide a method to utilize the multiplexing capability of the 'STA112 with vector delivery tools that do not handle the addressing protocol.

Stitcher in Transparent Mode - This mode allows the 'STA112 to function as an externally (pin) controlled multiplexer. There are no registers or pad-bits placed into the scan chains. This mode is very useful when the user is in a lab environment using multiple tools. With the addition of the IgnoreReset bit in the Control Register, the TAPs on the LSPs can be reset by way of the 5 high TMS reset without the 'STA112 responding to it. It is possible to lose software control of the device in this mode where the only method of recovery is to toggle the $\overline{RESET}$ pin or cycle power.

Resets and the Various Operational Modes - To combine the Stitcher function with the ScanBridge function it is necessary to define three types of reset available to the device and what effects that they have on the device. The first is power-up and $\overline{RESET}$. When power is first applied or the $\overline{RESET}$ pin is asserted and then deasserted, the device will execute its most complete reset. At this time all internal registers are reset to the initial value. Registers whose initial values are controlled by external pins will read the value on the pin and set the register value accordingly as in *Table 1*. Register bits not defined in *Table 1* are set to an initial value of zero.

TABLE 1. Initial Register Values

Register	External Pins	Internal Value
Instruction	N/A	XXH ID code
Mode0	N/A	01H Select LSP_{00}
Control	$MPsel_{B1/\overline{B0}}$, $SB/\overline{S}$, TRANS, TLR_TRST, TLR_TRST_6	0b IgnoreReset
LSPSel	$LSPsel_{(0-6)}$	

The second is the $\overline{TRST}$ pin. This is the classical IEEE1149.1 reset pin. This pin is masked by the Control Register IgnoreReset bit to disable it via software control. This feature will enable users to propagate a $\overline{TRST}$ reset pulse through the 'STA112 without resetting the Level 1 and 2 protocols. This will place all unparked LSP TAP controllers in the *Unparked* state. All parked LSP TAPs will be placed in the *Parked-TLR* state.

Lastly is 5 High TMS. This exploits the fact that the IEEE1149.1 state machine will be in the *Test-Logic-Reset* (TLR) state after 5 high TMS. This reset behaves in two distinct ways. When the device is utilized as a standard ScanBridge, not in transparent mode, this reset will reset all TAP controllers and the Level 1 and 2 protocols. This is the same functionality as $\overline{TRST}$. When the 'STA112 is utilized as ScanBridge in Transparent Mode, this method of reset is ignored. This second reaction is hardwired into the device and is not software controllable.

It should be noted that when the IgnoreReset bit is set and a $\overline{TRST}$ is performed, target devices with $\overline{TRST}$ pins on unparked LSP's will receive a $\overline{TRST}$ assertion while target devices without a $\overline{TRST}$ pin do not. In this case the tester should sequence the target TAPS back to the TLR state to ensure synchronization between all the targeted TAPs.

When utilizing the 'STA112 there are times in which the user may wish to reset devices that are connected to the LSPs without resetting the 'STA112. The $\overline{RESET}$ pin is the ultimate reset and will override all software control. Software masking of the various reset is controlled via the IgnoreReset bit that is contained in the Control Register.

Table 2 indicates the effect of the resets during the various modes of operation when IgnoreReset is deasserted (set to "0"). *Table 3* indicates the effect of the resets during the various modes of operation when IgnoreReset is asserted (set to "1").

TABLE 2. Reset effect when IgnoreReset is deasserted (set to "0")

IgnoreReset=0	ScanBridge Mode	Transparent Mode (Note 1)	Stitcher Mode
$\overline{RESET}$	Full Reset	Full Reset	Full Reset
$\overline{TRST}$	Full Reset	Full Reset	Full Reset
5 high TMS	Full Reset	Ignored	Full Reset

TABLE 3. Reset effect when IgnoreReset is asserted (set to "1")

IgnoreReset=1	ScanBridge Mode	Transparent Mode (Note 1)	Stitcher Mode
$\overline{RESET}$	Full Reset	Full Reset	Full Reset
$\overline{TRST}$	Ignored	Ignored	Ignored
5 high TMS	Ignored	Ignored	Ignored

Note 1: Transparent mode is available in both ScanBridge and Stitcher mode

Value of LSPn Ports while Parked in TLR

When a 'STA112 LSP is parked in *TLR*, the pins of the LSP are driven to a safe value (e.g. $\overline{TRST}$n = "0"). The LSP pins can be tristated via the $\overline{OE}$ pin. The value of "0" for $\overline{TRST}$n was selected to insure that all TAPs that are connected to LSPs are held in *TLR*. There are devices that are not IEEE-1149.1 compliant and do not function properly when their $\overline{TRST}$ pin is held low. To overcome this limitation, the 'STA112 has a TLR_TRST and a TLR_TRST_6 input pin. The value on these pins will be the default driven on the $\overline{TRST}_{(0-5)}$ and $\overline{TRST}_6$ pins while their TAP controllers are in *TLR*. If the TLR_TRST pin is set to "1", the outputs of the $\overline{TRST}_n$ pins will force a "1" - except when $\overline{RESET}$ is forced to

Value of LSPn Ports while Parked in TLR (Continued)

a "0". Additionally, $\overline{TRST}_{(0-5)}$ pins will force a "0" when $\overline{TRST}_b$ is forced to a "0" regardless of the IgnoreReset bit in the Control Register.

Switching between Modes of Operation

Stitcher Mode to Stitcher Transparent Mode - This change of operational modes may be useful if the user needs to change the LSPs in the chain and then use the device as a buffered version of the backplane signals. (Note the same functionality can be accomplished in Transparent ScanBridge Mode) When the 'STA112 is hardwired to be in Stitcher Mode, the chain consists of the currently selected internal 'STA112 register, plus the LSPs that are selected via the LSPSEL (LSP Select) Register, plus the pad bits associated with the selected LSPs. The LSPSEL register contents were initialized as the value of the respective $LSPSel_{(0-6)}$ pins, but may be changed by selecting the LSPSEL register (using the *LSPSEL* instruction) and loading in new values. Always make a note as to which LSP's are currently on the scan chain, both for instructions and data. The Control Register may then be modified in the same manner as the LSPSEL register. Note that the Control Register assumed the default values (see *Table 12*) at power-up. A caution regarding $MPsel_{B1/\overline{B0}}$ is described in the section titled **Level 2 Protocol** (CONTROLSEL instruction) and the section titled **Register Descriptions** (Control Register Description). Changing the Control Register contents will allow the 'STA112 to be placed into the Stitcher Transparent Mode. Because the TAPs on the LSPs and the TAP of the master have to be synchronized at all times, there is no need to go through a re-synchronization. As the TAPs move into the *UPDATE-DR* state the internal instruction, data, and pad-bit registers of the 'STA112 are removed from the chain. Therefore, the next data or instruction scans only need to account for the registers that reside on selected LSPs. This mode can only be exited by a reset, $\overline{TRST}_B$ (if the IgnoreReset bit is not asserted), or a $\overline{RESET}$, or by a power cycle. Note: during this mode of operation 5 TMS high resets are ignored.

Stitcher Transparent Mode to Stitcher Mode - This can only be accomplished by performing a $\overline{TRST}$ or $\overline{RESET}$ reset.

State Machines

The 'STA112 is IEEE 1149.1-compatible, in that it supports all required 1149.1 operations. In addition, it supports a higher level of protocol, (Level 1), that extends the IEEE 1149.1 Std. to a multi-drop environment.

In multi-drop scan systems, a scan tester can select individual 'STA112s for participation in upcoming scan operations. 'STA112 selection is accomplished by simultaneously scanning a device address out to multiple 'STA112s. Through an on-chip address matching process, only those 'STA112s whose statically-assigned address matches the scanned-out address become selected to receive further instructions from the scan tester. 'STA112 selection is done using a Level-1 protocol, while follow-on instructions are sent to selected 'STA112s by using a Level-2 protocol.

The 'STA112 contains three distinct but coupled types of state-machines (see *Figure 1*). The first of these is the TAP-control state-machine, which is used to drive the 'STA112s scan ports in conformance with the 1149.1 Standard. The second is the 'STA112-selection state-machine (*Figure 2*). The third state-machine actually consists of seven identical but independent state-machines (see *Figure 3*), one per 'STA112 local scan port. Each of these scan port selection state-machines allows individual local ports to be inserted into and removed from the 'STA112s overall scan chain.

The 'STA112 selection state-machine performs the address matching which gives the 'STA112 its multi-drop capability. That logic supports single-'STA112 access, multi-cast, and broadcast. The 'STA112 selection state-machine implements the chip's Level-1 protocol.

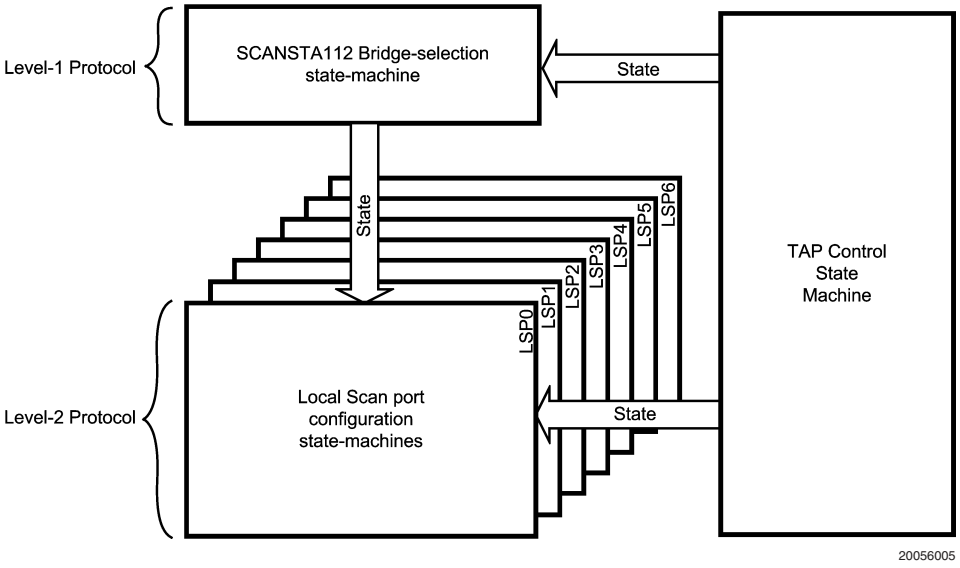

FIGURE 1. SCANSTA112 State Machines

State Machines (Continued)

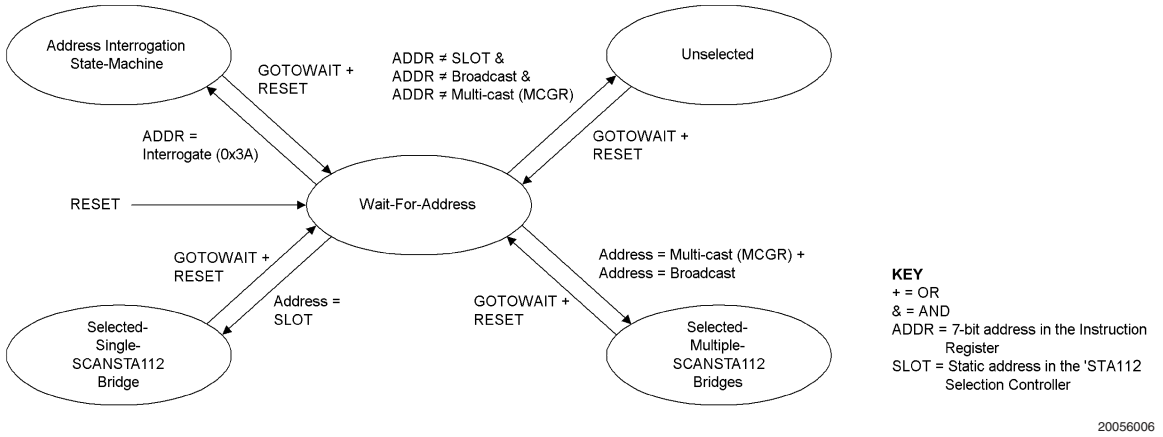

FIGURE 2. State Machine for SCANSTA112 Selection Controller

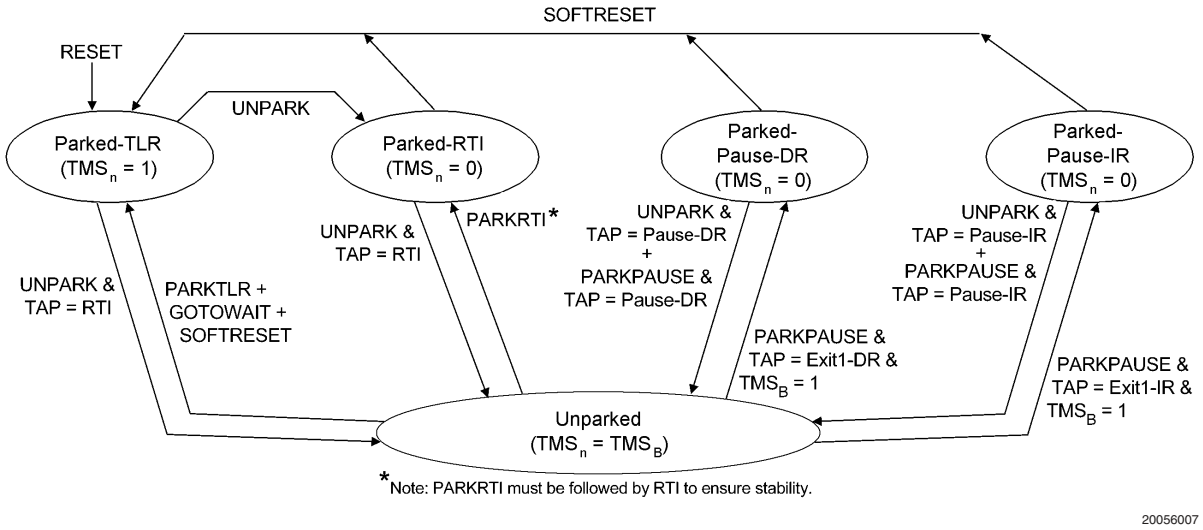

FIGURE 3. Local SCANSTA112 Port Configuration State Machine

The 'STA112's scan port-configuration state-machine is used to control the insertion of local scan ports into the overall scan chain, or the isolation of local ports from the chain. From the perspective of a system's (single) scan controller, each 'STA112 presents only one scan chain to the master. The 'STA112 architecture allows one or more of the 'STA112's local ports to be included in the active scan chain.

Each local port can be parked in one of four stable states (*Parked-TLR*, *Parked-RTI*, *Parked-Pause-DR* or *Parked-Pause-IR*), either individually or simultaneously with other local ports. Parking a chain removes that local chain from the active scan chain. Conversely, a parked chain can be unparked, causing the corresponding local port to be inserted into the active scan chain.

As shown in *Figure 3*, the 'STA112's seven scan port-configuration state-machines allow each of the part's local ports to occupy a different state at any given time. For example, some ports may be parked, perhaps in different states, while other ports participate in scan operations. The state-diagram shows that some state transitions depend on the current state of the TAP-control state-machine. As an example, a local port which is presently in the *Parked-RTI* state does not become unparked (i.e., enter the *Unparked* state) until the 'STA112 receives an *UNPARK* instruction and the 'STA112's TAP state-machine enters the *Run-Test/Idle* state.

Similarly, certain transitions of the scan port-configuration state-machine can force the 'STA112's LSP-control state-machine into specific states. For example, when a local port is in the *Unparked* state, the 'STA112 receives the *PARKRTI* instruction and the TAP is transitioned through *Run-Test/Idle* state, the Local Port controller enters the *Parked-RTI* state in which TMS_n will be held low until the port is later unparked. Once the *Park-RTI* instruction has been updated into the instruction register the TAP MUST be transitioned through the *Run-Test/Idle* state. While TMS_n is held low, all devices on that local scan chain remain in their current TAP State (the *RTI* TAP controller state in this example).

The 'STA112's scan port-configuration state-machine implements part of the 'STA112's Level-2 protocol. In addition, the

State Machines (Continued)

'STA112 provides a number of Level-2 instructions for functions other than local scan port confguration. These instructions provide access to and control of various registers within the 'STA112. This set of instructions includes:

BYPASS	*CNTRSEL*	*EXTEST*
LFSRON	*SAMPLE/PRELOAD*	*LFSROFF*
IDCODE	*CNTRON*	*MODESEL*
CNTROFF	*MCGRSEL*	*GOTOWAIT*
LFSRSEL		

Figure 4 illustrates how the 'STA112's state-machines interact. The 'STA112-selection state-machine enables or disables operation of the chip's seven port-selection state-machines. In 'STA112s which are selected via Level-1 protocol (either as individual 'STA112s or as members of broadcast or multi-cast groups), Level-2 protocol commands can be used to park or unpark local scan ports. Note that most transitions of the port-configuration state-machines are gated by particular states of the 'STA112's TAP-control state-machine, as shown in *Figure 3* or *Figure 4*.

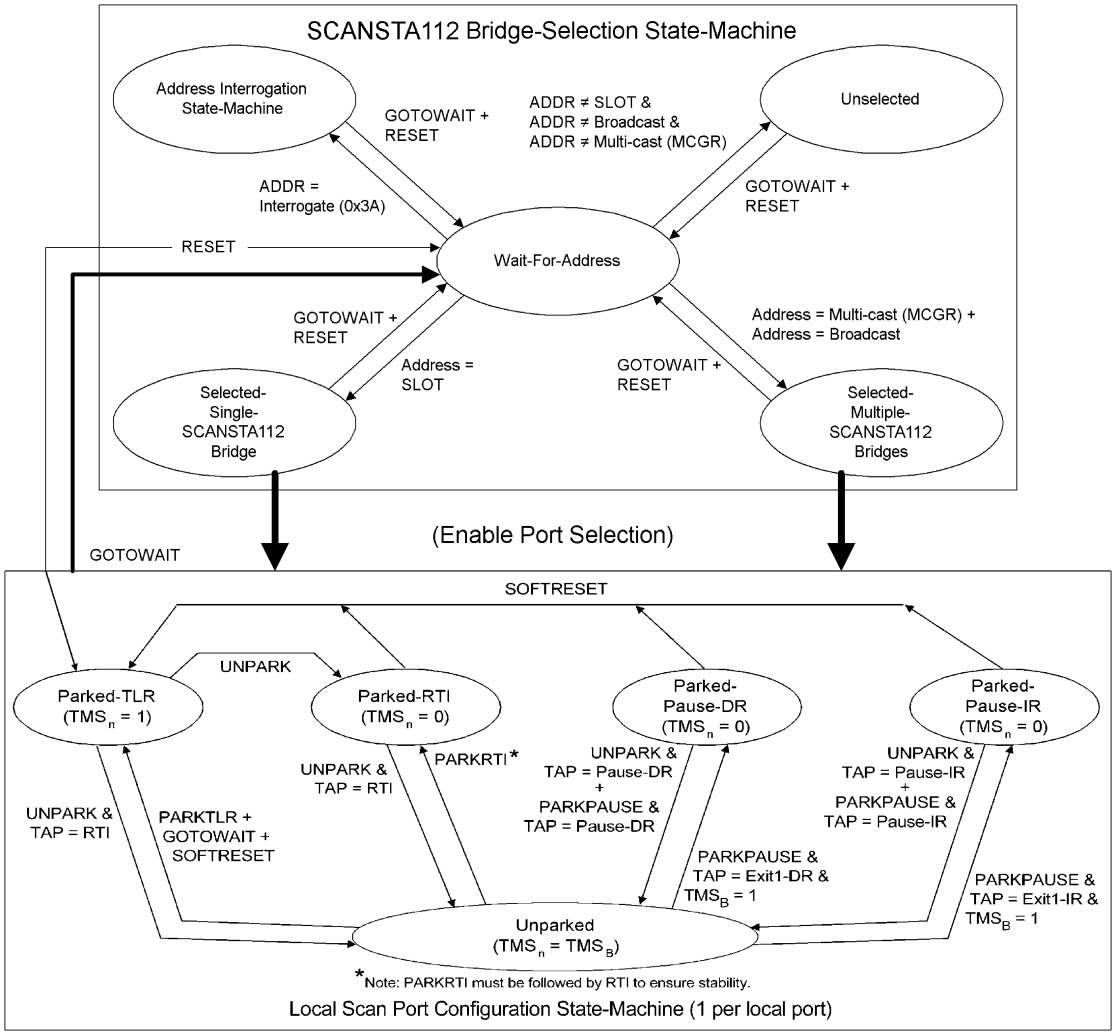

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FIGURE 4. Relationship Between SCANSTA112 State Machines

Following a hardware reset, the TAP controller state-machine is in the *Test-Logic-Reset* (TLR) state; the 'STA112-selection state-machine is in the *Wait-For-Address* state; and each of the seven port-selection state-machines is in the *Parked-TLR* state. The 'STA112 is then ready to receive Level-1 protocol, followed by Level-2 protocol.

Tester/SCANSTA112 Interface

An IEEE 1149.1 system tester sends instructions to a 'STA112 via that 'STA112's backplane scan-port. Following test logic reset, the 'STA112's selection state-machine is in the *Wait-For-Address* state. When the 'STA112's TAP controller is sequenced to the *Shift-IR* state, data shifted in through the TDI_B input is shifted into the 'STA112's instruction register. Note that prior to successful selection of a 'STA112, data is not shifted out of the instruction register and out through the 'STA112's TDO_B output, as it is during normal scan operations. Instead, as each new bit enters the instruction register's most-significant bit, data shifted out from the least-significant bit is discarded, and the TDO_B output is held in tristate to prevent contention with other data.

When the instruction register is updated with the address data, the 'STA112's address-recognition logic compares the 8 least-significant bits of the instruction register with the 8-bit assigned address which is statically present on the $S_{(0-7)}$ inputs. Simultaneously, the scanned-in address is compared with the reserved Broadcast and Multi-cast addresses. If an address match is detected, the 'STA112-selection state-machine enters one of the two selected states. If the scanned address does not match a valid single-slot address or one of the reserved broadcast/multi-cast addresses, the 'STA112-selection state-machine enters the *Unselected* state.

Note that the SLOT inputs should not be set to a value corresponding to a multi-cast group, or to the broadcast address. Also note that the single 'STA112 selection process must be performed for all 'STA112s which are subsequently to be addressed in multi-cast mode. This is required because each such device's Multicast Group Register (MCGR) must be programmed with a multi-cast group number, and the MCGR is not accessible to the test controller until that 'STA112 has first entered the *Selected-Single-'STA112* state.

Once a 'STA112 has been selected, Level-2 protocol is used to issue commands and to access the chip's various registers.

Register Set

The 'STA112 includes a number of registers which are used for 'STA112 selection and configuration, scan data manipulation, and scan-support operations. These registers can be grouped as shown in *Table 4*.

The specific fields and functions of each of these registers are detailed in the section of this document titled Register Descriptions.

Note that when any of these registers is selected for insertion into the 'STA112's scan-chain, scan data enters through that register's most-significant bit. Similarly, data that is shifted out of the register is fed to the scan input of the next-downstream device in the scan-chain.

TABLE 4. Register Descriptions

Register Name	Bits	BSDL Name	Description
Instruction Register	8	INSTRUCTION	'STA112 addressing and instruction-decode IEEE Std. 1149.1 required register
Boundary-Scan Register	22	BOUNDARY	IEEE Std. 1149.1 required register
Bypass Register	1	BYPASS	IEEE Std. 1149.1 required register
Device Identification Register	32	IDCODE	IEEE Std. 1149.1 optional register
Multi-Cast Group Register	2	MCGR	'STA112 group address assignment
Mode $Register_0$	8	$MODE_0$	'STA112 local-port configuration and control bits
Mode $Register_1$	8	$MODE_1$	'STA112 local-port configuration and control bits
Mode $Register_2$	8	$MODE_2$	'STA112 Shared GPIO configuration bits
Linear-Feedback Shift Register	16	LFSR	'STA112 scan-data compaction (signature generation)
TCK Counter Register		CNTR	Local-port TCK clock-gating (for BIST)
Shared GPIO $Register_{(0-n)}$	8	$SGPIO_n$	*'STA112 Shared GPIO control bits*
Control Register	8	CONTROL	Control Scanbridge/Stitcher mode, Master Port Selection, and more
LSP Select Register	8	LSPSEL	Selection of LSPs for Stitcher mode

Level 1 Protocol (Addressing Modes)

The 'STA112 supports single and multiple modes of addressing a 'STA112. The single mode will select one 'STA112 and is called Direct Addressing. More than one 'STA112 device can be selected via the Broadcast and Multi-Cast Addressing modes.

DIRECT ADDRESSING: The 'STA112 enters the *Wait-For-Address* state when:

1. its TAP Controller enters the *Test-Logic-Reset* state, or
2. its instruction register is updated with the *GOTOWAIT* instruction (while either selected or unselected).

Each 'STA112 within a scan network must be statically configured with a unique address via its $S_{(0-7)}$ inputs. While the 'STA112 controller is in the *Wait-For-Address* state, data shifted into bits 7 through 0 of the instruction register is compared with the address present on the $S_{(0-7)}$ inputs in the *Update-IR* state. If the eight (8) bits of the instruction register match the address on the $S_{(0-7)}$ inputs, (see *Figure 5*) the 'STA112 becomes selected, and is ready to receive Level 2 Protocol (i.e., further instructions). When the 'STA112 is selected, its device identification register is inserted into the active scan chain.

All 'STA112s whose $S_{(0-7)}$ address does not match the instruction register address become unselected. They will remain unselected until either their TAP Controller enters the *Test-Logic-Reset* state, or their instruction register is updated with the *GOTOWAIT* instruction.

BROADCAST ADDRESSING: The Broadcast Address allows a tester to simultaneously select all 'STA112s in a test network. This mode is useful in testing systems which contain multiple identical boards. To avoid bus contention between scan-path output drivers on different boards, each 'STA112's TDO_B buffer is always TRI-STATEd while in Broadcast mode. In this configuration, the on-chip Linear Feedback Shift Register (LFSR) can be used to accumulate a test result signature for each board that can be read back later by direct-addressing each board's 'STA112.

MULTICAST ADDRESSING: As a way to make the broadcast mechanism more selective, the 'STA112 provides a Multi-cast addressing mode. A 'STA112's multi-cast group register (MCGR) can be programmed to assign that 'STA112 to one of four (4) Multi-Cast groups. When 'STA112s in the *Wait-For-Address* state are updated with a Multi-Cast address, all 'STA112s whose MCGR matches the Multi-Cast group will become selected. As in Broadcast mode, TDO_B is always TRI-STATEd while in Multi-cast mode.

TABLE 5. SCANSTA112 Address Modes

Address Type	Hex Address	Binary Address	TDO_B State
Direct Address	00 to 39, 40 to FF.	00000000 to 00111010 01000000 to 11111111	Normal IEEE Std. 1149.1
Interrogation Address	3A	00111010	Force strong "0" or weak "1" as ones-complement address is shifted out.
Broadcast Address	3B	00111011	Always TRI-STATED
Multi-Cast Group 0	3C	00111100	Always TRI-STATED
Multi-Cast Group 1	3D	00111101	Always TRI-STATED
Multi-Cast Group 2	3E	00111110	Always TRI-STATED
Multi-Cast Group 3	3F	00111111	Always TRI-STATED

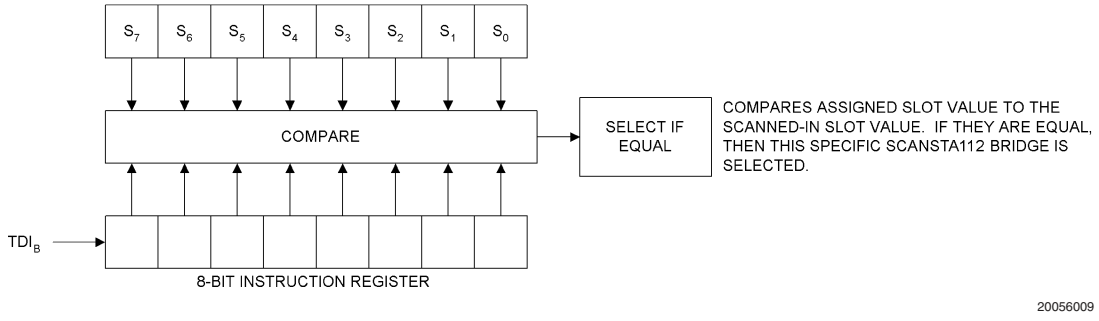

FIGURE 5. Direct Addressing: Device Address Loaded into Instruction Register

Level 1 Protocol (Addressing Modes) (Continued)

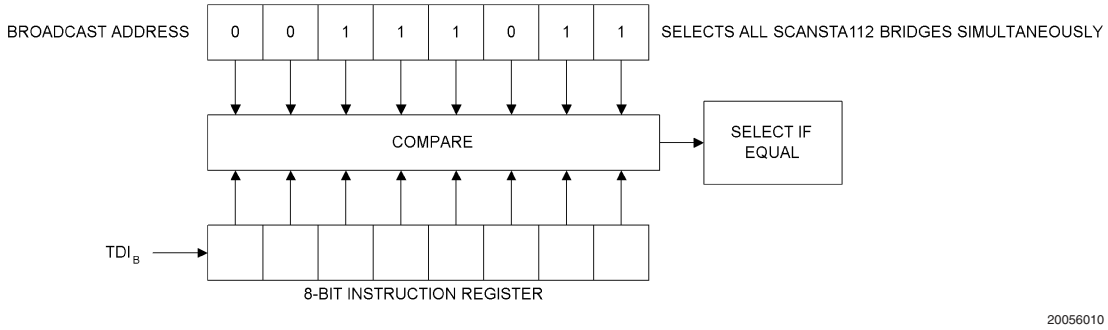

FIGURE 6. Broadcast Addressing: Address Loaded into Instruction Register

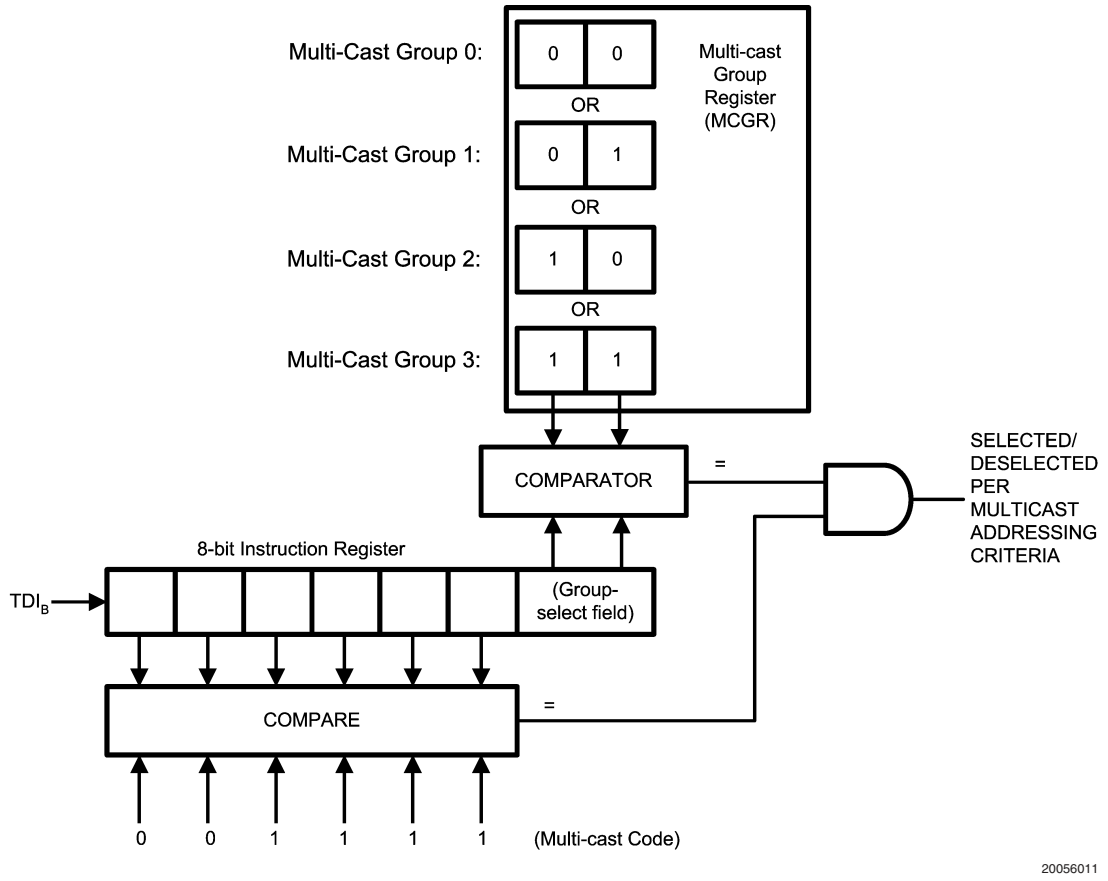

FIGURE 7. Multi-Cast Addressing: Address Loaded into Instruction Register

Level 2 Protocol

Once the ’STA112 has been successfully addressed and selected, its internal registers may be accessed via Level-2 Protocol. Level-2 Protocol is compliant to IEEE Std. 1149.1 TAP protocol with one exception: if the ’STA112 is selected via the Broadcast or Multi-Cast address, TDO_B will always be TRI-STATED. (The TDO_B buffer must be implemented this way to prevent bus contention.) Upon being selected, (i.e., the ’STA112 Selection controller transitions from the *Wait-For-Address* state to one of the Selected states), each of the local scan ports (LSP_0, LSP_1, LSP_2, LSP_3, LSP_4, LSP_5, LSP_6) remains parked in one of the following four TAP Controller states: *Test-Logic-Reset*, *Run-Test/Idle*, *Pause-DR*, or *Pause-IR* and the active scan chain will consist of: TDI_B through the instruction register (or the IDCODE register) and out through TDO_B.

$TDI_B \rightarrow$ Instruction Register $\rightarrow TDO_B$

The *UNPARK* instruction (described later) is used to insert one or more local scan ports into the active scan chain. *Table 8* describes which local ports are inserted into the chain, and in what order.

LEVEL 2 INSTRUCTION TYPES There are two types of instructions (reference *Table 6*):

1. Instructions that insert a ’STA112 register into the active scan chain so that the register can be captured or updated (*BYPASS*, *SAMPLE/PRELOAD*, *EXTEST*, *IDCODE*, *MODESEL*, *MCGRSEL*, *LFSR-SEL*, *CNTRSEL*, *CONTROLSEL*, *LSPSEL*).
2. Instructions that configure local ports or control the operation of the linear feedback shift register and counter registers (*UNPARK*, *PARKTRL*, *PARKRTI*, *PARKPAUSE*, *GOTOWAIT*, *SOFTRESET*, *LFSRON*, *LFSROFF*, *CNTRON*, *CNTROFF*, *TRANSPARENTENABLE*). These instructions, along with any other yet undefined Op-Codes, will cause the device identification register to be inserted into the active scan chain.

Level 2 Protocol (Continued)

TABLE 6. Level 2 Protocol and Op-Codes

Instructions	Hex Op-Code	Binary Op-Code	Data Register
BYPASS	FF	1111 1111	Bypass Register
EXTEST	00	0000 0000	Boundary-Scan Register
SAMPLE/PRELOAD	81	1000 0001	Boundary-Scan Register
IDCODE	AA	1010 1010	Device Identification Register
UNPARK	E7	1110 0111	Device Identification Register
PARKTLR	C5	1100 0101	Device Identification Register
PARKRTI	84	1000 0100	Device Identification Register
PARKPAUSE	C6	1100 0110	Device Identification Register
GOTOWAIT (Note 2)	C3	1100 0011	Device Identification Register
MODESEL	8E	1000 1110	Mode $Register_0$
$MODESEL_1$	82	1000 0010	Mode $Register_1$
$MODESEL_2$	83	1000 0011	Mode $Register_2$
$MODESEL_3$	85	1000 0101	Mode $Register_3$
MCGRSEL	03	0000 0011	Multi-Cast Group Register
SOFTRESET	88	1000 1000	Device Identification Register
LFSRSEL	C9	1100 1001	Linear Feedback Shift Register
LFSRON	0C	0000 1100	Device Identification Register
LFSROFF	8D	1000 1101	Device Identification Register
CNTRSEL	CE	1100 1110	32-Bit TCK Counter Register
CNTRON	0F	0000 1111	Device Identification Register
CNTROFF	90	1001 0000	Device Identification Register
DEFAULT_BYPASS	07	0000 0111	Set Bypass_reg as default data register
TRANSPARENT0	A0	1010 0000	(no register - Transparent to LSP_0)
TRANSPARENT1	A1	1010 0001	(no register - Transparent to LSP_1)
TRANSPARENT2	A2	1010 0010	(no register - Transparent to LSP_2)
TRANSPARENT3	A3	1010 0011	(no register - Transparent to LSP_3)
TRANSPARENT4	A4	1010 0100	(no register - Transparent to LSP_4)
TRANSPARENT5	A5	1010 0101	(no register - Transparent to LSP_5)
TRANSPARENT6	A6	1010 0110	(no register - Transparent to LSP_6)
$SGPIO_0$	B8	1011 1000	Shared GPIO $Register_0$
$SGPIO_1$	B9	1011 1001	Shared GPIO $Register_1$
$SGPIO_2$	BA	1011 1010	Shared GPIO $Register_2$
$SGPIO_3$	BB	1011 1011	Shared GPIO $Register_3$
$SGPIO_4$	BC	1011 1100	Shared GPIO $Register_4$
$SGPIO_5$	BD	1011 1101	Shared GPIO $Register_5$
$SGPIO_6$	BE	1011 1110	Shared GPIO $Register_6$
CONTROLSEL	87	1000 0111	Control Select Register
LSPSEL	86	1000 0110	LSP Select Register
TRANSPARENTENABLE	A8	1010 1000	(no register - Transparent to selected LSPs)
TESTMODE	37	0011 0111	Used for factory test mode only
Other Undefined	TBD	TBD	Device Identification Register

Note 2: All other instructions act on selected 'STA112s only.

Level 2 Protocol (Continued)

LEVEL 2 INSTRUCTON DESCRIPTIONS

BYPASS: The *BYPASS* instruction selects the bypass register for insertion into the active scan chain when the 'STA112 is selected.

EXTEST: The *EXTEST* instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of the sample only shift cells connected to pins as described in the 'STA112 BSDL file. The BSDL can be found on our website at http://www.national.com/scan. Note that cell 0 (S_0) is located closest to TDO_B. On the 'STA112, the *EXTEST* instruction performs the same function as the *SAMPLE/PRELOAD* instruction, since there aren't any scannable outputs on the device.

SAMPLE/PRELOAD: The *SAMPLE/PRELOAD* instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of the sample only shift cells connected to pins as described in the 'STA112 BSDL file. The BSDL can be found on our website at http://www.national.com/scan. Note that cell 0 (S_0) is located closest to TDO_B.

IDCODE: The *IDCODE* instruction selects the device identification register for insertion into the active scan chain. When *IDCODE* is the current active instruction the device identification 0FC2501F Hex is captured upon exiting the *Capture-DR* state.

UNPARK: This instruction unparks the Local Scan Port Network and inserts it into the active scan chain as configured by Mode $Register_0$ and Mode $Register_1$ (see *Table 8*). Unparked LSPs are sequenced synchronously with the 'STA112's TAP controller. When an LSP has been parked in the *Test-Logic-Reset* or *Run-Test/Idle* state, it will not become unparked until the 'STA112's TAP Controller enters the *Run-Test/Idle* state following the *UNPARK* instruction. An LSP which has been parked in *Test-Logic-Reset* will be parked in *Run-Test/Idle* upon update of an *UNPARK* instruction. If an LSP has been parked in one of the stable pause states (*Pause-DR* or *Pause-IR*), it will not become unparked until the 'STA112's TAP Controller enters the respective pause state. (See *Figure 8*, *Figure 9*, *Figure 10*, and *Figure 11*).

PARKTLR: This instruction causes all unparked LSPs to be parked in the *Test-Logic-Reset* TAP controller state and removes the LSP network from the active scan chain. The LSP controllers keep the LSPs parked in the *Test-Logic-Reset* state by forcing their respective TMS_n output with a constant logic "1" while the LSP controller is in the *Parked-TLR* state (see *Figure 3*).

PARKRTI: This instruction causes all unparked LSPs to be parked in the *Run-Test/Idle* state. The update of the *PARKRTI* instruction MUST immediately be followed by a TMS_B=0 (to enter the *RTI* state) in order to assure stability. When a LSP_n is active (unparked), its TMS_n signals follow TMS_B and the LSP_n controller state transitions are synchronized with the TAP Controller state transitions of the 'STA112. When the instruction register is updated with the *PARKRTI* instruction, TMS_n will be forced to a constant logic 0, causing the unparked local TAP Controllers to be parked in the *Run-Test/Idle* state. When an LSP_n is parked, it is removed from the active scan chain.

PARKPAUSE: The *PARKPAUSE* instruction has dual functionality. It can be used to park unparked LSPs or to unpark parked LSPs. The instruction places all unparked LSPs in one of the TAP Controller pause states. A local port does not become parked until the 'STA112's TAP Controller is sequenced through *Exit1-DR/IR* into the *Update-DR/IR* state. When the 'STA112 TAP Controller is in the *Exit1-DR* or *Exit1-IR* state and TMSB is high, the LSP controller forces a constant logic "0" onto TMSL thereby parking the port in the *Pause-DR* or *Pause-IR* state respectively (see *Figure 3*). Another instruction can then be loaded to reconfigure the local ports or to deselect the 'STA112 (i.e., *MODESEL*, *GOTOWAIT*, etc.).

If the *PARKPAUSE* instruction is given to an 'STA112 whose LSPs are parked in *Pause-IR* or *Pause-DR*, the parked LSPs will become unparked when the 'STA112's TAP controller is sequenced into the respective Pause state.

The *PARKPAUSE* instruction was implemented with this dual functionality to enable backplane testing (interconnect testing between boards) with simultaneous Updates and Captures.

Simultaneous Update and Capture of several boards can be performed by parking LSPs of the different boards in the *Pause-DR* TAP controller state, after shifting the data to be updated into the boundary registers of the components on each board. The broadcast address is used to select all 'STA112s connected to the backplane. The *PARKPAUSE* instruction is scanned into the selected 'STA112s and the 'STA112 TAP controllers are sequenced to the *Pause-DR* state where the LSPs of all 'STA112s become unparked. The local TAP controllers are then sequenced through the *Update-DR*, *Select-DR*, *Capture-DR*, *Exit1-DR*, and parked in the *Pause-DR* state, as the 'STA112 TAP controller is sequenced into the *Update-DR* state. When an LSP is parked, it is removed from the active scan chain.

GOTOWAIT: This instruction is used to return all 'STA112s to the *Wait-For-Address* state. All unparked LSPs will be parked in the *Test-Logic-Reset* TAP controller state (see *Figure 4*).

$MODESEL_n$: The $MODESEL_n$ instruction inserts Mode $Register_n$ into the active scan chain.

MCGRSEL: This instruction inserts the multicast group register (MCGR) into the active scan chain. The MCGR is used to group 'STA112s into multicast groups for parallel TAP sequencing (i.e., to simultaneously perform identical scan operations).

SOFTRESET: This instruction causes all 7 Port configuration controllers (see *Figure 3*) to enter the *Parked-TLR* state, which forces TMS_n high; this parks each local port in the *Test-Logic-Reset* state within 5 TCK_B cycles.

LFSRSEL: This instruction inserts the linear feedback shift register (LFSR) into the active scan chain, allowing a compacted signature to be shifted out of the LFSR during the *Shift-DR* state. (The signature is assumed to have been computed during earlier *LFSRON* shift operations.) This instruction disables the LFSR register's feedback circuitry, turning the LFSR into a standard 16-bit shift register. This allows a signature to be shifted out of the register, or a seed value to be shifted into it.

LFSRON: Once this instruction is executed, the linear feedback shift register samples data from the active scan path (including all unparked TDI_n) during the *Shift-DR* state. Data from the scan path is shifted into the linear feedback shift register and compacted. This allows a serial stream of data to be compressed into a 16-bit signature that can subse-

Level 2 Protocol (Continued)

quently be shifted out using the *LFSRSEL* instruction. The linear feedback shift register is not placed in the scan chain during this mode. Instead, the register samples the active scan-chain data as it flows from the LSPN to TDO_B.

LFSROFF: This instruction terminates linear feedback shift register sampling. The LFSR retains its current state after receiving this instruction.

CNTRSEL: This instruction inserts the 32-bit TCK counter shift register into the active scan chain. This allows the user to program the number of n TCK cycles to send to the parked local ports once the *CNTRON* instruction is issued (e.g., for BIST operations). Note that to ensure completion of count-down, the 'STA112 should receive at least n TCK_B pulses.

CNTRON: This instruction enables the TCK counter. The counter begins counting down on the first rising edge of TCK_B following the *Update-IR* TAP controller state and is decremented on each rising edge of TCK_B thereafter. When the TCK counter reaches terminal count, 00000000 Hex, TCK_n of all parked LSP's is held low. This function overrides Mode $Register_0$ TCK control bit (bit-3).

If the *CNTRON* instruction is issued when the TCK counter is 00000000 (terminal count) the local TCKs of parked LSPs will be gated. The counter will begin counting on the rising edge of TCK_B when the TCK counter is loaded with a non-zero value following a *CNTRSEL* instruction (see BIST Support in Special Features section for an example).

CNTROFF: This instruction disables the TCK counter, and TCK_n control is returned to Mode $Register_0$ (bit-3).

DEFAULT_BYPASS: This instruction selects the Bypass register to be the default for 'STA112 commands that do not explicitly require a data register. The default after RESET is the Device ID register.

CONTROLSEL: This instruction inserts the Control Register into the active scan chain. Caution should be used when writing to this register. Changing the value of the MPSel bit will result in the reconfiguration of the Master port and thus the tester will loose control of the bridge. Also, The TMS, TCK, and $\overline{TRST}$ pins connected to the tester change directions and will result in bus contention.

LSPSEL: This instruction inserts the LSP SELECT register into the active scan chain.

TRANSPARENTENABLE: This instruction is only available when the 'STA112 is in ScanBridge mode. It is used along with the contents of Mode $Register_0$ and Mode $Register_1$ to place the selected LSPs into the scan chain without ScanBridge registers or pad-bits (transparent mode).

$TRANSPARENT_n$: These instructions are only available when the 'STA112 is in ScanBridge mode. They are used to select the respective LSP_n, and place it alone into the transparent mode, which removes all STA112 registers and pad bits from the scan chain and inserts LSP_n.

TESTMODE: This Instruction places the 'STA112 into production scan test-mode. This instruction is reserved and should not be used in system.

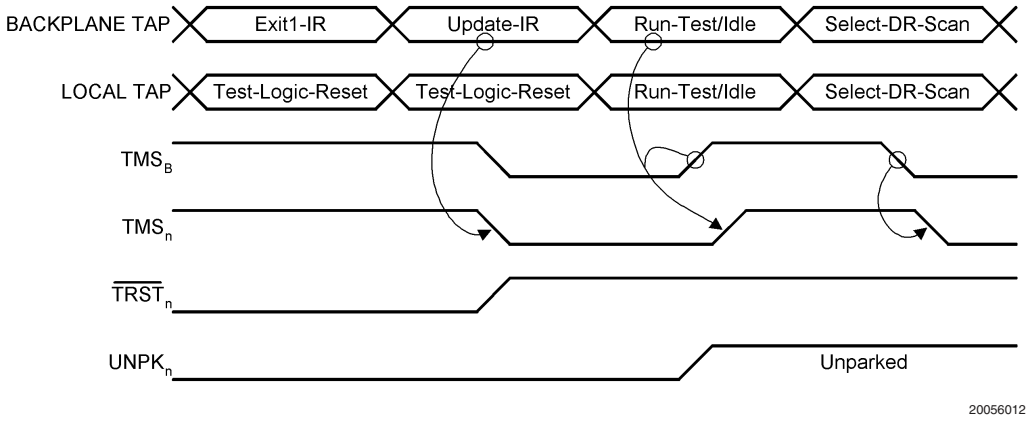

FIGURE 8. Local Scan Port Synchronization from Parked-TLR State

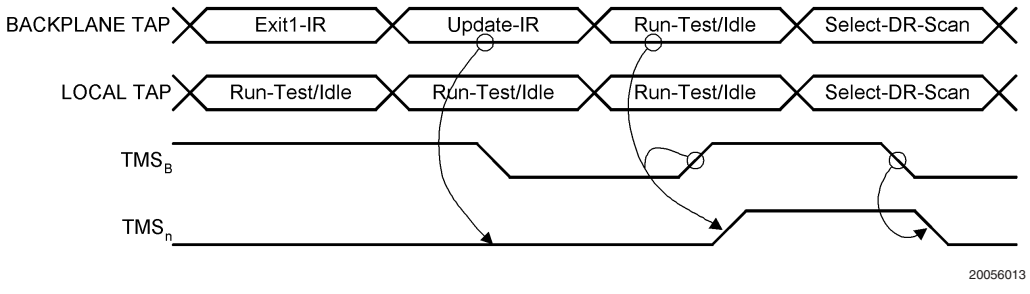

FIGURE 9. Local Scan Port Synchronization from Parked-RTI State

Register Descriptions

INSTRUCTION REGISTER: The instruction shift register is an 8-bit register that is in series with the scan chain whenever the TAP Controller of the 'STA112 is in the *Shift-IR* state. Upon exiting the *Capture-IR* state, the value XXXXXX01 is captured into the instruction register, where XXXXXX represents the value on the $S_{(0-5)}$ inputs. When the 'STA112 controller is in the *Wait-For-Address* state, the instruction register is used for 'STA112 selection via address matching. In addressing individual 'STA112s, the chip's addressing logic performs a comparison between a statically-configured (hard-wired) value on that 'STA112's slot inputs, and an address which is scanned into the chip's instruction register.

Binary address codes 00000000 through 00111010 and 01000000 through 11111111 (00 through 39, and 40 to FF Hex) are reserved for addressing individual 'STA112s. Addresses 3A Hex through 3F Hex are reserved for Interrogation and Broadcast modes.

During multi-cast (group) addressing, a scanned-in address is compared against the (previously scanned-in) contents of a 'STA112's Multi-Cast Group register. Binary address codes 00111110 through 00111111 (3A through 3F Hex) are reserved for multi-cast addressing, and should not be assigned as 'STA112 slot-input values.

Furthermore, address 00000000 should be avoided if Address Interrogation may be used.

BOUNDARY-SCAN REGISTER: The boundary-scan register is a sample only shift register containing cells from all the inputs. The register allows testing of circuitry external to the 'STA112. It permits the signals flowing between the system pins to be sampled and examined without interfering with the operation of the on-chip system logic.

The scan chain is arranged as described in the BSDL file located on our website at http://www.national.com/scan. Note that cell 0 (S_0) is located closest to TDO_B.

BYPASS REGISTER: The bypass register is a 1-bit register that operates as specified in IEEE Std. 1149.1 once the 'STA112 has been selected. The register provides a minimum length serial path for the movement of test data between TDI_B and the LSP. This path can be selected when no other test data register needs to be accessed during a board-level test operation. Use of the bypass register shortens the serial access-path to test data registers located in other components on a board-level test data path.

MULTI-CAST GROUP REGISTER: Multi-cast is a method of simultaneously communicating with more than one selected 'STA112. The multi-cast group register (MCGR) is a 2-bit register used to determine which multi-cast group a particular 'STA112 is assigned to. Four addresses are reserved for multi-cast addressing. When an 'STA112 is in the *Wait-For-Address* state and receives a multi-cast address, and if that 'STA112's MCGR contains a matching value for that multi-cast address, the 'STA112 becomes selected and is ready to receive Level 2 Protocol (i.e., further instructions).

The MCGR is initialized to 00 upon entering the *Test-Logic-Reset* state.

TABLE 7. Multi-Cast Group Register Addressing

MCGR Bits 1,0	Hex Address	Binary Address
00	3C	00111100
01	3D	00111101
10	3E	00111110
11	3F	00111111

The following actions are used to perform multi-cast addressing:

1. Assign all target 'STA112s to a multi-cast group by writing each individual target 'STA112's MCGR with the same multi-cast group code (see *Table 7*). This configuration step must be done by individually addressing each target 'STA112, using that chip's assigned slot value.
2. Scan out the multi-cast group address through the TDI_B input of all 'STA112s. Note that this occurs in parallel, resulting in the selection of only those 'STA112s whose MCGR was previously programmed with the matching multi-cast group code.

MODE REGISTER$_0$: Mode Register$_0$ is an 8-bit data register used primarily to configure the Local Scan Port Network. Mode Register$_0$ is initialized to 00000001 binary upon entering the *Test-Logic-Reset* state. Bits 0, 1, 2, and 4 are used for scan chain configuration as described in *Table 8*. When the *UNPARK* instruction is executed, the scan chain configuration will be as shown in *Table 8* below. When all LSPs are parked, the scan chain configuration will be $TDI_B \rightarrow$ 'STA112-register $\rightarrow TDO_B$. Bit 3 is used for TCK_n configuration, see *Table 9*.

Register Descriptions (Continued)

TABLE 8. Mode Register Control of LSPN

Mode Register(s)	Scan Chain Configuration (if unparked)
MR0: X000X000 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow TDO_B$
MR0: X000X001 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X010 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X011 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X100 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X101 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X110 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X111 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X010X000 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X010X001 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X010X010 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X010X011 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X010X100 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
...	...
MR0: X110X111 MR1: XXXXX000	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow LSP_4 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X000 MR1: XXXXX001	$TDI_B \rightarrow$ Register $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X001 MR1: XXXXX001	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X010 MR1: XXXXX001	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$
...	...
MR0: X110X111 MR1: XXXXX001	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow LSP_4 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: X000X000 MR1: XXXXX010	$TDI_B \rightarrow$ Register $\rightarrow LSP_6 \rightarrow$ PAD $\rightarrow TDO_B$
...	...
MR0: X110X111 MR1: XXXXX111	$TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow LSP_4 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow LSP_6 \rightarrow$ PAD $\rightarrow TDO_B$
MR0: XXX1XXXX MR1: XXXXXXXX	$TDI_B \rightarrow$ Register $\rightarrow TDO_B$ (Loopback)

Note 3: In this device with 7 LSPs, there are 2^7 possible LSP configurations: no LSPs, each individual LSP, and combinations of 2 to 7 LSPs.

Register Descriptions (Continued)

TABLE 9. Test Clock Configuration

Bit 3	LSP n	TCK n
1	Parked	Stopped
0	Parked	Free-running
1	Unparked	Free-running
0	Unparked	Free-running
X	Parked-TLR	Stopped after 512 clock pulses

Bit 3 is normally set to logic "0" so that TCK_n is free-running when the local scan ports are parked in the *Parked-RTI*, *Parked-Pause-DR* or *Parked-Pause-IR* state. When the local ports are parked, bit 3 can be programmed with logic "1", forcing all of the LSP TCK_n's to stop. This feature can be used in power sensitive applications to reduce the power consumed by the test circuitry in parts of the system that are not under test. When in the *Parked-TLR* state, TCK_n is gated (stopped) after 512 clock pulses have been received on TCK_B independent of the bit 3 value.

Bit 7 is a status bit for the TCK counter. Bit 7 is only set (logic "1") when the TCK counter is on and has reached terminal count (zero). It is cleared (logic "0") when the counter is loaded following a *CNTRSEL* instruction. The power-on value for bit 7 is "0".

TABLE 10. Mode Register Bits (Note 4)

Bit	Mode Register$_0$	Mode Register$_1$	Mode Register$_2$
0	LSP_0	LSP_5	$LSP_0/GPIO_0$
1	LSP_1	LSP_6	$LSP_1/GPIO_1$
2	LSP_2	Reserved	$LSP_2/GPIO_2$
3	TCK Free Run Disable (*Table 9*)	Reserved	$LSP_3/GPIO_3$
4	TDI_B to TDO_B Loopback	Reserved	$LSP_4/GPIO_4$
5	LSP_3	Reserved	$LSP_5/GPIO_5$
6	LSP_4	Reserved	$LSP_6/GPIO_6$
7	TCK Counter Status	Reserved	Reserved

Note 4: The default value for all of the mode register bits is "0" - except for bit 0 of Mode Register$_0$ which is "1"

MODE REGISTER$_1$: Bits 0 and 1 function similarly to Mode Register$_0$, but apply as shown in *Table 10*.

MODE REGISTER$_2$: The 8 bit Mode Register$_2$ is described in *Table 10*, and selects which of the LSPs will be put in the shared GPIO mode (and thus further controlled by the $SGPIO_n$ Register)

SHARED $GPIO_n$ REGISTER: There are seven (7) GPIO registers, one for each LSP. Each 8 bit register controls the function of the TMS, TDO, and TDI pins as shown in *Table 11* when the Mode Register$_2$ activates the respective LSP.

TABLE 11. Shared GPIO Register Bits (Note 5)

Bit	SGPIO Register$_n$
0	Output (TMS)
1	Output (TDO)
2	Input (TDI)
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved

Note 5: The default value for all of the Shared GPIO register bits is "0".

DEVICE IDENTIFICATION REGISTER: The device identification register (IDREG) is a 32-bit register compliant with IEEE Std. 1149.1. When the *IDCODE* instruction is active, the identification register is loaded with the Hex value upon leaving the *Capture-DR* state (on the rising edge of the TCK_B). Refer to our currently available BSDL file on our website for the most accurate Device ID.

LINEAR FEEDBACK SHIFT REGISTER: The 'STA112 contains a signature compactor which supports test result evaluation in a multi-chain environment. The signature compactor consists of a 16-bit linear-feedback shift register (LFSR) which can monitor local-port scan data as it is shifted upstream from the 'STA112's local-port network. Once the LFSR is enabled, the LFSR's state changes in a reproducible way as each local-port data bit is shifted in from the local-port network. When all local-port data has been scanned in, the LFSR contains a 16-bit signature value which can be compared against a signature computed for the expected results vector.

The LFSR uses the following feedback polynomial:

$F(x) = X^{16} + X^{12} + X^3 + X + 1$

This signature compactor is used to compress serial data shifted in from the local scan chain, into a 16-bit signature. This signature can then be shifted out for comparison with an expected value. This allows users to test long scan chains in parallel, via Broadcast or Multi-Cast addressing modes, and check only the 16-bit signatures from each module. The LFSR is initialized with a value of 0000 Hex upon reset.

32-BIT TCK COUNTER REGISTER: The 32-bit TCK counter register enables BIST testing that requires n TCK cycles, to be run on a parked LSP while another 'STA112 port is being tested. The *CNTRSEL* instruction can be used to load a count-down value into the counter register via the active scan chain. When the counter is enabled (via the *CNTRON* instruction), and the LSP is parked, the local TCKs will stop and be held low when terminal count is reached.

The TCK counter is initialized with a value of 00000000 Hex upon reset.

CONTROL REGISTER: The Control Register consists of 8 bits as shown in *Table 12*. All bits are initialized at power-up, $\overline{\text{RESET}}$ and a $\overline{\text{TRST}}$ reset (if the IgnoreReset bit in the Control Register is set to a logic "0"). Five of the bits are

Register Descriptions (Continued)

initialized by values on external pins, the last bit, the IgnoreReset, has a default value of "0". The user can overwrite this register via the ControlSel Instruction.

Caution should be used when writing to this register. Changing the value of the MPSel bit will result in the reconfiguration of the Master port and thus the tester will lose control of the bridge. Also, The TMS, TCK, and $\overline{TRST}$ pins connected to the tester change directions and will result in bus contention.

TABLE 12. Control Register

Bit	Function	Default Value
0	IgnoreReset	0
1	TRANS	External Pin
2	SB/$\overline{S}$	External Pin
3	$MPsel_{B1/\overline{B0}}$	External Pin
4	TLR_TRST	External Pin
5	TLR_TRST_6	External Pin
6	Future Expansion	0
7	Future Expansion	0

LSP SELECT REGISTER: The LSPSEL register consists of 8 bits with the MSB set to a logic "0". The value of this register will be initialized during a RESET reset and a $\overline{TRST}$ reset (if the IgnoreReset bit in the Control Register is set to a logic "0") based on the value of the $LSPSel_{(0-6)}$ pins. if $LSPsel_n$ = "1" then LSP_n will be included in the scan chain.

The contents of this register are used to determine which of the LSPs are to be stitched together in stitcher mode. The value of this register can be modified allowing the chain configuration to be modified. In ScanBridge mode this register has no affect on the LSP configuration.

BOUNDARY REGISTER: The boundary register for the 'STA112 is defined as follows: {tlr_trst_6, tlr_trst, sb/s, mpsel, trans, addmask, lspsel, oe_n, slot}. All of these bits are inputs to the 'STA112, therefore *EXTEST* will act the same as the *SAMPLE* instruction.

TRANSPR(n): NOTE: There are NO registers associated with this set of instructions as the ScanBridge becomes transparent.

Special Features

TRANSPARENT MODE

While this mode is activated, the selected LSP n ports will follow the backplane ports. $\overline{TRST}_n$ will be a buffered version of $\overline{TRST}_B$, TCK_n will be a buffered version of TCK_B, TMS_n will be a buffered version of TMS_B, TDO_n will be a buffered version of TDI_B and TDO_B will be a buffer version of TDI_n. $TRIST_B$ and $TRIST_n$ will be asserted when the state machine is in either the *Shift-DR* or *Shift-IR* states. The unselected LSPs will be placed in the *PARKTLR* state, and their clocks will be gated after 512 TCK_B clock cycles.

Transparent Mode will be controlled by 8 new instructions, *TRANSPARENT0* through *TRANSPARENT7*. Transparent Mode will override any other active mode. When one of the transparent mode instructions is shifted into the instruction register and the tap controller goes through the *UPDATE-IR* state, $\overline{TRST}_n$ will go high, and TMS_n will go low. This will force the targets connected to the LSP_n ports to go into the *RTI* state. Then as the 'STA112 state machine goes into the *RTI* state, all of the LSP_n signals will follow the back-plane signals. This is identical to the method that is typically used to unpark an LSP. The 'STA112 will remain in this mode until a $\overline{TRST}_B$ is asserted or a power cycle forces a reset. Once in the Transparent Mode, the 'STA112 will not be able to be reset by a 5 TMS high reset.

The sequence of operations to use Transparent Mode on an LSP are as follows (example uses LSP_0):

1. IR-Scan the 'STA112 address into the instruction register (address a 'STA112).
2. IR-Scan the *TRANSPARENT0* instruction to enable Transparent Mode on LSP_0. Transparent Mode will be enabled when the TAP enters the *RTI* state at the end of this shift operation ($\overline{TRST}_0$, TDO_0, TMS_0 and TCK_0 become buffered versions of $\overline{TRST}_B$, TDI_B, TMS_B and TCK_B and TDO_B becomes a buffered version of TDI_0).

NOTE: Transparent Mode will persist until the 'STA112 is reset using $\overline{TRST}_B$. The *GOTOWAIT* and *SOFTRESET* instructions will not work in this mode.

MASTER PORT SELECTION

The 'STA112 has the capability to use one of two Master Ports - either the backplane B_0 port, or the port on LSP_0. This feature is useful to allow an alternate test master to take control of the scan chains.

Selection of the master port is accomplished by using the master port select pin, $MPsel_{B0/\overline{B1}}$.

To accomodate the change in position of the master port boundary scan cells, there are two BSDL files available on the website to support both modes.

Changing the state of the $MPsel_{B0/\overline{B1}}$ input without a reset is an undefined operation.

The TAP port which is NOT selected as the Master Port will assume the function of LSP_0.

STITCHER MODE

When the pin SB/$\overline{S}$ (ScanBridge/not-Stitcher) is held Low, the 'STA112 enters the Stitcher mode of operation (see Switching Between Modes of Operation). The LSPs which will be stitched together are determined by the contents of the LSPSEL Register, which becomes initialized at power-up, reset, or $\overline{TRST}_{Bn}$ to be equal to the value on the pins $LSPsel_{(0-6)}$. Configurations other than what is indicated by the $LSPsel_{(0-6)}$ pins are possible by altering the value of the LSPSEL Register, which is accessed by using the *LSPSEL* Instruction while the 'STA112 is in ScanBridge mode.

BIST SUPPORT

The sequence of instructions to run BIST testing on a parked 'STA112 port is as follows:

1. Pre-load the Boundary register of the device under test if needed.
2. Issue the *CNTRSEL* instruction and initialize (load) the TCK counter to 00000000 Hex. Note that the TCK counter is initialized to 00000000 Hex upon *Test-Logic-Reset*, so this step may not be necessary.
3. Issue the *CNTRON* instruction to the 'STA112, to enable the TCK counter.

Special Features (Continued)

4. Shift the *PARKRTI* instruction into the 'STA112 instruction register and *BIST* instruction into the instruction register of the device under test. With the counter on (at terminal count) and the LSP parked, the local TCK will be gated.
5. Issue the *CNTRSEL* instruction to the 'STA112.
6. Load the TCK counter (Shift the 32-bit value representing the number of TCK_n cycles needed to execute the BIST operation into the TCK counter register). The Self test will begin on the rising edge of TCK_B following the *Update-DR* TAP controller state.
7. Bit 7 of Mode $Register_0$ can be scanned to check the status of the TCK counter, (*MODESEL* instruction followed by a *Shift-DR*). Bit 7 logic "0" means the counter has not reached terminal count, logic "1" means that the counter has reached terminal count and the BIST operation has completed.
8. Execute the *CNTROFF* instruction.
9. Unpark the LSP and scan out the result of the BIST operation

RESET

Reset operations can be performed at three levels. The highest level resets all 'STA112 registers and all of the local scan chains of selected and unselected 'STA112s. This Level 1 reset is performed whenever the 'STA112 TAP Controller enters the *Test-Logic-Reset* state. *Test-Logic-Reset* can be entered synchronously by forcing TMS_B high for at least five (5) TCK_B pulses, or asynchronously by asserting the $TRST_B$ pin. A Level 1 reset forces all 'STA112s into the *Wait-For-Address* state, parks all local scan chains in the *Test-Logic-Reset* state, and initializes all 'STA112 registers.

The *SOFTRESET* instruction is provided to perform a Level 2 reset of all LSP's of selected 'STA112s. *SOFTRESET* forces all TMS_n signals high, placing the corresponding local TAP Controllers in the *Test-Logic-Reset* state within five (5) TCK_B cycles.

The third level of reset is the resetting of individual local ports. An individual LSP can be reset by parking the port in the *Test-Logic-Reset* state via the *PARKTLR* instruction. To reset an individual LSP that is parked in one of the other parked states, the LSP must first be unparked via the *UNPARK* instruction.

PORT SYNCHRONIZATION

When an LSP is not being accessed, it is placed in one of the four TAP Controller states: *Test-Logic-Reset*, *Run-Test/Idle*, *Pause-DR*, or *Pause-IR*. The 'STA112 is able to park a local chain by controlling the local Test Mode Select outputs ($TMS_{(0-2)}$) (see *Figure 3*). TMS_n is forced high for parking in the *Test-Logic-Reset* state, and forced low for parking in *Run-Test/Idle*, *Pause-IR*, or *Pause-DR* states. Local chain access is achieved by issuing the *UNPARK* instruction. The LSPs do not become unparked until the 'STA112 TAP Controller is sequenced through a specified synchronization state. Synchronization occurs in the *Run-Test/Idle* state for LSPs parked in *Test-Logic-Reset* or *Run-Test/Idle*; and in the *Pause-DR* or *Pause-IR* state for ports parked in *Pause-DR* or *Pause-IR*, respectively.

Figure 10 and *Figure 11* show the waveforms for synchronization of a local chain that was parked in the *Test-Logic-Reset* state. Once the *UNPARK* instruction is received in the instruction register, the LSPC forces TMS_n low on the falling edge of TCK_B .

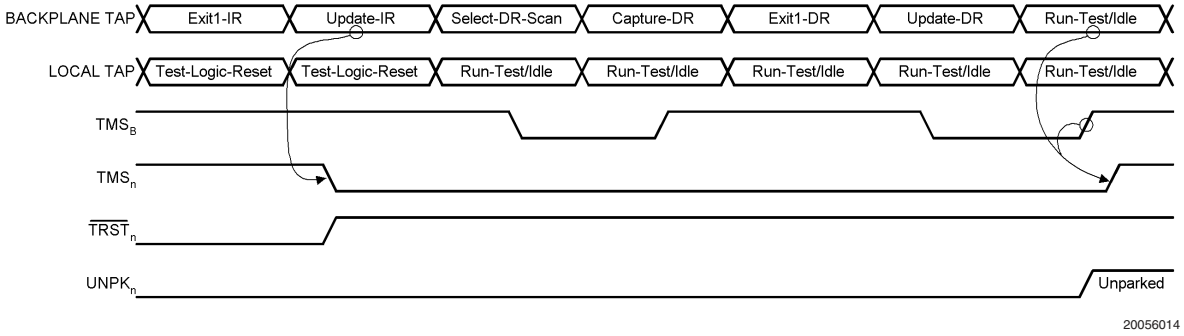

FIGURE 10. Local Scan Port Synchronization on Second Pass

Special Features (Continued)

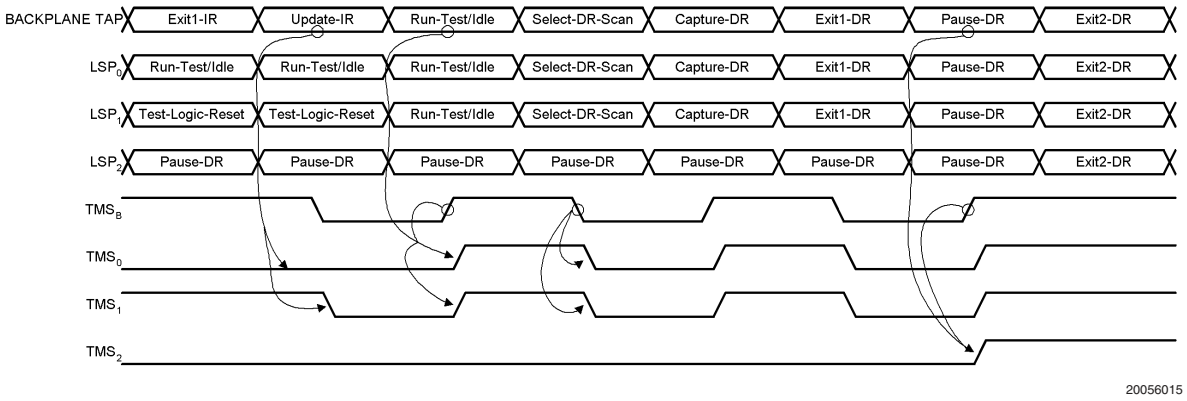

FIGURE 11. Synchronization of the Three Local Scan Ports

This moves the local chain TAP Controllers to the synchronization state (*Run-Test/Idle*), where they stay until synchronization occurs. If the next state of the 'STA112 TAP Controller is *Run-Test/Idle*, TMS_n is connected to TMS_B and the local TAP Controllers are synchronized to the 'STA112 TAP Controller as shown in *Figure 11*. If the next state after *Update-IR* were *Select-DR*, TMS_n would remain low and synchronization would not occur until the 'STA112 TAP Controller entered the *Run-Test/Idle* state, as shown in *Figure 10*.

Each local port has its own Local Scan Port Controller. This is necessary because the LSP's can be configured in any one of 128 (2^7) possible combinations. Either one, some, or all of the local ports can be accessed simultaneously. Configuring the LSP is accomplished with Mode $Register_0$ and Mode $Register_1$, in conjunction with the *UNPARK* instruction.

The LSP's can be unparked in one of 128 different configurations. Using multiple ports presents not only the task of synchronizing the 'STA112 TAP Controller with the TAP Controllers of an individual local port, but also of synchronizing the individual local ports to one another.

When multiple local ports are selected for access, it is possible that two ports are parked in different states. This could occur when previous operations accessed the two ports separately and parked them in the two different states. The LSP Controllers handle this situation gracefully. *Figure 11* shows the *UNPARK* instruction being used to access LSP_0, LSP_1, and LSP_2 in series (Mode $Register_0$ = XXX0X111 binary). LSP_0 and LSP_1 become active as the 'STA112 controller is sequenced through the *Run-Test/Idle* state. LSP_2 remains parked in the *Pause-DR* state until the 'STA112 TAP Controller is sequenced through the *Pause-DR* state. At that point, all the local ports are synchronized for access via the active scan chain.

KNOWN POWER-UP STATE

Refer to the various operating modes for descriptions of the resets.

TRST

$\overline{TRST}_B$: Assertion of $\overline{TRST}_B$ will return the device back to its known power-up state.

$\overline{TRST}_n$: $\overline{TRST}_n$ is an output on the LSP side of the 'STA112. While the LSP state-machine (level 2 protocol) is in the *Parked-TLR* state the $\overline{TRST}_n$ pin will be driven low. In all other states the $\overline{TRST}_n$ pin will be driven high.

PHYSICAL LAYER CHANGES

TRIST for TDO_B and TDO_n are signals for enabling an external buffer circuit between the 'STA112 and the backplane/LSP. This would allow, for example, a CMOS-to-LVDS converter to drive an LVDS JTAG backplane test bus. These signals are always driving. A seperate TRIST is provided for the Backplane TAP port and for LSP_0, LSP_2, and LSP_3 (only), to report a TRI-STATE on TDO when the LSP is not in a shift state.

PASS-THROUGH PINS

LSP_0, LSP_1, and the Backplane port have two pass-through pins. The pair of pass-through pins will consist of an input (A_n) and an output (Y_n). The LSP pass-through output (Y_n) will drive the level being received by the backplane pass-through input (A_B). Conversly, the level on the LSP pass-through input (A_n) will be driven on the backplane pass-through output (Y_B).

The Pass-through pins are available only when a single LSP is selected. For each LSP these pins will be enabled when the level 2 protocol state-machine is not in the *Parked-TLR* state. When not enabled they will be TRI-STATED.

LSP GATING

While the LSP_n state-machine (level 2 protocol) is in the *Parked-TLR* state, the four LSP_n signals shall be controlled as shown in *Table 13*. Upon entry into the *Parked-TLR* state (*power-up*, *reset*, *PARKTLR* or *GOTOWAIT*) a counter in the LSP_n state-machine allows 512 TCK_B clock pulses to occur on TCK_n before gating. Once gated, TCK_n will drive a logic "0".

Letting 512 TCK_B pulses pass through to TCK_n allows a five high TMS reset to occur on over 100 levels of hierarchy before the 'STA112 gates TCK_n (for power saving in a free-running clock system).

Special Features (Continued)

TABLE 13. Gated LSP Drive States

LSP Connection	Drive State
TDO_n	Pull-up resistor to provide a weak HIGH
TMS_n	Pull-up resistor to provide a weak HIGH
TDI_n	Pull-up resistor to provide a weak HIGH
TCK_n	TCK_B for 512 pulses, then gated LOW

The 'STA112 does not require that any clock pulses are received on TCK_B while in the *Parked-TLR* state.

Setting Bit 3 of Mode $Register_0$ to 1 gates TCK_n when in the *Parked-RTI*, *Parked-Pause-DR* and *Parked-Pause-IR* states. Default is free-running (bit 3 = 0). The value stored in bit 3 of Mode $Register_0$ does not effect the requirement of 512 clock pulses before gating TCK_n in the *Parked-TLR* state. (See section on Mode $Register_0$).

GPIO CONNECTIONS

General Purpose I/O (GPIO) pins are registered inputs and outputs. The GPIO's used in the 'STA112 are described below.

LSP SHARED: In the shared mode of operation, the 1149.1 LSP pins TDI_n, TDO_n and TMS_n pins become GPIO pins. TMS_n and TDO_n will be outputs, TDI_n will be an input in the GPIO mode.

The sequence of operations to use shared GPIOs on an LSP are as follows (example uses LSP_0):

1. IR-Scan the 'STA112 address into the instruction register (address a 'STA112).
2. IR-Scan the *MODESEL*$_3$ instruction into the instruction register to select Mode $Register_3$ (Shared GPIO configuration register) as the data register.
3. DR-Scan 00000001 into Mode $Register_3$ to enable GPIOs on LSP_0. The GPIOs will be enabled when the TAP enters the *RTI* state at the end of this shift operation (TDO_0 and TMS_0 will be forced to logic "0" as defined by the default value in the Shared GPIO $Register_0$).
4. IR-Scan the *SGPIO*$_0$ instruction into the instruction register to select the Shared GPIO $Register_0$ as the data register.
5. DR-Scan 00000011 into the Shared GPIO $Register_0$ to set TDO_0 and TMS_0 to a logic "1" (when TAP enters *Update-DR*). During this operation, when the TAP enters *Capture-DR*, the present value on the TDI_0 pin and the values of TDO_0 and TMS_0 (as set by Shared GPIO $Register_0$) will be captured into bits 2, 1 and 0 of the shift register and will be scanned out 00000X00 (X = value present on TDI_0 when TAP enters *Capture-DR*).
6. Step 5 can be repeated to generate waveforms on TDO_0 and TMS_0. If step 5 was repeated with 00000000 as data, TDO_0 and TMS_0 would be set to a logic "0" (when TAP state = *Update-DR*) and 00000X11 would be scanned out (X = value present on TDI_0 when TAP enters *Capture-DR*).
7. IR-Scan the *GOTOWAIT* or *SOFTRESET* instruction, or generate a $\overline{TRST}_B$ reset to disable the GPIOs.

ADDRESS MASK

This feature masks S_5-S_0 and allows the 'STA112 to respond to an address on pins S_7-S_6 only. For example if ADDMASK is deasserted, a 'STA112's address could be 73H. With ADDMASK asserted, the same 'STA112 would respond to an address range of 40H-7FH. This feature is used when a local controller utilizes one address space and a remote tester uses a second address space. This feature enables identical cards with local controllers to contain vectors that utilize the same address space. Once an external tester is connected and AddressMask is deasserted the card then have unique address. This feature requires additional bus control logic.

The Broadcast, Multicast, and Interrogate addresses are reserved and still recognized when an address mask is used.

ADDRESS INTERROGATION

The 'STA112 has four states that it can go to from the *Wait-For-Address* state: *Unselected*, *Singularly-selected*, *Multi/Broadcast-selected*, and *Address-interrogation* (see *Figure 12*).

After a reset (or *GOTOWAIT* command) has been issued, the 'STA112 TAP is sequenced to the *Capture-IR* state where XXXXXX01 is loaded into the shift register. Upon entering the *Shift-IR* state, the instruction register is filled with the address interrogation value (3A hex) which is loaded into the address register as the TAP is sequenced into the *Update-IR* state. On the next loop through *Capture-IR* the shift register is loaded with the ones-complement of the slot address. In the *Shift-IR* state the address interrogation value is loaded into the instruction register. The value presented on TDO_B will be a wired-and address of all of the 'STA112s on the bus. As this value is being shifted out, each 'STA112 will monitor its TDO_B to see if it is receiving the same value it is driving. If the device shifts all bits of its ones-complement address and never gets a compare error it will tri-state TDO_B and go to the *Wait-For-Reset* state. Alternately, if the device sees a compare error while it is shifting its ones-complement address it will stop shifting its address and tri-state TDO_B until the next shift operation; during the next *Shift-IR* operation it will again try to present its address (if the previous instruction was 3A hex) while monitoring TDO_B.

Shifting 3A hex into the instruction registers of the 'STA112s will continue until all 'STA112s have presented their address. At this time all devices will be waiting to be reset, and if a 3A is shifted into the 'STA112 instruction registers the address read by the tester will be all weak 1s due to all TDO_B's being tri-stated. Reading all ones will signal the tester that address interrogation is complete. Since all ones signifies the end of *Address-Interrogation*, no device can have an address of all zeros (ones-complement).

If at any time, during the address interrogation mode, any other instruction besides 3A hex is shifted into the instruction register, then the 'STA112 will exit the interrogation mode. Also, the 'STA112's state machine will go to the *Wait-For-Address* state.

This address interrogation scheme presumes that TDO_B is capable of driving a weak "1" and that an 'STA112 driving a "0" will overdrive an 'STA112 driving a weak "1".

The following is an example of the *Address-Interrogation* function. Assume there are three 'STA112s (U1, U2 and U3) on a dot1 backplane with slot addresses 00010100, 00100000 and 00000001 respectively (assuming 8 address pins).

1. The 'STA112s are reset and the interrogation address/op-code (3A hex) is shifted into the instruction registers.
2. At the end of the instruction shift (*Update-IR*) the 'STA112 address registers are loaded with 3A hex.

Special Features (Continued)

3. The TAPs are sequenced to *Capture-IR* and the shift registers latch the ones-complement slot addresses (U1=00101011, U2=00011111 and U3=00111110).
4. The TAPs are sequenced to *Shift-IR* and the LSB of the interrogation address is presented on the TDI_B's. Concurrently, the LSBs of the ones-complement slot addresses are presented on the respective TDO_B's.
5. The weak "1" being driven on U1 and U2 is overdriven by the "0" from U3. U1 and U2 enter the *Wait-For-Next-Interrogation* state.
6. The shift operation continues and U3 finishes shifting its ones-complement address (00111110) out on TDO_B. U3 enters the *Wait-For-Reset* state when the TAP enters *Update-IR*.
7. The TAPs are again sequenced to *Capture-IR* and U1 and U2 shift registers latch the ones-complement addresses (U1=00101011, U2=00011111).
8. The TAPs are sequenced to *Shift-IR* and the LSB of the interrogation address is presented on the TDI_B's. Concurrently, the LSBs of the ones-complement addresses are presented on the respective TDO_B's.
9. Since both U1 and U2 are driving a weak "1" the shift continues.
10. Again U1 and U2 drive weak "1" and the shift continues.
11. U2s weak "1" is overdriven by U1s "0" and U2 enters the *Wait-For-Next-Interrogation* state.
12. The shift operation continues and U1 finishes shifting its ones-complement address (00101011) out on TDO_B. U1 enters the*Wait-For-Reset* state.
13. The instruction shift operation is repeated and U2 shifts its ones-complement address (00011111) out on TDO_B. U2 enters the *Wait-For-Reset* state.
14. The instruction shift operation is repeated, however, all devices have been interrogated and are waiting for a reset. The master device will receive all ones. This implies that there can not be an 'STA112 with address 0!

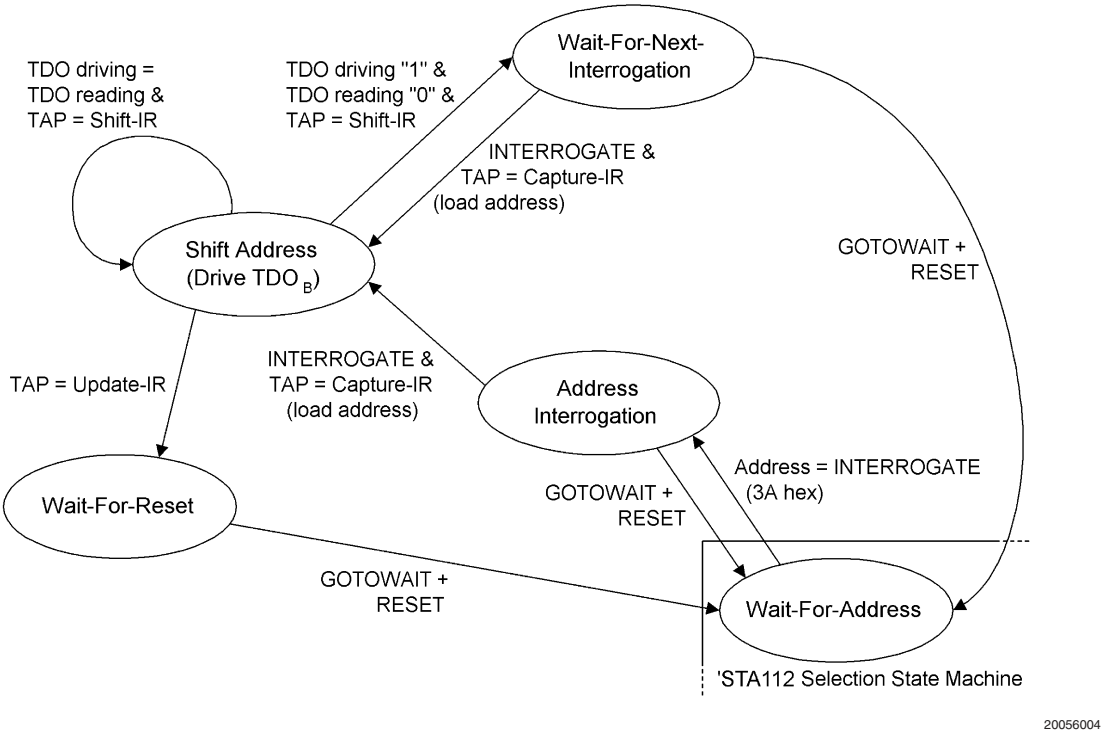

FIGURE 12. Address Interrogation State Machine

TABLE 14. Glossary

LFSR	Linear Feedback Shift Register. When enabled, will generate a 16-bit signature of sampled serial test data.
LSP	Local Scan Port. A four signal port that drives a local (i.e. non-backplane) scan chain. (e.g., TCK_0, TMS_0, TDO_0, TDI_0).
Local	Local is used to describe IEEE Std. 1149.1 compliant scan rings and the 'STA112 Test Access Port that drives them. The term local was adopted from the system test architecture that the 'STA112 will most commonly be used in; namely, a system test backplane with a 'STA112 on each card driving up to 7 local scan rings per card. (Each card can contain multiple 'STA112s, with 7 local scan ports per 'STA112.)
Park/Unpark/Unparked	Parked, unpark, and unparked, are used to describe the state of the LSP controller and the state of the local TAP controllers (the local TAP controllers refers to the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking a LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when a LSP controller is in one of the parked states, TMS_n is held constant, thereby holding or parking the local TAP controllers in a given state.
TAP	Test Access Port as defined by IEEE Std. 1149.1.
Selected/Unselected	Selected and Unselected refers to the state of the 'STA112 Selection Controller. A selected 'STA112 has been properly addressed and is ready to receive Level 2 protocol. Unselected 'STA112s monitor the system test backplane, but do not accept Level 2 protocol (except for the *GOTOWAIT* instruction). The data registers and LSPs of unselected 'STA112s are not accessible from the system test master.
Active Scan Chain	The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When a 'STA112 is selected with all of its LSPs parked, the active scan chain is the current scan register only. When a LSP is unparked, the active scan chain becomes: $TDI_B \rightarrow$ the current 'STA112 register $\rightarrow$ the local scan ring registers $\rightarrow$ a PAD bit $\rightarrow TDO_B$.
Level 1 Protocol	Level 1 is the protocol used to address a 'STA112.
Level 2 Protocol	Level 2 is the protocol that is used once a 'STA112 is selected. Level 2 protocol is IEEE Std. 1149.1 compliant when an individual 'STA112 is selected.
PAD	A one bit register that is placed at the end of each local scan port scan-chain. The PAD bit eliminates the prop delay that would be added by the 'STA112 LSPN logic between TDI_n and $TDO_{(n+1)}$ or TDO_B by buffering and synchronizing the LSP TDI inputs to the falling edge of TCK_B, thus allowing data to be scanned at higher frequencies without violating set-up and hold times.
LSB	Least Significant Bit, the right-most position in a register (bit 0).
MSB	Most Significant Bit, the left-most position in a register.
Transparent	A mode of operation which eliminates any STA112 registers or pad bits from the scan chain.
Stitcher	A mode of operation where LSPs to include in the scan chain may be defined by external pins, or by the contents of a register.

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