PC97317 RTC Oscillator Design Guidelines

National Semiconductor
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1.0 Scope

The National Semiconductor® PC97317 SuperI/O device uses a 32.768 KHz clock signal for operation of the Real Time Clock module (RTC).

The clock is generated by an on-chip amplifier and off-chip crystal, capacitors and resistors (see Figure 2-2).

The PC backup battery keeps the oscillator alive when both main and standby power are off. The oscillator circuit is designed to provide kick-start drive and current and to enable steady-state minimal power consumption, thus increasing battery life.

This application note describes design guidelines for optimal operation of the oscillator and battery circuits.

2.0 Oscillator Circuit Considerations

The design of the oscillator circuit affects RTC accuracy, as well as clock wake-up time. Close attention must be paid to noise, signal integrity and load capacitance.

Figure 2-1 shows the recommended layout for the oscillator circuit.

2.1 NOISE AND SIGNAL INTEGRITY

Typically, PC motherboards are noisy environments.

The PC97317 oscillator circuit's very low power consumption and the resulting high impedance make it sensitive to noise on the X1C, X2C and VBAT pins.

Noise may cause:

- False pulses
- A false power-fail alarm due to a glitch on V_{BAT}

Section 3.0 provides guidelines for minimizing noise.

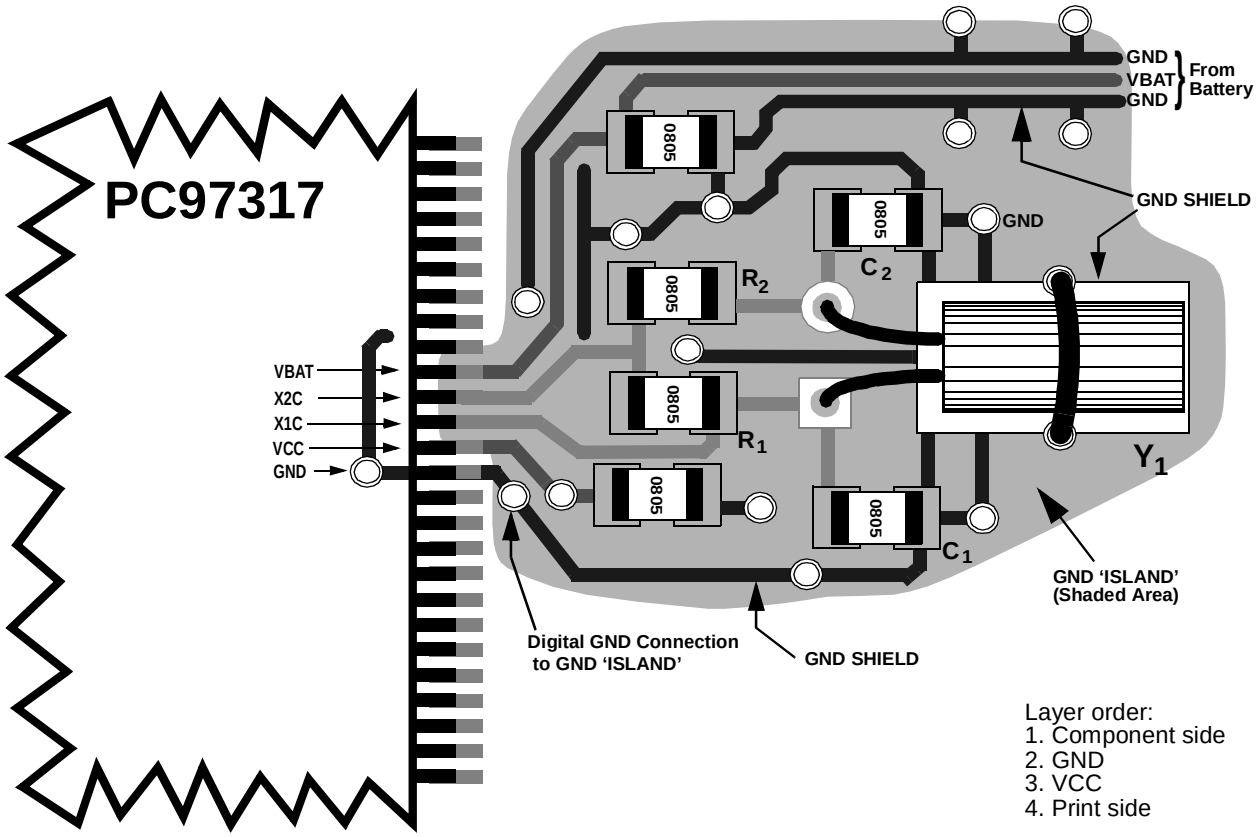

Figure 2-1. On-Chip Oscillator Circuit Layout

2.2 LOAD CAPACITANCE

The load capacitance (C_L) should be within the crystal manufacturer's recommended limits (typically 12.5 pF).

The load capacitance consists of C_1 in series with C_2 and in parallel with the parasitic capacitance of the oscillator circuit, as shown in Figure 2-2.

The following equation shows how C_L is calculated:

$$C_L = \left(\frac{1}{\frac{1}{C_1+C_{IN1}+C_{TRACE1}} + \frac{1}{C_2+C_{IN2}+C_{TRACE2}}} \right) + C_{PARASITIC}$$

where:

C_L = load capacitance

C_{IN1}, C_{IN2} = input capacitance of X1C, X2C

C_{TRACE1} = capacitance of the trace between the crystal and X1C

C_{TRACE2} = capacitance of the trace between the crystal and X2C

$C_{PARASITIC}$ = parasitic capacitance of the crystal

Parasitic capacitance should be kept to a minimum to improve control over the oscillator circuit.

Section 3.0 provides guidelines for minimizing parasitic capacitance.

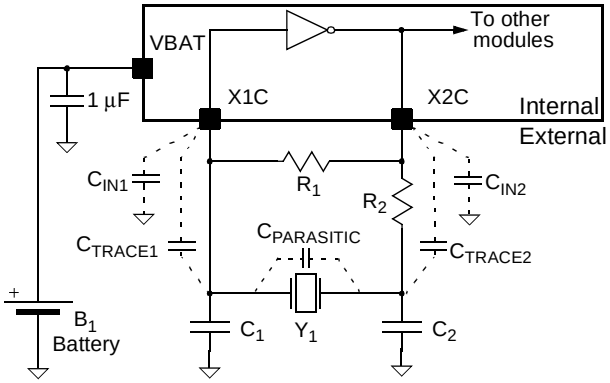

Figure 2-2. "On-Chip" Oscillator Circuitry

3.0 Design Guidelines

The guidelines in this section help to minimize noise and parasitic capacitance on the X1C, X2C and VBAT pins.

3.1 DESIGN

- Use small SMD parts where possible. The recommended parts, as shown in Figure 2-1, are: SMD 0805-size capacitors and resistors, and a crystal in a cylindrical package; however, other package types may be used.
- Connect the battery directly to the PC87317 VBAT pin (i.e., do not use a resistor or diode).
  — The PC97317 is UL compliant (E146664), with an internal current-limiting resistor (~1 KΩ).
  — The PC97317 has a switch that disconnects the battery when main power is on; thus a diode is not needed for switching.

3.2 COMPONENT PLACEMENT

- Place C_1, C_2, R_1, R_2 and the crystal as close as possible to the X1C and X2C pins.
- Place the 1 µF ceramic capacitor as close as possible to the VBAT pin.
- Place the battery near the PC87317 to make VBAT signal routing easier.

3.3 SIGNAL ROUTING

- Make X1C, X2C and VBAT traces as short as possible, with no (or minimum) vias.
- Do not run digital signals near the oscillator circuit area.
- Place a ground layer "island" beneath the oscillator components and the battery, immediately below the upper layer (component side). The ground layer "island" is shown in the shaded area in Figure 2-1. Connect the "island" to the digital ground plane close to pin 60 (GND) of the PC97317. This prevents the switching currents that flow through the ground plane from penetrating the ground layer "island".
- Shield the X1C and X2C signals to minimize the stray capacitance of the X1C and X2C traces:
  — Traces should not be wider than 8 mil.
  — Ground shielding should not be too close.
- To minimize parasitic capacitance between X1C and X2C, do not run X1C and X2C traces in parallel over long distances.
- If the battery is placed at a distance of more than 30 mm from the VBAT pin, shield the VBAT wire, as shown in Figure 2-1.

4.0 Oscillator Accuracy

RTC timekeeping accuracy depends on the oscillator frequency, which depends on the crystal circuit design and the operating environment, as detailed below:

- Crystal tolerance is a crystal parameter that measures the maximum and minimum frequency. It is usually measured in parts per million (ppm) of the nominal frequency (f0). The higher the ppm, the larger the difference between different crystals. Figure 4-1 shows an example of a 100 ppm crystal.

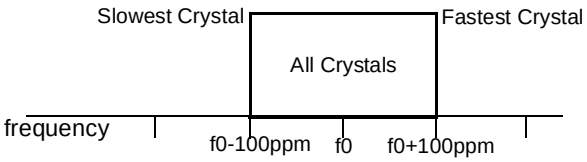

Figure 4-1. Crystal Tolerance

- The operating temperature affects the oscillating frequency. The formula for frequency deviation at temperature is: $\Delta F = F^* K (T_0 - T)^2$
  where: ΔF = Frequency Deviation
  F = Nominal Frequency
  K = Temperature Characteristic
  T_0 = Turnover Temperature
  T = Operating Temperature

  As the formula indicates, a crystal with a lower temperature characteristic (K) has smaller frequency changes over a specified temperature range.

  Figure 4-2 shows typical frequency deviation with temperature.

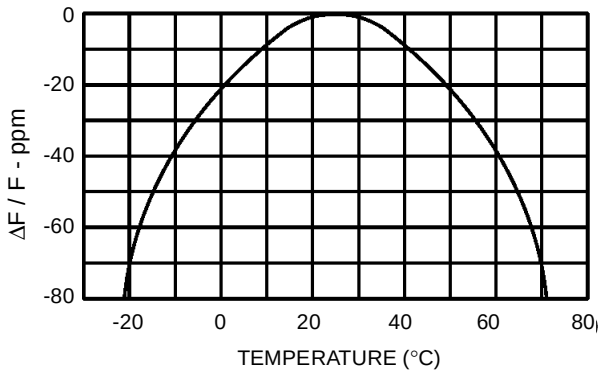

Figure 4-2. Crystal Oscillator Accuracy as a Function of Temperature

- Changes in the load capacitance affect the oscillating frequency. The load capacitance is affected by the routing of X1C and X2C (see Section 3.3). Humidity also affects load capacitance. Painting the area of the board above the GND island (Figure 2-1) with water resistant paint can reduce the effect of humidity. Note that the more accurate the capacitors, the smaller the differences between systems.
- The oscillation frequency changes over time due to internal changes in the crystal. This phenomena is called 'aging', and is typically expressed in parts per million per year [ppm/year].

Appendix: Oscillator Calibration

Usually, calibrating the oscillator is not necessary. However, if a highly accurate clock is required, the procedure described in "Calibration" can be used.

As Figure 4-3 shows, a faster board of a specific design might oscillate at a frequency below 32.768KHz, (Block A); for another design, a slower board might oscillate at a frequency above 32.768KHz (Block C).

The suggested calibration process 'centers' the average frequency of a specific design at 32.768KHz, thereby decreasing the maximum and minimum timekeeping error (Block B).

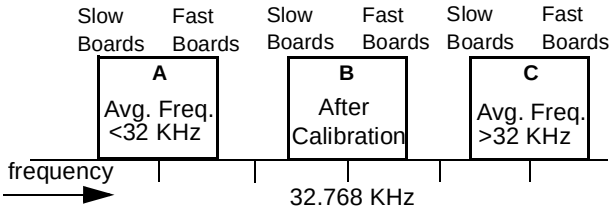

Figure 4-3. Average Frequency before and after Calibration

Calibration is performed by changing C_1 capacitance (see Figure 2-2) to increase or decrease the oscillator frequency.

When calibrating the oscillator, the system temperature must be considered: calibration at system operating temperature may provide better results if the system is expected to be running constantly; calibration at a temperature somewhere between room temperature and operating temperature may provide better overall results.

Calibration

To calibrate the oscillator:

1) Record the oscillator frequency of each board in the first batch of boards:
   a) Configure an operational amplifier (op-amp) with very high input impedance (LMC6041) as a unity gain amplifier.
   b) Connect the input of the amplifier to the PC97317 X2C pin.
   c) Attach a probe to the output of the amplifier, and use a scope or a frequency meter to measure the clock frequency.

   Note: Another option is to read the system time, and compare it with a reference clock. However, this option is less accurate and takes more time.
2) Select a board whose frequency is the average frequency of all the boards tested, and replace C_1 with a capacitor of higher or lower value to get a frequency of exactly 32.768 KHz. If replacing C_1 does not yield the desired result, also replace C_2.
3) Use the new value of the C_1 capacitor (and C_2 capacitor, if changed) in the board design instead of the nominal value suggested in the *PC97317 Datasheet*.

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National Semiconductor Corporation
Americas
Email:
new.feedback@nsc.com

National Semiconductor
Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 87 90

National Semiconductor
Asia Pacific Customer
Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507
Email: nsj.crc@jksmtp.nsc.com

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