Dual Foot Print Layout Notes for DP83865 Gig PHYTER® V and DP83847 DS PHYTER II

National Semiconductor
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1.0 Introduction

This document contains information needed to combine the 10/100 DS PHYTER II and the 10/100/1000 Gig PHYTER V on the printed circuit board.

The objectives are:

- To accommodate 10/100 or Gigabit PHY on the same board as a stuff option
- A separate reference bill of material for each of the PHY option
- Retain optimal performance for each option
- Minimize board space
- Use integrated magnetics/RJ45
- Minimize component cost for each PHY option

Since the DS PHYTER has a smaller LLP package, it fits within the Gig PHYTER foot print. On the MDI side, the 10/100 and the Gigabit signals remains almost the same. This is achieved by having a integrated magnetics that maintain the same foot print but having different windings for the 10/100 and the Gigabit options. On the MAC side, the GMII and MII data lines are combined to save board space and termination resistors.

This document is divided into two sections:

- Layout notes
- BOM and component selection

A schematic diagram of the reference design can be downloaded from the following web link:

http://networks.national.com, in the center column, under Resources, Schematic (DP83847 and DP83865)

To ease the PCB design job, the design notes for DS PHYTER II and Gig PHYTER V are included in this documentation. The integrated magnetics/RJ45 that has the same foot print for both the 10/100 version and Gigabit version is included in the BOM.

If a discrete magnetics is desired, there are transformers available from Pulse Engineering that share the same foot print between 10/100 and Gigabit.

2.0 Layout Notes

The most critical parts of the dual foot print layout are the MDI section, the RGMII/MII section, and the crystal oscillator section.

The MDIO clock rate is 2.5 MHz maximum. However, the clock edge may be fast. Care should be taken to minimize reflection that may cause glitches on the edge that could cause double clocking.

Please check out the design notes section of the datasheet and follow the recommendations.

2.1 MDI SIDE

The MDI connection between the DS PHYTER II and the Gig PHYTER V should be kept at minimum. In the Gigabit operation, the PC trace stubs could cause reflection that may degredate the cable length performance of the Gigabit mode.

The MDI termination resistors should be placed as close to the Gig PHYTER as possible. The power supply decoupling caps (C2 and C5) should be placed close to the termination resistors.

The transformer center tap decoupling caps (C3 and C4) should be placed as close to the magnetics as possible.

The MDI traces are differential signal pairs. The spacing between the pairs should be kept at least 0.25 inch apart. The differential pairs should be running close in parallel to minimize common mode noise pick up. In addition, avoid placing via on the differential trace since via presents extra capacitive load.

Place solid ground plane under the differential signals to minimize EMI radiation.

Please refer to datasheet design notes section for more information.

2.2 MAC SIDE

The RGMII signaling is 125 MHz using both rising and falling edges of the clock. The Tx and the RX side trace length should be matched within the signal group to minimize timing skew. It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.

Minimize the number of via on the RGMII lines to minimize timing skew. Since the signal rise and fall time are sub-nano second, transmission line design guide lines should be followed. Please refer to datasheet design notes section and DP83865 application notes on the RGMII.

2.3 CLOCK CIRCUITRY

The crystal is shared between the DS PHYTER II and the Gig PHYTER V. Please keep all the crystal circuitry traces as short as possible and as close to the PHY as possible.

Place the RF6 stuff option resistor as close to the Gig PHYTER clock pad as possible. In the Gigabit mode, the RF6 resistor is not stuffed so that the X0 signal terminates at the Gig PHYTER V clock input. This minimizes the trace stub. (*Figure 1*)

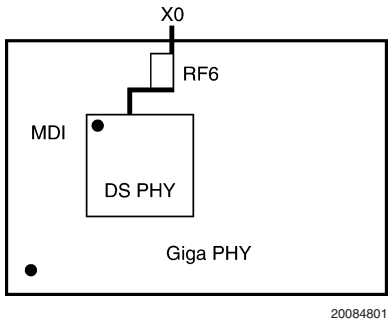

FIGURE 1. Use RF6 for Reduce Stubb

2.0 Layout Notes (Continued)

Mentioned in the previous section, care should be taken on the MDC signal to minimize glitch on the clock edge. The glitch on the clock edge may cause double clocking. Connect the MDC as multidrop instead of branched between the DS PHYTER II and Gig PHYTER V pads. (*Figure 2* and *Figure 3*)

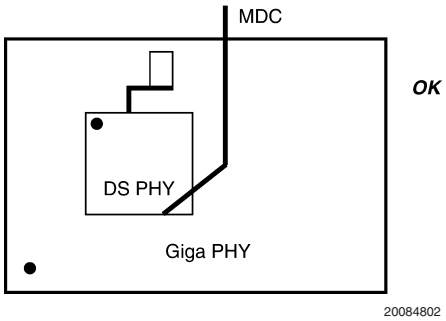

FIGURE 2. A "multidrop" Connection

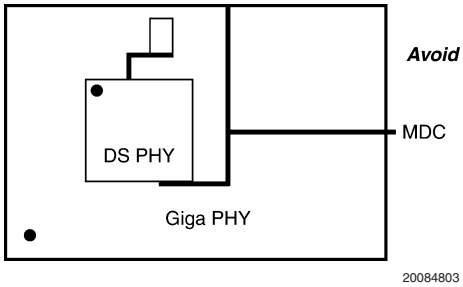

FIGURE 3. Avoid Stubb

For notes on reset requirement, power supply decoupling, sensitive pins, PCB layer stacking, and other information, please refer to the design notes in the datasheet or application notes.

3.0 BOM and Component Selection

Reference designators R and C are shared in both DS PHYTER and Gig PHYTER circuitries. References CG and RG are used in Gig PHYTER circuitry only. Reference CF and RF are used in the DS PHYTER only. ("G" stands for Gigabit; "F" stands for Fast Ethernet.) RX and TX values are different between the DS PHYTER II and the Gig PHYTER V.

3.1 DS PHYTER II BOM

The 10/100 BOM is listed in the following table.

Item	Qty	Reference	Description	MFG Part Number
1	2	C7,C9	Cap, 0.01uF, ceramic, SMD 0603	
2	7	C2, C3, C4, C5, C6, C8, CF2	Cap, 0.1uF, Ceramic, SMD 0603	
3	2	C1, CF1	Cap, 10uF, 16V, Tant, SMD 3528	
4	2	C10,C11	Cap, 33pF, Ceramic, SMD 0603	
5	1	RF1	Res, 10K, 1%, SMD 0603	
6	7	RF2,RF3,RF4, R5, R6, R7, R8	Res, 33R, 5%, SMD 0603	
7	2	RF5,RF6	Res, 0R, SMD 0603	
8	6	R3,R4,R9,R10,R11,R12	Res, 49R9, 1%, SMD 0603	
9	2	RX1,RX2	Res, 54R9, 1%, SMD 0603	
10	3	R1,R2,R13	Res, 2K0, 5%, SMD 0603	
11	1 TX1		10/100 Magnetics-RJ45	PulseEng JK0-0003
12	1	UF1	IC, 10/100 PHY, LLP	NSC DP83847 LQA56A
13	1	Y1	Crystal, 25MHz, 50PPM	

3.2 Gig PHYTER V BOM

The 10/100/1000 Gig PHYTER V BOM is listed in the following table.

Item	Qty	Reference	Description	MFG Part Number
1	6	CG1,CG4,CG6,C7,CG8,C9	Cap, 0.01uF, ceramic, SMD 0603	
2	1	CG2	Cap, 22uF, 16V, Tant, SMD 3528	
3	9	C2,CG3,C3,C4,CG5,C5,C6,CG7,C8	Cap, 0.1uF, Ceramic, SMD 0603	
4	2	C1,CG9	Cap, 10uF, 16V, Tant, SMD 3528	
5	2	C10, C11	Cap, 33pF, Ceramic, SMD 0603	
6	6	RG5, R5, RG6, R6, R7, R8	Res, 33R, 5%, SMD 0603	
7	3	RG1, RG2, RG4	Res, 0R, SMD 0603	
8	1	RG3	Res, 18R, 5%, SMD 0603	
9	1	RG7	Res, 9K76, 1%, SMD 0603	
10	8	RX1,RX2,R3,R4,R9,R10,R11,R12	Res, 49R9, 1%, SMD 0603	
11	3	R1,R2,R13	Res, 2K0, 5%, SMD 0603	
12	1 TX1		10/100/1000 Magnetics-RJ45	PulseEng JK065421
13	1	UG1	IC, 10/100/1000 PHY, PQFP	NSC DP83865BVH
14	1	Y1	Crystal, 25MHz, 50PPM	

3.3 COMPONENT SELECTION

The listed Pulse Engineering Magnetics/RJ45 shares the same foot print between the 10/100 and the 10/100/1000 modules.

Pulse Engineering also has a 10/100 discrete transformer (H1267) that shares the same foot print with the commonly used H5007 Gigabit transformer.

The crystal requirement is listed in the section 8.0 of the DP83865 datasheet. Please follow the recommendations in the design guide of the datasheet.

3.4 REFERENCE SCHEMATIC DIAGRAM

Please download the schematic diagram from the following web link:

http://networks.national.com, in the center column, under Resources, Schematic (DP83847 and DP83865)

Notes

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