# Application Brief

## 2.5 Gbps LVDS 4 x 4 Crosspoint Switch

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The unique architecture, diminutive size and flow through pinout of the DS90CP04 (*Figure 1*) make it an ideal building block for today's high performance systems. This 4 x 4 crosspoint switch easily expands to build larger or uniquely shaped switch arrays. Digital control pins give the designer direct access to common building block functionality. Low power LVDS (Low Voltage Differential Signal) design and an efficient, low profile 6 mm square LLP (Leaded Leadless Package), allow the CP04 to be placed into the tightest board designs. Each CP04 is guaranteed to operate at datarates to 2.5 Gbps. Clock distribution applications will support output clock rates up to 1.5 GHz.

**Programming The Switch**

The DS90CP04 can be programmed in two ways, via external control pins (Mode = 1), or through a serial link (Mode = 0). The digital control pins provide immediate access to commonly used switch configurations:

1. Broadcast (1:4)
2. Buffer/Repeater (4:4)
3. Redundancy (Dual 1:2)

For applications where multiple CP04s will be utilized as larger switch arrays, or when flexible hardware configurations are required, a serial programming link is provided. This link enables the designer to daisy-chain multiple CP04s together and reprogram individual ICs based on an address determined by IC placement in the serial stream. For array applications, row and column links can simplify the programming model and ease board routing constraints.



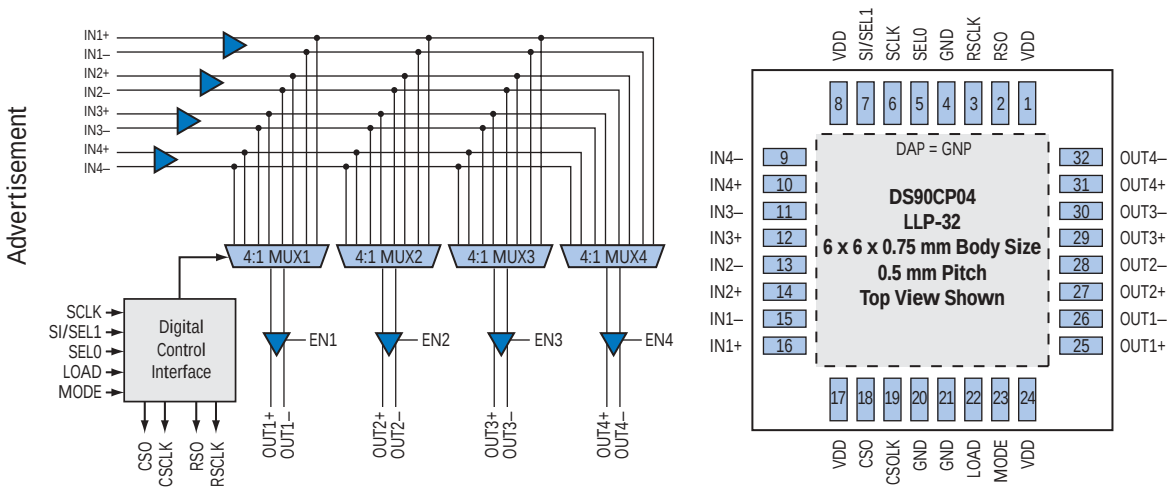


*Figure 1: DS90CP04 Block Diagram and Pinout*

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## Highly Adaptable I/Os

Designers are often faced with various signaling issues between subsystems or even adjacent ICs. At the forefront is signal interface of signal translation. This problem isn't limited to low speed TTL signals. High-speed differential lines can also require special conditioning or translation.

The CP04 allows for an extended input common mode range, easily translating from other widely used high-speed technologies like CML (Current Mode Logic) or LVPECL (Low Voltage Positive ECL) to LVDS. The chart shown in *Figure 2* highlights typical voltage swings generated by various high-speed I/O technologies.

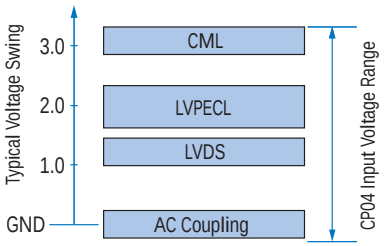


*Figure 2: I/O Voltage Levels*

## Performance Measurements

For high-speed data communications, just being able to detect various I/O standards isn't enough. The CP04 is tuned to produce low jitter LVDS outputs for a wide range of the input signal conditions. Running at the maximum specified datarate of 2.5 Gbps a PRBS datastream (shown in *Figure 3*) will have 35 ps pp of total jitter. The CP04 AC response is flat across the entire common mode range with input voltage swings of as low as 100 mV. Whether it's being used to switch clock and data in a CDR application or for simple distribution, the CP04 delivers low skew (40 ps typical, 100 ps maximum, see *Figure 4*) performance for all possible datapaths.

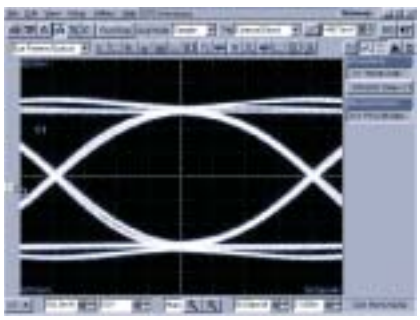

*Figure 3: 2.5 Gbps Eye Diagram*

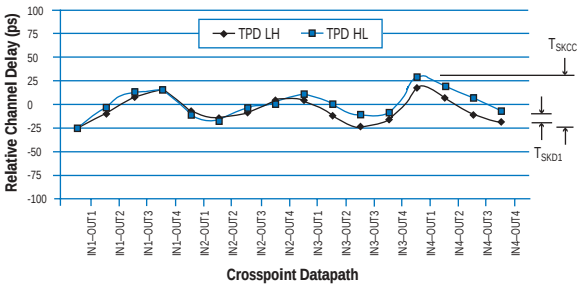


*Figure 4: Channel to Channel Skew*

**LVDS Specialty Function Selection Guide**

| Part Number | Description | Data Rate | Jitter (ps) |
|---|---|---|---|
| DS92CK16 | 1 to 6 LVDS Clock Distribution | DC to 125 MHz | -- |
| DS90LV110 | 1 to 10 LVDS Clock Distribution | DC to 400 MHz | $2.8_{RMS}$ |
| DS90LV110 | 1 to 10 LVDS Data Distribution | DC to 800 Mbps | 145 |
| DS90CP04 | 4 x 4 Digital Crosspoint Switch (Data) | DC to 2.5 Gbps | 35 |
| DS90CP04 | 4 x 4 Digital Crosspoint Switch (Clock) | DC to 1.25 GHz | $2.5_{RMS}$ |
| DS90CP22 | 2 x 2 Digital Crosspoint Switch | DC to 800 Mbps | 75 |
| DS90LV001 | 1-Bit LVDS Repeater | DC to 800 Mbps | 100 |
| DS92001 | 1-Bit BLVDS Backplane Driver (27Ω) | DC to 400 Mbps | -- |


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