National Semiconductor

December 2003
Revision 1.1

PC87383
Legacy-Reduced SuperI/O with Fast Infrared Port, Serial Port, Parallel Port and GPIOs for Portable Applications

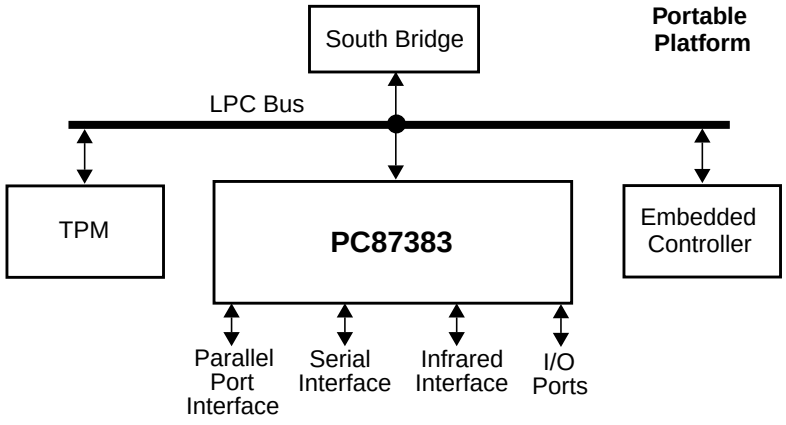
General Description

The PC87383, a member of the National Semiconductor LPC SuperI/O family, is targeted for a wide range of portable applications. The PC87383 is PC2001 and ACPI compliant, and features Fast Infrared port (FIR, IrDA 1.1 compliant), Serial Port, Parallel Port and General-Purpose Input/Output (GPIO) support for a total of 21 ports.

Outstanding Features

- LPC bus interface, based on Intel's *LPC Interface Specification* Revision 1.1, August 2002 (supports CLKRUN and LPCPD signals)
- Fast Infrared port
- PC2001 and ACPI Revision 2.0 compliant
- Serial IRQ support (15 options)
- Protection features, including GPIO lock and pin configuration lock
- 21 GPIO ports, including 14 with "assert IRQ" capability
- XOR Tree and TRI-STATE® device pins (or ICT) testability modes.
- 5V tolerant and back-drive protected pins (except LPC bus pins)
- 64-pin TQFP package

System Block Diagram



Features

- LPC System Interface
  - Synchronous cycles, up to 33 MHz bus clock
  - 8-bit I/O cycles
  - Up to four 8-bit DMA channels
  - $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support
  - Implements PCI mobile design guide recommendation (*PCI Mobile Design Guide 1.1, Dec. 18, 1998)*
- PC2001 and ACPI Compliant
  - PnP Configuration Register structure
  - Flexible resource allocation for all logical devices
    - Relocatable base address
    - 15 IRQ routing options
    - Three optional 8-bit DMA channels (where applicable) selected from four possible DMA channels
- Clock Sources
  - 14.318 MHz or 48 MHz clock input
  - LPC clock, up to 33 MHz
- Power Supply
  - 3.3V supply operation
  - All pins are 5V tolerant, except LPC bus pins
  - All pins are back-drive protected, except LPC bus pins
- 21 General-Purpose I/O (GPIO) Ports
  - 14 support assert IRQ
  - Programmable drive type for each output pin (open-drain, push-pull or output disable)
  - Programmable option for internal pull-up resistor on each input pin
  - Output lock option
  - Programmable option for input debounce mechanism
- Serial Port (SP1)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
- IEEE 1284-compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the PC87383 is in power-down state)
- Fast Infrared Port (FIR)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - FIR IrDA 1.1 compliant
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
  - DMA support: 1 or 2 channels
- Strap Configuration
  - Base Address (BADDR) strap to determine the base address of the Index-Data register pair
  - Strap Inputs to select testability mode
- Testability
  - XOR Tree
  - TRI-STATE device pins

Revision Record

Revision Date	Status	Comments
October 2003	Draft 1.0	First draft.
December 2003	Revision 1.1	Added I_{DD} and I_{DDLP} current numbers. Added IR register map and bit map. Technical writing edits and typos.

Table of Contents

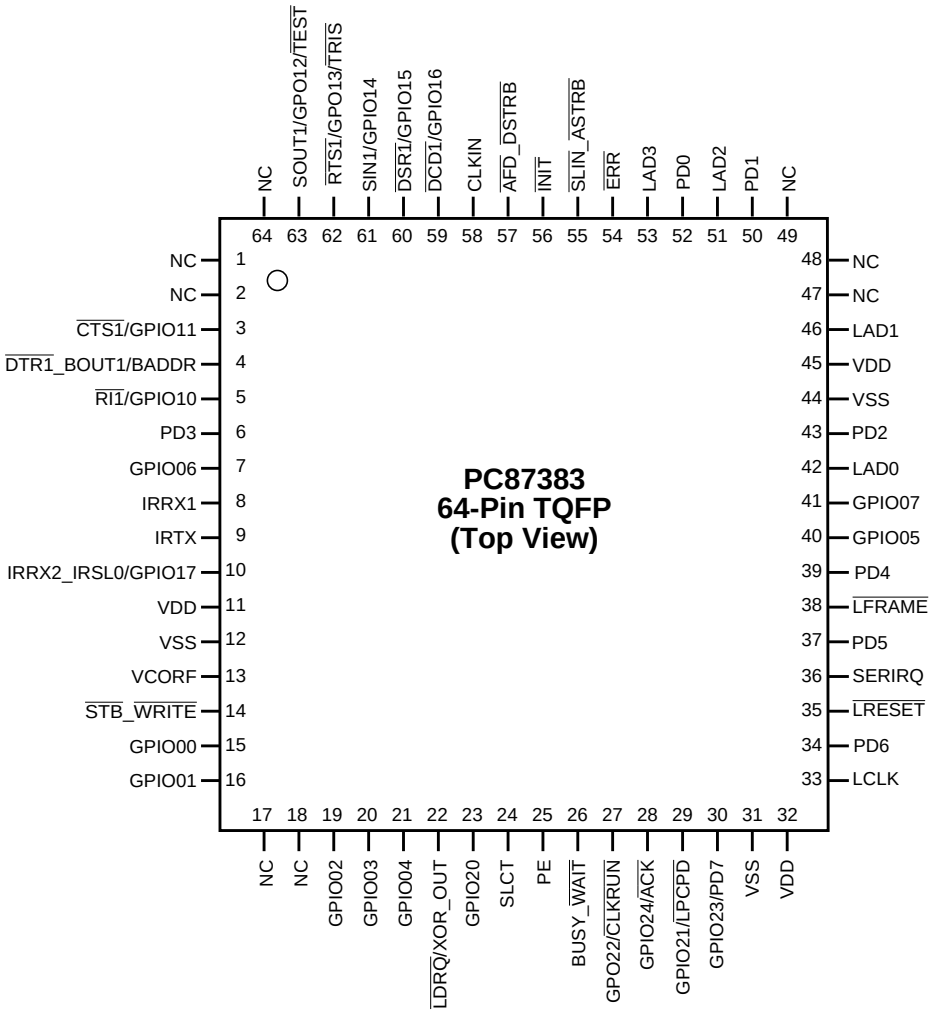
Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM



64-Pin Thin Quad Flatpack (TQFP)
NS Package Number VEC064A
Order Number PC87383-VS

1.0 Signal/Pin Connection and Description (Continued)

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

This section describes all signals. Signals are organized in functional groups.

Buffer Types

The signal DC characteristics are denoted by a buffer type symbol, described briefly in Table 1and in further detail in Chapter 7 on page 63.

Table 1. Buffer Types

Symbol	Description
IN_{PCI}	Input, PCI 3.3V
IN_{T}	Input, TTL compatible
IN_{TS}	Input, TTL compatible, with Schmidt Trigger
O_{PCI}	Output, PCI 3.3V
$O_{p/n}$	Output, push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA
OD_{n}	Output, open-drain output buffer that is capable of sinking *n* mA
PWR	Power pin
GND	Ground pin

Table 2. Pin Multiplexing Configuration

Functional Block	Signal	Functional Block	Signal	Configuration Select	Functional Block	Signal	Configuration Select
Serial Port	$\overline{\text{DTR1}}$_BOUT1	Straps	BADDR	Strap			
GPIO	GPIO10	Serial Port	$\overline{\text{RI1}}$	SIOCF2[0]			
GPIO	GPIO11	Serial Port	$\overline{\text{CTS1}}$				
GPIO	GPO12	Serial Port	SOUT1		Straps	$\overline{\text{TEST}}$	Strap
GPIO	GPO13	Serial Port	$\overline{\text{RTS1}}$		Straps	$\overline{\text{TRIS}}$	Strap
GPIO	GPIO14	Serial Port	SIN1				
GPIO	GPIO15	Serial Port	$\overline{\text{DSR1}}$				
GPIO	GPIO16	Serial Port	$\overline{\text{DCD1}}$				
GPIO	GPIO17	Infrared	IRRX2_IRSL0	SIOCF2[1]			
GPIO	GPIO21	LPC	$\overline{\text{LPCPD}}$	SIOCF2[3]			
GPIO	GPO22	LPC	$\overline{\text{CLKRUN}}$	SIOCF2[5]			
GPIO	GPIO23	Parallel Port	PD7	SIOCF2[7]			
GPIO	GPIO24	Parallel Port	$\overline{\text{ACK}}$	SIOCF2[7]			
LPC	$\overline{\text{LDRQ}}$	Testability	XOR_OUT	Strap			

1.0 Signal/Pin Connection and Description (Continued)

1.3 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all PC87383 signals.

1.3.1 LPC Bus Interface

Signal	Pin(s)	I/O	Buffer Type	Description
LAD3-0	53, 51, 46, 42	I/O	IN_{PCI}/O_{PCI}	**LPC Address-Data.** Multiplexed command, address bidirectional data and cycle status.
LCLK	33	I	IN_{PCI}	**LPC Clock**. Same as PCI clock (up to 33 MHz).
$\overline{LDRQ}$	22	O	O_{PCI}	**LPC DMA Request**. Encoded DMA request for LPC interface.
$\overline{LFRAME}$	38	I	IN_{PCI}	**LPC Frame**. Low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.
$\overline{LRESET}$	35	I	IN_{PCI}	**LPC Reset.** In a practical implementation, it is connected to the PCI system reset.
SERIRQ	36	I/O	IN_{PCI}/O_{PCI}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.
$\overline{LPCPD}$	29	I	IN_{PCI}	**Power Down.** Indicates that the peripheral should prepare for power to be shut down on the LPC interface.
$\overline{CLKRUN}$	27	I/OD	IN_{PCI}/OD_6	**Clock Run.** Same as PCI $\overline{CLKRUN}$.

1.3.2 Clocks

Signal	Pin(s)	I/O	Buffer Type	Description
CLKIN	58	I	IN_T	**Clock In.** 14.318 MHz or 48 MHz clock input.

1.3.3 Parallel Port

Signal	Pin(s)	I/O	Buffer Type	Description
$\overline{ACK}$	28	I	IN_T	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the parallel port.
$\overline{AFD\_DSTRB}$	57	O	OD_{14}, $O_{14/14}$	**$\overline{AFD}$ - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{DSTRB}$ - Data Strobe (EPP).** Active low; used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{DSTRB}$ becomes inactive (high).
BUSY_$\overline{WAIT}$	26	I	IN_T	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the parallel port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	54	I	IN_T	**Error.** Set active low by the printer when it detects an error.
$\overline{INIT}$	56	O	OD_{14}, $O_{14/14}$	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin.
PD7-0	30, 34, 37, 39, 6, 43, 50, 52	I/O	$IN_T/O_{14/14}$	**Parallel Port Data.** Transfers data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability.
PE	25	I	IN_T	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Description
SLCT	24	I	IN_T	**Select.** Set active high by the printer when the printer is selected.
$\overline{SLIN}$_$\overline{ASTRB}$	55	O	OD_{14}, $O_{14/14}$	**$\overline{SLIN}$ - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{ASTRB}$ - Address Strobe (EPP).** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{ASTRB}$ becomes inactive (high).
$\overline{STB}$_$\overline{WRITE}$	14	O	OD_{14}, $O_{14/14}$	**$\overline{STB}$ - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{WRITE}$ - Write Strobe.** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{WRITE}$ becomes inactive (high).

1.3.4 Infrared (IR)

Signal	Pin(s)	I/O	Buffer Type	Description
IRRX1	8	I	IN_{TS}	**IR Receive 1.** Primary input to receive serial data from the IR transceiver.
IRRX2_IRSL0	10	I/O	$IN_{TS}/O_{3/6}$	**IRRX2 - IR Receive 2.** Auxiliary IR receiver input to support a second transceiver. **IRSL0 - IR Select**. Output used to control the IR transceiver.
IRTX	9	O	$O_{6/12}$	**IR Transmit.** IR serial output data.

1.3.5 Serial Port (SP1)

Signal	Pin(s)	I/O	Buffer Type	Description
$\overline{CTS1}$	3	I	IN_{TS}	**Clear to Send.** When low, indicates that the modem or other data transfer device is ready to exchange data.
$\overline{DCD1}$	59	I	IN_{TS}	**Data Carrier Detected.** When low, indicates that the modem or other data transfer device has detected the data carrier.
$\overline{DSR1}$	60	I	IN_{TS}	**Data Set Ready.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{DTR1}$_BOUT1	4	O	$O_{3/6}$	**Data Terminal Ready.** When low, indicates to the modem or other data transfer device that the UART is ready to establish a communications link. **Baud Output.** Provides the associated serial channel baud rate generator output signal if Test mode is selected, i.e., if bit 7 of the EXCR1 register is set.
$\overline{RI1}$	5	I	IN_{TS}	**Ring Indicator.** When low, indicates that a telephone ring signal was received by the modem. It is monitored during power-off for wake-up event detection.
$\overline{RTS1}$	62	O	$O_{3/6}$	**Request to Send.** When low, indicates to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets this signal to inactive high; a loopback operation holds it inactive.
SIN1	61	I	IN_{TS}	**Serial Input.** Receives composite serial data from the communications link (peripheral device, modem or other data transfer device).
SOUT1	63	O	$O_{3/6}$	**Serial Output.** Sends composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.

1.0 Signal/Pin Connection and Description (Continued)

1.3.6 General-Purpose Input/Output (GPIO) Ports

Signal	Pin(s)	I/O	Buffer Type	Description
GPIO00-07	15, 16, 19, 20, 21, 40, 7, 41	I/O	IN_{TS}/ OD_6, $O_{3/6}$	**General-Purpose I/O Port 0, bits 0-7.** Each pin is configured independently as input or I/O, with or without static pull-up, and with either open-drain or push-pull output type. The port supports interrupt assertion, and each pin can be enabled or masked as an interrupt source.
GPIO10-11, GPIO14-17	5, 3, 61, 60, 59, 10	I/O	IN_{TS}/ OD_6, $O_{3/6}$	**General-Purpose I/O Port 1, bits 0-1 and bits 4-7.** Same as Port 0.
GPO12-13	63, 62	O	OD_6, $O_{3/6}$	**General-Purpose Output Port 1, bits 2-3.** Each pin is configured independently with or without static pull-up, and with either open-drain or push-pull output type.
GPIO20-21, GPIO23-24	23, 29, 30, 28	I/O	IN_{TS}/ OD_6, $O_{3/6}$	**General-Purpose I/O Port 2, Bits 0, 1, 3, 4.** Same as Port 0, but without interrupt support.
GPO22	27	O	OD_6, $O_{3/6}$	**General-Purpose Output Port 2, bit 2.** The pin is configured with or without static pull-up, and with either open-drain or push-pull output type.

1.3.7 Power and Ground

Signal	Pin(s)	I/O	Buffer Type	Description
V_{DD}	11, 32 45	I	PWR	**Main 3.3V Power Supply.**
V_{SS}	12, 31, 44	I	GND	**Ground.**

1.0 Signal/Pin Connection and Description (Continued)

1.3.8 Strap Configuration

Signal	Pin(s)	I/O	Buffer Type	Description
BADDR	4	I	IN_{TS}	**Base Address.** Sampled at V_{DD} Power-Up to determine the base address of the configuration Index-Data register pair. – No pull-down resistor (default) - the Index-Data pair at 164Eh-164Fh. – 10 KΩ[1] external pull-down resistor - the Index-Data pair at 2Eh-2Fh[1]. The external pull-down resistor must be connected to V_{SS}.
$\overline{TRIS}$	62	I	IN_{TS}	**TRI-STATE Device.** Sampled at V_{DD} Power-Up to force the device to float all its output and I/O pins. – No pull-down resistor (default) - normal pin operation – 10 KΩ[1] external pull-down resistor - floating device pins The external pull-down resistor must be connected to V_{SS}. When $\overline{TRIS}$ is set to 0 (by an external pull-down resistor), $\overline{TEST}$ must be 1 (i.e., left unconnected).
$\overline{TEST}$	63	I	IN_{TS}	**XOR Tree Test Mode.** Sampled at V_{DD} Power-Up to force the device pins into a XOR tree configuration. – No pull-down resistor (default) - normal device operation – 10 KΩ[1] external pull-down resistor - pins configured as XOR tree. The external pull-down resistor must be connected to V_{SS}. When $\overline{TEST}$ is set to 0 (by an external pull-down resistor), $\overline{TRIS}$ must be 1 (i.e., left unconnected).

1. Because the strap function is multiplexed with the Serial Port pins, a CMOS transceiver device is recommended for Serial Port functionality; in this case, the value of the external pull-down resistor is 10 KΩ. If, however, a TTL transceiver device is used, the value of the external pull-down resistor must be 470Ω, and since the Serial Port pins are not able to drive this load, the external pull-down resistor must disconnect t_{EPLV} after V_{DD} power-up (see Section 7.4.4 on page 70).

1.3.9 Test and Miscellaneous

Signal	Pin(s)	I/O	Buffer Type	Description
XOR_OUT	22	O	$O_{3/6}$	**XOR Tree Output.** All the device pins (except power, ground and Not Connected pins) are internally connected in a XOR tree structure.
VCORF	13		-	**On-Chip Core Power Converter Filter.** Powers the core logic of all the device modules. An external 0.1 µF ceramic filter capacitor must be connected between this pin and V_{SS}.

1.0 Signal/Pin Connection and Description (Continued)

1.4 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 3 can optionally support internal pull-up (PU) and/or pull-down (PD) resistors. See Section 7.3 for the values of each resistor type.

Table 3. Internal Pull-Up and Pull-Down Resistors

Signal	Pin(s)	Type	Comments
General-Purpose Input/Output (GPIO) Ports			
GPIO00-07	15, 16, 19, 20, 21, 40, 7, 41	PU_{30}	Programmable
GPIO10-11, GPIO14-17	5, 3, 61, 60, 59, 10	PU_{30}	Programmable
GPO12-13	63, 62	PU_{30}	Programmable
GPIO21	29	PU_{80}	Programmable
GPIO20, GPIO23, GPIO24	23, 30	PU_{30}	Programmable
GPO22	27	PU_{80}	Programmable
Strap Configuration and Testability			
BADDR	4	PU_{30}	Strap[1]
$\overline{\text{TEST}}$	63	PU_{30}	Strap[1]
$\overline{\text{TRIS}}$	62	PU_{30}	Strap[1]
Parallel Port			
$\overline{\text{ACK}}$	28	PU_{30}	
$\overline{\text{AFD}}$_$\overline{\text{DSTRB}}$	57	PU_{440}	
BUSY_$\overline{\text{WAIT}}$	26	PD_{120}	
$\overline{\text{ERR}}$	54	PU_{30}	
$\overline{\text{INIT}}$	56	PU_{440}	
PE	25	PU_{220}/ PD_{120}	Programmable
SLCT	24	PD_{30}	
$\overline{\text{SLIN}}$_$\overline{\text{ASTRB}}$	55	PU_{80}	
$\overline{\text{STB}}$_$\overline{\text{WRITE}}$	14	PU_{440}	

1. Active only during V_{DD} Power-Up reset.

2.0 Power, Reset and Clocks

2.1 POWER

2.1.1 Power Planes

The PC87383 has a single 3.3V power source, V_{DD}. Internally, an additional power plane (V_{CORF}) is generated using an on-chip voltage converter. This power plane feeds all the core logic.

2.1.2 Power States

The following terminology is used in this document to describe the power states:

- **Power On** - V_{DD} is active
- **Power Off** - V_{DD} is inactive

2.1.3 Power Connection and Layout Guidelines

The PC87383 requires a power supply voltage of 3.3V ± 10% for the V_{DD} supply. The on-chip Core voltage converter generates a voltage below 3V for the internal logic.

V_{DD} and V_{CORF} use a common ground return marked V_{SS}.

To obtain the best performance, bear in mind the following recommendations.

Ground Connection. The following items must be connected to the ground layer (V_{SS}) as close to the device as possible:

- The ground return (V_{SS}) pins
- The decoupling capacitors of the Main power supply (V_{DD}) pins
- The decoupling capacitor of the on-chip Core power converter (V_{CORF}) pin

Note that a low-impedance ground layer also improves noise isolation.

Decoupling Capacitors. The following decoupling capacitors must be used in order to reduce EMI and ground bounce:

- Main power supply (V_{DD}): Place one 0.1 µF capacitor on each V_{DD}-V_{SS} pin pair, as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the device as possible.
- On-chip Core power converter (V_{CORF}): Place one 0.1 µF ceramic capacitor on the V_{CORF}-V_{SS} pin pair as close to the pin as possible.

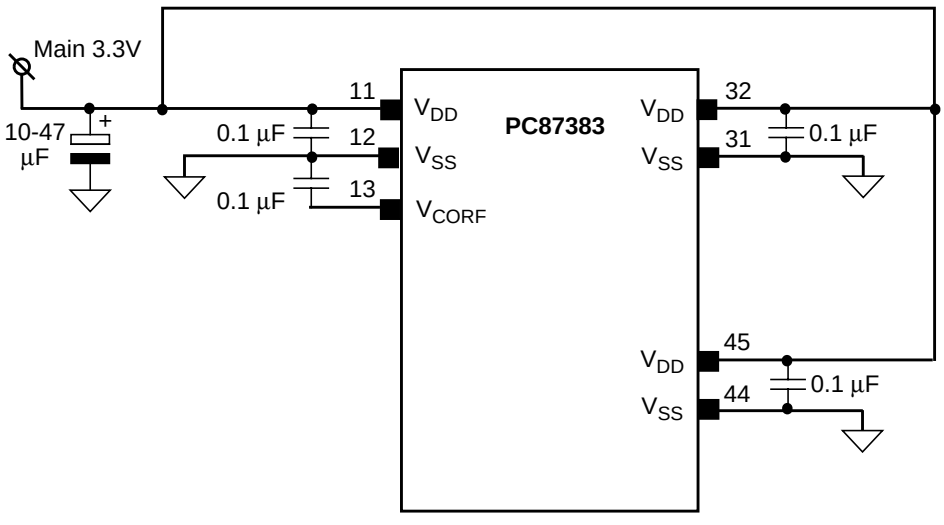


Figure 1. Decoupling Capacitors Connection

2.0 Power, Reset and Clocks (Continued)

2.2 RESET SOURCES AND TYPES

The PC87383 has the following reset sources:

- **V_{DD} Power-Up Reset** - activated when V_{DD} is powered up.
- **Hardware Reset** - activated when the $\overline{\text{LRESET}}$ input is asserted (low)

2.2.1 V_{DD} Power-Up Reset

V_{DD} Power-Up reset is generated by an internal circuit when V_{DD} power is turned on. V_{DD} Power-Up reset time (t_{IRST}) lasts until the $\overline{\text{LRESET}}$ signal is de-asserted. The Hardware reset ($\overline{\text{LRESET}}$) must be asserted for a minimum of 10 ms to ensure that the PC87383 operates correctly.

External devices must wait at least t_{IRST} before accessing the PC87383. If the host processor accesses the PC87383 during this time, the PC87383 LPC interface ignores the transaction (that is, it does not return a SYNC handshake).

V_{DD} Power-Up reset performs the following actions:

- Puts pins with strap options into TRI-STATE and enables their internal pull-up resistors
- Samples the logic levels of the strap pins
- Executes all the actions performed by the Hardware reset; see Section 2.2.2

2.2.2 Hardware Reset

Hardware reset is activated by assertion of $\overline{\text{LRESET}}$ input while V_{DD} is “good”. When V_{DD} power is off, the PC87383 ignores the level of the $\overline{\text{LRESET}}$ input. Hardware reset performs the following actions:

- Resets all lock bits in configuration registers
- Loads default values to all the bits in the Configuration Control.
- Resets all the logical devices.
- Loads default values to all the module registers.

2.3 CLOCK DOMAINS

The PC87383 has two clock domains, as shown in Table 4.

Table 4. Clock Domains of the PC87383

Clock Domain	Frequency	Source	Usage
LPC	Up to 33 MHz	LPC clock input (LCLK)	LPC bus interface and Configuration Registers
48 MHz	48 MHz	On-chip Clock Generator or directly from Clock Input (CLKIN)	Legacy functions (Serial Port, Parallel Port, Infrared)

2.3.1 LPC Domain

The LPC clock signal at the LCLK pin must become valid before the end of the Hardware reset ($\overline{\text{LRESET}}$) (see Section 2.2.2). This clock can be slowed down or stopped using the $\overline{\text{CLKRUN}}$ protocol.

2.3.2 48 MHz Domain

The 48 MHz clock domain is sourced either by the on-chip Clock Generator or directly by the CLKIN input pin. The Clock Generator is fed by applying a clock source at a frequency of 14.31818 MHz. The Clock Generator generates two internal clocks, 24 MHz and 48 MHz. After power-up or Hardware reset, the clock (Clock Generator or external clock) is disabled.

Clock Generator Functional Description

The on-chip Clock Generator starts working when it is enabled by bit 7 of the CLOCKCF register, Index 29h, i.e., when the bit value changes from 0 to 1 (only for 14.31818 MHz clock source). Once enabled, the output clock is frozen to a steady logic level until the clock generator provides a stable output clock that meets all requirements. Then the clock starts toggling.

On Hardware reset, the chip wakes up with the on-chip Clock Generator disabled. The input clock of the Clock Generator may toggle regardless of the state of the $\overline{\text{LRESET}}$ pin. The Clock Generator waits for a toggling input clock.

Bit 4 (read only) of the CLOCKCF register is the Valid Clock Generator status bit. While stabilizing, the output clock is frozen to a steady logic level, and the status bit is cleared to 0 to indicate a frozen clock. When the clock generator is stable, the output clock starts toggling and the status bit is set to 1. The status bit tells the software when the Clock Generator is ready. The software should poll this status bit until it is set (1), and only then activate the UART and the Infrared interface.

The clock generator and its output clock do not consume power when they are disabled.

2.3.3 Chip Power-Up

To ensure proper operation, proceed as follows after power-up:

1. Set bit 5 of the Clock Generator Control register (CLOCKCF) at Index 29h according to the clock source used; see Table 5.
2. Enable the clock. If the clock source is 14.31818 MHz:
   — Poll bit 4 of the CLOCKCF register while the clock generator is stabilizing.
   — When bit 4 of CLOCKCF is set to 1, go to step 3.
3. Enable any module in the chip, as needed.

Table 5. Clock Generator Encoding Options

CLKIN Pin Frequency	CLOCKCF Bit 5
48 MHz	0
14.31818 MHz	1

2.3.4 Specifications

Wake-up time is 33 msec (maximum). This is measured from the time the Clock Generator is enabled until the clock is stable.

Note: The reference clock must be stable at the time the Clock Generator is enabled. Tolerance (long term deviation) of the generator output clock, relative to the input clock, is ±110 ppm. Total tolerance is therefore ± (input clock tolerance + 110 ppm).

2.4 TESTABILITY SUPPORT

The PC87383 supports two testability modes:

- In-Circuit Testing (ICT)
- XOR Tree Testing

2.4.1 ICT

The In-Circuit Testing (ICT) technique, also known as “bed-of-nails”, injects logic patterns to the input pins of the devices mounted on the tested board. It then checks their outputs for the correct logic levels.

The PC87383 supports this testing technique by floating (putting in TRI-STATE) all the device pins. This prevents “back-driving” the PC87383 pins by the ICT tester when a device normally controlled by PC87383 is tested (device inputs are driven by the ICT tester).

2.4.2 XOR Tree Testing

When the PC87383 is mounted on a board, it can be tested using the XOR Tree technique. This test also checks the correct connection of the device pins to the board.

In XOR Tree mode, all PC87383 pins are configured as inputs, except the last pin in the tree, which is the XOR_OUT output. The buffer type of the input pins participating in the XOR tree is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode (see Section 1.3 on page 10). The input pins are chained through XOR gates, as shown in Figure 2. The Not Connected, power and ground pins (NC, VDD, VSS, VCORF) are excluded from the XOR tree.

2.0 Power, Reset and Clocks (Continued)

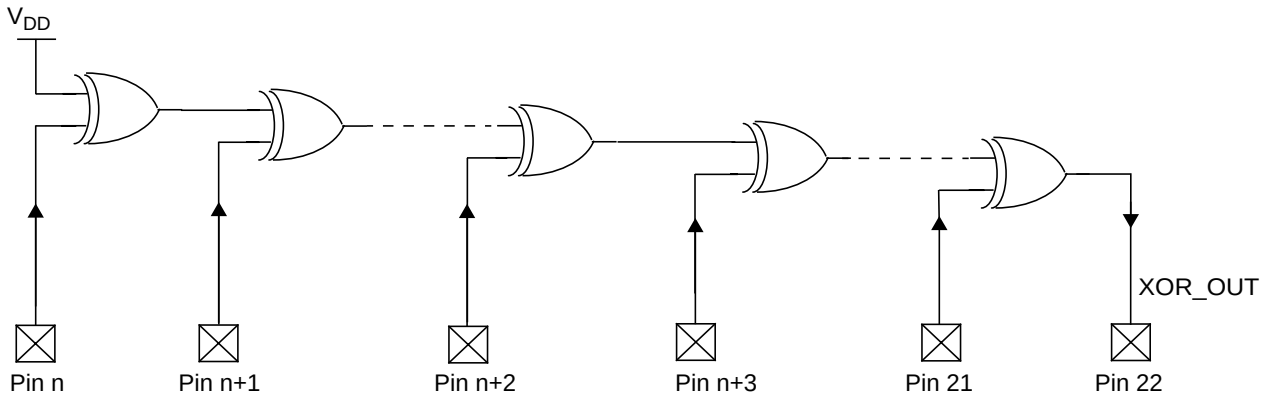


Figure 2. XOR Tree (Simplified Diagram)

The maximum propagation delay through the XOR tree, from the first pin in the chain to XOR_OUT is 200 ns.

2.4.3 Test Mode Entry Sequence

Table 6 shows the decoding values required to enter each test mode. The test modes are decoded from the $\overline{\text{TEST}}$ and $\overline{\text{TRIS}}$ strap pins and are latched into PC87383 on power up.

Table 6. Test Mode Selection

Test Mode	$\overline{\text{TEST}}$	$\overline{\text{TRIS}}$
No Test Mode Selected	1	1
ICT	1	0
XOR Tree	0	1
Reserved exclusively for NSC use	0	0

3.0 Device Architecture and Configuration

The PC87383 comprises a collection of legacy and proprietary functional blocks. Each functional block is described in a separate chapter. This chapter describes the PC87383 structure and provides all logical device specific information, including special implementation of generic blocks, system interface and device configuration.

3.1 OVERVIEW

The PC87383 consists of four logical devices, the host interface, and a central set of configuration registers, all built around a central internal bus. Figure 3 illustrates the blocks and related logic.

The system interface serves as a bridge between the external LPC interface and the internal bus. It supports 8-bit read and write transactions for I/O and DMA, as defined in Intel's *LPC Interface Specification, Revision 1.1*.

The central configuration register set is ACPI compliant and supports a PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard registers, defined in Appendix A of the *Plug and Play ISA Specification, Revision 1.0a* by Intel and Microsoft. All system resources assigned to the functional blocks (I/O address space, DMA channels and IRQ lines) are configured in, and managed by, the central configuration register set. In addition, some function-specific parameters are configurable through the configuration registers and distributed to the functional blocks through special control signals.

3.2 CONFIGURATION STRUCTURE AND ACCESS

The configuration structure is comprised of a set of banked registers which are accessed via a pair of specialized registers.

3.2.1 The Index-Data Register Pair

Access to the PC87383 configuration registers is via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during V_{DD} Power-Up reset, according to the state of the hardware strapping option on the BADDR pin. Table 7 shows the selected base addresses as a function of BADDR.

Table 7. BADDR Strapping Options

BADDR	I/O Address	
	Index Register	Data Register
0	2Eh	2Fh
1 (default)	164Eh	164Fh

The Index register is an 8-bit read/write register located at the selected base address (Base+0). It is used as a pointer to the configuration register file, and holds the index of the configuration register that is currently accessible via the Data register. Reading the Index register returns the last value written to it (or the default of 00h after reset).

The Data register is an 8-bit register (Base+1) used as a data path to any configuration register. Accessing the Data register actually accesses the configuration register that is currently pointed to by the Index register.

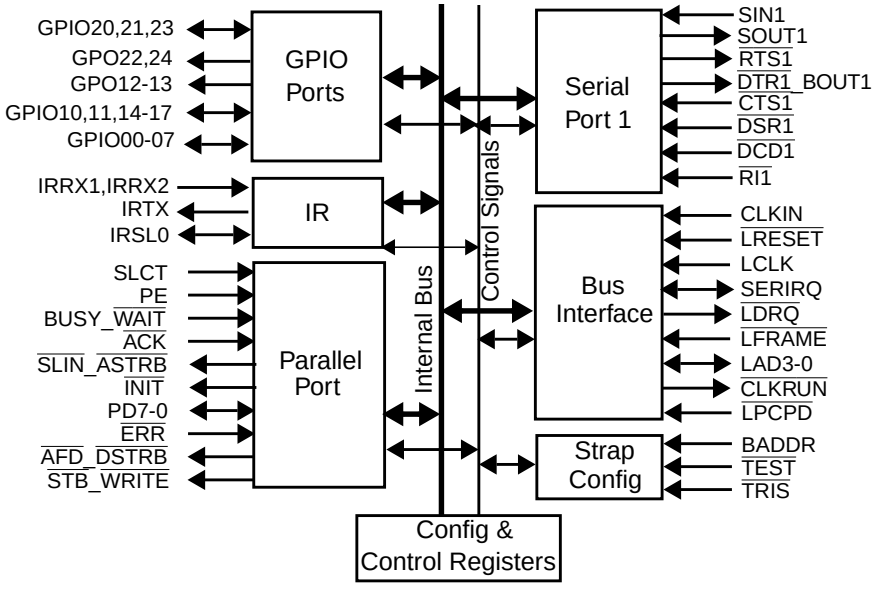


Figure 3. PC87383 Detailed Block Diagram

3.0 Device Architecture and Configuration (Continued)

3.2.2 Banked Logical Device Registers Structure

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 8 shows the LDN values of the PC87383 functional blocks. Any value not listed is reserved.

Figure 4 shows the structure of the standard configuration register file. The LDN and PC87383 configuration registers are not banked and are accessed by the Index-Data register pair only, as described in Section 3.2.1. However, the device control and device configuration registers are duplicated over four banks for four logical devices. Therefore, accessing a specific register in a specific bank is performed by two-dimensional indexing, where the LDN register selects the bank (or logical device) and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher physically accesses the logical device configuration registers currently pointed to by the Index register, within the logical device currently selected by the LDN register.

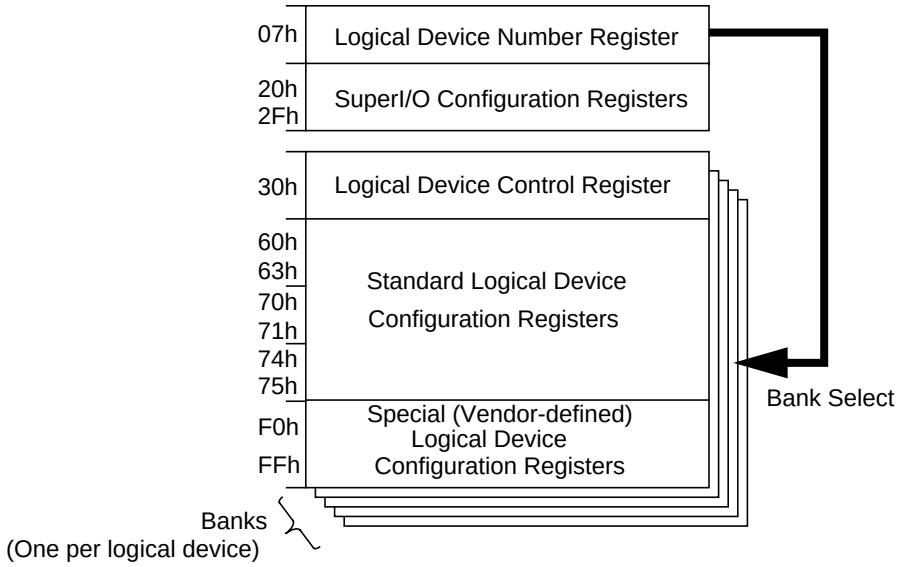


Figure 4. Structure of Standard Configuration Register File

Table 8. Logical Device Number (LDN) Assignments

LDN	Functional Block
01h	Parallel Port (PP)
02h	Infrared (IR)
03h	Serial Port 1 (SP1)
07h	General-Purpose I/O (GPIO) Ports

Write accesses to unimplemented registers (i.e. accessing the Data register while the Index register points to a non-existing register) are ignored; reads return 00h on all addresses, except 74h and 75h (DMA configuration registers), which return 04h (indicating no DMA channel is active). The configuration registers are accessible immediately after reset.

3.0 Device Architecture and Configuration (Continued)

3.2.3 Standard Configuration Register Definitions

In the registers below, any undefined bit is reserved. Unless otherwise noted, the following definitions also hold true:

- All registers are read/write.
- All reserved bits return 0 on reads, except where noted otherwise. To prevent unpredictable results, do not modify these bits. Use read-modify-write to prevent the values of reserved bits from being changed during write.
- Write-only registers must not use read-modify-write during updates.

Table 9. Standard General Configuration Registers

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device. See Table 8 for valid numbers. All other values are reserved.
20h-2Fh	PC87383 Configuration	PC87383 configuration registers and ID registers.

Table 10. Logical Device Activate Register

Index	Register Name	Description
30h	Activate	Bits 7-1: Reserved. Bit 0: Logical device activation control; see Section 3.3 on page 25. 0: Disabled. 1: Enabled.

Table 11. I/O Space Configuration Registers

Index	Register Name	Description
60h	I/O Port Base Address Bits 15-8 Descriptor 0	Indicates selected I/O lower limit address bits 15-8 for I/O Descriptor 0.
61h	I/O Port Base Address Bits 7-0 Descriptor 0	Indicates selected I/O lower limit address bits 7-0 for I/O Descriptor 0.

3.0 Device Architecture and Configuration (Continued)

Table 12. Interrupt Configuration Registers

Index	Register Name	Description
70h	Interrupt Number	Indicates selected interrupt number. Bits 7-4: Reserved. Bits 3-0: These bits select the interrupt number. A value of 1 selects IRQ1. A value of 15 selects IRQ15. IRQ0 is not a valid interrupt selection and represents no interrupt selection. **Note:** Avoid selecting the same interrupt number (except 0) for different logical devices, as it causes the PC87383 to behave unpredictably.
71h	Interrupt Request Type Select	Indicates the type and polarity of the interrupt request number selected in the previous register. If a logical device supports only one type of interrupt, the corresponding bit is read only. Bits 7-2: Reserved. Bit 1: Polarity of interrupt request selected in previous register. 0: Low polarity. 1: High polarity. Bit 0: Type of interrupt request selected in previous register. 0: Edge. 1: Level.

Table 13. DMA Configuration Registers

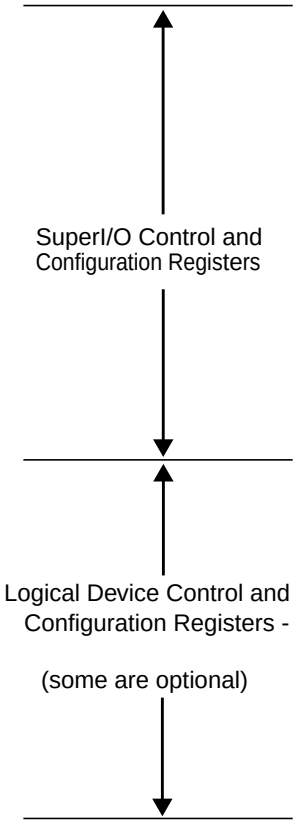
Index	Register Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 of the logical device (0 is the first DMA channel if more than one DMA channel is used). Bits 7-3: Reserved. Bits 2-0: These select the DMA channel for DMA 0, where: - A value of 0, 1, 2, or 3 selects DMA channel 0, 1, 2, or 3, respectively. - A value of 4 indicates that no DMA channel is active. - The values 5-7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different logical devices, as it causes the PC87383 to behave unpredictably.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 of the logical device (1 is the second DMA channel if more than one DMA channel is used). Bits 7-3: Reserved. Bits 2-0: These select the DMA channel for DMA 1, where: - A value of 0, 1, 2, or 3 selects DMA channel 0, 1, 2, or 3, respectively. - A value of 4 indicates that no DMA channel is active. - The values 5-7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different logical devices, as it causes the PC87383 to behave unpredictably.

Table 14. Special Logical Device Configuration Registers

Index	Register Name	Description
F0h-FFh	Logical Device Configuration	Special (vendor-defined) configuration options.

3.0 Device Architecture and Configuration (Continued)

3.2.4 Standard Configuration Registers



Index	Register Name
07h	Logical Device Number
20h	SuperI/O ID
21h	SuperI/O Configuration 1
22h	SuperI/O Configuration 2
23h-25h	Reserved
26h	SuperI/O Configuration 6
27h	SuperI/O Revision ID
28h	Reserved
29h	Clock Generator Control
2Ah - 2Fh	Reserved exclusively for National use
30h	Logical Device Control (Activate)
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
70h	Interrupt Number and Wake-Up on IRQ Enable
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h - FFh	Device Specific Logical Device Configuration 1 to 16

Figure 5. Configuration Register Map

SuperI/O Configuration Registers

The PC87383 configuration registers at Indexes 20h and 27h are used for part identification. The other configuration registers are used for global power management and the selection of pin multiplexing options. For details, see Section 3.7 on page 27.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. See the functional block descriptions in the following sections.

Control

The only implemented control register for each logical device is the Activate register at Index 30h. Bit 0 of the Activate register controls the activation of the associated functional block. Activation enables access to the functional block's registers, and attaches its system resources, which are unassigned as long as it is not activated. Other effects may apply on a function-specific basis (such as clock enable and active pinout signaling). Access to the configuration register of the logical device is enabled even when the logical device is not activated.

Standard Configuration

The standard configuration registers manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60-61h, holding the first 16-bit base address for the register set of the functional block. An optional 16-bit second base-address (descriptor 1) at Index 62-63h is used for logical devices with more than one continuous register set. Interrupt Number (Index 70h) and IRQ Type Select (Index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (Index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (Index 75h) allocates a second DMA channel, where applicable.

3.0 Device Architecture and Configuration (Continued)

Special Configuration

The vendor-defined registers, starting at Index F0h, control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, and non-standard extensions to generic functions.

3.2.5 Default Configuration Setup

In the event of a V_{DD} Power-Up or Hardware reset, the PC87383 wakes up with the following default configuration setup:

- The configuration base address is 2Eh or 164Eh, according to the BADDR strap pin value, as shown in Table 7 on page 19.
- All logical devices are disabled.
- All multiplexed GPIO pins are configured to their respective default function. When configured as GPIO, they have an internal static pull-up (default direction is input).
- The legacy devices (Serial Port, Parallel Port and IR) are assigned with their legacy system resource allocation.
- National Semiconductor proprietary functions are not assigned with any default resources, and the default values of their base addresses are all 00h.

See Section 2.2 on page 16 for more details on PC87383 reset sources and types.

3.0 Device Architecture and Configuration (Continued)

3.3 MODULE CONTROL

3.3.1 Module Enable/Disable

Module control is performed primarily through the Activation bit (bit 0 of Index 30h) of each logical device. The operation of each module can be controlled by the host through the LPC bus.

Module enable/disable by the host through the LPC bus is controlled by the following bits:

- Activation bit (bit 0) in Index 30h of the Standard configuration registers; see Section 3.2.3 on page 21.
- Fast Disable bit in SIOCF6 register; for the Serial Port 1, Parallel Port and IR modules only; see Section 3.7.4 on page 30.
- Global Enable bit (GLOBEN) in SIOCF1 register; see Section 3.7.2 on page 28.

A module is enabled only if all of these bits are set to their “enable” value.

When a legacy (SP1, Parallel Port or IR) module is disabled, the following takes place:

- The host system resources of the logical device (IRQ, DMA and runtime address range) are unassigned.
- Access to the standard- and device-specific Logical Device configuration registers through the LPC bus remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).
- The module’s internal clock is disabled (the module is not functional) to lower the power consumption.

When the GPIO module is disabled, the following takes place:

- The host system resources of the logical device (IRQ and runtime address range) are unassigned.
- Access to the standard- and device-specific Logical Device configuration registers through the LPC bus remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).
- The module is functional.

3.3.2 Floating Module Output

The pins of the Legacy modules (Serial Port, Parallel Port, Infrared) can be floated. When the TRI-STATE Control bit (bit 0) is set in the specific module configuration register (at Index F0h of the specific logical device in the configuration space) **and** the module is disabled (see Section 3.3.1), the module output signals are floated and the I/O signals are configured as inputs (note that the logic level at the inputs is ignored by the module, which is disabled).

Figure 6 shows the control mechanism for floating the pins of a Legacy module.

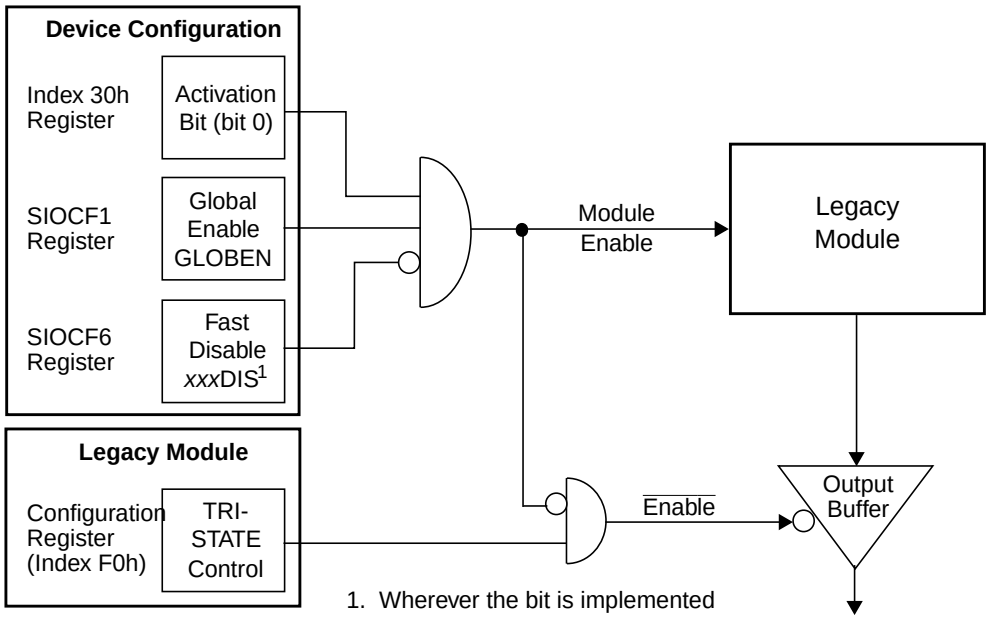


Figure 6. Control of Floating Legacy Module Pins

3.0 Device Architecture and Configuration (Continued)

3.4 INTERNAL ADDRESS DECODING

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers varies for each logical device.

The lower 1, 2, 3, 4 or 5 address bits are decoded within the functional block to determine the offset of the accessed register within the logical device's I/O range of 2, 4, 8, 16 or 32 bytes, respectively. The remaining bits are matched with the base address register to decode the entire I/O range allocated to the logical device. Therefore the lower bits of the base address register are forced to 0 (read only), and the base address is forced to be 2, 4, 8, 16 or 32 byte-aligned, according to the size of the I/O range.

The base addresses of the Serial Port 1 and FIR modules are limited to the I/O address range of 00h to 7FXh only (bits 11-15 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses of the non-legacy logical devices are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 10 in the Parallel Port). For more details, see the description of the base address register for each logical device.

3.5 PROTECTION

The PC87383 provides features to protect the hardware configuration from changes made by application software running on the host.

The protection is activated by the software setting a "sticky" lock bit. Each lock bit protects a group of configuration bits located either in the same register or in different registers. When the lock bit is set, the lock bit and all the protected bits become read only and cannot be further modified by the host through the LPC bus. All the lock bits are reset by Hardware reset, thus unlocking the protected configuration bits.

The bit locking protection mechanism is optional.

The protected groups of configuration bits are described below.

3.5.1 Multiplexed Pins Configuration Lock

Protects the configuration of all the multiplexed device pins.

Lock bit: LOCKMCF in SIOCF1 register (Device Configuration).

Protected bits: LOCKMCF and IOWAIT (in SIOCF1 register) and all bits in SIOCF2 register (Device Configuration).

3.5.2 GPIO Ports Configuration Lock

Protects the configuration (but not the data) of all the GPIO Ports.

Lock bit: LOCKGCF in SIOCF1 register (Device Configuration).

Protected bits for each GPIO Port: LOCKGCF in SIOCF1 register, and all bits in GPCFG register (except LOCKCFP bit) and GPEVR register (Device Configuration).

3.5.3 Fast Disable Configuration Lock

Protects the Fast Disable bits for all the Legacy modules.

Lock bit: LOCKFDS in SIOCF6 register (Device Configuration).

Protected bits: All bits in SIOCF6 register (except General-Purpose Scratch bits) and GLOBEN bit in SIOCF1 register (Device Configuration).

3.5.4 Clock Control Lock

Protects the Clock Generator control bits.

Lock bit: LOCKCCF in CLOCKCF register (Device Configuration).

Protected bits: All bits in CLOCKCF register (Device Configuration).

3.5.5 GPIO Ports Lock

Protects the configuration **and** data of all the GPIO Ports.

Lock bit: LOCKCFP in GPCFG register, for each GPIO Port (Device Configuration).

Protected bits for each GPIO Port:
PUPCTL, OUTTYPE and OUTENA in GPCFG register; the corresponding bit (to the port pin) in GPDO register (GPIO Ports).

3.0 Device Architecture and Configuration (Continued)

3.6 REGISTER TYPE ABBREVIATIONS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write.
- RO = Read Only.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

3.7 SUPERI/O CONFIGURATION REGISTERS

This section describes the SuperI/O configuration and ID registers (those registers with first level indexes in the range of 20h-2Eh). See Table 15 for a summary and directory of these registers.

Note: Set the configuration registers to enable functions or signals that are relevant to the specific device. The values of fields that select functions, or signals, that are excluded from a specific device are treated as reserved and should not be selected.

Table 15. SuperI/O Configuration Registers

Index	Mnemonic	Register Name	Type	Section
20h	SID	SuperI/O ID	RO	3.7.1
21h	SIOCF1	SuperI/O Configuration 1	R/W	3.7.2
22h	SIOCF2	SuperI/O Configuration 2	R/W	3.7.3
23h-25h	Reserved for National use			
26h	SIOCF6	SuperI/O Configuration 6	R/W	3.7.4
27h	SRID	SuperI/O Revision ID	RO	3.7.5
29h	CLOCKCF	Clock Generator Control Register	R/W	3.7.6
2Ah - 2Fh	Reserved exclusively for National use			

3.7.1 SuperI/O ID Register (SID)

This register contains the identity number of the chip. The PC87383 family is identified by the value F4h.

Location: Index 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Chip ID**							
Reset	F4h							

3.0 Device Architecture and Configuration (Continued)

3.7.2 SuperI/O Configuration 1 Register (SIOCF1)

Location: Index 21h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKMCF**	**LOCKGCF**	**Reserved**		**IOWAIT**		**Reserved**	**GLOBEN**
Reset	0	0	0	1	0	0	0	1

Bit	Type	Description
7	R/W1S	**LOCKMCF (Lock Multiplexing Configuration).** When set to 1, this bit locks the configuration of registers SIOCF1 and SIOCF2 by disabling writing to all bits in these registers (including the LOCKMCF bit itself), except for the LOCKGCF and GLOBEN bits in SIOCF1. Once set, this bit can only be cleared by Hardware reset. 0: R/W bits are enabled for write (default). 1: All bits are RO.
6	R/W1S	**LOCKGCF (Lock GPIO Pins Configuration).** When set to 1, this bit locks the configuration registers of all GPIO pins (see Section 3.11.3 on page 37) by disabling writes to all their bits (including the LOCKGCF bit itself). The locked registers include the GPCFG (except LOCKCFP bit) and GPEVR registers of all GPIO pins. Once set, this bit can only be cleared by Hardware reset. 0: R/W bits are enabled for write (default). 1: All bits are RO.
5-4		**Reserved**. These bits must be '01'.
3-2	R/W or RO	**IOWAIT (Number of I/O Wait States).** These bits set the number of wait states for I/O transactions through the LPC bus. **Bits 3 2 Number of Wait States** 0 0: 0 (default) 0 1: 2 1 0: 6 1 1: 12
1		**Reserved**. This bit must be 0.
0	R/W or RO	**GLOBEN (Global Device Enable).** This bit makes it possible to disable all logical devices by setting a single bit (to 0). In addition, when the bit is set to 1, it enables the operation of all the logical devices of the PC87383, as long as the logical device is itself enabled (see Table 8 on page 20). The behavior of the different devices is explained in Section 3.3 on page 25. 0: All logical devices in the PC87383 are disabled and their resources are released. 1: Enables each PC87383 logical device that is itself enabled (default); see Section 3.3.1 on page 25.

3.0 Device Architecture and Configuration (Continued)

3.7.3 SuperI/O Configuration 2 Register (SIOCF2)

This register is reset by hardware to 63h.

Location: Index 22h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**PPSEL**	**Reserved**	**CLKRUNSEL**	**Reserved**	**LPCPDSEL**	**Reserved**	**IRRX2SEL**	**SP1SEL**
Reset	0	1	1	0	0	0	1	1

Bit	Description
7	**PPSEL (Parallel Port Selection Control).** Selects the functions connected to pins 28 and 30. 0: GPIO24, GPIO23 (default). 1: $\overline{\text{ACK}}$, PD7.
6	**Reserved.**
5	**CLKRUNSEL ($\overline{\text{CLKRUN}}$ Selection Control).** Selects the functions connected to pin 27. This bit is reset on V_{DD} power-up only. 0: GPO22. 1: $\overline{\text{CLKRUN}}$ (default).
4	**Reserved.**
3	**LPCPDSEL ($\overline{\text{LPCPD}}$ Selection Control).** Selects the function connected to pin 29. This bit is reset on V_{DD} power-up only. 0: GPIO21 (default) 1: $\overline{\text{LPCPD}}$
2	**Reserved.**
1	**IRRX2SEL (IRRX2 Selection Control).** Selects the function connected to pin 10. 0: GPIO17. 1: IRRX2_IRSL0 (default).
0	**SP1SEL (Serial Port 1 Selection Control).** Selects the function connected to pins 5, 3, 63, 62, 61, 60 and 59. 0: GPIO10-GPIO16. 1: $\overline{\text{RI1}}$, $\overline{\text{DTR1}}$_BOUT1, $\overline{\text{CTS1}}$, SOUT1, $\overline{\text{RTS1}}$, SIN1, $\overline{\text{DSR1}}$, $\overline{\text{DCD1}}$ (default).

Note: During initialization, bits 6 and 4 must be initialized to 0 to allow correct operation of the chip.

3.0 Device Architecture and Configuration (Continued)

3.7.4 SuperI/O Configuration 6 Register (SIOCF6)

This register provides a fast way to disable one or more modules without having to access the Activate register of each; see Section 3.3.1 on page 25.

Location: Index 26h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKFDS**	**General-Purpose Scratch**		**Reserved**	**SER1DIS**	**IRDIS**	**PARPDIS**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCKFDS (Lock Fast Disable Configuration).** When set to 1, this bit locks itself, SER1DIS, PARPDIS and IRDIS bits in this register and GLOBEN bit in SIOCF1 register by disabling writing to all of these bits. Once set, this bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default). 1: All bits are RO.
6-5	R/W	**General-Purpose Scratch.**
4		**Reserved.**
3	R/W or RO	**SER1DIS (Serial Port 1 Disable).** 0: Enabled or Disabled, according to Activation bit (default). 1: Disabled.
2	R/W or RO	**IRDIS (Infrared Disable).** 0: Enabled or Disabled, according to Activation bit (default). 1: Disabled.
1	R/W or RO	**PARPDIS (Parallel Port Disable).** When set to 1, this bit forces the Parallel Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (Index 30). 0: Enabled or Disabled, according to Activation bit (default). 1: Disabled.
0		**Reserved.**

3.7.5 SuperI/O Revision ID Register (SRID)

This register contains the ID number of the specific family member (Chip ID) and the chip revision number (Chip Rev).

Location: Index 27h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Chip ID**			**Chip Rev**				
Reset	0	0	0	X	X	X	X	X

Bit	Description
7-5	**Chip ID.**
4-0	**Chip Rev.** These bits identify the device revision.

3.0 Device Architecture and Configuration (Continued)

3.7.6 Clock Generator Control Register (CLOCKCF)

Location: Index 29h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**CKEN**	**Reserved**	**CK48SEL**	**CKVALID**	**LOCKCCF**	**Reserved**		
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W or RO	**CKEN (Clock Enable).** This bit enables the internal clock of PC87383. If the clock source selected by CK48SEL bit is the Clock Generator, this bit enables the Clock Generator. Otherwise it enables the path from the CLKIN input pin. 0: Clock disabled (default). 1: Clock enabled.
6		**Reserved.**
5	R/W or RO	**CK48SEL (48 MHz Clock Select).** Selects the source of the internal 48 MHz clock. 0: The source of the internal 48 MHz clock is CLKIN pin (default). Use when CLKIN pin is connected to 48 MHz clock source. 1: The source of the internal 48 MHz clock is the Clock Generator. Use when CLKIN pin is connected to 14.31818 MHz clock source.
4	RO	**CKVALID (Valid Clock Generator, Clock Status).** This bit indicates the status of the on-chip, 48 MHz Clock Generator and controls the generator output clock signal. The PC87383 modules using this clock may be enabled (see Section 3.3.1 on page 25) only after this bit is read high (generator clock is valid). 0: Generator output clock frozen (default). 1: Generator output clock active (stable and toggling).
3	R/W1S	**LOCKCCF (Lock Clock Configuration).** When set to 1, this bit locks the configuration register CLOCKCF by disabling writing to all its bits (including to the LOCKCCF bit itself). Once set, this bit can be cleared by Hardware reset. 0: The R/W bits are enabled for write (default). 1: All the bits are Read-Only.
2-0		**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.8 PARALLEL PORT (PP) CONFIGURATION

3.8.1 General Description

The PC87383 Parallel Port supports all IEEE1284 standard communication modes: Compatibility (also known as Standard or SPP), Bi-directional (known also as PS/2), FIFO, EPP (also known as mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers (see Section 6.1 on page 49):

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in Extended ECP mode.
- A group of four registers, used only in Extended ECP mode, is accessed by a second level offset.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. The Parallel Port functional block registers are shown in Section 6.1 on page 49.

3.8.2 Logical Device 1 (PP) Configuration

Table 16 lists the configuration registers that affect the Parallel Port. Only the last register (F0h) is described here. See Sections 3.2.3 and 3.2.4 for descriptions of the other configuration registers.

Table 16. Parallel Port Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate (see Section 3.3.1 on page 25).	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, ‘00000’. Bit 2 (for A10) must be ‘0’.	R/W	02h
61h	Base Address LSB register. Bits 1 and 0 (A1 and A0) are read only, ‘00’. For ECP mode 4 (EPP) or when using Extended registers, bit 2 (A2) must also be ‘0’.	R/W	78h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	07h
71h	Interrupt Type: - Bits 7-2 are read only. - Bit 1 is a read/write bit. - Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode. This bit is set to 1 (level interrupt) in Extended mode and cleared (edge interrupt) in all other modes.	R/W	02h
74h	DMA Channel Select.	R/W	04h
75h	Report no second DMA assignment.	RO	04h
F0h	Parallel Port Configuration register.	R/W	F2h

3.0 Device Architecture and Configuration (Continued)

3.8.3 Parallel Port Configuration Register

This register is reset to F2h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Parallel Port Mode Select**			**Extended Register Access**	**Reserved**		**Power Mode Control**	**TRI-STATE Control**
Reset	1	1	1	1	0	0	1	0

Bit	Description
7-5	**Parallel Port Mode Select.** **Bits 7 6 5 Mode** 0 0 0: SPP-Compatible mode. PD7-0 are always output signals 0 0 1: SPP Extended mode. PD7-0 direction is controlled by software 0 1 0: EPP 1.7 mode 0 1 1: EPP 1.9 mode 1 0 0: ECP mode (IEEE1284 register set), with no support for EPP mode 1 0 1: Reserved 1 1 0: Reserved 1 1 1: ECP mode (IEEE1284 register set), with EPP mode selectable as mode “100” (default) Selection of EPP 1.7 or 1.9 in ECP mode “100” is controlled by bit 4 of the Control2 configuration register of the Parallel Port at offset 02h. **Note**: Before setting bits 7-5, enable the Parallel Port and set CTR/DCR (at base address + 2) to C4h.
4	**Extended Register Access.** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored). 1: Registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports runtime configuration within the Parallel Port address space (default).
3-2	**Reserved.**
1	**Power Mode Control.** When the logical device is active: 0: Parallel Port clock disabled. ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel Port clock enabled. All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 25). 0: Normal outputs (default). 1: TRI-STATE outputs when the logical device is inactive.

3.0 Device Architecture and Configuration (Continued)

3.9 INFRARED CONFIGURATION

3.9.1 Logical Device 2 (IR) Configuration

Table 17 lists the configuration registers that affect the Infrared. Only the last register (F0h) is described here. See Sections 3.2.3 and 3.2.4 for descriptions of the other registers.

Table 17. Infrared Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 2 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	02h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	DMA Channel Select 0 (RX_DMA)	R/W	04h
75h	DMA Channel Select 1 (TX_DMA)	R/W	04h
F0h	Infrared Configuration register	R/W	02h

3.9.2 Infrared Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable.** Enables bank switching for Infrared. 0: All attempts to access the extended registers in Infrared are ignored (default). 1: Enables bank switching for Infrared.
6-3	**Reserved.**
2	**Busy Indicator.** This read-only bit can be used by power management software to decide when to power down the Infrared logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Infrared clock disabled. The output signals are set to their default states. Registers are maintained (unlike Active bit in Index 30, which also prevents access to Infrared registers). 1: Normal power mode Infrared clock enabled. Infrared is functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. One exception is the IRTX pin, which is driven to 0 when Infrared is inactive and is not affected by this bit. 0: TRI-STATE disabled (default). 1: TRI-STATE enabled.

3.0 Device Architecture and Configuration (Continued)

3.10 SERIAL PORT 1 CONFIGURATION

3.10.1 Logical Device 3 (SP1) Configuration

Table 18 lists the configuration registers that affect the Serial Port 1. Only the last register (F0h) is described here. See Sections 3.2.3 and 3.2.4 for descriptions of the other registers.

Table 18. Serial Port 1 Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 3 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	Report no DMA Assignment.	RO	04h
75h	Report no DMA Assignment.	RO	04h
F0h	Serial Port 1 Configuration register.	R/W	02h

3.10.2 Serial Port 1 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable.** Enables bank switching for Serial Port 1. 0: Disabled (default). 1: Enabled.
6-3	**Reserved.**
2	**Busy Indicator.** This read-only bit can be used by power management software to decide when to power down the Serial Port 1 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 1 clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Register values are maintained (unlike Active bit in Index 30, which also prevents access to Serial Port 1 registers). 1: Normal power mode Serial Port 1 clock enabled. Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: TRI-STATE disabled (default). 1: TRI-STATE enabled.

3.0 Device Architecture and Configuration (Continued)

3.11 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS CONFIGURATION

3.11.1 General Description

The GPIO functional block includes 21 pins,arranged in three 8-bit ports (ports 0, 1 and 2):

- Port 0 contains eight GPIOE pins (i.e., GPIO pins with event detection).
- Port 1 contains six GPIOE pins and two GPO pins.
- Port 2 contains three GPIO pins (i.e., GPIO pins without event detection).

All pins in port 0 and 1 have full event detection capability, enabling them to trigger the assertion of IRQ signals. Pins in port 2 do not have event detection capability. The runtime registers associated with the three ports are arranged in the GPIO address space as shown in Table 19. The GPIO base address is 16-byte aligned. Address bits 3-0 are used to indicate the register offset.

Table 19. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Register Name	Port	Type
00h	GPDO0	GPIO Data Out 0	0	R/W
01h	GPDI0	GPIO Data In 0		RO
02h	GPEVEN0	GPIO Event Enable 0		R/W
03h	GPEVST0	GPIO Event Status 0		R/W1C
04h	GPDO1	GPIO Data Out 1	1	R/W
05h	GPDI1	GPIO Data In 1		RO
06h	GPEVEN1	GPIO Event Enable 1		R/W
07h	GPEVST1	GPIO Event Status 1		R/W1C
08h	GPDO2	Data Out 2	2	R/W
09h	GPDI2	Data In 2		RO

3.11.2 Implementation

The standard GPIO port with event detection capability (such as port 0, and port 1 bits 0, 1, 4, 5, 6, and 7) has four runtime registers. Each pin is associated with a GPIO Pin Configuration register that includes seven configuration bits. Port 2 is a non-standard port that does not support event detection, and therefore differs from the generic model as follows:

- It has two runtime registers for basic functionality: GPDO2 and GPDI2. Event detection registers GPEVEN2 and GPEVST2 are not available.
- Only bits 3-0 are implemented in the GPIO Pin Configuration register of port 2. Bits 6-4, associated with the event detection functionality, are reserved.

3.0 Device Architecture and Configuration (Continued)

3.11.3 Logical Device 7 (GPIO) Configuration

Table 20 lists the configuration registers that affect the GPIO. Only the last three registers (F0h - F2h) are described here. See Sections 3.2.3 and 3.2.4 for a detailed description of the other registers.

Table 20. GPIO Configuration Register

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 7 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register.	R/W	00h
61h	Base Address LSB register. Bits 3-0 (for A3-0) are read only, 0000b.	R/W	00h
70h	Interrupt Number register.	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment.	RO	04h
75h	Report no DMA assignment.	RO	04h
F0h	GPIO Pin Select register (GPSEL).	R/W	00h
F1h	GPIO Pin Configuration register (GPCFG).	Varies per bit	04h or 44h[1]
F2h	GPIO Pin Event Routing register (GPEVR).	R/W or RO	01h

1. Depending on port number

Figure 7 shows the organization of these registers.

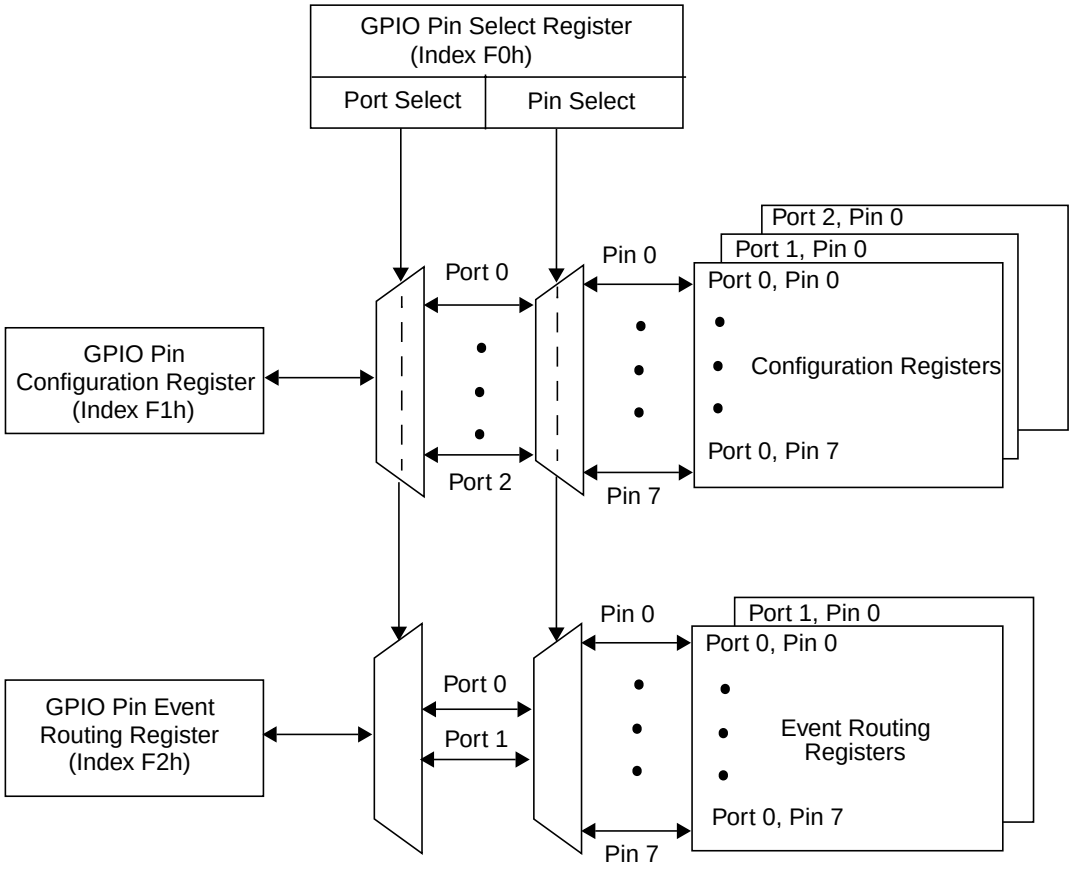


Figure 7. Organization of GPIO Pin Registers

3.0 Device Architecture and Configuration (Continued)

3.11.4 GPIO Pin Select Register (GPSEL)

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO Pin Configuration register). It is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**PORTSEL**		**Reserved**	**PINSEL**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5-4	**PORTSEL (Port Select).** These bits select the GPIO port to be configured: **Bits 5 4 GPIO Port** 0 0: Port 0 (default) 0 1: Port 1 1 0: Port 2 1 1: Reserved
3	**Reserved.**
2-0	**PINSEL (Pin Select).** These bits select the GPIO pin to be configured in the selected port: 000, 001,... 111: Binary value of the pin number, 0, 1,... 7 respectively (default=0). Only values that correspond to implemented GPIO pins are legal; for example, for GPIO11, GPO13, and GPIO17, the value of GPIO11 (Port 1, bit 1) is '001', the value of GPO13 (Port 1, bit 3) is '011', and the value of GPIO17 (Port 1, bit 7) is '111', and only these three values would be legal.

3.11.5 GPIO Pin Configuration Register (GPCFG)

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register (GPSEL). All the GPIO Pin registers that are accessed via this register have a common bit structure, as shown below. This register is reset by hardware to 44h for ports 0 and 1, and to 04h for port 2.

Location: Index F1h

Type: Varies per bit

Port 0 and Port 1, bits 0, 1, 4, 5, 6, and 7 (with event detection capability)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**EVDBNC**	**EVPOL**	**EVTYPE**	**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	0	1	0	0	0	1	0	0

Port 1, bits 2 and 3 (without event detection capability)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	0	1	0	0	0	1	0	0

Port 2 (without event detection capability), bits 0-4

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	0	0	0	0	0	1	0	0

3.0 Device Architecture and Configuration (Continued)

Bit	Type	Description
7	-	**Reserved.**
6	R/W or RO	**EVDBNC (Event Debounce Enable).** (Ports 0 and 1 with event detection capability). Enables transferring the signal only after a predetermined debounce period. 0: Disabled. 1: Enabled (default). **Reserved.** (Port 2 and Port 1 - bits 2 and 3).
5	R/W or RO	**EVPOL (Event Polarity).** (Ports 0 and 1 with event detection capability). This bit defines the polarity of the signal that issues an interrupt from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default). 1: Rising edge or high level input. **Reserved.** (Port 2). Always 0.
4	R/W or RO	**EVTYPE (Event Type).** (Ports 0 and 1 with event detection capability). This bit defines the type of the signal that issues an interrupt from the corresponding GPIO pin (edge or level). 0: Edge input (default). 1: Level input. **Reserved.** (Port 2). Always 0.
3	R/W1S	**LOCKCFP (Lock Configuration of Pin).** When set to 1, this bit locks the GPIO pin configuration and data (see also Section 5.4 on page 45) by disabling writing to itself, to GPCFG register bits PUPCTL, OUTTYPE and OUTENA, and to the corresponding bit in GPDO register. Once set, this bit can only be cleared by Hardware reset. 0: R/W bits are enabled for write (default). 1: All bits are RO.
2	R/W or RO	**PUPCTL (Pull-Up Control).** This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals. 0: Disabled. 1: Enabled (default).
1	R/W or RO	**OUTTYPE (Output Type).** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default). 1: Push-pull.
0	R/W or RO	**OUTENA (Output Enable).** This bit indicates the GPIO pin output state. It has no effect on the input path. 0: TRI-STATE (default). 1: Output enabled.

3.0 Device Architecture and Configuration (Continued)

3.11.6 GPIO Event Routing Register (GPEVR)

This register enables the routing of the GPIO event to IRQ signals. It is implemented only for ports 0,1 which have event detection capability. This register is reset by hardware to 00h.

Location: Index F2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**EV2IRQ**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Reserved.**
0	**EV2IRQ (Event to IRQ Routing).** Controls the routing of the event from the selected GPIO pin to IRQ (see Section 5.3.2 on page 44). 0: Disabled (default). 1: Enabled.

4.0 LPC Bus Interface

4.1 OVERVIEW

The LPC host Interface supports 8-bit I/O Read and Write and 8-bit DMA transactions, as defined in Intel's *LPC Interface Specification, Revision 1.1*.

4.2 LPC TRANSACTIONS

The LPC Interface of the PC87383 can respond to the following LPC transactions:

- 8-bit I/O read and write cycles
- 8-bit DMA read and write cycles
- DMA request cycles

4.3 $\overline{\text{CLKRUN}}$ FUNCTIONALITY

The PC87383 supports the $\overline{\text{CLKRUN}}$ signal, which is implemented according to the specification in *PCI Mobile Design Guide*, *Revision 1.1,* December 18, 1998. The PC87383 supports operation with both a slow and stopped clock in ACPI state S0 (when the system is active but is not being accessed). In the following cases, the PC87383 drives the $\overline{\text{CLKRUN}}$ signal low to force the LPC bus clock into full speed operation:

- An IRQ is pending internally, waiting to be sent through the serial IRQ.
- A DMA request is pending internally, waiting to be sent through the serial DMA.

Note: When the $\overline{\text{CLKRUN}}$ signal is not in use, the PC87383 assumes a valid clock on the LCLK pin.

4.4 INTERRUPT SERIALIZER

The Interrupt Serializer translates parallel interrupt request signals received from internal IRQ sources, into serial interrupt request data transmitted over the SERIRQ bus.

The internal IRQs are fed into a Mapping, Enable and Polarity Control block, which maps them to their associated IRQ slots. The IRQs are then fed into the Interrupt Serializer, where they are translated into serial data and transmitted over the SERIRQ bus.

The same slot cannot be shared among different interrupt sources in the device.

5.0 General-Purpose Input/Output (GPIO) Port

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For the device specific implementation, see Section 3.11 on page 36.

5.1 OVERVIEW

The GPIO port is an 8-bit port, which is based on eight pins. It features:

- Software capability to manipulate and read pin levels
- Controllable system notification by several means based on the pin level or level transition
- Ability to capture and manipulate events and their associated status
- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Pin Configuration registers, mapped in the Device Configuration space. These registers are used to statically set up the logical behavior of each pin. There are two 8-bit registers for each GPIO pin.
- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Event Enable (GPEVEN) and GPIO Event Status (GPEVST). These registers are mapped in the GPIO device I/O space (which is determined by the base address registers in the GPIO Device Configuration). They are used to manipulate and/or read the pin values, and to control and handle system notification. Each runtime register corresponds to the 8-pin port, such that bit n in each one of the four registers is associated with GPIOXn pin, where X is the port number.

Each GPIO pin is associated with ten configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 8.

The functionality of the GPIO port is divided into basic functionality, which includes the manipulation and reading of the GPIO pins, and enhanced functionality. Basic functionality is described in Section 5.2. Enhanced functionality, which includes event detection and system notification, is described in Section 5.3.

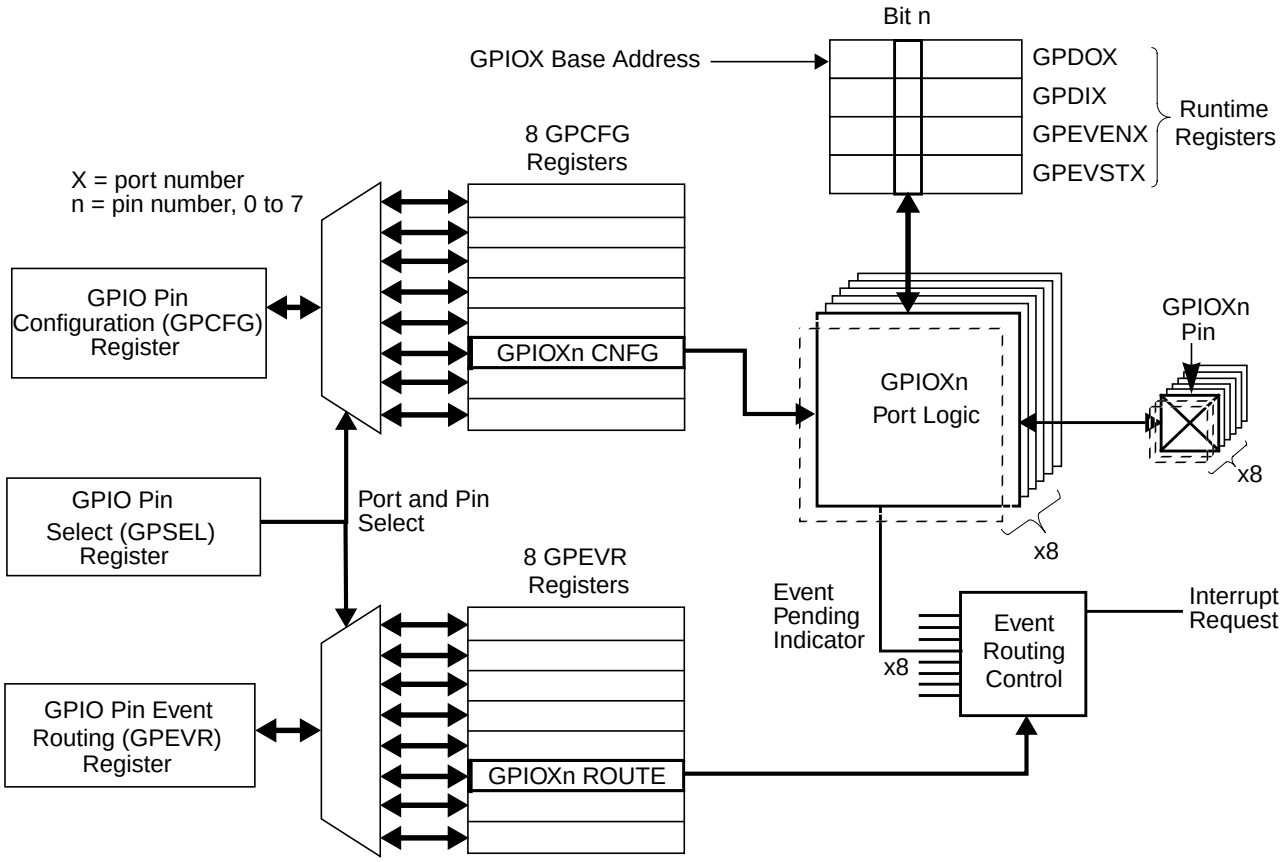


Figure 8. GPIO Port Architecture

5.0 General-Purpose Input/Output (GPIO) Port (Continued)

5.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI. The configuration and operation of a single GPIOXn pin (pin n in port X) is shown in Figure 9.

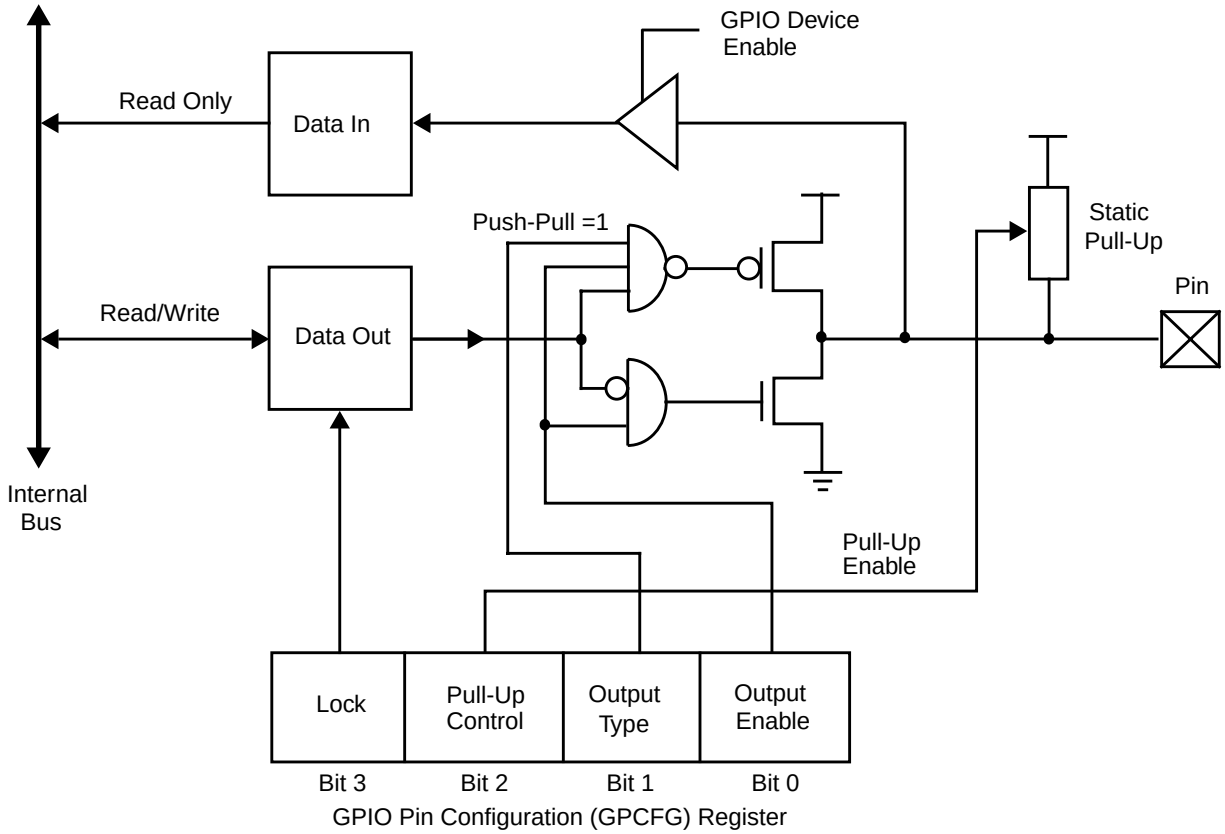


Figure 9. GPIO Basic Functionality

5.2.1 Configuration Options

The GPCFG register controls the following basic configuration options:

- Port Direction - Controlled by the Output Enable bit (bit 0).
- Output Type - Push-pull vs. open-drain. It is controlled by Output Buffer Type (bit 1) by enabling/disabling the pull-up portion of the output buffer.
- Weak Static Pull-Up - May be added to any type of port (input, open-drain or push-pull). It is controlled by Pull-Up Control (bit 2).
- Pin Lock - GPIO pin may be locked to prevent any changes in the output value and/or the output characteristics. The lock is controlled by Lock (bit 3). It disables writes to the GPDO register bits, and to bits 0-3 of the GPCFG register (Including the Lock bit itself). Once locked, it can be released by Hardware reset only.

5.2.2 Operation

The value that is written to the GPDO register is driven to the pin if the output is enabled. Reading from the GPDO register returns its contents, regardless of the pin value or the port configuration. The GPDI register is a read-only register. Reading from the GPDI register returns the pin value, regardless of what is driving it (the port itself, configured as an output port, or the external device when the port is configured as an input port). Writing to this register is ignored.

Activation of the GPIO port is controlled by an external device-specific configuration bit (or a combination of bits). When the port is inactive, access to GPDI and GPDO registers is disabled. However, there is no change in the port configuration and in the GPDO value, and hence there is no effect on the outputs of the pins.

5.0 General-Purpose Input/Output (GPIO) Port (Continued)

5.3 EVENT HANDLING AND SYSTEM NOTIFICATION

The enhanced GPIO port supports system notification based on event detection. This functionality is based on six configuration bits and a bit slice of runtime registers GPEVEN and GPEVST. The configuration and operation of the event detection capability is shown in Figure 10. System notification is shown in Figure 11.

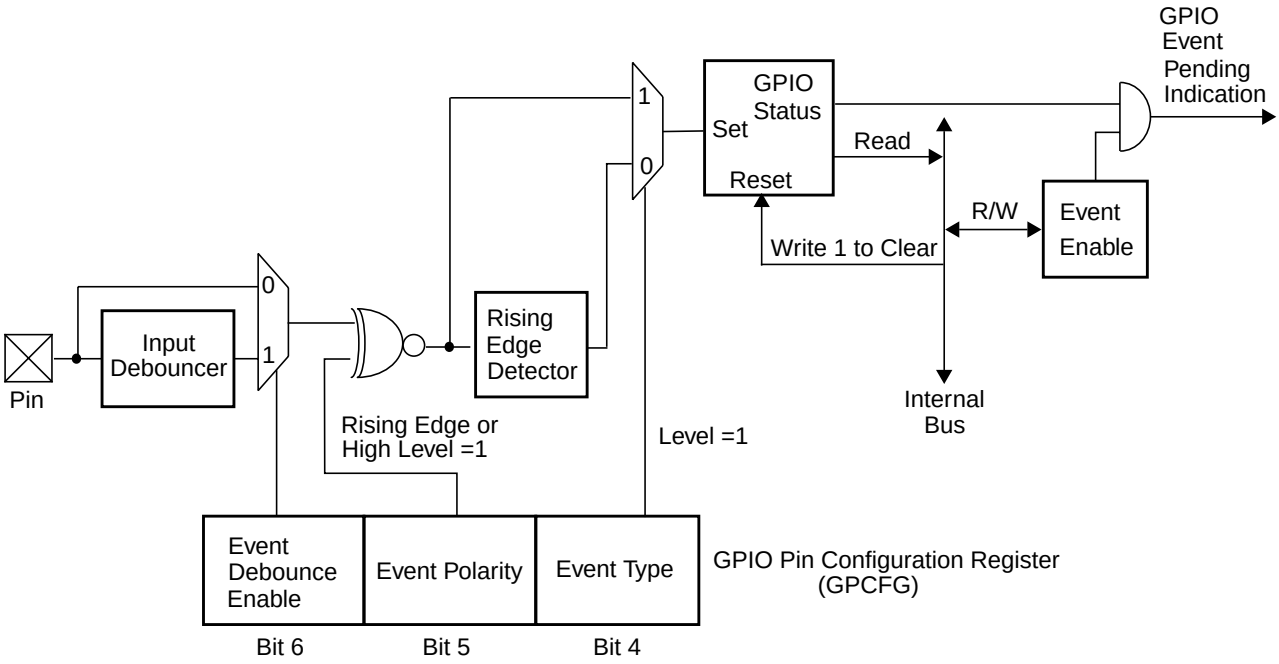


Figure 10. Event Detection

5.3.1 Event Configuration

Each pin in the GPIO port is a potential input event source. The event detection can trigger a system notification on predetermined behavior of the source pin. The GPCFG register determines the event detection trigger type for the system notification.

Event Type and Polarity

Two trigger types of event detection are supported: edge and level. An edge event may be detected on a source pin transition either from high to low or low to high. A level event may be detected when the source pin is at active level. The trigger type is determined by Event Type (bit 4 of the GPCFG register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5 of the GPCFG register).

Active edge refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit in GPEVST register is set by hardware whenever an active edge or an active level is detected, regardless of the GPEVEN register setting. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

Event Debounce Enable

The input signal can be debounced for at least 16 msec before entering the Rising Edge detector. The signal state is transferred to the detector only after a debouncing period during which the signal has no transitions, to ensure that the signal is stable. The debouncer adds 16 msec delay to both assertion and de-assertion of the event pending indicator. Therefore, when working with a level event and system notification by IRQ, it is recommended to disable the debounce if the delay in the IRQ de-assertion is not acceptable. The debounce is controlled by Event Debounce Enable (bit 6 of the GPCFG register).

5.3.2 System Notification

System notification on GPIO-triggered events is done by asserting an Interrupt Request (via the device's Bus Interface).

The system notification for each GPIO pin is controlled by the corresponding bits in the GPEVEN and GPEVR registers. System notification by a GPIO pin is enabled if the corresponding bit of the GPEVEN register is set to 1. The event routing mechanism is described in Figure 11.

5.0 General-Purpose Input/Output (GPIO) Port (Continued)

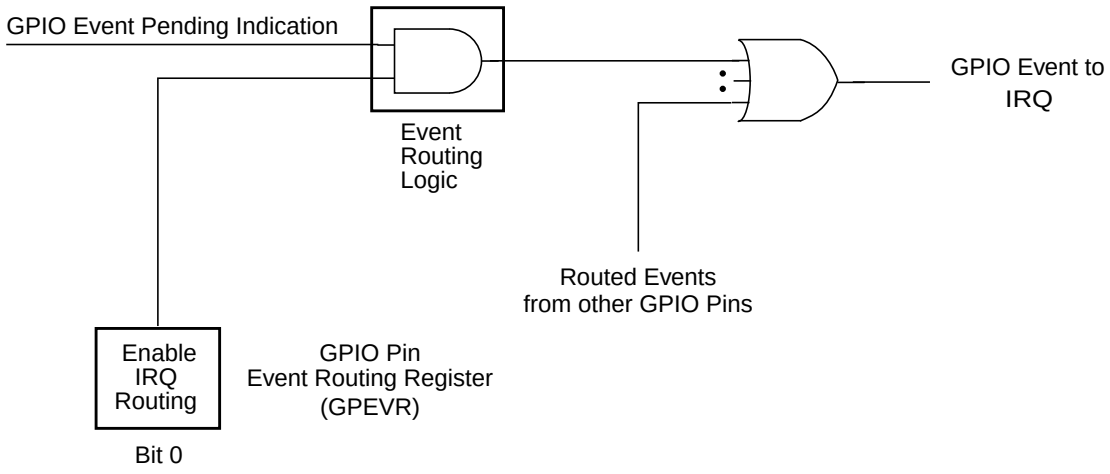


Figure 11. GPIO Event Routing Mechanism

The GPEVST register reflects the event source pending status.

Active edge refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit of the GPEVST register is set by hardware whenever an active edge is detected, regardless of any other bit settings. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

A GPIO pin is in event pending state if the corresponding bit of the GPEVEN register is set and one of the following is true:

- The Event Type is level and the pin is at active level.
- The Event Type is edge and the corresponding bit of the GPEVST register is set.

The target means of system notification is asserted if at least one GPIO pin is in event pending state.

The selection of the target means of system notification is determined by the GPEVR register. If IRQ is selected as one of the means for the system notification, the specific IRQ line is determined by the IRQ selection procedure of the device configuration. The assertion of any means of system notification is blocked when the GPIO functional block is deactivated.

System event notification functionality is provided even when the GPIO pin is enabled as output.

A pending edge event may be cleared by clearing the corresponding GPEVST bit. However, a level event source must not be released by software (except for disabling the source) as long as the pin is at active level. When a level event is used, it is recommended to disable the input debouncer.

On de-activation of the GPIO port, the GPEVST register is cleared, and access to both the GPEVST and GPEVEN registers is disabled. The target IRQ line is detached from the GPIO and de-asserted.

Before enabling any system notification, it is recommended to first set the desired event configuration and then verify that the status registers are cleared.

5.4 GPIO PORT REGISTERS

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

5.0 General-Purpose Input/Output (GPIO) Port (Continued)

5.4.1 GPIO Pin Configuration Registers Structure

For each GPIO Port, there is a group of eight identical sets of configuration registers. Each set is associated with one GPIO pin. The entire group is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register (see Section 3.11.4 on page 38), which functions as an index register for the pin, and the selected GPCFG and GPEVR registers, which reflect the configuration of the currently selected pin (see Table 21).

Table 21. GPIO Configuration Registers

Index	Configuration Register or Action	Type	Reset
F0h	GPIO Pin Select register (GPSEL)	R/W	00h
F1h	GPIO Pin Configuration register 1 (GPCFG)	Varies per bit	04h or 44h[1]
F2h	GPIO Pin Event Routing register (GPEVR)	R/W or RO	01h

1. Depending on port number

5.4.2 GPIO Port Runtime Register Map

Offset	Mnemonic	Register Name	Type	Section
Device specific [1]	GPDO	GPIO Data Out	R/W	5.4.3
Device specific [1]	GPDI	GPIO Data In	RO	5.4.4
Device specific [1]	GPEVEN	GPIO Event Enable	R/W	5.4.5
Device specific [1]	GPEVST	GPIO Event Status	R/W1C	5.4.6

1. The location of this register is defined in Section 3.11.3 on page 37.

5.4.3 GPIO Data Out Register (GPDO)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DATAOUT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**DATAOUT (Data Out).** Bits 7-0 correspond to pins 7-0 of the specific Port. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data, unless the bit is locked by the GPCFG register Lock bit. Reading the bit returns its value regardless of the pin value and configuration. 0: Corresponding pin driven to low. 1: Corresponding pin driven or released (according to buffer type selection) to high (default).

5.0 General-Purpose Input/Output (GPIO) Port (Continued)

5.4.4 GPIO Data In Register (GPDI)

Location:Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**DATAIN**							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7-0	**DATAIN (Data In).** Bits 7-0 correspond to pins 7-0 of the specific Port. Reading each bit returns the value of the corresponding GPIO pin. Pin configuration and the GPDO register value may influence the pin value. Writes are ignored. 0: Corresponding pin level low. 1: Corresponding pin level high.

5.4.5 GPIO Event Enable Register (GPEVEN)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**EVTENA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**EVTENA (Event Enable).** Bits 7-0 correspond to pins 7-0 of the specific Port. Each bit enables system notification by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in GPEVST register. 0: Event pending by corresponding GPIO pin masked. 1: Event pending by corresponding GPIO pin enabled.

5.4.6 GPIO Event Status Register (GPEVST)

Location: Device specific

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**EVTSTAT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7–0	**EVTSTAT (Event Status).** Bits 7–0 correspond to pins 7–0 of the specific Port. The setting of each bit is independent of the Event Enable bit in GPEVEN register. An active event sets the Status bit, which may be cleared only by software writing 1 to the bit. 0: No active edge or level detected since last cleared. 1: Active edge or level detected.

6.0 Legacy Functional Blocks

This chapter briefly describes the following blocks, which provide legacy device functions:

- Parallel Port (PP)
- Serial Port 1 (SP1)
- Infrared (IR)

The description of each Legacy block includes the sections listed below. For details on the general implementation of each legacy block, see the *SuperI/O Legacy Functional Blocks Datasheet*.

- General Description
- Register Map table(s)
- Bitmap table(s).

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C= Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

6.0 Legacy Functional Blocks (Continued)

6.1 PARALLEL PORT

6.1.1 General Description

The Parallel Port supports all IEEE1284 standard communication modes:

- Compatibility (known also as Standard or SPP)
- Bi-directional (known also as PS/2)
- FIFO
- EPP (known also as Mode 4)
- ECP (with an optional Extended ECP mode)

6.1.2 Parallel Port Register Map

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in Extended ECP mode.
- A group of four registers, used only in Extended ECP mode, accessed by a second level offset.

EPP and second level offset registers are available only when the base address is 8-byte aligned.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers and which address bits are used for the base address. See Tables 22 and 23 for a listing of all registers, their offset addresses and the associated modes. All registers are V_{DD3} powered.

Table 22. Parallel Port Register Map for First Level Offset

Group	Offset	Mnemonic	Register	Type	Mode(s)
Common Set	000h	DATAR	Data	R/W	Standard, PS/2 and EPP
		AFIFO	ECP Address FIFO	W	ECP
	001h	DSR	Status	RO	All Modes
	002h	DCR	Control	R/W	All Modes
EPP Only[1]	003h	ADDR	EPP Address	R/W	EPP
	004h	DATA0	EPP Data Port 0	R/W	
	005h	DATA1	EPP Data Port 1	R/W	
	006h	DATA2	EPP Data Port 2	R/W	
	007h	DATA3	EPP Data Port 3	R/W	
PP FIFO, ECP, Test and Configuration Set	400h	CFIFO	PP Data FIFO	W	PP FIFO
		DFIFO	ECP Data FIFO	R/W	ECP
		TFIFO	FIFO Test	R/W	FIFO Test
		CNFGA	Configuration A	RO	Configuration
	401h	CNFGB	Configuration B	RO	
	402h	ECR	Extended Control	R/W	All Modes
Extended Set[1, 2]	403h	EIR	Extended Index	R/W	
	404h	EDR	Extended Data	R/W	
	405h	EAR	Extended Auxiliary Status	R/W	

1. These registers are not accessible when the base address is four-byte aligned (i.e. A2=1).
2. These registers are extended to the register set as defined by MS standard. They are accessible only when enabled by the chip Configuration.

6.0 Legacy Functional Blocks (Continued)

Table 23. Parallel Port Registers at Second Level Offset

Offset	Mnemonic	Register Name	Type
00h	Control0	Extended Control 0	R/W
02h	Control2	Extended Control 1	R/W
04h	Control4	Extended Control 4	R/W
05h	PP Confg0	Configuration 0	R/W

6.1.3 Parallel Port Bitmap Summary

The Parallel Port functional block bitmaps are grouped according to first and second level offsets.

Table 24. Parallel Port Bitmap for First Level Offset

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
000h	DATAR	Data Bits							
000h	AFIFO	Data Type	Address/RLE Field						
001h	DSR	BUSY Status	$\overline{\text{ACK}}$ Status	PE Status	SLCT Status	$\overline{\text{ERR}}$ Status	Reserved[1]		EPP Timeout Status
002h	DCR	Reserved		Direction Control	$\overline{\text{ACK}}$ Interrupt Enable	$\overline{\text{SLIN}}$ Control	$\overline{\text{INIT}}$ Control	$\overline{\text{AFD}}$ Control	$\overline{\text{STB}}$ Control
003h	ADDR	EPP Device or Register Selection Address Bits							
004h	DATA0	EPP Device or R/W Data							
005h	DATA1	EPP Device or R/W Data							
006h	DATA2	EPP Device or R/W Data							
007h	DATA3	EPP Device or R/W Data							
400h	CFIFO	Data Bits							
400h	DFIFO	Data Bits							
400h	TFIFO	Data Bits							
400h	CNFGA	Reserved				Bit 7 of PP Confg0	Reserved		
401h	CNFGB	Reserved	IRQ Signal Value	Interrupt Select			Reserved	DMA Channel Select	
402h	ECR	Parallel Port Mode Control			Interrupt Mask	DMA Enable	Interrupt Service	FIFO Full	FIFO Empty
403h	EIR	Reserved					Second Level Offset		
404h	EDR	Data Bits							
405h	EAR	FIFO Tag	Reserved						

1. See Note in the Register description (see the *SuperI/O Legacy Functional Blocks* datasheet, Section 3.6.5.)

6.0 Legacy Functional Blocks (Continued)

Table 25. Parallel Port Bitmap for Second Level Offset

Register		Bits							
Second Level Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	Control0	Reserved		DCR Register Live	Freeze	Reserved			EPP Timeout Interrupt Mask
02h	Control2	SPP Compatibility	Channel Address Enable	Reserved	EPP 1.7 or 1.9 Select	Reserved			
04h	Control4	Reserved	PP DMA Request Inactive Time			Reserved	PP DMA Request Active Time		
05h	PP Confg0	Bit 3 of CNFGA	Demand DMA Enable	IRQ Channel Number			PE Internal Pull-Up or Pull-Down	DMA Channel Number	

6.0 Legacy Functional Blocks (Continued)

6.2 SERIAL PORT 1 (SP1)

6.2.1 General Description

The Serial Port functional block supports serial data communication with a remote peripheral device or modem using a wired interface. The Serial Port can function in one of three modes:

- 16450-Compatible mode (Standard 16450)
- 16550-Compatible mode (Standard 16550)
- Extended mode

Extended mode provides advanced functionality for the UART.

The Serial Port provides receive and transmit channels that can operate concurrently in full-duplex mode. It performs all functions required to conduct parallel data interchange with the system and composite serial data exchange with the external data channel, including:

- Format conversion between the internal parallel data format and the external programmable composite serial format
- Serial data timing generation and recognition
- Parallel data interchange with the system using a choice of bidirectional data transfer mechanisms
- Status monitoring for all phases of communication activity
- Complete MODEM-control capability.

Existing 16550-based legacy software is completely and transparently supported. Module organization and specific fallback mechanisms switch the module to 16550-Compatible mode on reset or when initialized by 16550 software.

6.2.2 UART Mode Register Bank Overview

6.2.3 Register Bank Overview

Four register banks, each containing eight registers, control Serial Port operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software.

The Bank Selection register (BSR) selects the active bank and is common to all banks as shown in Figure 12.Therefore, each bank defines seven new registers.

The default bank selection after system reset is 0.

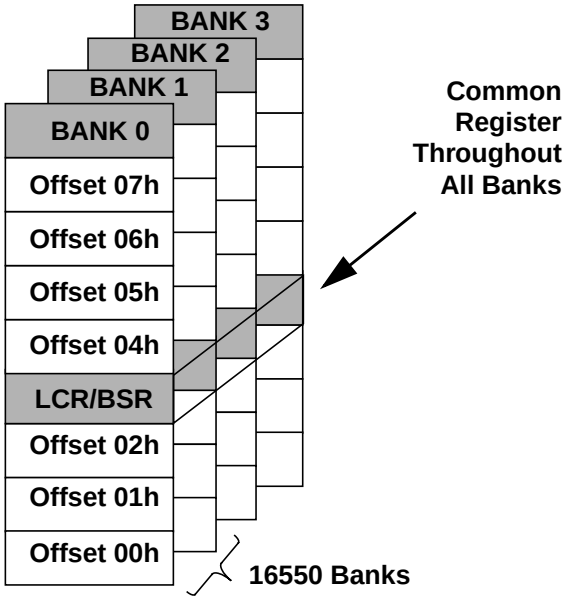


Figure 12. UART Mode Register Bank Architecture

6.0 Legacy Functional Blocks (Continued)

6.2.4 SP1 Register Maps

Table 26. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data	RO
	TXD	Transmitter Data	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification	R
	FCR	FIFO Control	W
03h	LCR	Link Control	W
	BSR	Bank Select	R/W
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	R/W
06h	MSR	Modem Status	R
07h	SPR	Scratch Pad	R/W
	ASCR	Auxiliary Status and Control	RO

Table 27. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor (High Byte)	R/W
02h		Reserved	
03h	LCR/BSR	Link Control/ Bank Select	R/W
04h-07h		Reserved	

Table 28. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor (High Byte)	R/W
02h	EXCR1	Extended Control 1	R/W
03h	BSR	Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	RO
07h	RXFLV	RX_FIFO Level	RO

6.0 Legacy Functional Blocks (Continued)

Table 29. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Identification and Revision ID	RO
01h	SH_LCR	Shadow of LCR	RO
02h	SH_FCR	Shadow of FIFO Control	RO
03h	BSR	Bank Select	R/W
04h-07h		Reserved	

6.2.5 SP1 Bitmap Summary

Table 30. Bank 0 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	RXD	RXD7-0							
00h	TXD	TXD7-0							
01h	IER[1]	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER[2]	Reserved		TXEMP_IE	Reserved	MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
02h	EIR[1]	FEN1-0		Reserved		RXFT	IPR1-0		IPF
	EIR[2]	Reserved		TXEMP_EV	Reserved	MS_EV	LS_EV	TXLDL_EV	RXHDL_EV
	FCR[1]	RXFTH1-0		Reserved			TXSR	RXSR	FIFO_EN
	FCR[2]	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h	MCR[1]	Reserved			LOOP	ISEN/ DCDLP	RILP	RTS	DTR
	MCR[2]	Reserved				TX_DFR	Reserved	RTS	DTR
05h	LSR	ER_INF	TXEMP	TXRDY	BRK	FE	PE	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR[1]	Scratch Data							
	ASCR[2]	Reserved							RXF_TOUT

1. Non-Extended mode
2. Extended mode

6.0 Legacy Functional Blocks (Continued)

Table 31. Bank 1 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	LBGD(L)	LBGD7-0							
01h	LBGD(H)	LBGD15-8							
02h		Reserved							
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h-07h		Reserved							

Table 32. Bank 2 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	BGD(L)	BGD7-0							
01h	BGD(H)	BGD15-8							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	Reserved			EXT_SL
03h	BSR	BKSE	BSR6-0						
04h	EXCR2	LOCK	Reserved	PRESL1-0		Reserved			
05h		Reserved							
06h	TXFLV	Reserved			TFL4-0				
07h	RXFLV	Reserved			RFL4-0				

Table 33. Bank 3 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	MRID	MID3-0				RID3-0			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
02h	SH_FCR	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	BSR	BKSE	BSR6-0						
04-07h		Reserved							

6.0 Legacy Functional Blocks (Continued)

6.3 IR FUNCTIONALITY (IR)

6.3.1 General Description

This functional block provides advanced, versatile serial communications features with IR capabilities. It supports six modes of operation: UART, Sharp-IR, IrDA 1.0 SIR (hereafter SIR), Consumer Electronic IR (also called TV Remote or Consumer remote control, hereafter CEIR), IrDA 1.1 MIR, and FIR. In UART mode, the Serial Port can function in 16450-Compatible mode, 16550-Compatible mode, or Extended mode. This chapter describes general implementation of the Enhanced Serial Port with Fast IR. For device specific implementation, see *Device Architecture and Configuration* in the datasheet of the relevant device.

Note: UART operation of IR module is not supported in the PC87383.

Existing 16550-based legacy software is completely and transparently supported. Organization and specific fallback mechanisms switch the Serial Port to 16550-Compatible mode on reset or when initialized by 16550 software.

This module has two DMA channels; the device can use either one or both of them. One channel is required for IR-based applications, since IR communication works in half-duplex fashion. Two channels would normally be needed to handle high-speed, full-duplex, UART-based applications.

6.3.2 Register Bank Overview

Eight register banks, each containing eight registers, control the module operation. All registers use the same 8-byte address space to indicate offsets 00h-07h. The active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software.

The Bank Selection register (BSR) selects the active bank and is common to all banks. See Figure 13. Therefore, each bank defines seven new registers.

The default bank selection after system reset is 0.

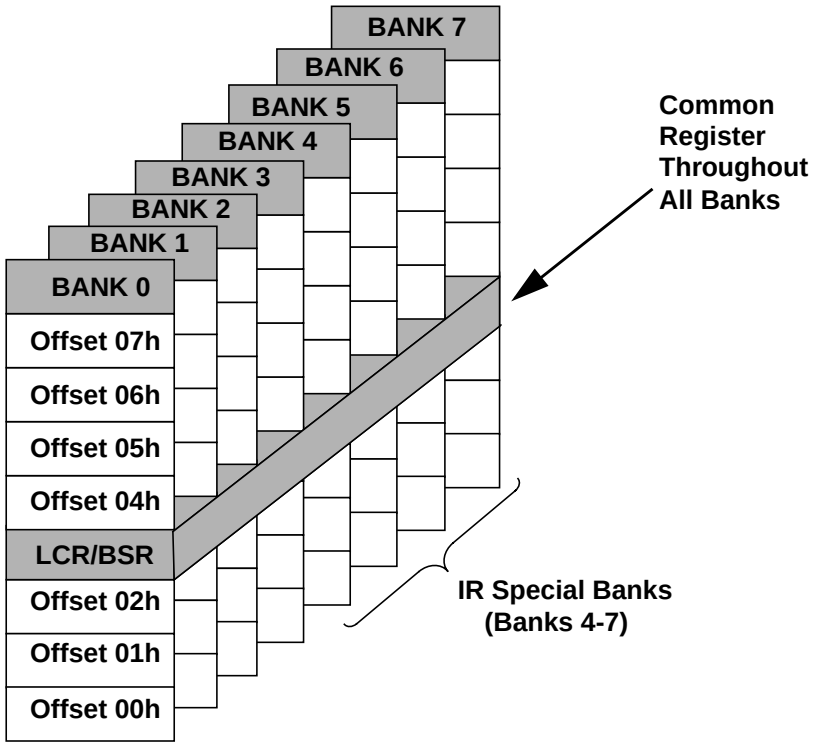


Figure 13. IR Register Bank Architecture

Table 34 shows the main functions of the registers in each bank. Banks 0-3 control both UART and IR modes of operation; banks 4-7 control and configure the IR modes only.

6.0 Legacy Functional Blocks (Continued)

6.3.3 IR Register Map for IR Functionality

Table 34. Register Bank Summary

Bank	UART Mode	IR Mode	Main Functions
0	✓	✓	Global Control and Status
1	✓	✓	Legacy Bank
2	✓	✓	Alternative Baud Generator Divisor, Extended Control and Status
3	✓	✓	Module Revision ID and Shadow registers
4		✓	IR mode setup
5		✓	IR Control and Status FIFO
6		✓	IR Physical Layer Configuration
7		✓	CEIR and Optical Transceiver Configuration

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write.
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write.
- RO = Read Only.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

6.3.4 IR Register Map for IR Functionality

Table 35. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data	RO
	TXD	Transmitter Data	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification	R
	FCR	FIFO Control	W
03h	LCR	Link Control	W
	BSR	Bank Select	R/W
04h	MCR	Modem / Mode Control	R/W
05h	LSR	Link Status	R/W
06h	MSR	Modem Status	R
07h	SPR	Scratch Pad	R/W
	ASCR	Auxiliary Status and Control	Varies per bit

Table 36. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor (High Byte)	R/W
02h		Reserved	

6.0 Legacy Functional Blocks (Continued)

Table 36. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
03h	LCR/BSR	Link Control / Bank Select	R/W
04h - 07h		Reserved	

Table 37. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor (High Byte)	R/W
02h	EXCR1	Extended Control1	R/W
03h	BSR	Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	RO
07h	RXFLV	RX_FIFO Level	RO

Table 38. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Identification and Revision ID	RO
01h	SH_LCR	Shadow of LCR	RO
02h	SH_FCR	Shadow of FIFO Control	RO
03h	BSR	Bank Select	R/W
04h-07h		Reserved	

Table 39. Bank 4 Register Map

Offset	Mnemonic	Register Name	Type
00h	TMR(L)	Timer (Low Byte)	R/W
01h	TMR(H)	Timer (High Byte)	R/W
02h	IRCR1	IR Control 1	R/W
03h	BSR	Bank Select	R/W
04h	TFRL(L)/ TFRCC(L)	Transmitter Frame Length (Low Byte) / Transmitter Frame Current Count (Low Byte)	R/W
05h	TFRL(H)/ TFRCC(H)	Transmitter Frame Length (High Byte) / Transmitter Frame Current Count (High Byte)	R/W
06h	RFRML(L)/ RFRCC(L)	Receiver Frame Maximum Length (Low Byte) / Receiver Frame Current Count (Low Byte)	R/W
07h	RFRML(H)/ RFRCC(H)	Receiver Frame Maximum Length (High Byte) / Receiver Frame Current Count (High Byte)	R/W

6.0 Legacy Functional Blocks (Continued)

Table 40. Bank 5 Register Map

Offset	Mnemonic	Register Name	Type
00h	SPR2	Scratch Pad 2	R/W
01h	SPR3	Scratch Pad 3	R/W
02h		Reserved	
03h	BSR	Bank Select	R/W
04h	IRCR2	IR Control 2	R/W
05h	FRM_ST	Frame Status	RO
06h	RFRL(L)/LSTFRC	Received Frame Length (Low Byte) / Lost Frame Count	RO
07h	RFRL(H)	Received Frame Length (High Byte)	RO

Table 41. Bank 6 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRCR3	IR Control 3	R/W
01h	MIR_PW	MIR Pulse Width Control	R/W
02h	SIR_PW	SIR Pulse Width Control	R/W
03h	BSR	Bank Select	R/W
04h	BFPL	Beginning Flags / Preamble Length	R/W
05h-07h		Reserved	

Table 42. Bank 7 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRRXDC	IR Receiver Demodulator Control	R/W
01h	IRTXMC	IR Transmitter Modulator Control	R/W
02h	RCCFG	CEIR Configuration	R/W
03h	BSR	Bank Select	R/W
04h	IRCFG1	IR Interface Configuration 1	Varies per bit
05h		Reserved	
06h		Reserved	
07h	IRCFG4	IR Interface Configuration 4	R/W

6.0 Legacy Functional Blocks (Continued)

6.3.5 IR Bitmap Summary for IR Functionality

Table 43. Bank 0 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	RXD	RXD7-0							
00h	TXD	TXD7-0							
01h	IER[1]	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER[2]	TMR_IE	SFIF_IE	TXEMP_IE	DMA_IE	MS_IE	LS_IE/ TXHLT_IE	TXLDL_IE	RXHDL_IE
02h	EIR[1]	FEN1-0		Reserved		RXFT	IPR1-0		IPF
	EIR[2]	TMR_EV	SFIF_EV	TXEMP_EV	DMA_EV	MS_EV	LS_EV/ TXHLT_EV	TXLDL_EV	RXHDL_EV
	FCR[1]	RXFTH1-0		Reserved			TXSR	RXSR	FIFO_EN
	FCR[2]	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h	MCR[1]	Reserved			LOOP	ISEN/ DCDLP	RILP	RTS	DTR
	MCR[2]	MDSL2-0			IR_PLS	TX_DFR	DMA_EN	RTS	DTR
05h	LSR	ER_INF/ FR_END	TXEMP	TXRDY	BRK/ MAX_LEN	FE/ PHY_ERR	PE/ BAD_CRC	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR[1]	Scratch Data							
	ASCR[2]	CTE	TXUR	RXACT/ RXBSY	RXWDG/ LOST_FR	TXHFE	S_EOT	FEND_INF	RXF_TOUT

1. Non-Extended mode
2. Extended mode

Table 44. Bank 1 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	LBGD(L)	LBGD7-0							
01h	LBGD(H)	LBGD15-8							
02h		Reserved							
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04-07h		Reserved							

6.0 Legacy Functional Blocks (Continued)

Table 45. Bank 2 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	BGD(L)	BGD7-0							
01h	BGD(H)	BGD15-8							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	DMASWP	DMATH	DMANF	EXT_SL
03h	BSR	BKSE	BSR6-0						
04h	EXCR2	LOCK	Reserved	PRESL1-0		RF_SIZ1-0		TF_SIZ1-0	
05h		Reserved							
06h	TXFLV	Reserved		TFL5-0					
07h	RXFLV	Reserved		RFL5-0					

Table 46. Bank 3 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	MRID	MID3-0				RID3-0			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
02h	SH_FCR	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	BSR	BKSE	BSR6-0						
04h-07h		Reserved							

Table 47. Bank 4 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	TMR(L)	TMR7-0							
01h	TMR(H)	Reserved				TMR11-8			
02h	IRCR1	Reserved				IR_SL1-0		CTEST	TMR_EN
03h	BSR	BKSE	BSR6-0						
04h	TFRL(L)/ TFRCC(L)	TFRL7-0 /TFRCC7-0							
05h	TFRL(H)/ TFRCC(H)	Reserved			TFRL12-8 / TFRCC12-8				
06h	RFRML(L)/ RFRCC(L)	RFRML7-0 / RFRCC7-0							
07h	RFRML(H)/ RFRCC(H)	Reserved			RFRML12-8 / RFRCC12-8				

6.0 Legacy Functional Blocks (Continued)

Table 48. Bank 5 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	SPR2	Scratch Pad 2							
01h	SPR3	Scratch Pad 3							
02h		Reserved							
03h	BSR	BKSE	BSR6-0						
04h	IRCR2	Reserved	SFTSL	FEND_MD	AUX_IRRX	TX_MS	MDRS	IRMSSL	IR_FDPLX
05h	FRM_ST	VLD	LOST_FR	Reserved	MAX_LEN	PHY_ERR	BAD_CRC	OVR1	OVR2
06h	RFRL(L)/ LSTFRC	RFRL7-0 / LSTFRC7-0							
07h	RFRL(H)	Reserved			RFRL12-8				

Table 49. Bank 6 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	IRCR3	SHDM_DS	SHDM_DS	FIR_CRC	MIR_CRC	Reserved	TXCRC_INV	TXCRC_DS	Reserved
01h	MIR_PW	Reserved				MPW3-0			
02h	SIR_PW	Reserved				SPW3-0			
03h	BSR	BKSE	BSR6-0						
04h	BFPL	MBF7-4				FPL3-0			
05h-07h		Reserved							

Table 50. Bank 7 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	IRRXDC	DBW2-0			DFR4-0				
01h	IRTXMC	MCPW2-0			MCFR4-0				
02h	RCCFG	R_LEN	T_OV	RXHSC	RCDM_DS	Reserved	TXHSC	RC_MMD1-0	
03h	BSR	BKSE	BSR6-0						
04h	IRCFG1	STRV_MS	Reserved	SIRTX	IRRX1 Level	IRID3	IRIC2-0		
05h		Reserved							
06h		Reserved							
07h	IRCFG4	Reserved	IRRX_MD	IRSL0_DS	RXINV	IRSL21_DS	Reserved		

7.0 Device Characteristics

7.1 GENERAL DC ELECTRICAL CHARACTERISTICS

7.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
T_A	Operating Temperature	0		+70	°C

7.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		-0.5	+4.1	V
V_I	Input Voltage		-0.5	V_{DD} + 0.5	V
V_I	Input Voltage	All other pins	-0.5	5.5	V
		LPC pins[1]	-0.5	V_{DD} + 0.5	V
V_O	Output Voltage		-0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		-65	+165	°C
P_D	Power Dissipation			500	mW
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[2]	2000		V

1. LCLK, LAD3-0, $\overline{\text{LFRAME}}$, $\overline{\text{LRESET}}$, SERIRQ, $\overline{\text{LPCPD}}$, $\overline{\text{LDRQ}}$, $\overline{\text{CLKRUN}}$.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

7.1.3 Capacitance

Symbol	Parameter	Min[2]	Typ[1]	Max[2]	Unit
C_{LCLK}	LCLK Pin Capacitance	5	8	12	pF
C_{PIN}	Other Pins Capacitance		8	10	pF

1. T_A = 25°C, f = 1 MHz
2. Not tested. Guaranteed by design

7.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD}	V_{DD} Average Main Supply Current	V_{IL} = 0.5 V, V_{IH} = 2.4 V No Load	7	10	mA
I_{DDLP}	V_{DD} Quiescent Main Supply Current in Low Power Mode	V_{IL} = V_{SS}, V_{IH} = V_{DD} No Load	1	1.5	mA

7.0 Device Characteristics (Continued)

7.1.5 Voltage Thresholds

Symbol	Parameter[1]	Min[2]	Typ	Max[2]	Unit
V_{DDON}	V_{DD} Detected as Power-on	2.2	2.6	2.9	V
V_{DDOFF}	V_{DD} Detected as Power-off	2.1	2.5	2.8	V

1. All parameters specified for $0°C \leq T_A \leq 70°C$.
2. Not tested. Guaranteed by characterization.

7.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in Section 1.2 on page 9. The characteristics describe the general I/O buffer types defined in Table 1 on page 9. For exceptions, refer to Section 7.2.7. The DC characteristics of the system interface meet the PCI2.2 3.3V DC signaling.

7.2.1 Input, PCI 3.3V

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		$0.5V_{DD}$	$V_{DD} + 0.5$[1]	V
V_{IL}	Input Low Voltage		-0.5[1]	$0.3V_{DD}$	V
I_{IL}[2]	Input Leakage Current	$0 < V_{in} < V_{DD}$		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with TRI-STATE outputs.

7.2.2 Input, TTL Compatible

Symbol: IN_T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		-0.5[1]	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		1	µA
		$V_{IN} = V_{SS}$		-1	µA

1. Not tested. Guaranteed by design.

7.2.3 Input, TTL Compatible with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		-0.5 [1]	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		1	µA
		$V_{IN} = V_{SS}$		-1	µA
V_H	Input Hysteresis		250[2]		mV

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.

7.0 Device Characteristics (Continued)

7.2.4 Output, PCI 3.3V

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{out} = -500 µA	$0.9V_{DD}$		V
V_{OL}	Output Low Voltage	I_{out} =1500 µA		$0.1\ V_{DD}$	V

7.2.5 Output, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, Push-Pull buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = -*p* mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V

7.2.6 Output, Open-Drain Buffer

Symbol: OD_n

Output, Open-Drain output buffer, capable of sinking *n* mA. Output from these signals is open-drain and cannot be forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V

7.2.7 Exceptions

1. All pins are 5V tolerant except for the pins with PCI (IN_{PCI}, O_{PCI}) buffer types.
2. All pins are back-drive protected, except for the pins with PCI (IN_{PCI}, O_{PCI}) buffer types.
3. The following pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current from V_{DD} (when V_{IN} = 0): GPIO00-07, GPIO10-11, GPO12-13, GPIO14-17, GPIO20-21, GPO22, GPIO23-24, $\overline{ACK}$, $\overline{AFD\_DSTRB}$, $\overline{ERR}$, $\overline{INIT}$, PE, $\overline{SLIN\_ASTRB}$, $\overline{STB\_WRITE}$.
4. The following pins have an internal static pull-down resistor (when enabled) and therefore may have leakage current to V_{SS} (when $V_{IN} = V_{DD}$): BUSY_$\overline{WAIT}$, PE and SLCT.
5. The following strap pins have an internal static pull-up resistor enabled during V_{DD} Power-Up Reset and therefore may have leakage current to V_{DD} (when V_{IN} = 0): BADDR, $\overline{TRIS}$, $\overline{TEST}$.
6. Output from SLCT, BUSY_$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 register is 0) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
7. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 register is set to 1) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
8. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP-Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
9. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
10. In XOR Tree mode, the buffer type of the input pins participating in the XOR Tree (Section 2.4.2 on page 17) is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode; see Section 1.3 on page 5.

7.0 Device Characteristics (Continued)

7.2.8 Terminology

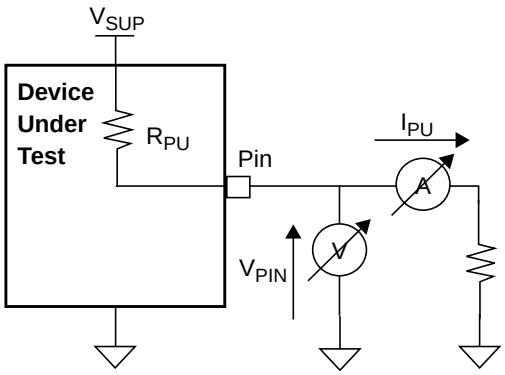
Back-Drive Protection. A pin that is back-drive protected does not sink current into the supply when an input voltage higher than the supply, but below the pin's maximum input voltage, is applied to the pin. This is true even when the supply is inactive. Note that active pull-up resistors and active output buffers are typically not back-drive protected.

5-Volt Tolerance. An input signal that is 5V tolerant can operate with input voltage of up to 5V even though the supply to the device is only 3.3V. The actual maximum input voltage allowed to be supplied to the pin is indicated by the maximum high voltage allowed for the input buffer. Note that some pins have multiple buffers, not all of which are 5V tolerant. In such cases, there is a note that indicates at what conditions a 5V input may be applied to the pin; if there is no note, the low maximum voltage among the buffers is the maximum voltage allowed for the pin.

7.3 INTERNAL RESISTORS

DC Test Conditions

Pull-Up Resistor Test Circuit



Pull-Down Resistor Test Circuit

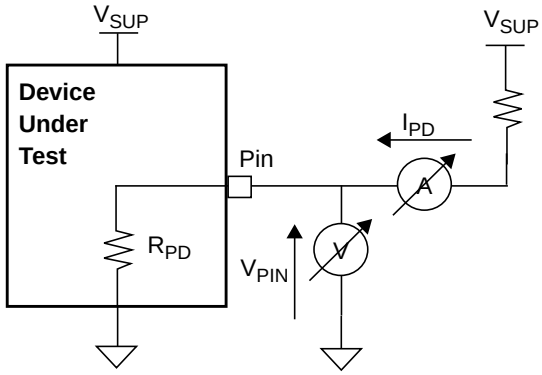


Figure 14. Internal Resistor Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V

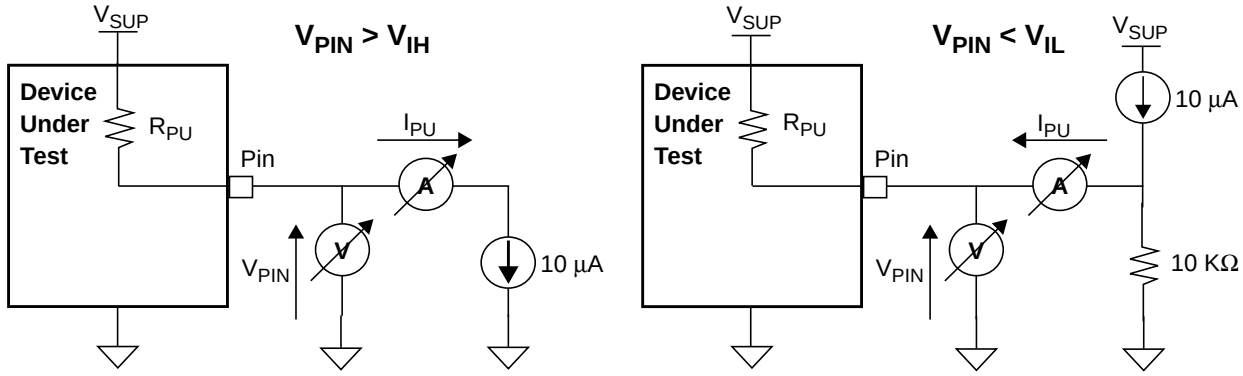


Figure 15. Internal Pull-Down Resistor for Straps, T_A = 0°C to 70°C, V_{SUP} = 3.3V

Notes for Figures 14 and 15:

1. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
2. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

7.0 Device Characteristics (Continued)

7.3.1 Pull-Up Resistor

Symbol: PU_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-up equivalent resistance	V_{PIN} = 0V	*nn* – 30%	*nn*	*nn* + 30%	KΩ
		V_{PIN} = 0.8 V_{SUP}[3]			*nn* – 38%	KΩ
		V_{PIN} = 0.17 V_{SUP}[3]	*nn* – 35%			KΩ

1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.
3. For strap pins only.

7.3.2 Pull-Down Resistor

Symbol: PD_{nn}

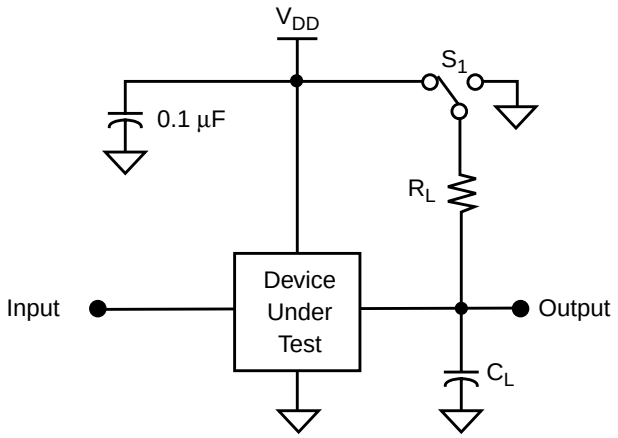
Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PD}	Pull-down equivalent resistance	V_{PIN} = V_{SUP}	*nn* – 30%	*nn*	*nn* + 30%	KΩ

1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.

7.4 AC ELECTRICAL CHARACTERISTICS

7.4.1 AC Test Conditions

Load Circuit (Notes 1, 2)



AC Testing Input, Output Waveform

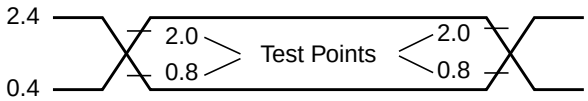


Figure 16. AC Test Conditions, T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ±10%

Notes:

1. C_L = 50 pF for all output pins; this value includes both jig and oscilloscope capacitance.
2. S_1 = Open for push-pull output pins.
   S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements.
   S_1 = GND for high impedance to active high and active high to high impedance measurements.
   R_L = 1.0 KΩ for all the pins.

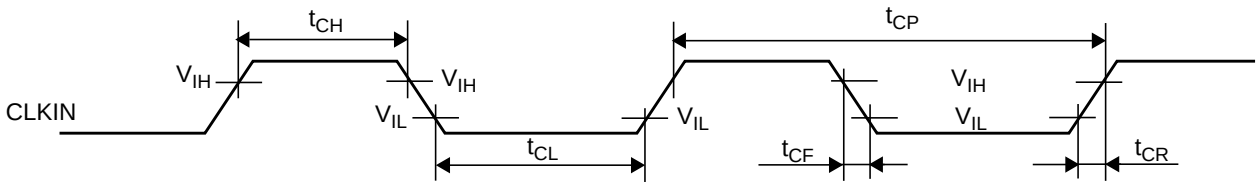
7.0 Device Characteristics (Continued)

7.4.2 Clock Input Timing

Symbol	Parameter	48 MHz		14.31818 MHz		
		Min	Max	Min	Max	Unit
t_{CH}	Clock High Pulse Width[1]	6		29.5		ns
t_{CL}	Clock Low Pulse Width[1]	6		29.5		ns
t_{CP}	Clock Period [2]	20	21.5	69.14	70.54	ns
F_{CIN}	Clock Frequency	48 - 0.1%	48 + 0.1%	14.31818 - 0.02%	14.31818 + 0.02%	MHz
t_{CR}	Clock Rise Time[2] (0.8V-2.0V)		5		5	ns
t_{CF}	Clock Fall Time[2] (2.0V-0.8V)		5		5	ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.

.

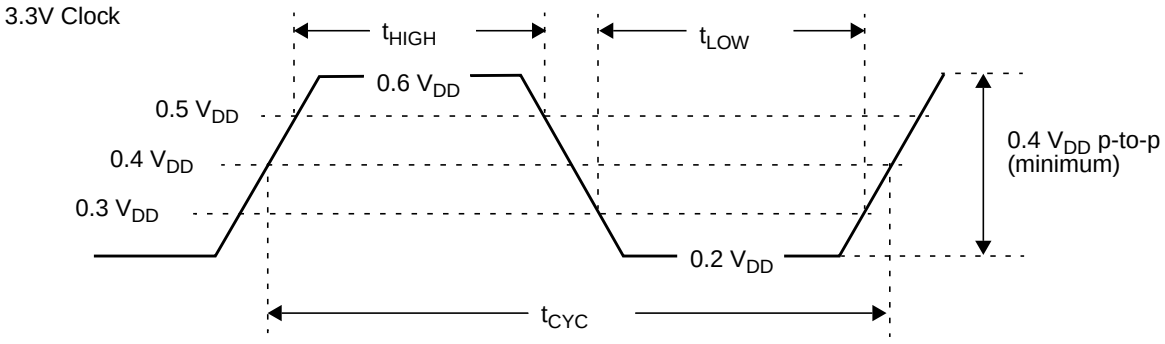


7.0 Device Characteristics (Continued)

7.4.3 LCLK and $\overline{\text{LRESET}}$

Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	LCLK Cycle Time	30		ns
t_{HIGH}	LCLK High Time[2]	11		ns
t_{LOW}	LCLK Low Time[2]	11		ns
-	LCLK Slew Rate[3,4]	1	4	V/ns
-	$\overline{\text{LRESET}}$ Slew Rate[3,5]	50		mV/ns
t_{WRST}	$\overline{\text{LRESET}}$ pulse width	100		ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz can be guaranteed by design rather than by testing. The clock frequency can be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.
2. Not tested. Guaranteed by characterization.
3. Not tested. Guaranteed by design
4. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering as shown below.
5. The minimum $\overline{\text{LRESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal, and ensures that system noise cannot render an otherwise monotonic signal to appear to bounce in the switching range.

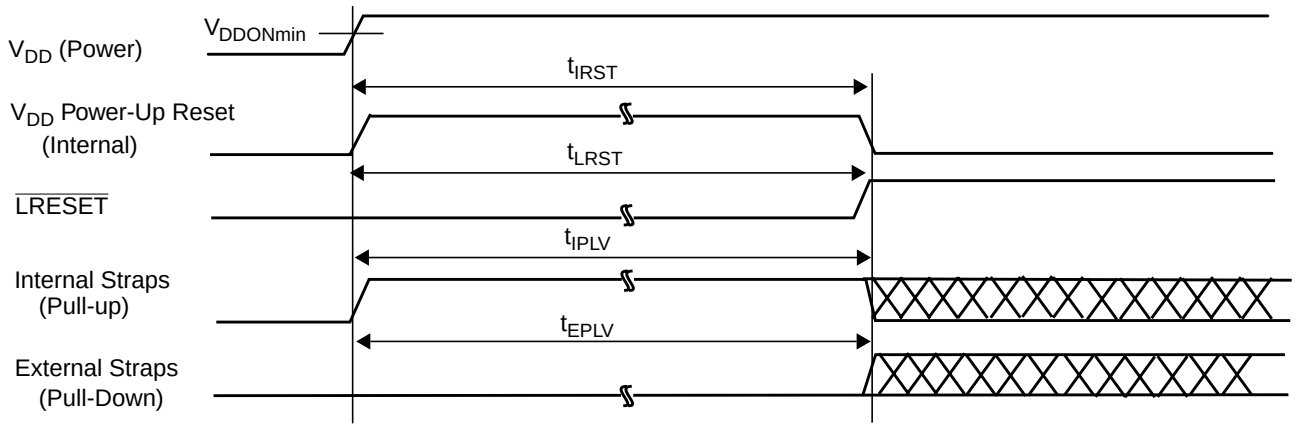


7.0 Device Characteristics (Continued)

7.4.4 V_{DD} Power-Up Reset

Symbol	Description	Reference Conditions	Min[1]	Max[1]
t_{IRST}	Internal Power-Up reset time	V_{DD} power-up to end of internal reset		t_{LRST}
t_{LRST}	$\overline{\text{LRESET}}$ active time	V_{DD} power-up to end of $\overline{\text{PCI\_RESET}}$	10 ms	
t_{IPLV}	Internal strap pull-up resistor, valid time[2]	Before end of internal reset	t_{IRST}	
t_{EPLV}	External strap pull-up resistor, valid time	Before end of internal reset	t_{IRST}	

1. Not tested. Guaranteed by design.
2. Active only during V_{DD} Power-Up reset.

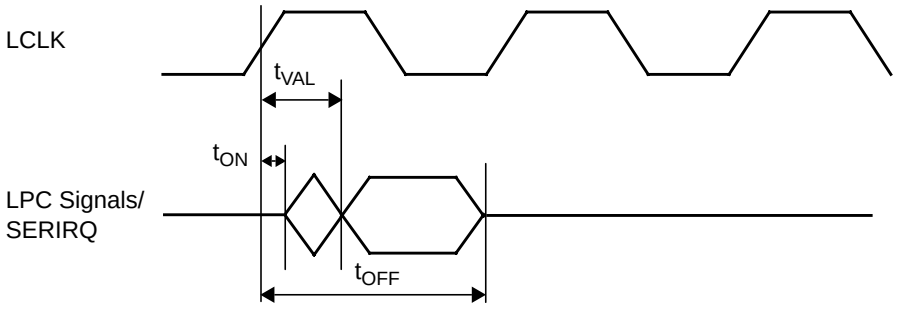


7.0 Device Characteristics (Continued)

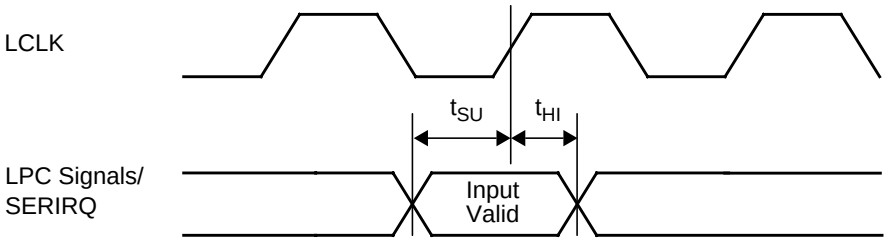
7.4.5 LPC and SERIRQ Signals

Symbol	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Output Valid Delay	After RE LCLK	2	11	ns
t_{ON}	Float to Active Delay	After RE LCLK	2		ns
t_{OFF}	Active to Float Delay	After RE LCLK		28	ns
t_{SU}	Input Setup Time	Before RE LCLK	7		ns
t_{HI}	Input Hold Time	After RE LCLK	0		ns

Output



Input



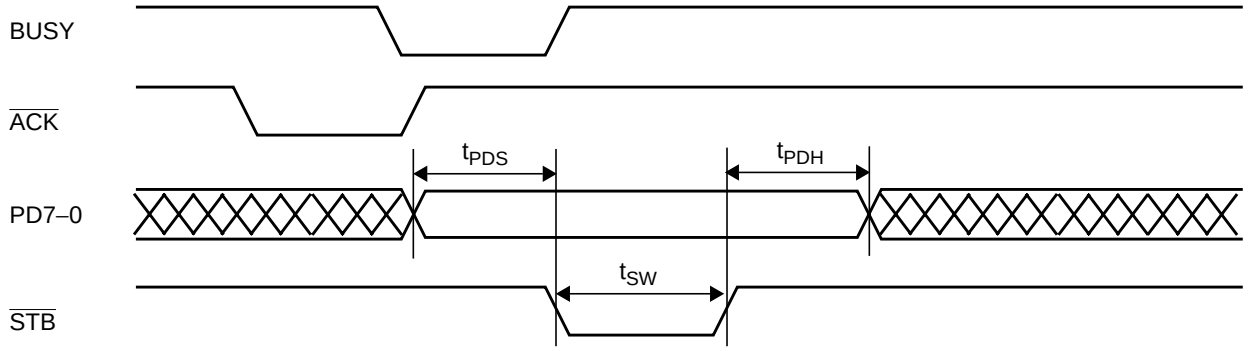
7.0 Device Characteristics (Continued)

7.4.6 Parallel Port Timing

Standard Parallel Port Timing

Symbol	Parameter	Conditions	Min[1]	Max[1]	Unit
t_{PDH}	Port Data Hold	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{PDS}	Port Data Setup	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{SW}	Strobe Width	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns

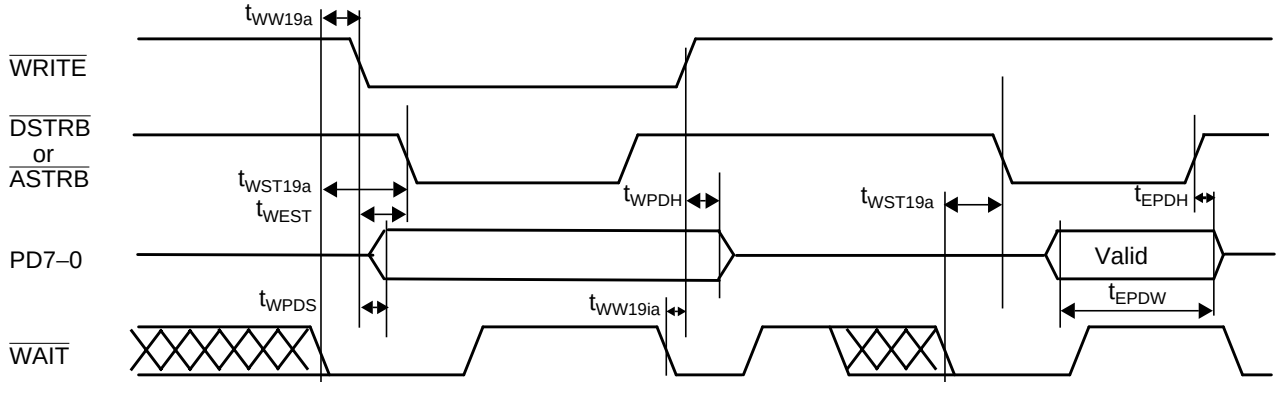
1. Not tested. Guaranteed by design.



Enhanced Parallel Port Timing

Symbol	Parameter	Min[1]	Max[1]	EPP 1.7[2]	EPP 1.9[2]	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WAIT}$ Low		45		✔	ns
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low		45		✔	ns
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WAIT}$ Low		65		✔	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	10		✔	✔	ns
t_{WPDH}	PD7–0 Hold after $\overline{WRITE}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7–0 Valid after $\overline{WRITE}$ Active		15	✔	✔	ns
t_{EPDW}	PD7–0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7–0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive	0		✔	✔	ns

1. Not tested. Guaranteed by characterization.
2. Also in ECP Mode 4



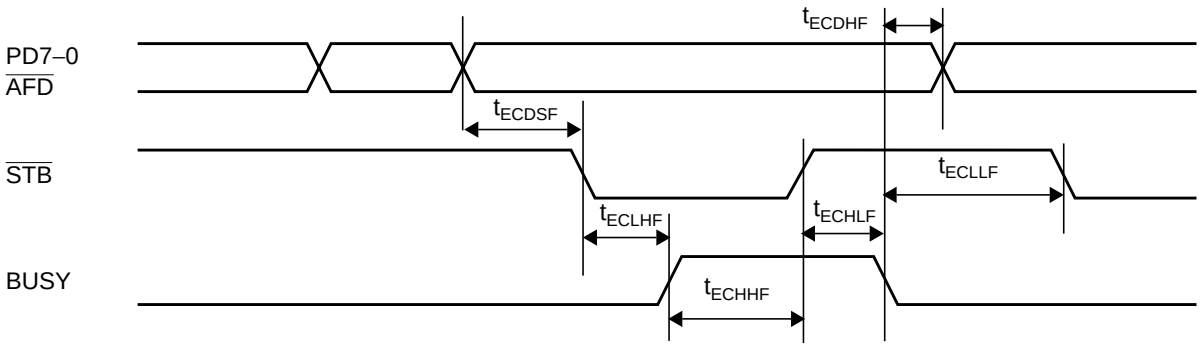
7.0 Device Characteristics (Continued)

Extended Capabilities Port (ECP) Timing

Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active[1]	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive[1]	0		ns
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active[1]	75		ns
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active[2]	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Active[2]	0	35	ms
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive[1]	0		ns

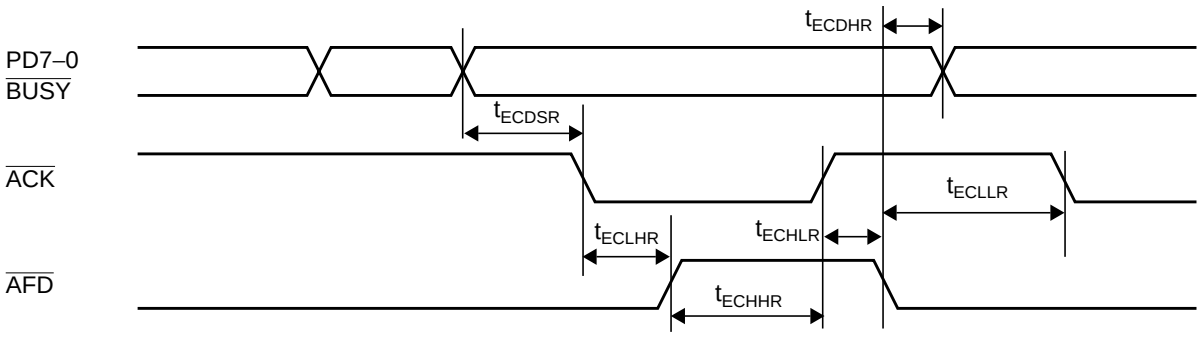
1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.



Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active[1]	0		ns
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active[1]	0		ns
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active[1]	75		ns
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive[2]	0	35	ms
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive[2]	0	1	s
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active[1]	0		ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.

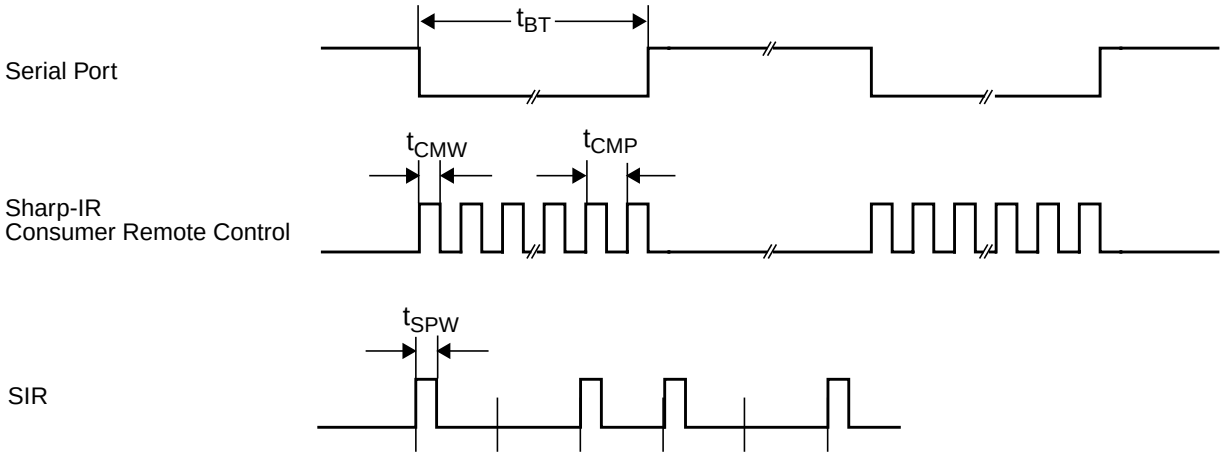


7.0 Device Characteristics (Continued)

7.4.7 Serial Port, Sharp-IR, SIR and Consumer Remote Control Timing

Symbol	Parameter	Conditions	Min[1]	Max[1]	Unit
t_{BT}	Single Bit Time in Serial Port and Sharp-IR	Transmitter	t_{BTN} - 25 [2]	t_{BTN} + 25	ns
		Receiver	t_{BTN} - 2%	t_{BTN} + 2%	ns
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	t_{CWN} - 25 [3]	t_{CWN} + 25	ns
		Receiver	500		ns
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	t_{CPN} - 25 [4]	t_{CPN} + 25	ns
		Receiver	t_{MMIN} [5]	t_{MMAX} [5]	ns
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(3/16)$ x t_{BTN} - 15 [2]	$(3/16)$ x t_{BTN} + 15 [2]	ns
		Transmitter, Fixed	1.48	1.78	µs
		Receiver	1		µs
S_{DRT}	SIR Data Rate Tolerance. % of Nominal Data Rate.	Transmitter		± 0.87%	
		Receiver		± 2.0%	
t_{SJT}	SIR Leading Edge Jitter. % of Nominal Bit Duration.	Transmitter		± 2.5%	
		Receiver		± 6.5%	

1. Not tested. Guaranteed by design.
2. t_{BTN} is the nominal bit time in Serial Port, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers.
3. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCPW field (bits 7-5) of the IRTXMC register and the TXHSC bit (bit 2) of the RCCFG register.
4. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCFR field (bits 4-0) of the IRTXMC register and the TXHSC bit (bit 2) of the RCCFG register.
5. t_{MMIN} and t_{MMAX} define the time range within which the period of the in-coming subcarrier signal must fall for the signal to be accepted by the receiver. These time values are determined by the contents of the IRRXDC register and the setting of the RXHSC bit (bit 5) of the RCCFG register.



7.0 Device Characteristics (Continued)

7.4.8 MIR and FIR Timing

Symbol	Parameter	Conditions	Min[1]	Max[1]	Unit
t_{MPW}	MIR Signal Pulse Width	Transmitter	t_{MWN} - 25 [2]	t_{MWN} + 25	nsec
		Receiver	60		nsec
M_{DRT}	MIR Transmitter Data Rate Tolerance			± 0.1%	
t_{MJT}	MIR Receiver Edge Jitter, % of Nominal Bit Duration			± 2.9%	
t_{FPW}	FIR Signal Pulse Width	Transmitter	120	130	nsec
		Receiver	90	160	nsec
t_{FDPW}	FIR Signal Double Pulse Width	Transmitter	245	255	nsec
		Receiver	215	285	nsec
F_{DRT}	FIR Transmitter Data Rate Tolerance			± 0.01%	
t_{FJT}	FIR Receiver Edge Jitter, % of Nominal Bit Duration			± 4.0%	

1. Not tested. Guaranteed by design.
2. t_{MWN} is the nominal pulse width for MIR mode. It is determined by the M_PWID field (bits 4-0) in the MIR_PW register at offset 01h in bank 6.

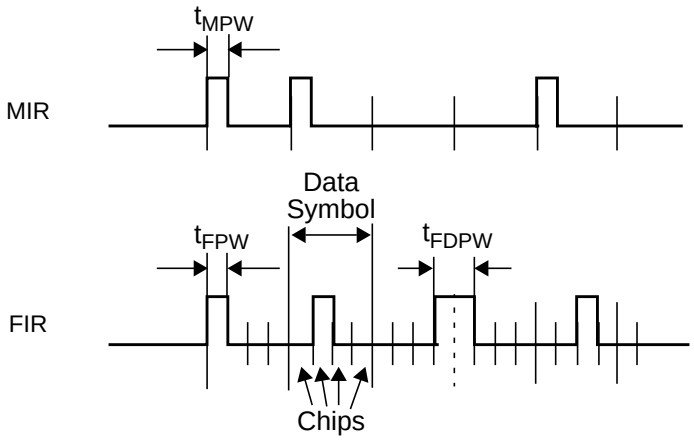


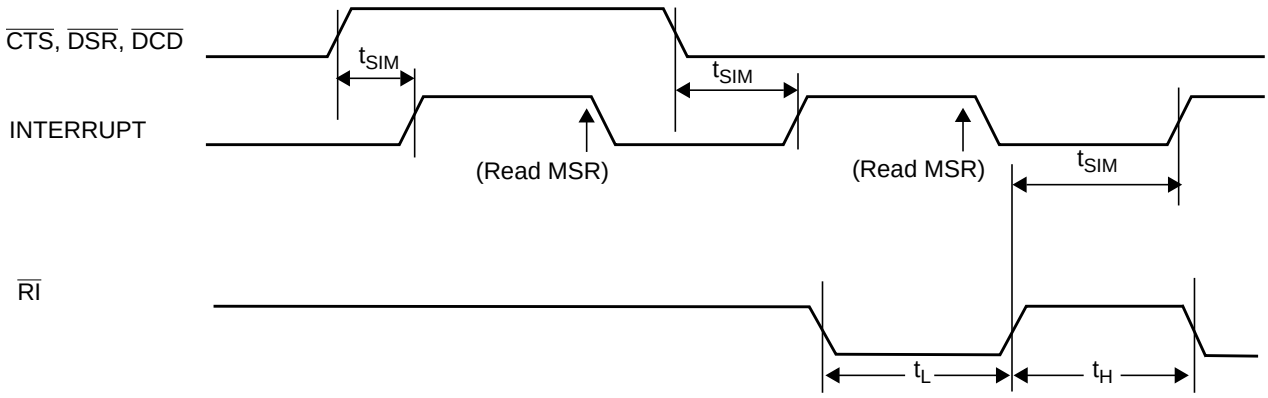
Figure 17. MIR and FIR Timing

7.0 Device Characteristics (Continued)

7.4.9 Modem Control Timing

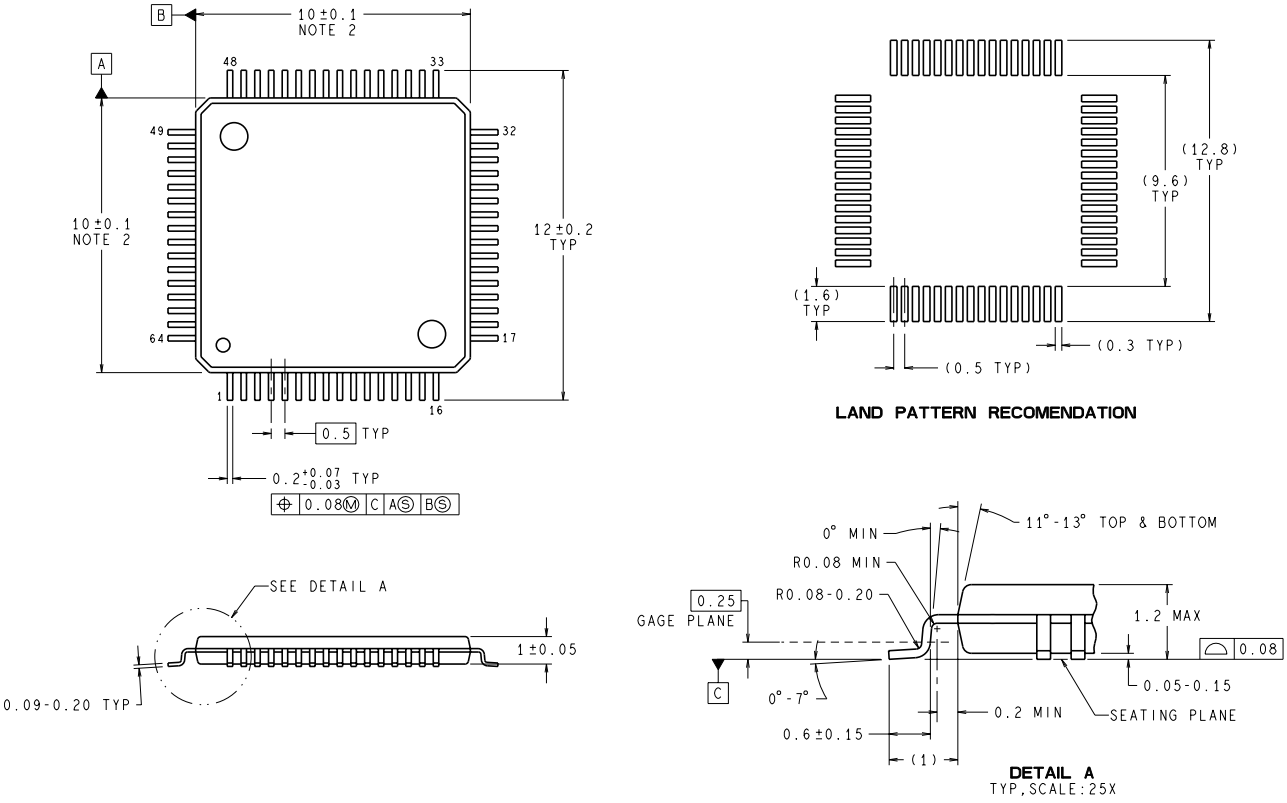
Symbol	Parameter	Min	Max	Unit
t_L	$\overline{RI1}$ Low Time[1]	10		ns
t_H	$\overline{RI1}$ High Time[1]	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input[2]		40	ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.



Physical Dimensions

All dimensions are in millimeters



64-Pin Thin Quad Flatpack (TQFP)
NS Package Number VEC064A
Order Number PC87383-VS

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National Semiconductor Corporation
Americas
Email:
new.feedback@nsc.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 87 90

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507
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