National Semiconductor

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PC87436 Advanced IPMI Baseboard Management Controller

General Description

The PC87436 is a highly-integrated Enhanced IPMI Baseboard Management Controller (BMC), or satellite management controller, with an embedded RISC core and advanced functions. It is targeted for a wide range of host-independent controlled platforms such as servers and desktops.

The PC87436 incorporates National's CompactRISC™ CR16B core (a high-performance 16-bit RISC processor), on-chip RAM, system support functions, Low Pin Count (LPC) host interface and a Bus Interface Unit (BIU) that directly interfaces with optional expansion memory and I/O devices.

System support functions include: four SMBus® channels; high-accuracy analog-to-digital (ADC) for system control, system health monitoring and analog controls; two USARTs for Emergency Management Port (EMP) and ICMB extension; watchdog and other timers; and interrupt control and general-purpose I/O (GPIO).

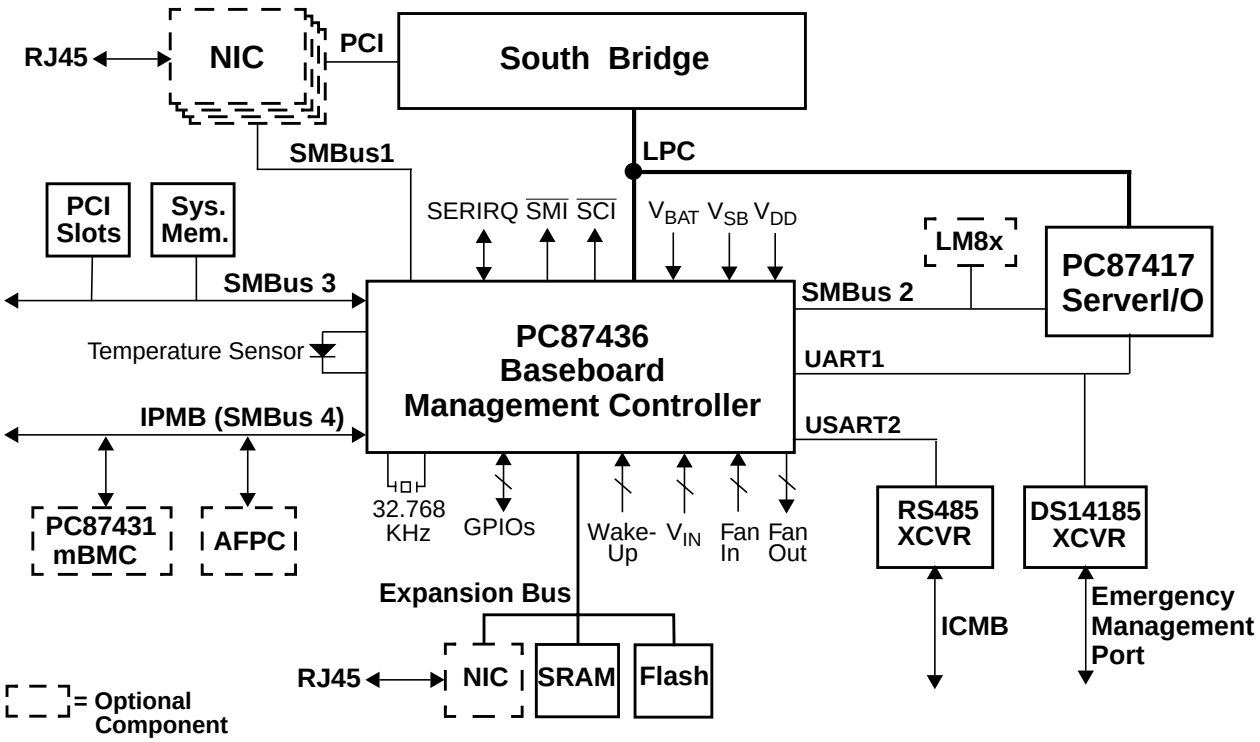
The PC87436 interfaces with the host via an LPC bus that provides three interface channels, with peripherals and IPMI devices via four independent SMBuses and with additional memory and I/O ports via a private expansion bus.

The PC87436 is PC01 and ACPI compliant.

Outstanding Features

- Intelligent Platform Management Interface (IPMI)-optimized BMC
- 16-bit RISC core, with 2 Mbyte linear address space and running at up to 28 MHz
- Host interface, based on Intel's *LPC Interface Specification Revision 1.0*, September 29th, 1997
- Four SMBus interface modules (each module can be master and slave)
- Two USARTs, one for ICMB interface extension and one for EMP
- Integrated ADC channels and thermo-diode interface
- 112 GPIO ports with a variety of wake-up events
- Integrated RTC
- Low current consumption
- JTAG-based debugger interface
- 176-pin LQFP package

System Connection Diagram



Device-Specific Information

The following table shows the differences between the PC87436 devices.

Function	PC87436S	PC87436M	PC87436L
ADC (Accuracy)	10-bit	8-bit	
TMS	✔		
USART Interfaces	2	2	2
SMBus Interfaces	4	4	4

Features

- Supports *Intelligent Platform Management Interface (IPMI) Specification v1.5*, rev 1.1, February 20, 2002
- Supports Microsoft® *Advanced Power Management (APM) Specifications Revision 1.2*, February 1996

Embedded Controller Features

- Processing Unit
  - CompactRISC CR16B 16-bit embedded RISC processor core
  - 2 Mbytes of linear address space
- Internal Memory
  - 4 Kbytes of ROM for CR16B Boot block
  - Memory contents protection
  - 4 Kbytes of on-chip RAM
- Expansion Memory
  - Three address zones for static devices, with configurable wait states and 8- or 16-bit-wide bus
  - Up to 2 Mbytes of additional code and data
  - Supports host-controlled code download and on-board flash update
  - Memory access protection
- Host Interface Channels
  - Three KCS host interface channels
  - IRQ, $\overline{\text{SMI}}$ and SCI ($\overline{\text{PWUREQ}}$) generation
- Multi-Input Wake-Up (MIWU)
  - Supports up to 32 wake-up or interrupt inputs
  - Special input for system On/Off switch
  - Generates wake-up event to PMC (Power Management Control) module
  - Generates interrupts to ICU module
  - Provides user-selectable trigger conditions
- Interrupt Control Unit (ICU)
  - 31 maskable vector interrupt sources
  - 26 general-purpose external interrupt inputs through MIWU
  - Enable and pending indication for each interrupt
  - Non-maskable interrupt input
- General-Purpose I/O (GPIO)
  - 112 port pins
  - I/O pins individually configured as input or output with optional pull-up resistors
  - 27 external wake-up events
  - Low-cost external GPIO expansion
  - 14 mA output buffers for glueless LED logic
- Four SMBus Interface modules.

  Each module:
  - Is master and slave
  - Supports 7- or 10-bit addressing
  - Monitors three slave addresses simultaneously
  - Supports polling and interrupt controlled operation
  - Generates a wake-up signal on detection of a Start Condition while in Idle mode
  - Has optional internal pull-up on SDA and SCL pins
  - Allows data buffering with DMA support
- Two 16-bit Multi-Function Timer (MFT16) modules. Each module:
  - Contains two 16-bit timers
  - Supports Pulse Width Modulation (PWM), Capture and Counter modes
- Two Universal Synchronous/Asynchronous Receiver-transmitters (USART); for each USART:
  - A full-duplex USART channel
  - Programmable baud rate
  - Optional Synchronous mode with either internal or external clock
  - 7-, 8- or 9-bit protocols
  - Data transfer via Interrupt, polling
  - Data double buffering with DMA support
- Pulse Width Modulation (PWM) Module
  - Eight outputs
  - 8/16-bit resolution
  - Common input clock 8/16-bit prescaler

Features (Continued)

- Timer and Watchdog
  - 16-bit periodic interrupt timer with 30 µs resolution and 5-bit prescaler for embedded controller tick and periodic wake-up tasks
  - 8-bit watchdog timer
- Hardware Monitoring (by ADC)
  - 14 inputs, with 10-bit resolution
  - Controlled by embedded controller
  - System Voltage Measurement
    - Up to eight external measurement points
    - Four internal measurement points
  - Diode-Based Temperature Measurement
    - Software-controlled fault detection
    - Hardware-monitored over-temperature detection
- Development Support Features
  - Interface to debugger via JTAG pins
    - ISE/ADB mode
    - On-board Debug mode
- CR16B Access to Host Controlled Functions
  - Enabled when host inactive

Host Controlled Function Features

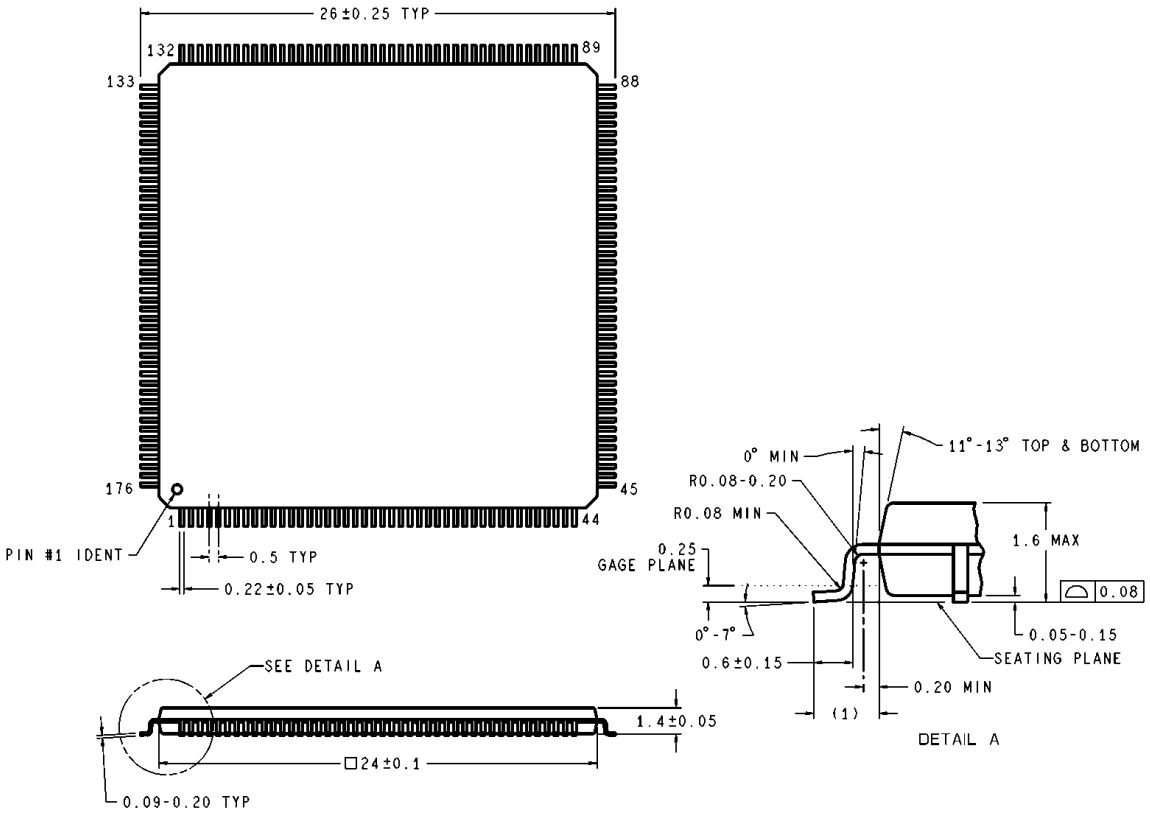
- LPC System Interface
  - Synchronous cycles, up to 33 MHz bus clock
  - Serial IRQ
  - I/O and Memory read and write cycles
  - LPC and FWH read cycles
- Base Address (BADDR) strap to determine the base address of the configuration Index-Data register pair
- PC01 and ACPI Compliant
  - PnP Configuration Register structure
  - Flexible resource allocation for all logical devices
    - Relocatable base address
    - 15 IRQ routing options
  - Generates SCI ($\overline{\text{PWUREQ}}$) for ACPI systems
- Shared Memory and Protection
  - Bridges LPC access to expansion memory
  - CR16B controlled, LPC access protection
  - FWH transaction support
- Real-Time Clock (RTC)
- System Wake-Up Control (SWC)
  - Wake-up detection
  - Software controlled off events
  - Optional routing of power-up request to IRQ, $\overline{\text{SMI}}$ and SCI ($\overline{\text{PWUREQ}}$) lines

Clocking, Supply and Package Information

- Strap Input Controlled Operating Modes
  - TRI-STATE® of all the pins
  - Development (ISE/ADB)
  - On-board development
  - Programing Environment
- Clocks
  - Single 32.768 KHz crystal oscillator
  - On-chip high frequency clock generator
    - CPU clock 4-28 MHz
    - Software-controlled frequency generation
    - Based on the 32.768 KHz input
  - 32.768 KHz clock output
  - CPU clock output
- Power Management Control (PMC)
  - Separate 3.3V supply for the CPU and its peripherals (V_{SB}), Analog (AV_{CC}) and for the other functions (V_{DD})
  - All pins are 5V tolerant and back-drive protected (except the LPC bus pins)
  - Backup battery input for RTC, and wake-up configuration
  - Reduced power consumption capability
  - Automatic wake-up on system events
- Testability
  - XOR-Tree Structure
    - Includes all device pins (except supply and analog pins
    - Selected at power up by strap input
  - TRI-STATE device pins, selected at power up by strap input (TRIS)
- Package
  - 176-pin LQFP package

Physical Dimensions

All dimensions are in millimeters



176-Low Profile Plastic Quad Flatpack (LQFP)
Order Number PC87436S-VPC, PC87436M-VPC, PC87436L-VPC
NS Package Number VPC176

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