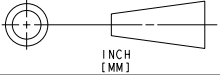


REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
	SEE SHEET 1			

PACKAGE DIMENSIONS					
X1 DESIGNATOR	X1 PACKAGE WIDTH ±30μm	X2 DESIGNATOR	X2 PACKAGE LENGTH ±30μm	X3 DESIGNATOR	X3 PACKAGE HEIGHT ±100μm
A	1514	A	1996	A	795
B	1539	B	2022	B	945
C	1565	C	2047	C	995
D	1590	D	2073		
E	1615	E	2098		
F	1641	F	2123		
G	1666	G	2149		
H	1692	H	2174		
J	1717	J	2200		
K	1742	K	2225		
L	1768	L	2250		
M	1793	M	2276		
N	1819	N	2301		
P	1844	P	2327		
Q	1869	Q	2352		
R	1895	R	2377		
S	1920	S	2403		
T	1946	T	2428		
U	1971	U	2454		
V	1996	V	2479		
W	2022	W	2504		
X	2047	X	2530		
Y	2073	Y	2555		
Z	2098	Z	2581		
1	2123	1	2606		
2	2149	2	2631		
3	2174	3	2657		
4	2200	4	2682		
5	2225	5	2708		
6	2250	6	2733		

APPROVALS		DATE		 <i>National Semiconductor</i> 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN MARTA SUCHY		08/17/2001			
DFTG. CHK. THANH LEQUANG		02/11/2002			
ENGR. CHK. VIRAJ PATWARDHAN		02/11/2002			
 PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	C	(SC)MKT-BLP10XXX	B
		DO NOT SCALE DRAWING		SHEET 2 of 2	