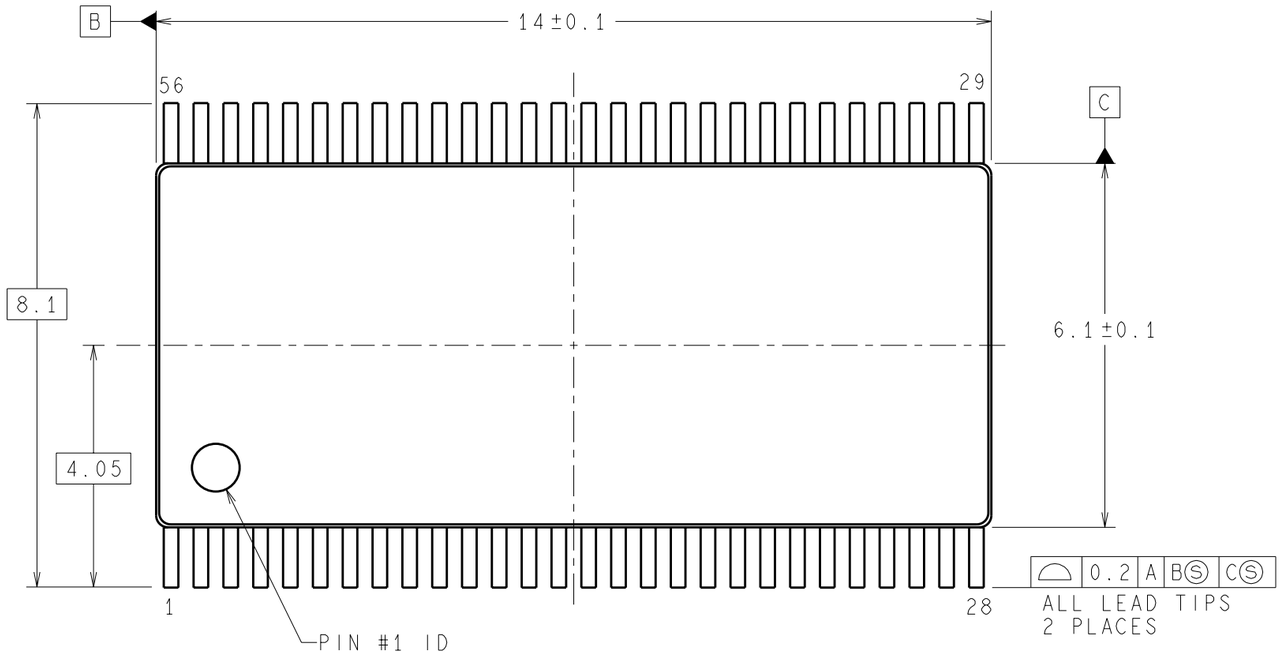
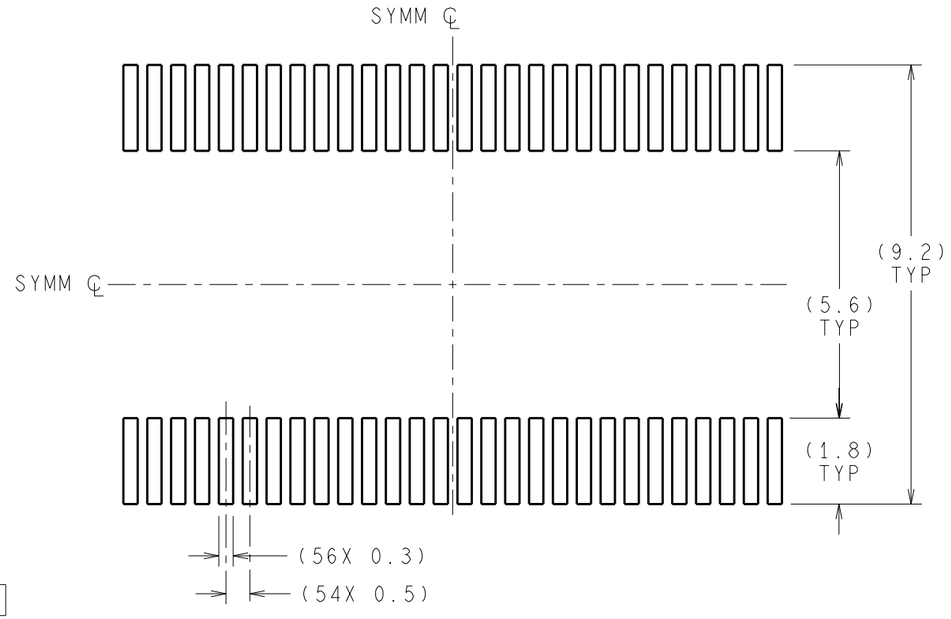
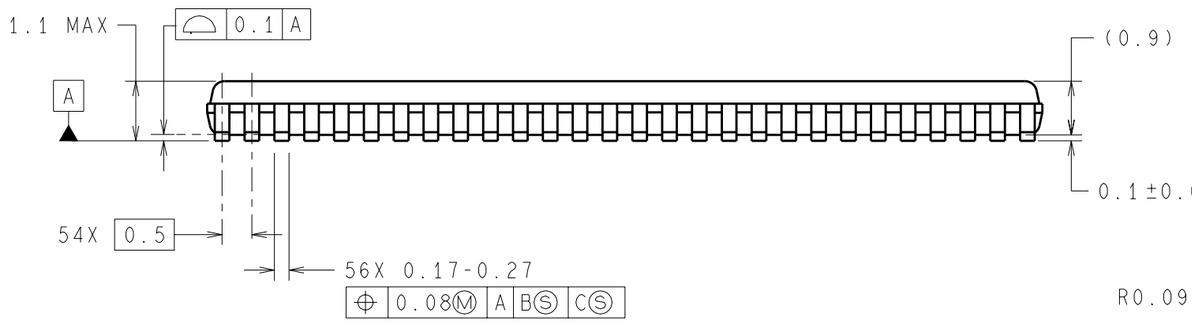
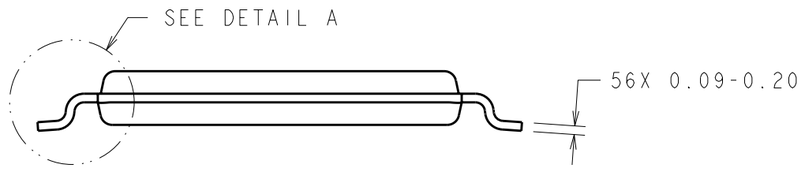
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
B	REDRAW ON PRO/E; ADD LAND PATTERN RECOMENDATION	11323	02/16/1996	MS/CS
C	POS. TOL. OF LEADS WAS 0.13; CHANGE SHT. TO "B" SIZE; UPDATE NOTE 1.	721	06/05/2002	MS/RW
D	ADD LEAD FINISH NOTE & UPDATE TITLE.	976	04/02/2003	MS/RW

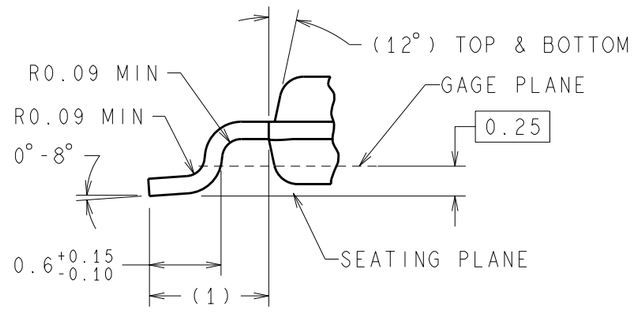




LAND PATTERN RECOMENDATION







DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. REFERENCE JEDEC REGISTRATION MO-153, VARIATION EE.

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/16/1996
DFTG. CHK.: THANH LEQUANG	04/02/2003
ENGR. CHK.: RANDALL WALBERG	04/02/2003

PROJECTION MM

National Semiconductor
2900 Semiconductor Dr, Santa Clara, CA 95052-8090

MOLDED TSSOP, JEDEC, 14x6.1x0.9mm BODY, 56 LD, 0.50mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-MTD56	D

FORMERLY: N/A SHEET 1 of 1