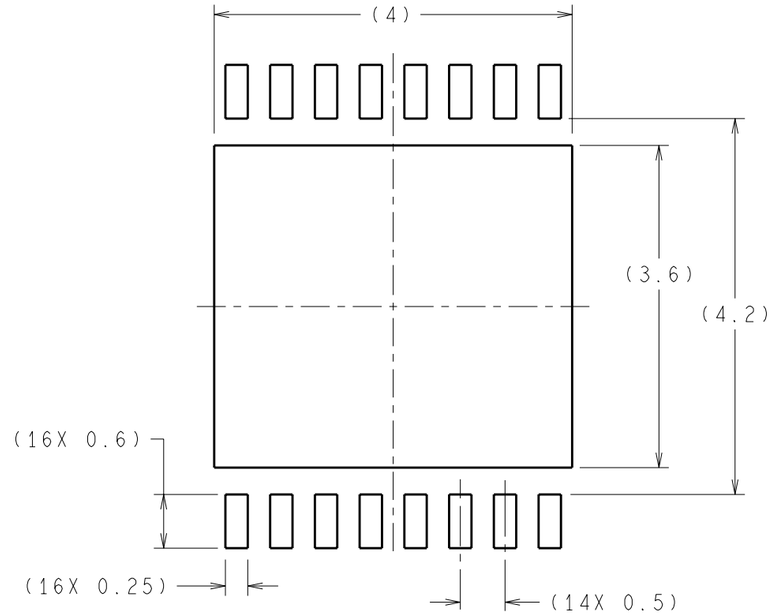
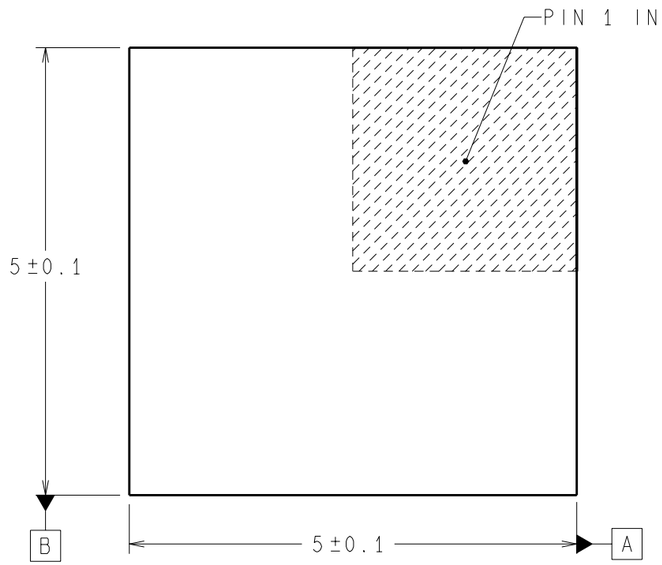
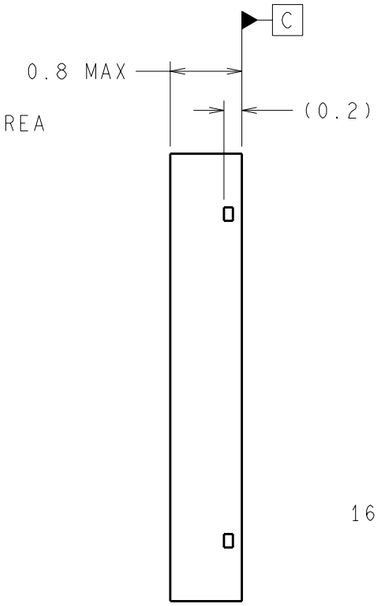
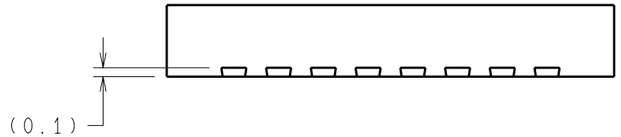
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1053	05/16/2003	HR/MS/SN

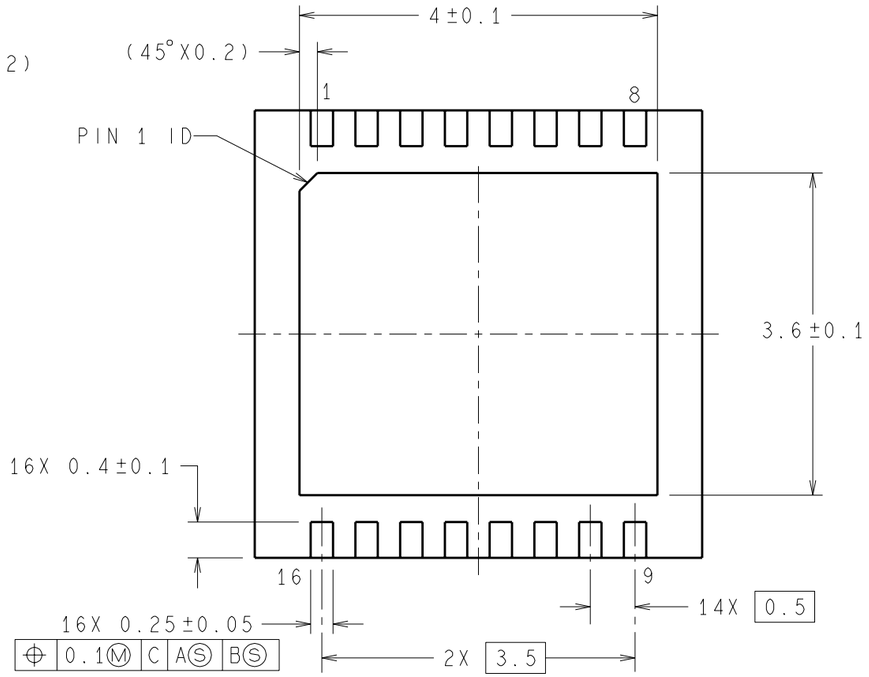


RECOMMENDED LAND PATTERN









DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF MAY 2003.

APPROVALS	DATE
DRAWN HASFIZA RAMLEY	05/16/2003
DFTG. CHK. MARTA SUCHY	05/16/2003
ENGR. CHK. SANTHIRAN N	05/16/2003

PROJECTION MM

National Semiconductor
2900 Semiconductor Dr. Santa Clara, CA 95052-8090

LLP, PLASTIC, DUAL, 5x5x0.8mm BODY, 16 LD, 0.5mm PITCH, NO PULLBACK

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SDA16A	A

FORMERLY: N/A SHEET 1 of 1