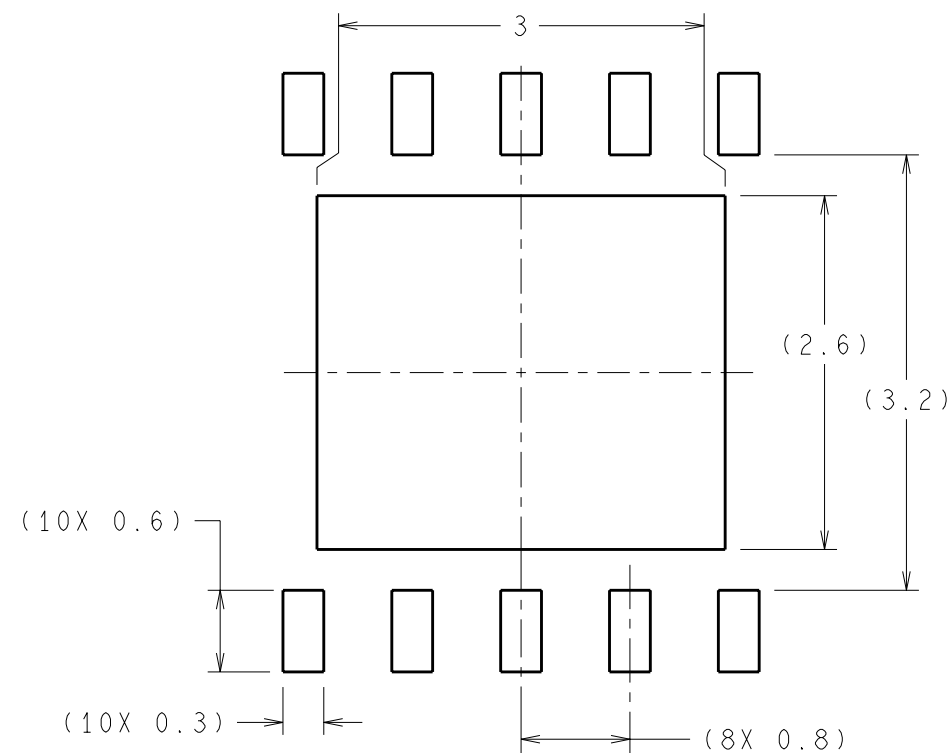
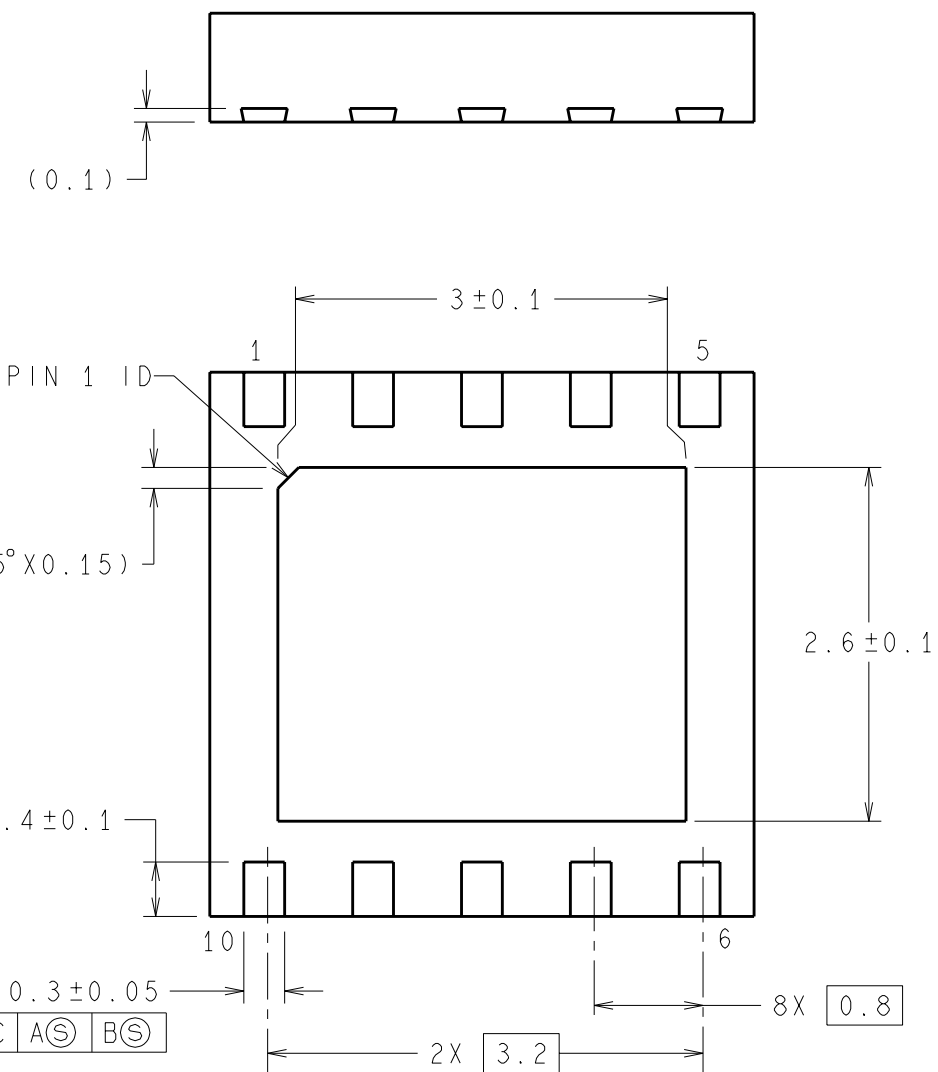
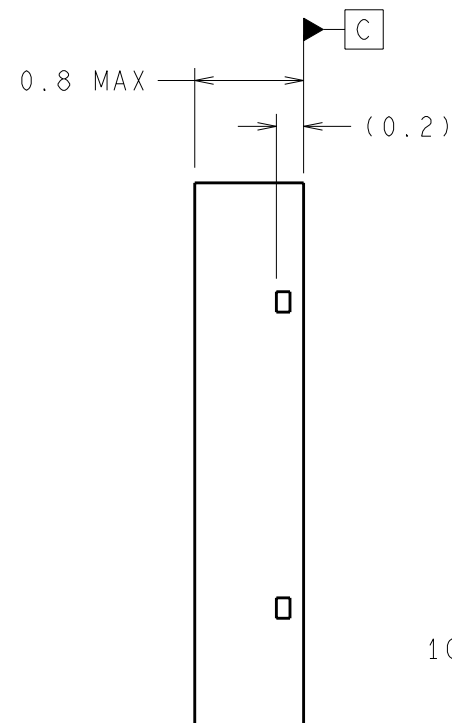
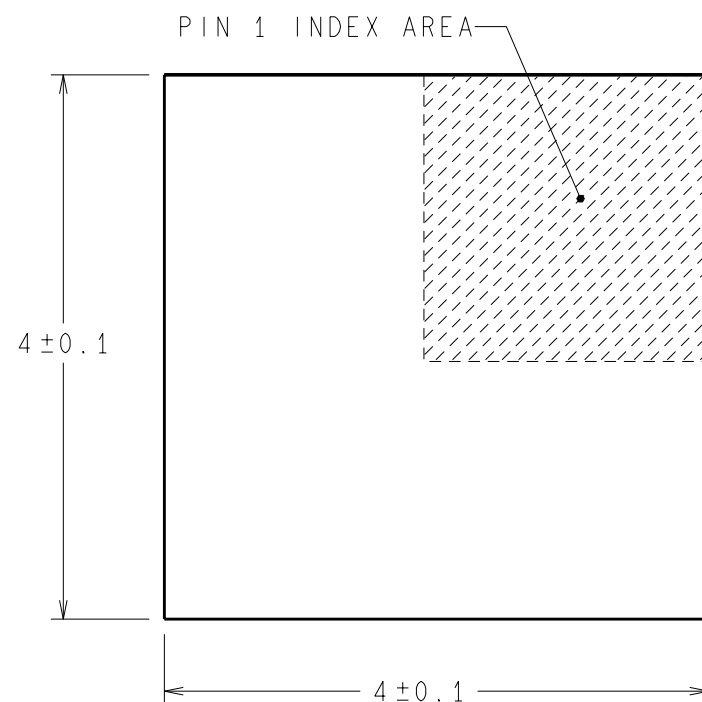


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1054	05/16/2003	HR/MS/SN



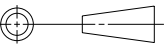
RECOMMENDED LAND PATTERN



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF MAY 2003.

DIMENSIONS ARE IN MILLIMETERS

APPROVALS		DATE		 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	HASFIZA RAMLEY		05/16/2003		
DFTG. CHK.	MARTA SUCHY		05/16/2003	LLP, PLASTIC, DUAL, 4x4x0.8mm BODY, 10 LD 0.8mm PITCH, NO PULLBACK	
ENGR. CHK.	SANTHIRAN N		05/16/2003		
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
 MM		NTS	B	(SC)MKT-SDC10A	A
FORMERLY: N/A				SHEET 1 of 1	