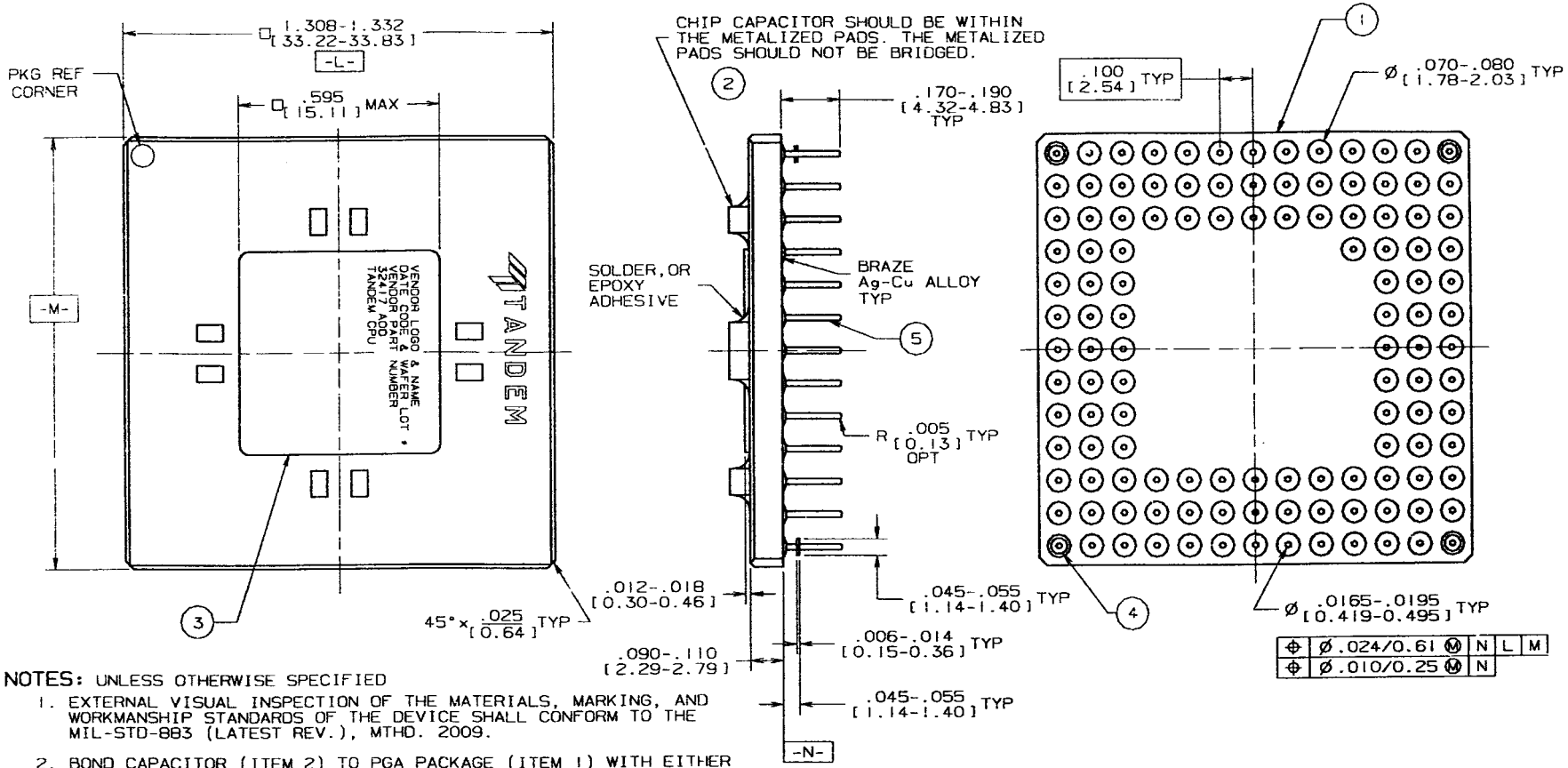
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	08033	07/31/90	PG/[illegible]



NOTES: UNLESS OTHERWISE SPECIFIED

1. EXTERNAL VISUAL INSPECTION OF THE MATERIALS, MARKING, AND WORKMANSHIP STANDARDS OF THE DEVICE SHALL CONFORM TO THE MIL-STD-883 (LATEST REV.), MTHD. 2009.
2. BOND CAPACITOR (ITEM 2) TO PGA PACKAGE (ITEM 1) WITH EITHER EPOXY OR SOLDER. THERE SHALL NOT BE ANY EPOXY OR SOLDER BRIDGING BETWEEN THE TWO METALIZED PADS OR CAPACITOR TERMINATIONS. THE BOND INTERFACE MUST WITHSTAND A LATERAL SHEAR FORCE OF 7.0 LBF MINIMUM WHEN APPLIED TO THE FULL LENGTH OF THE CAPACITOR PER MIL-STD-883 (LATEST REV.), MTHD. 2019.
3. MARK THE PACKAGE LID (ITEM 3) WITHIN THE AREA SHOWN WITH 4 POINT LETTER OR LARGER, INK TO BE BLACK, RESISTANCE TO SOLVENTS PER MIL-STD-883 (LATEST REV.) MTHD. 2015, INDELIBLE AND HEAT RESISTANT TO 150° C.
4. THIS PGA PACKAGE (ITEM 1) TO BE USED WITH THE MC CHIP ONLY.
5. BALLING OR BUILDUP OF LID-SEAL SOLDER ON TOP OF THE LID (ITEM 3) IS NOT ACCEPTABLE.
6. MECHANICAL INTERPRETATION OF THIS DOCUMENT SHOULD COMPLY WITH THE ANSI 14.5 (LATEST REV.).
7. THE PGA PACKAGE (ITEM 1) PINS SOLDERABILITY SHOULD CONFORM TO MIL-STD-883 (LATEST REV.), MTHD. 2003.

ITEM	DESCRIPTION	QTY
5	PIN, KOVAR OR ALLOY 42	121
4	BRIM PIN, KOVAR OR ALLOY 42	4
3	LID, KOVAR, Au-Ni PLATED	1
2	CHIP CAP, Z5U 50V +80-20%, .12UF	4
1	PIN GRID ARRAY PKG. (PGA121)	1

MATERIALS

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN P. GIFFORD	07/31/90
DRTG. CHK. [illegible]	08/03/90
ENGR'G CHK. [illegible]	08/07/90
APPROVAL	

PROJECTION INCH [MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

PIN GRID ARRAY, CERAMIC, 121 PIN, CAVITY UP

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-U121A	A

FORMERLY: N/A SHEET 1 OF 1