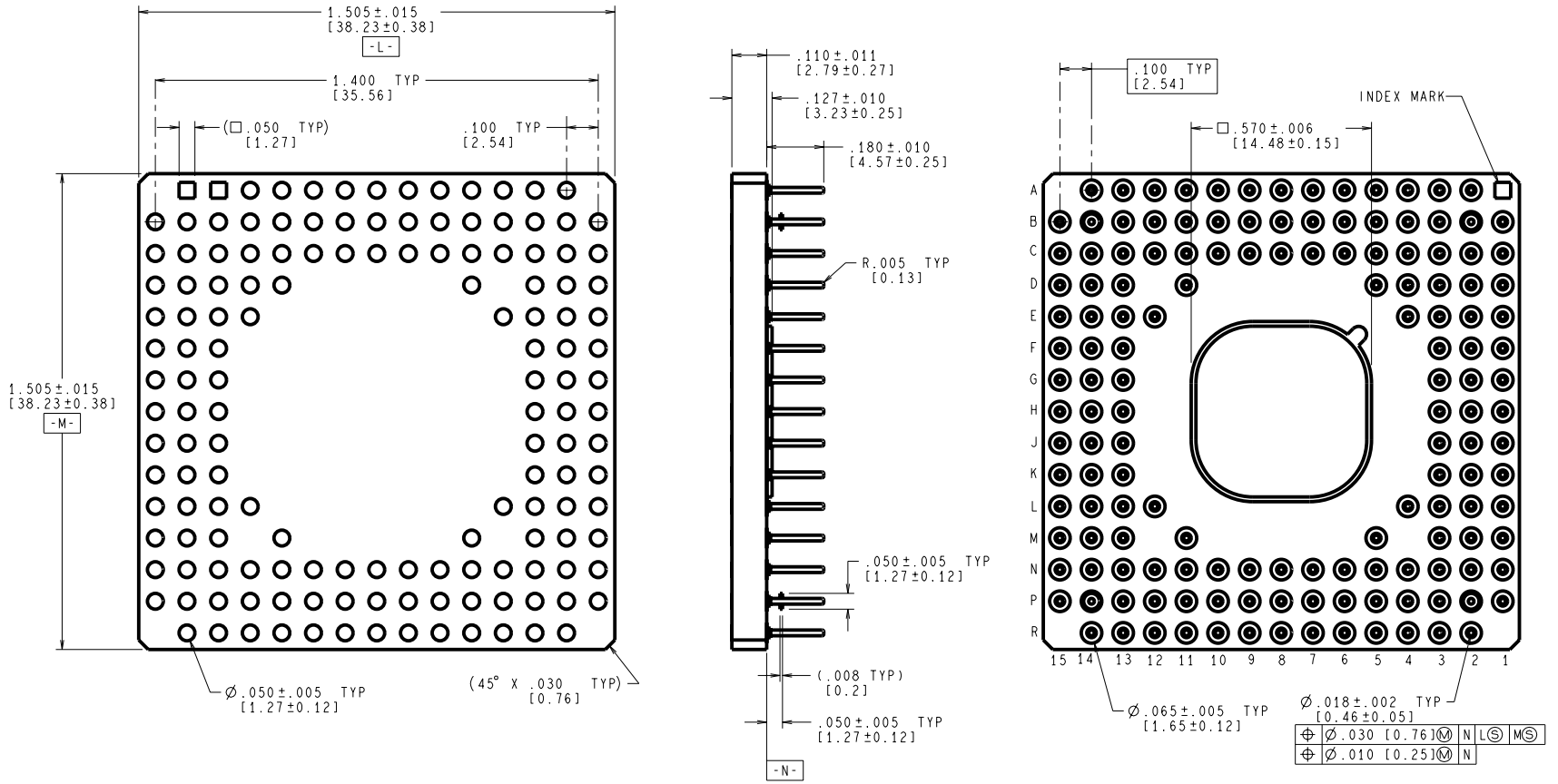
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	10729	12/06/94	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. PLATING: ALL EXPOSED METAL AND METALIZED AREAS TO BE GOLD PLATED 100 MICROINCHES/ 2.54 MICROMETERS MINIMUM OVER 80-350 MICROINCHES/ 2.03-8.89 MICROMETERS OF NICKEL.
2. NO JEDEC REGISTRATION AS OF 12/06/94.

APPROVALS	DATE
DRAWN MARTA SUCHY	12/06/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

PIN GRID ARRAY, CERAMIC, 149 PIN, CAVITY DOWN

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-UA149A	A

DO NOT SCALE DRAWING | SHEET 1 of 1