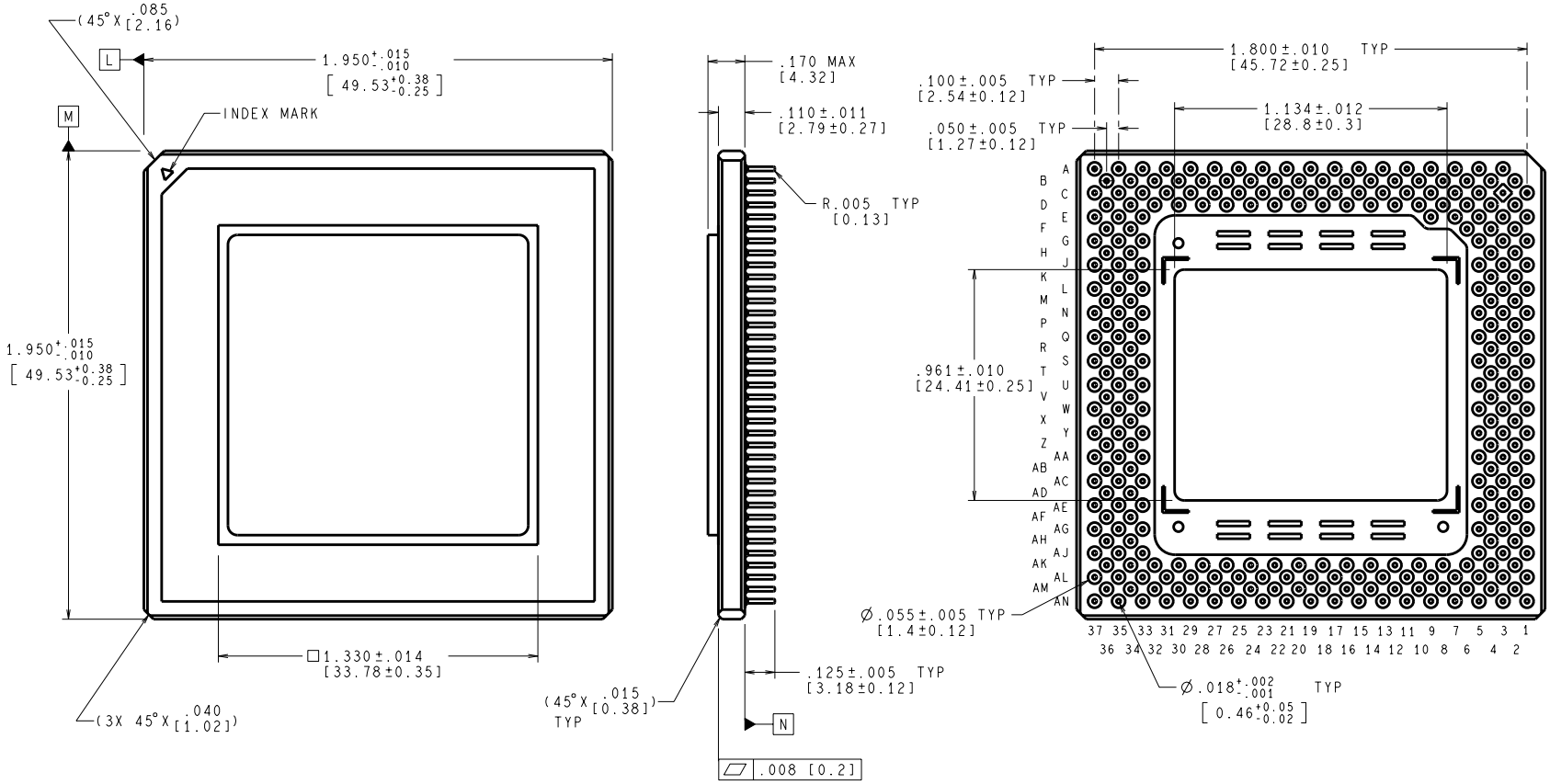
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11972	05/21/1998	TL/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. PLATING: ALL EXPOSED METAL AND METALLIZED AREAS TO BE GOLD PLATED 50 MICROINCHES/ 1.27 MICROMETERS MINIMUM OVER 50 TO 350 MICROINCHES/ 1.27 TO 8.89 MICROMETERS OF NICKEL.
2. NO JEDEC REGISTRATION AS OF MAY 1998.

APPROVALS	DATE
DRAWN T. LEQUANG	05/21/1998
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CPGA, 1.95X1.95X.110 IN BODY,296 PIN, .050 IN PITCH, CAVITY DOWN

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-UA296A	A

DO NOT SCALE DRAWING | SHEET 1 of 1