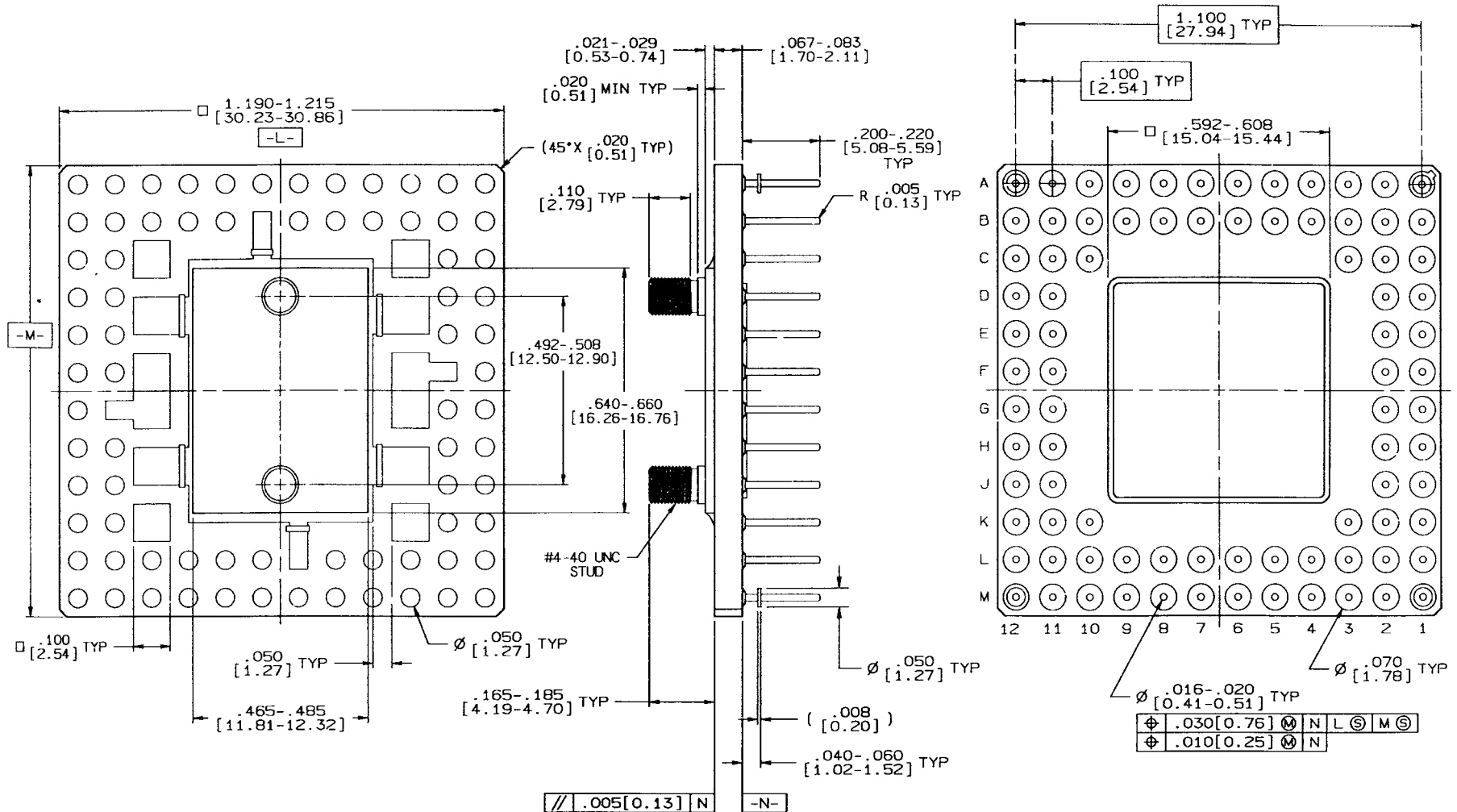
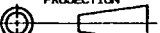


REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	09632	04/23/93	KES/ <i>SY</i>



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL EXPOSED METAL AND METALIZED AREAS TO BE GOLD PLATED 60 MICROINCHES/1.52 MICROMETERS MINIMUM OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS OF NICKEL.
2. NO JEDEC REGISTRATION AS OF 4-2-93.

CONTROLLING DIMENSION: INCH				
APPROVALS		DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DRAWN Walt Stacenko		04/23/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
DESIGN CHK Marta Insley		05/06/93	PIN GRID ARRAY, CERAMIC, 84 PIN, CAVITY DOWN, W/STUD	
ENGR/CHK David Wells		5/6/93		
APPROVAL				
 PROJECTION 1st ANGLE		SCALE	SIZE	DRAWING NUMBER
		N/A	C	MKT-UA84E
		DO NOT SCALE DRAWING		SHEET 1 OF 1
				REV A