General Description

The WL-CSP housings with solder balls from ESPROS Photonics are wafer level chip scale packages for use in standard SMT assembly lines with standard SMT processes and equipments. Underfill is not required as far not necessary by the application or mentioned in the datasheet of the product.

The bumped die products have direct connections, without wires, to a printed circuit board by flipping the die and connecting by solder balls. The solder bumps are located on the active side of the silicon IC.

This application note gives advice on some important points of the process.

Features

- **Use of standard SMT assembly lines with standard SMT processes and equipments.**
- **High assembly yields resulting from the self-aligning characteristic of the low mass die during solder attachment.**
- **Considerable space savings: Package size equal to die size and smallest footprint per I/O count.**
- **Thinner package profile, due to bare die thickness. Wafer-thinned devices for opto-electronics applications.**
- **Improved electrical performance, such as reduced inductance and capacitance, due to the elimination of wire bonds and leads used in standard plastic packaging.**

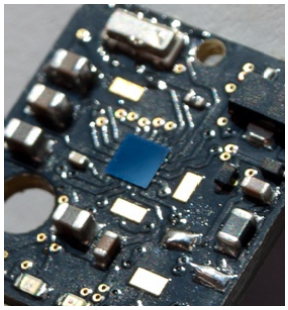

Figure 1: epc600 WL-CSP on PCB

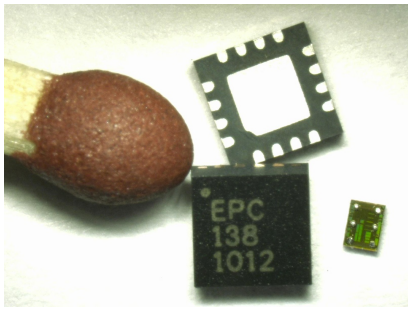

Figure 2: Size comparison
The head of a match vs. QFN-16 vs. CSP6

1. Process flow

epc CSP flip chip assembly follows standard SMT assembly processes:

- Printing of solder paste on PCB.
- Component placement uses standard SMT pick and place equipment.
- Standard SMT reflow process.
- Cleaning step (depending on type of flux used).
- Underfill (depending on chip size).

2. Recommended PCB design guidelines

2.1. SMT Footprint Design

For PCB fabrication the following two types of PCB pads/land patterns, referred in Figure 3, are used for surface mount assembly:

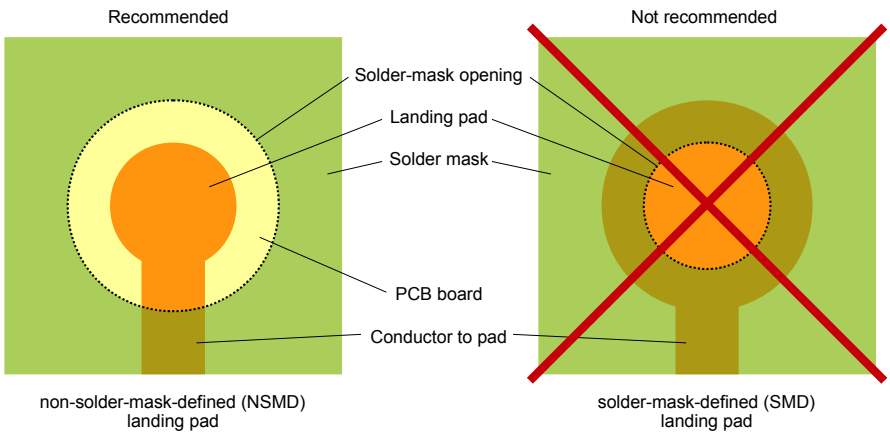

Figure 3: Basic foot print designs

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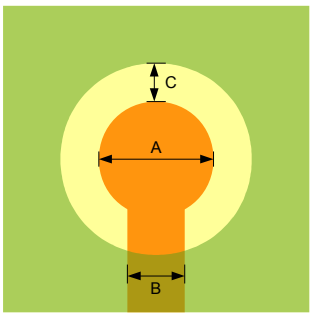
- Non-solder mask defined (NSMD):
  The metal pad on the PCB (to which a package I/O is attached) is smaller than the solder mask opening.
  We recommend NSMD pads for CSP, because the copper etching process has a better definition than the solder masking process and improves the reliability of solder joints.
- Solder mask defined (SMD):
  The solder mask opening is smaller than the metal pad.
  Not recommended, because lower pitches may not utilize this layout due to PCB limitations and a misalignment of the solder mask can cause failures.

The design of the landing pads has to follow the recommendations for trace, space and solder mask capabilities of the PCB manufacturer. The recommended pad geometry in Table 1 is for the use of fine-line PCB board:

Dimension	Ref.	Fine-line PCB
Pitch		(450µm)
Landing pad diameter on chip		(140µm)
Landing pad diameter on PCB	A	max. 300µm
Line width	B	[min. 150µm]
Ratio line to landing pad	B / A	max. 50%
Space line to line		[min. 150µm]
Space line to solder mask	C	[min. 100µm] max. 100µm for solderable lines



Remarks: (...) Dimensions defined by chip; […] Dimensions defined by PCB design rules

Table 1: Recommended PCB design guidelines e.g. epc300

For the NSMD pad geometry the designer has to take care of the wettable area of the connection lines to the landing pad to have a limited solder drain. The trace width at the connection to the landing pad should be as small as possible and must not exceed 50% of the pad diameter. The distance from the solder mask to the landing pad needs to be a minimum. When designing the board, the solder mask registration capability of the board manufacturer should be checked to ensure that the solder mask opening dimension is maximum 100 µm on either side of the copper pad. The fan-out for the traces should be symmetrical and balanced across X and Y directions to avoid part rotation due to surface tension of solder, refer to Figure 4.

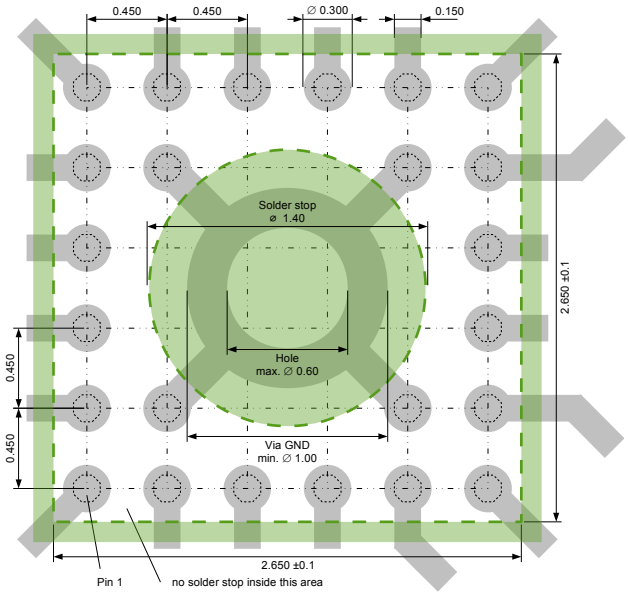


Figure 4: Example of a recommended, balanced fine-line PCB design for epc600

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2.2. Board material

Standard epoxy glass substrates are compatible with the CSP process. Assembly can be performed on standard epoxy glass substrate; however, changing from standard FR-4 to high temperature FR-4, which has a smaller thermal expansion, improves package reliability.

A copper layer thickness of less than 35µm (1 oz) is necessary to achieve the required definition. Greater copper thickness results in a lower NSMD and SMD pad definition.

We do not recommend the use of via-in-pad to prevent voiding of the solder joint due to uneven planarity of the pad.

The finish layer on the metal pads has a significant effect on assembly yield and reliability. Organic surface preservative (OSP), immersion tin or electroless nickel/immersion gold with gold thickness limited to <0.2 µm is the most appropriate finish. HASL (Hot Air Solder Leveled) board finish is not recommended.

3. Stencil Printing

When CSPs become incorporated into standard assembly processes, particular attention should be paid to the paste printing.

3.1. Solder volume: Stencil design considerations and thickness

The stencil should be laser cut and electropolished. The polishing helps in smoothing the stencil walls, which results in better paste release. The stencil should be maximum 100µm (4mil) thick, even better 80µm (3mil). We recommend to reduce the apertures in the stencil for the landing pads by 10% compared to the landing pads on the PCB board.

3.2. Solder paste and printing

For fine pitch printing solder paste with a small particle size is suggested. Use type 4.5 or finer (preferably 5) solder paste for printing 0.3mm diameter landing pads. Type 4 paste is not recommended. Due to the limited space available underneath the part after reflow, use "no-clean" type. A good choice is SAC305 solder paste (SnAg3Cu0.5) with no-clean flux. Furthermore we suggest using metal squeegees. Its pressure and speed need to be well controlled during printing. The usual in-process controls (for example, print height) should be applied.

4. Pick-and-Place

Component placement uses standard SMT pick and place equipment for SMT flip chip mounting. No need of die preparation, because epc's bare silicon dies are not moisture sensitive (moisture level MSL 1).

4.1. Machine Capability/Requirements

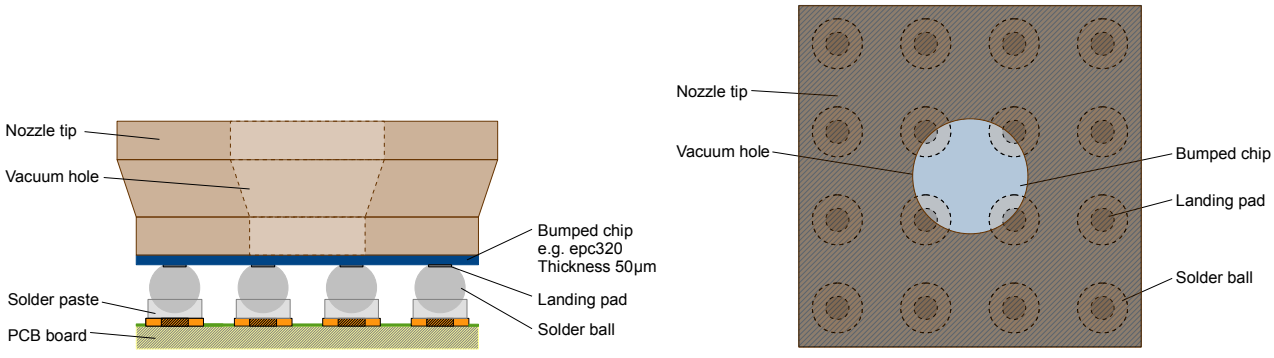
Pick and Place machine capability should have a repeatability and accuracy capable of placing 0402 components or better. Standard feeders for tape and reel can be used. Automated placement with vision alignment should be used to place the parts.

Placing by use of the standard fiducials on the panel works well. Local fiducials are not necessary required. epc's CSP devices with solder bumps self-align when placed at an offset due to self centering nature of solder.

Attention should be given to z-height placement to insure that the balls or thin chips are not damaged (compressed) during placement. The placement force should be kept to a minimum to slightly press the balls into the solder paste.

4.2. Nozzle

To minimize mechanical damage, the pickup tool must have a compliant tip. Standard nozzles will easily pick up the part. Recommended is a plastic or ceramic tips with a contact area equal to the chip size, refer to Figure 5.



side view of the tip

top view of chip - minimum contact area of the tip

Figure 5: Pick & place tool for epc320

5. Solder Reflow

epc's CSP devices are compatible with industry standard reflow process for both lead-free (RoHS) and Sn/Pb eutectic solder compositions to form solder joint interconnections. They are qualified for reflow operations +260°C peak for 4 sec. per JEDEC-STD-020. Nitrogen purge is not necessary, but an advantage during reflow.

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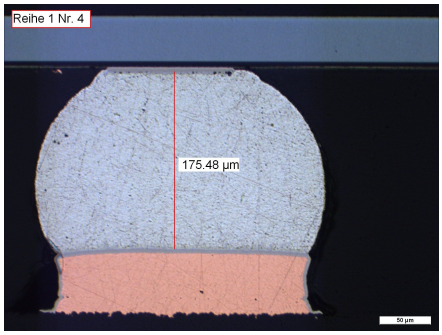

Figure 6: Cross section of a solder ball:
epc600 on top of a fine-line PCB

Once reflowed the WL-CSP package remains fragile and should be protected against mechanical contact.

6. Cleaning

No cleaning is necessary, if solder paste with no-clean flux is used. Otherwise the cleaning step depends on type of flux used.

7. Underfill

Underfill of the components reduces stress to the solder pads caused by e.g. temperature cycling or mechanical bending.The thermal and mechanical fatigue will be reduced and the longterm reliability will be increased. Underfill and underfill selection is application specific. It shall follow JEDEC-STD JEP150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface- Mount Components.

8. Inspection

Regular quality inspections per lot are suggested. Cross-sections of the bumps show voids, oxides and solder failures can be detected easily.

9. Wafer-thinned and opto-electronics devices

Note that the CSP balls, wafer-thinned devices (e.g. 50µm thickness) and optical surfaces are very fragile. Care must be taken during handling and assembly to avoid touching the CSP device. Therefore, they should be machine placed with appropriate and clean tooling.

With tooling for “use only for optical devices” you can keep the surfaces clean and prevent of any damages of the very sensitive surface of photosensitive parts.

For very thin and fragile devices the transmission of forces must always be on the landing pads to avoid cracking.

10. Rework

A replacement of the component, before underfilling is started, is possible using the appropriate standard rework equipments.

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POLYTEC GmbH Polytec-Platz 1 - 7 D -76337 Waldbronn GERMANY
Tel: +49 (72 43) 604 1730 Fax: +49 (72 43) 6 99 44 E-Mail: oek@polytec.de www.polytec.de