Fully integrated configurable light barrier driver & receiver

RoHS Compliant

General Description

The epc110 is a general purpose, fully integrated self-contained CMOS circuit to be used in light-barrier applications.

The chip contains a controller which drives an LED, typically an IR-LED. The LED is used in a pulsed mode to increase the signal-to-noise ratio even when there is very strong sunlight biasing the photo diode.

It contains also a high sensitive photo diode amplifier and a signal conditioning circuitry to cancel unwanted environmental light including strong sunlight and pulsed light sources. The receiver is built around a synchronous demodulator circuitry. Two output signals with different threshold levels are implemented in order to trigger the light barrier output or to indicate light reserve.

The chip also includes a power supply circuitry to establish all internally required voltages from one source only.

It can be used either as a standalone device, forming the whole core of an industrial light barrier. It can also be used together with a micro-controller (µC) for more advance applications.

Features

- Fully integrated light barrier chip
- Needs just a photo diode and a LED with a LED driver
- Customer configurable version
  for i.e. high sensitivity or high speed applications
- Integrated clock generator
- CSP10 package with very small footprint

Applications

- Light barriers ranging from millimeters to tens of meters
- Smoke detectors
- Liquid detectors

Functional Block Diagram

for 10-Pin Chip Scale Package (for 16-pin QFN Package)

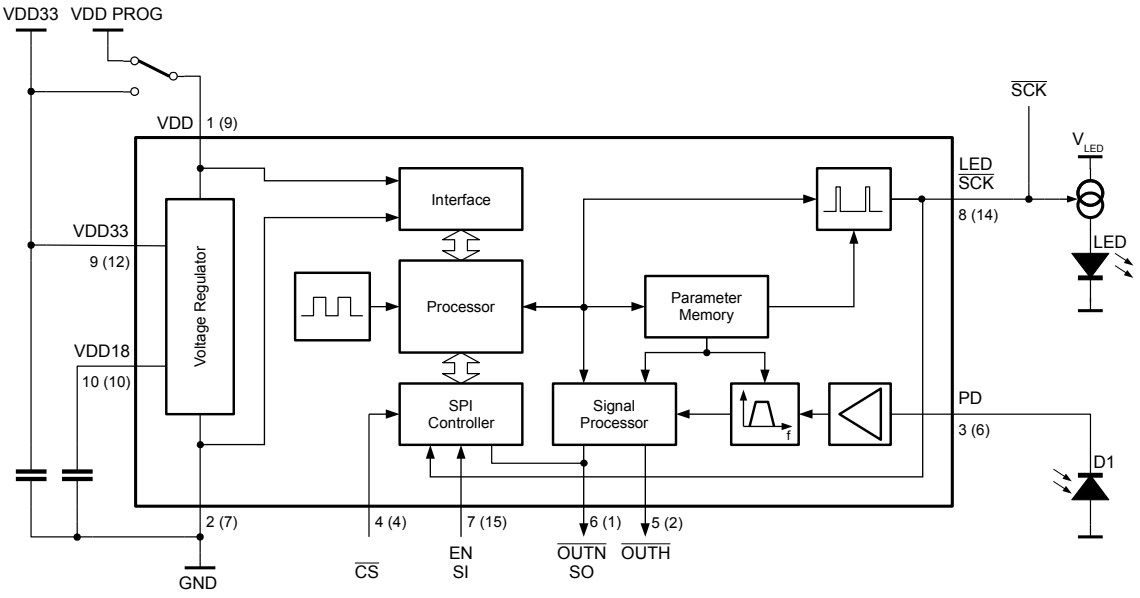

Figure 1: Block Diagram

Configuration	Fix-parameter mode	Dynamic mode	
standalone	**epc110**	**µC --> "SPI" --> epc110**	*Internal controlled light barrier read rate*
controlled	**"EN" --> epc110**	**µC --> "SPI / EN" --> epc110**	*External controlled light barrier read rate*
	Static parameters	*Ambient adaptive reading*	***Application***

Table 1: Configurations versus applications

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Absolute Maximum Ratings (Notes 1, 2)

Voltage at any pin except pin VDD	-0.3V to V_N +0.3 V
Power Supply Voltage at pin VDD	-0.3V to +5.5V
Programming Voltage at pin VDD	-0.3V to +8.0V
Power Supply Voltage at pin VDD33	-0.3V to +5.5V
Output current at any pin except pin LED	-6mA to +6mA
Power Consumption with maximum load	125 mW
Lead Temperature solder, 4 sec. (T_L)	+260°C

Recommended Operating Conditions

	Min.	Max.	Units
Operating supply voltage at VDD	3.0	3.6	V
Programming voltage at VDD	7.0	8.0	V
Operating supply voltage at VDD33	3.0	3.6	V
Operating Temperature (T_O)	-40°	+85°	C
Humidity (non-condensing)	+5	+95	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics.

Note 2: This device is a highly sensitive CMOS ac current amplifier with an ESD rating of JEDEC HBM class 0 (<250V). Handling and assembly of this device should only be done at ESD protected workstations.

Electrical Characteristics

3.0V < V_N < 3.6V, -40°C < T_A < +85°C, unless otherwise specified

General Data

Symbol	Parameter	Conditions/Comments		Values			Units
				Min.	Typ.	Max.	
V_N	Operating power supply voltage	at VDD33 (and VDD)		3		3.6	
V_{PUP}	Power-up Threshold Voltage	Voltage at VDD33 when the device starts up		2.4		3	V
V_{PP}	Ripple on supply voltage, peak to peak		Input pulse $I_{PD\ NST}$				
			36nA			70	mV
			48nA			150	mV
			72nA			350	mV
			108nA			600	mV
I_N	Current consumption operating	in operation mode, I_{PD} = 0 mA, no load				2	mA
I_{Prog}	Current consumption programming	in program mode, VDD @ 8.0V, I_{PD} = 0 mA, no load				4	mA
V_{OH}	Output high voltage	except $\overline{OUTH}$ and LED		V_N - 0.5V			V
V_{OL}	Output low voltage	@ 4mA source, including $\overline{OUTH}$ and LED				0.5	V
V_{HOH}	Output high voltage $\overline{OUTH}$	see Figure 8					
V_{LEDH}	Output high voltage LED	@ 0.1mA sink current		V_N - 0.5V			V
I_{LED}	Source current maximum	at Pin LED, V_{LED} @ 0... V_N - 1.0V		0.7		1.3	mA
V_{IH}	Input high voltage			0.7*V_N		V_N	V
V_{IL}	Input low voltage			GND		0.3*V_N	V
I_{LEAKD}	Input leakage current					10	µA
R_{PU}	Pull-up resistor	internal at digital input		30		200	kΩ
f_{clk}	Reference clock	of internal oscillator - for information only All internal timings are referenced to this clock			32		MHz
df_{clk}	Temperature drift	of the oscillator - for information only			640		ppm/K

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SPI Interface Data (for more details refer to “SPI Interface“)

Symbol	Parameter	Conditions/Comments	Values			Units
			Min.	Typ.	Max.	
$f_{\overline{SCK}}$	$\overline{SCK}$ Clock frequency				10	MHz
t_H	High period of $\overline{SCK}$		50			ns
t_L	Low period of $\overline{SCK}$		50			ns
$t_{rf\overline{SCK}}$	Serial clock rise / fall time of $\overline{SCK}$				20	ns
t_1	Edge time $\overline{CS}$ --> $\overline{SCK}$		50			ns
t_{SU}	Set-up time of SI		15			ns
t_{hold}	Hold time of SI		15			ns
t_D	Output data of SO valid after $\overline{SCK}$				20	ns
t_{rf}	Output data rise / fall time of SO				20	ns

Other Data (refer to “Functional Description“)

Symbol	Parameter	Conditions/Comments	Para-meter	Values			Units
				Min.	Typ.	Max.	
I_{PDN}	Photo Current Sensitivity $\overline{OUTN}$	Pulse height to trigger internal threshold $\overline{OUTN}$. Refer to Functional Description	SENSN	Programmable between 24...108			nA
I_{PDH}	Photo Current Sensitivity $\overline{OUTH}$	Pulse height to trigger internal threshold $\overline{OUTH}$. Refer to Functional Description	SENSH	Programmable between 60...144			nA
I_{pulse}	Maximum Input Pulse Current	If the input current pulse is above this level, the recovery time t_{REC} becomes t_{relax}. (refer to parameter t_{relax})				100	µA
I_{N_Imin}	Input related noise	@ I_{PDDC} =0				15	nA $_{RMS}$
I_{N_Imax}	Input related noise	@ I_{PDDC} =$I_{PDDCMax}$				20	nA $_{RMS}$
I_{PDDC}	DC Photo Diode Current	generated by ambient light with no effect to the sensitivity		0.0		2	mA
C_{PD}	Photodiode Capacitance	Refer to section Application Information, Photodiode Capacitance				50	pF
t_{Pulse}	LED Pulse Length		TPULSE	Programmable between 1…8			µs
t_{Cycle}	LED Cycle Time	for fork light barrier, standalone mode	TPER	Programmable between 5…100'000			µs
		for fork light barrier, controlled mode		controlled by EN input			
t_{relax}	Recovery time	after a strong current pulse (I_{pulse} = 100µA)				50	µs
t_R	Response Time	Minimum time from light beam detection to status change of the output $\overline{OUTN}$ or $\overline{OUTH}$. t_{R_MAX} = (n_V + 1) * t_{Cycle}	refer to t_{Cycle} / n_V	Programmable between 10µs...3.3s			
t_F	Release Time (fall time)	Minimum time from beam interruption to status change of the output $\overline{OUTN}$ or $\overline{OUTH}$. t_{F_MAX} = (n_M + 1) * t_{Cycle}	refer to t_{Cycle} / n_M	Programmable between 10µs...54.6min			
n_V	Valid pulse counts	Number of weighted valid (non-missing) pulses to trigger the output. Refer to Functional Description	INC	(Programmable between 1…32 pulses)			
n_M	Missing pulse counts	Number of weighted missing pulses to release the output. Refer to Functional Description	DEC	(Programmable between 1…32'767 pulses)			

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Other Parameters

(typical values, T_{amb} = 25°C, V_{DD} = 3.3V)

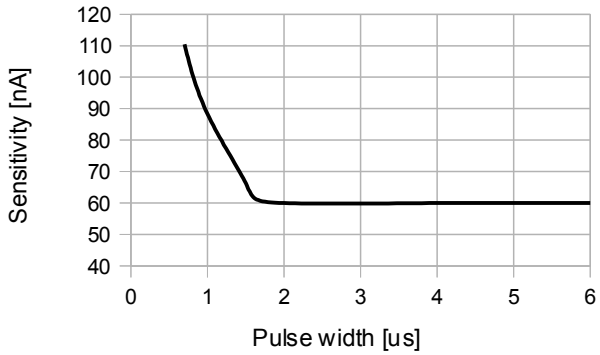

Figure 2: Input Sensitivity vs. LED pulse width

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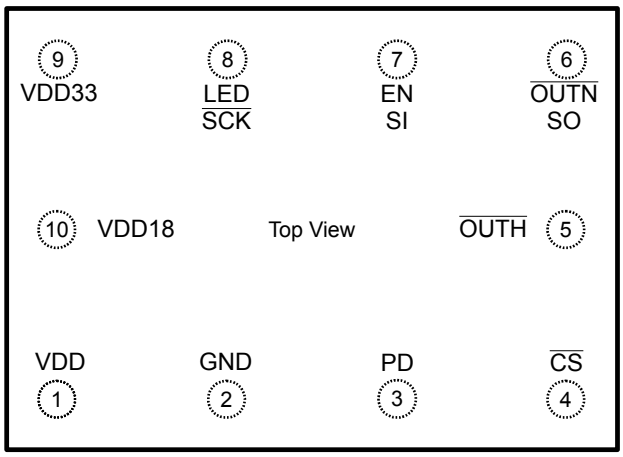
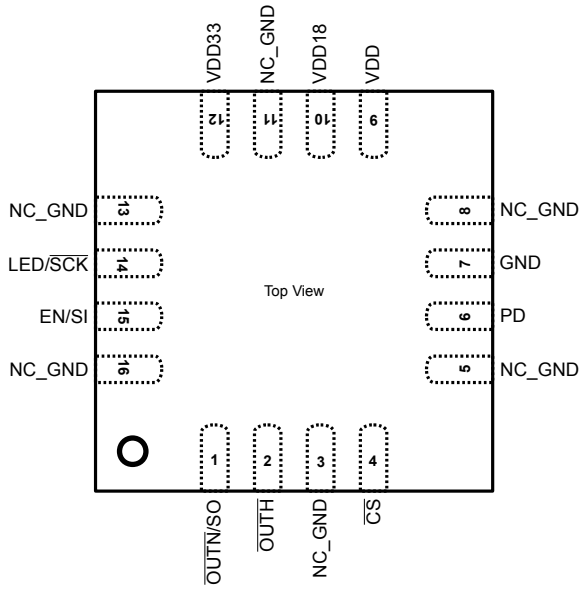
Connection Diagrams



10-Pin Chip Scale Package (CSP)



16-Pin QFN Package
Note: For sampling only. Limited quantities. Please inquire.

10-Pin CSP	16-Pin QFN	Pin Name	Type	Description
1	9	VDD	Power Supply	Positive power supply. Operation mode: to be connect to VDD33. During command PROG: to be connected to programming voltage.
2	7	GND	Power Supply	Negative power supply pin.
3	6	PD	Analog Input	Photo diode input.
4	4	CS	Digital Input	Terminated with internal pull up resistor Light barrier: Mode selection: CS = 1: Operation Mode (LED, EN, OUTN active) SPI interface: Chip select, CS = 0: Command/Program Mode (SCK, SI, SO active)
5	2	OUTH	Digital Output Load depending	Light reserve detected - see Figure 8. Refer to section Light Reserve Output OUTH Open drain output
6	1	OUTN SO	Digital Output	Open drain output Light barrier: Light pulses detected, amplified and filtered signal see Functional Description SPI interface: Serial data output
7	15	EN SI	Digital Input	Terminated with internal pull up resistor Light barrier: Fork light barrier controlled mode: LED pulse stimulation Fork light barrier standalone mode: No function. SPI interface: Serial data input
8	14	LED SCK	Digital Output Digital Input	Light barrier: Output to LED driver SPI interface: Serial input/output clock. For start/stop condition of SPI communication (while CS = 1): Set SCK =1 and SCK line in tristate mode (high ohmic)
	12	VDD33	Power Supply	Positive power supply.
10	10	VDD18	Decoupling	Pin for external filter/decoupling of the internal 1.8V supply: 4.7nF ceramic type Not for supply of external circuits
n/a	3, 5, 8, 11, 13, 16	NC_GND		Not connected. Connect this pins to GND (Guarding).

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Functional Description

Light barrier applications

To cover different aspects of applications the epc110 device can operate in various modes:

1. **Standalone mode**
   The LED flashes in a predefined/programmed cycle time.
2. **Controlled mode together with a micro-controller**
   The LED pulse starts on the positive edge of the input EN. The light is detected while the enable signal EN is high.
3. **Fix-parameter mode**
   This is the use of a pre-programmed parameter setting all the time. Usually the programming takes place during configuration and test period of the board.
4. **Ambient adaptive reading by dynamic parameters**
   In this mode the micro-controller is doing the parameter setting during the operation mode. For the communication the SPI interface is used. For more technical details refer to chapter “SPI Interface“.
   Application is for enhanced functionality and requirements as additional filtering of environmental ac light, adjustments of the sensitivity on the fly, controlling the LED current by micro-processor, etc. Example of a sensitivity control: The photo diode current is compared to two threshold levels. The result from the higher comparison (OUTH) may be used to regulate the LED current as well the photodiode receiving parameters appropriate to the environmental conditions.

Light barrier application without an additional controller

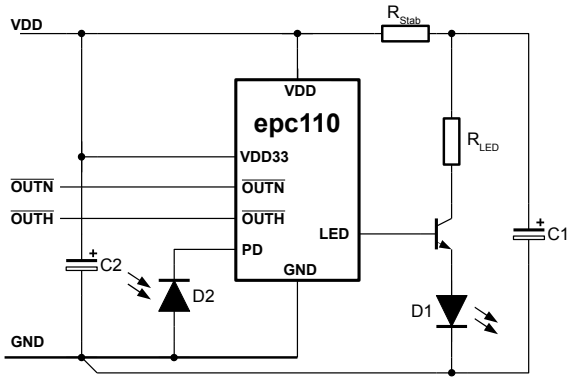

Figure 3: Principle of standalone light barrier application

Figure 3 shows the epc110 in a light barrier application with minimal part count. The LED flashes with a predefined rate. If the current of the light reflected (e. g. from a diffuse reflecting object or a retro reflector) to the photo diode at pin PD exceeds the threshold val ue I_{PDN}, the output OUTN goes to the low state for a time which is longer than the time to the next LED pulse. Thus, the signal at the pin OUTN is constantly low when the photo diode generates a photo current which exceeds the threshold level. The stored flashing parameters of the LED can be programmed using the SPI interface described in this manual.
The photo diode current is compared to two threshold levels. The result OUTH from the higher comparison level may be used to detect the light reserve.

Light barrier application using a micro-controller

If additional functionality is required in a specific application, a micro-controller can be used. Such additional requirements can be power saving modes, additional filtering of environmental ac light, counting purposes, etc. In this configuration, the LED emits one light pulse on the positive edge at the pin EN. The photo diode bias and amplifier chain is enabled while the enable signal EN is high so a light pulse can be detected.

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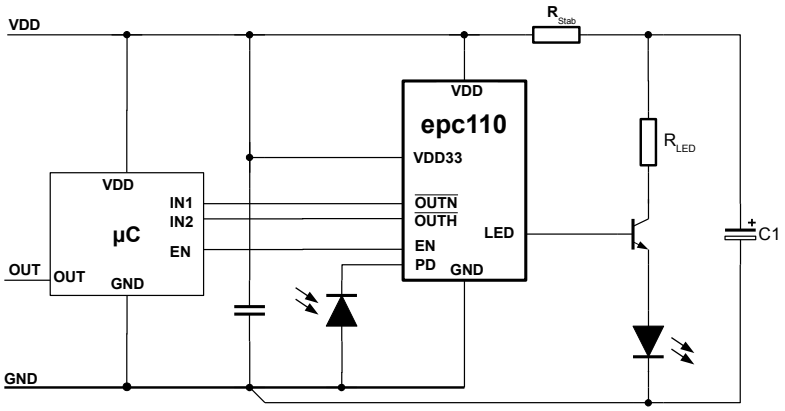

Figure 4: Principle of controlled light barrier application using a micro-controller

The photo diode current is compared to two threshold levels. The result $\overline{OUTH}$ from the higher comparison level may be used to detect the light reserve.

Evaluation of a single light pulse

The photodiode is operated against ground and is reverse biased at a constant voltage of 1.2V. The input impedance of pin PD is kept low (<1 kOhm @ 100kHz) in order to minimize the influence of the parasitic capacitance of the photodiode. To ensure proper operation under high ambient-light conditions, the photo diode DC current can be up to 2 mA.

The resulting current from the light pulses are converted to a voltage, filtered, amplified and compared to two different threshold levels. The lower threshold SENSN (input related 60nA typical) is used for the detection of the signal, the higher threshold SENSH (input related to 96nA typical) is used to provide an output when a certain signal reserve is achieved.

To detect the received light pulse properly, the given threshold must be at least five times higher than the rms value of the noise floor generated by the circuitry without AC light stimulation.

The comparator results are digitally filtered and output at pin $\overline{OUT}$ and $\overline{OUTH}$.

The parameter TPER defines the scan period in the standalone light barrier application but has also an impact to the settling time of the receiver in the controlled mode application. It this case it has to be set corresponding to the scan period. Refer to the description of the TPER command.

For each single light pulse, received and detected by the photodiode, the threshold levels for output $\overline{OUTN}$ and for output $\overline{OUTH}$ can be set by programming (parameter SENSN resp. SENSH). They are processed according to the following principle to propagate the output signals $\overline{OUTN}$ and $\overline{OUTH}$ resp. $OUTN_{INT}$ and $OUTH_{INT}$. As far the received light pulse signal exceeds the corresponding threshold level, the pulse will be recognized as a valid pulse and the detection circuit sets the appropriate output signal $OUTN_{INT}$ or $OUTH_{INT}$.

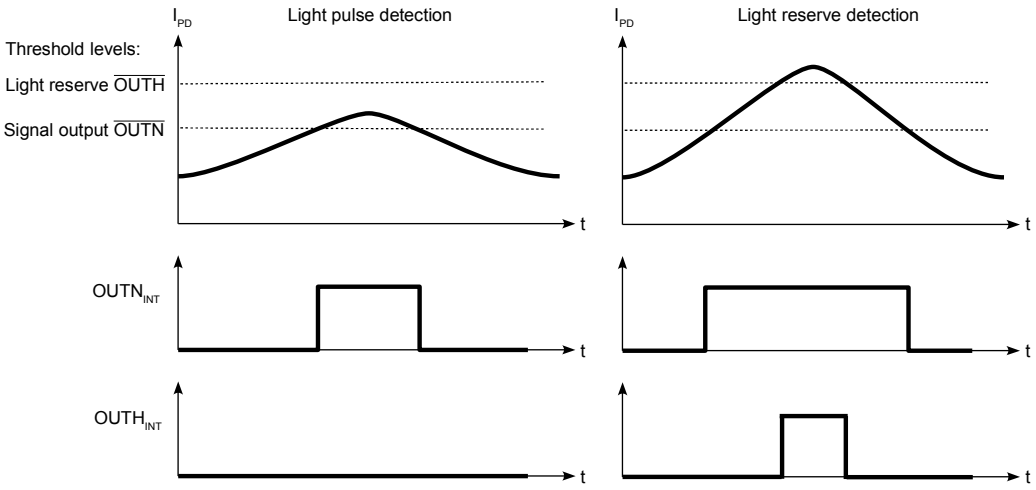

Figure 5: Pulse evaluation

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Pulse Modulated Operation (e.g. $OUTN_{int}$ to $\overline{OUTN}$)

The epc110 chip operates the LED and the receiver path on a pulse modulated concept. Thus, the LED is operated with short pulses whereas the receiver channel does synchronous demodulation of the received light pulses by reading the current pulses of the photo diode. This concept allows a very high sensitivity, high speed operation, and a high suppression of input ambient or foreign light (DC currents) generated by sunlight or other DC light sources like light bulbs. The pulse length is set by the parameter TPULSE.

In the standalone mode the whole system is clocked by the scan period defined by the programmed parameter TPER. In the controlled mode the timing is propagated from the external signal EN (positive edge, synchronized on the internal clock).

In order to eliminate interference caused by modulated light, e.g. a flashing light or by other light barriers, the input signal from the photodiode is amplified, filtered, and processed by an integrated signal processor. If the photo diode signal meets the required frequency, pattern and amplitude, the output(s) are triggered. The following timing diagram shows the basic concept.

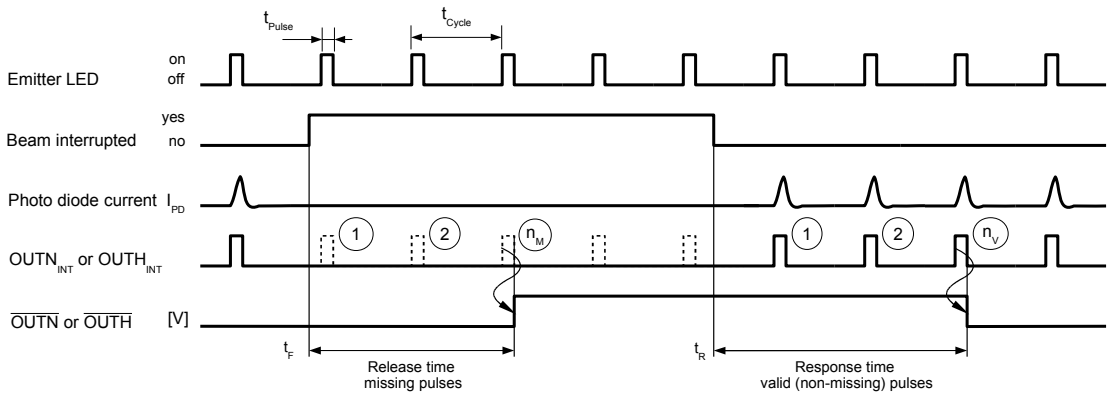

Figure 6: Pulse modulation concept

It is in fact a digital filter which counts missing and non-missing pulses to change the ou tput state of $\overline{OUTN}$ or $\overline{OUTH}$.

Working principle of the digital filter e.g. for the signal $OUTN_{int}$ to OUTN Filter:

The aim of this programmable filter is to suppress single pulses, so they cannot trigger the output and generate a false signals.

This filter is based on a counter, which is counting up (increment) the valid pulses and counting down (decrement) the missing pulses in a weighted manner. Separate weighting factors can be selected for valid pulses (parameter INC) and missing pulses (parameter DEC). If the counter reaches the upper limit (maximum count, response time), the signal $\overline{OUTN}$ is set to LOW. Similar in the opposite direction, if the counter reaches zero, the lower limit (minimum count, release time), the signal $\overline{OUTN}$ is put to HIGH. With the parameters INC and DEC the filter has the advantage of individual selectable gradients of the slopes. Counter will never exceed maximum nor minimum limit. In between it acts as an integrator of both parameters.

IF Pulse then

- IF Pulse = valid then
  Counter = Counter + (INC * 1024 for INC > 0 and 32 * 1024 for INC = 0)
  IF counter > 2^{15} (maximum limit) then Counter = maximum limit
  IF counter = maximum limit then $\overline{OUTN}$ = 0
- IF Pulse = missing then
  Counter = Counter - (2^{DEC})
  IF counter < 0 (minimum limit) then Counter = minimum limit
  IF counter = minimum limit then $\overline{OUTN}$ = 1

ELSE wait for Pulse

Lets assume that the photo diode does not receive light pulses for a long time: This means the light beam is interrupted. Then $\overline{OUTN}$ is at high level. If the light beam is not anymore interrupted, the photodiode receives light pulses which are strong enough to trigger the $OUTN_{INT}$ threshold and the internal pulse evaluation unit (designated in Figure 5 with 'Pulse evaluation') starts to count the receiving pulses. If the number of received pulses reach the set level n_V, the output $\overline{OUTN}$ turns to low level. Thus, single pulses cannot trigger the output and generate a false signal.

The same procedure is used when a beam changes from not interrupted to interrupted. The internal pulse evaluation unit counts the missing pulses. If the number of missing pulses reaches the set level n_M, $\overline{OUTN}$ is turned to high level.

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The same principle applies to the counter and signal of $\overline{OUTH}$.

The parameter INC defines the delay n_V in number of clock cycles from the start of a pulse chain to the negative edge of $\overline{OUTN}$.
The parameter DEC defines the delay n_M from the end of a pulse chain to the positive edge of $\overline{OUTN}$.

Application example	No. of Pulses n_M	No. of missing Pulses n_V
Long range	8	8
High speed	3	2

Table 2: Example: Settings based of filter coefficients INC and DEC

Light Pulse Detection Output $\overline{OUTN}$

The epc110 contains two digital outputs to indicate that a valid signal of light pulses are received by the photo diode. The first output $\overline{OUTN}$ is triggered, when the lower threshold is reached by the input signal (see Figure 5). This output is used usually to drive the output of the light barrier. This is a fully CMOS compatible digital output.

Light Reserve Output $\overline{OUTH}$

However, if the incoming signal is just at the trigger threshold of $\overline{OUTN}$, an unstable situation can occur. Thus, a second output $\overline{OUTH}$ is integrated with a higher trigger threshold to indicate that a certain 'light reserve' is reached (see Figure 5). This output is usually used to drive a visible LED to indicate to the operator a stable detection function of the light barrier. To have not too short pulses $\overline{OUTH}$, this signal is stimulated by signal $\overline{OUTH}$ Filter and synchronized reseted by $\overline{OUTN}$.

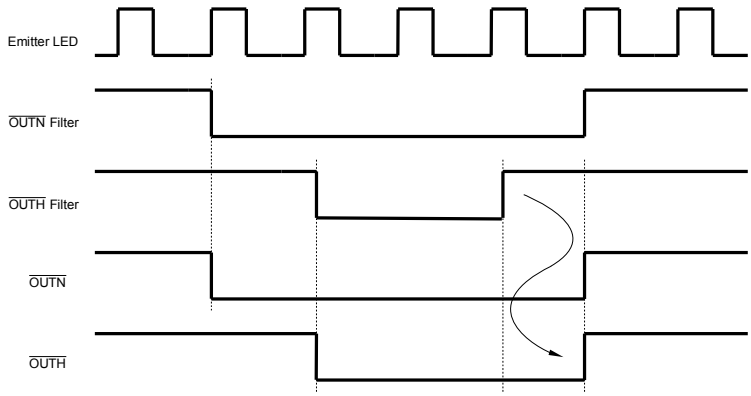

Figure 7: synchronization $\overline{OUTH}$ with $\overline{OUTN}$

The trigger threshold of $\overline{OUTH}$ is set usually approx. 50% above the trigger threshold of $\overline{OUTN}$.

This output is not CMOS compatible. Its voltage is depending of the load according to Figure 8.

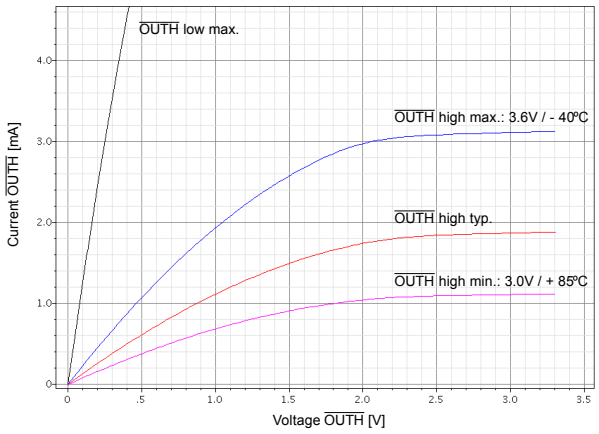

Figure 8: Output voltage versus output current of output $\overline{OUTH}$

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To have still digital compatible signals a level conversion is necessary. Below you find some examples for such circuits for converting $\overline{\text{OUTH}}$ levels to full CMOS compatible digital output.

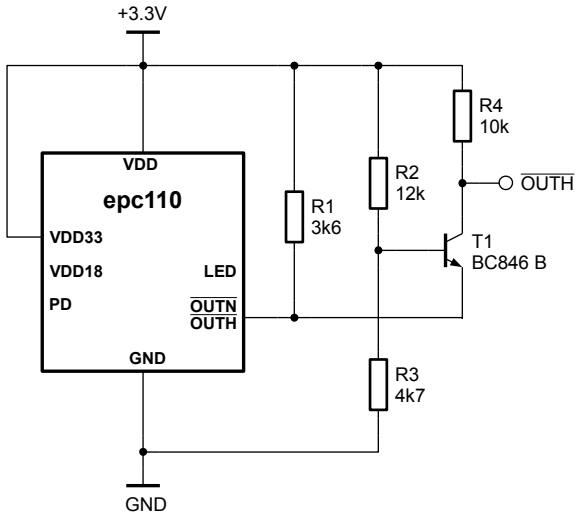

Figure 9: Non-inverting, low power level shifter (additional current approx. 0.6mA)

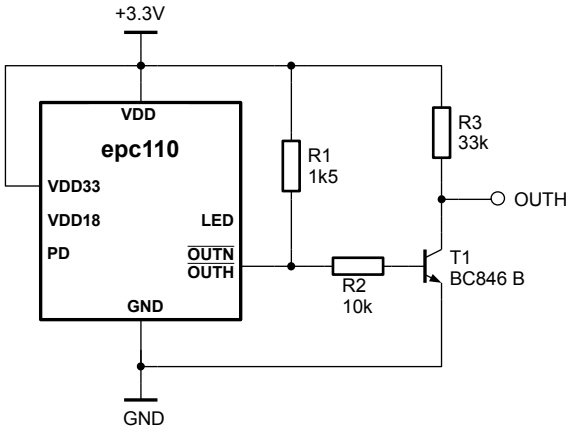

Figure 10: Simple inverting level shifter (additional current approx. 1.6mA or 2.6mA)

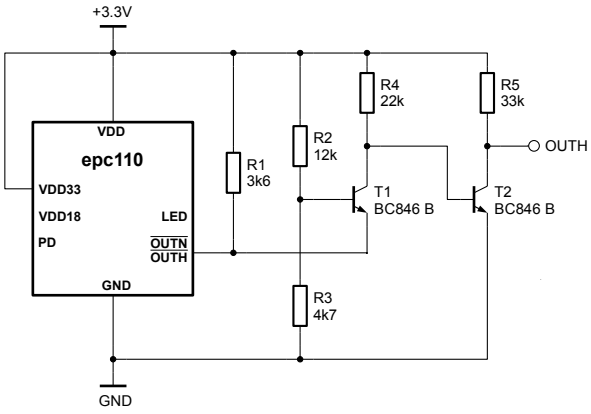

Figure 11: Inverting, low power level shifter (additional current approx. 0.8 ... 1.0mA)

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Parameters

The parameters are defining the functionality of the epc110. The big variety of possible settings allows to cover a wide range of applications.

The devices contains a memory to store the application parameters. They are stored into 16bit registers. The registers are organized into 2 blocks: a volatile and a non-volatile one.

Parameter Memory Organization (epc110)

The following classes of data are stored for each device:

- Application parameters
- Unique chip ID and chip adjustments (factory set)

This data can be permanently stored in a read-only memory (ROM)[1] and is mirrored in a volatile memory (RAM). At power up, the data (except the chip ID) is copied from the ROM to the RAM. During operation, the data from the RAM is used. Both memories are organized in 16 registers at 16 bits each. The data can be accessed on a 16-bit register base.

If a register has been burned (=stored into the ROM) the first bit is set: FUSEBIT = 1. If VMODE = 1 is selected, the register cannot be modified any more nor in RAM nor in ROM area. For VMODE = 0 the RAM area is still accessible.

So far the chip can be operated in two different modes:

- **Fix-parameter mode VMODE = 1: e.g. as standalone or pre-configured device**
  Operated with not modifiable data from RAM, which are stored permanently in ROM.
- **Dynamic mode VMODE = 0: e.g. for adaptive systems, dynamic systems**
  Operated with modifiable data from RAM. The SPI interface allows to modify these data in the RAM area at any time on the fly.
  At power up these data are loaded from the permanent stored data in the ROM. If the run-time configuration differs from the data set stored in the ROM, it has to be restored after each power-up again by the external micro-processor over the SPI interface.

The following table shows the memory organization:

Non-Volatile Memory Address Range (Register no.)	Volatile Memory Address Range (Register no.)	Description
0 - 3	16 - 19	Application parameters
4 - 6	20 - 22	Trim values, factory set
7	23	Device Address (not applicable)
8 - 15	-	Chip ID, factory set
-	24 - 31	For factory test purpose. Read only.

Table 3: Memory map overview

As shown in the table above, registers 0 – 3 are used for configuring the chip in the application. Before the devices can be used in a final light-barrier system, the required application parameters of the chip in the system have to be stored into the device memory.

The following table shows the allocation of the available parameters in the memory of the epc110:

			Bit #																
	ROM	RAM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Register #	0	16	VMODE	MODE			1	0	0	0	0	0	0	TPULSE			POL	FUSEBIT	Application parameters
	1	17	TPER			DEC				0	0	INC				0	0	FUSEBIT	
	2	18	0	0	0	0	1	0	1	0	1	SENSH			SENSN			FUSEBIT	
	3	19	don't use															FUSEBIT	
	4	20	don't use															FUSEBIT	Trimming
	5	21	don't use															FUSEBIT	
	6	22	don't use															FUSEBIT	
	7	23	don't use															FUSEBIT	Device Address
	8	24	Lot no. LSB															FUSEBIT	Chip ID
	9	25	Lot no. MSB															FUSEBIT	
	10	26	Chip ID															FUSEBIT	
	11	27	Factory use only															FUSEBIT	
	12	28	Revision no.															FUSEBIT	
	13	29	no function															FUSEBIT	
	14	30	no function															FUSEBIT	
	15	31	no function															FUSEBIT	

Figure 12: Detailed memory map epc110

1 The non-volatile memory is a one-time-programmable memory (OTP). Once the memory is programmed, the programmed values cannot be overwritten anymore.

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Parameter settings can be done by writing complete 16 bit registers only.

Bits marked up in white fields shall be modified or programmed only. Gray marked bits with a given value in the memory map above must be set to this. Never change the memory content of gray marked cells without numeric indication. Writing to this cells is not allowed.

The RAM can be written only, if the corresponding ROM memory hasn't been written before (FUSEBIT = 0) or if the volatile mode is active (VMODE = 0). The first bit of each 16-bit ROM register serves as write inhibit bit (FUSEBIT). To write to the ROM, the micro-controller has to write the data to the RAM first (with FUSEBIT = 0). From there, the micro-controller can first double check the data integrity. When a memory section is verified, the content can be transferred from the RAM memory to the ROM using the command PROG (refer to chapter Command PROG). While processing this instruction the FUSEBIT will be set to "1" by epc110.

The device is fully operational as well without programming the ROM, but data will be lost at power down. Operating the chip in this mode is helpful during the development of the product or if your application needs an adaptive mode. However, in the final application for a standalone or self-reboot operation, the parameters must be stored into the ROM memory.

Parameter Description (epc110)

<table>
<tr><th rowspan="2">Parameter Name</th><th colspan="2">Register No.</th><th>Bit No.</th><th>Function</th></tr>
<tr><th>ROM</th><th>RAM</th><th></th><th></th></tr>
<tr><td>FUSEBIT</td><td>0</td><td>16</td><td>0</td><td>During write operation to this RAM register, put this bit = 0.
This bit will be set automatically, when corresponding ROM register is programmed.</td></tr>
<tr><td colspan="4"><table><tr><th>0</th><th>Values</th></tr><tr><td>0</td><td>The corresponding ROM register is not programmed</td></tr><tr><td>1</td><td>The corresponding ROM register is programmed</td></tr></table></td></tr>
<tr><td>POL</td><td>0</td><td>16</td><td>1</td><td>Polarity of the LED pulse. Setting is depending on the LED driver circuitry.</td></tr>
<tr><td colspan="4"><table><tr><th>1</th><th>Values</th><th>Default</th><th>Recommended Setting</th></tr><tr><td>0</td><td>active high  </td><td>X</td><td>X</td></tr><tr><td>1</td><td>active low  </td><td></td><td></td></tr></table></td></tr>
<tr><td>TPULSE</td><td>0</td><td>16</td><td>4...2</td><td>Pulse length t_{Pulse} of the light pulse</td></tr>
<tr><td colspan="4"><table><tr><th>4</th><th>3</th><th>2</th><th>Values</th><th>Default</th><th>Recommended Setting</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1µs</td><td>X</td><td></td></tr><tr><td>0</td><td>0</td><td>1</td><td>2µs</td><td></td><td>X (typical setting)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3µs</td><td></td><td></td></tr><tr><td>0</td><td>1</td><td>1</td><td>4µs</td><td></td><td></td></tr><tr><td>1</td><td>0</td><td>0</td><td>5µs</td><td></td><td></td></tr><tr><td>1</td><td>0</td><td>1</td><td>6µs</td><td></td><td></td></tr><tr><td>1</td><td>1</td><td>0</td><td>7µs</td><td></td><td></td></tr><tr><td>1</td><td>1</td><td>1</td><td>8µs</td><td></td><td></td></tr></table></td></tr>
<tr><td>n/a</td><td>2</td><td>18</td><td>11...5</td><td>no function, must be set as listed below</td></tr>
<tr><td colspan="4"><table><tr><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table></td></tr>
<tr><td>MODE</td><td>0</td><td>16</td><td>14...12</td><td>Definition of operation mode.</td></tr>
<tr><td colspan="4"><table><tr><th>14</th><th>13</th><th>12</th><th>Value</th></tr><tr><td>1</td><td>0</td><td>1</td><td>Fork light barrier, standalone mode:
LED pulse and light detection reading generated internally.</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Fork light barrier, controlled mode:
Externally stimulated LED pulse by positive edge of signal on pin EN.
Externally controlled light detection by signal on pin EN=1.</td></tr><tr><td>x</td><td>x</td><td>x</td><td>All other settings forbidden. Function of the device not defined and guaranteed.</td></tr></table></td></tr>
</table>

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VMODE	0	16	15	Disables WRITE access to volatile RAM

11	Values	Default	Recommended Setting
0	On	X	WRITE access to RAM possible. 1. Fix-parameter mode / Debug mode: This setting allows to overwrite the RAM contents, which is useful during debugging. Once the system is fully developed, this parameter should be set to "1". 2. Dynamic mode: This setting could also be useful for dynamic system application, if the system parameters should be changed "on the fly" after power-up. It is recommended to program the parameters and burn it into the ROM first. All deviating run-time parameters have then to be downloaded on the fly after power-up every time.
1	Off		WRITE access to RAM denied. Set to "1" in the final product to avoid accidentally overwriting of the contents of the RAM registers.

Parameter Name	Register No. ROM	Register No. RAM	Bit No.	Function
FUSEBIT	1	17	0	During write operation to this RAM register, put this bit = 0. This bit will be set automatically, when corresponding ROM register is programmed.

0	Values
0	The corresponding ROM register is not programmed
1	The corresponding ROM register is programmed

n/a	1	17	2...1	no function, must be set to "0"

2	1
0	0

INC	1	17	6...3	Weight of valid pulse counts. Refer to Pulse Modulated Operation (e.g. OUTNint to OUTN): Minimum number of valid (non-missing) pulses n_V of light detection for counting the response time t_R.

6	5	4	3	INC	min. n_V	Setting
0	0	0	0	0	1	X (Default setting)
0	0	0	1	1	32	
0	0	1	0	2	16	
0	0	1	1	3	11	
0	1	0	0	4	8	X (typical setting)
0	1	0	1	5	7	
0	1	1	0	6	6	
0	1	1	1	7	5	
1	0	0	0	8	4	
1	0	0	1	9	4	
1	0	1	0	10	4	
1	0	1	1	11	3	
1	1	0	0	12	3	
1	1	0	1	13	3	
1	1	1	0	14	3	
1	1	1	1	15	3	

n/a	1	17	8...7	no function, must be set to "0"

8	7
0	0

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DEC — 1 — 17 — 12...9

Weight of missing pulse counts. Refer to Pulse Modulated Operation (e.g. OUTNint to OUTN):
Minimum number of missing pulses n_M of light detection for counting the release time (fall time) t_F.

12	11	10	9	DEC	Min. n_M	Setting
0	0	0	0	0	32768	X (Default setting)
0	0	0	1	1	16384	
0	0	1	0	2	8192	
0	0	1	1	3	4096	
0	1	0	0	4	2048	
0	1	0	1	5	1024	
0	1	1	0	6	512	
0	1	1	1	7	256	
1	0	0	0	8	128	
1	0	0	1	9	64	
1	0	1	0	10	32	
1	0	1	1	11	16	
1	1	0	0	12	8	X (typical setting)
1	1	0	1	13	4	
1	1	1	0	14	2	
1	1	1	1	15	1	

TPER — 1 — 17 — 15...13

For fork light barrier, standalone mode: LED cycle time t_{Cycle}.
For fork light barrier, controlled mode: Select next lower value then external EN cycle time.

15	14	13	Values	Default	Recommended Setting
0	0	0	5µs	X	
0	0	1	10µs		
0	1	0	30µs		
0	1	1	100µs		X (typical setting)
1	0	0	300µs		
1	0	1	1ms		
1	1	0	10ms		
1	1	1	100ms		

Parameter Name	Register No. ROM	Register No. RAM	Bit No.	Function
FUSEBIT	2	18	0	During write operation to this RAM register, put this bit = 0. This bit will be set automatically, when corresponding ROM register is programmed.

0	Values
0	The corresponding ROM register is not programmed
1	The corresponding ROM register is programmed

SENSN — 2 — 18 — 3...1

Lower threshold setting of the photo current sensitivity I_{PDN} to trigger output $\overline{OUTN}$.

3	2	1	Values	Default	Recommended	Comments
0	0	0	24nA	X		A lower value increases the sensitivity. A too sensitive setting leads to false readings because of shot noise of the receiver photo diode and the internal amplifier (typ. input noise level is 7nA RMS without photo diode). Also induced EMI can lead to false readings if the sensitivity is set too low. The EMI sensitivity is heavily depending on the system architecture and the electromechanical design. The better the shielding of the chip and the photo diode and the better the PCB layout, the better the EMI immunity. The tolerance of the threshold is approx. ±25%.
0	0	1	36nA			
0	1	0	48nA			
0	1	1	60nA		X	
1	0	0	72nA			
1	0	1	84nA			
1	1	0	96nA			
1	1	1	108nA			

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<table>
<tr><td>SENSH</td><td>2</td><td>18</td><td>6...4</td><td colspan="2">Upper threshold setting of the photo current sensitivity I_{PDH}. to trigger output $\overline{OUTH}$.</td></tr>
<tr><td></td><td></td><td></td><td colspan="4">
<table>
<tr><th>6</th><th>5</th><th>4</th><th>Values</th><th>Default</th><th>Recommended</th><th>Recommended Setting</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>60nA</td><td>X</td><td></td><td rowspan="8">Common use is to set this value 50% above the value used at SENSN, i.e., if SENSN is put to 48nA, set SENSH to 72nA.

The tolerance of the threshold is approx. ±25%.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>72nA</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>84nA</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>96nA</td><td></td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>108nA</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>120nA</td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>132nA</td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>144nA</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>n/a</td><td>2</td><td>18</td><td>15...7</td><td colspan="2">no function, must be set as listed below</td></tr>
<tr><td></td><td></td><td></td><td colspan="4">
<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
</table>
</td></tr>
</table>

Sample Parameter Setting

In the section “Applications“ you will find programming examples for “Long range light barrier application (refer also to datasheet epc111)“ and for “High speed detection rate design (refer also to datasheet epc112) “.

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SPI Interface

The serial peripheral interface (SPI) allows the micro-controller to communicate with the epc110 device. It allows the access to the internal memory of the chip for parameter setting and programming for configuration or in a dynamic mode to change parameters on the fly.

Hardware interface

This functionality is given by double-used pins: LED/ $\overline{SCK}$, EN/SI, $\overline{OUTN}$/SO.

The signal $\overline{CS}$ does the selection, if the operation mode or the command/program mode is active:

1. CS = 1: operation mode → LED, EN, $\overline{OUTN}$ are active.
2. CS = 0: command/program mode → SCK, SI, $\overline{OUTN}$ are active.
   As long as CS = 0 the pin LED/SCK is set to high-ohmic and defined as input pin.

IMPORTANT NOTICE:

Due to fact of the advantage of the flexibility in use of this devic e the responsibility of any possible hardware, LED load or LED driver conflicts have to be handled by the user and are depending of the final application schematic. Main items to take care of are:

- Double-use as input as well output of LED/ $\overline{SCK}$ signals/line. For non-standalone application a well done decoupling of the signals is needed.
- Parameter setting and programming of the device in final application environment e.g. if LED and LED drivers are not designed for continuous mode application, risk of overloading.
- During SPI access of the device in final application environment e.g. if LED and LED drivers are not designed for continuous mode application, risk of overloading.

Possible solutions are discussed at the example of the principal schematic “ Figure 13: Hardware interface micro-controller – epce110“.

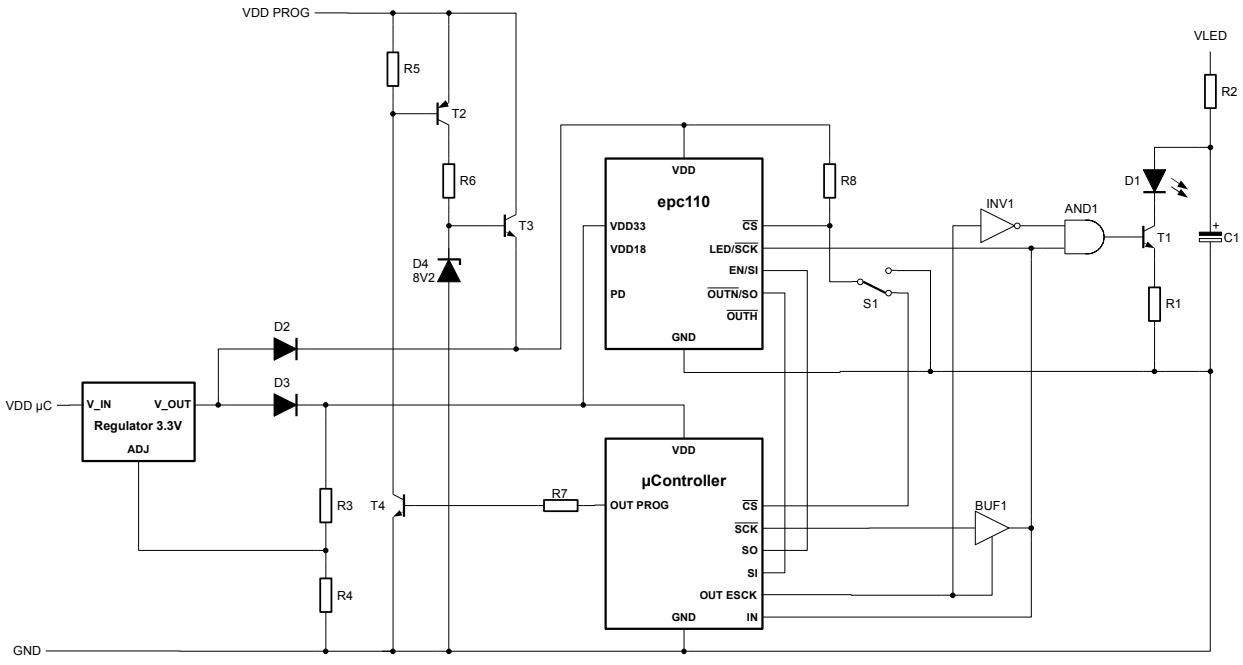

Figure 13: Hardware interface micro-controller – epce110

1. Mode selection: Operation mode - Parameter/Program mode
   As long the device is not connected to an LED driver, the access to the SPI interface is allowed while $\overline{CS}$ = 0. This can simply be done by the switch S1 before power up the circuit. In this case the output LED/ $\overline{SCK}$ will not be driven as an output.
2. Run-time access of SPI interface
   To have no conflicts together with a micro-processor on the bus line LED/$\overline{SCK}$ (Output/input) during run-time operation in this example, the decoupling and interfacing of the LED/ $\overline{SCK}$ line is done by the tristate buffer BUF1, the additional input IN and additional output enable $\overline{SCK}$ (OUT ESCK). While the LED is in operation, driven by the epc110, OUT ESCK = 0 will tristate the buffer and the $\overline{SCK}$ line from the micro-processor. With the input IN the micro-processor can read the status of the LED/ $\overline{SCK}$ line after the buffer for finding the correct transition time.

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Signal conditions and sequences:
Operation mode: CS = 1, SCK =1, BUF1 = tristate (OUT ESCK = 0), LED/SCK toggling by epc110.
Mode transition to SPI: If LED/SCK = 1: SCK =1, BUF1 = transparent (OUT ESCK = 1), CS = 0.
Parameter/program mode: CS = 0, BUF1 = transparent (OUT ESCK = 1), SCK and LED/SCK toggling by micro-processor.
Mode transition to operation: If LED/SCK =1: BUF1 = tristate (OUT ESCK = 0), CS = 1.

3. Overload-protection of LED and LED driver
Are the LED and LED driver not designed for continuous mode operation, there is a risk of overloading the LED or the LED driver in case of no decoupling of the LED driver input from the SPI interface as well from the command instructions. The signals on the line LED/SCK are depending of the status of the SCK signal itself and from the commands polarity of LED pulse POL, pulse length TPULSE, Mode selection MODE and the status of the line EN.
In the example circuitry this decoupling is done by the signal OUT ESCK, the inverter INV1 and the and-circuit AND1. In case of switching the buffer BUF1 transparent (OUT ESCK =1) the LED driver signal is set to low.

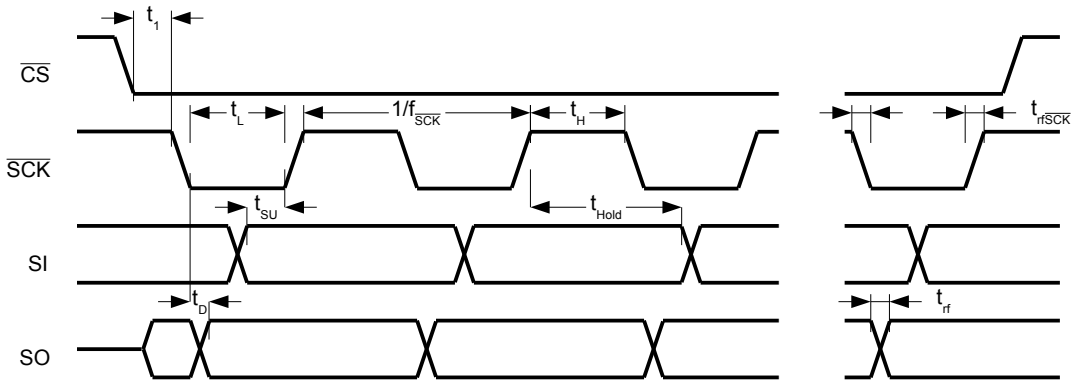
4. Supply of the programming voltage (VPROG 7.5V) at pin VDD (refer also to chapter " Programming Procedure")
To write the data from the volatile RAM section to the non-volatile ROM section a programming voltage has to be connected to the VDD pin of the epc110 following the timing diagram of Figure 17: Direct programming procedure.
This is done by an overwriting voltage source to the VDD pin in the proposed design. The main supply for he micro-processor and the epc110, pin VDD33 is done by the 3.3V voltage regulator, the diode D3 and the resistors R3 and R4. Pin VDD of the epc110 is fed by diode D2. This allows to overwrite the 3.3V operating supply by the higher 7.5V programming voltage. The programming voltage is produced by the voltage regulator T3, D4 and R6. Switch on/off of the programming voltage will be done by the R7,T4,R5 and T2 and the signal OUT PROG.

Timing Specifications of telegrams

While CS = 0 and serial clock SCK is toggling in bi-directional function data are

- on input SI read in (Command) with the positive edge and
- on output SO read out (Result) with the negative edge of the serial clock.

Means whilst data are sent to the epc110 chip by the micro-controller, in parallel the result of the last (or more generally: of a previous) command is sent back from the epc110 to the micro-controller according to the SPI protocol. The timing diagram is shown in Figure 14).



CS	Device selection
SCK	Serial input/output clock – positive edge: data read in; negative edge: data read out
SI	Serial data input
SO	Serial data output

Figure 14: SPI bus timing

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Symbol	Parameter	Comments / Conditions	Values			Units
			Min.	Typ.	Max.	
t_1	Edge time $\overline{CS}$ to $\overline{SCK}$	Falling edge $\overline{CS}$ to falling edge $\overline{SCK}$	50			ns
$f_{\overline{SCK}}$	Clock frequency of $\overline{SCK}$				10	MHz
t_H / t_L	HIGH and LOW period of $\overline{SCK}$		50			ns
t_{SU} / t_{Hold}	Set-up and hold time of SI	Data stable before and after positive edge of $\overline{SCK}$	15			ns
t_D	Output data of SO valid	Data valid after negative edge of $\overline{SCK}$			20	ns
t_{rf} / $t_{rf\,\overline{SCK}}$	Rise / fall time SO / $\overline{SCK}$				20	ns

Input Data Format and Command List

The communication is based on telegrams (Direct commands or results), which are sent and received over the SPI interface.

The input data format (telegram) is given in Figure 15. The first bit in the data stream from the microprocessor to the epc110 chip (SI pin) will be B = 0 always.

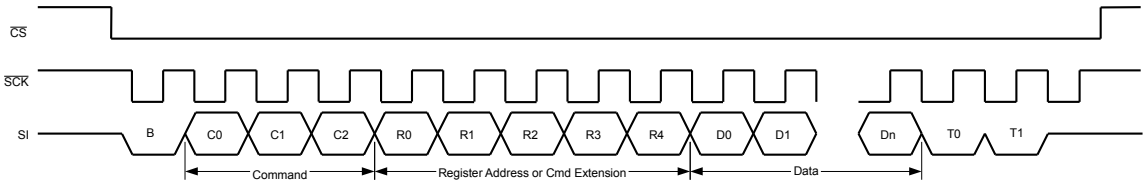

Figure 15: Communication to the epc110 device: Direct Command

Command set:

Name	Cmd Code Start B	Cmd Code Command C0...C2	Cmd Code Extension R0...R4	Cmd Code Data D0...D15	Cmd Code Termination T0, T1	Function	Result Data	No. of data bits on SPI interface Command / Result
NOP	0	000	---	---	---	No operation, or read out data	No	≧ 4
READ	0	010	Register address	---	00	Read register Rn	Yes	11 / 22
WRITE	0	011	Register address	Data	00	Write data to RAM (Register 16...18)	No	27 / --
PROG	0	110	Register address	---	---	Copy data to ROM	No	9 / --
RESET	0	111	11001	---	---	Reset the device	No	9 / --

Table 4: Command list

Remarks:

- The telegram data is transmitted with the LSB first.
- A telegram starts with the $\overline{CS}$ change from high to low (Synchronization) and ends with the change from low to high.
- Single telegrams either commands as well results have to be separated by a $\overline{CS}$ = 1 in between.
- Additional $\overline{SCK}$ clock cycles have no effect.
  This allows to extend the above given minimal telegram lengths to a standardized telegram lengths (Byte, word or double-word).
- The minimum telegram length is given in Table 3, section Number of data bits.

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Detailed Command & Result Descriptions

Command NOP: No operation

The command NOP can be used to fetch data without sending a new command – see next section Readout of Returned Results.

Readout of Returned Results

The results/data at output pin SO depend on the previous transmitted command to input pin SI.

Two ways to readout this data are possible:

1. Either it can be fetched in parallel of transmitting a next command
2. or by sending NOP commands just by toggling SCK while CS is low.

Remarks:

- The data is represented with the LSB first.
- Data is valid on positive edge of clock SCK while CS is low.
- If more clock toggles SCK are issued than data can be fetched, zeros are transmitted.

Command READ: Read register Rn

With the command READ the registers of the RAM and ROM memory can be read register by register.
The command extension “Register address” defines the requested register for reading it out.
After command transmission the expected result data can be readout on the SO pin.

Result readout frame (telegram):

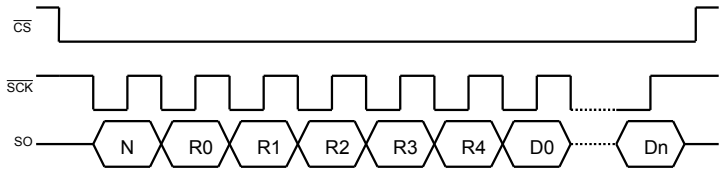

Figure 16: Timing Result Data

Result data format:

Data Bits	Function
N	Not used, have to be ignored
R0...R4	5 bit register address
D0...D15	16 bit returned data of the corresponding register (one complete register)

Table 5: Result of a READ command

Command WRITE: Write to RAM register 16 - 18

Data can be written into the volatile RAM register 16 – 18 by using the command WRITE. The command extension “Register address” selects the register. It is followed by the data to be written.

In VMODE = 1 it is possible to write to registers only, if the corresponding register in the ROM has not been written yet. It is not possible to write directly to a ROM register. If the data has to be stored into the ROM register, a subsequent command PROG has to be used.

In VMODE = 0 the RAM registers can be written at anytime.

Command PROG

The command PROG transfers the data from the RAM register to the corresponding ROM register. See chapter Parameter Programming for a detailed description.

Command RESET

The command RESET resets the device and initiates a startup.

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Parameter Programming

General Description

A description of the hardware interface for programming is given in chapter “ Hardware interface“.

The device is initially not parametrized. In order to operate the light barrier, the micro-controller (or programmer) needs to do the correct parameter settings for the selected functionality. This step is usually done in the factory of the light barrier manufacturer. After this the micro-controller can operate the light barrier or it can work in a standalone mode.

To do so, a specific parametrization of the devices must be executed first. The following procedure is an example thereof.

No.	Step	Description
1	Set parameters	Parameters like POL, TPULSE, MODE, VMODE, INC, DEC, TPER, SENSN, SENSH are stored into the RAM of the device using the command WRITE. Write them register by register.
2	Check parameters	The parameters should be checked by reading them back from each device using the READ command.
3	Program parameters	If all parameters are stored correctly, store the parameters into the non-volatile memory by using the command PROG. Please refer to chapter Programming Procedure.
4	Final test	To check the programming of the parameters, turn off the power supply and readout all parameters again.

Programming Procedure

Programming the device is a transfer of the data from the RAM to the corresponding ROM register. Each 16-bit register must be transferred individually. Thus, register 16 is transferred to register 0, register 17 to register 1, register 18 to register 2. All other registers must not be used. Figure 12 shows the timing of the programming sequence for one register:

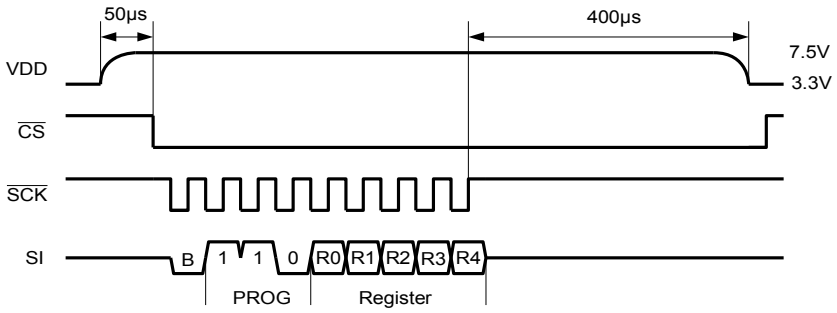

Figure 17: Direct programming procedure

“PROG” is the PROG command sequence (110). “Register” means the address of the target register (ROM), e.g. 0, 1, 2.

During programming the voltage at pin VDD has to be increased to VPROG (7.5V) and has to be kept stable buffered during the whole programming cycle. For an example of a hardware design to generate this supply refer to chapter “Hardware interface“ in the SPI interface section.

The timing parameters given in Figure 17 have to be obeyed.

Remarks:

- It is possible to program more than one register during a VDD high cycle. Between two PROG commands a delay of 400µs is needed.
- Each register can be programmed once only (ROM).
- After programming a register, bit no. 0 of this register becomes automatically a one to indicate that the register is programmed (FUSEBIT).

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Applications

Long range light barrier application (refer also to datasheet epc111)

Figure 18 shows the epc110 as an example in a long range light barrier application with minimal part count. The LED flashes according to the description of the previous chapter. Light of the LED is passing either direct, reflecting from a reflecting object or a retro reflector to the photo diode PD. If the received light fulfills the criteria according to the description in the previous chapter, the output signals $\overline{OUTN}$ and $\overline{OUTH}$ are set.

LED Driver:
The output LED of the epc110 to drive the LED driver circuit is a current source capable to drive typically 1mA. For a high performance long range light barrier (>8m), an LED peak current of up to 1.5A is needed. To generate such a high LED current, an external driver circuit is necessary. The circuitry in Figure 18 is a simple implementation of such a driver circuit. The darlington circuit with T2 and T3 and R2 and R3 does the job. In order to avoid interference on the supply voltage, the supply is isolated (filtered) with R1 and C1. The high peak LED pulse current is delivered by the capacitor C1, which itself is charged by R1. Make sure, that there is no coupling of the high LED current to the ground of the epc110 or to the cathode of the photo diode. This driver circuit operates with a VDD_{LED} in a range of 10 to 30 VDC.

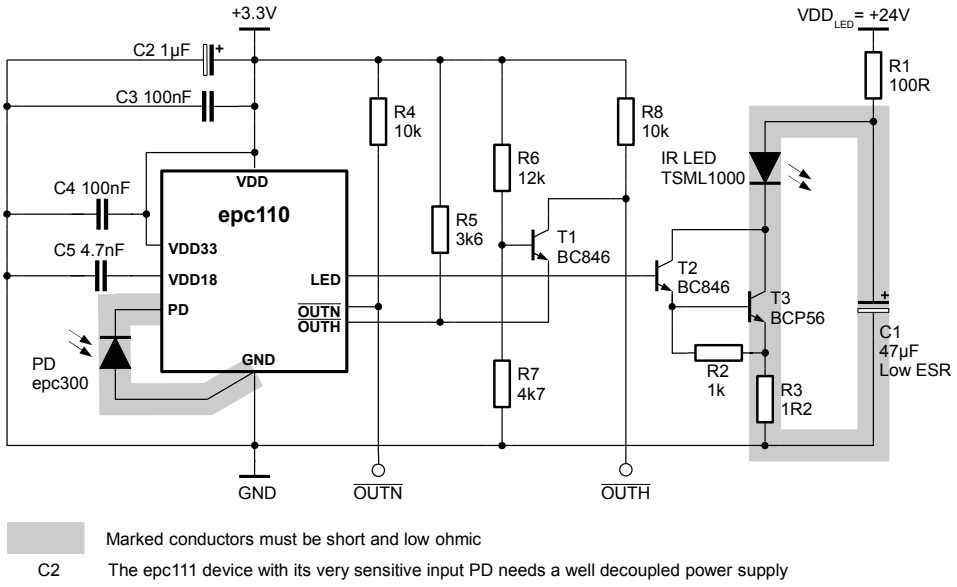

Figure 18: Long range light barrier application with minimal part count

Notice:
The schematic is for illustrating the basic circuit idea only. For the real built up the designer has to take all other additional influence factors in consideration too e.g. design rules, power rating, heat dissipation, ...

	ROM	RAM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Register #	0	16	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	FUSEBIT	Application parameters
	1	17	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	FUSEBIT	
	2	18	0	0	0	0	1	0	1	0	1	0	1	1	0	1	1	FUSEBIT	
	3	19	don't use															FUSEBIT	
	4	20	don't use															FUSEBIT	Trimming
	5	21	don't use															FUSEBIT	
	6	22	don't use															FUSEBIT	
	7	23	don't use															FUSEBIT	Device Address
	8	24	Lot no. LSB															FUSEBIT	Chip ID
	9	25	Lot no. MSB															FUSEBIT	
	10	26	Chip ID															FUSEBIT	
	11	27	Factory use only															FUSEBIT	
	12	28	Revision no.															FUSEBIT	
	13	29	no function															FUSEBIT	
	14	30	no function															FUSEBIT	
	15	31	no function															FUSEBIT	

Figure 19: Corresponding memory map epc110 "Long range"

Parameter settings can be done by writing complete 16 bit registers only.

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High speed detection rate design (refer also to datasheet epc112)

Figure 20 shows the epc 110 as an example in a high speed detection rate light barrier application with minimal part count. This design is optimized for a fast reading of light beam interruptions. Where as the working principle is similar to the above example. This driver circuit operates with a VDD_{LED} in a range of 6 to 20 VDC.

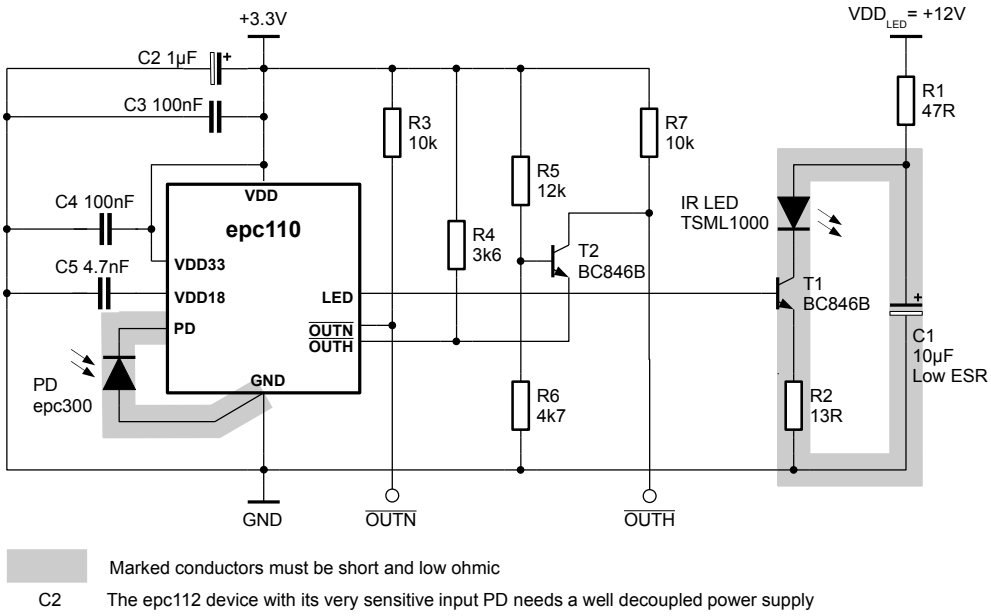

Figure 20: High speed detection rate light barrier application with minimal part count

Notice:
The schematic is for illustrating the basic circuit idea only. For the real built up the designer has to take all other additional influence factors in consideration too e.g. design rules, power rating, heat dissipation, ...

The following table shows the parameter allocation in the memory:

	ROM	RAM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Register #	0	16	1	1	0	1	1	0	0	0	0	0	0	0	0	0	1	FUSEBIT	Application parameters
	1	17	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	FUSEBIT	
	2	18	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	FUSEBIT	
	3	19	don't use															FUSEBIT	
	4	20	don't use															FUSEBIT	Trimming
	5	21	don't use															FUSEBIT	
	6	22	don't use															FUSEBIT	
	7	23	don't use															FUSEBIT	Device Address
	8	24	Lot no. LSB															FUSEBIT	Chip ID
	9	25	Lot no. MSB															FUSEBIT	
	10	26	Chip ID															FUSEBIT	
	11	27	Factory use only															FUSEBIT	
	12	28	Revision no.															FUSEBIT	
	13	29	no function															FUSEBIT	
	14	30	no function															FUSEBIT	
	15	31	no function															FUSEBIT	

Figure 21: Detailed memory map epc110 "High speed"

Parameter settings can be done by writing complete 16 bit registers only.

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Design Precautions: EMC shielding

The sensitivity at pin PD is very high in order to achieve a long operation range of light barriers even without lenses in front of the IR LED and/or the photo diode. Thus, the pin PD is very sensitive to EMI. Special care should be taken to keep the PCB track at pin PD as short as possible (a few mm only!). This track should be kept away from the IR LED signal tracks and from other sources which may induce unwanted signals. It is strongly recommended to cover the chip, the photodiode and all passive components around the chip with a metal shield. A recommended part is shown in Figure 22. The pins at the bottom are to solder the shield to the PCB with electrical connection to GND. The hole in the front is the opening window for the photo diode. The backside of the PCB below the sensitive area (PD, epc110) shall be a polygon connected to GND to shield the circuit from the backside as well.

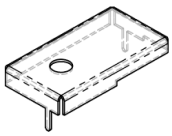

Figure 22: Recommended EMC shield

Ambient Light

Photodiode DC current can be generated by ambient light, e.g. sunlight. DC current at pin PD does not generate a DC output signal. However, if I_{PDDC} is above the stated maximal value, the input is saturated. This blocks the detection of AC current pulses.

Photodiode Capacitance

If the photo diode capacity is above the specified value, a lower detection sensitivity and a possible higher sensitivity spread results.

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Layout Information (all measures in mm,)

CSP-10 Package

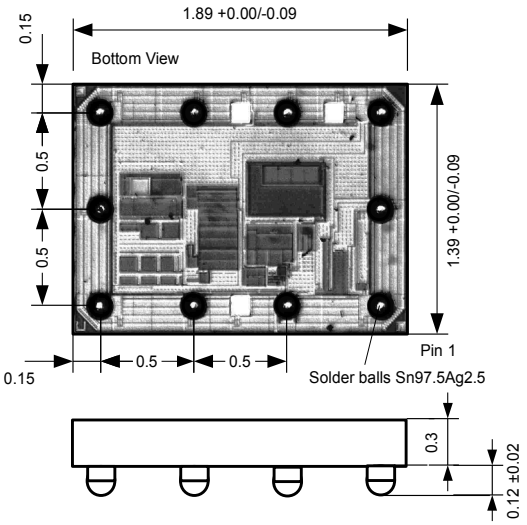

Figure 23: CSP10: Mechanical dimensions

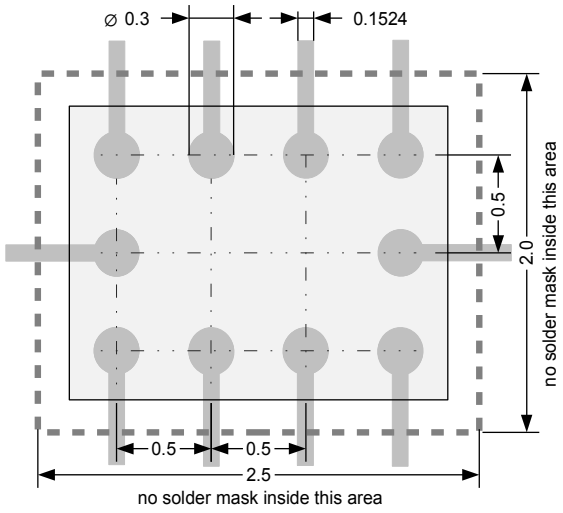

Figure 24: CSP10: Layout recommendation

Recommendations for reliable soldering of solder balls:

- Use a pad layout similar as given in Figure 24. Notice that all tracks should go underneath the solder mask area.
- Do not connect any pins direct pin to pin inside of the opening of the solder mask.
- In case of the conductors are with a Au-Ni surface finish the preferred landing pad design for the solder balls will be covering the round landing pad with a gold surface finish as a solderable area only.

QFN-16 Package

Note: For sampling only. Limited quantities. Please inquire.

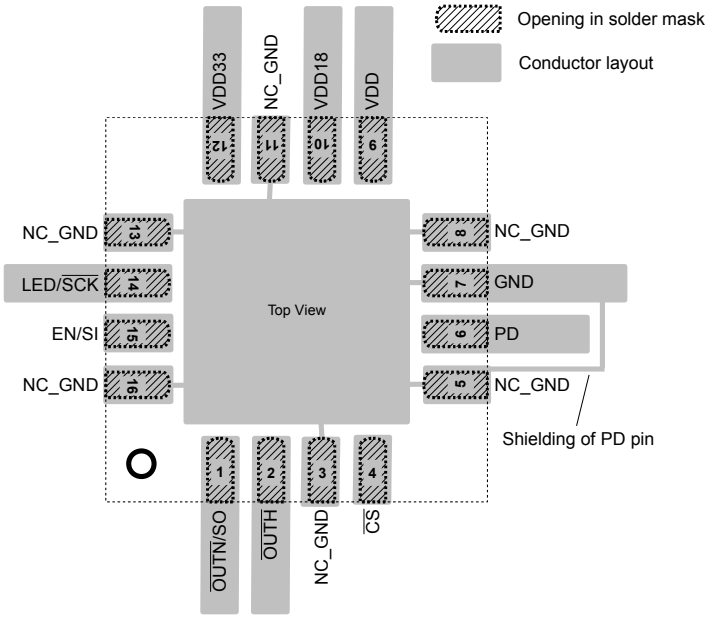

Figure 25: QFN-16: Layout recommendation

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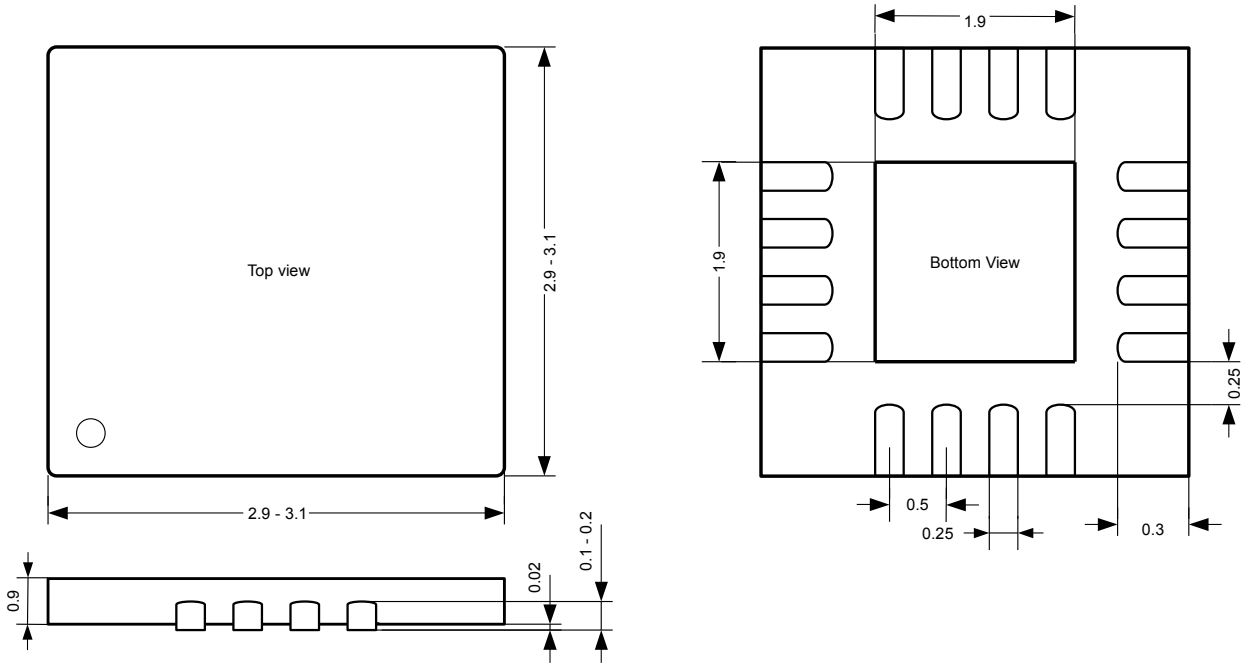

Figure 26: QFN-16: Mechanical dimensions

Reflow Solder Profile

For infrared or conventional soldering the solder profile has to follow the recommendations of IPC/JEDEC J-STD-020C (min. revision C) for Pb-free assembly for both types of packages. The peak soldering t emperature (T_L) should not exceed +260°C for a maximum of 4 sec.

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Packaging Information (all measures in mm)

Tape & Reel Information

The devices are mounted on embossed tape for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate data sheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.

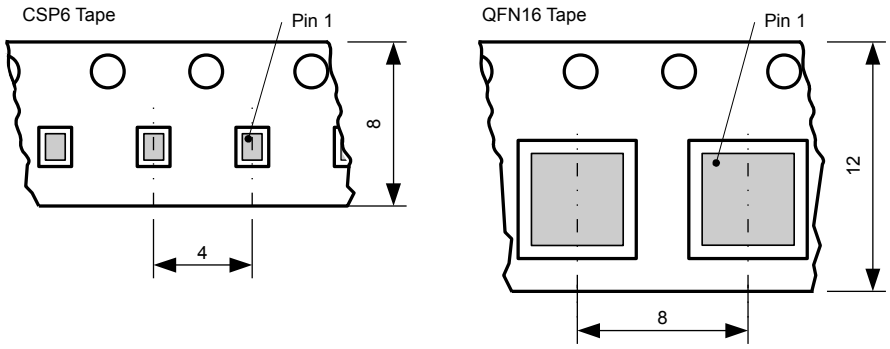

Figure 27: CSP10 and QFN16 Tape Dimension. Parts are placed with solder pads on bottom side

ESPROS Photonics AG does not guarantee that there are no empty cavities. Thus, the pick-and-place machine should check the presence of a chip during picking.

Ordering Information

Standard product:

Type	Package	RoHS compliance	Packaging Method
epc110-CSP10	CSP10	Yes	Reel

For sampling only. Limited quantities. Please inquire.

Type	Package	RoHS compliance	Packaging Method
epc110-QFN16	QFN16	Yes	Reel

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