Fully integrated Light-Barrier Chips with 2-Wire Bus Interface

General Description

The epc120 is a general purpose, fully integrated self-contained CMOS circuit to be used in light-barrier applications. The chips contain a controller which drives an LED, typically an IR-LED. The LED is used in a pulsed mode to increase the signal-to-noise ratio even when there is very strong sunlight biasing the photo diode.

It contains also a high sensitive photo diode amplifier and a signal conditioning circuitry to cancel unwanted environmental light including strong sunlight and pulsed light sources. The receiver is built around a synchronous demodulator circuitry. Two output signals with a different threshold level are implemented in order to trigger the light barriers output or to indicate light reserve.

The chips also include a power supply circuitry to establish all internally required voltages from the 2-wire bus.

They contain a 2-wire communication interface which is capable to operate as many as 1023 devices on a 2-wire bus at a speed of up to 2MBit/s over the power supply. This feature allows to design of a distributed light barrier system.

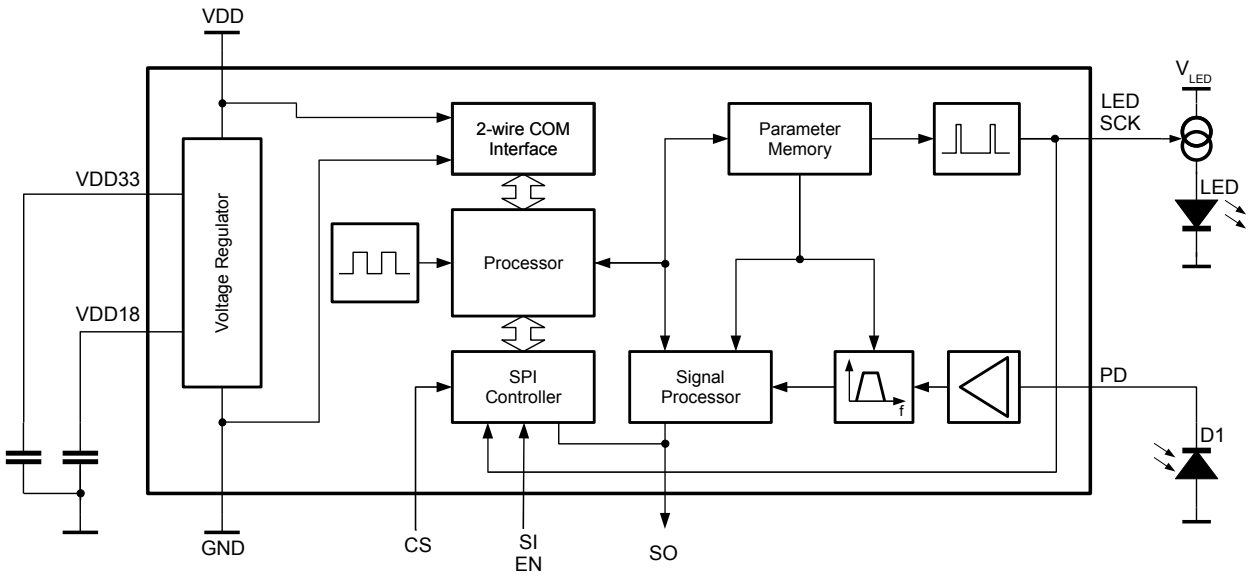
Features

- Fully integrated light barrier chip
- Needs just a photo diode and an LED with an LED driver
- Configurable
- High speed 2-wire bus
- Integrated clock generator
- CSP10 package with very small footprint
- Versions without 2-wire bus interface available (epc11x family)

Applications

- Light barriers ranging from millimeters to tens of meters
- Smoke detectors
- Liquid detectors

Functional Block Diagram



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Absolute Maximum Ratings (Notes 1, 2)

Voltage to any pin except V_{DD}	-0.3V to VDD+0.3 V
Supply Voltage on 2-wire bus V_{DD}	-0.3V to +8.0V
Programming Voltage on 2-wire bus V_{DD}	-0.3V to +8.0V
Input current at any pin except LED	-6mA to +6 mA
Power consumption with maximum load	125mW
Storage Temperature Range (T_S)	-55°C to +155°C
Lead Temperature solder, 4 sec. (T_L)	+260°C

Recommended Operating Conditions

	Min.	Max.	Units
Operating Voltage on 2-wire bus V_{DD}	4.5	5.5	V
Programming Voltage on V_{DD}	7.0	8.0	V
Operating Temperature (T_O)	-40°	+85	°C
Relative Humidity (non-condensing)	+5	+95	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics.

Note 2: This device is a highly sensitive CMOS ac current amplifier with an ESD rating of JEDEC HBM class 0 (<250V). Handling and assembly of this device should only be done at ESD protected workstations.

Electrical Characteristics

V_{DD} = 4.5V … 5.5V, -40°C < T_A < +85°C, unless otherwise specified

General Data

Symbol	Parameter	Conditions/Comments		Values			Units
				Min.	Typ.	Max.	
V_{PP}	Ripple on supply voltage, peak to peak	2-wire interface V_{det}	Input pulse $I_{PD\ NST}$				
		50mV	48nA			150	mV
		100mV	72nA			350	mV
		200mV	108nA			600	mV
I_{DD_OP}	Current consumption	in operation mode I_{PD} = 0 mA				2	mA
V_{det}	Detection level for 2-wire interface	configurable		50		200	mV
I_{MOD}	Modulation current for 2-wire interface			6.4		9.8	mA
f_{clk}	Reference clock	Internal oscillator			1		MHz
df_{clk}	Temperature drift of the oscillator				640		ppm/K
V_{PUP}	Power-up Threshold Voltage	The voltage at VDD33 when the device starts up		2.4		3	V
V_{IH}	INPUT	Logical high (V_N can be either VDD or VDD33)		0.7 *V_N		V_N	V
V_{IL}	INPUT	Logical low (V_N can be either VDD or VDD33)		GND		0.3 *V_N	V
I_{LEAKD}	Input leakage current					10	µA
V_{OH}	Output high voltage	@ 4mA sink except pin SCK/LED		V_{DD}- 0.5			V
V_{OL}	Output low voltage	@ 4mA source				0.5	V
$I_{SCK/LED}$	Source current	@ PIN SCK / LED		0.7		1.3	mA
V_{Hist}	Schmitt Trigger Hysteresis			0.1			V
R_{PU}	Pull-Up Resistor			30		200	kΩ
I_{PDDC}	DC Photo Diode Current	generated by ambient light with no effect to the sensitivity		0.0		2	mA
C_{PD}	Photodiode Capacitance	Photodiode Capacitance				40	pF
I_{N_Imin}	Input related noise	@ I_{PDDC} =0				15	nA $_{RMS}$
I_{N_Imax}	Input related noise	@ I_{PDDC} =$I_{PDDCMax}$				20	nA $_{RMS}$
I_{PDN}	Photo Current Sensitivity, normal threshold	Parameter SENSN = 011 (60nA). T_{Pulse} = 6µs Photodiode pulse to generate a status “pulse detected”		45	60	75	nA
I_{PDH}	Photo Current Sensitivity, upper threshold	Parameter SENSH = 011 (96nA). T_{Pulse} = 6µs Photodiode pulse to generate a status “pulse detected”		1.4	1.6	1.8	I_{PDN}

Symbol	Parameter	Conditions/Comments	Values	Units
I_{pulse}	Maximum Input Pulse Current	If the input current pulse is above this level, the recovery time t_{REC} is undefined (refer to section 'Other Parameters')	dependent on settings	µA
t_{Pulse}	LED Pulse Length		Programmable between 1 and 8	µs
t_{relax}	Relaxation time	After a strong current pulse (I_{pulse} = 100µA)	dependent on settings	µs

Other Parameters

(typical values, T_{amb} = 25°C, V_{DD} = 5.0V)

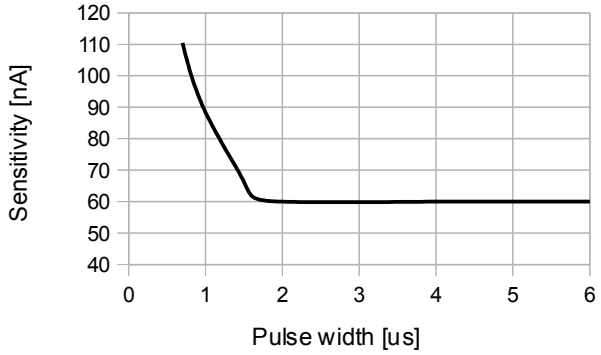
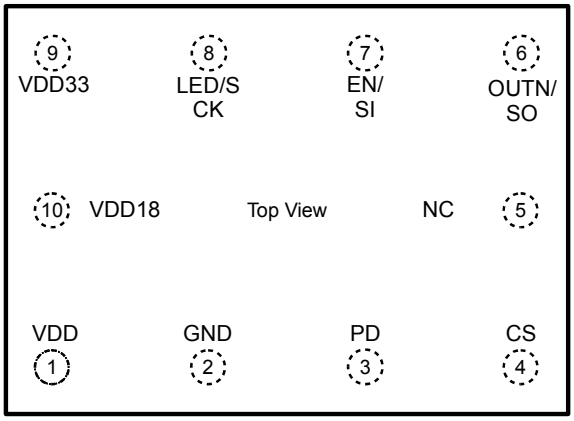
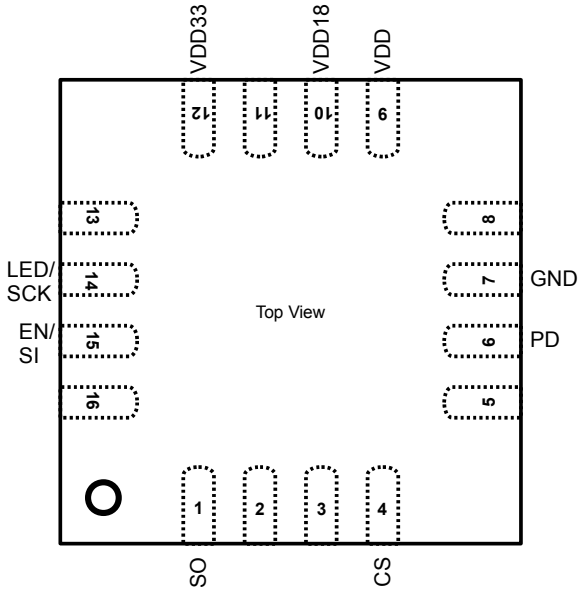


Figure 1: Input Sensitivity vs. LED pulse width

Connection Diagrams



10-Pin Chip Scale Package (CSP)



16-Pin QFN Package
Note: For sampling only. Limited quantities. Please inquire

10-Pin CSP	16-Pin QFN	Pin Name	Type	Description
1	9	VDD	Power supply	Positive power supply
2	7	GND	Power supply	Negative power supply pin.
3	6	PD	Analog Input	Photo diode input.
4	4	CS	Digital Input	SPI Interface: Chip Select. Active low, with pull up
6	1	SO	Digital Output	SPI interface serial out
7	15	SI	Digital Output	SPI interface serial input
8	14	LED SCK	Digital In / Out	Light barrier: LED control SPI Interface: Shift Clock
9	12	VDD33	Power Supply Decoupling	A power supply filter capacitor is connected to this pin.
10	10	VDD18	Analog Out	1.8V regulator output, used to connect a filter capacitor. Must not be used to supply any other circuits.
5	2	NC		Not connected. Leave that pin floating.
n/a	3, 5, 8, 11, 13, 16	NC		Not connected. Connect this pin with VSS.

1. Application Information

The epc120 chip set is a general purpose CMOS integrated circuit for light barrier applications. Up to 1023 devices may be connected to two respectively four wires in parallel. Each device can be individually addressed by an epc100 chip which acts as the interface between a microcontroller and the 2-wire bus. It manages the bus traffic between the microcontroller and the individual epc120 elements. Programmable fuses i.e. for the address, sensitivity, LED light pulse width, etc. allow the device to be parametrized in the final system (OTP memory).

The bus controller activates the emitting side of the epc120 and reads the status of the levels at the photodiode input. The status of the answers to the interface chip can be 'no light pulse received', 'low level light pulse received' and 'high level light pulse received'.

Each chip can be put into 'standby mode' or 'operating mode' to reduce power consumption. During 'standby mode', power consumption is reduced and the photo diode is shorted. In the 'operation mode', the device is active and ready to receive a light pulse generated by an LED activated by the LED pin. During a scan, the bus controller addresse s one device after the other and fetches the light barrier status.

This manual describes the various operation and programming modes in order to use epc120. For the interface chip epc100 please refer to the epc10x “Reference Manual”.

2. Hardware Design Information

Figure 2 shows the epc120 as an example in a long range light barrier application as a single bus module in a bus-chain configuration with minimal part count. The LED emits a light pulse when the chip is addressed by the bus controller. Light of the LED is reflected from a reflecting object or a retro reflector back to the photo diode PD. If the received light is strong enough it triggers the internal thresholds OUTN/H. The status of the receiver result can be read by the bus controller.

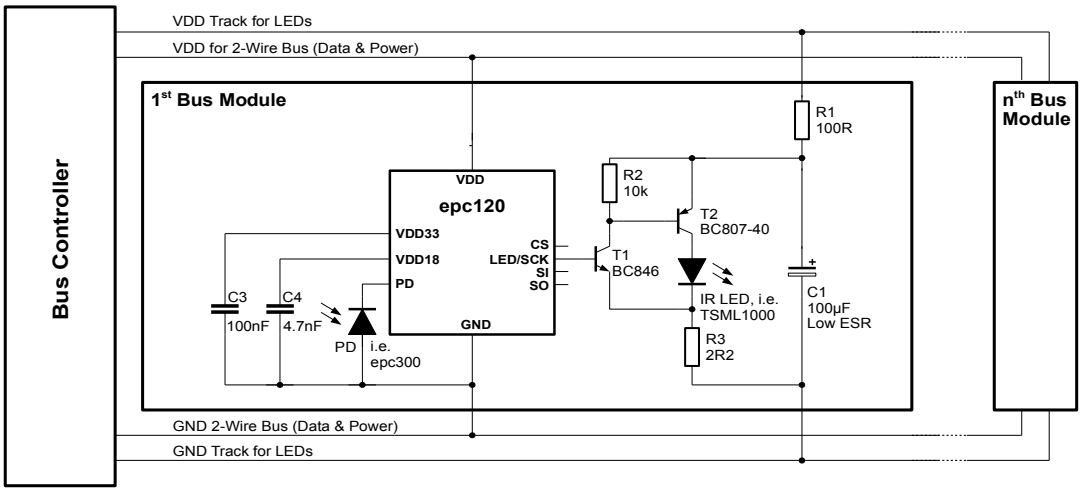


Figure 2: Long range light barrier chain application with minimal part count

The output to drive the LED is a current source capable to drive typically 1mA. For a high performance light barrier, an LED peak current of up to 2A is needed. To generate such a high LED current, an external amplifier is necessary. The circuitry in Figure 2 is a simple implementation of such an amplifier. The complementary Darlington circuit with T1 and T2 and R2 and R3 does the job. In order to avoid interference on the supply voltage, the supply is isolated (filtered) with R1 and C1. The high peak LED pulse current is delivered by the capacitor C1, which itself is charged more or less constantly by R1. Make sure, that there is no coupling of the high LED current to the ground and the supplies of the epc120 or to the cathode of the photo diode. This driver amplifier operates with a VDD_{LED} in a range of 5 to 30 VDC.

Design Precautions

The sensitivity at pin PD is very high in order to achieve a long operation range of light barriers even without lenses in front of the IR LED and/or the photo diode. Thus, the pin PD is very sensitive to EMI. Special care should be taken to keep the PCB track at pin PD as short as possible (a few mm only!). This track should be kept away from the IR LED signal tracks and from other sources which may induce unwanted signals. It is strongly recommended to cover the chip, the photodiode and all passive components around the chip with a metal shield. A recommended part is shown in Figure 3. The pins at the bottom are to solder the shield to the PCB with electrical connection to GND. The hole in the front is the opening window for the photo diode. The back side of the PCB below the sensitive area (PD, epc120) shall be a polygon connected to GND to shield the circuit from the back side as well.

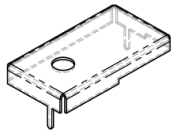


Figure 3: Recommended EMC shield

Ambient Light

Photodiode DC current can be generated by ambient light, e.g. sun light. DC currents at pin PD do not generate a DC output signal. However, if I_{PDDC} is above the stated maximal value, the input is saturated which blocks the detection of AC current pulses.

3. System Concept

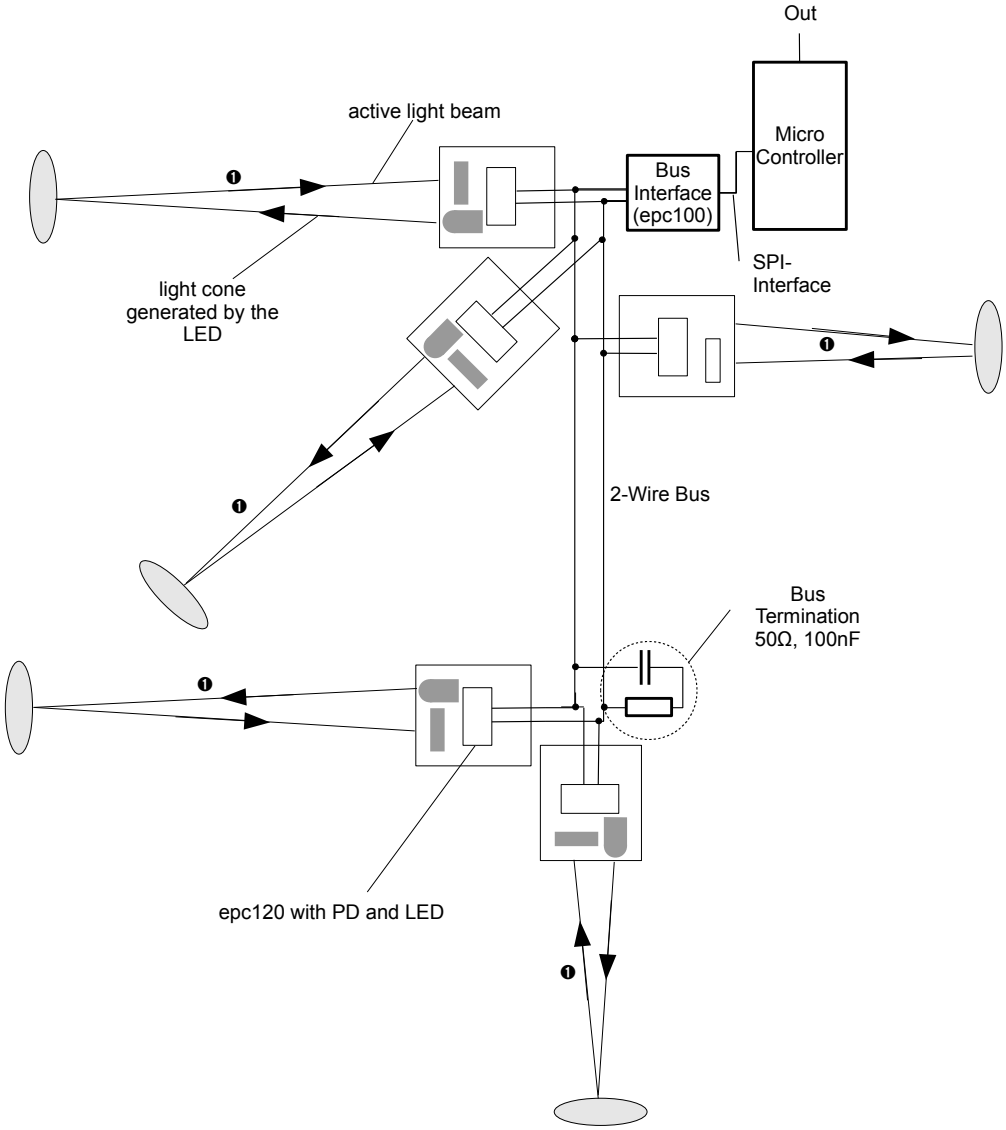


Figure 4: System overview

In a system with several reflective light barrier beams, each individual light barrier contains an emitter and a receiver. They are located at the same place. As a receiver acts a photodiode and as an emitter a LED. Both can be controlled by only one single epc120. In contrast to the epc11x-family, which are also light barrier chips, the epc120 can be used in a large distributed system. The devices are synchronized over the 2-wire bus line, organized by one epc100 and a microcontroller.

Figure 4 shows a typical distributed light barrier setup with five elements. Each element consist of an epc120, an emitter (LED), a receiver (photodiode) and a few other components. Every element is connected to the 2-wire bus[1], which is controlled by a microcontroller through an epc100. Because every epc120 element has a unique address, the microcontroller has individual access to all bus components.

Each of the epc120 elements sends light, typically infrared light, focused towards a reflector or an object. It reflects the light back to the photodiode. If multiple sensors like this would be operated in close proximity, scattered light from all sensors are probably reflected to the receivers. This would lead to false triggering. Thus, a sequential operation mode has to be implemented. Basically, a master controller activates one sensor after the other and reads back the status of each individual light beam.

1 If the LED pulse current is rather high, i.e. 1 A, two separate bus wires for the LED supply current are needed. Please refer to Figure 2 for detailed information.

In more detail, such a sequential operation is typically like as follows:

1. The first epc120 element is turned on (active mode).
2. On a second command this element sends a short light pulse towards his reflector or object, forming the active light beam ❶.
3. If there is no obstacle between epc120 and his reflector, the element receives this light pulse and stores it into a local memory.
4. The bus controller reads out the content of the memory in the epc120 chip and stores the status (light beam interrupted or not interrupted) into its data memory.
5. Finally, epc120 is turned off (standby mode).

This sequence, which is also called 'scan', is repeated until all beams are checked and their status is stored in the beam status memory of the bus controller.

The above mentioned sequence is repeated until power is switched off. Because of the fact, that an object can enter into a light beam right after a beam has been checked with the above mentioned procedure, up to two full scan sequences are necessary to reliably detect an object. Thus, the overall maximum response time of the system will be

$$t_R = 2 \cdot (n \cdot t_{beam} + t_{eval}) \qquad (1)$$

where

t_R = response time of the system
n = number of elements or light beams
t_{beam} = time to evaluate one beam
t_{eval} = time to evaluate the beam status memory and generate the output signal

For further reference in optical design considerations please refer to the respective application notes available from epc.

Figure 5 shows the epc120 in a distributed light barrier system application. The epc100 acts as a bus controller.

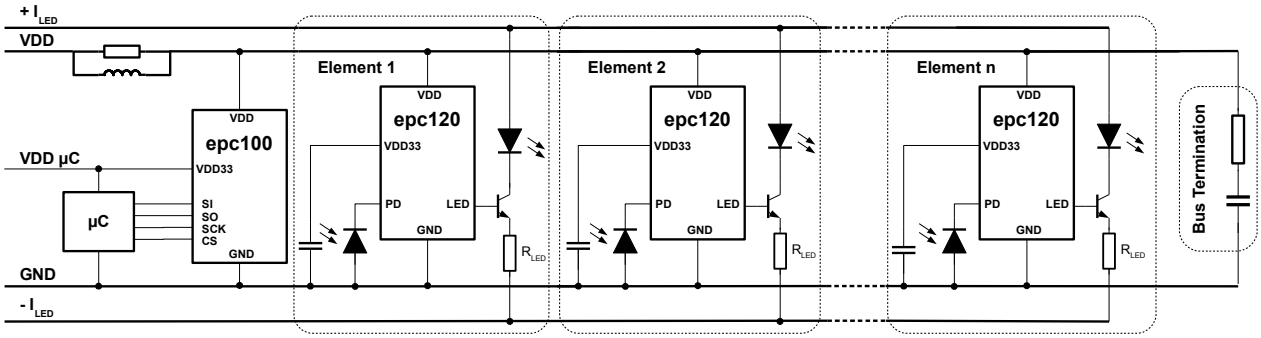


Figure 5: epc120 in the light barrier application as receivers and the interface chip to the microcontroller

From the point of view of the microcontroller, the whole system looks like a single device with several addressable sensors: the microcontroller activates one epc120 element and fetches the results after a predefined time.

In the circuit in Figure 5, the LED current is defined by a common current source in the I_{LED} line. The resistor R_{LED} limits the current through the LED and is not needed in non-safety applications. If such a resistor is inserted, a failure mode can be detected, if more than one LED is active due to a short circuit or a failure in the epc100. It is also possible to have a common voltage supply and to generate the LED current by a resistor.

4. 2-Wire Bus

The 2-wire bus and the power supply utilize the same two wires. The data is transmitted by modulating the current on the power-line. The modulated current, together with the resistor in the power supply, produce a voltage signal on the line. All devices receive this signal. The system is designed to operate with a line impedance of around 100Ω. The line impedance is for a flat band cable typ. 100Ω and for a 2-wire line typ. 120Ω. An inductor in parallel of the resistor (or a DC regulator with a lowpass feedback) shapes the pulses and keep the the DC voltage drop over the resistor low. The required corner frequency of this L/R-filter is listed in the table below.

The communication interface has been designed to be used for line lengths of up to 100m and with up to 1023 sensor devices. Independent of the line length, the 2-wire bus has to be terminated[2] by a network with a resistor R_{TE} in series to a capacitor C_{TE}, to achieve the correct voltage levels on the bus for the transmitted signals. The resistor R_{TE} is equal to the line impedance e.g. 100Ω. The corner frequency f_{TEC} of this RC-filter must be in minimum 10 times less the lowest data rate used on the 2-wire bus, e.g. < 25kHz. The lower the better. The capacitor C_{TE} should be a ceramic type with a value of 100nF or higher for a good termination. The equal capacitor value is close to the L/R-filter at the supply point VDD (beginning of the 2-wire bus) to keep the voltage on the bus stable. For detailed description refer to the Manual epc100/epc101.

The data rate on the 2-wire bus is set by the parameter DRATE. It also defines $T_{SCANmin}$ (refer to Chapter 9. Timing) and the required inductor according to Table 1. The maximum data rate allowed on the 2-wire bis is depending on the bus length. The longer the bus wire, the lower the data rate. Table 1 shows the possible bus wire length according to the data rate.

DRATE	k	Data Rate on the 2-Wire Bus	Minimal Data Rate Required on SPI Interface	Corner Frequency L/R	Inductor	Bus Wire Length[3]
00	8	250 kbit/s	300 kbit/s	0.5 MHz	16µH	12 … 100m
01	4	500 kbit/s	600 kbit/s	1 MHz	8µH	6 … 12m
10	2	1 Mbit/s	1.2 Mbit/s	2 MHz	4µH	3 … 6m
11	1	2 Mbit/s	2.4 Mbit/s	4 MHz	2µH	≤ 3m

Table 1: Data rate of the 2-wire communication

The default value of DRATE is 00. The parameter DRATE has to be identical for all devices on one physical 2-wire bus.

The SPI bus should be faster than the 2-wire bus, otherwise the communication does not work. Since the command length dependent on the command type, the delay time to the next command has to be adjusted to the previous command. The time delay can be calculated with the given data length in Table 7 on page 20.

The parameter CDET defines the optimal signal amplitude for the receiver. The maximum rate at pin VDDR (5.5V) should not be exceeded and signals which are smaller than 70% of the recommended values are not detected.

Since the command length is dependent on the command type, the delay time to the next command has to be adjusted to the previous command. The time delay can be calculated with the given data length in Table 7 on page 20. The data handling chain of the 2-wire communication channel is shown in Figure 6.

2 Independent of the electro-mechanical design and the bus location of the edge, the termination network is necessary. It is in the responsibility of the system designer that the data integrity on the bus is guaranteed. Data integrity can be tested by readout bus transmission errors. It is strongly recommended to do that during type qualification during EMI qualification tests .

3 The effective length is dependent on the electro-mechanical design of the edge. The values in the table are indicative only.

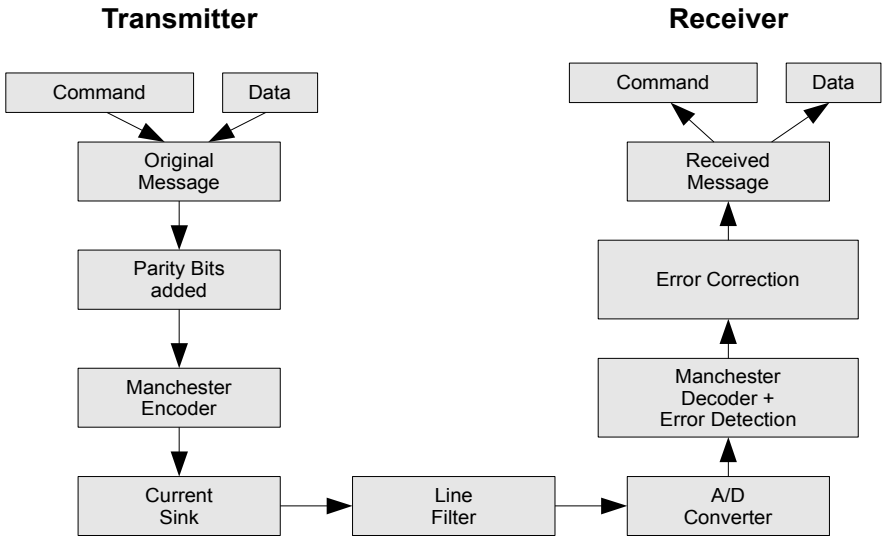


Figure 6: Data handling

Figure 7 shows the different messages with the parity bits. From the interface to the sensor/transmitter device the “normal command” is used except for the register write command. In the other direction only the register readout has a different format. Notice the different start bits which identify the direction of the transmission: 00 for the direction interface to sensor devices and 01 in the other direction. Between the telegrams, an idle time of 2 clock periods are need to detect the start of the transmission.

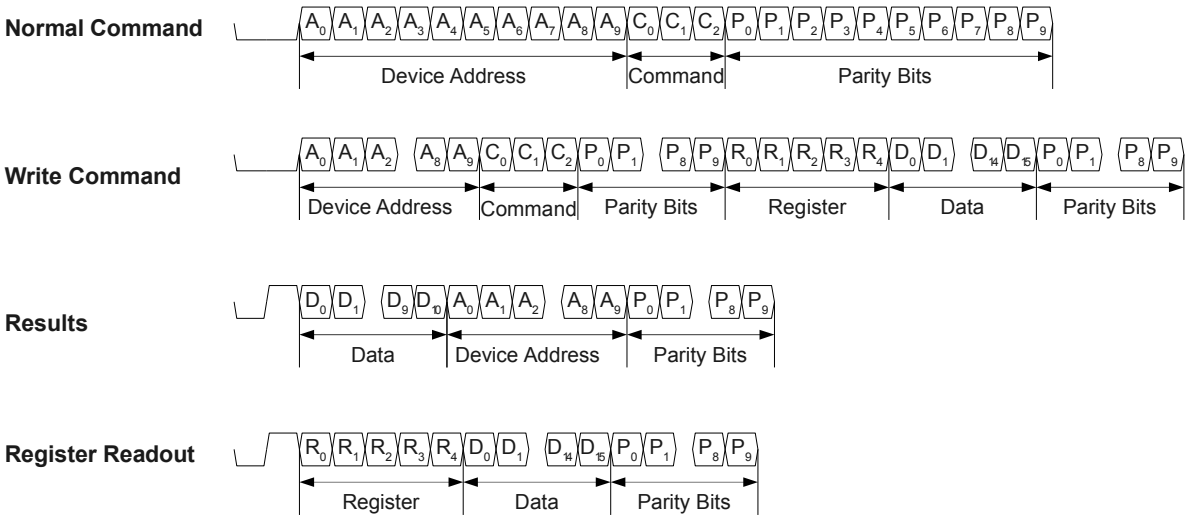


Figure 7: Message Structure

Bus Wire Considerations

The electromechanical design of a system using multiple epc10x devices on a twisted pair cable with an impedance of typically 100 Ohms has an impact on the overall impedance of the system. Figure 8 shows the change of the cable impedance with smaller element pitch.

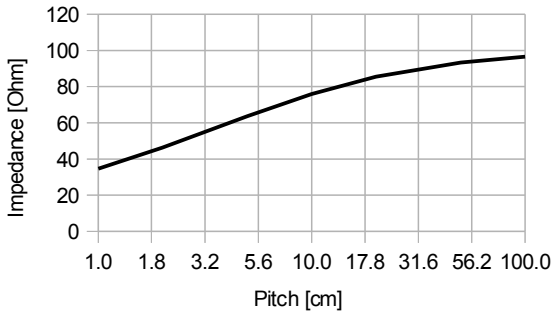


Figure 8: Line impedance as a function of the element pitch on a 100 Ohm twisted pair cable

It is highly recommended to terminate the bus line on both sides with an AC terminator network (shown in Figure 9) which matches the overall impedance of the system according to Figure 8. In order to avoid high DC currents in the termination resistor, a capacitor of C_T should be connected in series to the termination resistor. For detailed description refer to the Manual epc100/epc101.

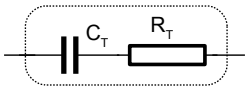


Figure 9: Bus termination network

Another aspect is the distribution velocity of the electrical signals on the 2-wire bus. Since the bus wire itself as well as the individual elements on the bus present a significant capacitance, the distribution velocity decreases with the number of elements and the pitch between the elements.

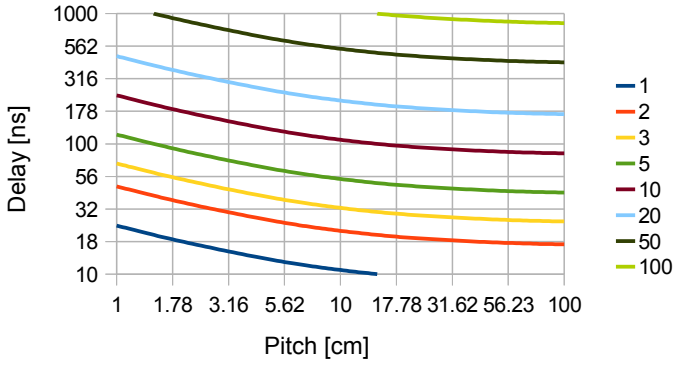


Figure 10: Delay vs Pitch. Parameter: Line length [m]

It is important that the overall delay is less than 50% of the clock period of the transmission. E.g. if the system is operated with 2 MBit/s data rate, the max. accepted delay must not be more than 125ns. Figure 10 shows, that a system operated at the full speed of 2 Mbit/s, a cable length of up to 5m are possible with an element pitch down to 1cm.

Example:

If we have a system that contains 100 elements in a pitch of 10cm, the total bus length is 10m. According to Figure 10, the delay time of a proper terminated bus is a little bit more than 100ns. Thus, such a system can be operated with the full speed of 2MBit/s.

Bus Signal Waveform

Figure 11 pictures the Manchester encoding and the signal on the bus. The signal on the bus can be monitored with an oscilloscope and should look like in the drawing.

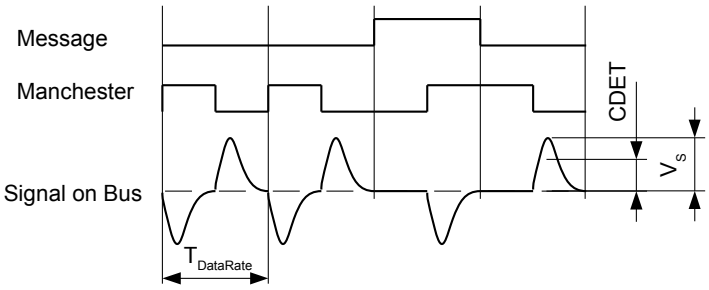


Figure 11: Manchester encoded signal on the bus

CDET is the threshold set in the 2-wire communication receiver of the chip to detect the communication signal on the bus. This parameter, described in Table 6 and Table 10, can be adjusted to mach the specific system requirements. Thus, the voltage swing V_S of the communication signal on the bus shall match this setting. A good principle is that the voltage swing V_S measured on the bus should be min. 25% and max. 150% above the CDET value.

Example:

If CDET is set to 200mV, the voltage swing V_S should be in a range of 250 to 500 mV. Ideal for this setting is a swing voltage V_S of 400mV.

The peak voltage of V_{Smax} is a function of the current amplitude CX2 on the 2-wire bus and the termination resistor R_{TE}.

$$V_{Smax} = C2X \cdot \frac{R_{TE}}{2} \qquad \text{e.g.} \qquad V_{Smax} = 8mA \cdot \frac{100ohm}{2} = 400mV$$

Notes:

Make sure that the voltage swing V_S is in the given tolerance range at every physical location of the bus. Due to reflections in the cable, losses of the wires (capacitive, inductive, and resistive), and the high bandwidth of the communication signals, significant differences can occur.

Be carful to have a low inductance wiring for the 2-wire bus including all connector transitions (except L_{TE} as given). Any series inductances on the bus reduce the slew rate of the signals and so far the maximum achievable signal amplitude on the 2-wire bus.

Parameter Memory

The epc120 device contains a memory to store the application parameters. The following classes of data are stored on each device:

- Unique chip ID and chip adjustments (factory set)
- Physical device address in the application, representing the beam number
- Application parameters

This data can be permanently stored in a read-only memory[4] and is mirrored in a volatile memory[5]. At power up, the data (except the chip ID) is copied from the ROM to the RAM. During operation, the data from the RAM is used. Both memories are organized in 16 registers at 16 bits each. The data can be accessed on a 16-bit register base. The following table shows the memory organization:

Non-Volatile Memory Address Range (Register no.)	Volatile Memory Address Range (Register no.)	Description
0 - 3	16 – 19	Application parameters
4 - 6	20 – 22	Trim values, factory set
7	23	Device Address
8 – 15	-	Chip ID, factory set
-	24 – 31	For factory test purpose. Read only.

Table 2: Memory map overview

As shown in the table above, registers 0 – 3 and 7 are used for configuring the chip in the application. Before the devices can be used in a given light curtain system, the required application parameters and the physical address of the chip in the system have to be stored into the devices memories. The following table shows a parameter memory overview:

ROM	RAM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	16	VMODE	MODE			SOFF	DRATE		TSTMP				TPULSE			POL	FUSEBIT	Application parameters
1	17	TPER															FUSEBIT	
2	18	TSET						SENS	IVCOFF	SLOW	SENSH			SENSN / VTHRLED			FUSEBIT	
3	19					CDET		C2X									FUSEBIT	
4	20																FUSEBIT	Trimming
5	21																FUSEBIT	
6	22																FUSEBIT	
7	23	Address															FUSEBIT	Device Address
8	24	Chip ID															FUSEBIT	Chip ID
9	25																	
10	26																	
11	27																	
12	28																	
13	29																	
14	30																	
15	31																	

Figure 12: Detailed memory map

Parameters in white fields only shall be programmed. Never change the memory content of gray marked cells. Because only complete registers can be programmed, the bits which are gray marked must be set to zero.

The RAM can only be written, if the corresponding ROM memory hasn't been written before or if the volatile mode is active (VMODE, refer to Table 3 on page 12). The last bit of each 16-bit ROM register serves as write inhibit bit. To write to the ROM, the microcontroller has to write to the RAM first. From there, the microcontroller can first double check the data integrity. When a memory section is verified, the content can be transferred from the RAM memory using the command PROG to the ROM (refer to chapter Command PROG).

The device is fully operational as well without programming the ROM but data will be lost at power down. Operating the chips in this mode is helpful during the development of the product. However, in the final application, the parameters must be stored into the ROM memory.

4 The non-volatile memory is a one-time-programmable memory (OTP). Once the memory is programmed, the programmed values cannot be overwritten anymore! This memory type is hereinafter called ROM.
5 Hereinafter called RAM.

5. Parameter Setting Registers 0/16

Parameter Name	Register No. RAM	Register No. ROM	Bit No.	Function
FUSEBIT	0	16	0	This bit will automatically be set when register 16 is programmed.

0	Values
0	Register 16 is not programmed
1	Register 16 is programmed

POL	0	16	1	Polarity of the LED pulse. Setting is depending on the LED driver circuitry.

1	Values	Default Setting	Recommended Setting
0	active high 	X	X
1	active low 		

TPULSE	0	16	4..2	Pulse length of the light pulse. Setting is dependent on the LED type, the LED current, the required response time of the system, the scan rate, the operating range, the lens, etc.

4	3	2	Values	Default Setting	Recommended Setting
0	0	0	1µs	X	
0	0	1	2µs		
0	1	0	3µs		
0	1	1	4µs		
1	0	0	5µs		X (typical setting)
1	0	1	6µs		
1	1	0	7µs		
1	1	1	8µs		

n/a	0	16	5	no function, must be set to “0”
TSTMP	0	16	8..6	Time stamp. The LED pulse is generates in the middle of the time stamp range.

8	7	6	Values	Default Setting	Recommended Setting
0	0	0	30µs	X	This parameter should be set to the same length as the receive window length, given by the scanning time by the microcontroller. I.e., if the time between the SCAN commands issued by the micro processor is 60µs, this parameter should be set to 60µs.
0	0	1	60µs		
0	1	0	90µs		
0	1	1	120µs		
1	0	0	150µs		
1	0	1	180µs		
1	1	0	210µs		
1	1	1	240µs		

DRATE	0	16	10..9	Data rate on the 2-wire bus

10	9	Values	Default Setting	Recommended Setting
0	0	250 kbit/s	X	if the physical 2-wire bus length is up to 100 meters
0	1	500 kbit/s		
1	0	1 Mbit/s		
1	1	2 Mbit/s		if the physical 2-wire bus length is less than 3 meters

...continued on next page...

<table>
<tr><th>Parameter Name</th><th>Register No.
RAM</th><th>Register No.
ROM</th><th>Bit No.</th><th>Function</th></tr>
<tr><td>SOFF</td><td>0</td><td>16</td><td>11</td><td>Status of voltage regulator for internal VDD
<table>
<tr><th>11</th><th>Values</th><th>Default Setting</th><th>Recommended Setting</th></tr>
<tr><td>0</td><td>On</td><td>X</td><td>when used a receiver</td></tr>
<tr><td>1</td><td>Off</td><td></td><td>when used as interface chip with 3.3V micro controller</td></tr>
</table></td></tr>
<tr><td>MODE</td><td>0</td><td>16</td><td>14..12</td><td>Mode for epc120 usage
<table>
<tr><th>14</th><th>13</th><th>12</th><th>Value</th></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
</table></td></tr>
<tr><td>VMODE</td><td>0</td><td>16</td><td>15</td><td>Volatile mode
<table>
<tr><th>15</th><th>Values</th><th>Default Setting</th><th>Recommended Setting</th></tr>
<tr><td>0</td><td>On</td><td>X</td><td>This setting allows to overwrite the RAM contents, which is useful during debugging. Once the system is fully developed, this parameter should be set to “1”. This setting could also be useful, if the system parameters should be changed “on the fly” in dynamic systems. it is recommended to program the address and burn it into the ROM first. All other parameters can then be downloaded upon power-up.</td></tr>
<tr><td>1</td><td>Off</td><td></td><td>Set to “1” in the final product to avoid accidentally overwriting of the contents of the RAM registers</td></tr>
</table></td></tr>
</table>

Table 3: epc120 Registers 0 and 16

6. Parameter Setting Registers 1/17

<table>
<tr><th>Parameter Name</th><th>Register No.
ROM</th><th>Register No.
RAM</th><th>Bit No.</th><th>Function</th></tr>
<tr><td>FUSEBIT</td><td>1</td><td>17</td><td>0</td><td>This bit will automatically be set when register 17 is programmed.
<table>
<tr><th>0</th><th>Values</th></tr>
<tr><td>0</td><td>Register 17 is not programmed</td></tr>
<tr><td>1</td><td>Register 17 is programmed</td></tr>
</table></td></tr>
<tr><td>n/a</td><td>1</td><td>17</td><td>12..1</td><td>no function, must be set to “0”</td></tr>
<tr><td>TPER</td><td>1</td><td>17</td><td>15..13</td><td>must be set to “010”
<table>
<tr><th>15</th><th>14</th><th>13</th></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
</table></td></tr>
</table>

Table 4: epc120 Registers 1 and 17

7. Parameter Setting Registers 2/18

Parameter Name	Register No. ROM	Register No. RAM	Bit No.	Function
FUSEBIT	2	18	0	This bit will automatically be set when register 18 is programmed.

0	Values
0	Register 18 is not programmed
1	Register 18 is programmed

SENSN	2	18	3..1	Lower threshold setting of the receiver input (sensitivity). A lower value increases the sensitivity. A too sensitive setting leads to false readings because of shot noise of the receiver photo diode and the internal amplifier (typ. input noise level is 7nA RMS without photo diode). Also induced EMI can lead to false readings if the sensitivity is set too low. The EMI sensitivity is heavily depending on the system architecture and the electromechanical design. The better the shielding of the chip and the photo diode and the better the PCB layout, the better the EMI immunity. The tolerance of the threshold is approx. ±25%.

3	2	1	Values	Default Setting	Recommended Setting
0	0	0	24nA	X	
0	0	1	36nA		
0	1	0	48nA		
0	1	1	60nA		X
1	0	0	72nA		
1	0	1	84nA		
1	1	0	96nA		
1	1	1	108nA		

SENSH	2	18	6..4	Upper threshold setting of the receiver input (light reserve level). The tolerance of the threshold is approx. ±25%.

6	5	4	Values	Default Setting	Recommended Setting
0	0	0	60nA	X	Set this value 50% above the value set at SENSN, i.e., if SENSN is set to 48nA, set SENSH to 72nA
0	0	1	72nA		
0	1	0	84nA		
0	1	1	96nA		
1	0	0	108nA		
1	0	1	120nA		
1	1	0	132nA		
1	1	1	144nA		

SLOW	2	18	7	no function, must be set to “1”
IVCOFF	2	18	8	no function, must be set to “0”
SENSLC	2	18	9	must be set to “1”
n/a	2	18	12..10	no function, must be set to “0”
TSET	2	18	15..13	Settling time delay from inactive to active mode.

15	14	13	Values	Default Setting	Comments
0	0	0	0	X	If T_{SCAN} >=60µs
0	0	1	1		If T_{SCAN} <60µs

Table 5: epc120 Registers 2 and 18

<table>
<tr><th>Parameter Name</th><th>Register No.
RAM</th><th>ROM</th><th>Bit No.</th><th>Function</th></tr>
<tr><td>FUSEBIT</td><td>3</td><td>19</td><td>0</td><td>This bit will automatically be set when register 18 is programmed.</td></tr>
<tr><td colspan="5">
<table>
<tr><th>0</th><th>Values</th></tr>
<tr><td>0</td><td>Register 18 is not programmed</td></tr>
<tr><td>1</td><td>Register 18 is programmed</td></tr>
</table>
</td></tr>
<tr><td>n/a</td><td>3</td><td>19</td><td>8..1</td><td>no function, must be set to “0”</td></tr>
<tr><td>C2X</td><td>3</td><td>19</td><td>9</td><td>Current amplitude on the 2-wire bus</td></tr>
<tr><td colspan="5">
<table>
<tr><th>9</th><th>Values</th><th>Default Setting</th><th>Recommended Setting</th></tr>
<tr><td>0</td><td>8mA</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>16mA</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>CDET</td><td>3</td><td>19</td><td>11..10</td><td>Detection level for the comparator on the 2-wire bus. The level represents the optimum signal amplitude on the bus.</td></tr>
<tr><td colspan="5">
<table>
<tr><th>11</th><th>10</th><th>Values</th><th>Default Setting</th><th>Recommended Setting</th></tr>
<tr><td>0</td><td>0</td><td>50mV</td><td>X</td><td></td></tr>
<tr><td>0</td><td>1</td><td>n/a</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>100mV</td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>200mV</td><td></td><td>X</td></tr>
</table>
</td></tr>
<tr><td>TPER</td><td>3</td><td>17</td><td>15..13</td><td>must be set to “010”</td></tr>
<tr><td colspan="5">
<table>
<tr><th>15</th><th>14</th><th>13</th></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
</table>

Table 6: epc120 Registers 3 and 19

All other registers are factory set and must not be used or altered.

8. Sample Parameter Setting

If we are going to use a system with a maximum cable length of 3 meters, and the maximum speed on the 2-wire bus, it is recommended to set the registers as follows:

			Bit #															
	ROM	RAM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register #	0	16	1	1	1	0	0	1	1	0	0	0	0	1	0	0	0	X
	1	17	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	X
	2	18	0	0	1	0	0	0	1	0	1	0	0	1	0	1	1	X
	3	19	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	X
	4	20	don't use															
	5	21	don't use															
	6	22	don't use															
	7	23	Address										don't use					X
	8	24	Chip ID															
	9	25																
	10	26																
	11	27																
	12	28																
	13	29																
	14	30																
	15	31																

Figure 13: Sample parameter setting for high speed operation

9. Timing

Overview

To operate the individual elements at the 2-wire bus, some steps per element are necessary. The following drawing shows the concept:

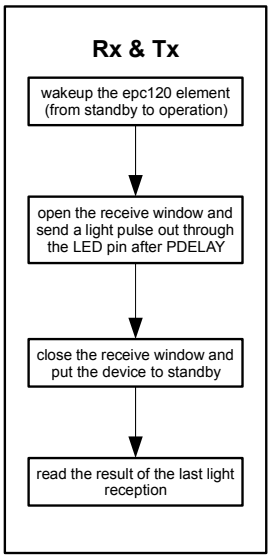


Figure 14: Basic sequence to operate one light beam. Note that the process in the receiver and in the transmitter are running concurrently.

The individual epc120 elements at the 2-wire bus are normally in a sleep mode in order to keep the overall power consumption as low as possible. Thus, an epc120 element has to be activated before it can be used. This wakeup procedure needs a certain time until all internal operating levels have been stabilized. This time is called settling time which can be set with the parameter TSET. Then, the receive window can be opened and the internal LED driver send a pulse out through the LED pin, which the chip can receive, if no obstacle is in the light beam. After that, the receive window must be turned off which also puts the receiver to standby. Finally, the receive results which are stored in the ecp120 element can be read.

In fact, there are several steps to operate one light beam only. This needs quite a long time if everything is done in a strictly sequential way. In order to improve the performance of the whole system, certain steps can be done in parallel. The following chapters describe the timing processes in more detail.

Timing

The microprocessor in the bus controller controls epc120 with SCAN commands. Every SCAN command includes an address which selects the requested epc120 element.

PD PIN operation: A first SCAN command switches the selected epc120 element from standby into operation mode. The process from standby to operation requires a certain time which is called settling time (see Figure 15). The settling time minimum is 60µs. The second SCAN command opens the the reception window, there also the pulse at the LED PIN is sent, where a third SCAN command closes the reception window and puts the epc120 element back to standby. The fourth SCAN command fetches the received results.

LED PIN operation: A first SCAN command switches the selected epc120 element from standby into operation mode. The process from standby to operation requires a certain time which is called settling time (see Figure 15). The second SCAN command starts the light pulse window. After the time PDELAY, one light pulse of the length TPULSE is generated. A third SCAN command puts the element back to standby. If the TSTMP and the period of the SCAN commands of the microprocessor are equal the pulse will be emitted exactly in the middle of the reception window.

The whole operation is optimized for shortest possible scan periods. Figure 15 shows the timing for a settling time of one scan period (TSET=0) and the addresses given in the shortest possible sequence.

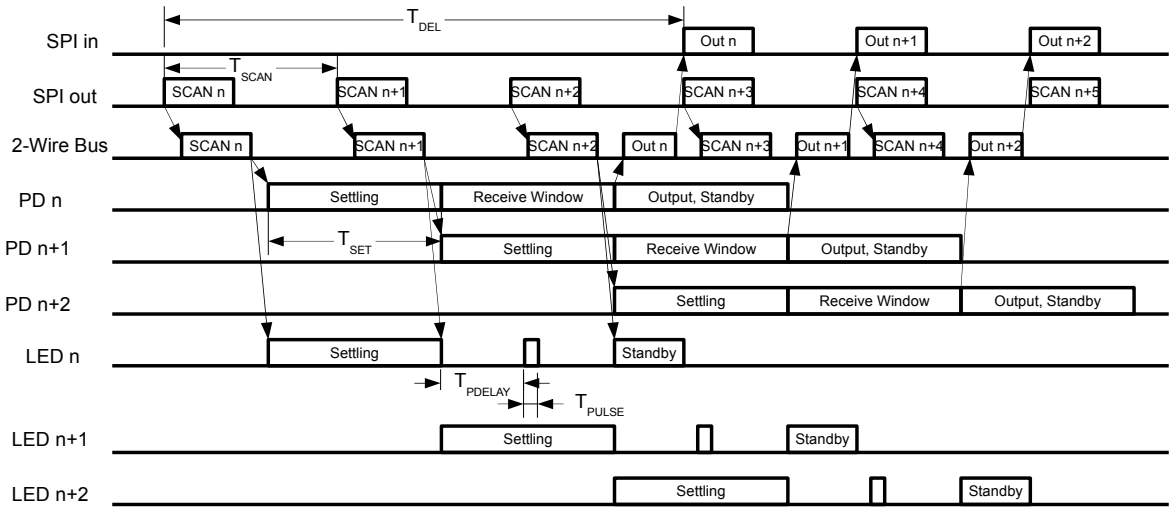


Figure 15: Timing of the scan process

where

n = element number

T_{SCAN} *= interval between two scan commands which is given by the micro processor*

The minimum delay time between the first SCAN command and the earliest possible access of the result can be calculated as a function of the scan period T_{SCAN}:

$$T_{DEL} = 3 \cdot T_{SCAN}$$

The sensor device counts the number of SCAN commands on the bus to present its result at the right time. If the number of a SCAN command is n, the result will arrive with the SCAN command n+3.

The timing of the emitter commands have to be adjusted in order to emit the light pulse near the center of the reception window of the corresponding receiver. E.g. if the reception window length is set to 30 µs, the light pulse shall be generated 15µs after the opening of the receive window. The length of the reception window is defined by the time elapsed between the second and the third SCAN command. The parameter TSTMP defines the time window to measure the arrival time of the received light pulse. This result is returned in the result TIMESTAMP. The timing position of the following light pulses can be optimized to the center of the receiving window. The resolution of TIMESTAMP is 4 bits. Thus, the value is 0000 if the pulse is received at the beginning of the window, and 1111 if it arrived at the end. A light pulse received approx. in the middle of the receive window would be represented as 0011, 0100 or 0101.

The minimal scan period, which is the time between two consecutive SCAN commands, is given by the communication on the 2-wire bus: 62 bits for the command and the results have to be transmitted in this time. The minimal scan period is then

$$T_{SCANmin} = 31 \cdot T_{CLK} \cdot k$$

k is given by the parameter DRATE and varies between 1 and 8 (refer to Table 1, Table 3 and Table 7). T_{CLK} is 1µs. Thus, the minimal scan period is 31µs or the 2Mbit/s transmission.

Special Cases

- If the same device is addressed again at the end of its reception window, it continues waiting for pulses. This procedure allows to synchronize the receiver with the transmitter on an optical basis, if there is no electrical synchronization.
- If a device detects a command during a scan operation which is not the command SCAN, it is put into standby mode.
- A SCAN command with address 0 can be used to fetch the results without starting a new scan command.

10. SPI Interface

The SPI interface allows the microcontroller to communicate with the sensors over the 2-wire bus system via the interface device.

While data are sent to the interface chip by the microcontroller, the result of the last (or more generally: a previous) command is sent from the interface chip to the microcontroller according to the SPI protocol. The timing diagram is shown in Figure 16).

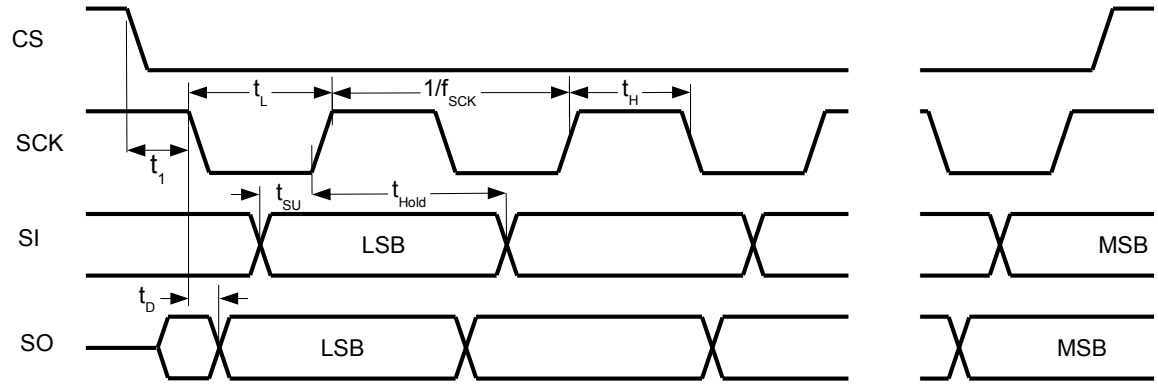


Figure 16: SPI bus timing

Timing Specification SPI Interface

Symbol	Parameter	Conditions/Comments	Values			Units
			Min.	Typ.	Max.	
f_{SCK}	SCK Clock frequency				10	MHz
t_H / t_L	HIGH and LOW period of SCK		50			ns
t_{SU} / t_{Hold}	Set-up and hold time SI		15			ns
t_1	Edge time CSB - SCK		50			ns
t_{rf} / t_{rfSCK}	Rise / fall time	SO, SCK			20	ns
t_D	Data valid after SCK edge	SO			20	ns

Command Overview

General Description

Communication is based on telegrams, which are sent and received over the 2-wire bus. Such telegrams are initiated by the respective command to the SPI interface. The epc10x chips accept two types of commands:

1. Commands which communicate to the interface chips, also called “Direct Commands” (Figure 17).
2. Commands which communicate to the chips at the 2-wire bus, also called “Broadcast Commands” (Figure 18).

The first bit in the data stream from the microprocessor to the interface chip (SI pin) defines whether it is a command to the interface chip (a “0”) or the the chips on the 2-wire bus (a ”1”).

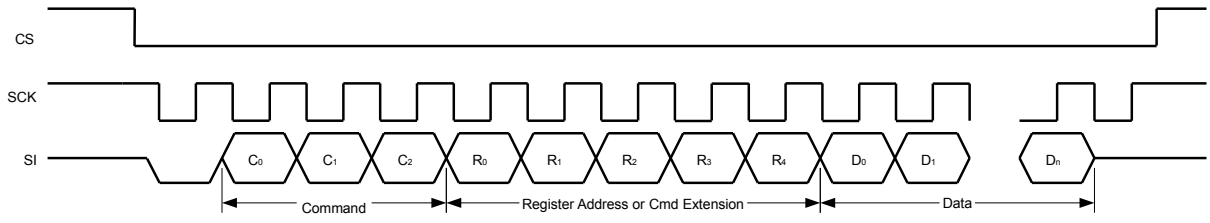


Figure 17: Communication to the interface device (Direct Command)

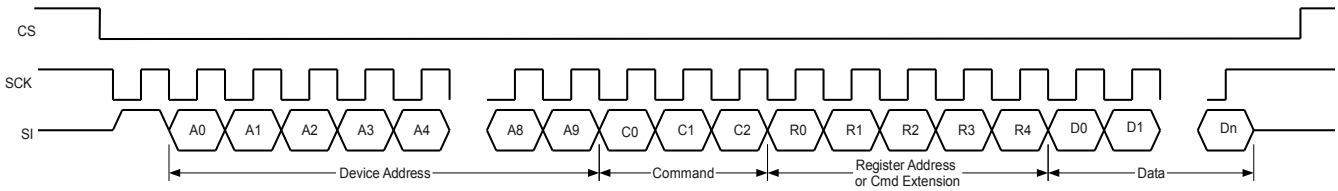


Figure 18: Communication to the sensor devices (Broadcast Command)

Command List

Name	Command Code C_0 .. C_2	Command Extension Code R_0 .. R_4	Function	Mode	Number of data bits on 2-wire bus D_0..D_n	Returned Data
SCAN	000		Scan	Broadcast	62	Yes
NOP	000		No operation	Direct	0	Yes
READ	010	Register address	Read	both	97	Yes
WRITE	011	Register address	Write to volatile register	both	62	No
ADRA	101		Address allocation	Broadcast	62	No
PROG	110	Register address	Program	both	62	No
TEST	111	10000	Test mode	both	80	Yes
RESET	111	11001	Reset the device	both	62	No

Table 7: Command list

Remarks:

- Additional SCK clock cycles have no effect.
- The telegram length on the 2-wire bus is given in the number of data clock cycles. It allows to calculate the minimum interval between two commands.
- If an SPI command is given while another command is being transmitted on the 2-wire bus, the new command is ignored.
- The READ and WRITE commands in the direct access mode require 2 additional SCK cycles.

Command SCAN

The command SCAN enables the addressed device, times the ongoing operation or fetches the scan result. The operation of the command SCAN is described more in detail in Chapter Timing.

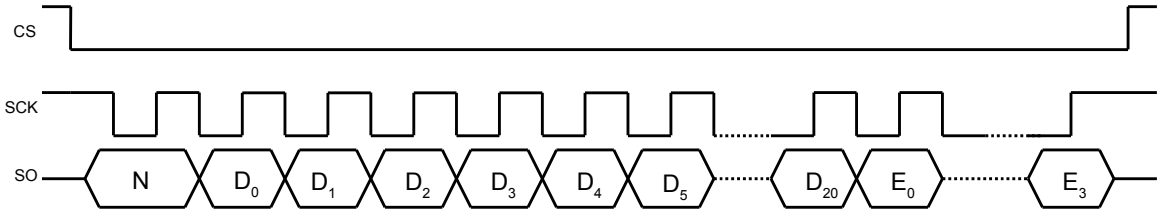


Figure 19: Timing of the results of a SCAN command

The bit N indicates whether a new result has been received. D_0...D_3 contains the timestamp, D_4 and D_5 contains the status, D_{11}...D_{20} contains the device address, E_0...E_3 contains an error code. D_6...D_{10} are empty.

Data Bits	Function
N	Indicates, if new data is available **N** / **Values** 0 / no new data available 1 / new data available
D_0 … D_3	Timestamp
D_4	Status of receiver threshold “normal” **D_4** / **Values** 0 / Receiver threshold set by SENSN not reached 1 / Receiver threshold set by SENSN exceeded
D_5	Status of receiver threshold “high” (light reserve) **D_4** / **Values** 0 / Receiver threshold set by SENSH not reached 1 / Receiver threshold set by SENSH exceeded
D_6… D_{10}	empty, not used
D_{11} … D_{20}	Device address
E_0 … E_3	Error codes, refer to Chapter Error Codes

Table 8: Result of a SCAN command

Command NOP

The command NOP can be used to fetch the last received data without sending a new command. With this command it is possible to monitor the 2-wire interface by a second interface device in a redundant system.

Command TEST

The command TEST issues an internal test pulse or a DC current at the PD input pin on a specific receiver. It simulates basically a received light pulse or DC sunlight influence to check the proper functionality of the receiver(s) without using an emitter. This mode is initialized by the command TEST and is left after a complete SCAN sequence.

Code C_0 … C_2	Extension R_0 … R_4	Amplitude D_0 … D_4		Current Shape
111	10000	1xxxxx	25nA	Pulse
		x1xxxx	50nA	Pulse
		xx1xxx	100nA	Pulse
		xxx1xx	100µA	Pulse
		xxxx1x	500µA DC	DC
		xxxxx1	2mA DC	DC

Table 9: Self Test

The applied current is the sum of different current sources: In column “Pulse Amplitude” of Table 9 a “1” means, that the corresponding current is added. Example: 110000 generates a pulse of 75nA without DC.

Command RESET

The command RESET resets the device and initiates a startup. All devices can be reset simultaneously by using address 0.

Command ADRA

ADRA is used during the configuration of a light curtain system to allocate a logical address to the physical position of the the emitter or receiver element.

The command ADRA stores the device address to the volatile memory only (RAM). If the device address has to be stored permanently, the command PROG has to be used to copy the previous stored device address from the RAM register into the ROM register. ADRA can only be used if there was no previous PROG command to the address register.

The address 0 is reserved to address all devices together or none and must not be used as an individual address.

The command ADRA generates no result.

For details refer to Chapter Address Programming.

Command READ

The RAM and ROM can be read by the command READ. The command is extended by the register address.

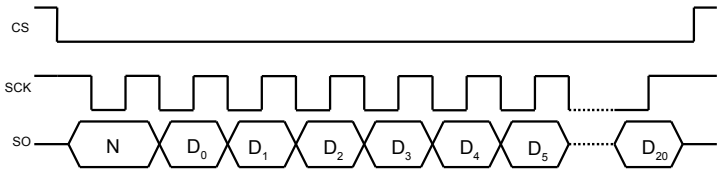


Figure 20: Timing Result Data

The bit N indicates whether a new result has been received (broadcast mode). D_0...D_4 contains the address, D_{11}...D_{20} contains the returned data.

Data Bits	Function
N	Indicates, if new data is available **N** / **Values** 0 / no new data available 1 / new data available
D_0 … D_4	5 bit register address
D_5 … D_{20}	16 bit returned data (one complete register)

Table 10: Result of a READ command

Note:
The result of READ command comes on the SO output in parallel with the transmission of the next instruction (according the SPI protocol).

Command WRITE

Data can be written into the RAM by using the command WRITE. The command is extended by the register address and the data. It is only possible to write to registers if the corresponding register in the ROM has not been written yet. It is not possible to write directly to a ROM register. If the data has to be stored into the ROM register, a subsequent command PROG has to be used.

Command PROG

The command PROG transfers the data from the RAM register to the corresponding ROM register. See chapter Address Programming for a detailed description.

Returned Results

The results at pin SO depends on one of the previous commands and can be fetched by any command or just by toggling SCK while CS is low (=NOP).

- The data is represented with the LSB first.
- After an SPI communication the data register is cleared.
- By holding the CS line to 0 it is possible to trigger on a positive edge of SO.
- If more clock toggles SCK are issued than data can be fetched, zeros are transmitted.

11. Address Programming

General Description

The device address is initially set to “00000” and the devices are not parametrized. However, all devices hold a unique chip ID. However, due to the 2-wire bus concept, the physical location of an individual device is not known to the microcontroller. In order to operate the light curtain, the microcontroller needs to allocate a specific receiver to a specific emitter. Usually, the receiver at one end of the 2-wire bus gets the address 1, the next receiver the address 2 and so on. The same must be done on the emitter side. Once all devices on the receiver and on the emitter side got their address, the microcontroller can operate the light curtain. The address allocation, meaning the allocation of a physical location to a logical address, is usually done in the factory of the light curtain manufacturer.

To do so, a specific address allocation procedure together with the parametrization of the devices must be executed first. The following procedure is an example how to allocate a unique address and how to parametrize each device.

No.	Step	Description
1	Set the address of the interface device	Set the address of the interface device with a direct command to a fix number, which should not be 0. It is recommended to use generally the address 1023 for the interface device.
2	Parametrize the devices on the 2-wire bus	The data rate DRATE of the 2-wire interface is initially set to 250 kbit/s. It shall be set to the correct value by addressing all devices, which are initially at address 0, simultaneously. During this step, all other parameters in register 16 can also be set.
3	Parametrize the interface device	The data rate of the 2-wire interface is initially set to 250 kbit/s. It has to be set to the same value like the other devices on the same 2-wire bus.
4	Set all other registers	For the address allocation the following parameters should be set: TPER = 2 SENSN = 7 SLOW=1 This can be done to all devices at the same time by writing the registers to device 0.
5	Address allocation	Since the devices have an open receive window, all of them are able to receive light pulses. This mode is used to allocate the logical address to the physical location. The procedure is as follows: • Issue the command ADRA using address n • flash a light pulse to the photo diode which is connected to the chip at the physical position n (make sure that all the other photo diodes cannot receive a light pulse). By receiving a light pulse, the address n is stored into the RAM of the element at the physical position n. Thus, the device, which receives a light pulse, memorizes the address n as its own address in the final system. This procedure has to be repeated for every individual element on the 2-wire bus. It is recommended to start with the address 1 for the element which is closest to the controller and increment the address by 1 with every individual element. In the case of a 20-beam light curtain, addresses from 1 to 20 on the receiver and on the emitter side are accessible. However, the interface chip is usually located at address 1023.
6	Address check	It is recommended to check the correct address setting by addressing every device in the system using the READ command. All devices addressed shall response to the READ command.
7	Address programming	Once all addresses of all devices at the 2-wire bus are stored into the RAM (register 23), the address should be transferred to the ROM (register 7) for each device separately by using the command PROG. Please refer to chapter 11. Address Programming.
8	Set parameters	Parameters like TSTMP, MODE, VMODE, TPULSE etc. are stored into the RAM of all devices using the command WRITE. If the global address “0” is used, all devices receive the parameters at the same time. Since the internal voltage regulator of the interface device is not needed, the parameter SOFF has to be set to “1” (refer to Table 3). All other devices at the 2-wire bus must have a “0” for SOFF.
9	Check parameters	The parameters should be checked by reading them back from each device using the READ command.
10	Program parameters	If all parameters are stored correctly, store the parameters into the non-volatile memory by using the command PROG.
11	Test programming and addressing	To check the programming of addresses and parameters, turn off the power supply or reset all devices and readout all addresses and parameters again.

Programming Procedure

Programming the device is a transfer of the data from the RAM to the corresponding ROM register. Each 16-bit register must be transferred individually. Thus, register 16 is transferred to register 0, register 17 to register 1, register 18 to register 2, register 19 to register 3, and register 23 to register 7. All other registers must not be used.

Figure 21 shows the timing of the programming sequence for one register:

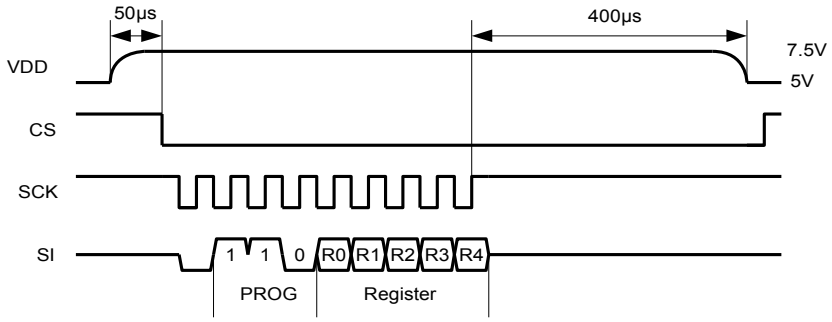


Figure 21: Direct programming procedure

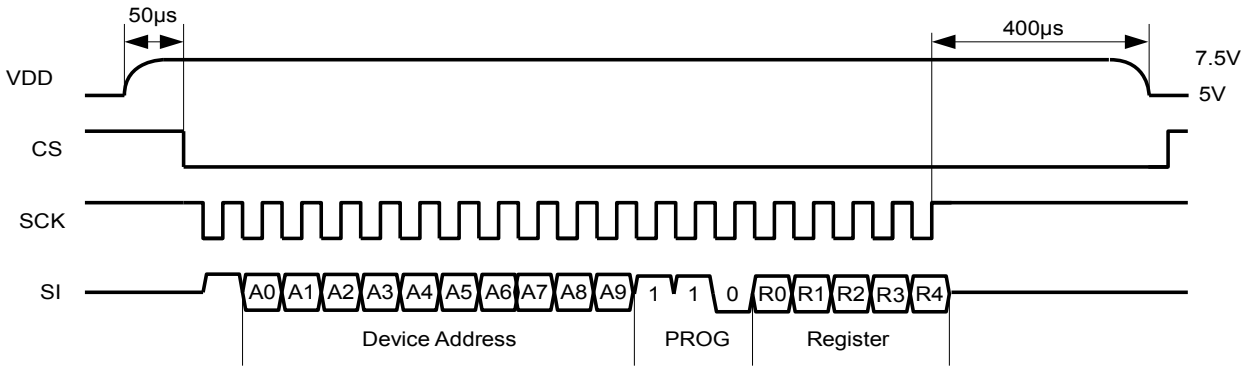


Figure 22: Broadcast programming procedure

"PROG" is the PROG command sequence (110).

"Register" means the address of the target register (ROM), e.g. 0, 1, 2, 3, 7.

During programming, the voltage at pin VDD has to be increased to V_{prog} (7.5V) and has to be kept stable buffered during the whole programming cycle. The timing parameters given in Figure 21 and Figure 22 have to be obeyed.

Remarks:

- It is possible to program more than one register during a VDD high cycle. Between two PROG commands a delay of 400 µs is needed.
- Each register can be programmed once only (OTP).
- After programming a register, bit no. 0 of this register becomes automatically a one to indicate that the register is programmed.

12. Considerations for Safety Applications

Since the epc120-family chips can be used in safety related products, like machine safety light products, certain data integrity mechanisms have been integrated. The safety concept on chip and communication level are described in this chapter.

Data Integrity on the 2-Wire Power-Bus

Several mechanisms on different layers are implemented to guarantee a low residual error rate on the 2-wire power-bus.

Physical layer

- Modulation and medium: Current modulation on a twisted pair line is highly immune to interference.
- Start bit detection: The start pulse must have the correct orientation. Otherwise, the pulse is discarded.
- Pulse alternation: Since Manchester coding is used, the pulses need to alternate. An error is detected, if this is not the case.
- Pulse timing: The timing of the information pulses is fixed. A missing bit (too long pause) is detected as an error.
- End bit detection: Since current modulation is used and the current is switched off when the message is completed, the last pulse has a specified orientation.
- Sequence length: The message length is well known. A too short or too long message is detected as an error.

Data link layer

- Error control coding: If no errors have been detected on the physical layer, the received pulse sequence is processed by an error control algorithm. Depending on the application, *either* 2 errors can be corrected, *or* 4 errors can be detected. A higher number of errors can be detected with a reliability of 1000:1.
- Strict master-slave system: A sensor may only respond, if a request from the microcontroller was correctly received.
- Explicit addressing: Each message (master > slave and slave > master) contains the address of the sensor element. Even if the wrong sensor replies to the microcontroller call, the error will be detected.

Residual Error Rate

Although no explicit calculations have been done yet, the residual error rate of the 2-wire power-bus is at least as good as in the ASi. The ASi has an residual error probability of a system with Hamming distance 5 (HD5) and belongs to the DIN 19244 data integrity class I2 for an error probability p=1e-2, and to class I3 for p=1e-3.

Error Cases

Each sensor device has its unique address. The microprocessor addresses each device individually and fetches the result some scan periods later. The result includes also the address of the answering device.

Error Cases	Consequences
2 sensor answer on the same address	Collision during the transmission of the result. → Error detection in the interface device → Error state.
Error during the scan command	No device answers → no data (all zero).
Error during result transmission	Error detection in the interface device → Error state.

Error Codes

Different error states are monitored:

	Device	Error	Action	Error Code E0 … E3
1	Sensor	Non-correctable error in the received telegram	Device doesn't response	-
2	Sensor	Command to fetch the result too early	Normal answer	-
4	Interface	No answer from the sensor device	Result data zero	-
5	Interface	Non-correctable error in the received telegram	Error reported	1xxx *)
6	Interface	Return telegram not complete	Error handling procedure	0100

Table 11: Error states

*) The last three error bits contain the number of detected errors.

Layout Information (all measures in mm,)

CSP-10 Package

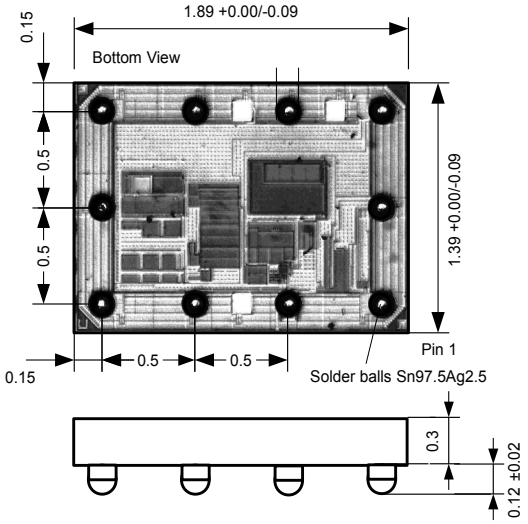


Figure 23: CSP10: Mechanical dimensions

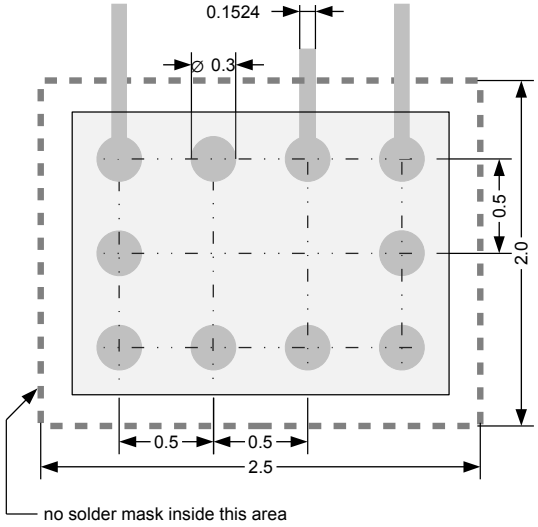


Figure 24: CSP10: Layout recommendation

QFN-16 Package

Note: For sampling only. Limited quantities. Please inquire

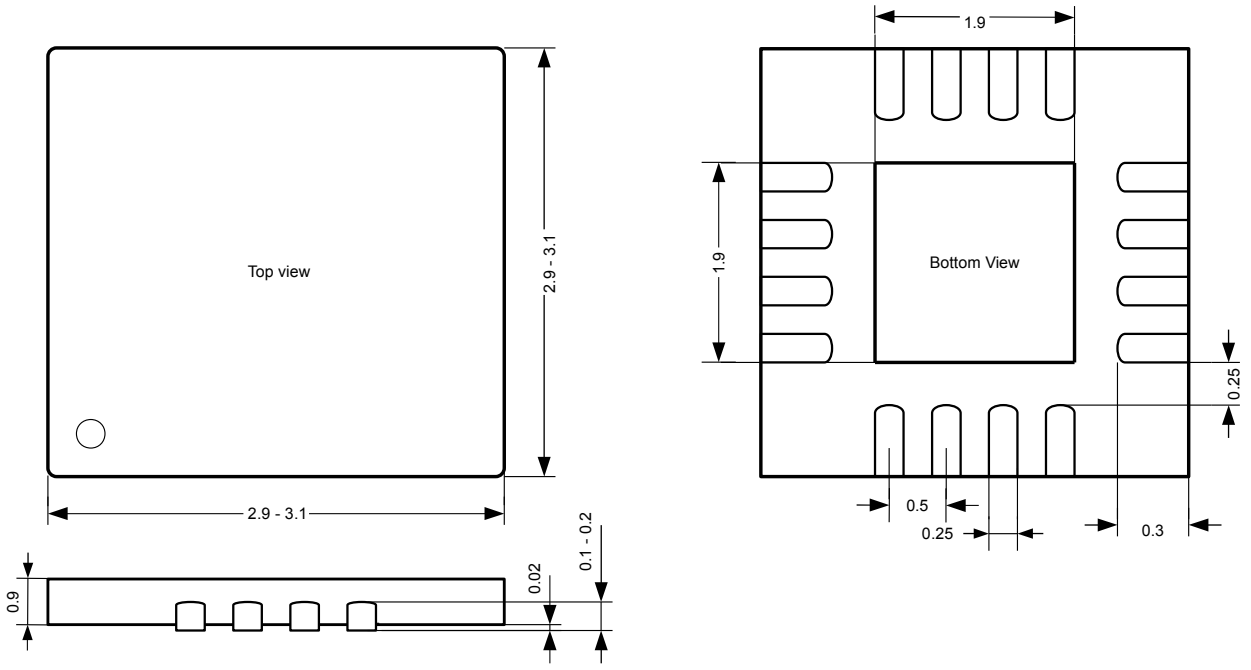


Figure 25: QFN-16: Mechanical dimensions

Reflow Solder Profile

For infrared or conventional soldering the solder profile has to follow the recommendations of IPC/JEDEC J-STD-020C (min. revision C) for Pb-free assembly for both types of packages. The peak soldering t emperature (T_L) should not exceed +260°C for a maximum of 4 sec.

Packaging Information (all measures in mm)

Tape & Reel Information

The devices are mounted on embossed tape for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate data sheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.

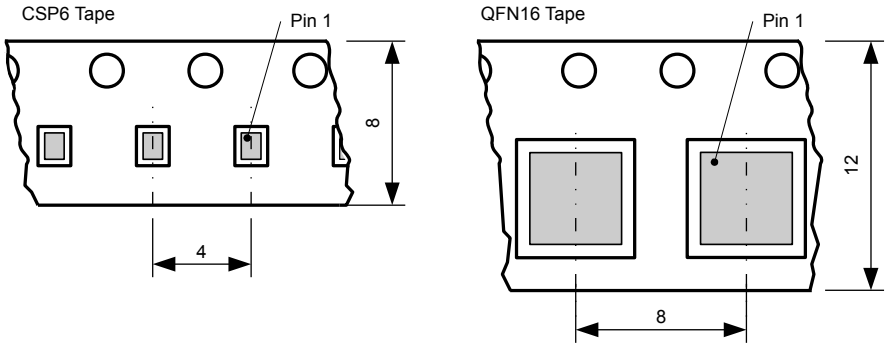


Figure 26: CSP10 and QFN16 Tape Dimensions

ESPROS Photonics AG does not guarantee that there are no empty cavities. Thus, the pick-and-place machine should check the presence of a chip during picking.

Ordering Information

1. Standard product:

Type	Package	RoHS compliance	Packaging Method
epc120-CSP10	CSP10	Yes	Reel

Note: For sampling only. Limited quantities. Please inquire.

Type	Package	RoHS compliance	Packaging Method
epc120-QFN16	QFN16	Yes	Reel

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