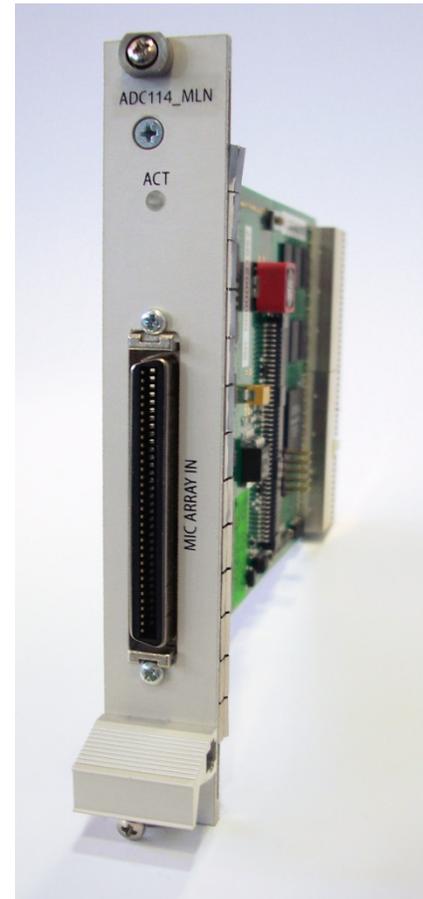


Features

- Multi-channel analog interface SyMBus24
MDR68 front connector for reliable repetitive plugging 24 symmetrical inputs for high disturbance immunity
 - 2x $\pm 1V$ input-voltage range biased at 2.5V
 - Low noise (typically $2\mu V_{20Hz-20kHz}$ input-referred)
 - 5V, 6V and switchable 12V for sensor supply
 - Pull-down activated bidirectional control-signal
 - Decoupled serial interface for intelligent sensors
- Simultaneous 24bit A/D-conversion at 48/96/192kS/s
DC- and AC-mode (for improved accuracy) available
- Advanced Record-Trigger capability
Adjustable between start and end of recording
Activated by software, hardware or input-voltage
- 32bit recording makes gain-setting obsolete
- 1536MB cPCI-independent onboard real time memory
16MS / input for up to 349s recording time (48kS/s)
- Concurrent cPCI-Streaming up to the limits of the harddisc (96/192kS/s down-sampled to 48kS/s)
- Nonvolatile calibration and configuration memory
- Onboard voltage and temperature monitoring
- Full Color RGB status LED (marked ACT)
- Low power consumption (8.75W typically)

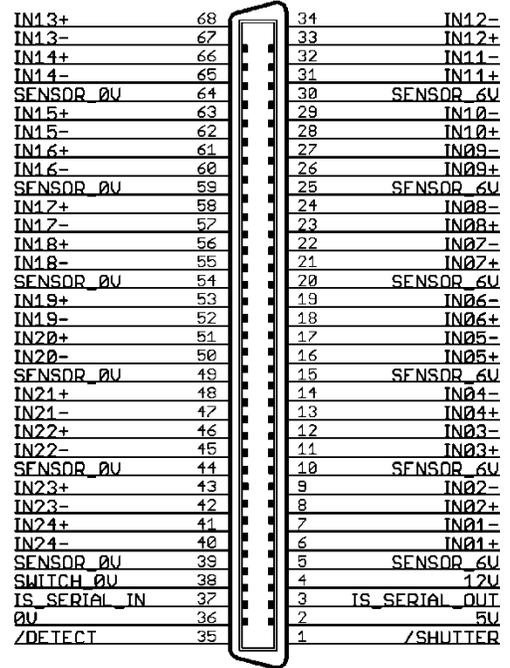
Description

The ADC114_MLN is a low power 3U 4HP cPCI slot-in card that has mainly been developed for the connection of microphone arrays to the mcdRec data-recorder. Its 24 channels have a 100% pure differential signal path from the input connector to the 5th-order multi-bit delta-sigma analog-to-digital-converters ensuring extraordinary immunity against disturbances being coupled into the cables. 12 contacts of the MDR68 front connector are for sensor supply. Furthermore 0V, 5V, 12V and a switchable 0V contact support various power-supply eventualities. /DETECT checks for plugged



MDR68 front connector scheme

sensors and an optically decoupled serial interface is used to communicate with self describing sensors. Concurrent capabilities allow for high-channel recording with many cards (1536MB onboard RAM) and Longtime Streaming. Results of the factory-calibration are stored in a nonvolatile memory and used for compensation while measuring.



cPCI J2 connector scheme (not standardized)

	e	d	c	b	a
22					
21	AGND	RC_ENA	AGND	PGA0	PGA1
20	AGND	GND	AGND	PGA2	PGA3
19	AGND	PGA4	AGND		
18	+6V5	GND	AGND		
17	+6V5	RS2_TX	+6V5	GND	/RS2_TX
16	+6V5	GND	+6V5	/RS2_RX	
15	+6V5	RS2_RX	+6V5	GND	
14		GND		/ENA_RECTRIG	
13		RS1_RX_TTL	VIO	GND	
12	RS2_TX_TTL	GND		/ENABLE	
11		RS1_TX_TTL	VIO	GND	
10	RS2_RX_TTL	GND		/SHUTTER	
9		/RECTRIGGER	VIO	GND	
8		GND	AUXIOP3	/STOPSTREAM	
7			VIO	GND	
6		GND	AUXIOP2	/SYNCHRONIZE	FPGA_TDO
5	FPGA_TCK		VIO	GND	FPGA_TDI
4	FPGA_TMS	GND	AUXIOP1		VIO
3	/FPGA_CE	FPGA_CONF_DONE	+3V3	GND	
2	/FPGA_CS	/FPGA_CONFIG	FPGA_DCLK	24576KHZ	
1	FPGA_ASD	FPGA_DATA	+3V3	GND	

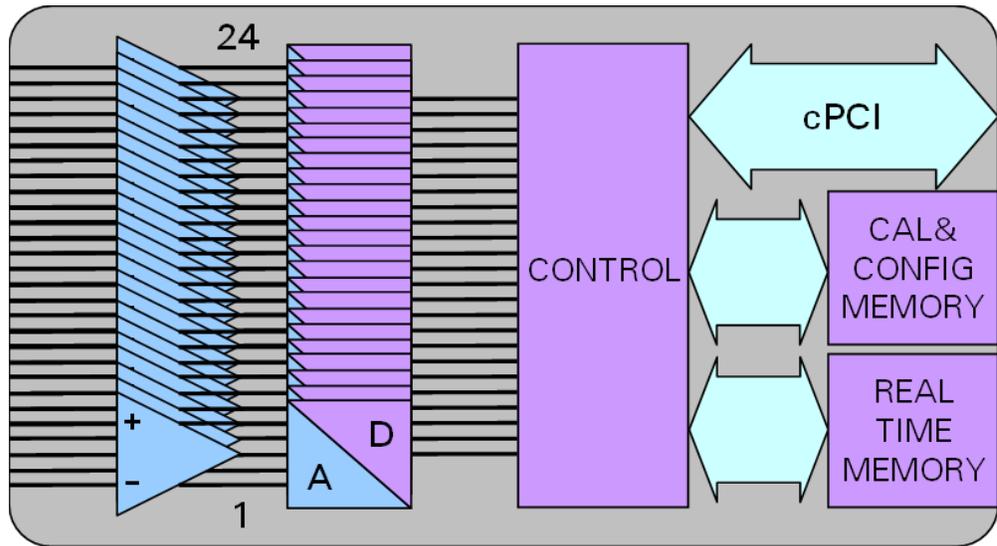
cPCI J1 connector scheme (standardized)

	e	d	c	b	a
25	+5V	+3V3			+5V
24		AD0	VIO	+5V	AD1
23	AD2	+5V	AD3	AD4	+3V3
22	AD5	AD6	+3V3	GND	AD7
21	C/BE0	M66EN	AD8	AD9	+3V3
20	AD10	AD11	VIO	GND	AD12
19	AD13	GND	AD14	AD15	+3V3
18	C/BE1	PAR	+3V3	GND	/SERR
17	/PERR	GND			+3V3
16	/LOCK	/STOP	VIO	GND	/DEVSEL
15	/TRDY		/IRDY	/FRAME	+3V3

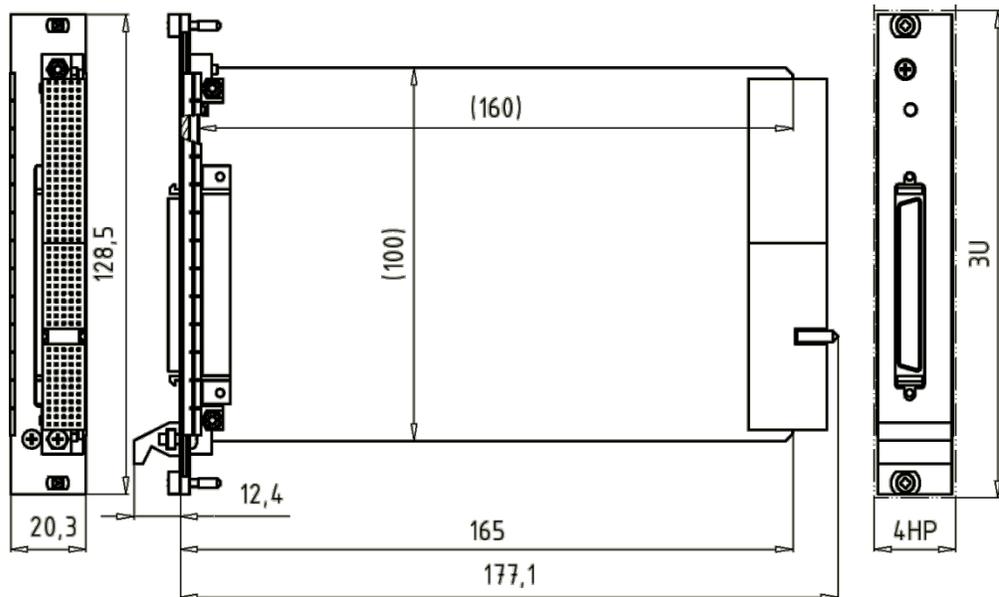
blanks are not connected on the card

11	C/BE2	GND	AD16	AD17	AD18
10	AD19	AD20	+3V3	GND	AD21
9	AD22	GND	AD23	IDSEL	C/BE3
8	AD24	AD25	VIO	GND	AD26
7	AD27	GND	AD28	AD29	AD30
6	AD31	CLK	+3V3	GND	/REQ
5	/GNT	GND	/RST		
4		+5V	VIO		/INTA
3	TDI	TDO		+5V	
2	+5V	+12V		-12V	+5V

Block diagram



Mechanical data



Weight

175g

Absolute maximum ratings

Parameter	Min	Max	Unit	Remarks
Power				
+12V to GND	-0.3	14	V	Stresses above these may cause permanent damage. This is a stress rating only; functional operation at these or any other conditions above is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Only one absolute maximum rating may be applied at any one time.
+6V5 to AGND	-0.3	8	V	
+5V to GND	-0.3	6	V	
+3V3 to GND	-0.3	4	V	
VIO to GND	-0.3	4	V	
Analog inputs to AGND	-3	8	V	
Digital inputs to GND	-0.3	4	V	
Storage temperature	-50	125	°C	

Conformity

Electrical safety	complies with DIN EN 61010-1
Electromagnetic compatibility (EMC)	complies with DIN EN 61326

Operating conditions

Parameter	Min	Typ	Max	Unit	Remarks
Power supply					
(+12V)	11.4	12.0	12.6	V	voltages at the cPCI connectors J1+J2 must be guaranteed to be within these limits
(+6V5)	6.3	6.5	6.7	V	
(+5V)	4.7	5.0	5.3	V	
(+3V3)	3.0	3.3	3.6	V	
(VIO)	3.0	3.3	3.6	V	
Output current (front)					
5V	0		55	mA	all outputs are short-circuit-proof 5V and 12V shall return at 0V or SWITCH_0V the six SENSOR_6V shall return at the six SENSOR_0V typical value is for SyMBus24 microphone array
12V	0		220	mA	
SWITCH_0V	-220		0	mA	
SENSOR_6V	0	336	660	mA	
Analog inputs					
IN+ to IN-	-1.7		1.7	V	analog inputs are DC-biased at 2.5V
IN+ to SENSOR_0V	-0.7	2.5	5.7	V	
IN- to SENSOR_0V	-0.7	2.5	5.7	V	
/DETECT input					
low	0		0.7	V	10k Ω pull-up-resistor to +3V3 is on the card
high	1.7		3.3	V	
IS_SERIAL_IN					
low	0		0.4	V	330 Ω resistor to optocoupler-cathode, anode to+3V3 (on card)
high	2.2		4	V	
IS_SERIAL_OUT					
low	0.5		2.4	V	applicable when connected to optocoupler-cathode and optocoupler-anode is connected to+5V (at sensor)
high	3.6		5	V	
/SHUTTER and /RECTRIGGER					
low	0		1	V	both these and also /STOPSTREAM must be pulled-up with 220 Ω resistors to VIO on the backplane
high	2		3.3	V	
Temperature	0		70	°C	the air surrounding the card must be within these limits
Relative humidity	10		80	%	not to be operated until condensation is evaporated

All other inputs and outputs are of the LVTTTL-type (max-low=0.7V, min-high=1.7V).
 /ENA_RECTRIG, /ENABLE and /SYNCHRONIZE must be pulled-up with 1k Ω resistors to VIO on the backplane.
 24576kHz is an input and shall be connected to a stable and accurate clock-source.
 SENSOR_0V is connected to AGND, 0V is connected to GND, AGND and GND are not connected on the card.
 AGND and GND shall be connected only once in the mainframe.

Electrical characteristics

Parameter	Min	Typ	Max	Unit	Condition
Differential full-scale input-voltage	1.2	1.3	1.6	V _{eff}	
Differential input-resistance	1861	1880	1899	Ω	between +inputs and - inputs
Input referred noise					
@ 48kS/s		2.0		μV _{eff}	inputs shorted, 20Hz...20kHz-weighted
@ 96kS/s		2.0		μV _{eff}	
@ 192kS/s		2.0		μV _{eff}	
Dynamic performance					
Dynamic range @ 48kS/s (A-weighted)	113	119		dB(A)	full-scale input related to noise, inputs shorted
(20Hz...20kHz-weighted)	110	116		dB	
Dynamic range @ 96kS/s (A-weighted)	113	119		dB(A)	
(20Hz...20kHz-weighted)	110	116		dB	
(20Hz...40kHz-weighted)	107	113		dB	
Dynamic range @ 192kS/s (A-weighted)	113	119		dB(A)	
(20Hz...20kHz-weighted)	110	116		dB	
(20Hz...40kHz-weighted)	107	113		dB	
(20Hz...80kHz-weighted)	105	111		dB	
Total harmonic distortion + noise					
@ 48kHz		tbd		dB	most distorted channel @ input 1kHz, -3dB, 20Hz...20kHz-weighted
@ 96kHz		tbd		dB	
@ 192kHz		tbd		dB	
Accuracy					
DC-offset-error		336k	1280k	LSB	worst channel @ 192kS/s, inputs shorted
Input referred DC-offset-error		297	1133	μV	
AC-offset-error		695	3200	LSB	
Input referred AC-offset-error		1	3	μV	
Channel separation					
Crosstalk @ 1kHz (800Hz...1250Hz-weighted)		-125	-100	dB	most disturbed channel related to driven channel @ input -3dB, 192kS/s
Crosstalk @ 10kHz (8kHz...15kHz-weighted)		tbd	-60	dB	
Disturbance immunity					
Common mode rejection ratio @ 100Hz, 500 mV _{eff}	36	tbd		dB	differential gain related to common gain of most disturbed channel @ 192kS/s, all inputs connected
Common mode rejection ratio @ 10kHz, 500 mV _{eff}	30	tbd		dB	
Common mode rejection ratio @ 50kHz, 500 mV _{eff}	27	tbd		dB	
Maximum common mode input voltage (100Hz...100kHz)	1.8	tbd		V _{eff}	
Power supply current					
(+12V)		0	10	mA	measured with 100mΩ shunt- resistors @ 192kS/s, open inputs
(+6V5)		1271	1600	mA	
(+5V)		19	25	mA	
(+3V3)		298	350	mA	
(VIO)		3	50	mA	
Power consumption					
(+12V)		0.00	0.13	W	supply currents from above, voltages measured between shunt-resistors and card
(+6V5)		7.67	10.56	W	
(+5V)		0.10	0.13	W	
(+3V3)		0.97	1.21	W	
(VIO)		0.01	0.17	W	
(total)		8.75	12.20	W	

Theory of operation

Real world measurement sites are full of disturbances. Shielding is common practice and helps to decrease the problems thereof. Another approach is to use symmetrical/differential transmission techniques where two signals are used. A positive and a negative signal of the same amplitude are subtracted from each other and since $1 - (-1) = 2$ the result is useful. When both symmetrical wires are close together or are a twisted pair any disturbance couples into them with the same amplitude and direction; both are positive or both are negative – that is called common-mode- disturbance. The subtractor eliminates that disturbance because $1 - 1 = 0$ and also $(-1) - (-1) = 0$.

Compared to the TWICE AS MUCH SINGLE ENDED AS DIFFERENTIAL INPUTS concept (figure 1) where the common-mode-disturbance can only be removed after the input-amplifiers this AS MUCH SINGLE ENDED AS DIFFERENTIAL INPUTS design (figure 2) uses a 100% pure differential signal path which removes any common-mode-disturbance when it enters the input-stage. The advantage is that the common-mode-disturbance does not reduce the differential input-voltage-range.

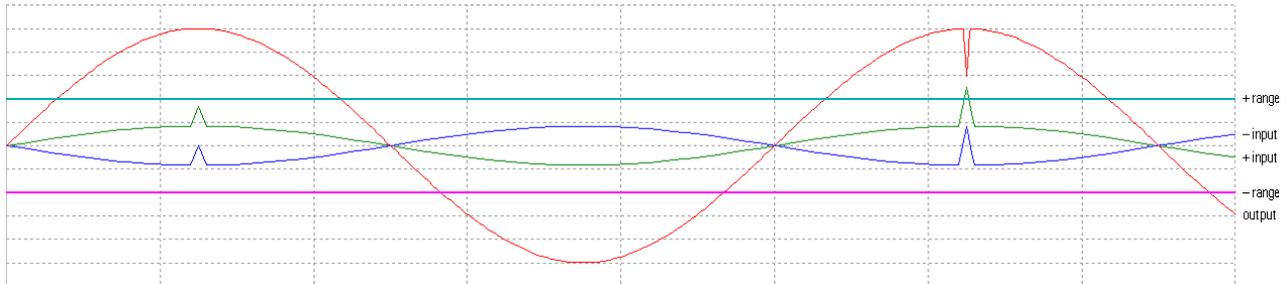


figure 1 common-mode removed after the input-stage: input-signal+disturbance must be within the input-voltage-range

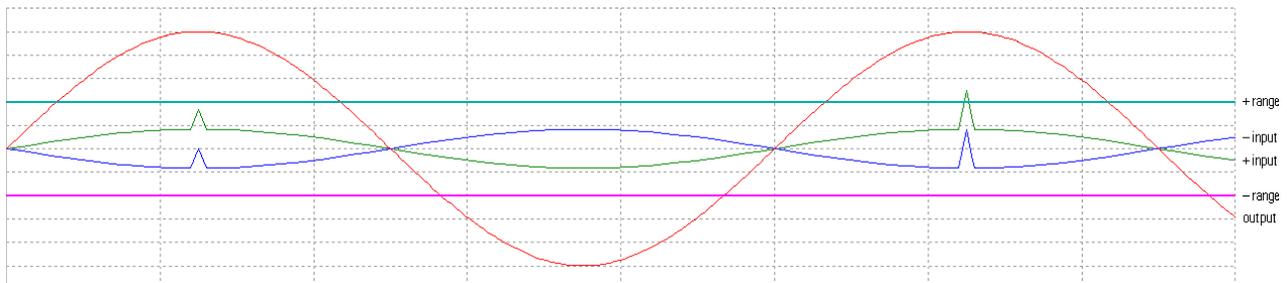


figure 2 common-mode removed at the input-stage: input-signal+disturbance can be above the input-voltage-range

Signals entering the card are passing ESD-protections and well balanced differential LRC-filters where high-frequency-components are removed that the following amplifiers cannot damp sufficiently. These symmetrical-I/O-amplifiers cancel common-mode-disturbances, amplify the differential-signals and add a pole for bandwidth-limitation. Together with the subsequent differential RC-filters a total attenuation of 61dB is achieved at half the oversampling-speed of the simultaneously sampling differential 5th-order multi-bit delta-sigma analog-to-digital-converters – low aliasing-distortions are the benefit. The converters offer selectable reduction-low-pass-filters for 48, 96 and 192kHz output rate and a high-pass-filter can be switched on to reduce the offset whenever DC is not of interest.

The digital control unit collects the serial 24bit data-streams from the converters, filters and optimizes them to 32bit words and stores up to 16MS / input in real time memory; when full, oldest data is overwritten by the latest.

Streaming via the cPCI bus is performed simultaneously; 48kS/s is sent directly, 96kS/s and 192kS/s are down-sampled to 48kS/s. End-point of recording can be between Record-Trigger and 349 seconds later. The Record-Trigger can be released by cPCI-command, pulling down /RECTRIGGER at J2 or reaching a cPCI-register definable value of one of the first eight input-channels.

/SHUTTER is a pull-down-activated bidirectional control-signal; it is available at J2 and the front connector and can be sensed and released through cPCI.

/DETECT is another pull-down-activated signal; it is available at the front connector and can be sensed through cPCI. IS_SERIAL_IN is decoupled by an optocoupler and connected to RS2_RX_TTL at J2; IS_SERIAL_OUT is a pull-down output and connected to RS2_TX_TTL at J2; both can be switched on and off by cPCI-commands.

The SENSOR_6V and SENSOR_0V contacts of the front connector are for the main sensor supply and 12V, 5V, 0V as well as SWITCH_0V offer further possibilities.

Temperature-sensor, voltage-check, front-panel-RGB-LED and nonvolatile calibration and configuration memory are available to cPCI. During factory-calibration gains of all channels are measured and stored in this memory.

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