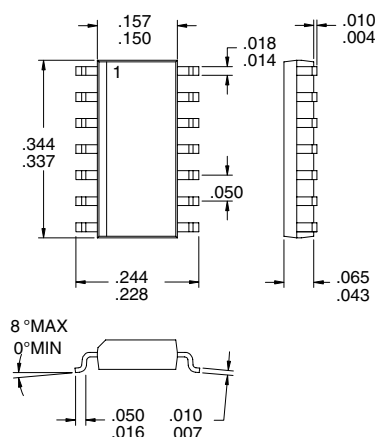


## Typical Applications

- Digital Communication Systems
- Spread Spectrum Communication Systems
- Driver for Higher Power Linear Applications
- Portable Battery Powered Equipment
- Commercial and Consumer Systems
- Base Station Equipment

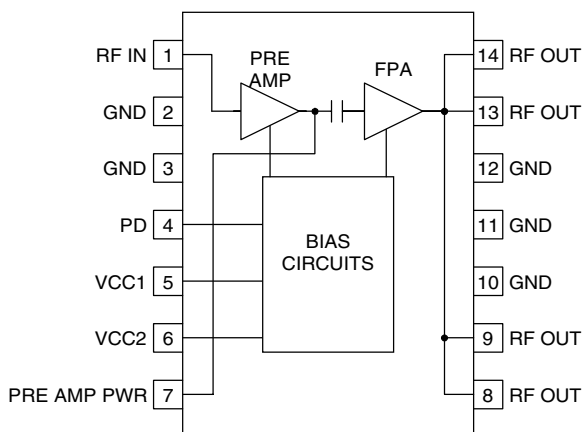
## Product Description

The RF2103P is a medium power linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final linear RF amplifier in UHF radio transmitters operating between 450MHz and 1000MHz. It may also be used as a driver amplifier in higher power applications. The device is self-contained with the exception of the output matching network, power supply feed line, and bypass capacitors, and it produces an output power level of 750mW (CW). The device can be used in 3 cell battery applications. The maximum CW output at 3.6V is 175mW. The unit has a total gain of 31dB, depending upon the output matching network.



## Optimum Technology Matching® Applied

- ☐ Si BJT      ☒ GaAs HBT      ☐ GaAs MESFET  
☐ Si Bi-CMOS      ☐ SiGe HBT      ☐ Si CMOS



### Functional Block Diagram

**Package Style: SOP-14**

## Features

- 450MHz to 1000MHz Operation
- Up to 750mW CW Output Power
- 31dB Small Signal Gain
- Single 2.7V to 7.5V Supply
- 47% Efficiency
- Digitally Controlled Power Down Mode

## Ordering Information

|              |                                  |
|--------------|----------------------------------|
| RF2103P      | Medium Power Linear Amplifier    |
| RF2103P PCBA | Fully Assembled Evaluation Board |

RF Micro Devices, Inc.  
7625 Thorndike Road  
Greensboro, NC 27409, USA

Tel (336) 664 1233  
Fax (336) 664 0454  
<http://www.rfmd.com>

### Absolute Maximum Ratings

| Parameter                             | Rating       | Unit            |
|---------------------------------------|--------------|-----------------|
| Supply Voltage                        | -0.5 to +7.5 | V <sub>DC</sub> |
| Power Down Voltage (V <sub>PD</sub> ) | -0.5 to +5   | V               |
| DC Supply Current                     | 350          | mA              |
| Input RF Power                        | +12          | dBm             |
| Output Load VSWR                      | 10:1         |                 |
| Operating Case Temperature            | -40 to +100  | °C              |
| Operating Ambient Temperature         | -40 to +85   | °C              |
| Storage Temperature                   | -40 to +150  | °C              |



**Caution!** ESD sensitive device.

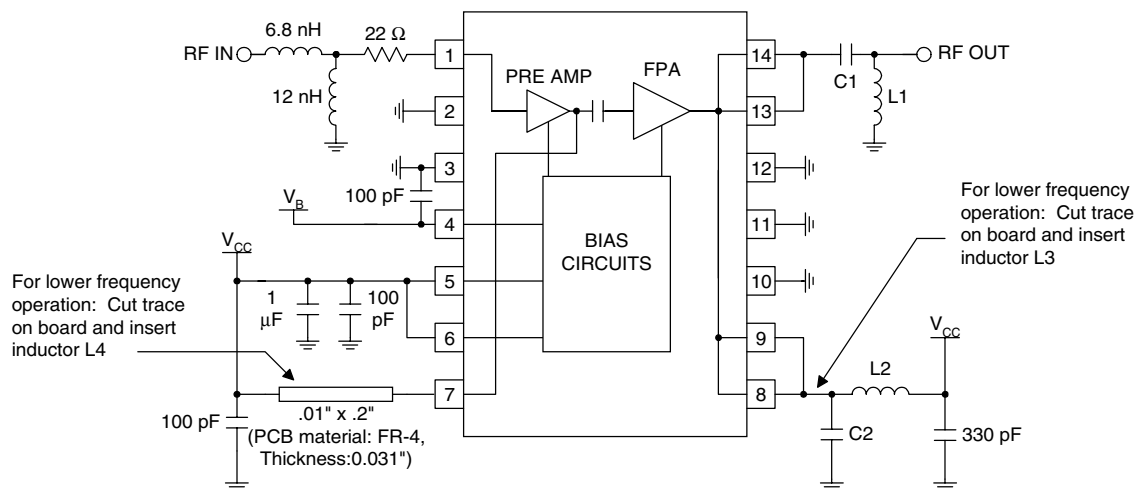
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

| Parameter                          | Specification |             |      | Unit   | Condition   |
|------------------------------------|---------------|-------------|------|--------|---|
|                                    | Min.          | Typ.        | Max. |        |   |
| <b>Overall</b>                     |               |             |      |        | T=25 °C, V <sub>CC</sub> =5.8V, V <sub>PD</sub> =5.0V, Z <sub>LOAD</sub> =18Ω, P <sub>IN</sub> =0dBm, Freq=915MHz |
| Frequency Range                    |               | 450 to 1000 |      | MHz    |   |
| Maximum Output Power               |               | +28.8       |      | dBm    | V <sub>CC</sub> =7.5V   |
| Maximum Output Power               |               | +26.5       |      | dBm    | V <sub>CC</sub> =5.8V   |
| Second Harmonic                    |               | -24         |      | dBc    | Without external second harmonic trap   |
| Third Harmonic                     |               | -30         |      | dBc    |   |
| Output Noise Power                 |               | <-125       |      | dBm/Hz |   |
| Input Impedance                    |               | 50          |      | Ω      | With external matching network; see application schematic   |
| Input VSWR                         |               | <2:1        |      |        | With external matching network; see application schematic   |
| Output Impedance                   |               | 18+j0       |      | Ω      | Load Impedance for Optimal Match  |
| <b>Nominal 5.8V Configuration</b>  |               |             |      |        | V <sub>CC</sub> =5.8V, V <sub>PD</sub> =4.0V, Z <sub>LOAD</sub> =18Ω, P <sub>IN</sub> =0dBm, Freq=830MHz          |
| Linear Power Gain                  | 24            | 31          |      | dB     |   |
| Saturated CW Output Power          |               | +26.5       |      | dBm    |   |
| IM <sub>3</sub>                    |               | -40         | -25  | dBc    | P <sub>OUT</sub> =+18.5dBm/tone   |
| IM <sub>5</sub>                    |               | -45         | -30  | dBc    | P <sub>OUT</sub> =+18.5dBm/tone   |
| Collector Current, I <sub>CC</sub> |               | 175         | 250  | mA     | Total of pins 7 and 8   |
| V <sub>PD</sub> Current            |               | <3.5        |      | mA     | Into pin 4  |
| CW Total Efficiency                |               | 47          |      | %      |   |
| Two Tone Total Efficiency          |               | 26          |      | %      | P <sub>OUT</sub> =+18.5dBm/tone   |
| <b>Power Supply</b>                |               |             |      |        |   |
| Power Supply Voltage               |               | 2.7 to 7.5  |      | V      |   |
| Power Supply Idle Current          |               | 45          | 80   | mA     |   |
| Total "OFF" Current Drain          |               | 1           | 10   | μA     | V <sub>PD</sub> <0.1V <sub>DC</sub>   |
| Turn-on Time                       |               | <100        |      | ns     | V <sub>PD</sub> =0 to V <sub>PD</sub> =+4V <sub>DC</sub>  |

| Pin | Function   | Description   | Interface Schematic |
|-----|------------|---|---------------------|
| 1   | RF IN      | RF input pin. There is an internal blocking capacitor between this pin and the preamp input, but not between the pin and an internal 2k $\Omega$ resistor to ground.  |                     |
| 2   | GND        | Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.   |                     |
| 3   | GND        | Same as pin 2.  |                     |
| 4   | PD         | Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at V <sub>CC</sub> (3V to 6.5V), the device will be in full power mode delivering maximum available gain and output power capability. This pin may also be used to perform some degree of gain control or power control when set to voltages between 0V and V <sub>CC</sub> . It is not optimized for this function so the transfer function is not linear over a wide range as with other devices specifically designed for analog gain control; however, it may be usable for coarse adjustment or in some closed loop AGC systems. This pin should not, in any circumstance, be higher in voltage than V <sub>CC</sub> . This pin should also have an external bypassing capacitor.  |                     |
| 5   | VCC1       | Positive supply for the active bias circuits. This pin can be externally combined with pin 6 (VCC2) and the pair bypassed with a single capacitor, placed as close as possible to the package. Additional bypassing of 1 $\mu$ F is also recommended, but proximity to the package is not as critical. In most applications, pins 5, 6, and 7 can share a single 1 $\mu$ F bypass capacitor.  |                     |
| 6   | VCC2       | Same as pin 5.  |                     |
| 7   | PREAMP PWR | Positive supply for the pre-amplifier. This is an unmatched transistor collector output. This pin should see an inductive path to AC ground (V <sub>CC</sub> with bypass capacitor). This inductance can be achieved with a short, thin microstrip line or with a low value chip inductor (approximately 1.8nH). At lower frequencies, the inductance value should be larger (longer microstrip line) and V <sub>CC</sub> should be bypassed with a larger bypass capacitor. This inductance forms a matching network with the internal series capacitor between the two amplifier stages, setting the amplifier's frequency of maximum gain. An additional 1 $\mu$ F bypass capacitor in parallel with the 100pF bypass capacitor is also recommended, but placement of this component is not as critical. In most applications, pins 5, 6, and 7 can share a single 1 $\mu$ F bypass capacitor. |                     |
| 8   | RF OUT     | Same as pin 14.   |                     |
| 9   | RF OUT     | Same as pin 14.   |                     |
| 10  | GND        | Same as pin 2.  |                     |
| 11  | GND        | Same as pin 2.  |                     |
| 12  | GND        | Same as pin 2.  |                     |
| 13  | RF OUT     | Same as pin 14.   |                     |

| Pin | Function | Description   | Interface Schematic |
|-----|----------|---|---------------------|
| 14  | RF OUT   | Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 8, 9, 13 and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through two of these four pins. Typically, pins 8 and 9 are connected to a network that provides the DC bias and also creates a second harmonic trap. For 915MHz operation, this harmonic trap network is simply a single 2pF capacitor from both pins to ground. This capacitor series resonates with internal bond wires at two times the operating frequency, effectively shorting out the second harmonic. Shorting out this harmonic serves to increase the amplifier's maximum output power and efficiency, as well as to lower the level of the second harmonic output. Typically, pins 13 and 14 are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output. Shunt protection diodes are included to clip peak voltage excursions above approximately 15V to prevent voltage breakdown in worst case conditions. |                     |

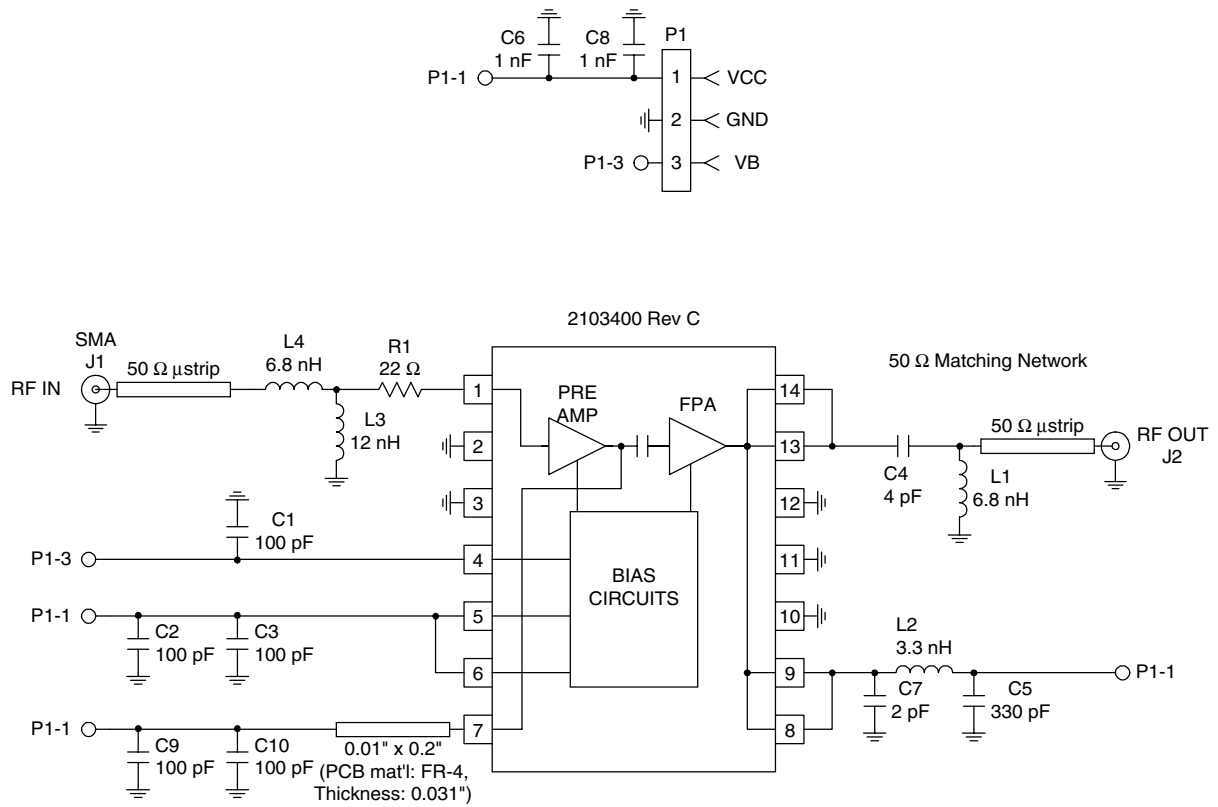
## Application Schematic



| FREQUENCY (MHz) | L1 (nH) | L2 (nH) | L3 (nH) | L4 (nH) | C1 (pF) | C2 (pF) |
|-----------------|---------|---------|---------|---------|---------|---------|
| 275             | 20      | 15      | 10      | 20      | 20      | 10      |
| 480             | 12      | 6.8     | 4.7     | 18      | 12      | 6.8     |
| 915             | 6.8     | 3.3     | —       | —       | 4       | 2       |

## Evaluation Board Schematic 915MHz Operation

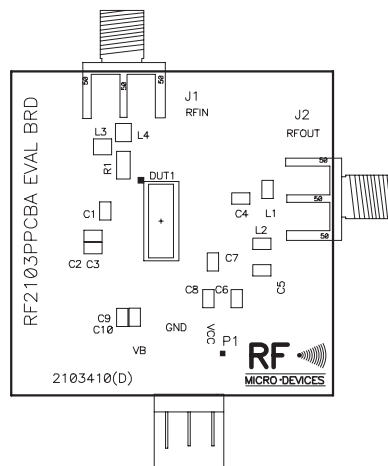
(Download [Bill of Materials](http://www.rfmd.com) from [www.rfmd.com](http://www.rfmd.com).)



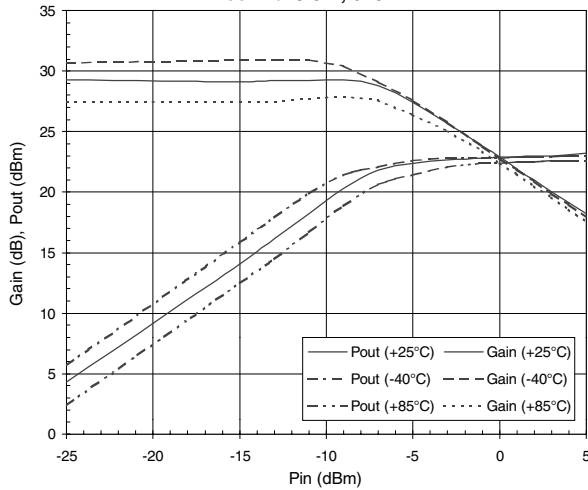
## Evaluation Board Layout 1.4" x 1.4"

2

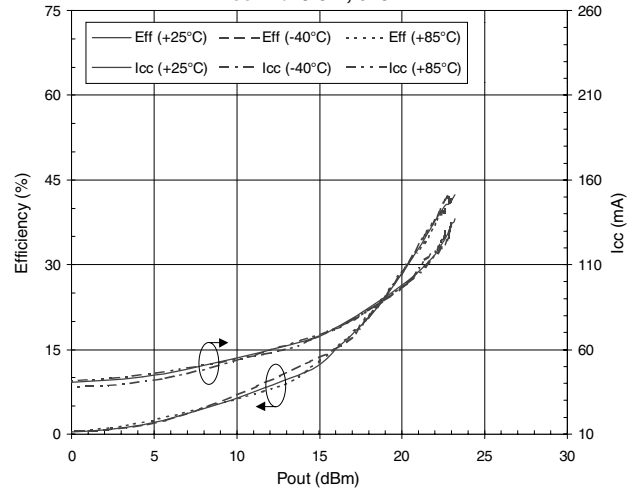
POWER AMPLIFIERS



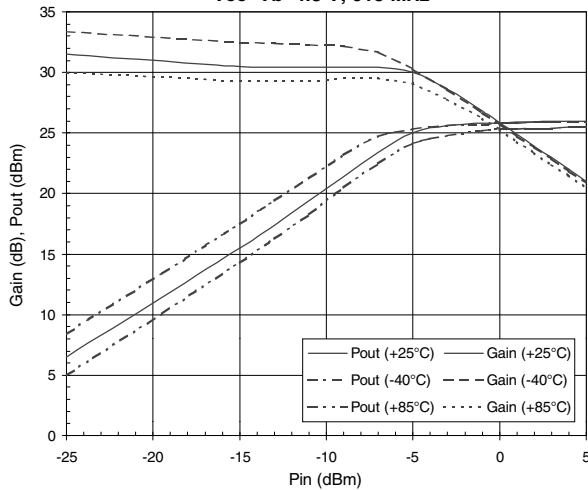
**Gain and Pout vs. Pin**  
**Vcc=Vb=3.6 V, 915 MHz**



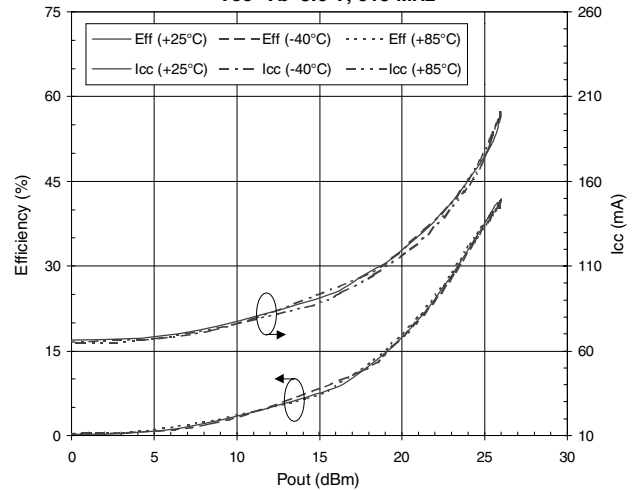
**Efficiency and Icc vs. Pout**  
**Vcc=Vb=3.6 V, 915 MHz**



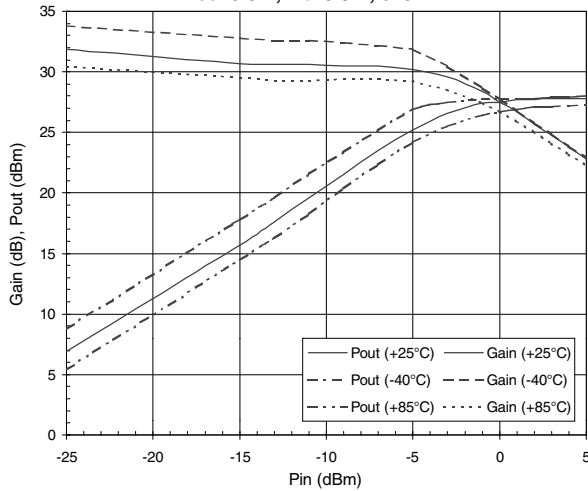
**Gain and Pout vs. Pin**  
**Vcc=Vb=4.8 V, 915 MHz**



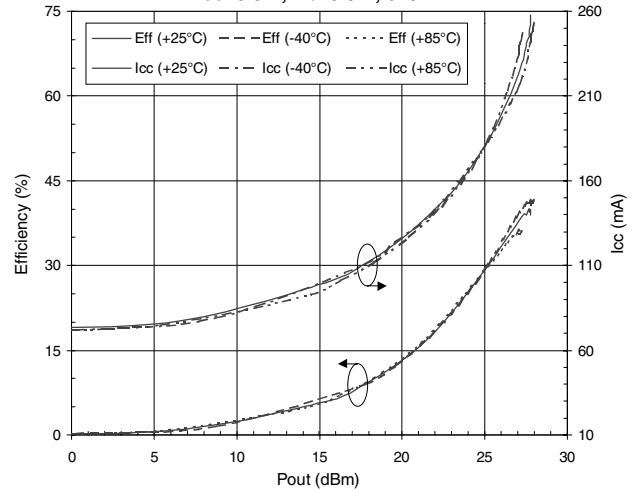
**Efficiency and Icc vs. Pout**  
**Vcc=Vb=3.6 V, 915 MHz**



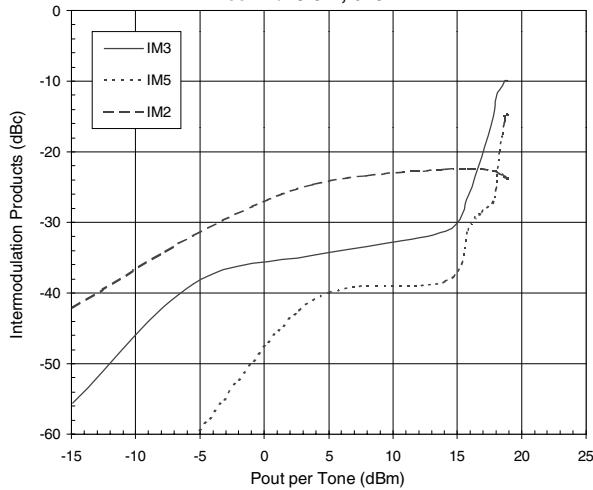
**Gain and Pout vs. Pin**  
**Vcc=6.0 V, Vb=5.0 V, 915 MHz**



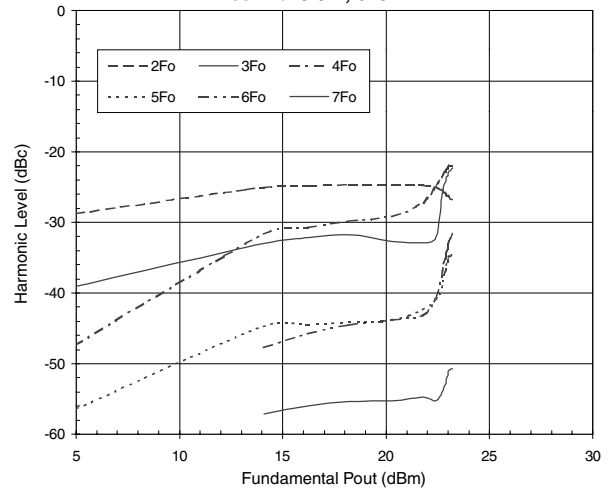
**Efficiency and Icc vs. Pout**  
**Vcc=6.0 V, Vb=5.0 V, 915 MHz**



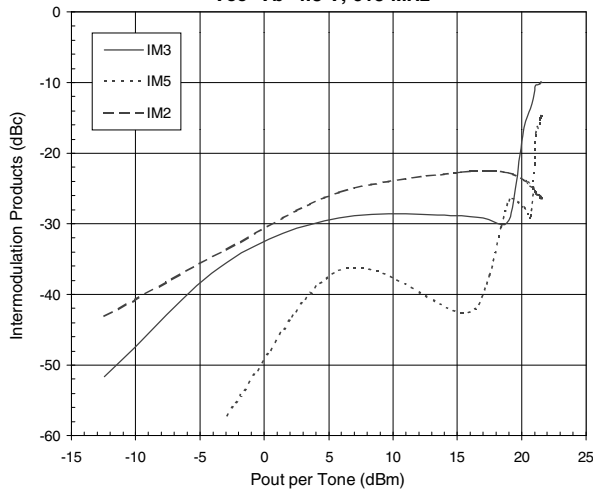
**IM3, IM5, and IM2 vs. Pout**  
Vcc=Vb=3.6 V, 915 MHz



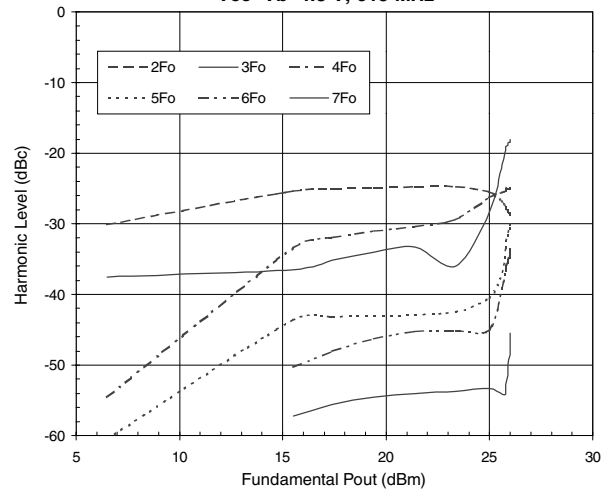
**Harmonics vs. Pout**  
Vcc=Vb=3.6 V, 915 MHz



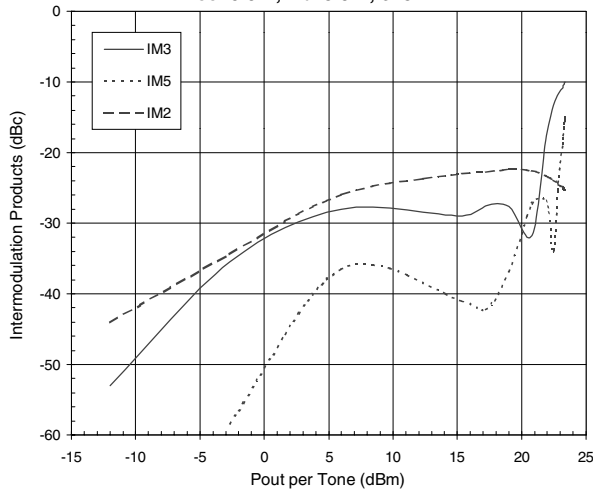
**IM3, IM5, and IM2 vs. Pout**  
Vcc=Vb=4.8 V, 915 MHz



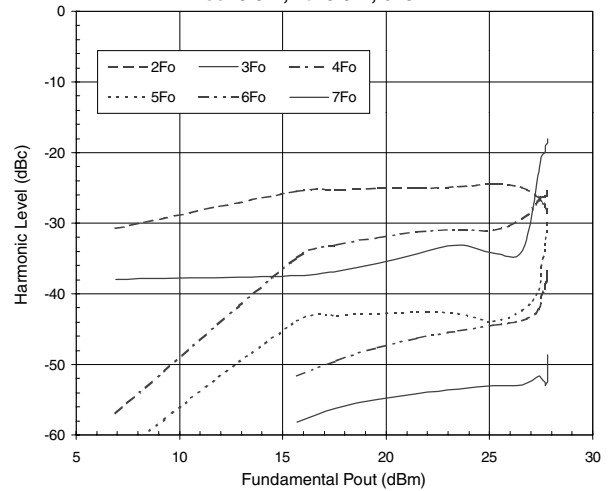
**Harmonics vs. Pout**  
Vcc=Vb=4.8 V, 915 MHz



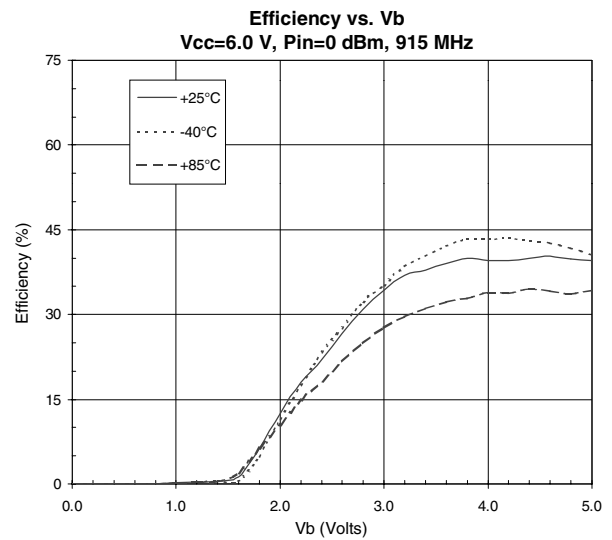
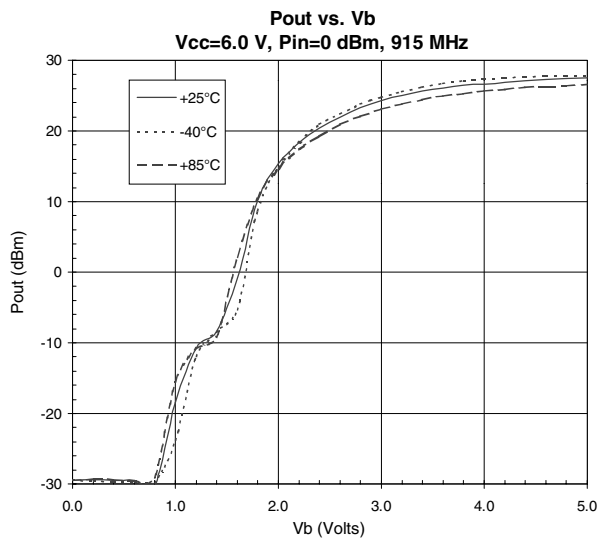
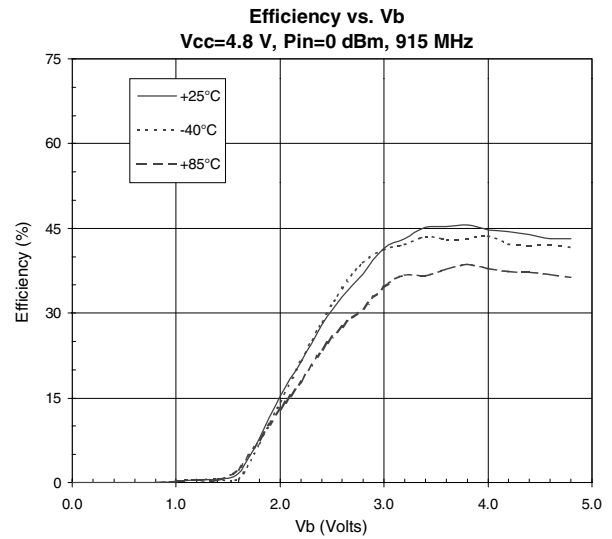
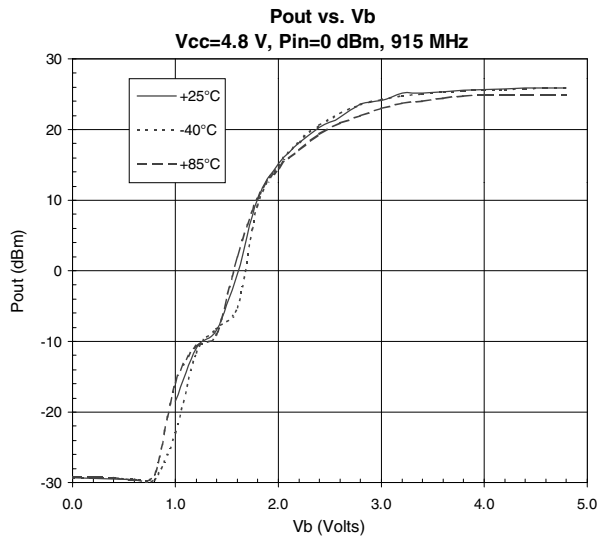
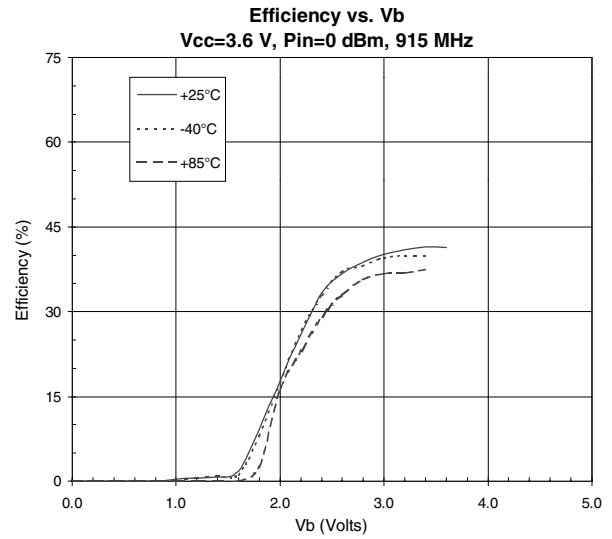
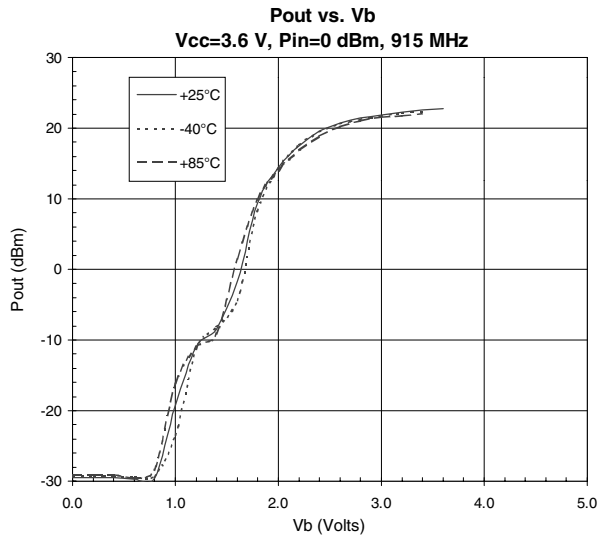
**IM3, IM5, and IM2 vs. Pout**  
Vcc=6.0 V, Vb=5.0 V, 915 MHz



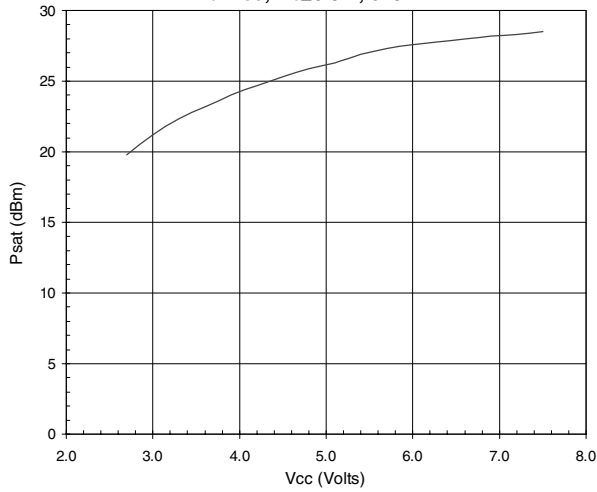
**Harmonics vs. Pout**  
Vcc=6.0 V, Vb=5.0 V, 915 MHz



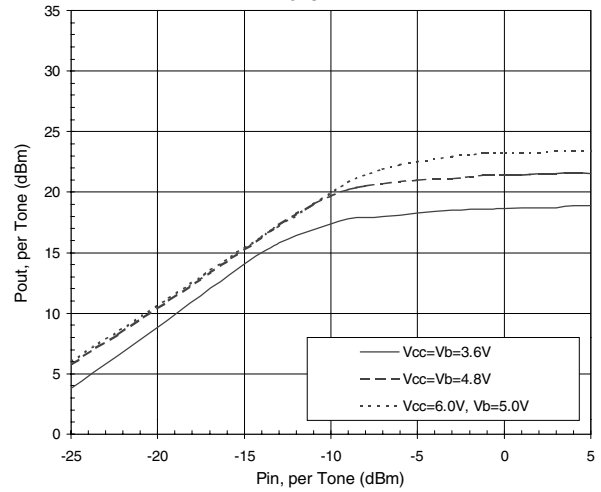




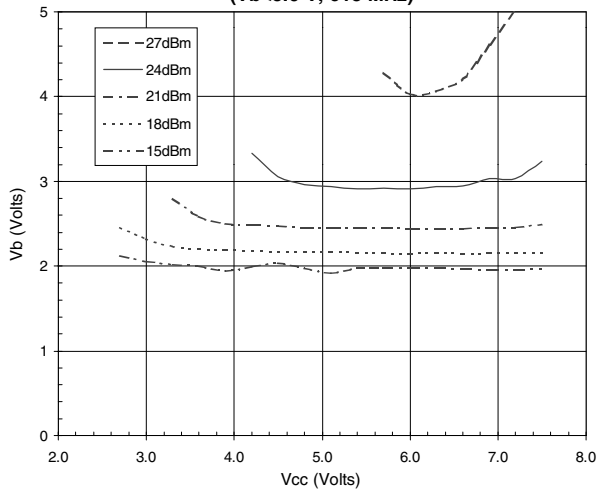
**Psat vs. Vcc**  
**Vb=Vcc; Vb≤5.0 V, 915 MHz**



**Two Tone Pout vs. Pin, 915 MHz**



**Vb Required to Achieve Specific Pout (Vb<5.0 V, 915 MHz)**



**Two Tone Efficiency and Icc vs. Pout, 915 MHz**

