RF2145

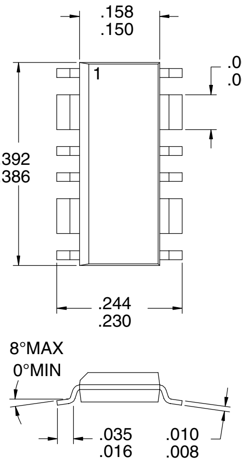
DCS1800/1900 POWER AMPLIFIER

Typical Applications

- 4.8V DCS1800/1900 Handsets
- 3V DECT Handsets and Base Stations
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

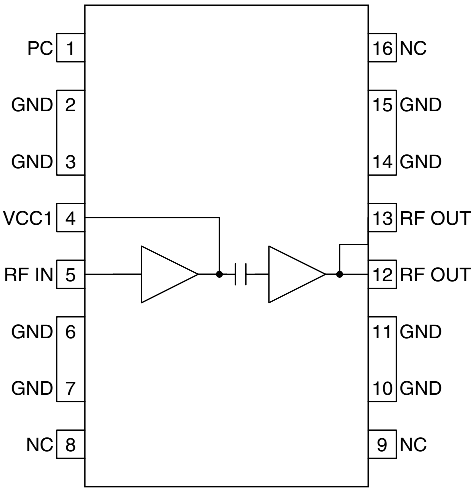
The RF2145 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in a 4-cell DCS1800 or DCS1900 handset. The device is packaged in a 16-lead plastic package with wide ground leads, and is self-contained with the exception of the output matching network and power supply feed line. Only a single positive voltage is required to operate with full power and efficiency, and on-board power control and power-down functions are provided.



Package Style: SOP-16 QBW1

Optimum Technology Matching® Applied

☐ Si BJT ☑ GaAs HBT ☐ GaAs MESFET
☐ Si Bi-CMOS ☐ SiGe HBT ☐ Si CMOS



Functional Block Diagram

Features

- Single 4.8V Power Supply
- +32dBm Output Power
- 28dB Small Signal Gain
- 55% Power Added Efficiency
- Power Control
- 1700MHz to 1900MHz Frequency Range

Ordering Information

RF2145	DCS1800/1900 Power Amplifier
RF2145 PCBA	Fully Assembled Evaluation Board

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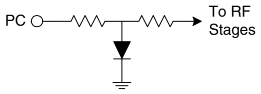
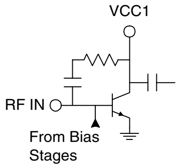
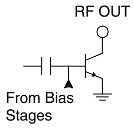
Absolute Maximum Ratings

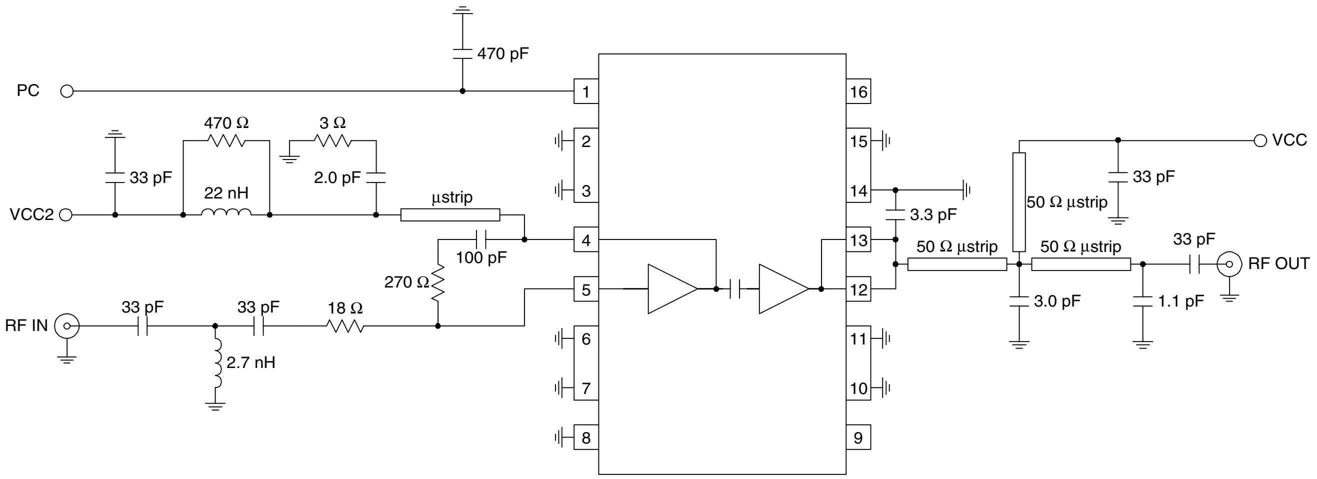
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +3.0	V
DC Supply Current	675	mA
Input RF Power	+12	dBm
Output Load VSWR	5:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.8V, V_{PC}=2.5V, P_{IN}=+8dBm, Freq=1750MHz
Operating Frequency Range		1710 to 1785 1850 to 1910		MHz	
Usable Frequency Range		1700 to 1990		MHz	
Maximum Output Power		+32		dBm	1/8 Duty cycle with 600µs pulse width
Total Efficiency		55		%	At maximum output power
Input Power for Max Output		+8		dBm	
Input Intermodulation Distortion		-57		dBc	Input signal consists of F_1 at 1785MHz at +8dBm, F_2 at 1765MHz at -42dBm. Output power at F_1 is set to +32.5dBm. Specified power level at 1805MHz relative to F_1. This refers to the amount of TX band noise which converts into the receive band.
		-48		dBc	Input signal consists of F_1 at 1785MHz at +8dBm, F_2 at 1765MHz at -32dBm. Output power at F_1 is set to +32.5dBm. Specified power level at 1805MHz relative to F_1. This refers to the amount of TX band noise which converts into the receive band.
Output Noise Power in Receive Band		-137		dBm/Hz	Any gain setting
Isolation		-25		dBm	In “OFF” state, P_{IN}=+8dBm
Second Harmonic		-48		dBc	
Third Harmonic		<-60		dBc	
Input Impedance		50		Ω	
Input VSWR			3.8:1		Worst-case across the band. Using evaluation board; can be different with other layouts
Output Load VSWR	3:1				Spurious<-60dBc
Power Control					
Power Control “ON”		2.5	3.0	V	Threshold voltage
Power Control “OFF”	0.2	0.5		V	Threshold voltage
Current into PC Input		15		mA	In “ON” state
			10	µA	In “OFF” state
Power Control Range	45			dB	
Turn On/Off TIme			100	ns	
Power Supply					
Power Supply Voltage		4.8		V	Specifications
	2.7		6.5	V	Operating limits
Power Supply Current		550		mA	DC Current at maximum output power
			10	µA	V_{PC}=0.5V

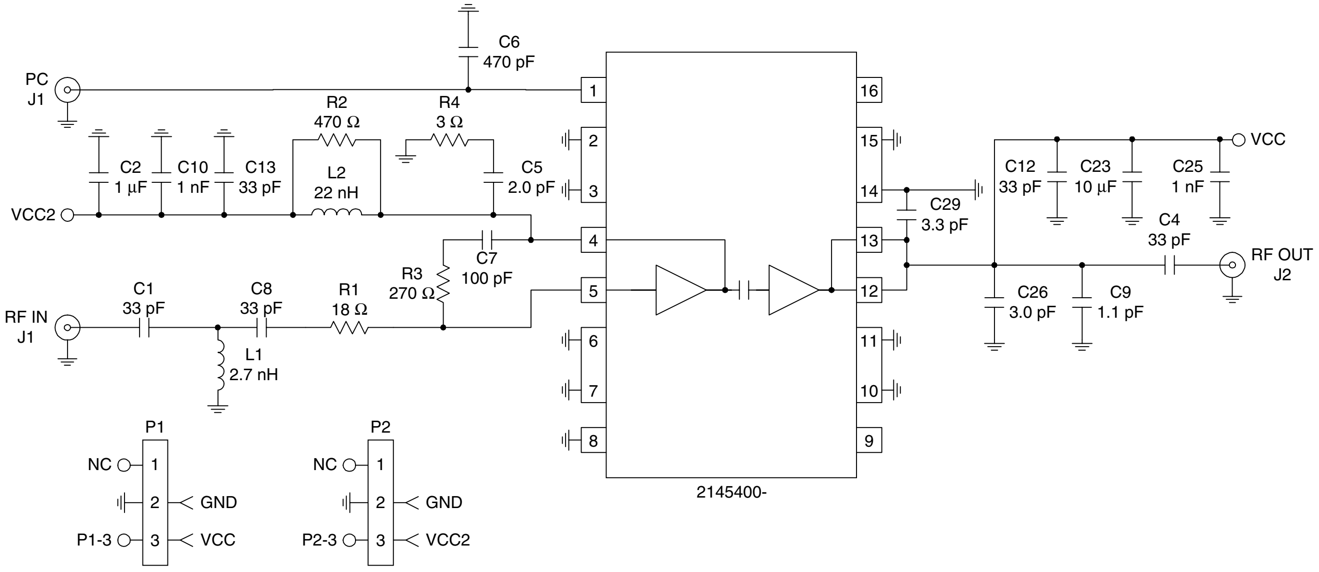
Pin	Function	Description	Interface Schematic
1	**PC**	Power control pin. This also provides power down when V_{PC} is less than +0.5V. Full power is achieved at 2.5V, and >45dB of gain control is obtainable over the full range. Approximately 15mA current is drawn into this pin at full power.	
2	**GND**	Ground connection. This pin should be connected to the ground plane through a short path and may be combined with the ground plane from Pins 3, 6, 7, 10, 11, 14, and 15. All four of these wide leads are tied together internally to provide a low-inductance and low thermal resistance path to external ground. Ground vias should be placed as close as possible to each ground lead.	
3	**GND**	Same as pin 2.	
4	**VCC1**	Power supply pin for the first stage. Also provides tuning for interstage match.	
5	**RF IN**	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path.	See pin 4 schematic.
6	**GND**	Same as pin 2.	
7	**GND**	Same as pin 2.	
8	**NC**	No connection.	
9	**NC**	No connection.	
10	**GND**	Same as pin 2.	
11	**GND**	Same as pin 2.	
12	**RF OUT**	RF output pin. Bias is also fed to the final stage through this wide lead. External matching is most easily achieved with a series transmission line and shunt capacitors, as shown in the application schematic.	
13	**RF OUT**	Same as pin 12.	
14	**GND**	Same as pin 2.	
15	**GND**	Same as pin 2.	
16	**NC**	No connection.	

Application Schematic DCS 1800



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 2”