BROADBAND LINEAR VARIABLE GAIN AMPLIFIER

Typical Applications

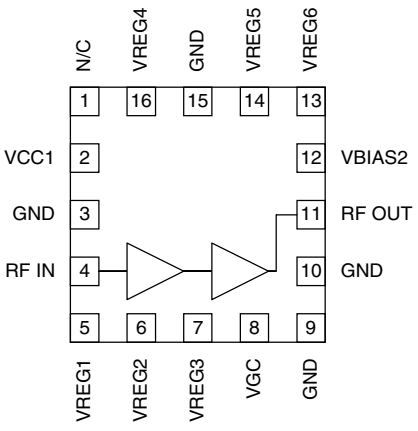
- CDMA Cellular/PCS and JCDMA Systems
- TDMA Cellular/PCS Systems
- Wideband CDMA Systems
- Wireless Local Loop Systems
- GSM Systems
- PDC Systems (950MHz and 1450MHz)

Product Description

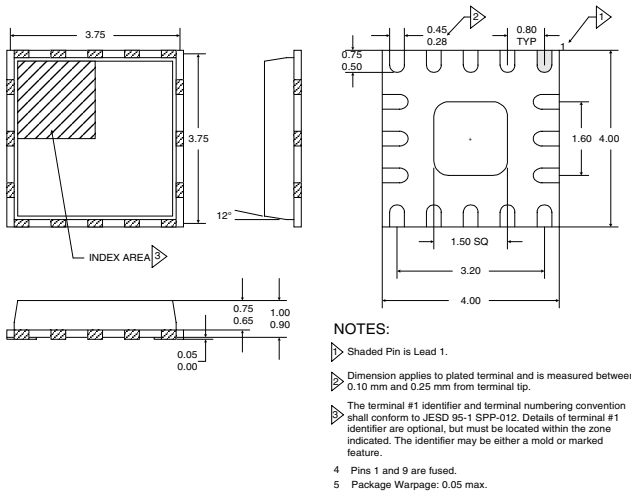
The RF2303 is a broadband linear variable gain amplifier that was designed specifically for digital communications systems that require linear amplification over a wide gain control range. It is suitable for use in WCDMA, as well as CDMA or TDMA systems in the cellular or PCS band, in DAMPS systems, and in PDC systems. Operating supply voltage ranges from 3V to 6V. The device operates over a large frequency band, from 100MHz to 2000MHz, and is tuned to a specific frequency band with an output bias feed inductor and blocking capacitor. Bias optimization may be achieved by adjusting the voltage to pin 5 (VREG). The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process and is featured in a 4mmx4mm leadless plastic MLF16 package.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: MLF16

Features

- 58dB Linear Gain Control range
- Single 3V to 6V Supply
- 25dB Max Gain at 1900MHz
- 4dB Min Noise Figure at 1900MHz

Ordering Information

RF2303	Broadband Linear Variable Gain Amplifier
RF2303 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

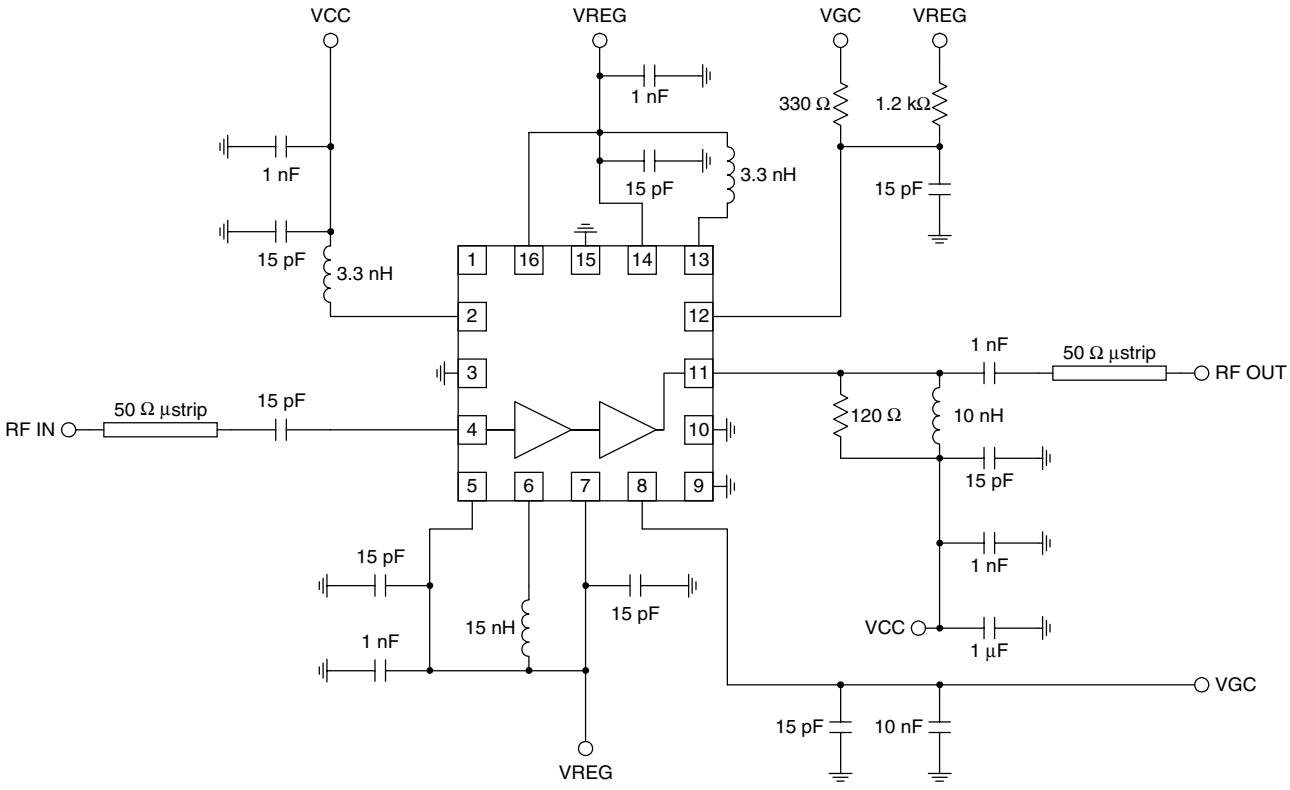
Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Power Down Voltage	0 to +3.1	V_{DC}
Gain Control Voltage	0 to +3.1	V_{DC}
DC Current	100	mA
Output Load VSWR	12:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=3.4V, V_{REG}=2.8V, V_{GC}=2.0V, T=25°C
RF Frequency Range	100		2000	MHz	
Small Signal Maximum Gain		23		dB	Freq=1900MHz
Small Signal Minimum Gain		-35		dB	Freq=1900MHz
Minimum Noise Figure		4			Freq=1900MHz
Linear Gain Control Range		50		dB	V_{GC}=0.5V to 2.0V
Gain Control Slope		TBD		V/V	Slope=ΔOutput peak voltage/ΔV_{GC}
Output P_{1dB}		16		dBm	Freq=1900 MHz, V_{CC}=3.4V at max gain
Input P_{1dB}		TBD		dBm	Freq=1900MHz; over entire V_{GC} range
Input VSWR		1.8:1	3:1		In 50Ω system; over entire V_{GC} range
Output VSWR		2.5:1			In 50Ω system
Power Supply					T=25°C
Supply Voltage	3		6	V	
Power Down Voltage High	2.7		2.9	V	Specifications
Power Down Voltage Low			1.0		
DC Current Consumption		25		mA	V_{CC}=3.4V, V_{REG}=2.8V, V_{GC}=2.0V
V_{REG} Current		TBD		µA	V_{REG}=2.8V
V_{GC} Current		15	60	µA	V_{GC}=2.0V
Power Down Current			10	µA	V_{REG}<1V, V_{GC}<1V
Turn On/Off Time			100	nS	

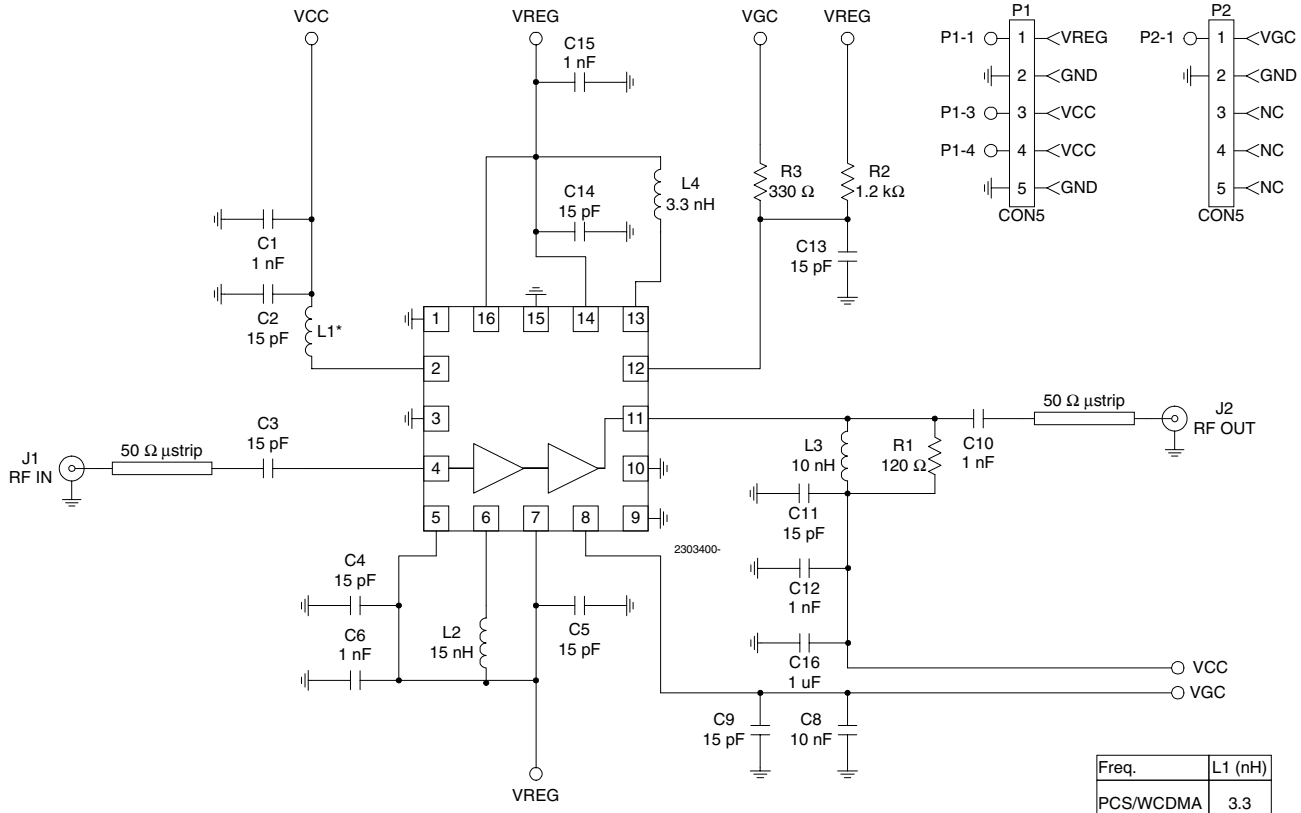
Pin	Function	Description	Interface Schematic
1	N/C	Not connected.	
2	VCC1	Power supply. This pin is connected to a battery or regulated supply. A series inductor and bypass capacitor should be placed as close to the part as possible. See application schematic for recommended component values.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	RF IN	RF input pin. There is an internal blocking capacitor for this pin.	
5	VREG1	Power down pin. This pin provides bias for the amplifier. To turn the amplifier on, this pin should be at 2.8V. Reducing this voltage below 0.5V ensures that the amplifier will draw less than 10μA current from the supply. Additionally, bias current can be optimized for lower output power by adjusting this voltage over a 2.7V to 2.9V range from a regulated supply.	
6	VREG2	Power down/bias pin. An inductor should be placed in series with this pin. See application schematic for recommended inductor value.	
7	VREG3	Same as pin 5.	
8	VGC	Analog gain control pin. This pin controls the gain of the IC. Minimum gain occurs at V_{GC}<1V and maximum gain is achieved with V_{GC}=2.2V. Greater than 50dB of linear gain control with no variation of input P_{1dB} is available, and additional attenuation is possible with V_{GC}<1V with input P_{1dB} variation. Bypass this pin near the device.	
9	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
10	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
11	RF OUT	RF output and bias pin. This pin is DC coupled and requires VCC through a bias inductor sized accordingly to provide a high pass transformation with a series capacitor.	
12	VBIAS2	Bias pin. Refer to application schematic for recommended biasing scheme.	
13	VREG6	Power down/bias pin. An inductor should be placed in series with this pin. See application schematic for recommended inductor value.	
14	VREG5	Same as pin 5.	
15	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
16	VREG4	Same as pin 5.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

PCS Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Freq.	L1 (nH)
PCS/WCDMA	3.3
Cellular	47

Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4