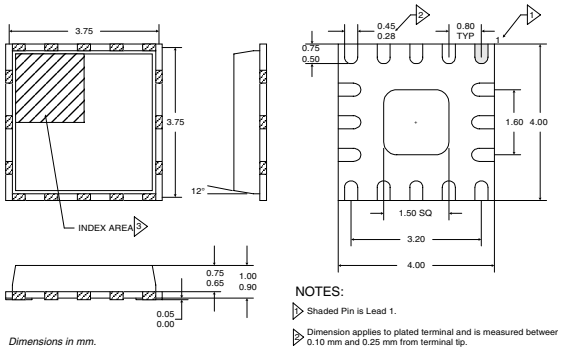
3V PCS CDMA SPLIT BAND PA DRIVER

Typical Applications

- CDMA PCS Systems
- TDMA PCS Systems
- GSM Systems
- Wireless Local Loop Systems
- Wideband CDMA Systems

Product Description

The RF2351 is a broadband linear gain amplifier that was designed specifically for digital communications systems. It is suitable for use in CDMA or TDMA systems in the PCS band. Operating supply voltage ranges from 3V to 6V. Bias optimization may be achieved by adjusting the power down voltage. The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process and is featured in an MLF16 package.



Dimensions in mm.

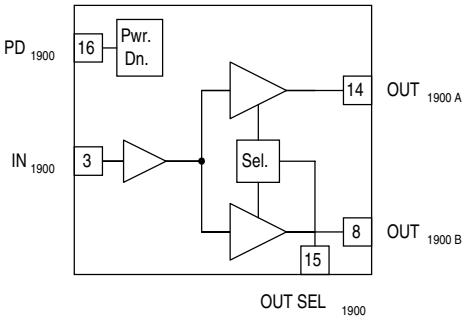
NOTES:

2. Shaded Pin is Lead 1.
3. Dimension applies to plated terminal and is measured betweer 0.10 mm and 0.25 mm from terminal tip.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MLF16



Functional Block Diagram

Features

- +16dBm OP1dB at 3.5V
- Single 3V to 6V Supply
- 21dB Gain
- 2.5dB Noise Figure
- Band Selection

Ordering Information

RF2351	3V PCS CDMA Split Band PA Driver
RF2351 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

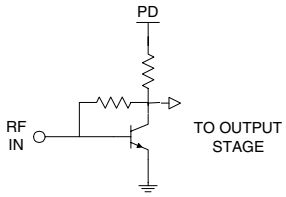
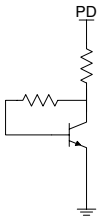
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

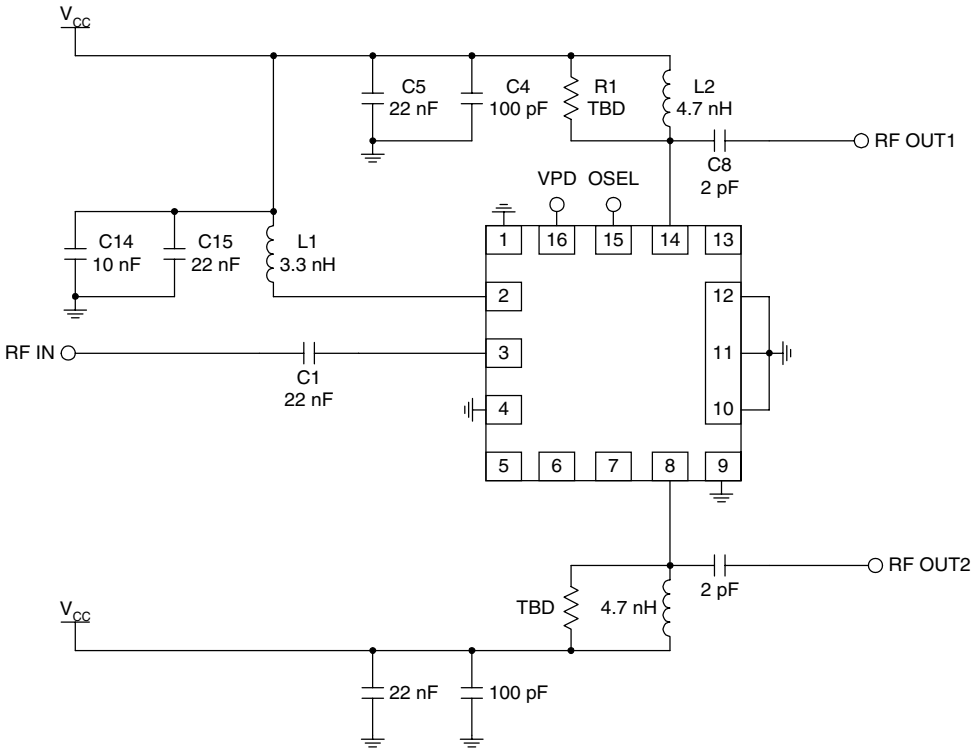
Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Power Down Voltage	0 to +3.1	V_{DC}
DC Current	100	mA
Output Load VSWR	12:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=3.5, T=25°C
RF Frequency Range		1710 to 1910		MHz	
Small Signal Gain	18	21	24	dB	Freq=1880MHz, V_{CC} = 3.5V, V_{PD} = 2.8V
Noise Figure		2.5		dB	Freq=1880MHz
Output P_{1dB}	+16			dBm	Freq=1880 MHz, V_{CC}=3.5V
Isolation Between Outputs		30		dB	
Input VSWR		1.5:1			In 50Ω system
Output VSWR		1.5:1			In 50Ω system
Adjacent Channel Power Rejection @ 1.25 MHz	-56	-60		dBc	IS-95A CDMA, P_{OUT}=+10dBm
Power Supply					T=25°C
Supply Voltage	3	3.5	6	V	
Power Down Voltage High	2.7	2.8	2.9	V	
Power Down Voltage Low			1.0		
Output Select Voltage High		2	3.5		
Output Select Voltage Low		0	0.4		
DC Current Consumption	30	48	55	mA	V_{CC}=3.5V, V_{PD}=2.8V
V_{PD} Current		8		mA	V_{PD}=2.8V
Power Down Current			10	µA	V_{PD}<1V
Turn On/Off Time			100	nS	

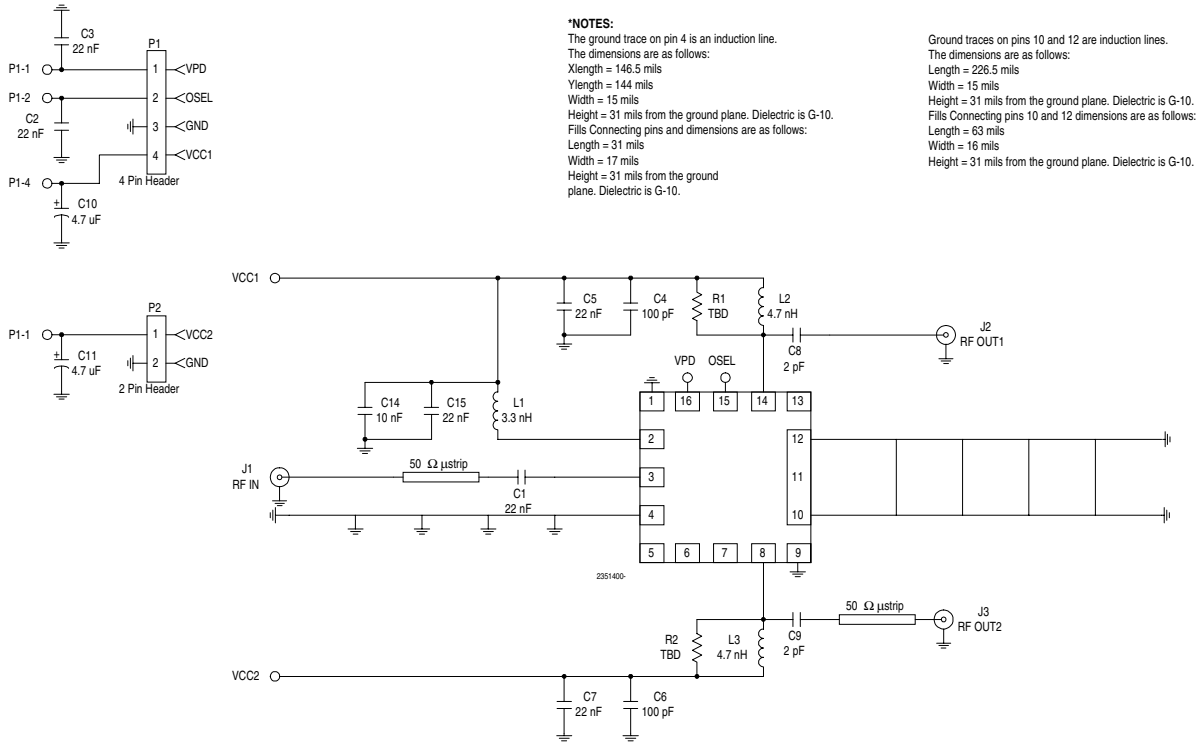
Pin	Function	Description	Interface Schematic
1	GND3	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	VCC1	Preamplifier output. This pin must be biased to V_{CC} through a matching inductor. Refer to application schematic.	
3	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 1880MHz.	
4	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	NC	No connection. This pin is typically left unconnected or grounded.	
6	NC	No connection. This pin is typically left unconnected or grounded.	
7	NC	No connection. This pin is typically left unconnected or grounded.	
8	RF OUT2	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 7 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
9	GND3	See pin 1.	
10	GND3	See pin 1.	
11	GND3	See pin 1.	
12	GND3	See pin 1.	
13	NC	No connection. This pin is typically left unconnected or grounded.	
14	RF OUT1	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 7 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
15	OSEL	2V to 3.5V range selects RF OUT2; 0V to 0.4V range selects RF OUT1.	
16	VPD	Power Down for the IC. $V_{PD} = 2.8V \pm 0.1V$ turns on the Part. $V_{PD} < 0.9V$ turns off the Part. External RF bypassing is required. Nominal current required for $V_{PD} = 2.8V$ is 8.5 mA typical.	
Pkg Base			

Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



***NOTES:**

The ground trace on pin 4 is an induction line.
The dimensions are as follows:
Xlength = 146.5 mils
Ylength = 144 mils
Width = 15 mils
Height = 31 mils from the ground plane. Dielectric is G-10.
Fills Connecting pins and dimensions are as follows:
Length = 31 mils
Width = 17 mils
Height = 31 mils from the ground plane. Dielectric is G-10.

Ground traces on pins 10 and 12 are induction lines.
The dimensions are as follows:
Length = 226.5 mils
Width = 15 mils
Height = 31 mils from the ground plane. Dielectric is G-10.
Fills Connecting pins 10 and 12 dimensions are as follows:
Length = 63 mils
Width = 16 mils
Height = 31 mils from the ground plane. Dielectric is G-10.

Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.031”, Board Material FR-4