

Preliminary

RF2363

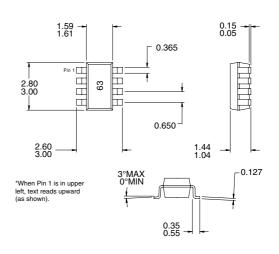
DUAL-BAND 3V LOW NOISE AMPLIFIER

Typical Applications

- GSM/DCS Dual-Band Handsets
- Cellular/PCS Dual-Band Handsets
- General Purpose Amplification
- Commercial and Consumer Systems

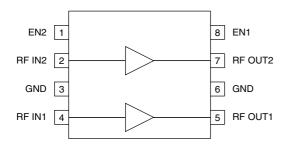
Product Description

The RF2363 is a dual-band Low Noise Amplifier designed for use as a front-end for 950MHz GSM/1850MHz DCS applications and may be used for dual-band cellular/PCS applications. The 900MHz LNA is a single-stage amplifier; the 1900MHz LNA is a 2-stage amplifier. The part may also be tuned for applications in other frequency bands. The device has an excellent combination of low noise figure and high linearity at a very low supply current. It is packaged in a very small industry standard SOT23 8-lead plastic package.



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Functional Block Diagram

Features

· Low Noise and High Intercept Point

Package Style: SOT23-8

- 18dB Gain at 900MHz
- 21dB Gain at 1900MHz
- Low Supply Current
- Single 2.5 V to 5.0 V Power Supply
- Very Small SOT23-8 Plastic Package

Ordering Information

RF2363 Dual-Band 3V Low Noise Amplifier RF2363 PCBA Fully Assembled Evaluation Board

RF Micro Devices, Inc. 7625 Thorndike Road Greensboro, NC 27409, USA Tel (336) 664 1233 Fax (336) 664 0454 http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



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Parameter		Specification			Condition	
Parameter	Min.	Тур.	Max.	Unit	Condition	
Overall						
RF Frequency Range		800 to 1000		MHz		
		1800 to 2000		MHz		
950MHz Performance					T=25°C, RF=950MHz, V _{CC} =2.8V,	
					EN1=2.8V, EN2=0V	
Gain	16	18	20	dB		
Isolation		16		dB	EN1=0V	
Gain Step		34		dB	Gain - Isolation	
Noise Figure		1.3		dB		
Output IP3	+18	+24		dBm		
Input P1dB		-10		dBm		
Reverse Isolation		20		dB		
Input VSWR		1.8:1	2:1		No external matching	
Output VSWR		1.8:1	2:1		With external match as per GSM/DCS Appli-	
					cation Schematic	
1850MHz Performance					T=25°C, RF=1850MHz, V _{CC} =2.8V,	
					EN2=2.8V, EN1=0V	
Gain	20	21.5	24	dB		
Isolation		10		dB	EN2=0V	
Gain Step		31.5		dB	Gain - Isolation	
Noise Figure		1.4		dB		
Output IP3	+17	+22		dBm		
Input P1dB		-12		dBm		
Reverse Isolation		30		dB		
Input VSWR		1.7:1	2:1		No external matching	
Output VSWR		1.7:1	2:1		With external match as per GSM/DCS Application Schematic	
LNA Select						
"Enable" Voltage		V_{CC}		V		
"Disable" Voltage		0		V		
Power Supply					T=25°C	
Voltage		2.8		V	Specifications	
-		2.5 to 5.0		V	Operating limits	
Current Consumption		5		mA	900 MHz LNA Enabled, 1900 MHz LNA Disabled; total DC current	
		7.5		mA	1900MHz LNA Enabled, 900MHz LNA Disabled; total DC current	
			1	μΑ	EN1=EN2=0V	

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Pin	Function	Description	Interface Schematic
1	EN2	Enable pin for ~1900MHz LNA. A voltage equal to the supply voltage LNA. This pin should be disabled (0V) when the ~900MHz LNA is in use. See package drawing for description of pin orientation.	
2	RF IN2	RF input pin for ~1900MHz. This pin is matched to approximately 50Ω at DCS/PCS frequencies. An external AC coupling capacitor is required at this pin.	RF IN2 O RF OUT2
3	GND	Ground connection. NOTE: Ground traces on pins 3 and 6 are equivalent to a small amount of inductance (~0.75nH). The dimensions of these lines are as follows. Pin 3: L=56mils, W=15mils, H=30mils Pin 6: L=56mils, W=15mils, H=30mils Dielectric is FR-4.	LNA1 LNA2 Pin 6 Pin 3
4	RF IN1	RF input pin for ~900MHz. This pin is matched to approximately 50Ω at GSM/Cellular frequencies. An external AC coupling capacitor is required at this pin.	RF IN1 O RF OUT2 To Bias = Circuits
5	RF OUT1	RF output pin for ~900MHz LNA. This pin is an open-collector output. It must be biased to either V_{CC} or pin 8 through a choke or matching inductor. It is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 4.
6	GND	See pin 3.	See pin 3.
7	RF OUT2	RF output pin for ~1900MHz LNA. This pin is an open-collector output. It must be biased to either V_{CC} or pin 8 through a choke or matching inductor. It is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 2.
8	EN1	Enable pin for $\sim 900\text{MHz}$ LNA. A voltage equal to the supply voltage LNA. This pin should be disabled (0V) when the $\sim 1900\text{MHz}$ LNA is in use.	

RF2363 Theory of Operation and Application Information

The RF2363 contains two independent low noise amplifiers which have been optimized for dual-band applications in the GSM (905MHz to 960MHz) and DCS (1805MHz to 1880MHz) frequency bands. Fabricated using heterojunction bipolar transistor (HBT) technology, the RF2363 delivers high linear gain at a very low noise figure and low power consumption. Internal temperature compensation keeps the gain tightly controlled over temperature extremes (typically less than 1dB of gain variation from -40°C to +85°C at 2.8V). A 50 Ω input impedance allows the part to be connected to standard receiver front end filters without additional matching components.

MODE CONTROL

The RF2363 incorporates two enable pins (EN1 and EN2) for biasing the desired LNA according to the table below.

EN1	EN2	Mode
GND	GND	Power Down
GND	VCC	1900MHz LNA On
VCC	GND	900MHz LNA On

900 MHz LNA

The 900MHz LNA is a single-stage, common emitter amplifier. Since the input pin contains a DC bias, an AC coupling capacitor is required at this pin. An external bias inductor from the output pin (RF OUT1) to VCC provides DC biasing for the amplifier transistor and assists in matching the output impedance to the next receiver stage. A capacitor having a good RF bypass characteristic at the frequency of operation should be placed as close as possible to the supply voltage side of the bias inductor; a low frequency bypass capacitor should also be included. The EN1 pin supplies VCC to the bias circuits of the LNA and should also be effectively bypassed with both low and high frequency capacitors.

1900MHz LNA

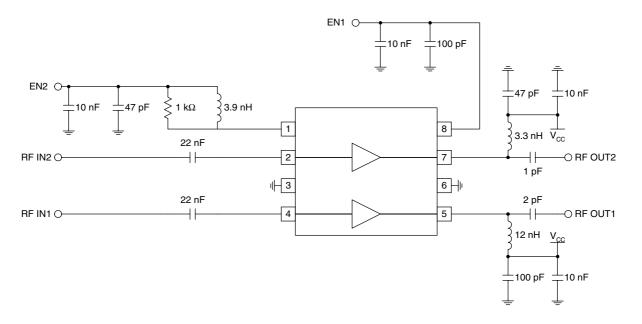
The 1900MHz LNA is implemented by two common emitter stages in cascade. The first stage is biased through an external inductor at the EN2 pin. This inductor also acts as an interstage match; a resistor in parallel with the inductor is recommended to 'de-Q' the inductor, thus providing a broader band interstage match. An external bias inductor from the output pin (RF OUT2) to VCC provides DC biasing for the second stage transistor and assists in matching the output impedance to the next receiver stage. Low and high frequency bypass capacitors should be used on the supply side of both the EN2 and RF OUT2 bias inductors. An AC coupling capacitor is required at the RF IN2 pin.

LAYOUT CONSIDERATIONS

To provide optimal balance of gain and linearity, a small amount of inductance is required in the ground traces of the PCB. The recommended inductance is between 0.5 and 1.0nH, with 0.75nH used on the Evaluation Board. Depending on the application, more gain with less linearity or more linearity with less gain may be desired. Appropriate adjustment of the ground inductance can accomplish these objectives. Minimizing the ground inductance will maximize the gain at the expense of linearity while increasing the ground inductance will increase the linearity at the expense of gain. It is important to remember that the Pin 3 ground inductance affects the performance of both LNAs, while the Pin 6 ground inductance affects only the 1900MHz LNA.

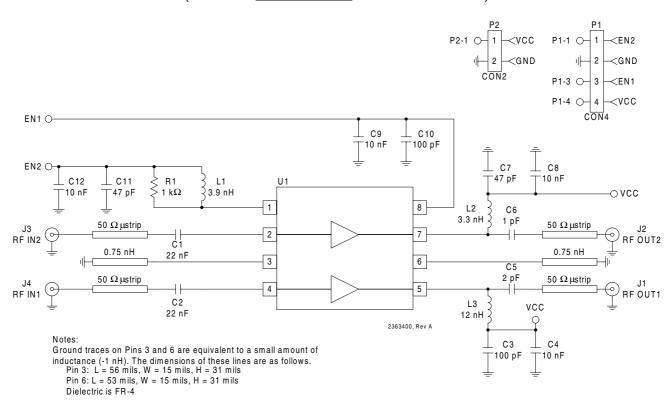
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Application Schematic (GSM/DCS)



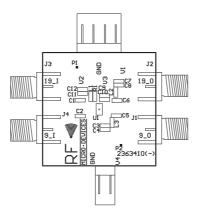
Evaluation Board Schematic

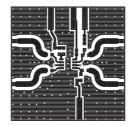
(Download Bill of Materials from www.rfmd.com.)



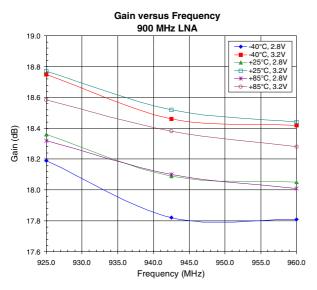
Evaluation Board Layout Board Size 1.0" x 1.0"

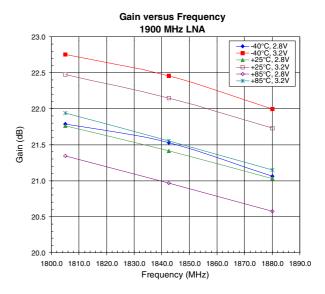
Board Thickness 0.031", Board Material FR-4

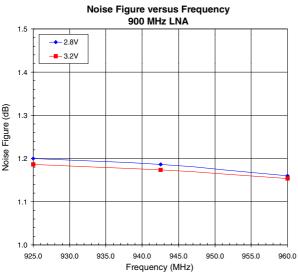


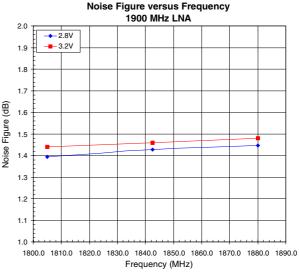


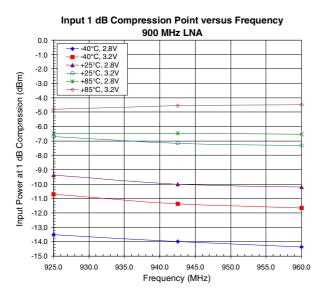
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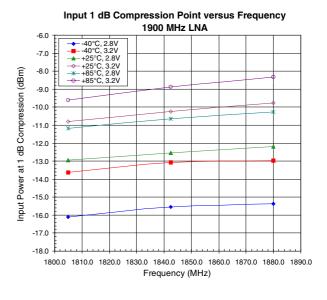


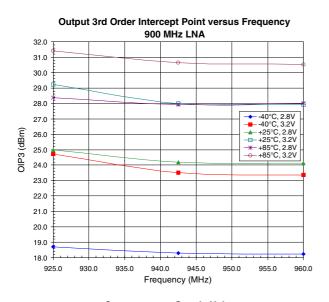


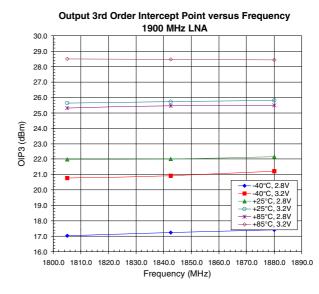


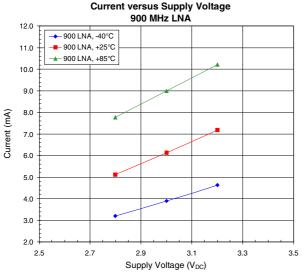


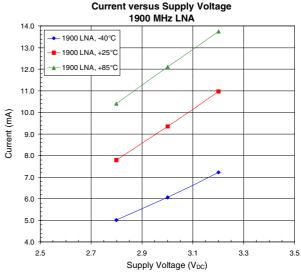




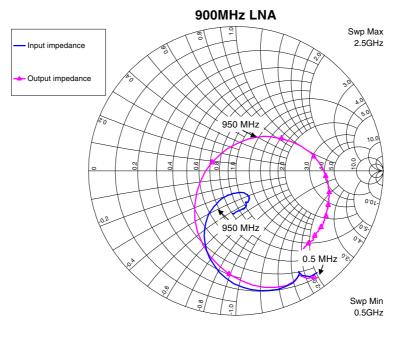


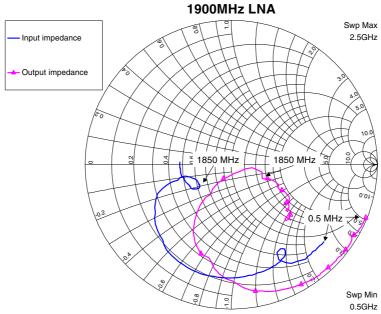






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