Typical Applications

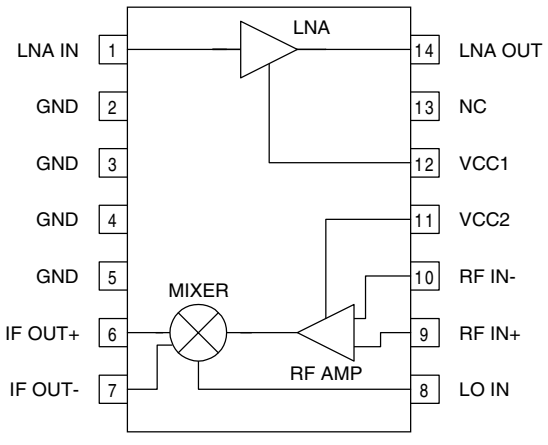
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

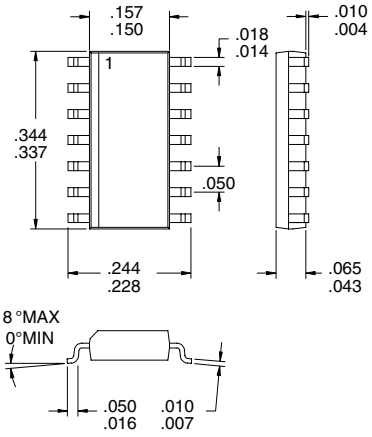
The RF2411 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, and a balanced mixer which can drive a single-ended or balanced load. The output of the LNA is made available as a pin to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA output is buffered to permit a wide range of choices for the interstage filter without altering the VSWR or noise figure at the LNA input and to provide high isolation from the LO to the input port. The LNA section may be disabled to conserve power.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Single 3V to 6.5V Power Supply
- 500MHz to 1900MHz Operation
- 25dB Small Signal Gain
- 2.5dB Cascaded Noise Figure
- 8.5mA DC Current Consumption
- -8dBm Input IP_3

Ordering Information

RF2411	Low Noise Amplifier/Mixer
RF2411 PCBA-L	Fully Assembled Evaluation Board (850MHz)
RF2411 PCBA-H	Fully Assembled Evaluation Board (1800MHz)

RF Micro Devices, Inc.
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Greensboro, NC 27409, USA

Tel (336) 664 1233
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http://www.rfmd.com

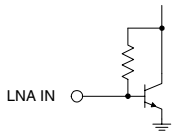
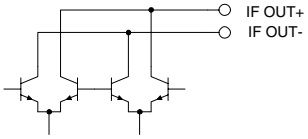
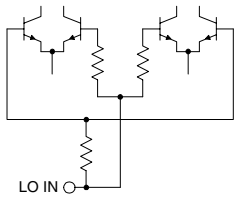
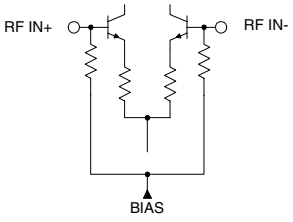
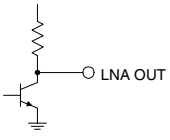
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

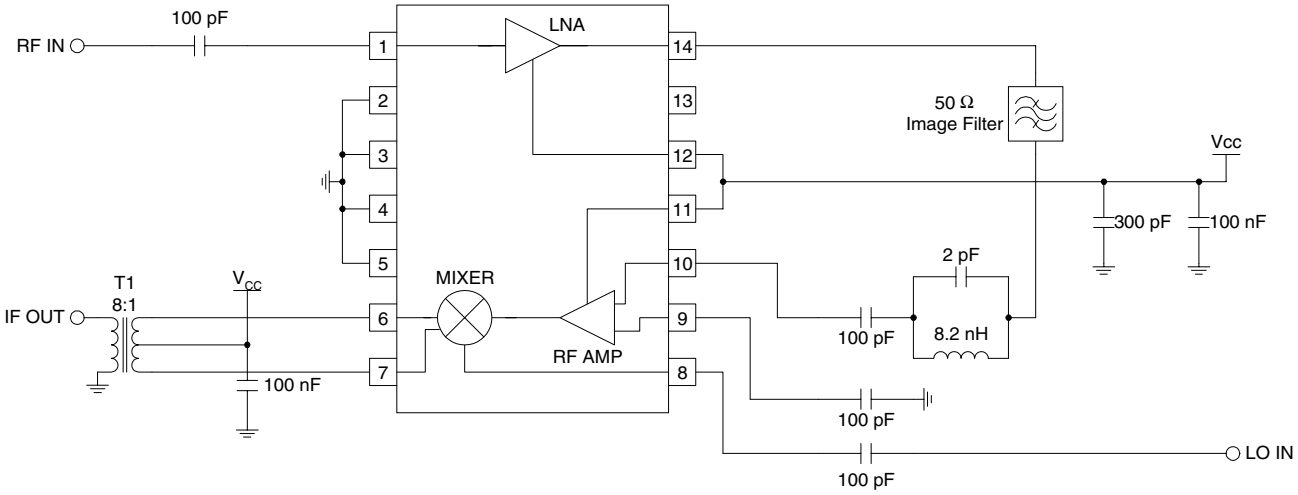
Caution! ESD sensitive device.

Parameter (850MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=850MHz, LO=0dBm, IF=50MHz, Application Schematic 2 configuration
RF Frequency Range		500 to 1900		MHz	
IF Frequency Range		DC to 150		MHz	
Cascade Gain		27		dB	IF=10MHz
	21	25	29		IF=50MHz
		20			IF=150MHz
Cascade IP3		-8		dBm	Referenced to the input
Cascade Noise Figure		2.4		dB	Single sideband, IF=10MHz
		2.4			Single sideband, IF=50MHz
		3.4			Single sideband, IF=150MHz
First Section (LNA)					
Noise Figure		1.6		dB	
Input VSWR		1.5:1			
Input IP3		-3.5		dBm	
Gain		14		dB	
Reverse Isolation		30		dB	
Output VSWR		2.0:1			
Second Section (RF Amp, Mixer, IF1)					
Noise Figure		11.0		dB	Single Sideband
Input VSWR		2.0:1			
Input IP3		+6		dBm	
Conversion Gain		11		dB	
Output Impedance		4		kΩ	Open Collector
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		30		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.5:1			
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		8		mA	V_{CC}=3.0V
		20		mA	V_{CC}=5.0V

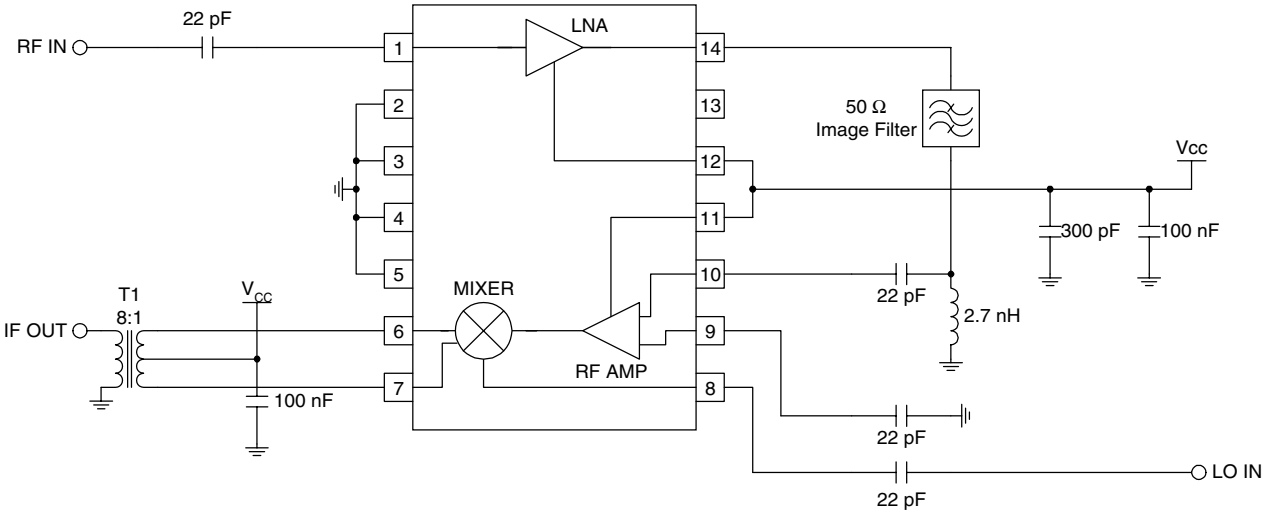
Parameter (1800MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=1800MHz, LO=0dBm, IF=50MHz, Application Schematic 2 configuration
RF Frequency Range		500 to 1900		MHz	
IF Frequency Range		DC to 100		MHz	
Cascade Gain		22		dB	IF=10MHz
		21			IF=50MHz
		17			IF=150MHz
Cascade IP3		-7		dBm	Referenced to the input
Cascade Noise Figure		4.0		dB	Single sideband, IF=10MHz
		4.0			Single sideband, IF=50MHz
		4.8			Single sideband, IF=150MHz
First Section (LNA)					
Noise Figure		2.6		dB	
Input VSWR		1.2:1			
Input IP3		-3.5		dBm	
Gain		10		dB	
Reverse Isolation		25		dB	
Output VSWR		1.5:1			
Second Section (RF Amp, Mixer, IF1)					
Noise Figure		10.0		dB	Single Sideband
Input VSWR		2.0:1			
Input IP3		+3		dBm	
Conversion Gain		11		dB	
Output Impedance		4		kΩ	Open Collector
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		30		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.2:1			

Pin	Function	Description	Interface Schematic
1	LNA IN	This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	IF OUT+	Balanced open collector output of the mixer. External bias needs to be supplied to this pin. This can be done with a resistor to V_{CC} (see application schematic 1), with a Bolan (see application schematic 2) or when used in a single-ended configuration by connecting directly to V_{CC} (see application schematic 3). When using a resistor to V_{CC} the resistor value will set the output impedance. Typical values for this resistor are 200Ω to 1kΩ. A shunt inductor/capacitor resonator to V_{CC} is needed to maintain proper DC voltage at the mixer. At low resistor values the resonator may be omitted at the expense of gain, output power and IP3. To obtain maximum gain and output power a Bolan as shown in application schematics 2 and 4 is recommended. Using both outputs and matching them correctly to a single ended load will result in a 6dB gain improvement over the plain single ended configuration.	
7	IF OUT-	Same as pin 6 except complementary output.	See pin 6.
8	LO IN	50Ω mixer LO input. This pin has an internal pull-up resistor to V_{CC} and is not DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz.	
9	RF IN+	Balanced mixer RF Input port. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz. Matching is required; see the applications schematics. To minimize the noise figure it is recommended to have a bandpass filter before this input. This will prevent noise at the image frequency from being converted to the IF.	
10	RF IN-	Same as pin 9 except complementary input.	See pin 9.
11	VCC2	Supply voltage for the mixer bias circuits.	
12	VCC1	Supply Voltage for the LNA only. A 47pF external bypass capacitor is required and an optional 0.01µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
13	NC	No connection.	
14	LNA OUT	50Ω output. An external DC blocking capacitor is required when this pin is connected to a DC path.	

Application Schematic
850MHz, Output Matching with Balun



Application Schematic
1800MHz, Output Matching with Balun



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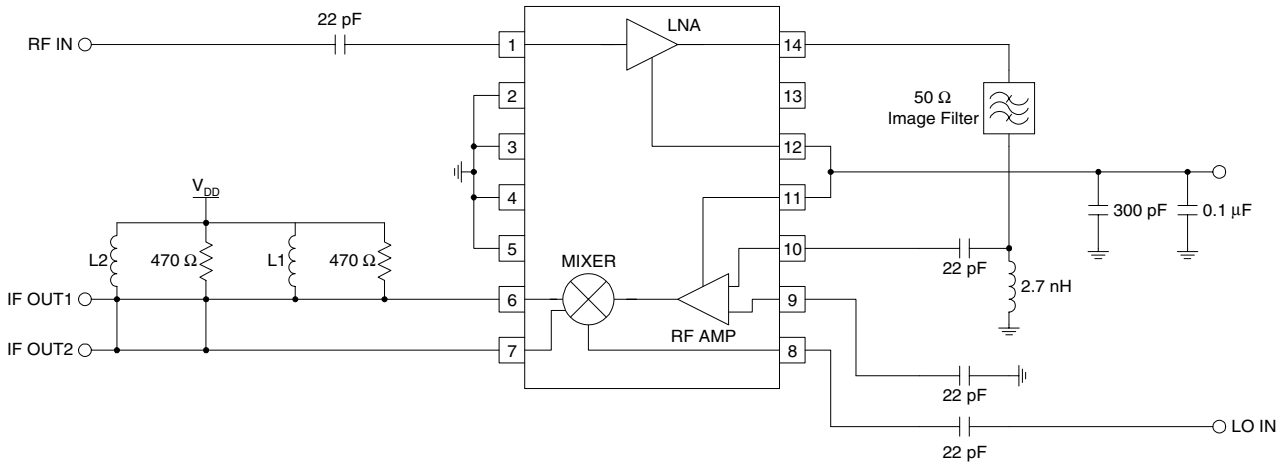
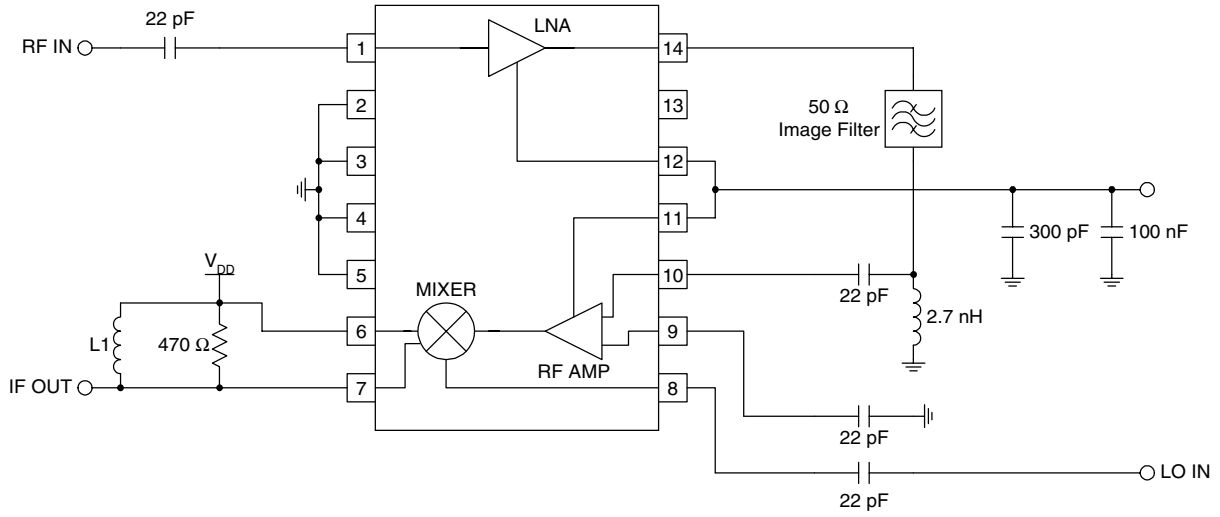
FRONT-ENDS

Application Schematic
1800MHz, Balanced Resistive Output Matching

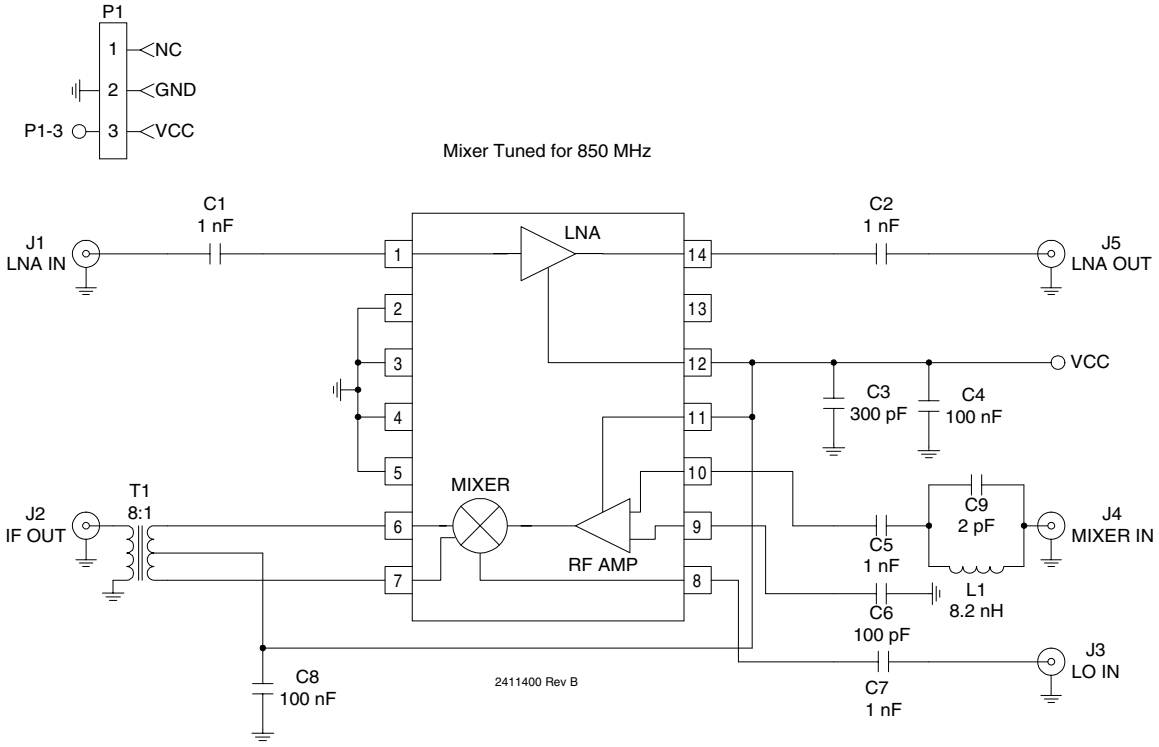


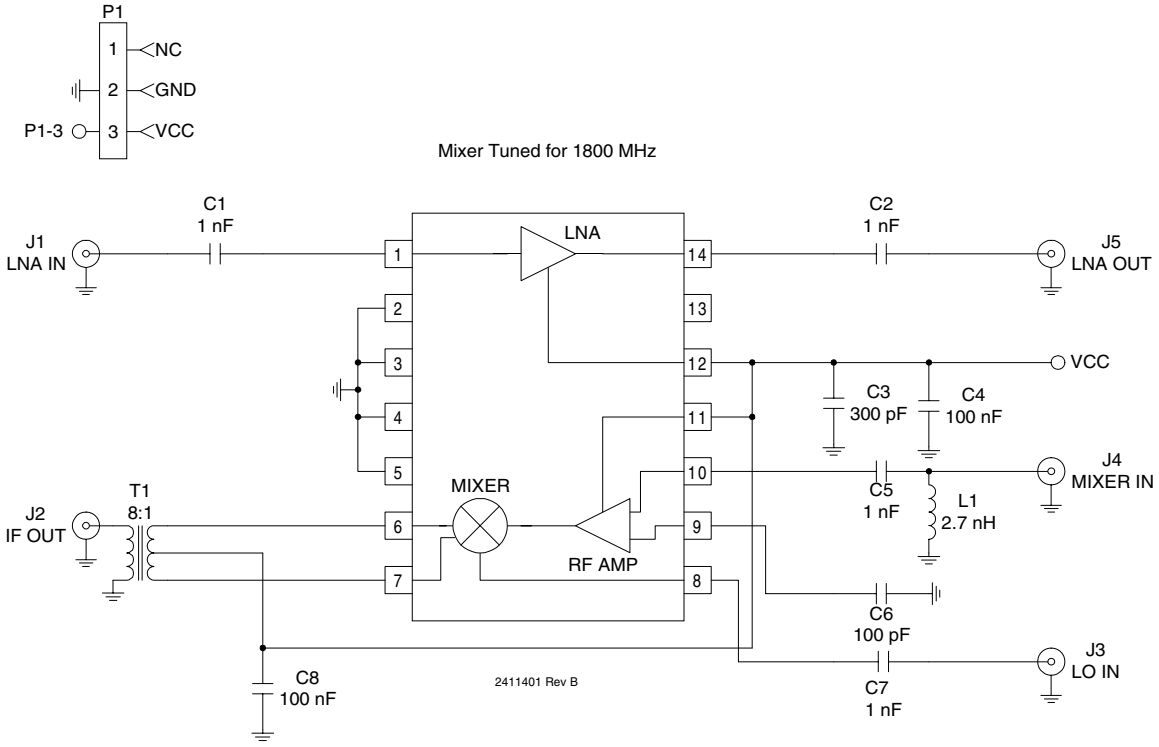
Application Schematic
1800MHz, Single-Ended Resistive Output Matching



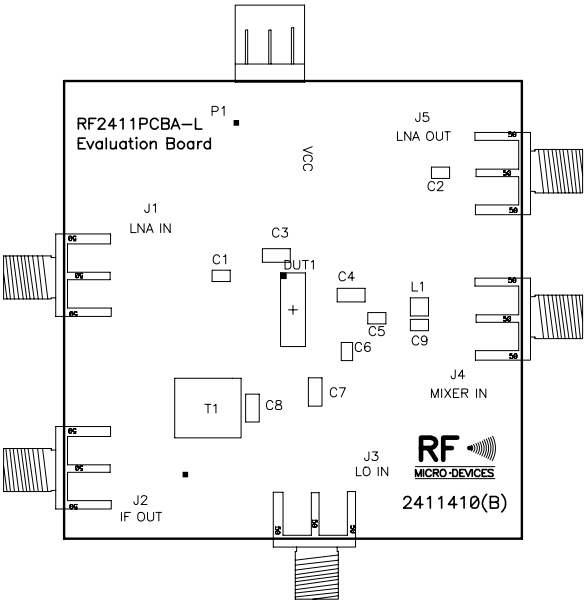
Evaluation Board Schematics

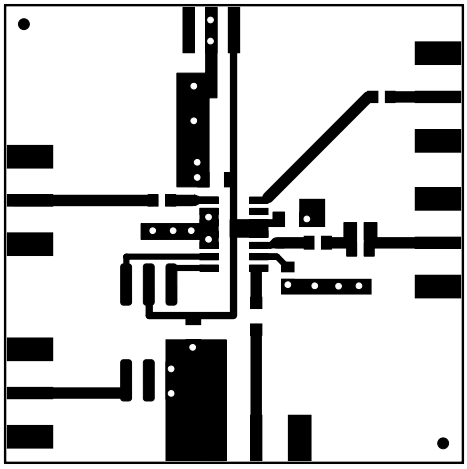
(Download Bill of Materials from www.rfmd.com.)



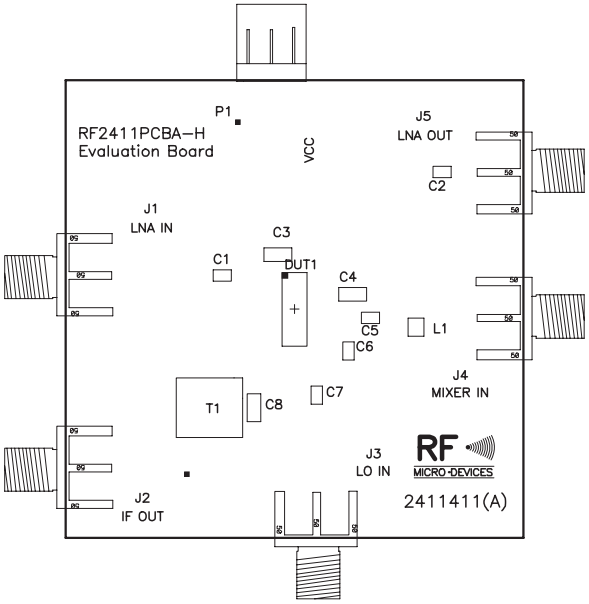


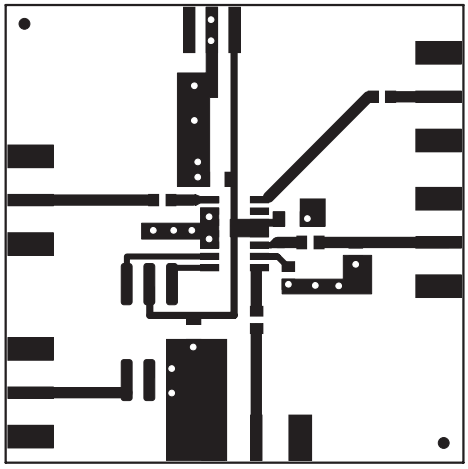
Evaluation Board Layout 850MHz
Board Size 2.0” x 2.0”

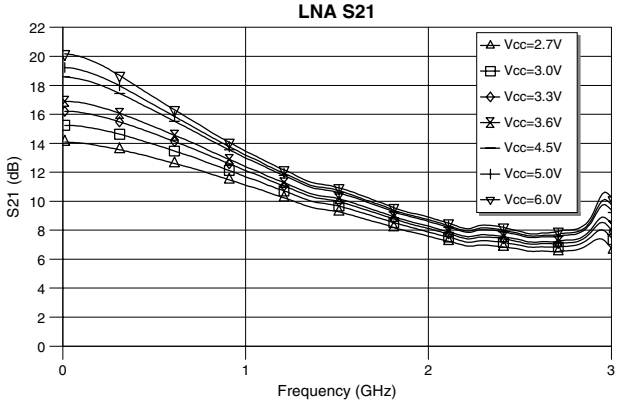


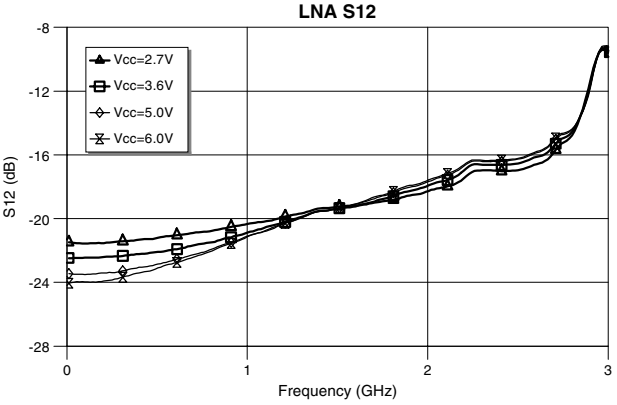


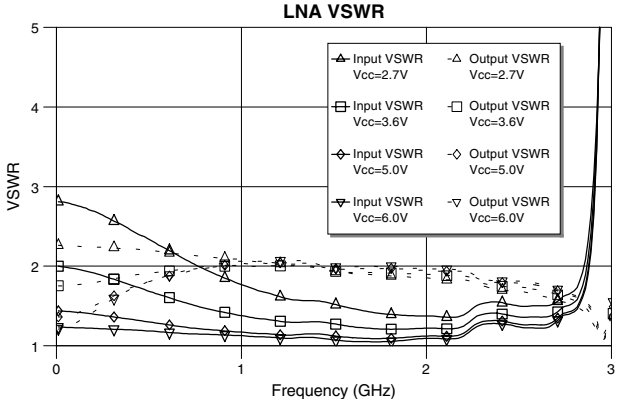
Evaluation Board Layout 1800MHz
Board Size 2.0” x 2.0”

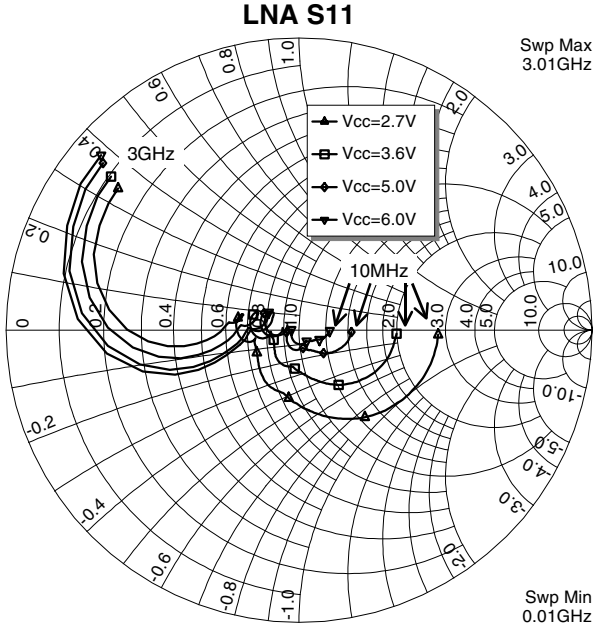


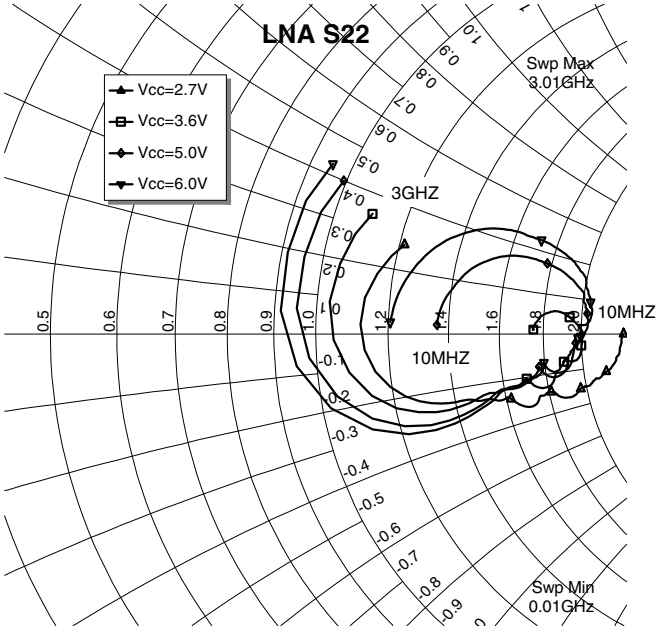



LNA S21
S21 (dB)
Frequency (GHz)
Vcc=2.7V
Vcc=3.0V
Vcc=3.3V
Vcc=3.6V
Vcc=4.5V
Vcc=5.0V
Vcc=6.0V

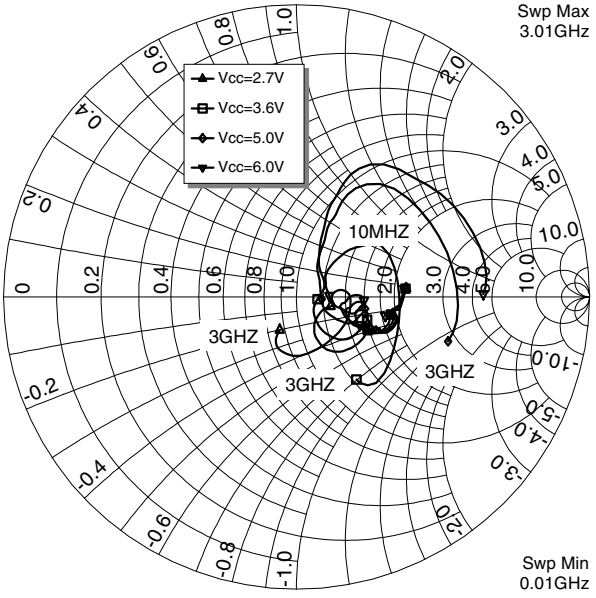

LNA S12
S12 (dB)
Frequency (GHz)
Vcc=2.7V
Vcc=3.6V
Vcc=5.0V
Vcc=6.0V


LNA VSWR
VSWR
Frequency (GHz)
Input VSWR Vcc=2.7V
Output VSWR Vcc=2.7V
Input VSWR Vcc=3.6V
Output VSWR Vcc=3.6V
Input VSWR Vcc=5.0V
Output VSWR Vcc=5.0V
Input VSWR Vcc=6.0V
Output VSWR Vcc=6.0V

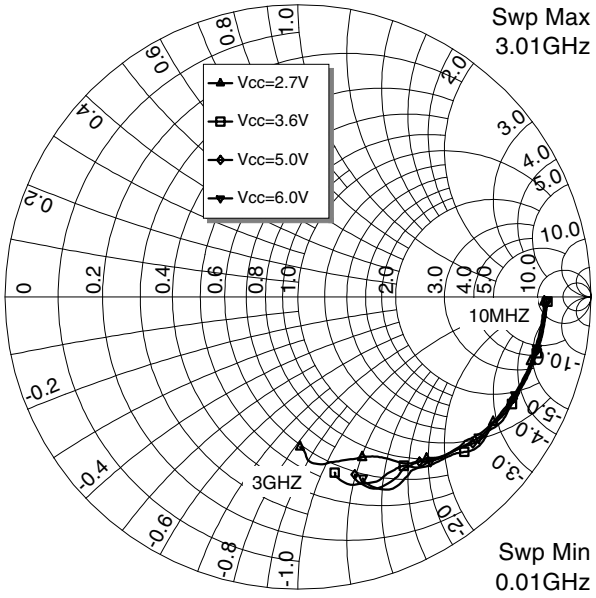

LNA S11
Swp Max
3.01GHz
Swp Min
0.01GHz
3GHz
10MHz
Vcc=2.7V
Vcc=3.6V
Vcc=5.0V
Vcc=6.0V


LNA S22
Swp Max
3.01GHz
Swp Min
0.01GHz
3GHZ
10MHZ
10MHZ
Vcc=2.7V
Vcc=3.6V
Vcc=5.0V
Vcc=6.0V

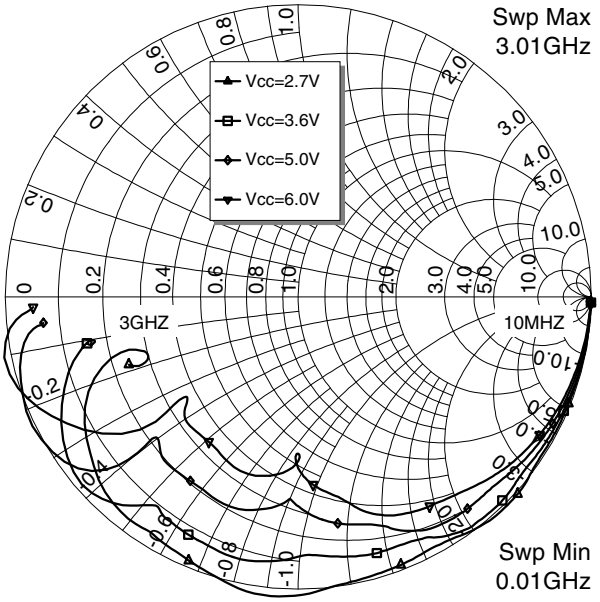
LO Input



RF Input (single ended)



IF Output



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