Typical Applications

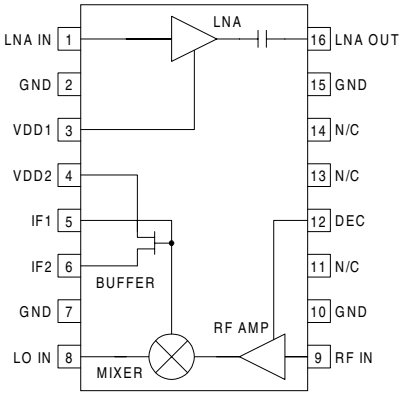
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

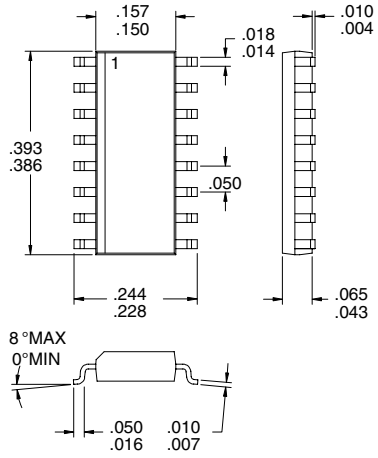
The RF2431 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, a dual-gate GaAs FET mixer, and an IF output buffer amplifier which will drive a 50Ω load. Alternatively, the IF output may be matched to a higher impedance at significantly reduced current. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA output is buffered to permit a wide range of choices for the interstage filter without altering the VSWR or noise figure at the LNA input and to provide high isolation from the LO to the input port.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-16

Features

- Single 3V to 6.5V Power Supply
- 1500MHz to 2500MHz Operation
- 23dB Small Signal Gain
- 3.5dB Cascaded Noise Figure
- 13mA DC Current Consumption
- -14dBm Input IP_3

Ordering Information

RF2431	High Frequency LNA/Mixer
RF2431 PCBA-L	Fully Assembled Evaluation Board (1.8GHz)
RF2431 PCBA-H	Fully Assembled Evaluation Board (2.5GHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

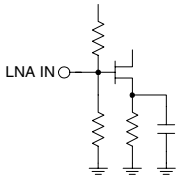
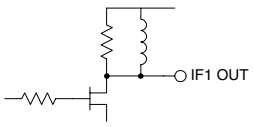
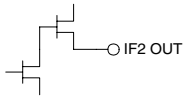
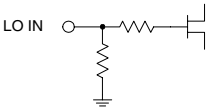
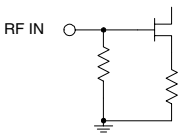
Absolute Maximum Ratings

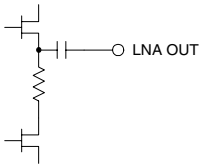
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

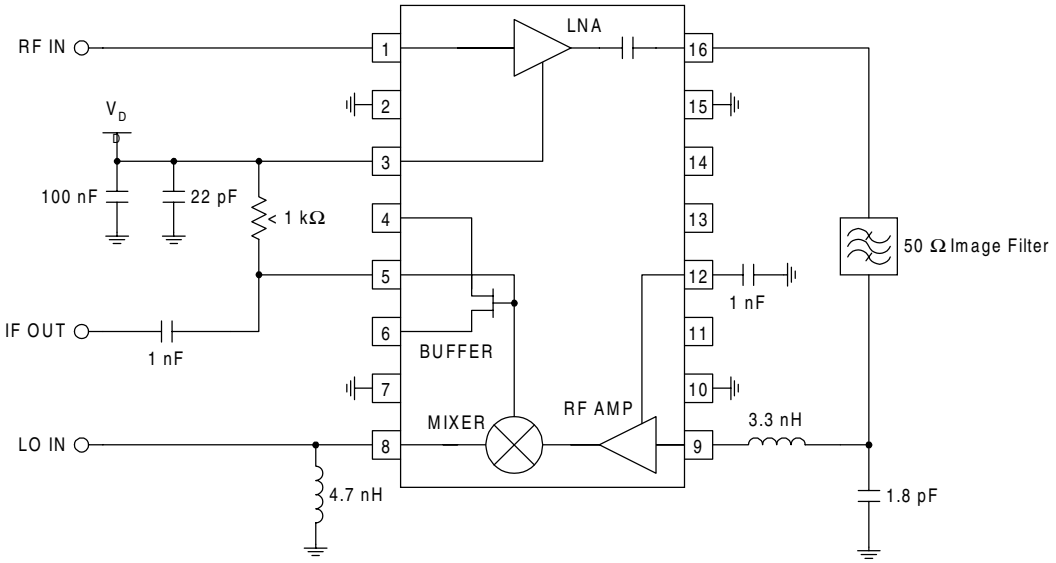
Parameter (1800MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=1800MHz, LO=0dBm
RF Frequency Range		1500 to 2500		MHz	
IF Frequency Range		DC to 400		MHz	
Cascade Gain		23		dB	IF=100MHz, 50Ω load
	15	19		dB	IF=350MHz, 50Ω load
Cascade IP3		-14		dBm	Referenced to the input
Cascade Noise Figure		3.5		dB	Single sideband
First Section (LNA)					
Noise Figure		2.6		dB	
Input VSWR		2.5:1			No external matching
Input IP3		+2		dBm	
Gain		13		dB	
Reverse Isolation		30		dB	
Output VSWR		1.5:1			No external matching
Second Section (RF Amp, Mixer, IF1)					High impedance output, 1.3kΩ load
Noise Figure		9.5		dB	Single sideband
Input VSWR		1.7:1			
Input IP3		-1		dBm	
Conversion Gain		6		dB	
Output Impedance		4		kΩ	Open drain
Second Section (RF Amp, Mixer, IF2)					Buffered output, 50Ω load
Noise Figure		9.5		dB	Single sideband
Input VSWR		1.7:1			
Input IP3		-1		dBm	
Conversion Gain		6		dB	
Output VSWR		1.2:1			
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		15		dB	
LO to IF Rejection		25		dB	
LO Input VSWR		1.5:1			
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		19	25	mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer On
		13		mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer Off

Parameter (2400MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=2400MHz, LO=0dBm
RF Frequency Range		2.0 to 2.5		GHz	
IF Frequency Range		DC to 400		MHz	
Cascade Gain		13		dB	IF=100MHz, 50Ω load
		10		dB	IF=350MHz, 50Ω load
Cascade IP_3		-11		dBm	Referenced to the input
Cascade Noise Figure		4.5		dB	Single sideband
First Section (LNA)					
Noise Figure		2.9		dB	
Input VSWR		1.8:1			No external matching
Input IP3		0		dBm	
Gain		10		dB	
Reverse Isolation		25		dB	
Output VSWR		1.6:1			No external matching
Second Section (RF Amp, Mixer, IF1)					High impedance output, 1.3kΩ load
Noise Figure		10		dB	Single sideband
Input VSWR		1.5:1			
Input IP_3		-1		dBm	
Conversion Gain		3		dB	
Output Impedance		4		kΩ	Open drain
Second Section (RF Amp, Mixer, IF2)					Buffered output, 50Ω load
Noise Figure		10		dB	Single sideband
Input VSWR		1.5:1			
Input IP_3		-1		dBm	
Conversion Gain		3		dB	
Output VSWR		1.2:1			
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		15		dB	
LO to IF Rejection		20		dB	
LO Input VSWR		1.4:1			
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		19		mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer On
		13		mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer Off

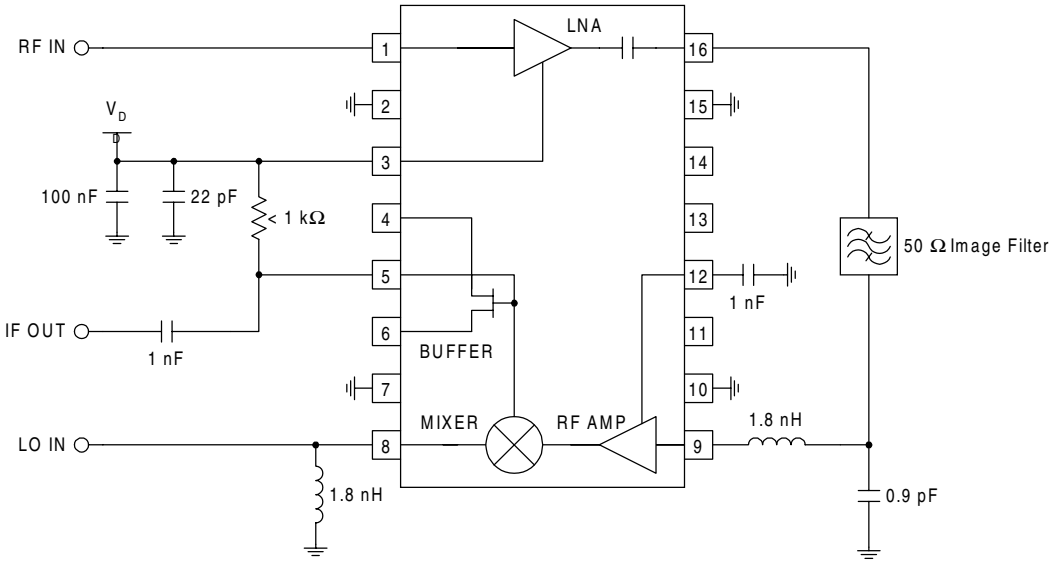
Pin	Function	Description	Interface Schematic
1	LNA IN	This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VDD1	Supply voltage for the LNA only. A 22pF external bypass capacitor is required and an additional 0.01µF is required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
4	VDD2	Power supply for the IF buffer amplifier. If the high impedance mixer output is being used, then this pin is not connected.	
5	IF1 OUT	Open drain output port, one of the two output options. This pin must be connected to V_{DD} through a resistor in order to bias the mixer, even when using the IF2 Output. In addition, a 0.1µF bypass capacitor is required at the other end of the bias resistor. This output is intended to drive high impedance IF filters. The intrinsic output impedance is about 4kΩ, which means that the actual impedance is set by the external resistor to V_{DD}.	
6	IF2 OUT	50Ω buffered output port, one of the two output options. This is an open drain output, therefore a resistor to ground is needed. The typical value for this resistor is 470Ω. Pin 4 must be connected to V_{DD} in order to turn the buffer amplifier on. Current drain will increase by approximately 6mA at 5V; by approximately 3mA at 3V.This pin is not connected when using the high impedance port.	
7	GND	Same as pin 2.	
8	LO IN	Mixer LO input. An high-pass matching network, such as a single shunt inductor (as shown in the application schematics), is the recommended topology because it also rejects IF noise at the mixer input. The value of this inductor is depending on the frequency, see the application schematics. This filtering is required to achieve the specified noise figures. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
9	RF IN+	Mixer RF Input port. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended. Matching is required; see the applications schematics.To minimize the noise figure it is recommended to have a bandpass filter before this input. This will prevent the noise at the image frequency from being converted to the IF.	
10	GND	Same as pin 2.	
11	NC	No connection	
12	RF BYP	Connection for the external bypass capacitor for the mixer input buffer amplifier. 1nF is recommended. The trace length between the pin and the capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
13	NC	No connection.	
14	NC	No connection.	
15	GND	Same as pin 2.	

16	LNA OUT	50Ω output. Internally DC blocked.	

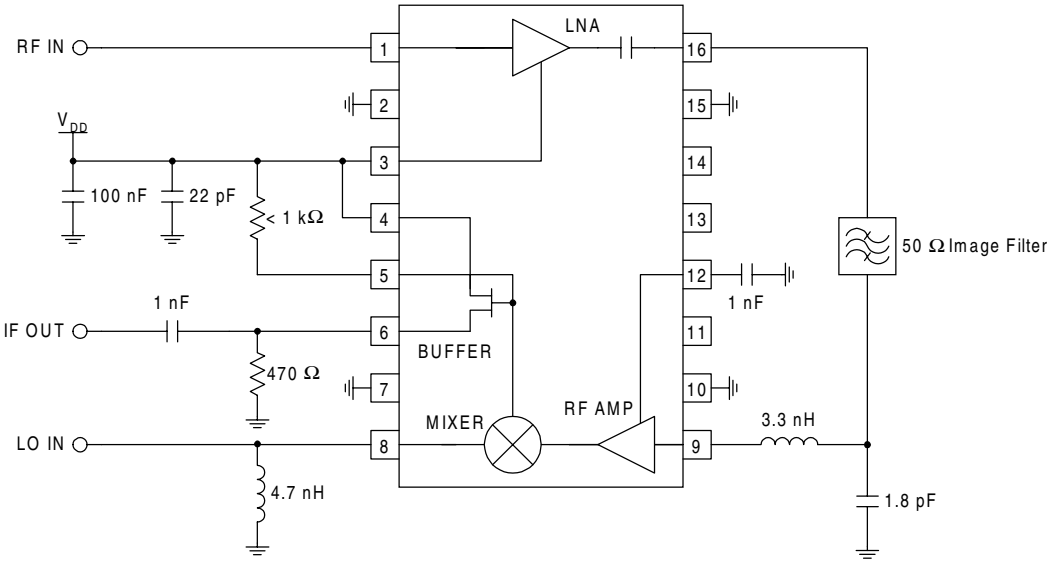
Application Schematic 1800MHz, High Impedance Output



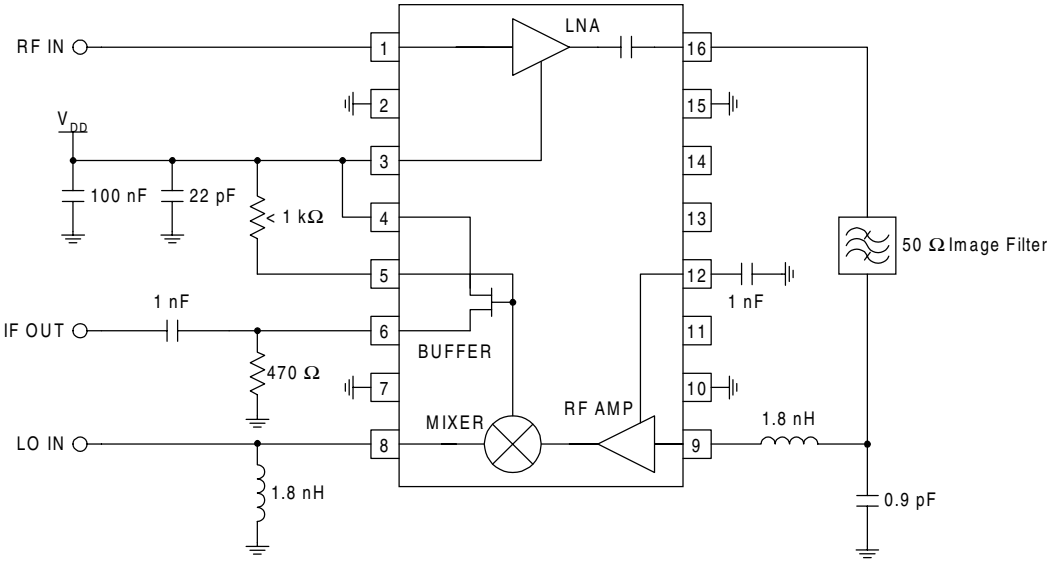
Application Schematic 2400MHz, High Impedance Output



Application Schematic
1800MHz, Buffered Output

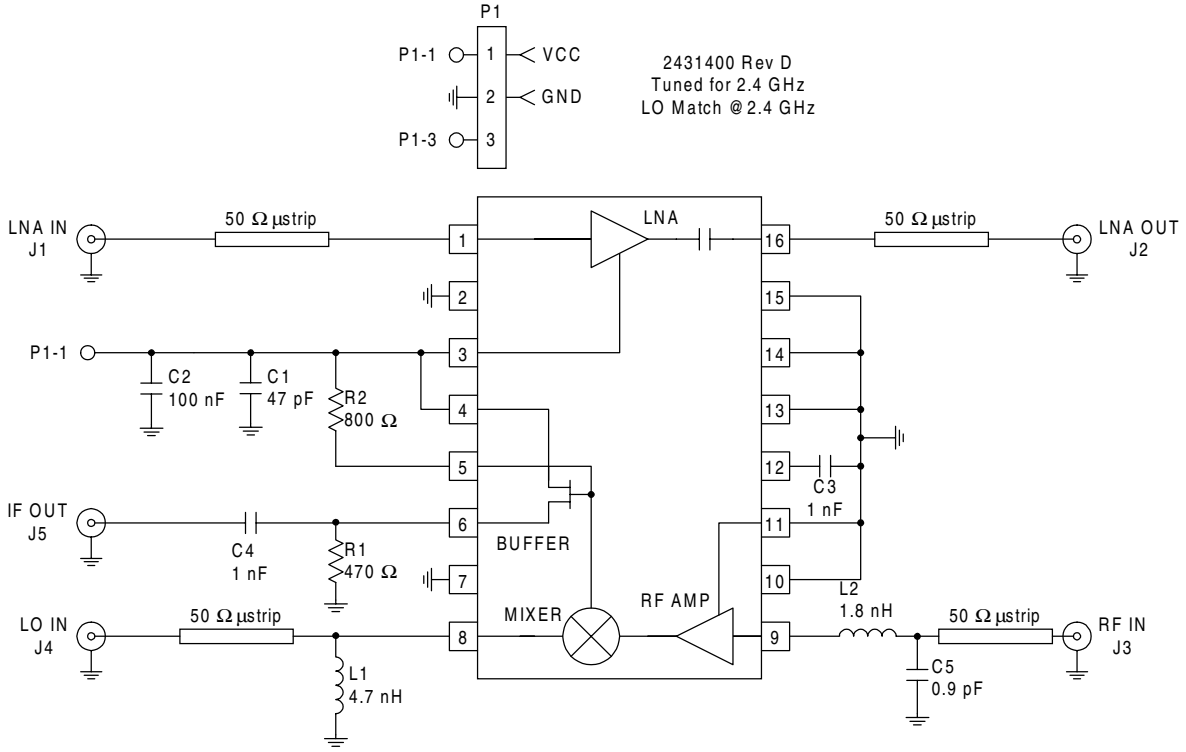


Application Schematic
2400MHz, Buffered Output



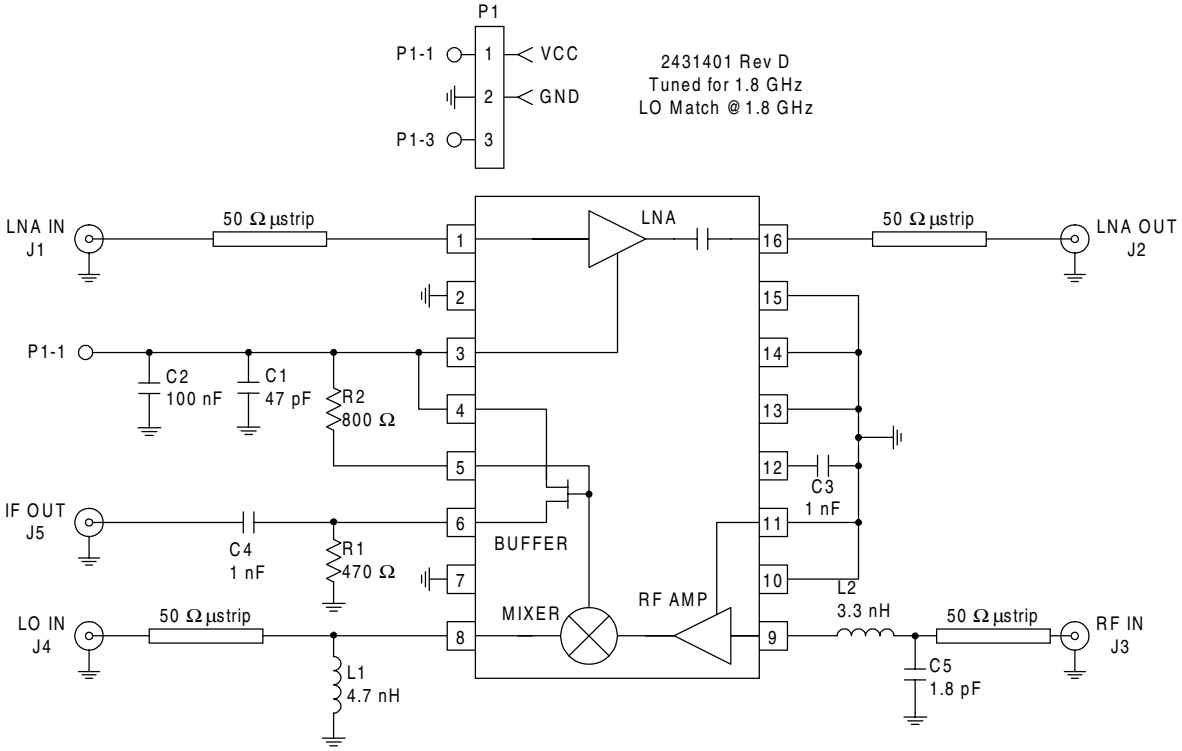
Evaluation Board Schematic
2400MHz

(Download Bill of Materials from www.rfmd.com.)

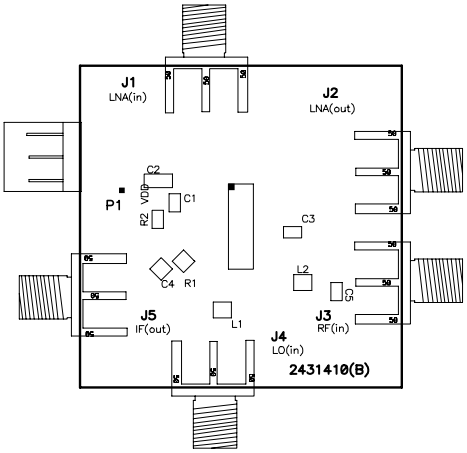


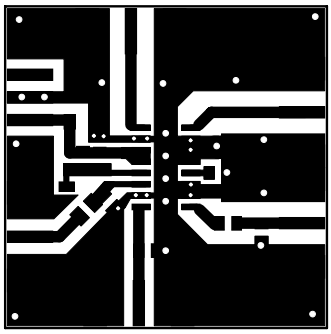
Evaluation Board Schematic
1800MHz

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2400MHz





Evaluation Board Layout
1800MHz