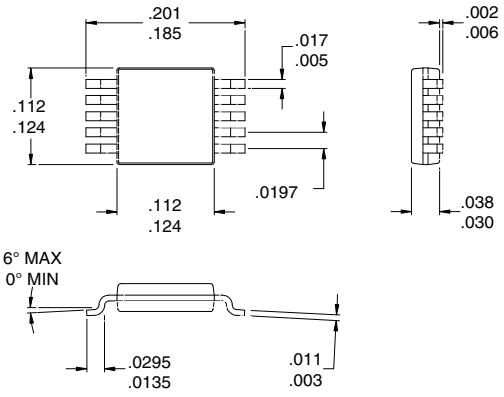
## Typical Applications

- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- General Purpose Frequency Conversion

## Product Description

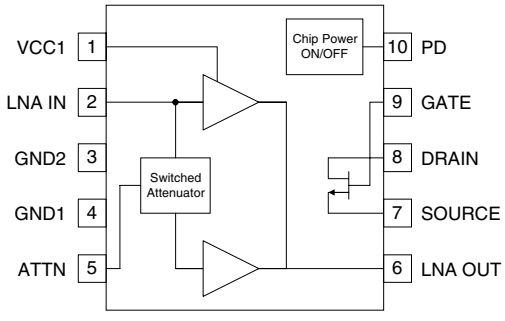
The RF2457 is a front-end receiver IC chip developed for the handset/portable battery-powered equipment markets. The chip contains an RF 15dB attenuator, an LNA and a passive mixer. By using a state-of-the-art Si Bi-CMOS process, the LNA has high dynamic range under very low DC operating conditions and the passive mixer requires no DC bias at all. Packaged in the industry-standard MSOP-10 package, the device is well-suited for limited board space applications.




**Optimum Technology Matching® Applied**

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS

**Package Style: MSOP-10**




**Functional Block Diagram**

## Features

- Single Supply 3V Operation
- 2.2dB LNA NF
- -3.0dBm IIP3
- Small MSOP-10 Package
- Very Low Current Drain (5mA maximum)
- Very Low Cost

**Ordering Information**

| | |
|---|---|
| RF2457 | 900MHz 3V Low Current LNA/Mixer |
| RF2457 PCBA | Fully Assembled Evaluation Board |

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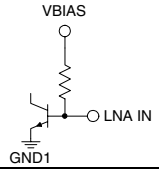
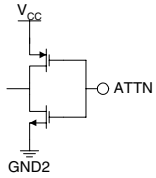
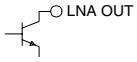
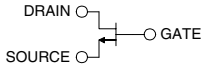
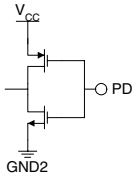
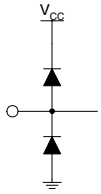
## Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage | -0.5 to +3.6 | $V_{DC}$ |
| Input RF Level | +10 | dBm |
| Operating Ambient Temperature | -40 to +85 | °C |
| Storage Temperature | -40 to +150 | °C |

**Caution!** ESD sensitive device.

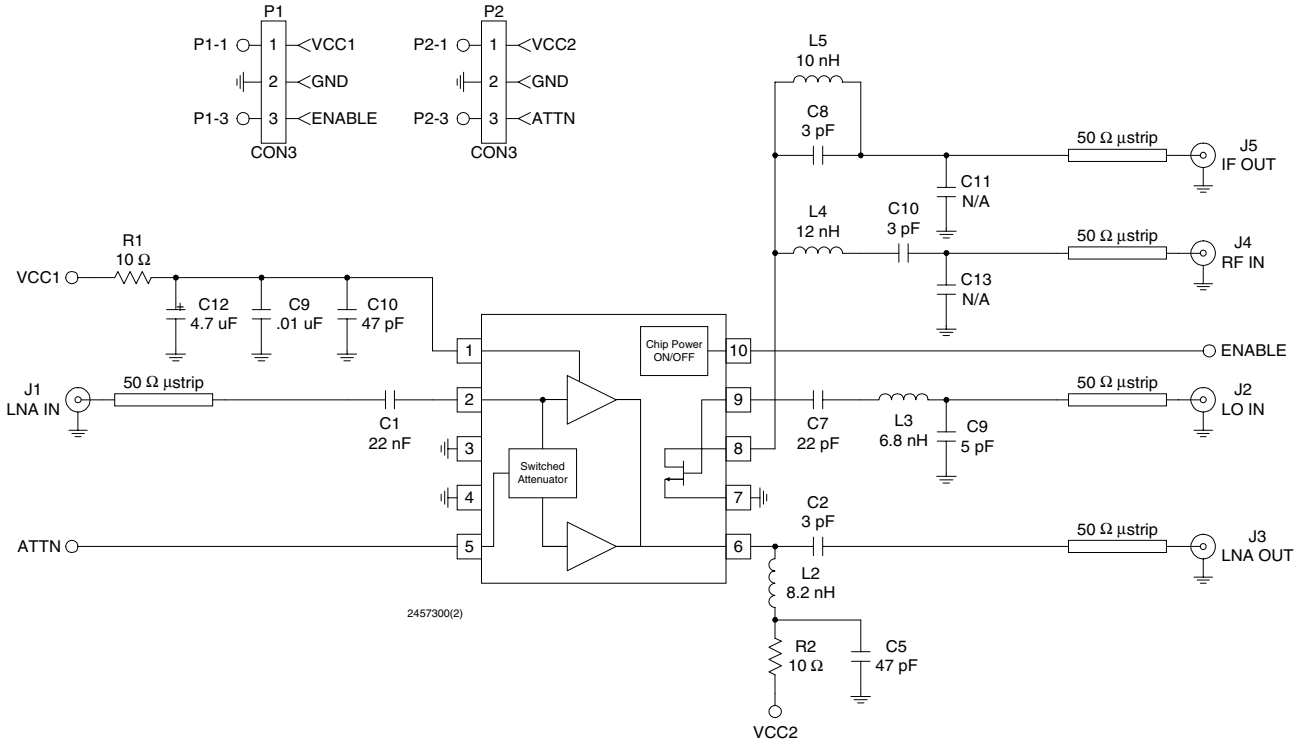
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Overall** | | | | | T=25°C, $V_{CC}$=2.8V, RF=915MHz |
| RF/LO Frequency Range | | 902 to 928 | | MHz | Specifications |
| | | 800 to 1000 | | MHz | Usable range |
| **LNA** | | | | | |
| Gain | 14.0 | 15.0 | | dB | High gain state |
| | 0.9 | 1.9 | | dB | Low gain state |
| Input IP3 | -4.0 | -3.0 | | dBm | High gain state, RF IN=-25dBm |
| | +5.5 | +6.5 | | dBm | Low gain state, RF IN=-15dBm |
| Noise Figure | | 2.2 | 2.4 | dB | High gain state |
| | | 15 | | dB | Low gain state |
| Input VSWR | | | 2.2:1 | | |
| Output VSWR | | | 2.0:1 | | |
| **Mixer** | | | | | |
| Conversion Gain | -7.5 | -6.5 | | dB | With LO=+2dBm |
| LO Input Level | -2.0 | 0 | +2.0 | dBm | |
| IIP3 | +10.0 | +12.0 | | dBm | With LO=+2dBm |
| **Attenuation** | | | | | |
| Attn enable | | >1.6 | | V | Low gain state |
| Attn disable | | 0 | | V | High gain state |
| **Power Down** | | | | | |
| Chip enable | | >1.6 | | V | Voltage applied to PD pin |
| Chip disable | | 0 | | V | Voltage applied to PD pin |
| Noise figure | | 6.5 | | dB | With LO=+2dBm |
| **Power Supply** | | | | | |
| Voltage | | 2.8 | | V | Specifications |
| | | 2.7 to 3.3 | | V | Operating limits |
| Current Consumption | | 5 | 6.5 | mA | Chip enabled |
| | | <1 | 1.0 | uA | Chip disabled |

| Pin | Function | Description | Interface Schematic |
|---|---|---|---|
| 1 | VCC1 | Supply voltage for the LNA, bias circuits, and control logic. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. | |
| 2 | LNA_IN | RF Input pin. This pin is internally matched for optimum noise figure from a 50Ω source. This pin is internally DC biased and, if connected to a device with DC present, should be blocked with a capacitor suitable for the frequency of operation. |  |
| 3 | GND2 | Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. | |
| 4 | GND1 | Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance. | See pin 2. |
| 5 | ATTN | Attenuation pin. A logic high reduces LNA gain by 15dB. |  |
| 6 | LNA OUT | LNA Output pin. This pin requires a connection to $V_{CC}$ through an inductor. |  |
| 7 | SOURCE | Connection to source of MOSFET transistor used as mixer. Drain and source are symmetric. |  |
| 8 | DRAIN | Connection to drain of MOSFET transistor used as mixer. | See pin 7. |
| 9 | GATE | Connection to gate of MOSFET transistor used as mixer. Internally DC biased. Use DC blocking capacitor. | See pin 7. |
| 10 | PD | Power control. A logic “low” turns the part off. A logic “high” (>1.6V) turns the part on. |  |
| | ESD | This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 9, 10. |  |

# Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



# Evaluation Board Layout
# Board Size 1.108" x 1.282"

Board Thickness 0.031", Board Material FR-4