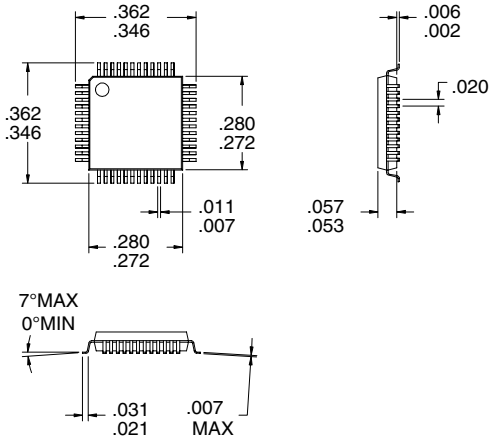
CDMA/FM TRANSMIT MODULATOR, IF AGC, AND UPCONVERTER WITH INTEGRATED PLL

Typical Applications

- CDMA/FM Cellular Systems
- CDMA PCS Systems
- W- CDMA Systems
- Wireless Local Loop Systems
- Spread Spectrum Cordless Phones
- High Speed Data Modems

Product Description

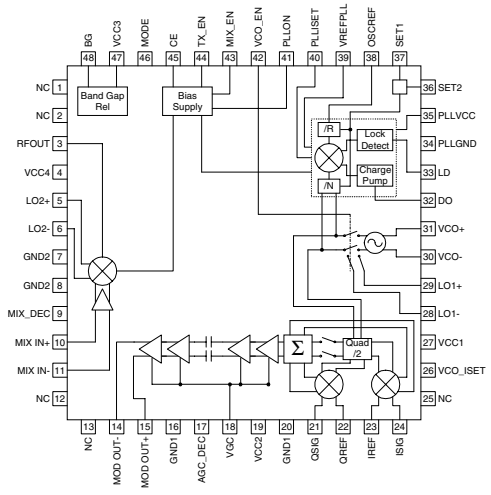
The RF2668 is an integrated complete Quadrature Modulator, IF AGC amplifier, Upconverter, and PLL, designed for the transmit section of dual-mode CDMA/FM cellular and PCS applications. It is designed to modulate baseband I and Q signals, amplify the resulting IF signals while providing 95dB of gain control range, and perform the final upconversion to UHF. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 Interim Standard for CDMA cellular communications. This circuit is designed as part of RFMD's newest CDMA Chip Set, which also includes the RF2667 CDMA/FM Receive IF AGC and Demodulator. The IC is manufactured on an advanced 18GHz F_T Silicon Bipolar process, and is supplied in a 48-lead plastic LQFP package.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation
- Digitally Controlled Power Down Modes
- 2.7V to 3.3V Operation
- Digital First LO Quadrature Divider
- Double-Balanced UHF Upconvert Mixer
- IF AGC Amp with 95dB Gain Control

Ordering Information

RF2668	CDMA/FM Transmit Modulator, IF AGC, and Upconverter with Integrated PLL
RF2668 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC} + 0.7	V
I and Q Levels, per pin	1	V_{PP}
LO1 Level, balanced	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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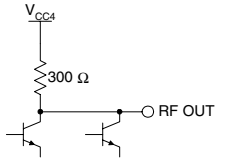
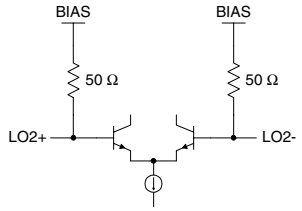
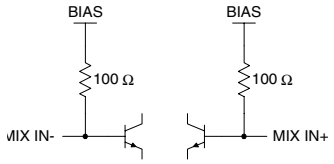
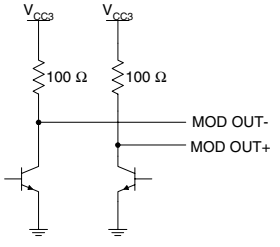
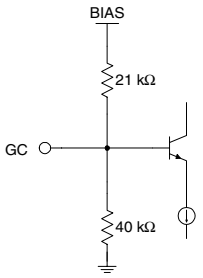
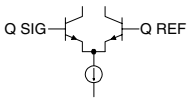
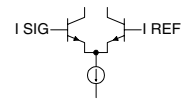
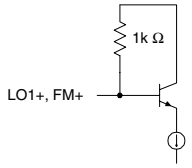
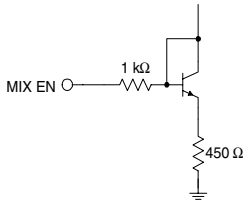
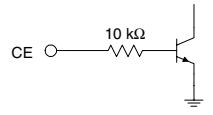
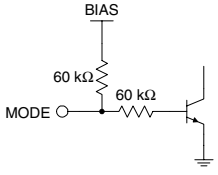
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q Modulator & AGC					T=25 °C, V_{CC}=3.0V, Z_{LOAD}=200Ω, LO1=-10dBm @ 260MHz, IF=130MHz, I SIG=Q SIG=300mV$_{PP}$, RF Output externally matched
I/Q Input Frequency Range		0 to 20		MHz	Balanced
I/Q Input Impedance		80		kΩ	Balanced
I/Q Input Reference Level		1.3		V_{DC}	Per Pin
LO1/FM Frequency Range	0		800	MHz	
LO1/FM Input Level	-15	-10	-5	dBm	
LO1/FM Input Impedance		200		Ω	Balanced
Sideband Suppression	35	40		dBc	I/Q Amplitude adjusted to within ±20mV
		27		dBc	Unadjusted
Carrier Suppression	40	50		dBc	I/Q DC Offset adjusted to within ±20mV
		30		dBc	Unadjusted
Max Output, FM Mode	+2.5	+5		dBm	V_{GC}=2.4V_{DC}, T=-20°C to +85°C
Max Output, CDMA Mode	-3	0		dBm	V_{GC}=2.4V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
	-2	0		dBm	ISIG=QSIQ=300mVpp @ 100kHz
Min Output, CDMA Mode		-95	-89	dBm	V_{GC}=0.3V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
Output Power Accuracy	-3		+3	dB	T=-20 to +85 °C, Ref=25 °C
	-2		+2	dB	1.4V≤GC≤2.5
Adjacent Channel Power Rejection @ 885kHz		-60		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Adjacent Channel Power Rejection @ 1.98MHz		-69		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Output Noise Power		-117	-111	dBm/Hz	P_{OUT} = -1dBm, T=-20°C to +85°C
Output Impedance		200		Ω	Balanced
Current Consumption		40		mA	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
UHF Upconverter					Output externally matched
General					
IF Input Impedance		200		Ω	Balanced
IF Input Frequency Range	0		400	MHz	
LO2 Input Impedance		50		Ω	Single Ended
LO2 Input Level	-6	-3	0	dBm	
LO2 Input Frequency Range			2.5	GHz	
RF to LO2 Isolation		30		dB	
LO Input VSWR		<2:1			50Ω
Current Consumption		24		mA	
Cellular					
Conversion Gain	-1.5	-0.5		dB	RF_{OUT}=830MHz
Noise Figure (SSB)		15		dB	RF_{OUT}=830MHz
Output IP3		+13		dBm	P_{IN}=-15dBm per tone, 200kHz tone separation, RF_{OUT}=830MHz, LO2=960MHz@-3dBm
RF Output VSWR		<2:1			RF_{OUT} = 830MHz
PCS					
Conversion Gain		-1.5		dB	RF_{OUT}=1950MHz
Noise Figure		TBD			
Output IP3		10			P_{IN}=15dBm per tone, 200kHz tone separation, RF_{OUT}=1950MHz, LO2=1570MHz@-3dBm
RF Output VSWR		<2:1			RF_{OUT}=1950MHz. See note on eval board schematic.
VCO					PLL locked with Loop BW=5kHz, Tank Values: 39nH and SMV1234 varactor.
Phase Noise @ 100kHz		-110		dBc/Hz	
Current Consumption		1		mA	
PLL					
Charge Pump Current			100	µA	
TCXO Input Level		0.8		V_{PP}	
PLL Lock Time		4/Loop		BW	S
Current Consumption		4		mA	
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		69		mA	
Power Down Current		<10		µA	
VPD HIGH Voltage	V_{CC}-0.3			V	
VPD LOW Voltage			0.3	V	
PLL Settings					
Application	**Japan**	**Japan**	**US/Korea**		
LO Frequency, MHz	333.7	333.7	260.76		IF Frequency=LO Frequency/2
Crystal, MHz	19.2	19.8	19.68		
Reference Divider	192	198	252		
Phase Detector Frequency, kHz	100	100	78.09524		
Prescaler	32/33	32/33	32/33		
Swallow Counter (A)	9	9	11		
Fixed Divider (N)	104	104	104		
Net N in VCO Path	3337	3337	3339		
SEL1	VCC	GND	GND		
SEL2	GND	VCC	GND		

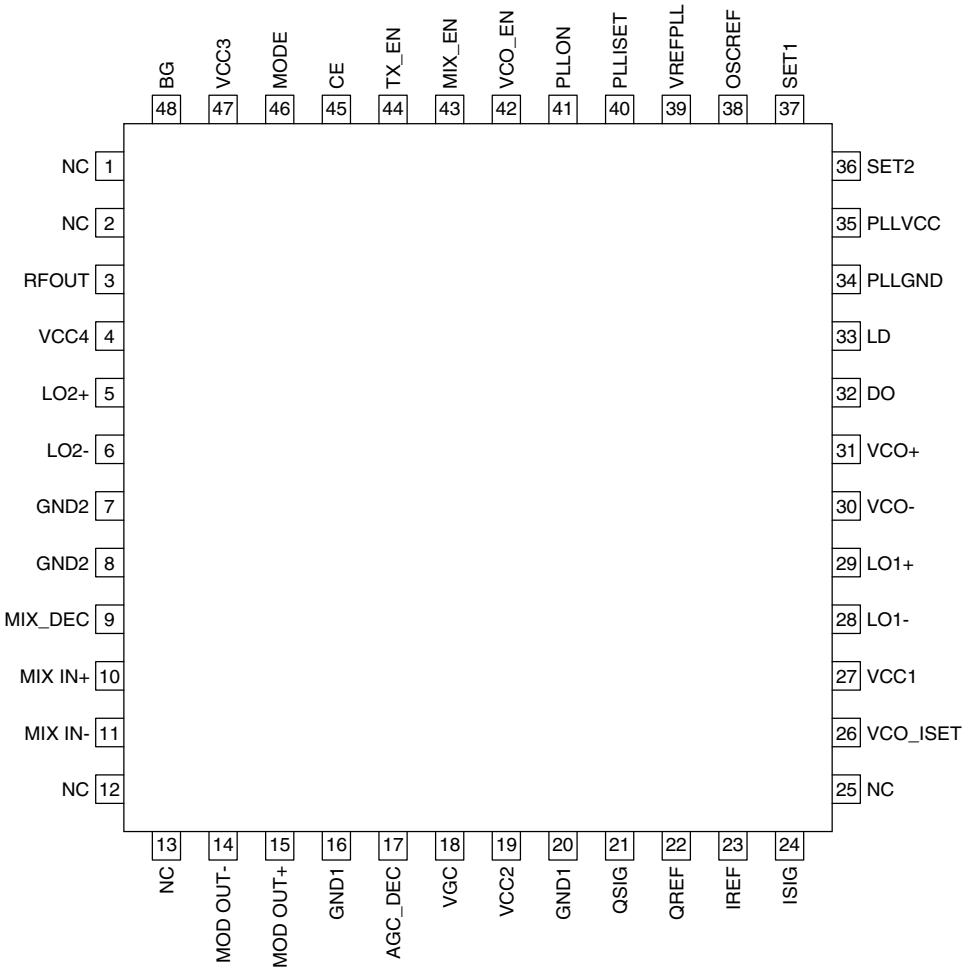
Pin	Function	Description	Interface Schematic
1	NC	Not connected.	
2	NC	Not connected.	
3	RF OUT	RF output pin. An external shunt inductor to V_{CC} plus a series blocking/ matching capacitor are required for 50Ω output.	
4	VCC4	Supply for the mixer stage only. The supply for the mixer is separated to maximize IF to RF isolations and reduce the carrier leakage. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	LO2+	One half of the balanced mixer LO2 input. In single-ended applications, the other half of the input, LO2- is AC grounded. This is a 50Ω impedance port. This pin is NOT internally DC blocked. An external blocking capacitor (100pF recommended) must be provided if the pin is connected to a device with DC present.	
6	LO2-	One half of the balance mixer LO2 input. In single ended applications, this pin is AC grounded with a 100pF capacitor.	See pin 19.
7	GND2	Ground connection for the mixer stage. Keep traces physically short and connect immediately to ground plane for best performance.	
8	GND2	Same as pin 16.	
9	MIX_DEC	Current Mirror decoupling pin. A 1000pF external capacitor is required to bypass this pin. The ground side of the bypass capacitors should connect immediately to ground plane.	
10	MIX IN+	Same as pin 11, except complementary input.	See pin 11.
11	MIX IN-	One half of the 200Ω balanced impedance input to the mixer stage. This pin is NOT internally DC blocked. An external blocking capacitor (1000pF recommended) must be provided if the pin is connected to a device with DC present. If no IF filter is needed this pin may be connected to MOD OUT+ through a DC blocking capacitor. An appropriate matching network may be needed if an IF filter is used.	
12	NC	Not connected.	
13	NC	Not connected.	
14	MOD OUT-	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. If no filtering is required, this pin can be connected to the MIX IN- pin through a DC blocking capacitor. This pin requires an inductor to V_{CC} to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
15	MOD OUT+	Same as pin 14, except complementary output.	See pin 14.
16	GND1	Ground connection for all baseband circuits including bandgap, AGC, flip-flop, modulator and FM amp. Keep traces physically short and connect immediately to ground plane for best performance.	

Pin	Function	Description	Interface Schematic
17	AGC_DEC	AGC decoupling pin. An external bypass capacitor of 1nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
18	VGC	Analog gain control for AGC amplifiers. Valid control voltage ranges are from $0.3V_{DC}$ to $2.4V_{DC}$. The gain range for the AGC is 95dB. These voltages are valid ONLY for a 39kΩ source impedance. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
19	VCC2	Supply for the modulator stage only. A 10nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
20	GND1	Same as pin 16.	
21	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The DC level of 1.3V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
22	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the Q SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 2.
23	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the I SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 5.
24	I SIG	Baseband input to the I mixer. This pin is DC coupled. The DC level of 1.3V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
25	NC	Not connected.	
26	VCO_ISET	An external resistor of 47kΩ is used to set the VCO current for minimum phase noise.	
27	VCC1	Supply Voltage for the LO1 flip-flop and limiting amp only. This supply is isolated to minimize the carrier leakage. A 1nF external bypass capacitor is required, and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
28	LO1-	External LO input to modulator. Controlled by VCO_EN signal. Logic low is internal VCO, while logic high is external VCO.	See pin 8.

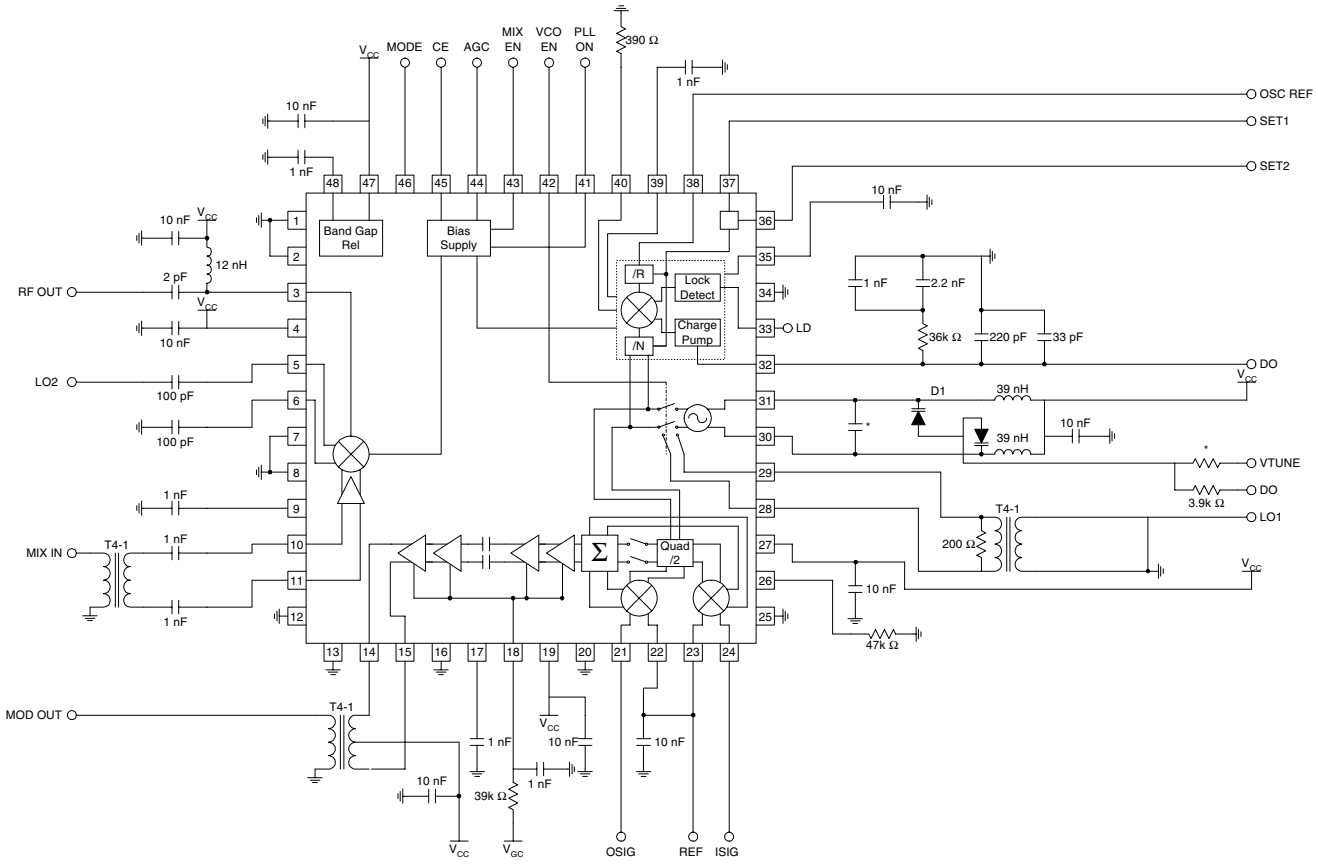
Pin	Function	Description	Interface Schematic
29	LO1+	External LO input to modulator. Controlled by VCO_EN signal. Logic low is internal VCO, while logic high is external VCO.	
30	VCO-	See VCO+ description.	
31	VCO+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 30 although a small imbalance can be used to tune in the proper frequency range.	
32	DO	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
33	LD	Lock detector output for synthesizer. Requires external transistor to provide hysteresis and inversion of signal. See Application circuit.	
34	PLLGND	Ground for synthesizer. Keep traces physically short and connect immediately to ground plane for best performance.	
35	PLLVCC	Supply for the PLLVCC only. A 10nF external bypass capacitor is required and an additional 0.1μF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
36	SET2	PLL Setting (Divider) pin. See the PLL settings table.	
37	SET1	See SET2.	
38	OSCREF	TCXO reference input for synthesizer.	
39	VREFPLL	Bypass pin for the synthesizer reference voltage.	
40	PLLISET	Current setting pin for synthesizer charge pump. For normal operation, a 390Ω resistor to ground should be used to set the current.	
41	PLLON	Synthesizer Enable pin.	See pin 45.
42	VCO_EN	VCO Enable pin. Switches between internal and external VCO.	See pin 45.
43	MIX_EN	Power down control for mixer only. When connected to logic “high” ($>V_{CC}$-0.3) the mixer circuits are operating; when connected to ground (≤0.3V), the mixer is turned off but all other circuits are operating. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
44	TX_EN	Shuts down the entire TX path. VCO is still active when TX disabled. Logic high (>VCC -0.3) for TX Enable.	
45	CE	Power down control for overall circuit. When logic “high” ($\geq V_{CC}$-0.3V), all circuits are operating; when logic “low” (≤0.3V), all circuits are turned off. The input impedance of this pin is >10kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
46	MODE	Selects between CDMA and FM mode. This is a digitally controlled input. A logic “high” ($\geq V_{CC}$-0.3V_{DC}) selects CDMA mode. A logic “low” (<0.3V_{DC}) selects FM mode. In FM mode, this switch enables the FM amplifier and turns off the I&Q modulator. The impedance on this pin is 30kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	

Pin	Function	Description	Interface Schematic
47	VCC3	Supply voltage for the AGC and the Bandgap circuitry. A 1nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
48	BG OUT	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 1nF external bypass capacitor is required.	

RF2668 Pin-Out

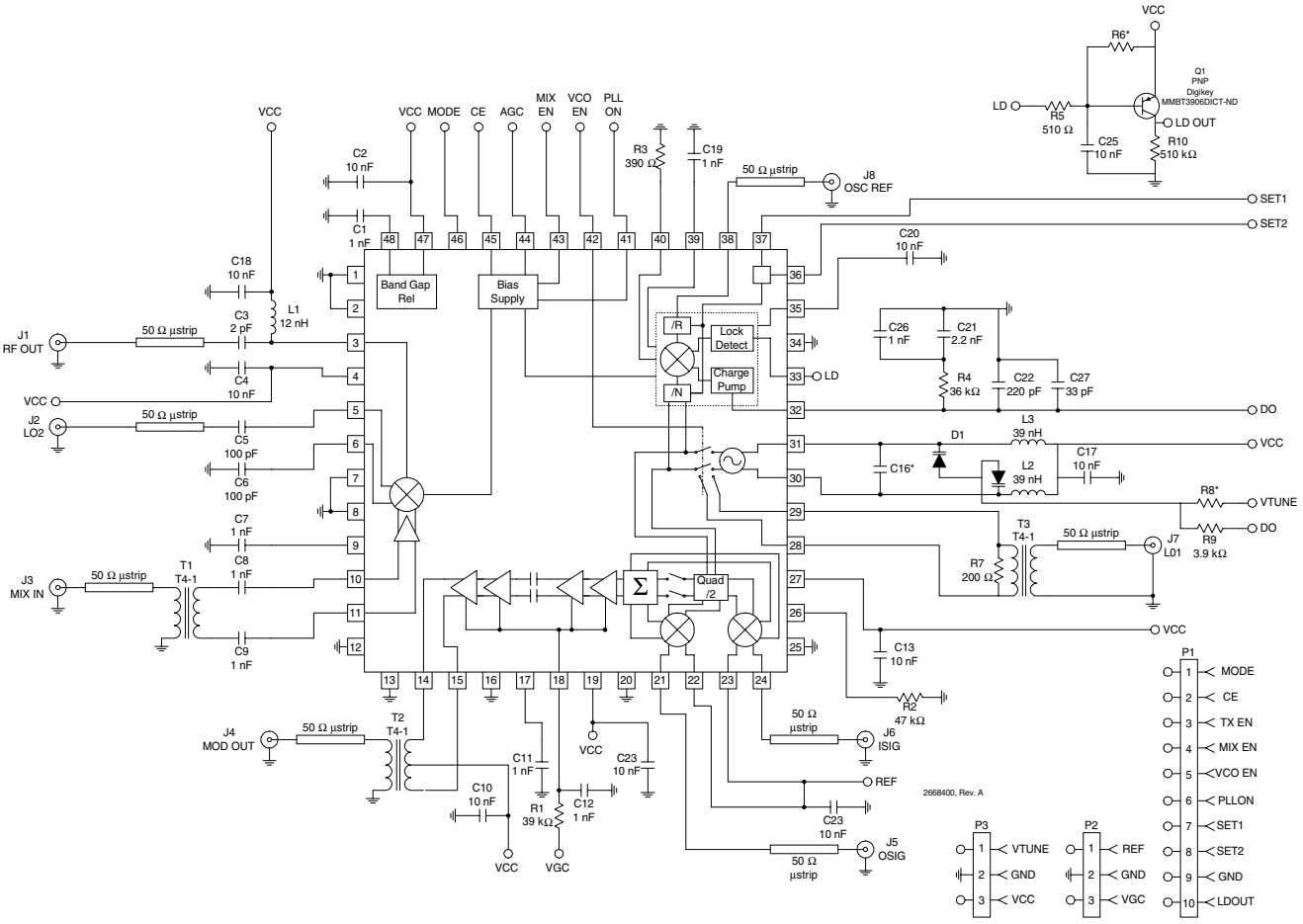


Application Schematic

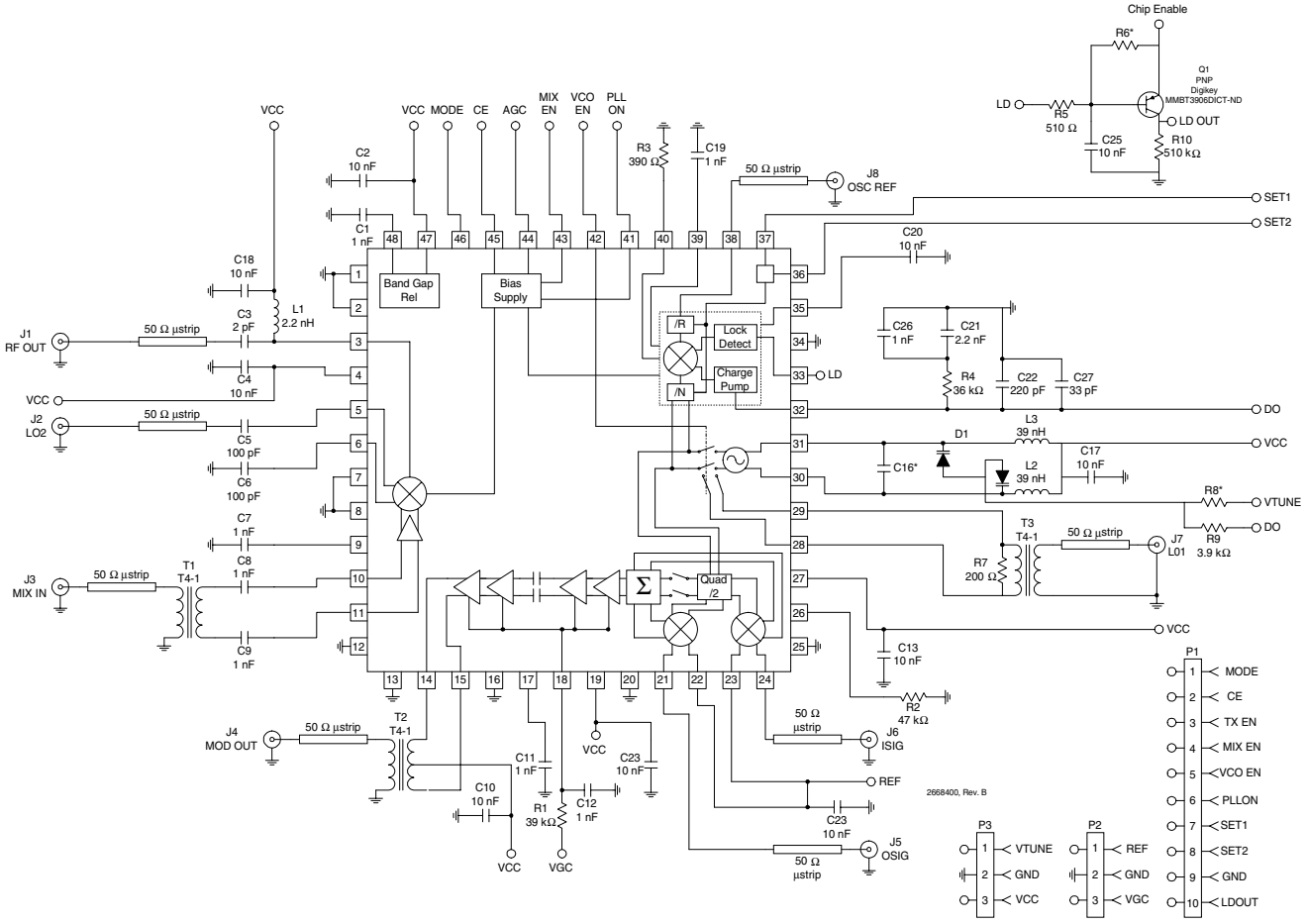


Evaluation Board Schematic
RF_{OUT}=830MHz

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Schematic
RF_{OUT} = 1950 MHz



Evaluation Board Layout
2.5" X 2.2"

Board Thickness 0.031”, Board Material FR-4