RF9986

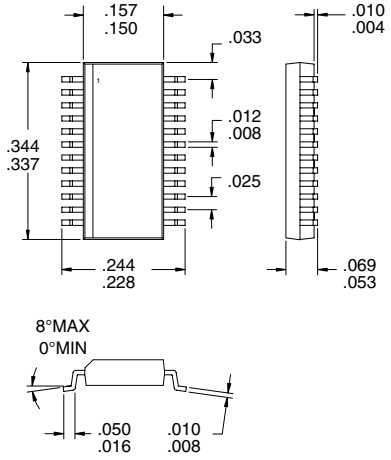
PCS LOW NOISE AMPLIFIER/MIXER

Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- General Purpose Down Converter
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

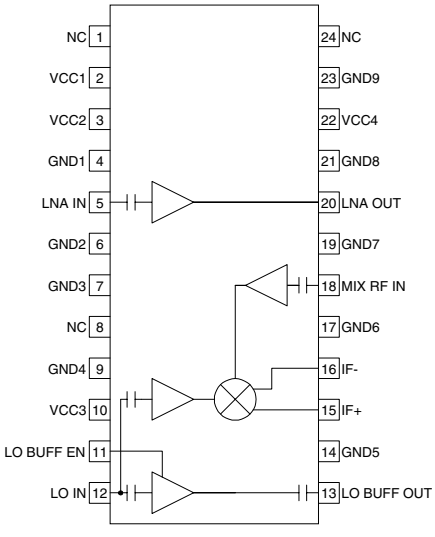
The RF9986 is a monolithic integrated receiver front-end for PCS, PHS, and WLAN applications. The IC contains all of the required components to implement the RF functions of the receiver front-end except for the passive filtering and LO generation. It contains an LNA (low-noise amplifiers), a double-balanced Gilbert cell mixer, a balanced IF output, an LO isolation buffer amplifier, and an LO output buffer amplifier for providing the buffered LO signal as an output. The IC is designed to operate from a single 3.6V power supply.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Extremely High Dynamic Range
- Single 3.6V Power Supply
- External LNA IP3 Adjustment
- 1500MHz to 2500MHz Operation

Ordering Information

RF9986	PCS Low Noise Amplifier/Mixer
RF9986 PCBA	Fully Assembled Evaluation Board

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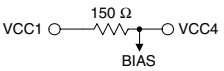
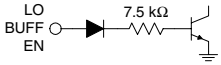
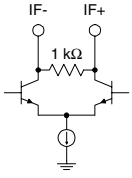
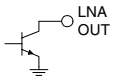
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

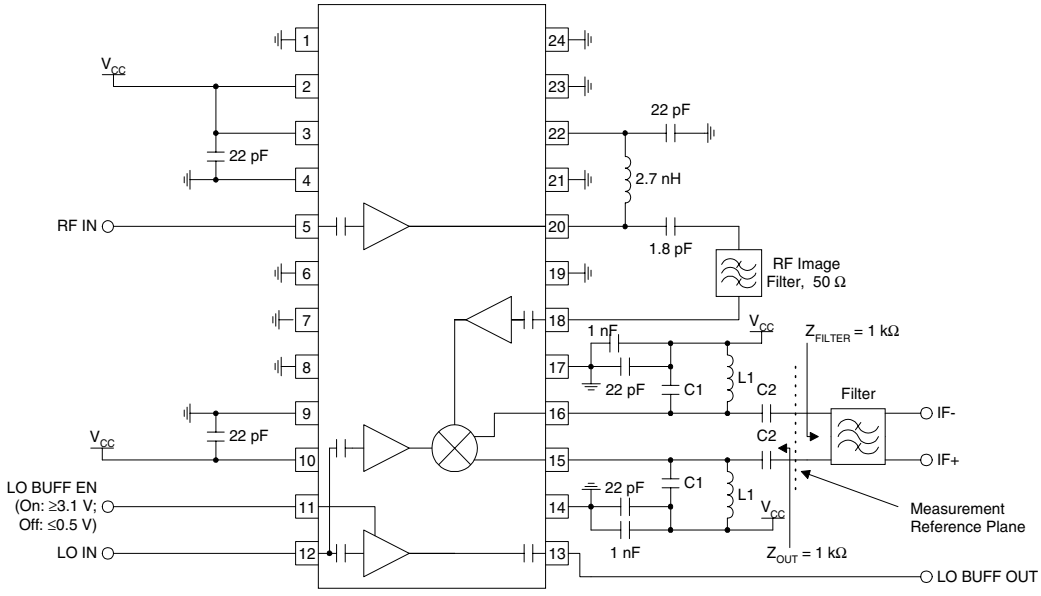
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T = 25°C, V_{CC} = 3.6V, RF = 1959MHz, LO = 1749MHz @ -2dBm
RF Frequency Range		1500 to 2500		MHz	
LO Frequency Range		1200 to 2500		MHz	
IF Frequency Range		DC to 500		MHz	
Cascaded Performance					1kΩ balanced load, 2.5dB Image Filter Loss.
Cascade Conversion Gain		25		dB	
Cascade Input IP3		-10		dBm	
Cascade Noise Figure		2.5		dB	Single Sideband
First Section (LNA)					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.4		dB	
Input VSWR		<2:1			Input is internally matched for optimum noise figure from a 50Ω source.
Input IP3		+5.5		dBm	IP3 may be increased 10dB by connecting pin 22 to V_{CC} through the matching inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made. See pin description for pin 20.
Gain		12		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			
Second Section (Mixer)					With 1kΩ balanced load.
Noise Figure		5.5		dB	Single Sideband
Input VSWR		1.5:1			
Input IP3		-0.5		dBm	
Conversion Gain		15.5		dB	
Output Impedance		1		kΩ	Balanced
LO Input					
LO Input Range		-5 to +3		dBm	
LO Output Level		-4		dBm	Buffer On, -2dBm input
		-25		dBm	Buffer Off, -2dBm input
LO to RF (Mix In) Rejection		30		dB	
LO to IF1, IF2 Rejection		20		dB	
LO Input VSWR		<2:1			Single ended
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		5		mA	LNA only
		52		mA	LNA + Mixer, LO Buffer On
		48		mA	LNA + Mixer, LO Buffer Off

Pin	Function	Description	Interface Schematic
1	NC	No Connection. This pin may be grounded (recommended) or left open.	
2	VCC1	Supply Voltage for the Mixer and RF Buffer Amplifier. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
3	VCC2	Supply Voltage for the LNA. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
4	GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA IN	RF Input pin for the LNA. This pin is internally DC blocked and internally matched for minimum noise figure (NOT for minimum VSWR), given a 50Ω source impedance.	
6	GND2	Same as pin 4.	
7	GND3	Ground connection for the RF Buffer Amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
8	NC	No Connection. This pin may be grounded (recommended) or left open.	
9	GND4	Same as pin 7.	
10	VCC3	Supply voltage for both LO buffer amplifiers. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	LO BUFF EN	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" (≥3.1V) turns the buffer amplifier on, and the current consumption increases by 3mA (with -2dBm LO input). A logic "low" (≤0.5V) turns the buffer amplifier off.	
12	LO IN	Mixer LO Input pin. This pin is internally DC blocked and matched to 50Ω.	
13	LO BUFF OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 11.	
14	GND5	Ground connection for both LO buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance.	
15	IF+	Open-collector IF Output pin. This is a balanced output. The output impedance is set by an internal 1000Ω resistor to pin 16. Thus the differential IF output impedance is 1000Ω. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
16	IF-	Same as pin 15, except complementary output.	See pin 15.
17	GND6	Ground connection for the Mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
18	MIX RF IN	Mixer RF Input Pin. This pin is internally DC blocked and matched to 50Ω.	
19	GND7	Same as pin 17.	

20	**LNA OUT**	LNA Output pin. This is an open-collector output. This pin is typically connected to pin 22 through a bias/matching inductor. This inductor, in conjunction with a series blocking/matching capacitor, forms a matching network to the 50Ω image filter and provides bias (see Application Example). The LNA's IP3 may be increased 10dB by connecting pin 20 to V_{CC} through the inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made by connecting resistance values between V_{CC} and the matching inductor. The two reference points for consideration are with 150Ω used, which is what connection to pin 22 achieves, the Input IP3 is +5.5dBm and the LNA I_{CC} is 5mA. Using no resistance, the Input IP3 is +15.5 dBm and the LNA I_{CC} is 15 mA. Desired operating points in between these values may be interpolated, roughly.	
21	**GND8**	Same as pin 17.	
22	**VCC4**	Output supply voltage for the LNA Output (pin 20). This pin is typically connected to pin 20 through a bias/matching inductor (see Application Example). External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	See pin 2.
23	**GND9**	Same as pin 17.	
24	**NC**	No Connection. This pin may be grounded (recommended) or left open.	

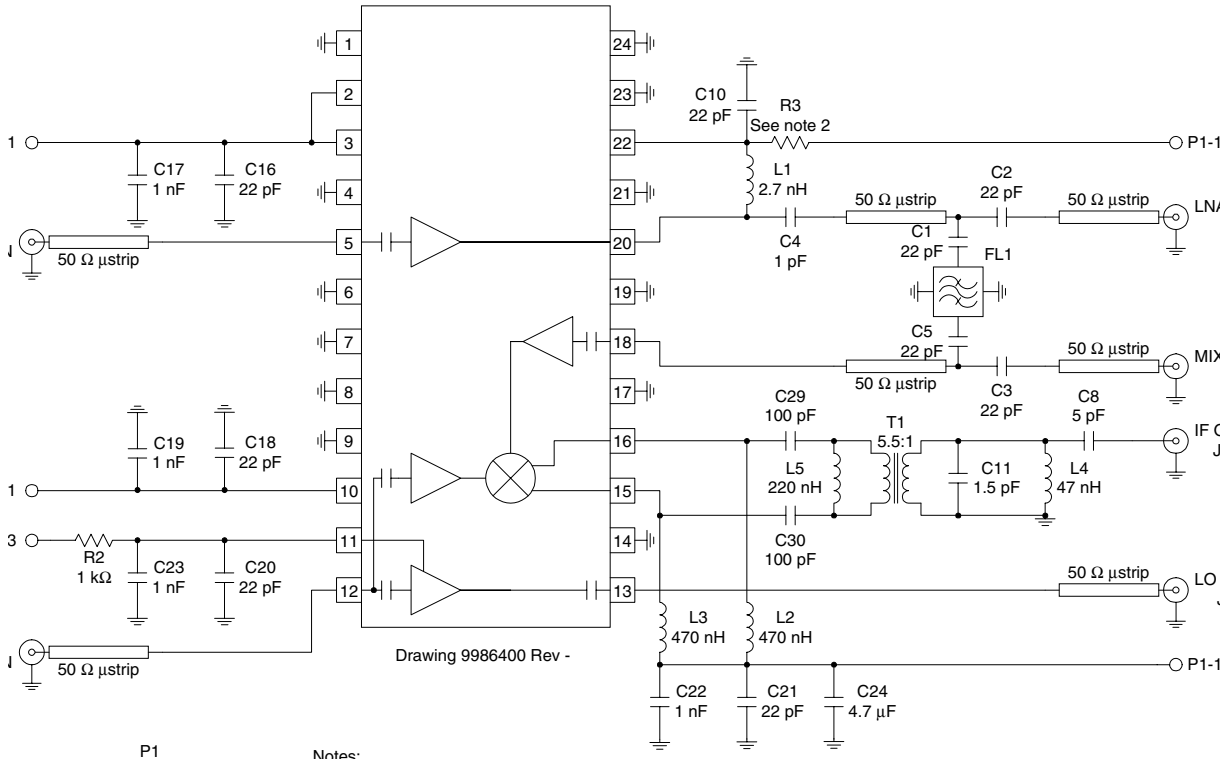
Application Schematic

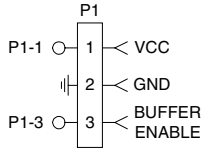


L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the IF filter's input impedance is not 1000Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circut at the IF when the IF filter's input impedance is 1000Ω.

Evaluation Board Schematic (IF=210MHz)

(Download Bill of Materials from www.rfmd.com.)

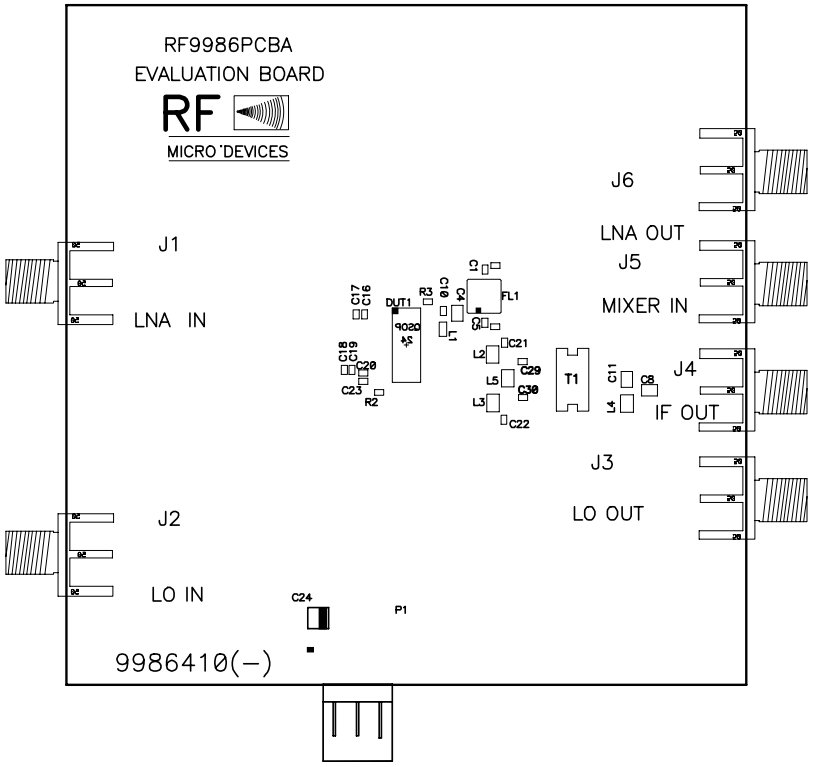




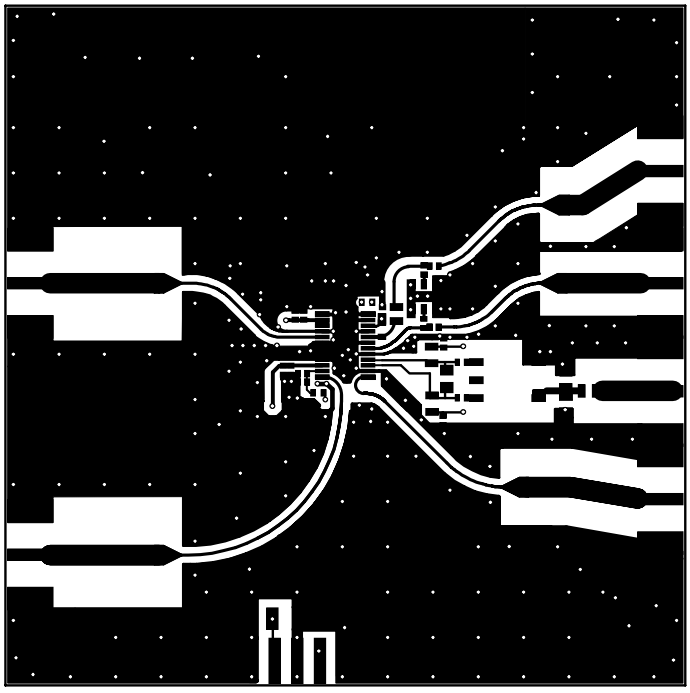
Notes:

1. C11 is selected to fine tune L4 for IF output match at 210 MHz.
2. R3 is not normally populated. For applications requiring additional LNA IP3, see the data sheet for recommended resistance values.
3: C2 and C3 are not normally populated. If C2 and C3 are populated, the LNA and mixer can be tested independently; in this case, C1 and C5 should be removed.

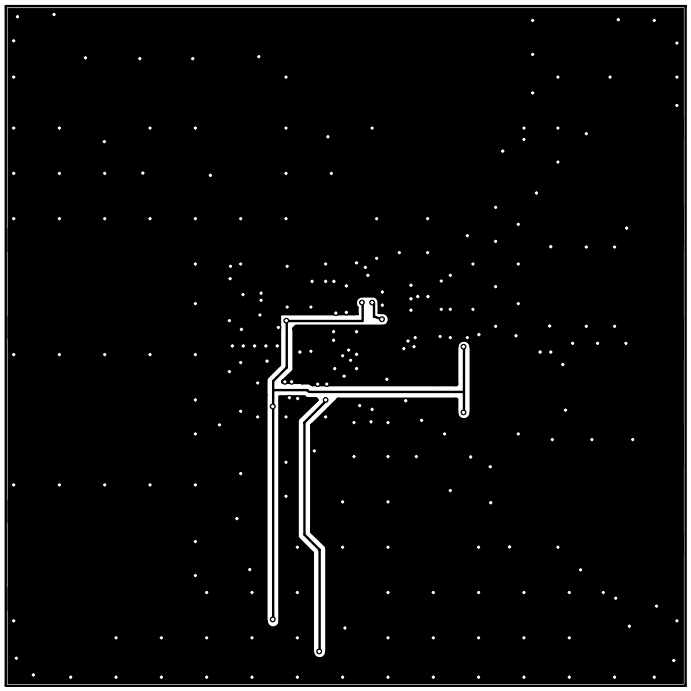
Evaluation Board Layout
3” x 3”
Assembly



Top layer



Bottom Layer



Internal Ground