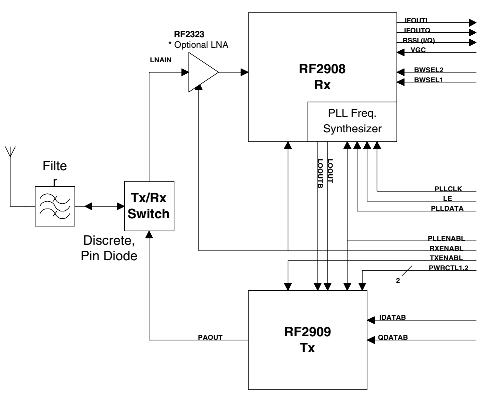
RF290X Digital Cordless Telephone Evaluation Kit

Product Description

The RF290X is an RF printed circuit board assembly (PCBA) intended to serve as a reference design for an RF module targeted for digital cordless telephone application. The RF290X PCBA includes the RF2908 Receiver/Synthesizer IC and the RF2909 Modulator/Transmitter IC that provide a two-chip monolithic radio solution of spread spectrum systems operating in the North American 902MHz to 928MHz ISM band under FCC Part 15.247. The chip-set is optimized for Time Division Duplex (TDD) applications. A block diagram of the radio is shown in Figure 1. The evaluation kit includes software and a cable for programming the PLL frequency synthesizer through the parallel port of a PC. RF shields for the PCBA are also included in the kit. Key features associated with the RF290X are as follows.

- RF290X Key Features
- 2-Chip Time-Division-Duplex (TDD) Transceiver Solution
- Compatible with Direct Sequence and Frequency Hop Spread Spectrum (DSSS/FHSS) Systems operating under FCC Part 15.247
- 2.7V to 3.6V Supply Voltage Range (2 Cell or 3 Cell Compatible)
- 50mW (@Antenna) Transmit Power
- Digital or Analog Tx Power Control
    - 3 Digitally Programmable Tx Levels (0dBm, 10dBm, 17dBm)
    - Analog Tx Level Control (1mW to 50mW)
    - QPSK/BPSK Linear Modulator
- Direct Conversion Receiver Architecture
- No Image Filter Required
- Quadrature RF Demodulator
- 1-Bit Stepped RF Gain Control for Adaptive IIP3
- 5-Pole On-chip Bessel Filter
- Dual (I&Q) Linear AGC or Limiting IF Output
- 86-Channel RF PLL Frequency Synthesizer
- On-Chip VCO (includes On-Chip Varactor)
- Serially Programmable
- Standard 3-Wire Interface

Figure 1: RF290X Evaluation PCB Block Diagram



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Initial Configuration

The RF290X PCBA can be configured to support a variety of applications and includes both selectable settings that can be configured through an SMT switch (SW1), and I/O components that can be changed with a soldering iron. The configuration of the PCBA can be optimized by the user to best address a given system requirement. Prior to applying power to the PCBA, it is recommended that the user become familiar with the configuration options that are described in the following sections.

Receiver Configuration

The following receiver settings are selectable by the user through the SW1 SMT switch:

4. Receiver Enable (RXENABL)
5. Receiver Baseband Bandwidth (0.96MHz, 1.92MHz, 3.84MHz, 9.6MHz)
6. RF2908 Front End Gain (IP3 Select)

The receiver electronics can be enabled by sliding SW1-6 to the right (toward the number 6) or by applying a logic high to P5-1.

Receiver Filter Configuration

Filtering in the receiver is accomplished in three filters:

1. Coaxial Resonator RF Filter (F1)
2. Dual 3-Pole Lumped Element LC Filters
3. On-Chip Selectable 5-Pole Bessel Filters

The coaxial resonator filter is recommended for rejection of large signal, out-of-band interferors. Other RF filters (SAW, LC, etc.) can be applied successfully with the chip-set. The selection of the RF filter will depend largely on the cost/performance goals of the end product. The coaxial resonator filter that is included on the RF2908X PCBA has a nominal -3dB bandwidth of 902MHz to 928MHz and an insertion loss of 2dB.

The receiver baseband bandwidth is established by the combination of dual lumped element LC-filters and dual 5-pole Bessel filters that are selectable on the RF2908. The combination of the LC filters and the on-chip filters establish the adjacent channel rejection of the receiver. For optimum performance in DSSS applications, the baseband cut-off frequency should be set to 0.7 to 0.8 times the chipping rate. The lumped element LC filters are populated at the factory with component values that provide a 0.96MHz 3-pole Bessel filter. Other filter bandwidths are possible and can be designed using the graphs provided in Figures 2 (Bessel filter values), 3a and 3b (Butterworth filter values). The PCBA components L6-9, C32, C33, C42, and C43 component values can be adjusted in accordance with Figures 2, 3a and 3b to provide the desired filter response and bandwidth. The dual, on-chip 5-pole Bessel filter bandwidths are selected by SW3 (BWSEL2) and SW4 (BWSEL1). Table 1 provides the control interface for selection of these bandwidths.

Figure 2: Bessel Filter Component Values (L in uH; C in pF; Freq. in Hz)

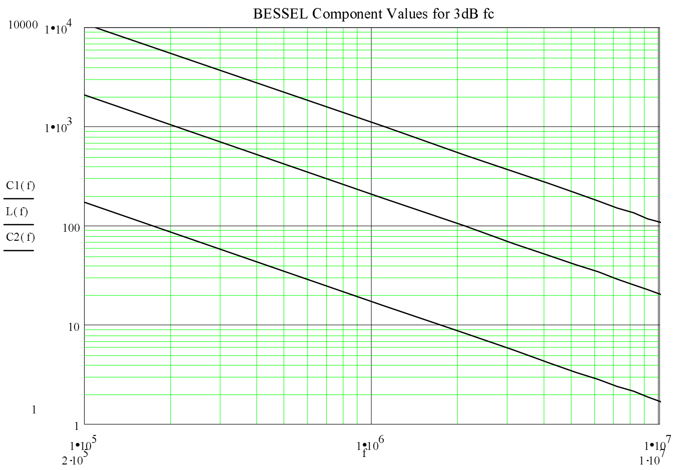

Figure 3a: Butterworth Filter Component Values (L in uH; C in pF; Freq. in Hz)

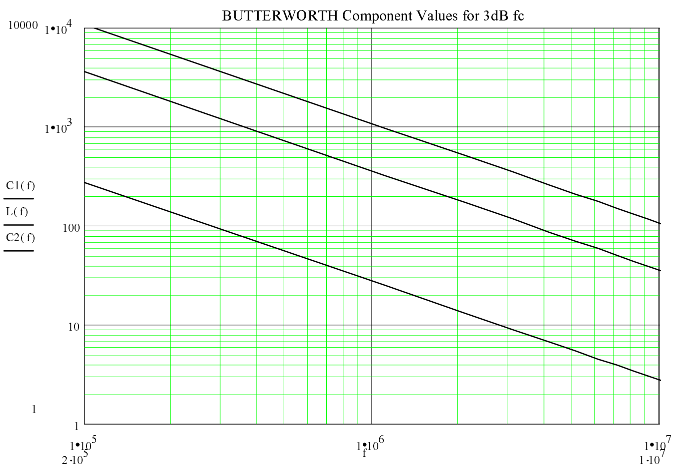

Figure 3b: External LC-Filter Circuit Architecture (For RF2908, Rs=125ohms-MOUTI/Q; R1=1kohm-INI/Q)

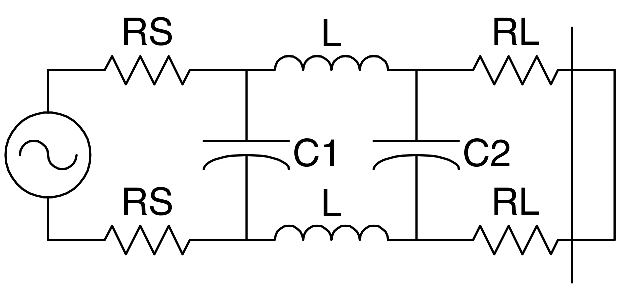

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Table1: On-Chip BW Control Logic

BWSEL1	BWSEL2	IF-3dB Bandwidth
Low	Low	960kHz
Low	High	1.92MHz
High	Low	3.84MHz
High	High	9.6MHz

Receiver Front End Configuration
The RF290X includes the RF2323 silicon low noise amplifier. By including the RF2323, the receiver system noise figure is improved by 4dB (5dB versus 9dB) over an implementation without the RF2323. The decision to use the RF2323 will depend largely on the cost/performance objectives of the product.

The RF2908 includes a 16dB switched attenuator that can be used to dynamically reduce the RF gain and increase the input IP3 of the RF2908. An example application for this switched attenuator might be in a digital cordless telephone application where the attenuator would be switched on to mitigate receiver desensitization from out-of-band large signal interference when the handset is within 100 feet of the base. Outside of the 100 foot radius, the attenuator would be switched off to maximize the range of the phone. The switched attenuator is enabled by SW1-7 on the PCBA.

Receiver IF Output Configuration
The following settings are hardwired on the PCB, but can be changed by moving or removing a component on the PCBA.

1. The I and Q channel IF linear outputs are connected as IF outputs (SMA connections J2 and J3). This configuration is intended for system applications that require a linear IF and utilize AGC. If the dual data comparators are not used, $V_{CC}3$ (Pin 20) should be disconnected (left open) to minimize noise degradation in the IF from the comparators.
2. For system applications that utilize IF limiting, and require a logic level baseband output, the dual data comparators can be used as 1-Bit A/D converters. The data comparators can be connected to the IF outputs by removing R12 and R10 and installing 0ohm resistors for R11 and R13.

Transmitter Configuration
The following transmitter settings are selectable by the user through the SW1 SMT switch.

1. Transmitter Enable (TXENABL)
2. Digital Tx Output Level (1mW, 10mW, 50mW P_{OUT})
3. Linear Tx Output Level Control (APC)

The transmitter electronics can be enabled by sliding SW1-5 to the right (toward the number 5) or by applying a logic high input voltage to P5-3.

Digital/Analog Transmit Output Power
The nominal peak output power from the part can be controlled digitally using the PWRCTRL1 (SW1-2) and PWRCTRL2 (SW1-1), or by using an analog input voltage at P1-3 (APC) for a continuously variable output level. In either case, the DC current consumption of the part will be optimized for selected output power.

Operating Mode	PWRCTRL1 (SW1-2)	PWRCTRL2 (SW1-1)	APC (P1-3)
Digital Low Power (1mW)	Low	Low	Low
Digital Med. Power (10mW)	High	Low	Low
Digital High Power (50mW)	Low	High	Low

Analog Power (1mW to 80mW)	Low	Low	0.5-V_{CC} (Max. APC input is 3.6V)

Best DC-RF efficiency at maximum output power is obtained when operating the RF2909 using APC control. For maximum output power, an APC input voltage of 2.8V provides the same RF output power as the Digital High Power state. With APC=2.8V, DC current consumption is approximately 40mA lower than the Digital High Power state.

The output power obtained will vary linearly with the modulation input voltage level applied to IDATAB (J4) and QDATAB (J5). Maximum output power (at a given level setting) will be achieved for an IDATAB and QDATAB input voltage level of 500mVp.

QPSK/BPSK Modulator

The RF2909 QPSK linear modulator is equally adept at BPSK and other PSK modulation techniques. To use the device as a BPSK modulator, the IDATAB (J4) and QDATAB (J5) should be wired (shorted) together. Data can then be input to the composite pin (J4/J5) to BPSK modulate the carrier.

Initial Power-Up of the RF290X Evaluation PCBA

The RF290X is designed to operate from a 3.3VDC+/-0.3VDC supply voltage. Three independent supply voltage connections must be made for proper operation of the PCBA. Although not required, it is a good practice to initialize these voltages simultaneously from a common power supply. It is also recommended that these voltage connections be made to the PCBA using twisted pair wiring.

V_{CC} Name	PCB Connection	Supply Voltage	Function
VBATT	P1-1	3.3V+/-0.3V	Supply voltage for the transmitter
PLLVCC	P5-1	3.3V+/-0.3V	Supply voltage for the PLL Frequency synthesizer and VCO
IFVCC	P4-1	3.3V+/-0.3V	Supply voltage for the receiver

The expected DC current consumption levels in the various operating modes are as shown in the table below.

RF290X Specifications

RF290X Cordless Telephone RF Module				
		Specification		
Parameter	**Min**	**Typical**	**Max**	**Units**
General Characteristics				
RF Frequency Range		902 to 928		MHz
Baseband Frequency Range		DC - 9.6		MHz
- Externally Programmable				
Receiver RF Characteristics				
Operating RF Frequency Band		902 to 928		MHz
Tangential Sensitivity (with RF2323)		-105		dBm
- IFBW=0.96MHz				
Tangential Sensitivity (without RF2323)		-101		dBm

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- IFBW=0.96MHz				
Noise Figure (with RF2323)		5		dB
Noise Figure (without RF2323)		9		dB
Input Third-Order Intercept Point				
- Minimum Gain (without RF2323)		-10		dBm
- Maximum Gain (without RF2323)		7.5		dBm
LO Leakage @ RFIN		-67		dBm
I/Q Phase Imbalance		+/-2		Deg
Baseband Lowpass Filter Cut-off		0.96		MHz
Baseband Highpass Filter Cut-off		0.1		MHz
Baseband Bandwidth Range		0.96 to 9.6		MHz
Transmitter RF Characteristics				
Output Power				
- Digital Low Power Mode		0.7		dBm
- Digital Med. Power Mode		9.5		dBm
- Digital High Power Mode		17.5		dBm
- Analog High Power Mode (V_{APC}=2.8V)		17.25		dBm
Harmonic Output			-25	dBm
Modulator LO Suppression (High Power)		-20		dBc
PLL Frequency Synthesizer				
RF Channels (902 to 928MHz)		85		
Step Size		300		kHz
VCO Tuning Range		120		MHz
Phase Noise				
@10kHz Offset/PLL BW=5kHz		-66		dBc
@100kHz Offset/PLL BW=5kHz		-96		dBc
Reference Frequency		9.6		MHz
Settling Time		1.5		msec
DC Power				
Supply Voltage Range (V_{CC})	3	3.3	3.6	V
I_{CC} - Receive (without RF2323)		55		mA
I_{CC} - Receive (with RF2323)		62		mA
I_{CC} - Transmit Digital Low Power Mode		78		mA
I_{CC} - Transmit Digital Med. Power Mode		89		mA
I_{CC} - Transmit Digital High Power Mode		236		mA

I_{CC} - Transmit Analog High Power Mode				
- V_{APC}=2.8V		196		mA
Supply Current (I_{CC}) - Sleep Mode		0.05		mA

Programming the PLL Frequency Synthesizer

The PLL Frequency synthesizer is programmed by connecting the parallel port of a PC to the 9-pin PCB connector with the cable provided. Prior to programming the PLL, PLLENABL should be connected logic high. This can be accomplished by sliding SW1-8 to the right (towards the 8) or by connecting P5-3 to V_{CC}.

The software used to program the PLL can be copied from the supplied diskette to the PC hard drive. The file RF2908.exe should then be executed from a DOS-shell. The program will prompt the user to enter the appropriate channel (swallow counter divisor). The table below provides a cross-reference for the specific data entry into the program to establish the desired operating frequency.

PLL Software Data Entry for Specific RF Operating Frequencies

Data	f,MHz	Data	f,MHz	Data	f,MHz	Data	f,MHz
0	902.4	22	909	44	915.6	66	922.2
1	902.7	23	909.3	45	915.9	67	922.5
2	903	24	909.6	46	916.2	68	922.8
3	903.3	25	909.9	47	916.5	69	923.1
4	903.6	26	910.2	48	916.8	70	923.4
5	903.9	27	910.5	49	917.1	71	923.7
6	904.2	28	910.8	50	917.4	72	924
7	904.5	29	911.1	51	917.7	73	924.3
8	904.8	30	911.4	52	918	74	924.6
9	905.1	31	911.7	53	918.3	75	924.9
10	905.4	32	912	54	918.6	76	925.2
11	905.7	33	912.3	55	918.9	77	925.5
12	906	34	912.6	56	919.2	78	925.8
13	906.3	35	912.9	57	919.5	79	926.1
14	906.6	36	913.2	58	919.8	80	926.4
15	906.9	37	913.5	59	920.1	81	926.7
16	907.2	38	913.8	60	920.4	82	927
17	907.5	39	914.1	61	920.7	83	927.3
18	907.8	40	914.4	62	921	84	927.6
19	908.1	41	914.7	63	921.3	85	927.9
20	908.4	42	915	64	921.6		
21	908.7	43	915.3	65	921.9		