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2000 DESIGNER'S HANDBOOK

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RF Solutions for the New Millenium

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1 Introduction And Selection Guide

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Product Application Selection Matrix

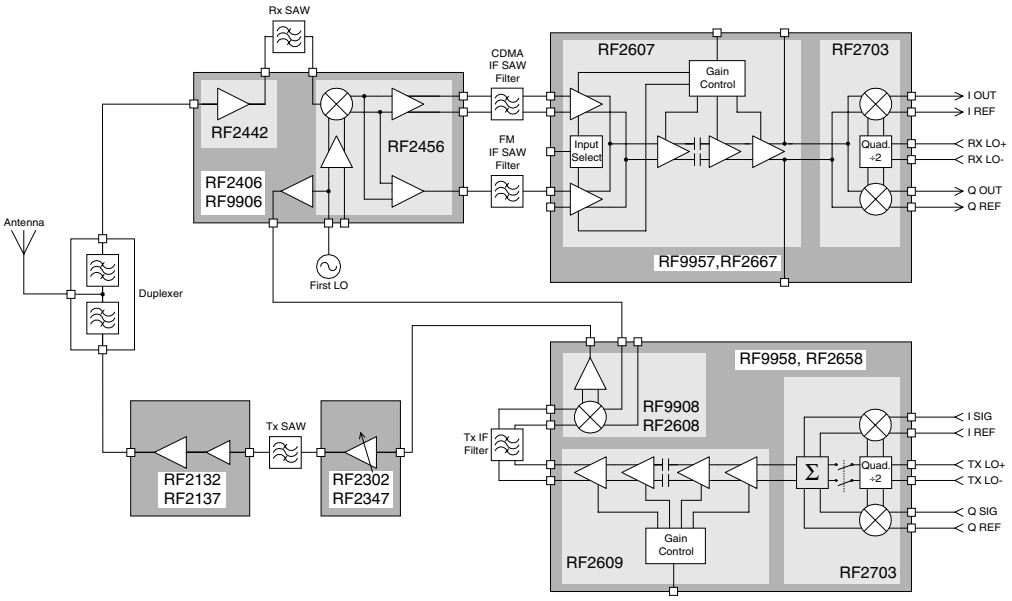
Application	Power Amplifier	Driver Amplifier	LNA/Mixer	Modulator/ Upconverter	Demodulator	IF/AGC	Transceiver	VCO/ Buffer
CDMA Cellular	RF2132 RF2137 RF2152 RF2162 RF2347	RF2303	RF2302 RF2347 RF2363 RF2406 RF2442 RF2449 RF2456 RF2642 RF9906	RF2608 RF2628 RF2658 RF9908 RF9958	RF2667 RF2711 RF9957	RF2607 RF2609 RF2617 RF2619 RF2627 RF2629	NA	RF2301
CDMA PCS	RF2125 RF2125P RF2126 RF2127 RF2146 RF2153 RF2157 RF2324	RF2303	RF2302 RF2363 RF2365 RF2442 RF2448 RF2445 RF9986	RF2638 RF2658 RF9938 RF9958	RF2667 RF2711 RF9957	RF2607 RF2609 RF2617 RF2619 RF2627 RF2629	NA	RF2301
WCDMA	RF2161	RF2303 RF2362	RF2463	RF2668	RF2667 RF9957	RF2667 RF2668 RF9957		
AMPS	RF2131 RF2137 RF2152 RF2119		RF2302 RF2363 RF2406 RF2411 RF2418 RF2442 RF2456	RF2608 RF2628 RF2658 RF9958	NA	NA	NA	RF2301
DCS1800 DCS1900	RF2126 RF2140 RF2145 RF2174		RF2302 RF2363 RF2365 RF2431 RF2442 RF2445 RF9936	RF2638 RF2639 RF2658 RF9938 RF9958	RF2667 RF2711 RF9957		NA	RF2301
GSM	RF2119 RF2138 RF2173		RF2302 RF2363 RF2406 RF2411 RF2418 RF2442	RF2402 RF2608 RF2628 RF2658 RF9958	RF2667 RF2711 RF9957		NA	RF2301 RF2504
ISM 433MHz	RF2103P RF2104 RF2105L RF2114 RF2115L RF2312 RF2317		RF2301 RF2302 RF2304 RF2401 RF2418	RF2412 RF2413 RF2454 RF2464	RF2667 RF2711 RF2903 RF9957	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629 RF2670	RF2510 RF2512 RF2513 RF2516 RF2905 RF2907 RF2915 RF2917 RF2919 RF2925 RF2926 RF2945	RF2301 RF2510 RF2512 RF2513 RF2516
ISM 868/915MHz	RF2103P RF2104 RF2105L RF2115L RF2119 RF2131 RF2132 RF2137 RF2152 RF2155 RF2172 RF2312 RF2317		RF2301 RF2302 RF2304 RF2314 RF2401 RF2406 RF2411 RF2418 RF2442 RF2456 RF2457 RF9936 RF9986	RF2402 RF2412 RF2413 RF2423 RF2608 RF2628 RF2638 RF2639 RF2658 RF2909 RF9908 RF9958	RF2667 RF2711 RF9957	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629 RF2670	RF2510 RF2512 RF2513 RF2905 RF2907 RF2908 RF2915 RF2917 RF2919 RF2925 RF2926 RF2945	RF2301 RF2504 RF2510 RF2512 RF2513 RF2516
ISM 2.4GHz	RF2126 RF2128 RF2129 RF2189		RF2301 RF2302 RF2304 RF2431 RF2442 RF9936 RF9986	RF2402 RF2412 RF2413 RF2422 RF2423 RF2454 RF2464 RF2608 RF2628 RF2638 RF2639 RF2658 RF2909 RF9908 RF9958	RF2667 RF2711 RF2903 RF9957	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629 RF2670	RF2938	RF2301 RF2510

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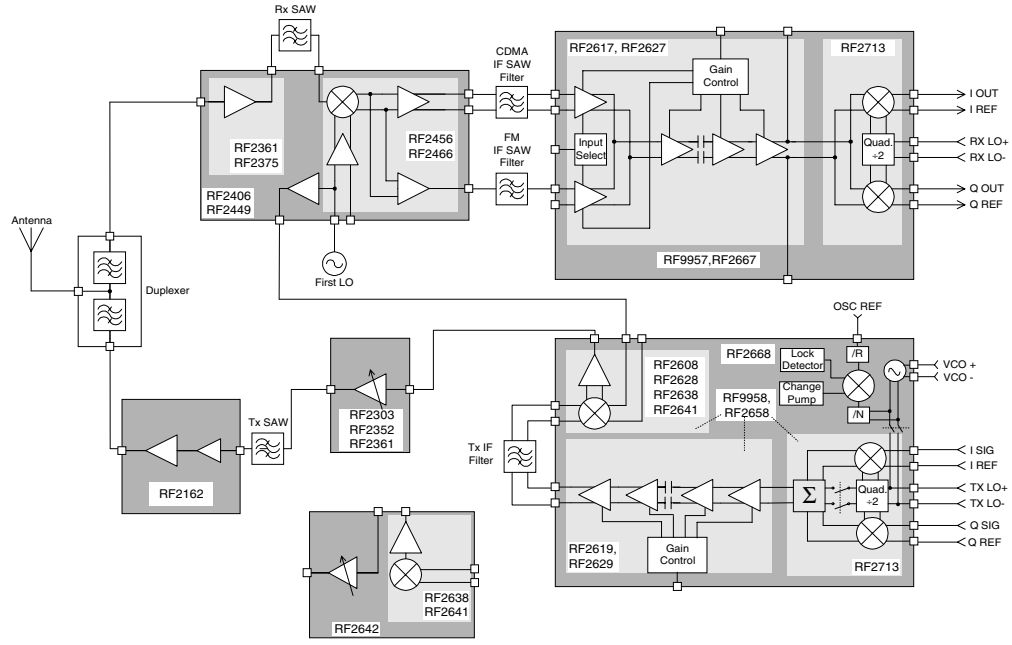
Application	Power Amplifier	Driver Amplifier	LNA/Mixer	Modulator/ Upconverter	Demodulator	IF/AGC	Transceiver	VCO/ Buffer
TDMA Cellular	RF2132 RF2137 RF2152 RF2162 RF2347		RF2302 RF2347 RF2406 RF2411 RF2442 RF9906	RF2402 RF2412 RF2413 RF2640 RF2658 RF9908 RF9958	RF2667 RF2711 RF9957	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629	NA	RF2301
TDMA PCS	RF2126 RF2127 RF2146 RF2153 RF2324		RF2302 RF2431 RF2442 RF2445 RF9936 RF9986	RF2422 RF2638 RF2639 RF2658 RF9938 RF9958	RF2667 RF2711 RF9957	RF2410 RF2420	NA	RF2301
Cable Modem	RF2312 RF2317		RF2302 RF2406 RF2411		RF2711	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629	-	RF2301 RF2504
Cable TV	RF2312 RF2317 RF2320 RF2360		NA	NA	NA	NA	NA	NA
Industrial Radio	RF2103P RF2104 RF2105L RF2114 RF2115L		RF2302 RF2401 RF2406 RF2411 RF2418 RF2442 RF2456	RF2412 RF2413 RF2454 RF2464 RF2608 RF2628 RF2658 RF9908 RF9958	RF2667 RF2711 RF9957	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629	-	RF2301 RF2504
Two-Way Paging	RF2119		RF2401 RF2411 RF2418	NA	NA	-	-	RF2301 RF2504
TETRA	RF2114 RF2132 RF2137		RF2302 RF2401 RF2406 RF2418 RF2442 RF2456	RF2464 RF2658 RF9958	RF2667 RF2711 RF9957	RF2410 RF2420 RF2607 RF2609 RF2617 RF2619 RF2627 RF2629	NA	RF2301
DECT	RF2145		RF2302 RF2431 RF2442 RF2445 RF9986		RF2667 RF2711 RF9957		NA	RF2301

System Block Diagrams

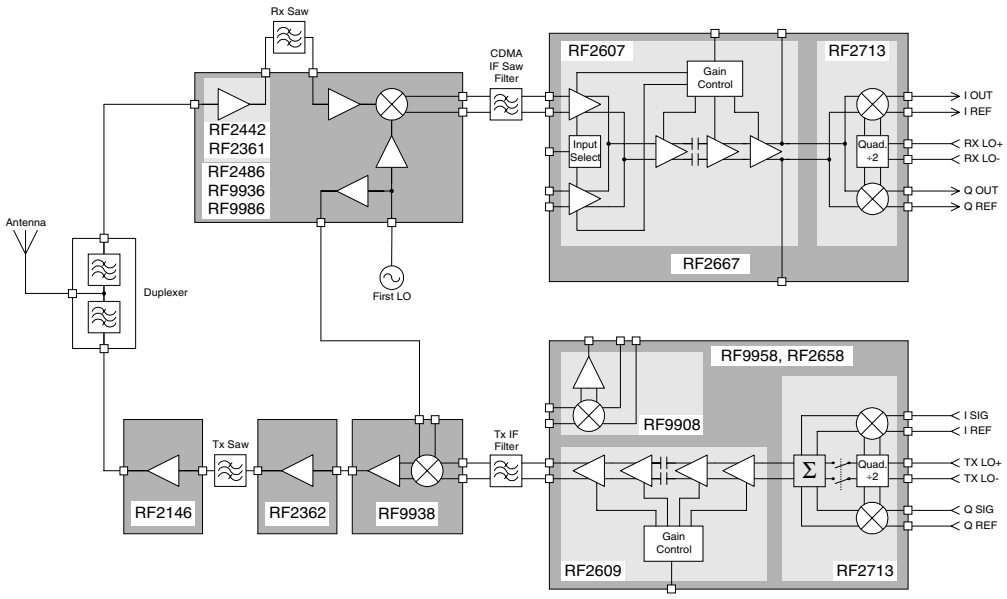
RFMD 3.6V/4.8V CDMA Cellular System Block Diagram



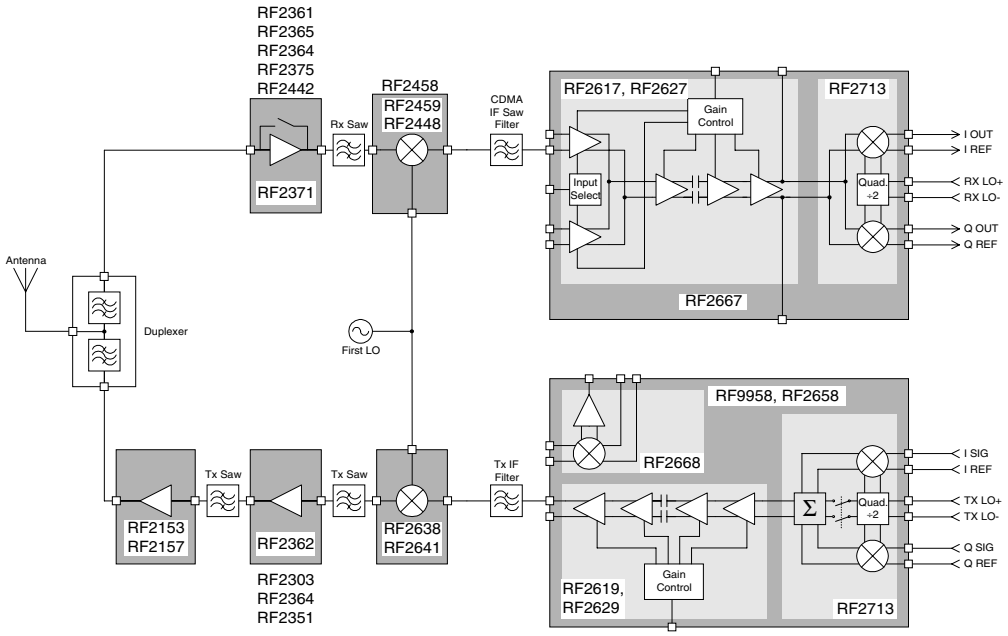
RFMD 3.0V CDMA Cellular System Block Diagram



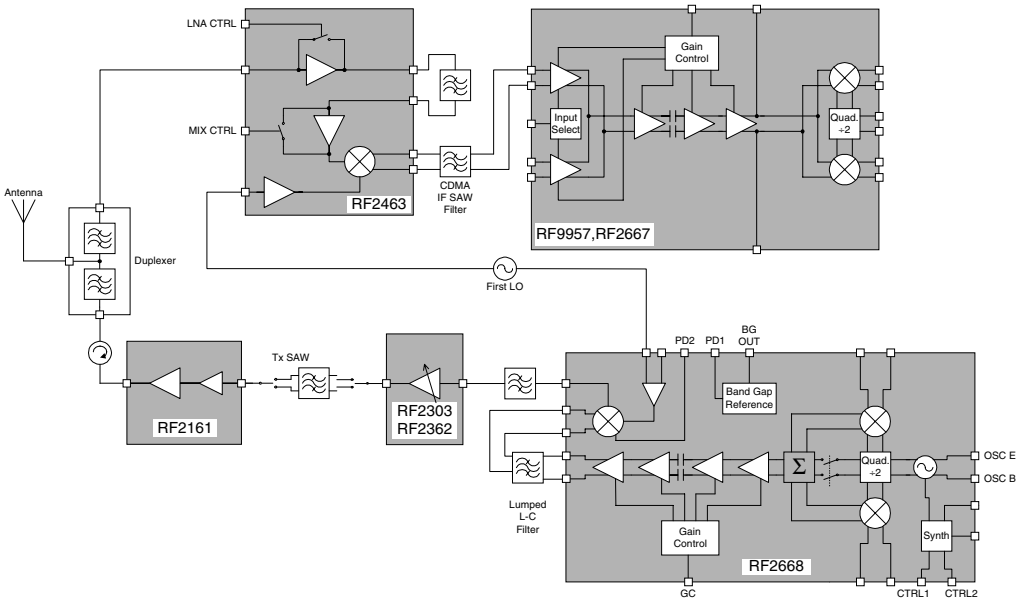
RFMD 3.6V/4.8V CDMA PCS
System Block Diagram



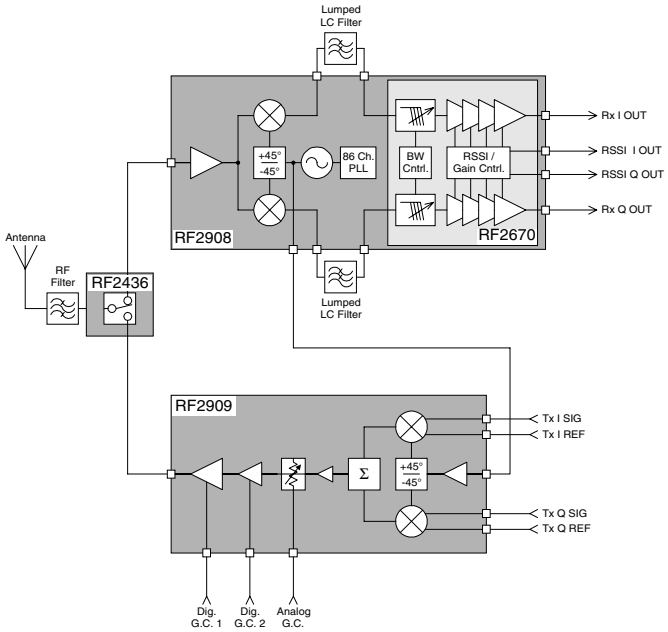
RFMD 3.0V CDMA PCS
System Block Diagram



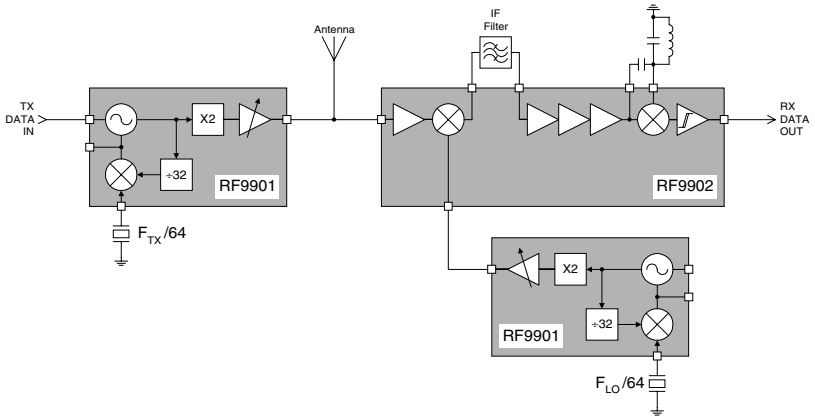
RFMD First Generation WCDMA Chipset Using Existing Products System Block Diagram



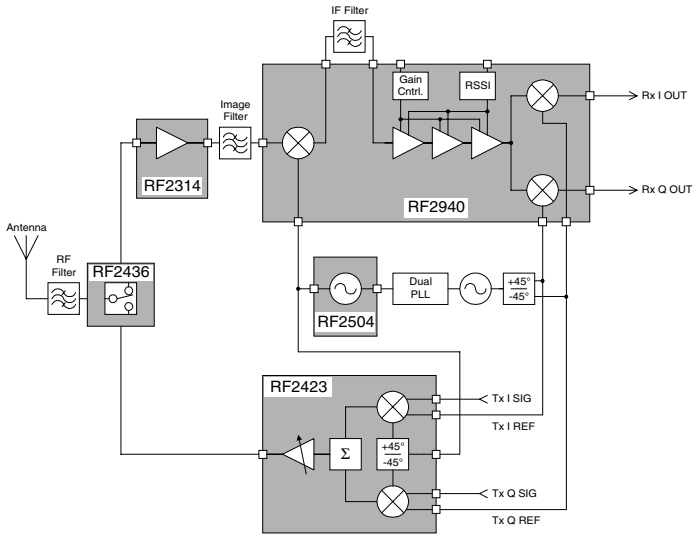
RFMD 915 MHz Spread Spectrum Chip Set System Block Diagram



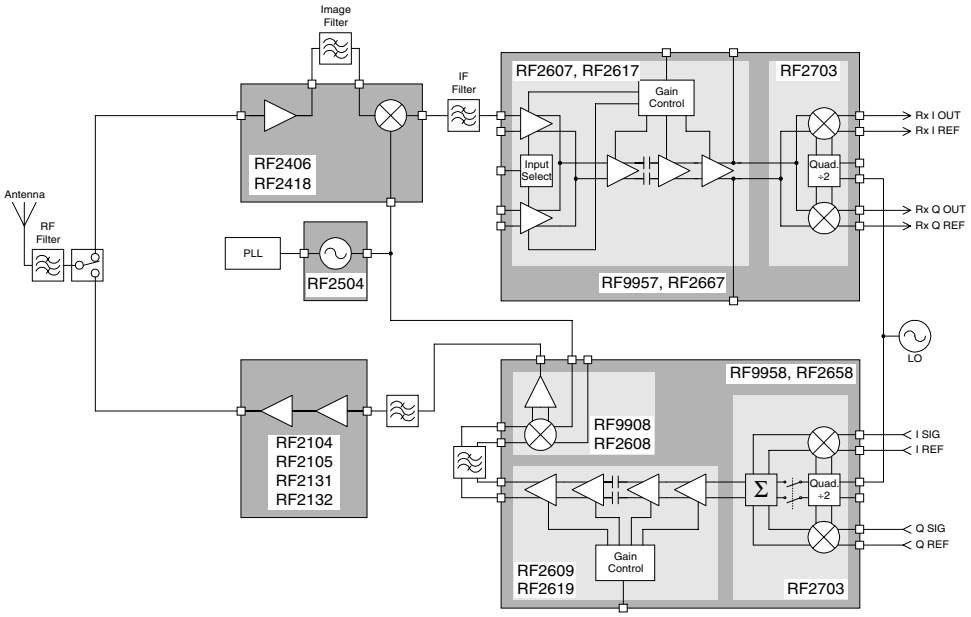
RFMD General Purpose FSK System Block Diagram



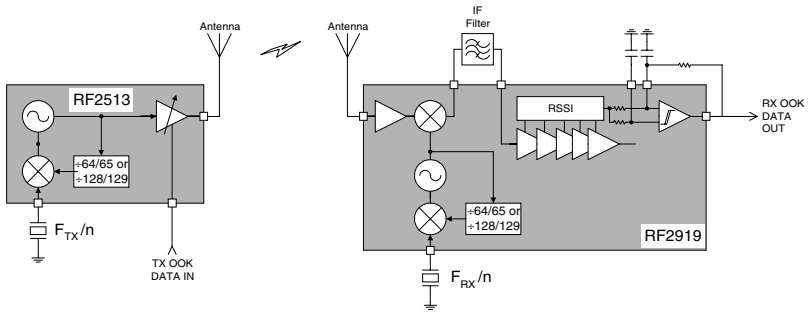
RFMD 915 MHz General Purpose Spread Spectrum System Block Diagram



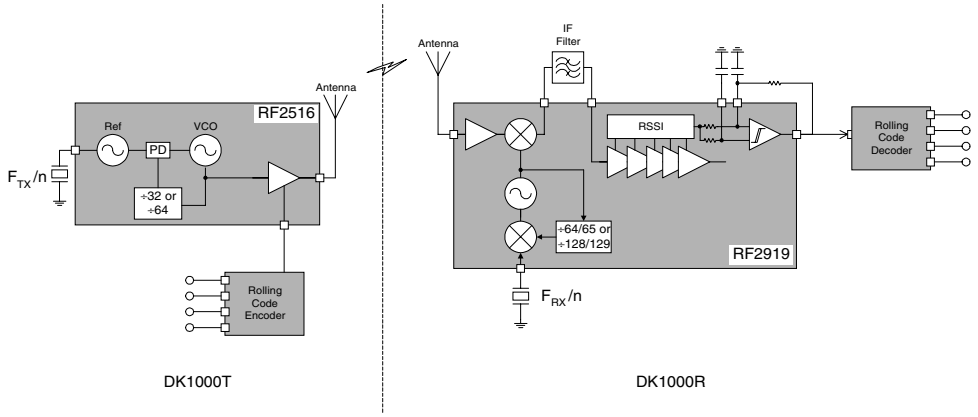
RFMD 915 MHz General Purpose Spread Spectrum System Block Diagram



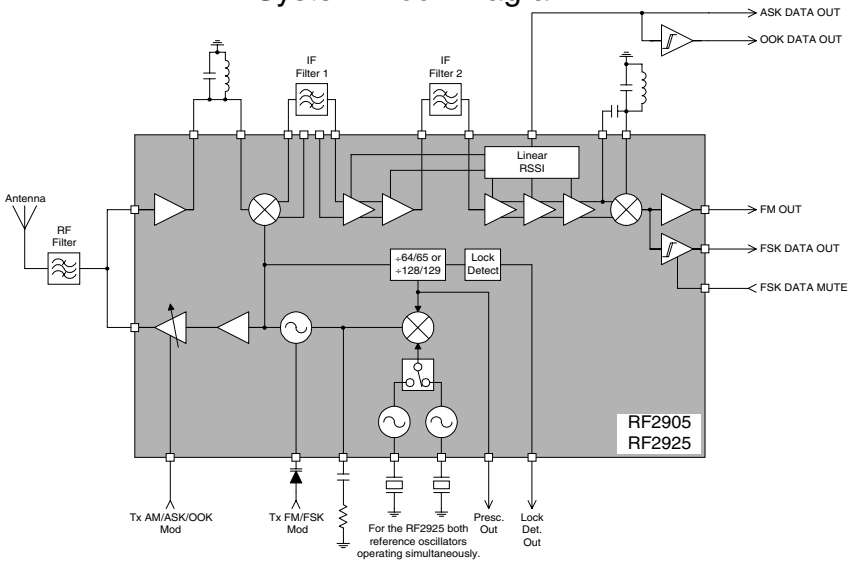
RFMD OOK Simplex Link System Block Diagram



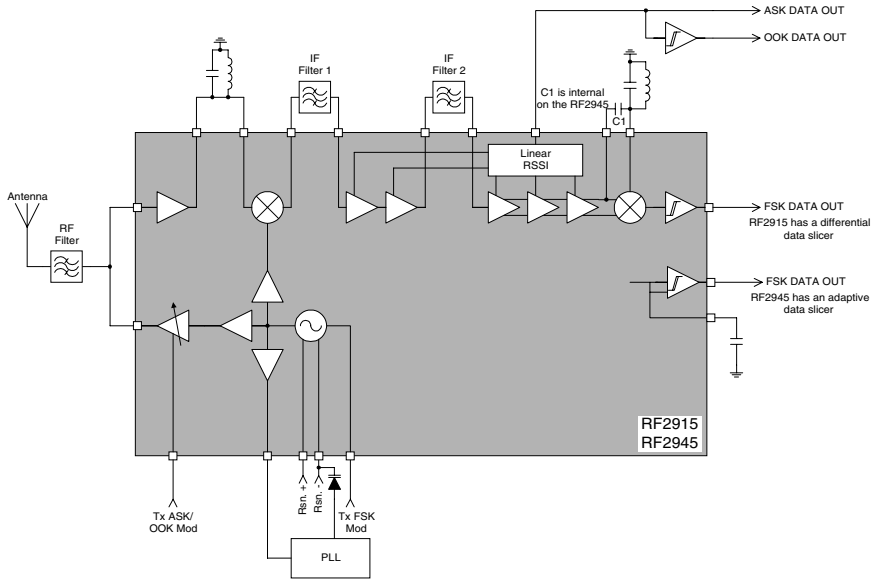
RFMD Remote Keyless Entry System Block Diagram



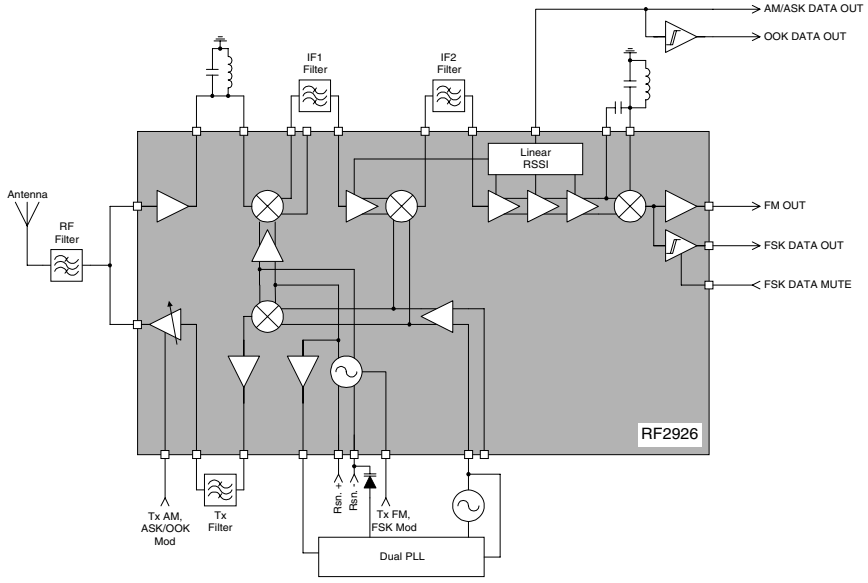
RFMD Single Chip 433/868/915 MHz Transceiver System Block Diagram



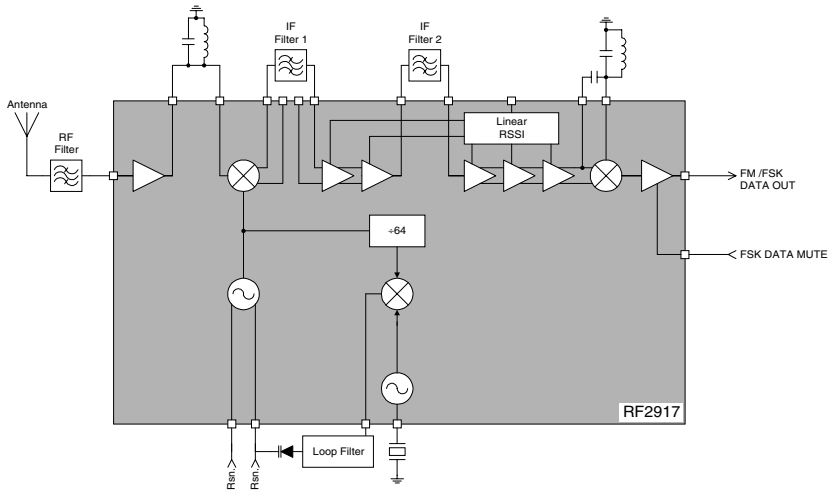
RFMD Single Chip 433/868/915 MHz FSK/ASK/OOK Transceiver System Block Diagram



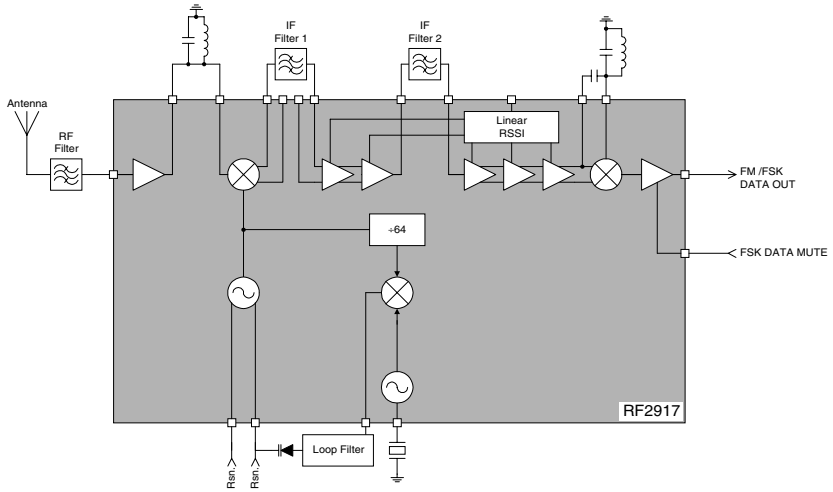
RFMD Single Chip 433/868/915 MHz FSK/ASK/OOK/FM/AM Dual Conversion Transceiver System Block Diagram



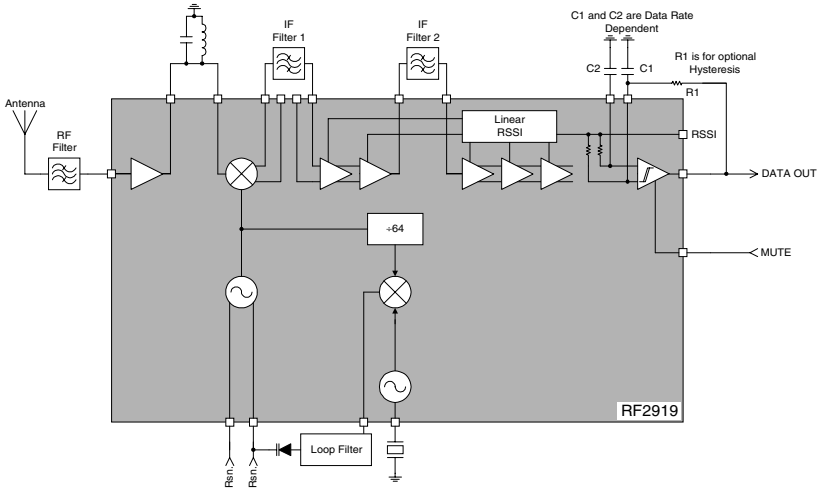
RFMD Single Chip 433/868/915 MHz FM/FSK Receiver System Block Diagram



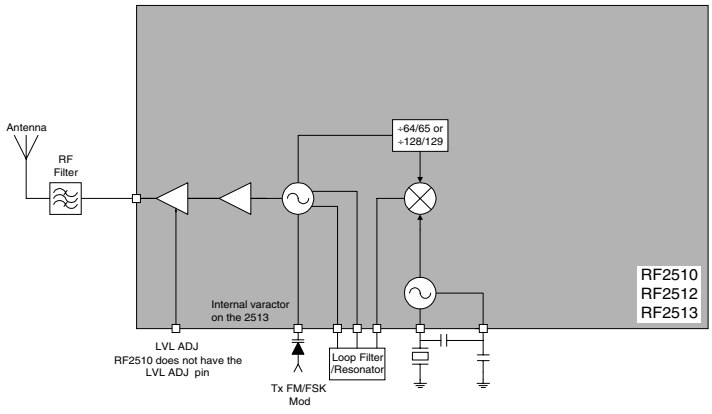
RFMD Single Chip 433/868/915 MHz FM/FSK Receiver System Block Diagram



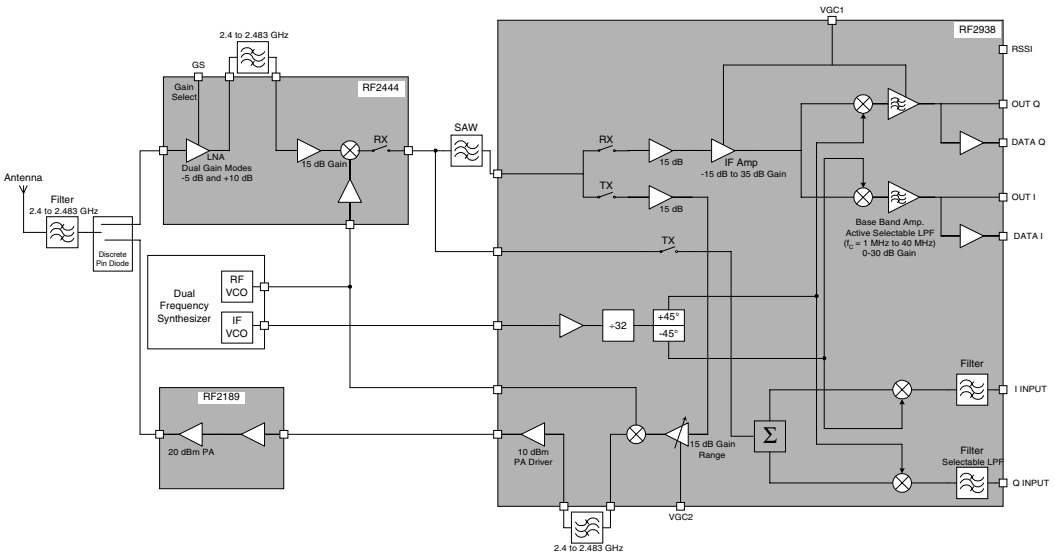
RFMD Single Chip 433/868/915 MHz ASK/OOK Receiver System Block Diagram



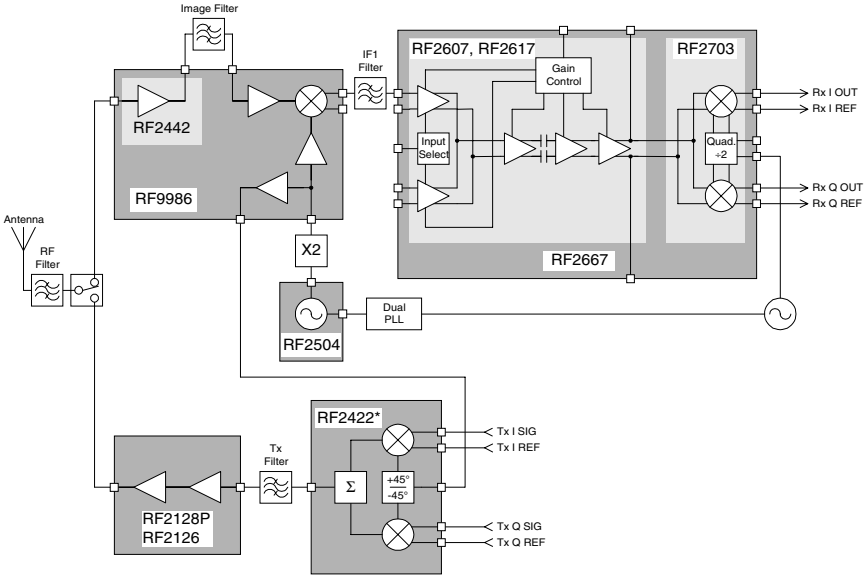
RFMD Single Chip 433/868/915 MHz FSK/FM Transmitter System Block Diagram



RFMD 2.4 GHz WLAN System Block Diagram



RFMD 2.4 GHz General Purpose System Block Diagram



Product Selection Guide

2 Power Amplifiers

Part	Description	Frequency (MHz)	Vcc (Volts)	Efficiency (%, Max)	Output Power	Package	Page
RF2103P	Medium Power Linear Amplifier	450 to 1000	2.7 to 7.5	47	750mW at 7.5V	SOP-14	2-1
RF2104	Medium Power Amplifier	400 to 1000	2.7 to 3.6	40	500mW at 3.6 V	SOP-16 QBW1	2-11
RF2105L	High Power Linear UHF Amplifier	430 to 930	2.7 to 6.5	48	1.2W at 5.8V	QLCC-16	2-19
RF2108	Linear Power Amplifier	800 to 950	4.2 to 7.5	57	1.4W at 4.8V	SOP-16 BW	2-27
RF2114	Medium Power Linear Amplifier	1 to 600	2.7 to 6.5	45	800mW at 5.8V	SOP-14	2-33
RF2115L	High Power UHF Amplifier	430 to 930	5.0 to 6.5	48	1.1W at 5.8V	QLCC-16	2-39
RF2117	High Efficiency 400MHz Amplifier	400 to 500	3.0 to 5.5	50		PSOP-16	2-47
RF2119	High Efficiency 2V Power Amplifier	800 to 960	2.0 to 5.0	53	2.0W at 3.0V	PSSOP-16	2-55
RF2125	High Power Linear Amplifier	1500 to 2200	2.7 to 7.5	45	1W at 6.0V	SOP-8-C	2-61
RF2125P	High Power Linear Amplifier	1500 to 2200	2.7 to 7.5	45	1W at 6.0V	PSOP-8	2-67
RF2126	High Power Linear Amplifier	1800 to 2500	3.0 to 6.5	45	1.3W at 6.0V	PSOP-8	2-73
RF2127	Medium Power Linear Amplifier	1500 to 1900	3.0 to 6.5	30	200mW at 6.0V	SOP-8	2-79
RF2128	Medium Power Linear Amplifier	1900 to 2500	3.0 to 6.5	30	200mW at 6.0V	SOP-8-C	2-85
RF2128P	Medium Power Linear Amplifier	1900 to 2500	3.0 to 6.5	33	200mW at 6.0V	PSOP-8	2-89
RF2129	3V, 2.5GHz Linear Power Amplifier	1800 to 2500	3.0 to 5.0	42	400mW at 3.3V	PSOP-8	2-93
RF2131	High Efficiency AMPS/ETACS Amplifier	800 to 950	4.0 to 7.0	64	1.2W at 4.8V	SOP-16 BW	2-99
RF2132	Linear Power Amplifier	800 to 950	4.2 to 6.0	55	1.6W at 4.8V	SOP-16 BW	2-109
RF2137	Linear Power Amplifier	800 to 950	4.2 to 6.0	55	1.6W at 5.0V	PSOP-8	2-115
RF2138	3V GSM Power Amplifier	800 to 950	2.7 to 4.8	58	4W at 3.5V	MP16K01A	2-119
RF2140	3V DCS Power Amplifier	1700 to 2000	2.7 to 4.8	51	2W at 3.5V	MP16K01A	2-129
RF2145	DCS1800/1900 Power Amplifier	1700 to 1900	2.7 to 6.5	55	1.6W at 4.8V	SOP-16 QBW1	2-141
RF2146	PCS Linear Power Amplifier	1500 to 2000	4.0 to 6.5	37	700 mW at 4.8V	SOP-16 QBW1	2-147
RF2152	Dual-Mode CDMA/AMPS or TDMA/AMPS 3V Power Amplifier	800 to 960	3.0 to 5.2	36/45	500 mW/1.1W at 3V	PSSOP-16	2-155
RF2153	CDMA/TDMA/PACS 1900MHz 3V Power Amplifier	1750 to 1910	3.0 to 4.5	40	800mW at 3.4V	MP16K01A	2-167
RF2155	3V Programmable Gain Power Amplifier	430 to 930	3.0 to 5.0	56	450mW at 3.6V	SOP-16 BW	2-179
RF2157	PCS CDMA/TDMA 3V Power Amplifier	1750 to 1910	3.0 to 4.5	35	800 mW at 3.4V	MLF16	2-187
RF2161	3V WCDMA Power 1900MHZ 3V Linear Power Amplifier	1850 to 2000	3.4	36	27dBm	MP16K01A	2-197
RF2162	3V 900MHz Linear Amplifier	800 to 960	3.4	35	800mW at 3.4V	MLF16	2-205
RF2172	900MHz ISM Band 3.6V, 250mW Amp with Analog Gain Control	902 to 928	3.0 to 3.6	58	24dBm at 3.6V	MLF16	2-213
RF2173	3V GSM Power Amplifier	800 to 950	2.7 to 4.8	56	36dBm at 3.5V	MLF16	2-221
RF2174	3V DCS Power Amplifier	1700 to 1950	2.7 to 4.8	51	33dBm at 3.5V	MLF16	2-231
RF2175	3V 400MHz Linear Amplifier	380 to 512	3.0 to 5.2	30	34dBm at 3.6V	PSSOP-16	2-243
RF2189	3V, 2.5GHz Linear Power Amplifier	1800 to 2500	3.0 to 5.0	42	26dBm at 3.3V	MLF16	2-249

3 Linear CATV Amplifiers

Part	Description	Frequency (GHz)	Vcc (Volts)	Icc (mA)	Isolation (dB)	Gain (dB)	NF (dB)	P1dB (dBm)	Package	Page
RF2312	Linear General Purpose Amplifier	DC to 2.5	5 to 12	40 to 115	20	15	3.8	+22	SOP-8	3-1
RF2317	Linear CATV Amplifier	DC to 3.0	12to15	100 to 200	20	14.5	4.9	+26	SOP-16 QBW1	3-13
RF2318	Linear Broadband Amplifier	DC to 5.0	9 to 12	50 to 65	15	8	6		SOP-8	3-21
RF2320	Linear General Purpose Amplifier	0.005 to 2.5	6 to 9	75 to 100	20	16	1.6	+22.5	SOP-16BW	3-27
RF2360	Linear General Purpose Amplifier	0.005 to 1.5	6 to 9	100	24	20	1.2	+24	SOP-16BW	3-37

4 General Purpose RF Amplifiers

Part	Description	Frequency (GHz)	Vcc (Volts)	Icc (mA)	Isolation (dB)	Gain (dB)	NF (dB)	P1dB (dBm)	Package	Page
RF2043	General Purpose Amplifier	DC to 6	5 to 6	70	16.5	11	7.6	+18.5	MicroX-CF	4-1
RF2044	General Purpose Amplifier	DC to 6	4.3 to 5.3	65	22	20	4.1	+18.5	MicroX-CF	4-7
RF2045	General Purpose Amplifier	DC to 6	4.6 to 5.6	65	18	14	5.0	+18	MicroX-CF	4-13
RF2046	General Purpose Amplifier	DC to 3	3 to 4	35	23	22	3.8	+12	MicroX-CF	4-19
RF2047	General Purpose Amplifier	DC to 6	3 to 4	40	19	16	4.2	+12	MicroX-CF	4-25
RF2048	General Purpose Amplifier	DC to 8	3 to 4	40	16.5	12	5.3	+12	MicroX-CF	4-31
RF2301	High Isolation Buffer Amplifier	0.3 to 2.5	2.7 to 6	18	50	21	8.0	+4	SOP-8	4-37
RF2302	Broadband Linear Variable Gain Amplifier	0.1 to 2.0	3.0 to 6.0	35		-11to14	4	+14	MSOP-8	4-43
RF2303	Broadband Linear Variable Gain Amplifier	0.1 to 2.0	3.0 to 6.0	25	35	-2 to 23	4	+16	MLF16	4-51
RF2304	General Purpose Low-Noise Amplifier	0.3 to 2.5	2.7 to 6.0	5 to 26	18	8	1.8	+6	SOP-8	4-57
RF2306	General Purpose Amplifier	DC to 2	>3.7	20 to 65	20	20	3.5	+12	SOP-8	4-63
RF2307	General Purpose Amplifier	DC to 3	>3.7	20 to 65	18	15	4.0	+14	SOP-8	4-67
RF2308	General Purpose Amplifier	DC to 4	>3.7	20 to 65	15	12	5.0	+13	SOP-8	4-71
RF2310	Wideband General Purpose Amplifier	DC to 2.5	3.5 to 6.0	20 to 65	20	15	5.0	+19	SOP-8	4-75
RF2311	General Purpose Amplifier	DC to 1.6	2.7 to 6.0	8 to 17	20	14	4.0	+8	SOP-8	4-81
RF2314	General Purpose Low Noise Amplifier	0.15 to 2.5	2.7 to 6.0	5 to 25	20	14	1.4	+8	SOT-23-5	4-87
RF2321	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	8	36	12	3.7	-7	SOT-23-5	4-91
RF2322	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	8	38	19	3.3	-7	SOT-23-5	4-99
RF2323	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	7	33	21	2.3	-7	SOT-23-5	4-107
RF2324	PCS CDMA/TDMA 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	24 to 43	36	22	1.8	+16	MSOP-8	4-115
RF2325	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	27	22	16	5.0	+7	SOT-23-5	4-121
RF2326	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	25	18	12	5.7	+7	SOT-23-5	4-129
RF2333	General Purpose Amplifier	DC to 6	5 to 6	70	17	10	8.2	+18.5	SOT-23-5	4-137
RF2334	General Purpose Amplifier	DC to 4	>4.8	65	20	16	5	+18.5	SOT-23-5	4-143
RF2335	General Purpose Amplifier	DC to 6	>5.0	65	17	12	5.6	+17	SOT-23-5	4-147
RF2336	General Purpose Amplifier	DC to 3	>3.5	35	21	20	3.8	+11	SOT-23-5	4-151
RF2337	General Purpose Amplifier	DC to 6	>3.6	40	17	15	4.5	+12	SOT-23-5	4-155
RF2338	General Purpose Amplifier	DC to 6	>3.6	40	16	12		+10.5	SOT-23-5	4-159
RF2347	3V Low Noise Amplifier/ 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	22	26	20.5	1.4	+15.5	MSOP-8	4-163
RF2351	3V PCS CDMA Split Band PA Driver	1.71 to 1.91	3.0 to 6.0	48	30	21	2.5	+16	MLF16	4-171
RF2352	3V CDMA Driver Amplifier	0.8 to 0.9	2.7 to 3.6	15		19.5	2.3		MLF16	4-177
RF2361	3V Low Noise Amplifier/ 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	22	26	20.5	1.4	+15.5	SOT23-5	4-183
RF2362	PCS CDMA/TDMA 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	38	32	20.1	2.2	+14.5	SOT23-5	4-193
RF2363	Dual-Band 3V Low Noise Amplifier	800 to 1000/ 1800 to 2000	2.5 to 5.0	5/ 7.5	20/ 30	18/ 21.5	1.3/ 1.4	-10/ -12	SOT23-8	4-199
RF2364	3V PCS Low Noise Amplifier	1.8 to 2.5	2.7 to 3.3	17	27	18	1.7	8.5	SOT23-5	4-209
RF2365	3V Low Noise Amplifier	1.5 to 2.5	3.0	5.0 to 8.0	25	18	1.6		SOT23-5	4-215
RF2371	3V Low Noise Amplifier	0.7 to 2.0	2.7 to 3.6	2.9		17	1.6		SOT23-8	4-221
RF2375	3V DCS Low Noise Amplifier	0.7 to 2.0	2.7 to 3.6	5.3		18	2.5		SOT23-8	4-227
RF2442	High-Linearity Low Noise Amplifier	0.50 to 2.5	2.5 to 5.0	16	24	20	1.5	+13	MSOP-8	4-231
RF2445	3V DCS Low Noise Amplifier	1700 to 2200	2.7 to 3.6	5	7	20	2.2	+2	MSOP-8	4-241
RF2451	3V Low Noise Amplifier	0.70 to 2.0	2.7 to 3.6	2.9		12	1.7	-3	MSOP-8	4-247

5 Modulators And Upconverters

Part	Description	Frequency (MHz)	Vcc (Volts)	Conversion Method	Icc (mA)	Gain Control (dB)	Mod BW (MHz)	Package	Page
RF2402	UHF Quadrature Modulator	600 to 1000	3 to 5.5	Direct	28	n/a	100	SOP-14	5-1
RF2412	Broadband Dual-Conversion Quadrature Modulator	100 to 1000	3 to 6.5	Dual	31	n/a	50	SOP-20	5-7
RF2413	Gain Controlled Dual-Conversion Quadrature Modulator	200 to 1000	3 to 6.5	Dual	35	60	25	SOP-20	5-19
RF2422	2.5GHz Direct Quadrature Modulator	800 to 2500	4.5 to 6.0	Direct	45	n/a	250	SOP-16	5-29
RF2423	100mW Spread-Spectrum Transmitter IC	800 to 1000	4.5 to 6.0	Direct	110	25	100	SOP-16	5-35
RF2424	UHF Quadrature Modulator	700 to 1000	2.7 to 5.5	Direct	45	n/a	TBD	SOP-16	5-43
RF2454	VHF Quadrature Modulator	200 to 600	3 to 5.5	Direct	28	n/a	100	SOP-14	5-49
RF2464	VHF Quadrature Modulator	200 to 600	4.5 to 5.5	Direct	28	n/a	100	SOP-14	5-55
RF2658	Transmit Modulator, IF AGC, and Upconverter	900 to 1000	2.7 to 3.3	Dual	43 to 63	88	50	SSOP-28	5-61
RF2668	CDMA/FM Transmit Modulator, IF AGC, and Upconverter with Integrated PLL	700 to 2000	2.7 to 3.3	Dual	40 to 69	95	20	LQFP-48	5-71
RF2713	Quadrature Modulator/Demodulator	0.1 to 250	2.7 to 6	Direct	10	n/a	50	SOP-14	5-83
RF2909	3V 915MHz Spread-Spectrum Transmitter IC	100 to 1100	2.7 to 5.0	Direct	30 to 175	20	10	SSOP-24	11-103
RF9958	CDMA/FM Transmit Modulator, IF AGC, and Upconverter	900 to 1000	2.7 to 3.3	Dual	43 to 63	88	50	SSOP-28	5-93

6 Mixers

Part	Description	Frequency (MHz)	IF (MHz)	Vcc (Volts)	Icc (mA)	Package	Page
RF2456	CDMA/FM Downconverter	500 to 1100	250	2.7 to 4.0	18	SSOP-16	6-1
RF2466	3V CDMA/FM Mixer	500 to 1100	0.1 to 250	2.7 to 4.0	18	MLF16	6-7
RF2608	CDMA/FM Upconverter/BPSK Modulator	500 to 1500	200	2.7 to 5.0	22	SOP-8	6-15
RF2628	CDMA/FM Upconverter/BPSK Modulator	500 to 1500	200	2.7 to 5.0	22	MSOP-8	6-19
RF2638	CDMA Upconverter/BPSK Modulator	500 to 2500	300	2.7 to 3.3	25	MSOP-8	6-25
RF2639	Upconverter/BPSK Modulator	500 to 2500	300	2.7 to 3.3	7	MSOP-8	6-31
RF2640	3V 900MHz Upconverter/ Driver Amplifier	824 to 849	180	2.7 to 3.3	45	MSOP-10	6-37
RF2641	CDMA Upconverter/BPSK Modulator	500 to 2500	DC to 300	2.7 to 3.3	13	MSOP-8	6-41
RF2642	3V 900MHz Upconverter/ Driver Amplifier with Bypass Mode	824 to 849	130	2.7 to 3.3	15	MLF16	6-49
RF9908	CDMA/FM Upconverter/BPSK Modulator	500 to 1500	200	3.6	18	SOP-8	6-57
RF9938	PCS Upconverter/BPSK Modulator	1200 to 2500	200	3.6	27	SOP-8	6-61

7 Quadrature Demodulators

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	LO Freq	Amp Phase Bal	Demod Gain (dB)	Package	Page
RF2667	Receive AGC and Demodulator	50 to 300	2.7 to 3.3	20	2xIF	0.1dB, ±1°	-55 to +50	SSOP-24	7-1
RF2711	Quadrature Demodulator	0.1 to 250	4.5 to 5.5	4.5	2xIF	0.1dB, ±1°	14	SOP-14	7-11
RF2713	Quadrature Modulator/Demodulator	0.1 to 250	2.7 to 6	8	2xIF	0.1dB, ±1°	20	SOP-14	7-17
RF9957	CDMA/FM Receive AGC and Demodulator	50 to 250	2.7 to 3.3	14	2xIF	0.1dB, ±1°	-55 to +50	SSOP-24	7-27

8 Front-Ends

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Casc. Gain (dB)	Gain Control (dB)	Casc. IIP_3 (dBm)	Casc. NF (dB)	Package	Page
RF2401	Low Noise Amplifier/Mixer	300 to 1100	5	20	24	21	-17	4.3	SOP-14	8-1
RF2406	CDMA/FM Low Noise Amplifier/Mixer	500 to 1100	2.7 to 4	23	27	19.5	-4	4.3	SSOP-28	8-13
RF2411	Low Noise Amplifier/Mixer	500 to 1900	3 to 6.5	20	27	n/a	-8	2.4	SOP-14	8-23
RF2418	Low Current LNA/Mixer	400 to 1100	3 to 6.5	4.5	19	n/a	-13	3.9	SOP-14	8-35
RF2431	High Frequency LNA/Mixer	1500 to 2500	3 to 6.5	13	23	n/a	-14	3.5	SOP-16	8-43
RF2442	High-Linearity Low Noise Amplifier	500 to 2500	3	12	19	n/a	+3	1.8	MSOP-8	4-231
RF2444	High Frequency LNA/Mixer	2400 to 2500	2.7 to 3.6	20	28	16	-23 to -8	4.5 to 18	SSOP-16 EPP	8-53
RF2448	PCS CDMA Low Noise Amplifier/Mixer 1500MHz to 2200MHZ Downconverter	1500 to 2200	2.65 to 3.9	8	-4 to +25	29	-11 to +17.5	3 to 23	SSOP-16 EDF	8-69
RF2449	CDMA/FM Low Noise Amplifier/Mixer 900MHz Downconverter	869 to 894	2.75	20	28	21			SSOP-24	8-75
RF2457	900MHz 3V Low Current LNA/Mixer	902 to 928	2.7 to 3.3	5	8.5	13	-3	2.5	MSOP-10	8-85
RF2458	3V PCS Downconverter	1500 to 2500	2.7 to 3.6	38	14	n/a	+3	10	MSOP-10	8-91
RF2459	3V PCS Downconverter	1500 to 2500	2.7 to 3.6	20	10	n/a	+7	14	MSOP-8	8-97
RF2486	PCS Low Noise Amplifier/Mixer	1500 to 2500	2.7 to 5.0	52	26	n/a	-15	4.0	SSOP-24	8-105
RF9906	CDMA/FM Low Noise Amplifier/Mixer	500 to 1500	3.6	30	30	9	-13	2.6	SSOP-24	8-113
RF9936	PCS Low Noise Amplifier/Mixer	1500 to 2500	3.6	5 to 46	28	10	-9 to -14	2.5 to 5.1	SSOP-24	8-121
RF9986	PCS Low Noise Amplifier/Mixer	1500 to 2500	3.6	5 to 48	26	n/a	-11	2.5	SSOP-24	8-131

9 Attenuators and Switches

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Ins. Loss (dB)	Attn. Range/ Isolation (dB)	Attn. Step (dB)	Package	Page
RF2410	UHF Programmable Attenuator	500 to 2100	5	6	4.0	38	2	SOP-16	9-1
RF2420	Programmable Attenuator	DC to 950	3 to 6	4	4.0	44	2	SOP-16	9-9
RF2421	10dB Switched Attenuator	500 to 3000	2.7 to 6	0.5	1.0	10	10	SOP-8	9-15
RF2425	4-Port Transfer Switch	800 to 2000	2.7 to 6	1.5	0.6	23	n/a	SOP-8	9-19
RF2436	Transmit/Receive Switch	100 to 2500	2.7 to 6	1.5	0.5	24	n/a	SOT-23-5	9-23

10 IF Amplifiers

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Gain (dB, Max)	Gain Control (dB)	RSSI	Package	Page
RF2607	CDMA/FM Receive AGC Amplifier	12 to 285	3.6	14	48	96	no	SSOP-16	10-1
RF2609	CDMA/FM Transmit AGC Amplifier	12 to 175	3.6	23	42	90	no	SSOP-16	10-9
RF2617	3V CDMA/FM Receive AGC Amplifier	12 to 285	3.0	14	48	96	no	SSOP-16	10-17
RF2619	3V CDMA/FM Transmit AGC Amplifier	12 to 175	3.0	23	42	90	no	SSOP-16	10-25
RF2627	3V CDMA Receive AGC Amplifier	12 to 285	2.7 to 3.3	14	48	96	no	MSOP-8	10-33
RF2629	3V CDMA/FM Transmit AGC Amplifier	12 to 175	2.7 to 3.3	23	42	90	no	MSOP-8	10-39
RF2670	8MHz Dual Baseband AGC with Programmable Low Pass Filtering	0.01 to 8	2.7 to 3.6	13	80	70	yes	SSOP-24	10-45
RF2903	Integrated Spread Spectrum Receiver	150 to 1000	3.0 to 6.0	23	90	90	yes	SSOP-24	10-57

11 Transceivers

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc-Rx (mA)	Icc-Tx (mA)	TX Power (dBm)	RX Sensitivity (dBm)	Package	Page
RF2510	VHF/UHF Transmitter	300 to 1000	2.4 to 5.0	n/a	13	-4	n/a	SSOP-16	11-1
RF2512	UHF Transmitter	300 to 1000	2.7 to 5.0	n/a	25	+10	n/a	SSOP-24	11-11
RF2513	UHF Transmitter	300 to 1000	2.7 to 5.0	n/a	25	+6	n/a	SSOP-24	11-23
RF2516	VHF/UHF Transmitter	100 to 960	2.0 to 3.6	n/a	10.5	+10	n/a	SSOP-16	11-35
RF2905	433/868/915MHz FM/FSK/ASK/OOK Transceiver	300 to 1000	2.7 to 5.0	9	25	+10	-101	LQFP-48	11-53
RF2907	433/868/915MHz AM/ASK/OOK Transceiver	300 to 1500	2.7 to 5.0	11.5	20	+7.0	-97	SSOP-28	11-75
RF2908	915MHz Spread Spectrum Receiver with PLL Frequency Synthesizer	700 to 1100	2.7 to 3.6	50	n/a	n/a	TBD	LQFP-48	11-85
RF2909	3V 915MHz Spread-Spectrum Transmitter IC	100 to 1100	2.7 to 5.0	n/a	30 to 175	17	n/a	SSOP-24	11-103
RF2915	433/868/915MHz FSK/ASK/OOK Transceiver	300 to 1000	2.4 to 5.0	5.6	22	+8.5	-99	LQFP-32	11-111
RF2917	433/868/915MHz FM/FSK Receiver	300 to 1000	2.7 to 5.0	9	n/a	n/a	-101	LQFP-32	11-129
RF2919	433/868/915MHz ASK/OOK Receiver	300 to 1000	2.7 to 5.0	10	n/a	n/a	-104	LQFP-32	11-143
RF2925	433/868/915MHz FM/FSK/ASK/OOK Transceiver	300 to 1000	2.7 to 5.0	9	25	+10	-101	LQFP-48	11-161
RF2926	UHF Dual Conversion Transceiver	300 to 1000	2.7 to 5.0	10	37	+8.5	-99	LQFP-48	11-185
RF2938	2.4GHz Spread Spectrum Transceiver	45 to 500 and 2.4 to 2.5GHz	2.7 to 3.6	65	105	+6	n/a	TQFP-48 EPP	11-193
RF2945	433/868/915MHz FSK/ASK/OOK Transceiver	300 to 1000	2.4 to 5.0	6.1	22	+8.5	-96	LQFP-32	11-215
RF9901	FSK Transmitter	400 to 930	3.0 to 5.0	n/a	30	+2	n/a	SOP-16	11-231
RF9902	FSK Receiver	400 to 930	3.0 to 5.0	25	n/a	n/a	-85	SOP-16	11-239

12 VCOs

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Output Power (dBm)	Package	Page
RF2504	VCO/High-Isolation Buffer Amplifier	700 to 1500	2.2 to 5.0	5.5	-6	SOP-8	12-1
RF2506	VHF/UHF VCO/High-Isolation Buffer Amplifier	10 to 1000	2.7 to 3.6	9	-3	SOP-8	12-9

Data Sheet Classification

Preliminary

The heading "***Preliminary***" on a data sheet indicates that the device has undergone initial testing, and the device is available for sampling and low volume orders. In some cases, the samples supplied in this stage may differ slightly from the final production version. The device is still under evaluation and characterization, and therefore specifications are subject to change without notice.

Released

When there is no specific header on a data sheet the device has been released for production. Production quantities are available. The guaranteed limits will not be changed without notice to the local sales organizations and customers with open orders.

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2 Power Amplifiers

Part	Description	Frequency (MHz)	Vcc (Volts)	Efficiency (%, Max)	Output Power	Package	Page
RF2103P	Medium Power Linear Amplifier	450 to 1000	2.7 to 7.5	47	750mW at 7.5V	SOP-14	2-1
RF2104	Medium Power Amplifier	400 to 1000	2.7 to 3.6	40	500mW at 3.6 V	SOP-16 QBW1	2-11
RF2105L	High Power Linear UHF Amplifier	430 to 930	2.7 to 6.5	48	1.2W at 5.8V	QLCC-16	2-19
RF2108	Linear Power Amplifier	800 to 950	4.2 to 7.5	57	1.4W at 4.8V	SOP-16 BW	2-27
RF2114	Medium Power Linear Amplifier	1 to 600	2.7 to 6.5	45	800mW at 5.8V	SOP-14	2-33
RF2115L	High Power UHF Amplifier	430 to 930	5.0 to 6.5	48	1.1W at 5.8V	QLCC-16	2-39
RF2117	High Efficiency 400MHz Amplifier	400 to 500	3.0 to 5.5	50		PSOP-16	2-47
RF2119	High Efficiency 2V Power Amplifier	800 to 960	2.0 to 5.0	53	2.0W at 3.0V	PSSOP-16	2-55
RF2125	High Power Linear Amplifier	1500 to 2200	2.7 to 7.5	45	1W at 6.0V	SOP-8-C	2-61
RF2125P	High Power Linear Amplifier	1500 to 2200	2.7 to 7.5	45	1W at 6.0V	PSOP-8	2-67
RF2126	High Power Linear Amplifier	1800 to 2500	3.0 to 6.5	45	1.3W at 6.0V	PSOP-8	2-73
RF2127	Medium Power Linear Amplifier	1500 to 1900	3.0 to 6.5	30	200mW at 6.0V	SOP-8	2-79
RF2128	Medium Power Linear Amplifier	1900 to 2500	3.0 to 6.5	30	200mW at 6.0V	SOP-8-C	2-85
RF2128P	Medium Power Linear Amplifier	1900 to 2500	3.0 to 6.5	33	200mW at 6.0V	PSOP-8	2-89
RF2129	3V, 2.5GHz Linear Power Amplifier	1800 to 2500	3.0 to 5.0	42	400mW at 3.3V	PSOP-8	2-93
RF2131	High Efficiency AMPS/ETACS Amplifier	800 to 950	4.0 to 7.0	64	1.2W at 4.8V	SOP-16 BW	2-99
RF2132	Linear Power Amplifier	800 to 950	4.2 to 6.0	55	1.6W at 4.8V	SOP-16 BW	2-109
RF2137	Linear Power Amplifier	800 to 950	4.2 to 6.0	55	1.6W at 5.0V	PSOP-8	2-115
RF2138	3V GSM Power Amplifier	800 to 950	2.7 to 4.8	58	4W at 3.5V	MP16K01A	2-119
RF2140	3V DCS Power Amplifier	1700 to 2000	2.7 to 4.8	51	2W at 3.5V	MP16K01A	2-129
RF2145	DCS1800/1900 Power Amplifier	1700 to 1900	2.7 to 6.5	55	1.6W at 4.8V	SOP-16 QBW1	2-141
RF2146	PCS Linear Power Amplifier	1500 to 2000	4.0 to 6.5	37	700 mW at 4.8V	SOP-16 QBW1	2-147
RF2152	Dual-Mode CDMA/AMPS or TDMA/AMPS 3V Power Amplifier	800 to 960	3.0 to 5.2	36/45	500 mW/1.1W at 3V	PSSOP-16	2-155
RF2153	CDMA/TDMA/PACS 1900MHz 3V Power Amplifier	1750 to 1910	3.0 to 4.5	40	800mW at 3.4V	MP16K01A	2-167
RF2155	3V Programmable Gain Power Amplifier	430 to 930	3.0 to 5.0	56	450mW at 3.6V	SOP-16 BW	2-179
RF2157	PCS CDMA/TDMA 3V Power Amplifier	1750 to 1910	3.0 to 4.5	35	800 mW at 3.4V	MLF16	2-187
RF2161	3V WCDMA Power 1900MHZ 3V Linear Power Amplifier	1850 to 2000	3.4	36	27dBm	MP16K01A	2-197
RF2162	3V 900MHz Linear Amplifier	800 to 960	3.4	35	800mW at 3.4V	MLF16	2-205
RF2172	900MHz ISM Band 3.6V, 250mW Amp with Analog Gain Control	902 to 928	3.0 to 3.6	58	24dBm at 3.6V	MLF16	2-213
RF2173	3V GSM Power Amplifier	800 to 950	2.7 to 4.8	56	36dBm at 3.5V	MLF16	2-221
RF2174	3V DCS Power Amplifier	1700 to 1950	2.7 to 4.8	51	33dBm at 3.5V	MLF16	2-231
RF2175	3V 400MHz Linear Amplifier	380 to 512	3.0 to 5.2	30	34dBm at 3.6V	PSSOP-16	2-243
RF2189	3V, 2.5GHz Linear Power Amplifier	1800 to 2500	3.0 to 5.0	42	26dBm at 3.3V	MLF16	2-249

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RF2103P

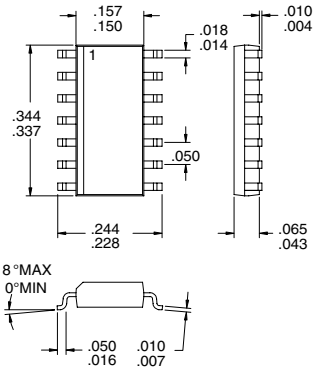
MEDIUM POWER LINEAR AMPLIFIER

Typical Applications

- Digital Communication Systems
- Spread Spectrum Communication Systems
- Driver for Higher Power Linear Applications
- Portable Battery Powered Equipment
- Commercial and Consumer Systems
- Base Station Equipment

Product Description

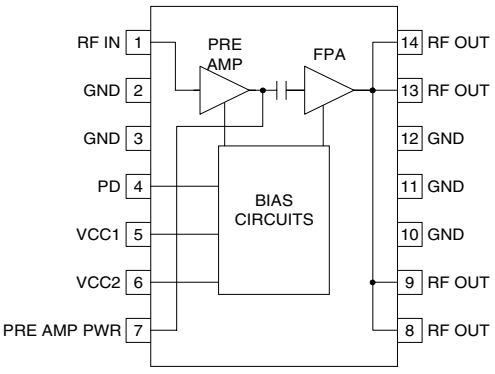
The RF2103P is a medium power linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final linear RF amplifier in UHF radio transmitters operating between 450MHz and 1000MHz. It may also be used as a driver amplifier in higher power applications. The device is self-contained with the exception of the output matching network, power supply feed line, and bypass capacitors, and it produces an output power level of 750mW (CW). The device can be used in 3 cell battery applications. The maximum CW output at 3.6V is 175mW. The unit has a total gain of 31dB, depending upon the output matching network.



Package Style: SOP-14

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 450MHz to 1000MHz Operation
- Up to 750mW CW Output Power
- 31dB Small Signal Gain
- Single 2.7V to 7.5V Supply
- 47% Efficiency
- Digitally Controlled Power Down Mode

Ordering Information

RF2103P	Medium Power Linear Amplifier
RF2103P PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
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http://www.rfmd.com

RF2103P

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5	V
DC Supply Current	350	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +100	°C
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5.8V, V_{PD}=5.0V, Z_{LOAD}=18Ω, P_{IN}=0dBm, Freq=915MHz
Frequency Range		450 to 1000		MHz	
Maximum Output Power		+28.8		dBm	V_{CC}=7.5V
Maximum Output Power		+26.5		dBm	V_{CC}=5.8V
Second Harmonic		-24		dBc	Without external second harmonic trap
Third Harmonic		-30		dBc	
Output Noise Power		<-125		dBm/Hz	
Input Impedance		50		Ω	With external matching network; see application schematic
Input VSWR		<2:1			With external matching network; see application schematic
Output Impedance		18+j0		Ω	Load Impedance for Optimal Match
Nominal 5.8V Configuration					V_{CC}=5.8V, V_{PD}=4.0V, Z_{LOAD}=18Ω, P_{IN}=0dBm, Freq=830MHz
Linear Power Gain		31		dB	
Saturated CW Output Power	24	+26.5		dBm	
IM_3		-40	-25	dBc	P_{OUT}=+18.5dBm/tone
IM_5		-45	-30	dBc	P_{OUT}=+18.5dBm/tone
Collector Current, I_{CC}		175	250	mA	Total of pins 7 and 8
V_{PD} Current		<3.5		mA	Into pin 4
CW Total Efficiency		47		%	
Two Tone Total Efficiency		26		%	P_{OUT}=+18.5dBm/tone
Power Supply					
Power Supply Voltage		2.7 to 7.5		V	
Power Supply Idle Current		45	80	mA	
Total "OFF" Current Drain		1	10	µA	V_{PD}<0.1V_{DC}
Turn-on Time		<100		ns	V_{PD}=0 to V_{PD}=+4V_{DC}

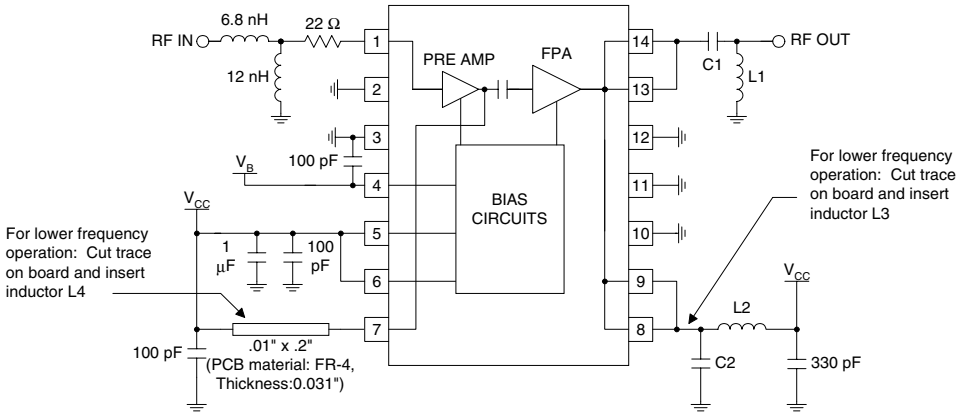
Db00.bk Page 3 Thursday, January 6, 2000 6:50 PM

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. There is an internal blocking capacitor between this pin and the preamp input, but not between the pin and an internal 2kΩ resistor to ground.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	PD	Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at V_{CC} (3V to 6.5V), the device will be in full power mode delivering maximum available gain and output power capability. This pin may also be used to perform some degree of gain control or power control when set to voltages between 0V and V_{CC}. It is not optimized for this function so the transfer function is not linear over a wide range as with other devices specifically designed for analog gain control; however, it may be usable for coarse adjustment or in some closed loop AGC systems. This pin should not, in any circumstance, be higher in voltage than V_{CC}. This pin should also have an external bypassing capacitor.	
5	VCC1	Positive supply for the active bias circuits. This pin can be externally combined with pin 6 (VCC2) and the pair bypassed with a single capacitor, placed as close as possible to the package. Additional bypassing of 1μF is also recommended, but proximity to the package is not as critical. In most applications, pins 5, 6, and 7 can share a single 1μF bypass capacitor.	
6	VCC2	Same as pin 5.	
7	PREAMP PWR	Positive supply for the pre-amplifier. This is an unmatched transistor collector output. This pin should see an inductive path to AC ground (V_{CC} with bypass capacitor). This inductance can be achieved with a short, thin microstrip line or with a low value chip inductor (approximately 1.8nH). At lower frequencies, the inductance value should be larger (longer microstrip line) and V_{CC} should be bypassed with a larger bypass capacitor. This inductance forms a matching network with the internal series capacitor between the two amplifier stages, setting the amplifier's frequency of maximum gain. An additional 1μF bypass capacitor in parallel with the 100pF bypass capacitor is also recommended, but placement of this component is not as critical. In most applications, pins 5, 6, and 7 can share a single 1μF bypass capacitor.	
8	RF OUT	Same as pin 14.	
9	RF OUT	Same as pin 14.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	GND	Same as pin 2.	
13	RF OUT	Same as pin 14.	

RF2103P

Pin	Function	Description	Interface Schematic
14	RF OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 8, 9, 13 and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through two of these four pins. Typically, pins 8 and 9 are connected to a network that provides the DC bias and also creates a second harmonic trap. For 915MHz operation, this harmonic trap network is simply a single 2pF capacitor from both pins to ground. This capacitor series resonates with internal bond wires at two times the operating frequency, effectively shorting out the second harmonic. Shorting out this harmonic serves to increase the amplifier's maximum output power and efficiency, as well as to lower the level of the second harmonic output. Typically, pins 13 and 14 are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output. Shunt protection diodes are included to clip peak voltage excursions above approximately 15V to prevent voltage breakdown in worst case conditions.	

Application Schematic

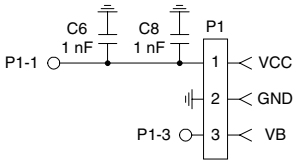


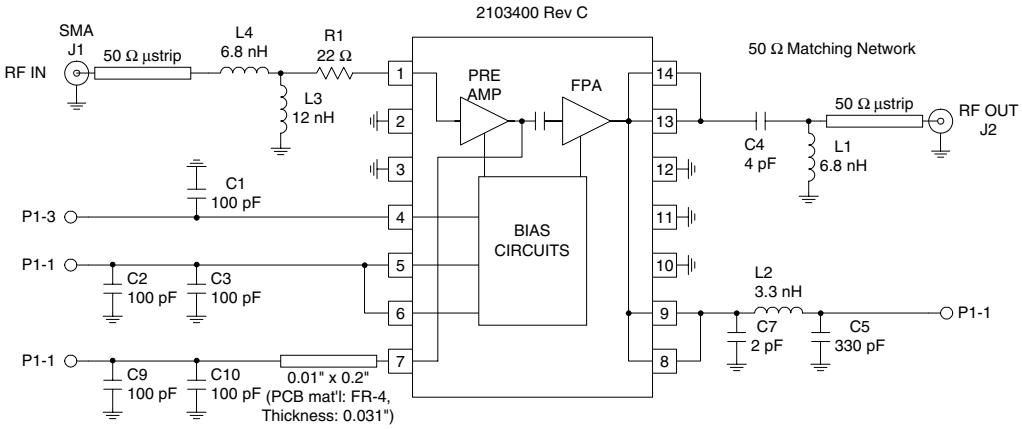
FREQUENCY (MHz)	L1 (nH)	L2 (nH)	L3 (nH)	L4 (nH)	C1 (pF)	C2 (pF)
275	20	15	10	20	20	10
480	12	6.8	4.7	18	12	6.8
915	6.8	3.3	—	—	4	2

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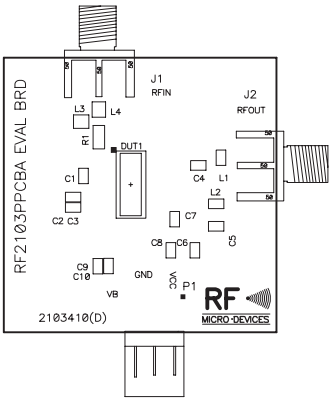
Evaluation Board Schematic
915MHz Operation

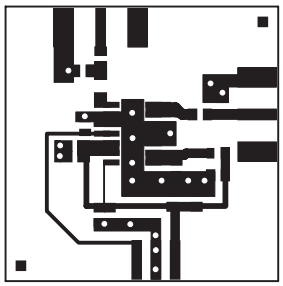
(Download Bill of Materials from www.rfmd.com.)



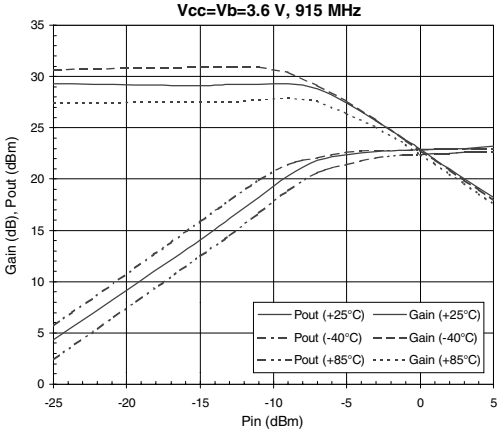


Evaluation Board Layout
1.4” x 1.4”

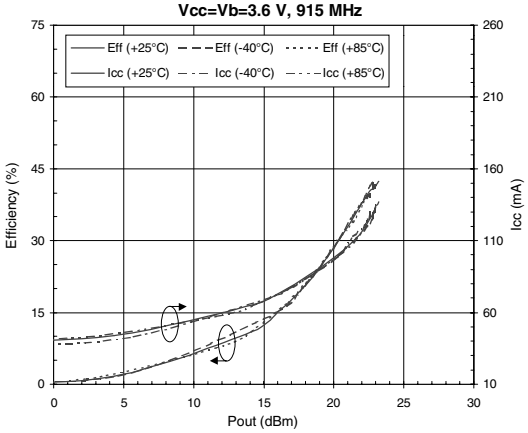




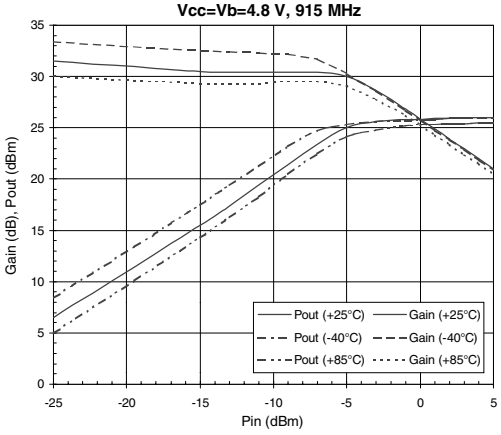
Gain and Pout vs. Pin
Vcc=Vb=3.6 V, 915 MHz



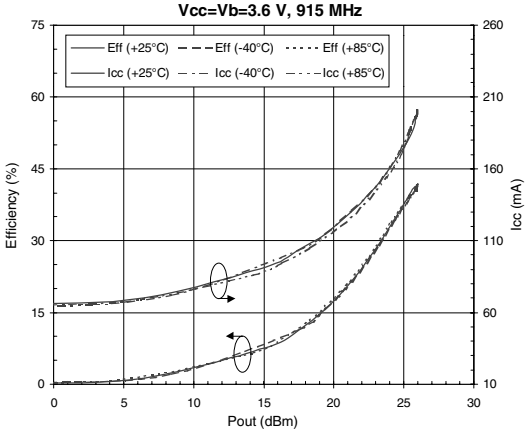
Efficiency and Icc vs. Pout
Vcc=Vb=3.6 V, 915 MHz



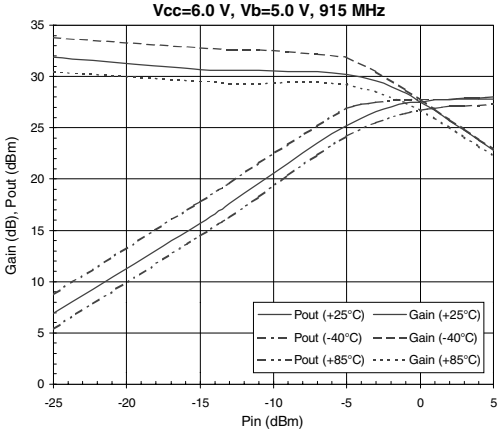
Gain and Pout vs. Pin
Vcc=Vb=4.8 V, 915 MHz



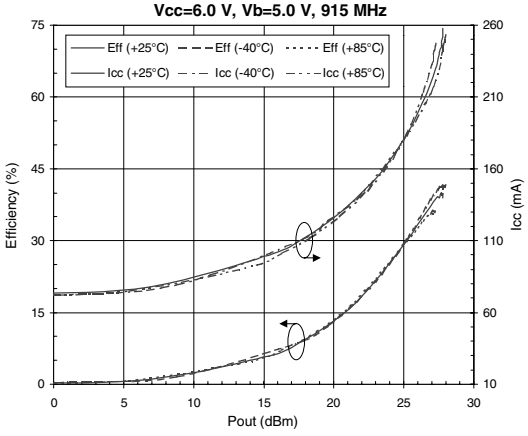
Efficiency and Icc vs. Pout
Vcc=Vb=3.6 V, 915 MHz



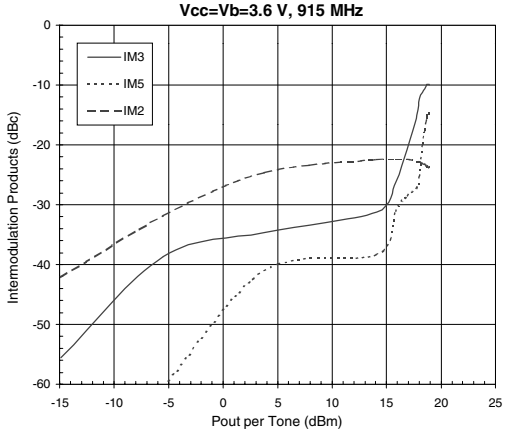
Gain and Pout vs. Pin
Vcc=6.0 V, Vb=5.0 V, 915 MHz



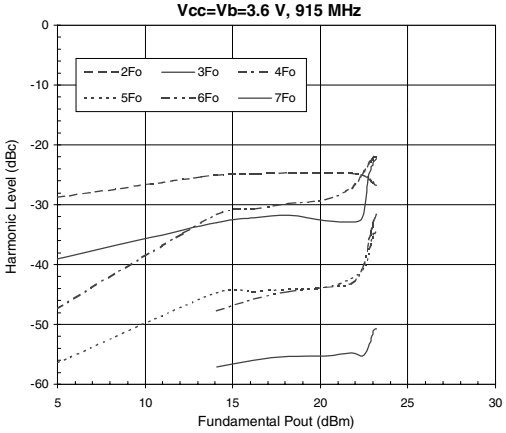
Efficiency and Icc vs. Pout
Vcc=6.0 V, Vb=5.0 V, 915 MHz



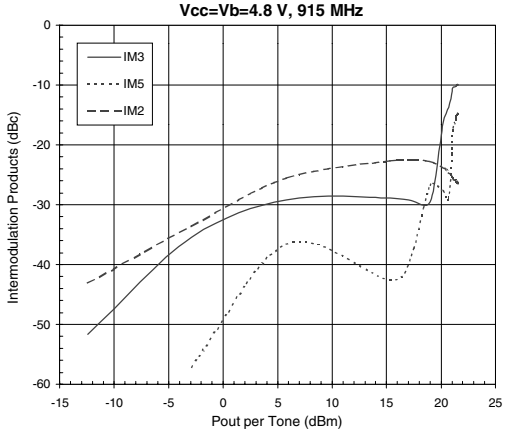
IM3, IM5, and IM2 vs. Pout
Vcc=Vb=3.6 V, 915 MHz



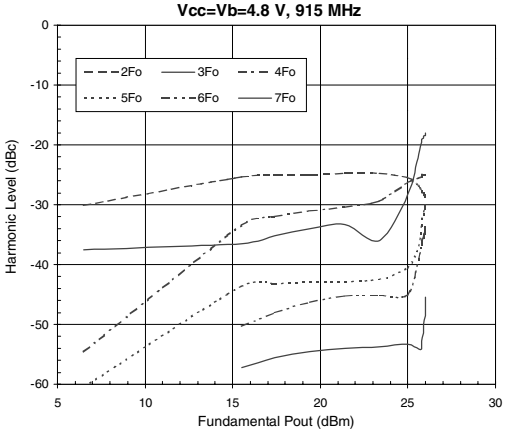
Harmonics vs. Pout
Vcc=Vb=3.6 V, 915 MHz



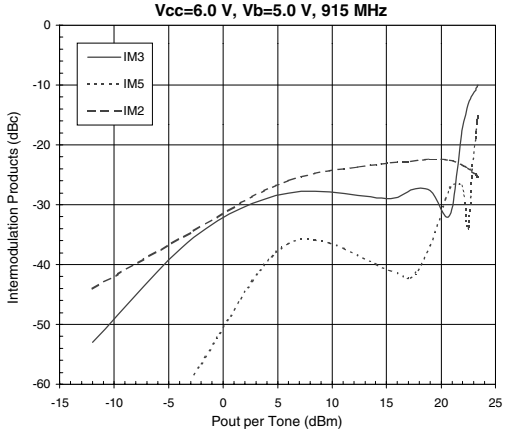
IM3, IM5, and IM2 vs. Pout
Vcc=Vb=4.8 V, 915 MHz



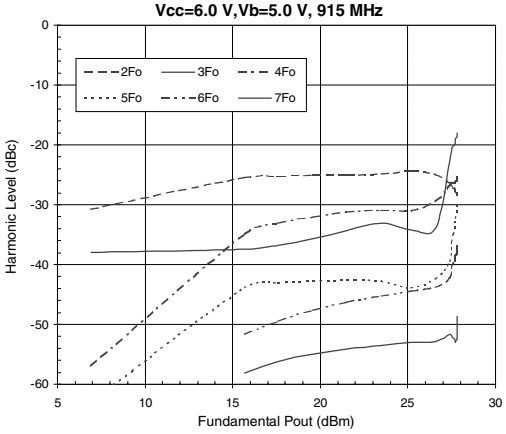
Harmonics vs. Pout
Vcc=Vb=4.8 V, 915 MHz

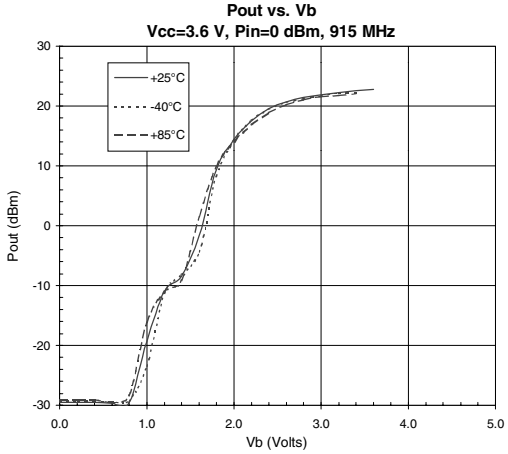


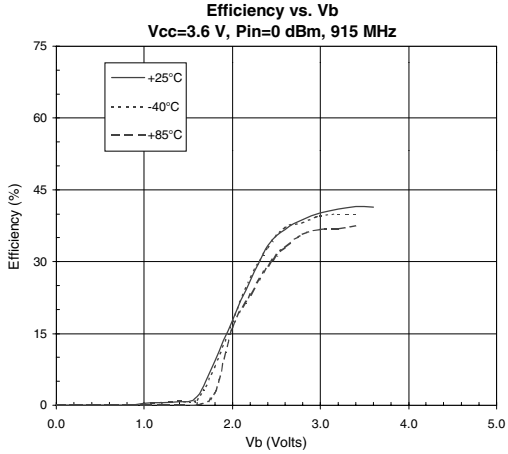
IM3, IM5, and IM2 vs. Pout
Vcc=6.0 V, Vb=5.0 V, 915 MHz

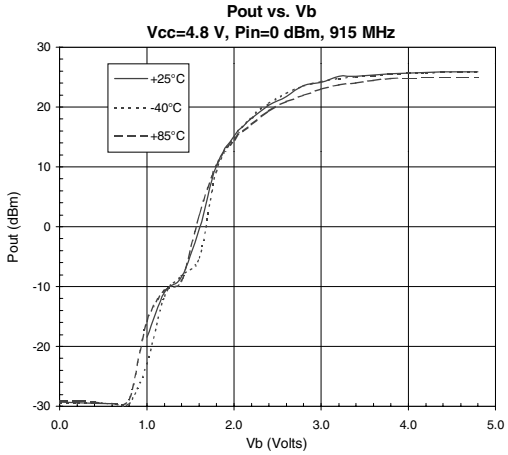


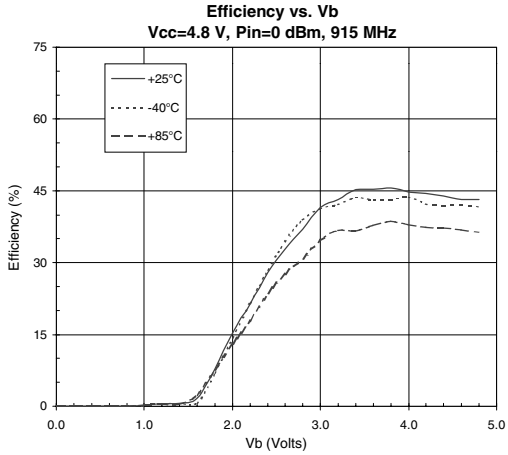
Harmonics vs. Pout
Vcc=6.0 V,Vb=5.0 V, 915 MHz

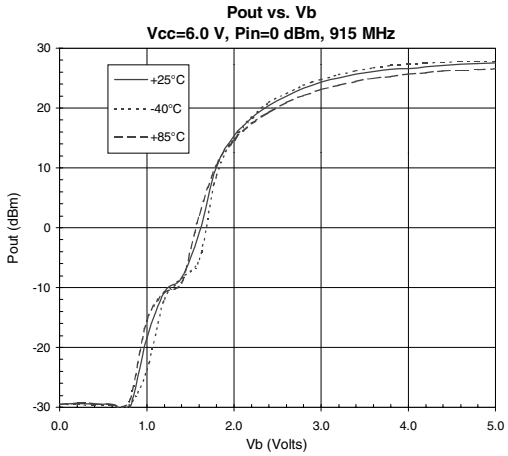


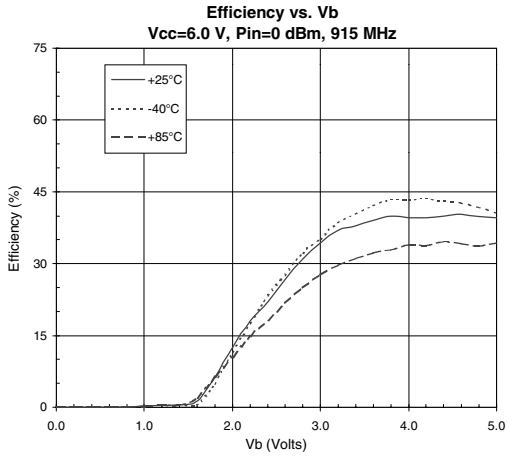

Pout vs. Vb
Vcc=3.6 V, Pin=0 dBm, 915 MHz
+25°C
-40°C
+85°C
Pout (dBm)
Vb (Volts)


Efficiency vs. Vb
Vcc=3.6 V, Pin=0 dBm, 915 MHz
+25°C
-40°C
+85°C
Efficiency (%)
Vb (Volts)

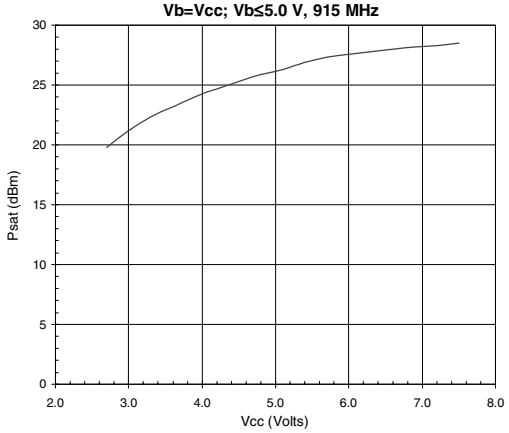

Pout vs. Vb
Vcc=4.8 V, Pin=0 dBm, 915 MHz
+25°C
-40°C
+85°C
Pout (dBm)
Vb (Volts)


Efficiency vs. Vb
Vcc=4.8 V, Pin=0 dBm, 915 MHz
+25°C
-40°C
+85°C
Efficiency (%)
Vb (Volts)

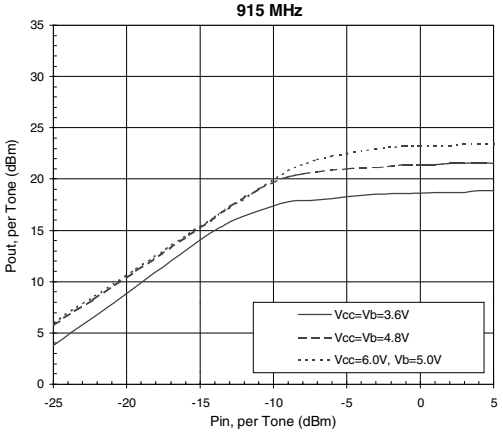

Pout vs. Vb
Vcc=6.0 V, Pin=0 dBm, 915 MHz
+25°C
-40°C
+85°C
Pout (dBm)
Vb (Volts)


Efficiency vs. Vb
Vcc=6.0 V, Pin=0 dBm, 915 MHz
+25°C
-40°C
+85°C
Efficiency (%)
Vb (Volts)

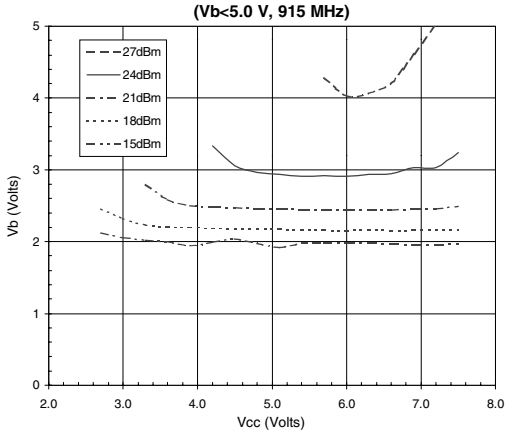
Psat vs. Vcc
Vb=Vcc; Vb≤5.0 V, 915 MHz



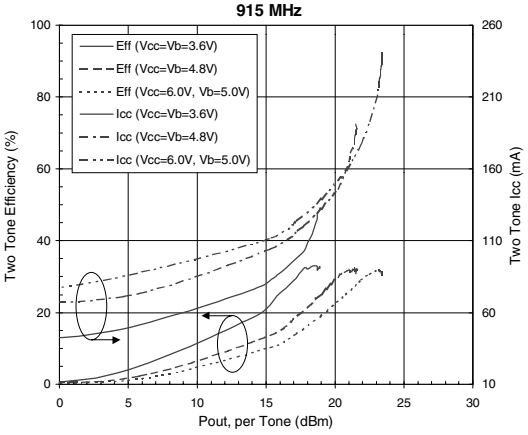
Two Tone Pout vs. Pin,
915 MHz



Vb Required to Achieve Specific Pout
(Vb<5.0 V, 915 MHz)



Two Tone Efficiency and Icc vs. Pout,
915 MHz



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RF2104

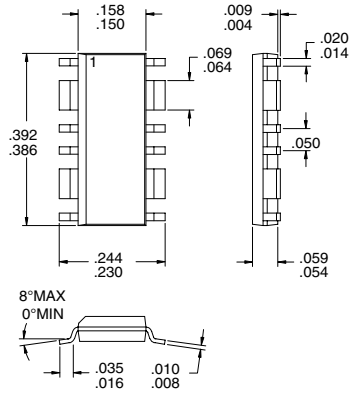
MEDIUM POWER AMPLIFIER

Typical Applications

- 900MHz ISM Band Applications
- 400MHz Industrial Radios
- Driver for Higher Power Applications
- Portable Battery Powered Equipment
- Commercial and Consumer Systems
- Base Station Equipment

Product Description

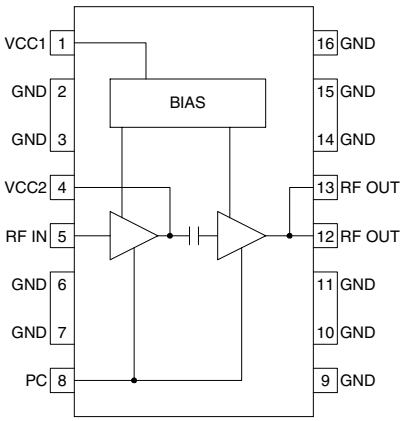
The RF2104 is a medium power amplifier IC. The device is manufactured on a low cost Silicon process, and has been designed for use as the final RF amplifier in UHF radio transmitters operating between 400MHz and 1000MHz. It may also be used as a driver amplifier in higher power applications. The device is packaged in a plastic quad-batwing 16-lead package, and is self-contained with the exception of the output matching network, power supply feed line, and bypass capacitors. It produces an output power level of up to 500mW (CW) at 3.6V. The device can be used in 3 cell battery applications. The maximum CW output at 3.6V is +27dBm. The unit has a total gain of 26dB, depending upon the output matching network.



Package Style: SOP-16 QBW1

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 400MHz to 1000MHz Operation
- Up to 500mW CW Output Power
- 26dB Small Signal Gain
- 40dB Gain Control Range
- Single 2.7V to 3.6V Supply
- 40% Efficiency

Ordering Information

RF2104	Medium Power Amplifier
RF2104 PCBA-L	Fully Assembled Evaluation Board (830MHz)
RF2104 PCBA-H	Fully Assembled Evaluation Board (915MHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2104

Absolute Maximum Ratings

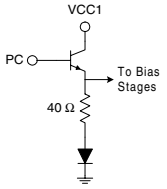
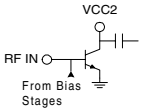
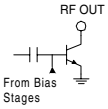
Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Gain Control Voltage (V_{PC})	-0.5 to +3.0	V
DC Supply Current	500	mA
Input RF Power	+12	dBm
Output Load VSWR	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

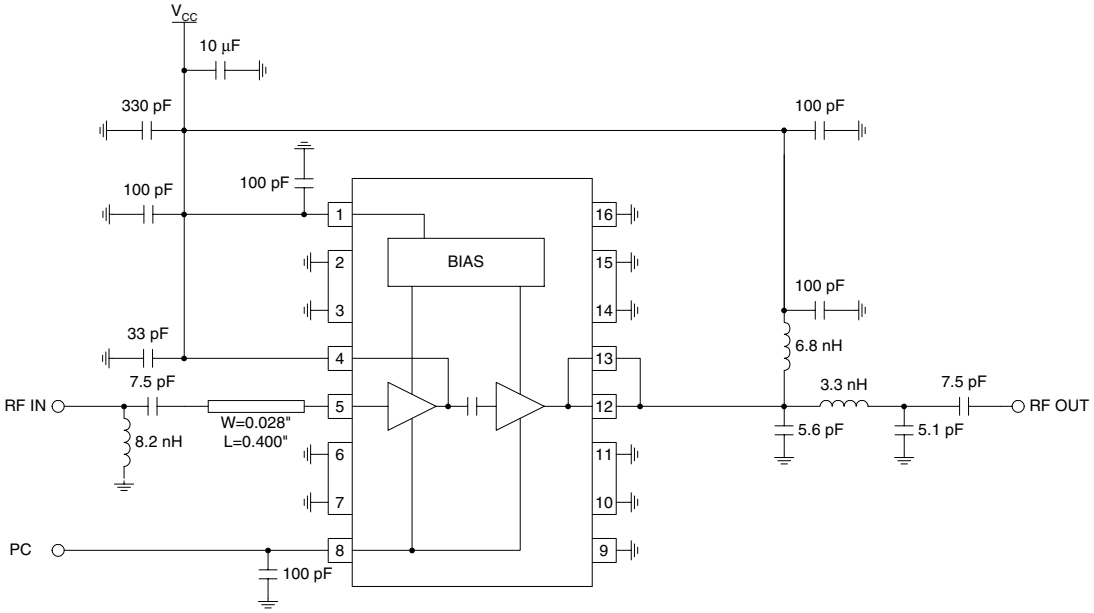
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, V_{PC}=2.5V, Z_{LOAD}=10Ω, P_{IN}=+6dBm, Freq=850MHz
Frequency Range		400 to 1000		MHz	
Bandwidth		150		MHz	With fixed matching network
Maximum Output Power		+27		dBm	V_{CC}=3.6V, P_{IN}=+6dBm
Maximum Output Power		+27		dBm	V_{CC}=3.0V, P_{IN}=+6dBm
Output Third Order Intercept		+36		dBm	V_{CC}=3.6V
Power Added Efficiency		40		%	V_{CC}=3.6V, P_{OUT}=+27dBm, P_{IN}=+6dBm
Small Signal Gain	24	25	28	dB	
Gain Control Range		35	40	dB	V_{PC}=0V to 2.5V
Second Harmonic		-50		dBc	Without external second harmonic trap
Third Harmonic		-50		dBc	
Noise Figure		5.5	7.0	dB	
Input Impedance		50		Ω	
Input Return Loss		-20	-15	dB	With external matching network; see application schematic
Input Return Loss		-10		dB	Without external matching network
Output Impedance		50		Ω	Not matched for maximum output power
Output Return Loss		-13		dB	Without external matching network
Load Impedance		5+j0		Ω	Load Impedance for Optimal Power Match
Power Supply					
Power Supply Voltage		2.7 to 3.6		V	
Power Supply Idle Current		250	300	mA	V_{PC}=2.5V
Total "OFF" Current Drain		1	10	µA	V_{PC}<0.25V_{DC}; No RF input power
Total "OFF" Current Drain		4		mA	V_{PC}<0.25V_{DC}; P_{IN}=+6dBm
Current into PC pin			1	mA	V_{PC}=2.5V
Current into PC pin		0		µA	V_{PC}=0V
Turn-on Time		<100		ns	V_{PC}=0V to V_{PC}=+2.5V_{DC}

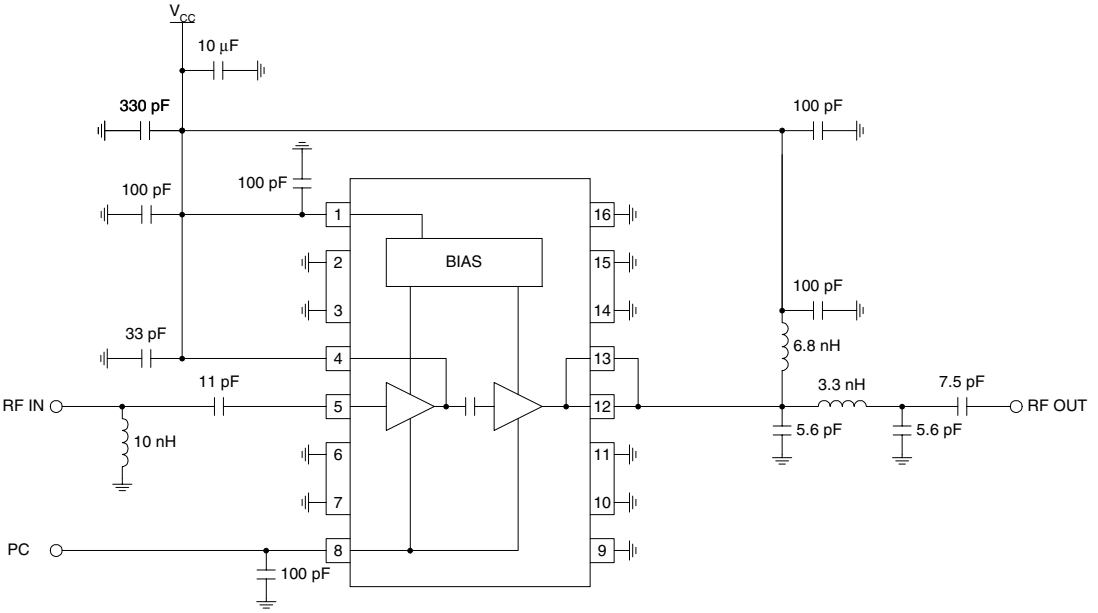
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Pin	Function	Description	Interface Schematic
1	VCC1	Power supply for the bias circuits.This pin draws current proportional to V_{PC}. When V_{PC} is 2.5V the maximum current is about 30mA. When V_{PC} goes down to 0V the current also goes down to 0mA.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. A via hole under each ground pin to the ground plane is recommended.	
3	GND	Same as pin 2.	
4	VCC2	Power supply for the driver stage and interstage matching. An external decoupling capacitor is required. The electrical length between the pin and this capacitor affects the gain. See the application schematic for recommended line length for optimum gain. For operation at frequencies below 600MHz a series inductor is required.	
5	RF IN	50Ω RF input. DC voltages are present at this pin, and an external blocking capacitor is required when connecting this pin to a DC path to ground. For optimum impedance matching, a shunt inductor to ground is recommended; see the application schematic for details.	See pin 4 schematic.
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	PC	Power control pin. A DC voltage between 0V and 3.0V can be applied to control the gain. When no gain control is required this pin should be connected to a fixed voltage between 2.5V and 3.0V. This pin draws some current proportional to V_{PC}. When V_{PC} is 2.5V the maximum current into this pin is about 1mA.	See pin 1 schematic.
9	GND	Same as pin 2.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	RF OUT	RF output. The power supply for the output stage also needs to be supplied to this pin through the external matching circuit. The load impedance to this pin should be 5+j0Ω for maximum output power.	
13	RF OUT	Same as pin 12.	See pin 12 schematic.
14	GND	Same as pin 2.	
15	GND	Same as pin 2.	
16	GND	Same as pin 2.	

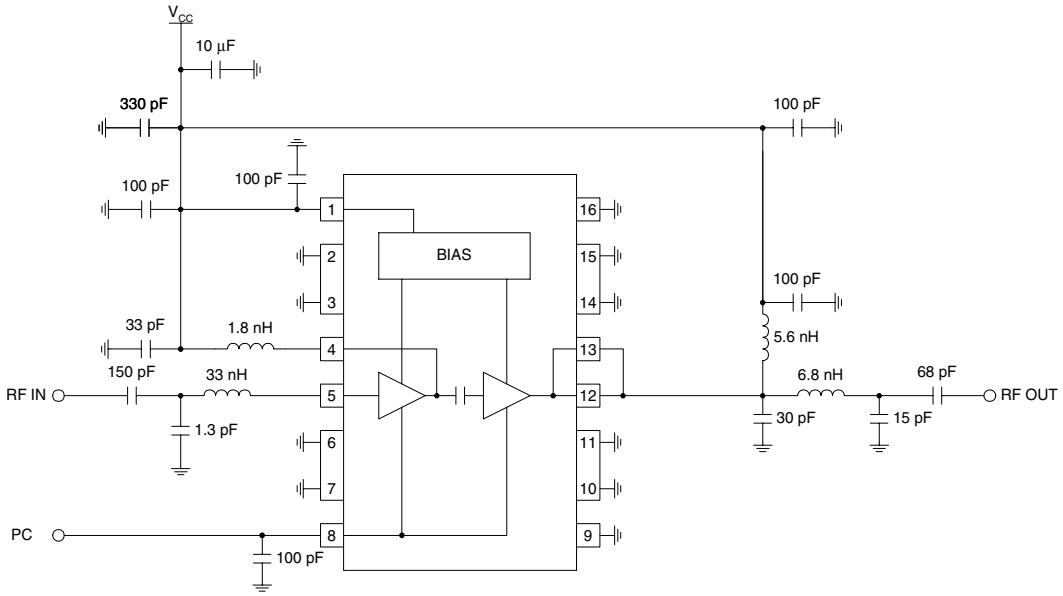
Application Schematic 915MHz



Application Schematic 830MHz

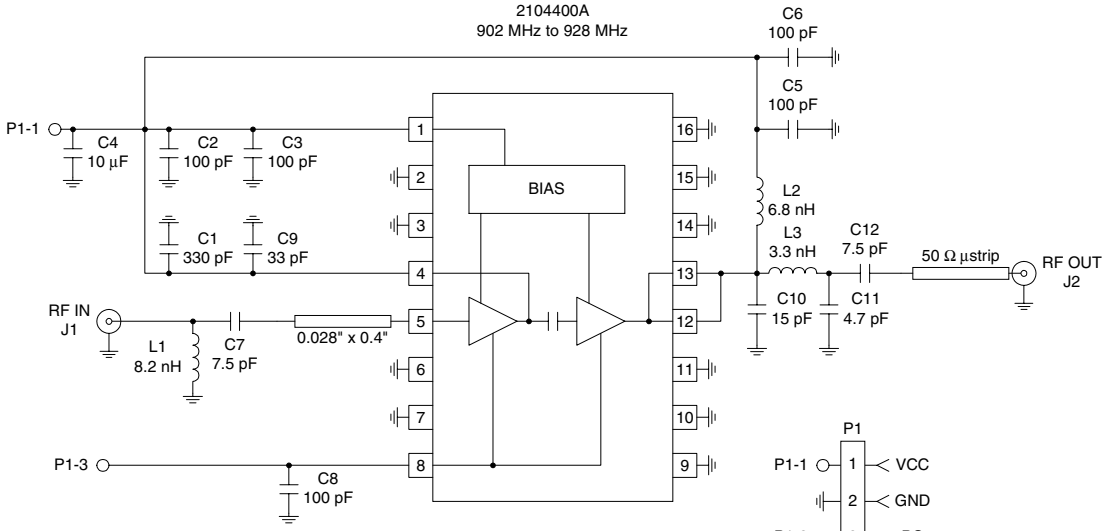


Application Schematic
420MHz



Evaluation Board Schematic
915MHz

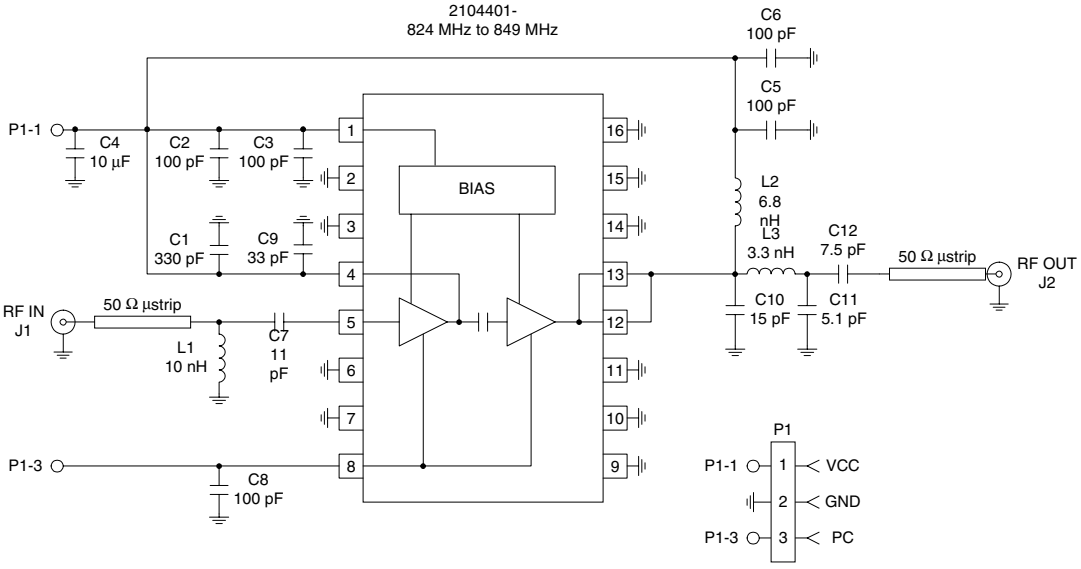
(Download Bill of Materials from www.rfmd.com.)



Note: Efficiency is affected by actual position of C9 and C10; C9 is mounted close to DUT and C10 mounted away from DUT.

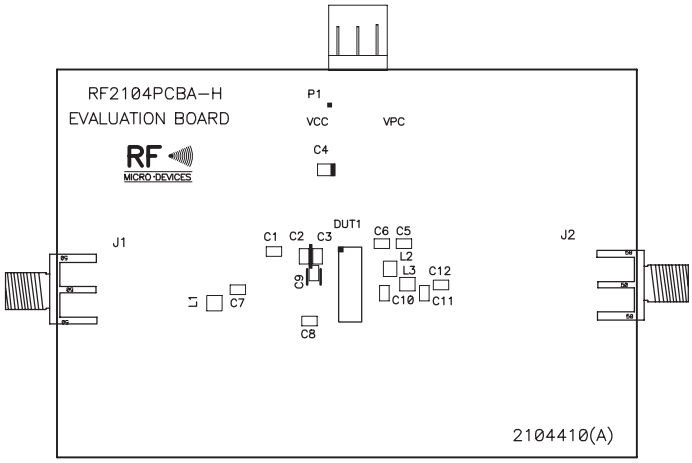
Evaluation Board Schematic
830MHz

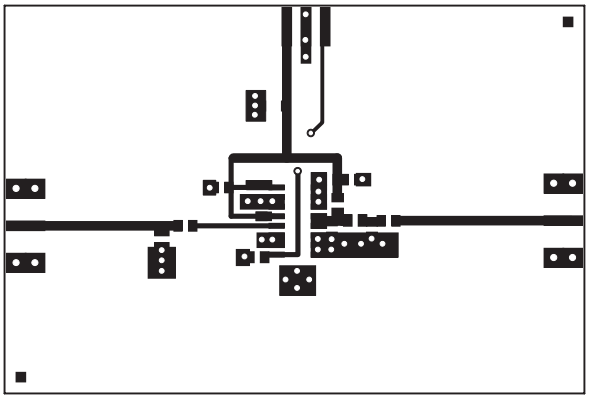
(Download Bill of Materials from www.rfmd.com.)

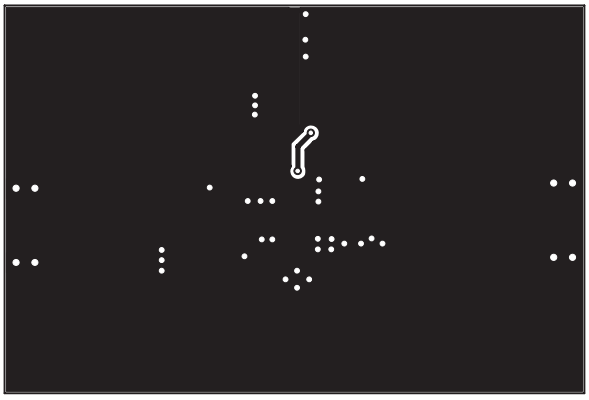


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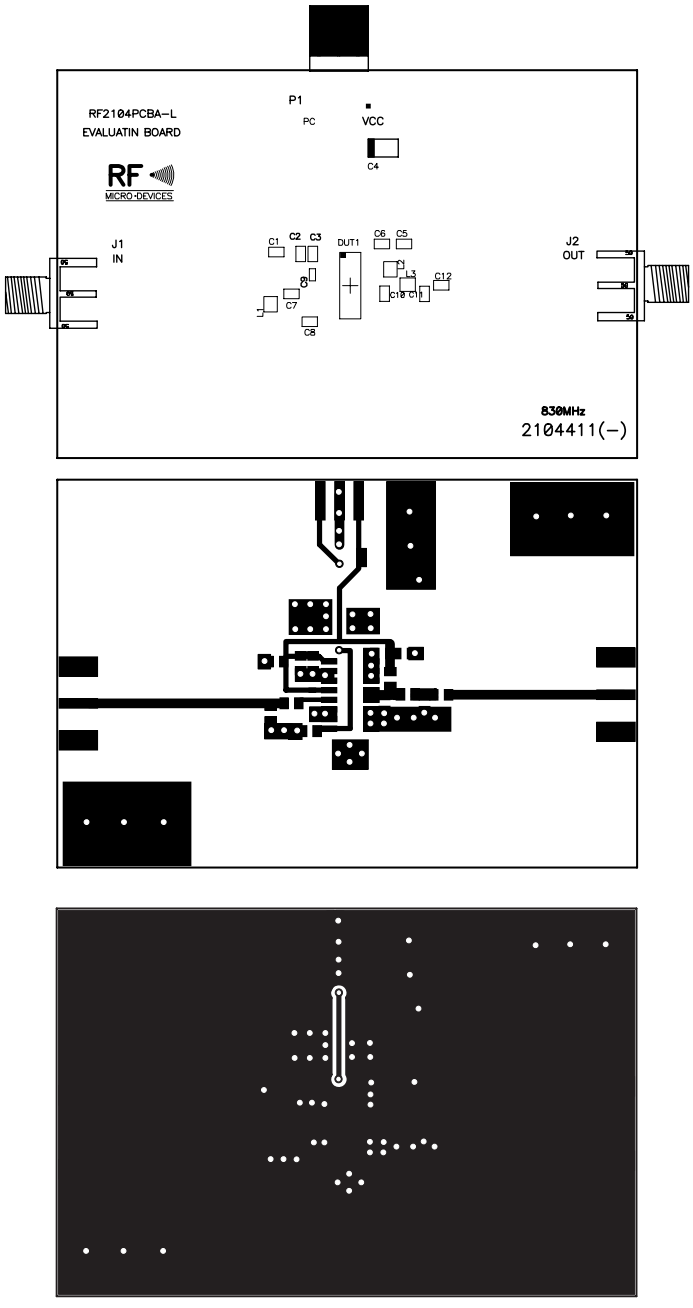
Evaluation Board Layout
915MHz
3" x 2"







Evaluation Board Layout
830MHz
3" x 2"



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MICRO·DEVICES

RF2105L

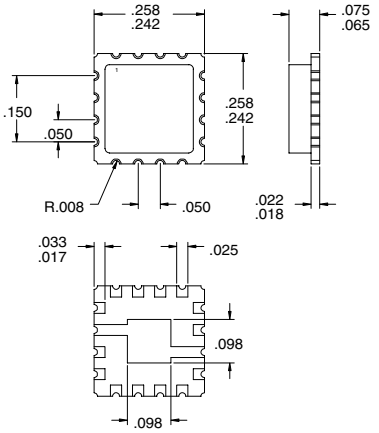
HIGH POWER LINEAR UHF AMPLIFIER

Typical Applications

- 900 MHz ISM Band Applications
- 400 MHz Industrial Radios
- Digital Communication Systems
- Driver Stage for Higher Power Applications
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

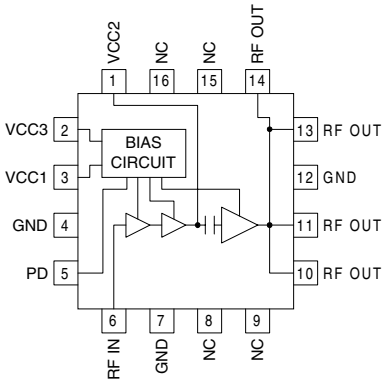
The RF2105L is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in digital cellular phone transmitters or ISM applications requiring linear amplification. It is packaged in a 16-lead ceramic package with a backside ground. The device is self-contained with the exception of the output matching network and power supply feed line.



Package Style: QLCC-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2.7V to 6.5V Supply
- Up to 1.2W CW Output Power
- 33dB Small Signal Gain
- 48% Efficiency
- Digitally Controlled Power Down Mode
- Small Package Outline (0.25" x 0.25")

Ordering Information

RF2105L	High Power Linear UHF Amplifier
RF2105L PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2105L

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +8.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +6.5	V_{DC}
DC Supply Current	700	mA
Input RF Power	+12	dBm
Output Load	20:1	
Operating Case Temperature	-40 to +100	°C
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5.8V, V_{PD}=5.8V, Z_{LOAD}=9Ω, P_{IN}=0dBm, Freq=840MHz
Frequency Range		430 to 930		MHz	
Maximum CW Output Power		+30.8		dBm	V_{CC}=5.8V, V_{PD}=5.8V, Z_{LOAD}=9Ω
					Note that increasing V_{CC} above 5.8V does not result in higher output power; power may actually decrease.
		+29.3		dBm	V_{CC}=5.0V, V_{PD}=5.0V, Z_{LOAD}=9Ω
		+28.5		dBm	V_{CC}=4.4V, V_{PD}=4.4V, Z_{LOAD}=9Ω
		+30		dBm	V_{CC}=5.8V, V_{PD}=5.8V, Z_{LOAD}=12Ω
		+27.8		dBm	V_{CC}=5.0V, V_{PD}=5.0V, Z_{LOAD}=12Ω
		+27		dBm	V_{CC}=4.4V, V_{PD}=4.4V, Z_{LOAD}=12Ω
CW Efficiency at Max Output		48		%	
DC Current at Max Output		450		mA	
Small-signal Gain		33		dB	
Second Harmonic		-23		dBc	Without external second harmonic trap
Third Harmonic		-36		dBc	
Fourth Harmonic		-35		dBc	
Input VSWR		<2:1			With external matching network; see application schematic
Input Impedance		50		Ω	With external matching network; see application schematic
Two-Tone Specification					
Average Two-Tone Power		+27.0		dBm	PEP-3dB
IM_3		-30	-25	dBc	P_{OUT}=+24.0dBm/tone
IM_5		-32	-30	dBc	P_{OUT}=+24.0dBm/tone
IM_7		-40		dBc	P_{OUT}=+24.0dBm/tone
Two-Tone Current Drain	225	260	350	mA	
Two-Tone Power-Added Eff.		33		%	
Power Control					
Power Down "ON"		V_{CC}		V	Voltage supplied to the input
Power Down "OFF"		0		V	Voltage supplied to the input
PD Input Current		3.7	5.0	mA	Only in "ON" state
Power Supply					
Power Supply Voltage		2.7 to 6.5		V_{DC}	
Total Idle Current Drain		2	10	μA	V_{PD}<0.1V_{DC}, V_{CC}=6.5V
		60		mA	V_{PD}=4.4V_{DC}, V_{CC}=6.5V
		80		mA	V_{PD}=5.0V_{DC}, V_{CC}=6.5V
	80	100	165	mA	V_{PD}=5.8V_{DC}, V_{CC}=6.5V
		120		mA	V_{PD}=6.5V_{DC}, V_{CC}=6.5V

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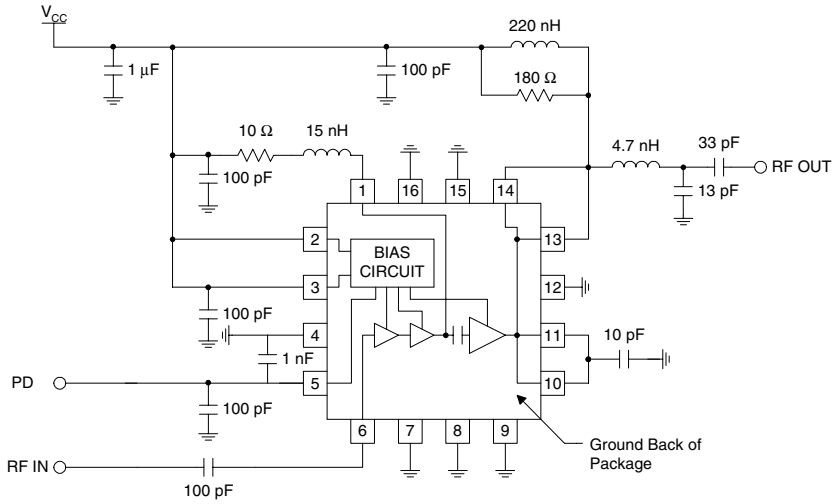
Pin	Function	Description	Interface Schematic
1	VCC2	Positive supply for the second stage (driver) amplifier. This is an unmatched transistor collector output. This pin should see an inductive path to AC ground (V_{CC} with a UHF bypassing capacitor). This inductance can be achieved with a short, thin microstrip line or with a low value chip inductor (~2.7nH). At lower frequencies, the inductance value should be larger (longer microstrip line) and V_{CC} should be bypassed with a larger bypass capacitor (see the application schematic for 430MHz operation). This inductance forms a matching network with the internal series capacitor between the second and third stages, setting the amplifier's frequency of maximum gain. An additional 1µF bypass capacitor in parallel with the UHF bypass capacitor is also recommended, but placement of this component is not as critical. In most applications, pins 1, 2, and 3 can share a single 1µF bypass capacitor.	
2	VCC3	Positive supply for the active bias circuits. This pin can be externally combined with pin 3 (VCC1) and the pair bypassed with a single UHF capacitor, placed as close as possible to the package. Additional bypassing of 1µF is also recommended, but proximity to the package is not as critical. In most applications, pins 1, 2, and 3 can share a single 1µF bypass capacitor.	
3	VCC1	Positive supply for the first stage (input) amplifier. This pin can be externally combined with pin 2 (VCC3) and the pair bypassed with a single UHF capacitor, placed as close as possible to the package. Additional bypassing of 1µF is also recommended, but proximity to the package is not as critical. In most applications, pins 1, 2, and 3 can share a single 1µF bypass capacitor.	
4	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. In addition, for specified performance, the package's backside metal should be soldered to ground plane.	
5	PD	Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at V_{CC} (3V to 6.5V), the device will be in full power mode delivering maximum available gain and output power capability. This pin may also be used to perform some degree of gain control or power control when set to voltages between 0V and V_{CC}. It is not optimized for this function so the transfer function is not linear over a wide range as with other devices specifically designed for analog gain control; however, it may be usable for coarse adjustment or in some closed loop AGC systems. This pin should not, in any circumstance, be higher in voltage than V_{CC}, nor should it ever be higher than 6.5V. This pin should also have an external UHF bypassing capacitor.	
6	RF IN	Amplifier RF input. This is a 50Ω RF input port to the amplifier. It does not contain internal DC blocking and therefore should be externally DC blocked before connecting to any device which has DC present or which contains a DC path to ground. A series UHF capacitor is recommended for the DC blocking.	
7	GND	Same as pin 4.	
8	NC	Not internally connected.	
9	NC	Not internally connected.	

RF2105L

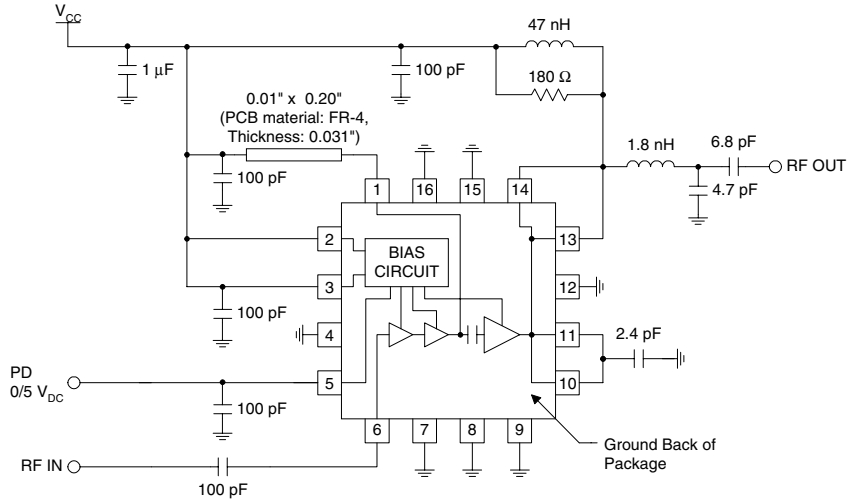
Pin	Function	Description	Interface Schematic
10	RF OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 10, 11, 13, and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through two of these four pins. Typically, pins 10 and 11 are connected to a network that creates a second harmonic trap. For 830MHz operation, this network is simply a single 2.4pF capacitor from both pins to ground. This capacitor series resonates with internal bond wires at two times the operating frequency, effectively shorting out the second harmonic. Shorting out this harmonic serves to increase the amplifier's maximum output power and efficiency, as well as to lower the level of the second harmonic output. Typically, pins 13 and 14 are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output. An additional network of a bias inductor and parallel resistor provides DC bias and helps to protect the output from high voltage swings due to severe load mismatches. Shunt protection diodes are included to clip peak voltage excursions above ~15V to prevent voltage breakdown in worst case conditions.	
11	RF OUT	Same as pin 10.	
12	GND	Same as pin 4.	
13	RF OUT	Same as pin 10.	
14	RF OUT	Same as pin 10.	
15	NC	Not internally connected.	
16	NC	Not internally connected.	
Pkg Base	GND	This contact is the main ground contact for the entire device. Care should be taken to ensure that this contact is well soldered in order to prevent performance from being degraded from that indicated in the specifications.	

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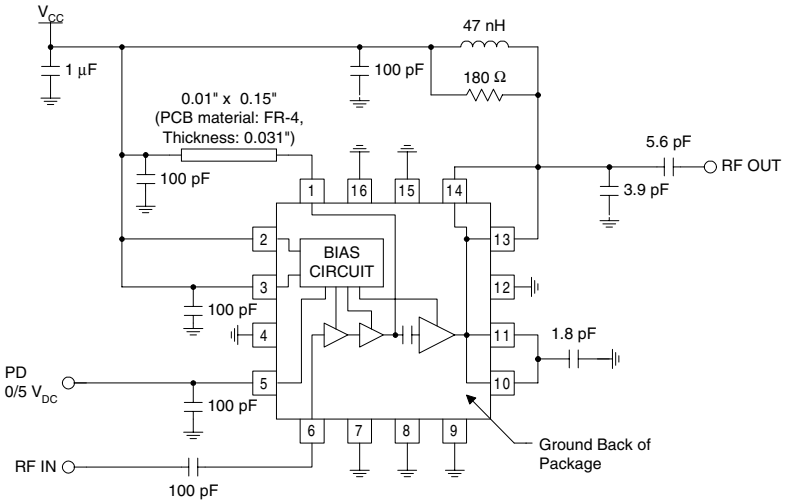
Application Schematic for 430MHz Operation



Application Schematic for 840MHz Operation

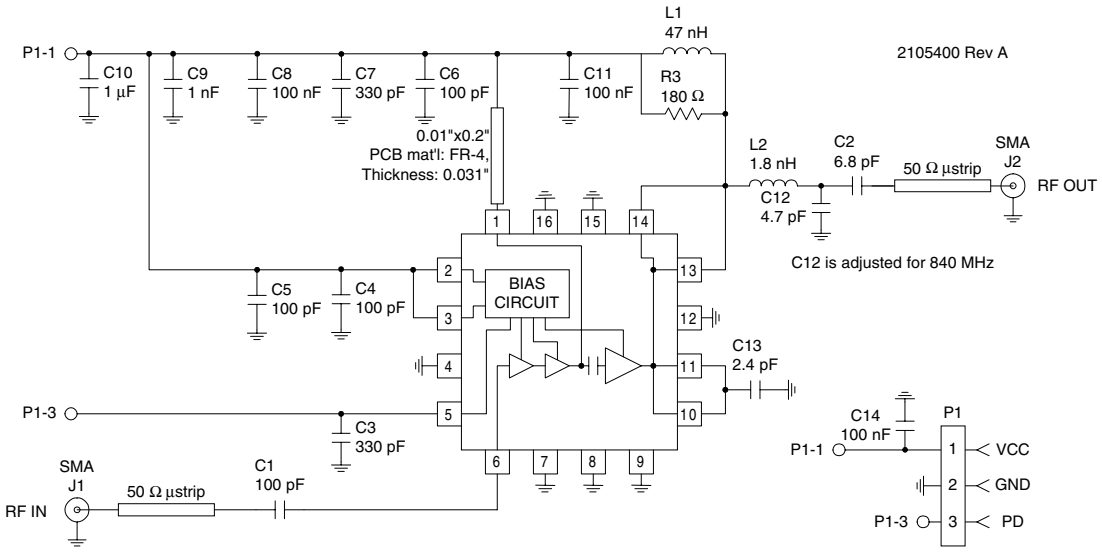


Application Schematic for 915MHz Operation

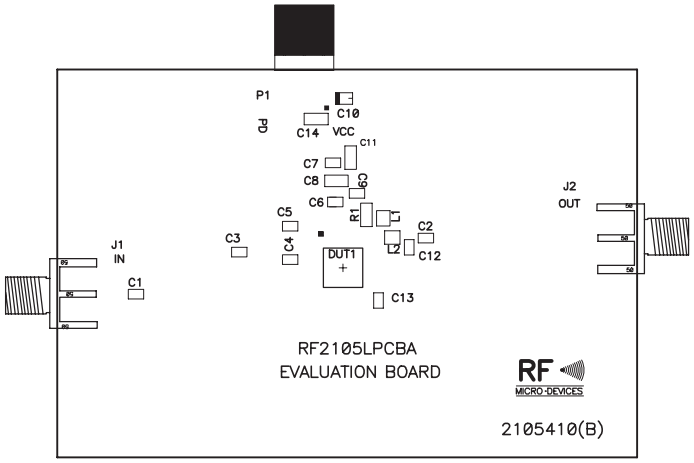


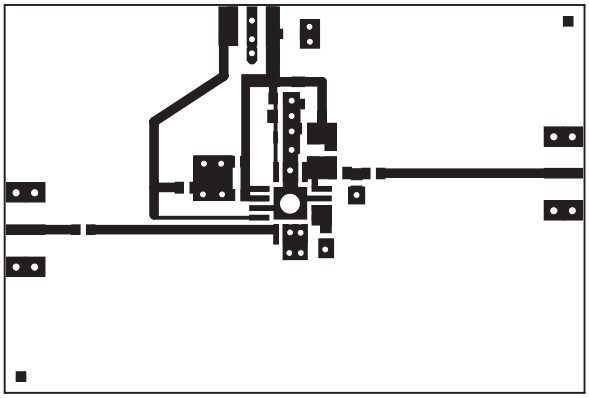
Evaluation Board Schematic (840MHz)

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 3”





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RF2108

LINEAR POWER AMPLIFIER

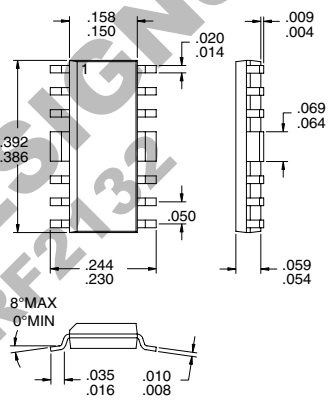
Typical Applications

- 4.8V AMPS Cellular Handsets
- 4.8V CDMA/AMPS Cellular Handsets
- Driver Amplifier in Cellular Base Stations
- Portable Battery Powered Equipment

NOT FOR NEW DESIGNS
See Upgraded Product RF2132

Product Description

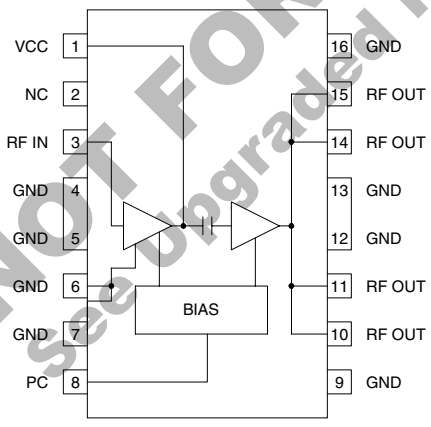
The RF2108 is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 4-cell CDMA/AMPS hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 950MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics.



Package Style: SOP-16 Batwing

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 4.2V to 6.0V Supply
- 28dBm Linear Output Power
- 29dB Gain With Analog Gain Control
- 45% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 950MHz Operation

Ordering Information

RF2108	Linear Power Amplifier
RF2108 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2108

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V_{DC}
Supply Voltage (P_{OUT}<31dBm)	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +6.0 or V_{CC}	V
DC Supply Current	800	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Storage Temperature	-40 to +150	°C
Junction Temperature	200	°C

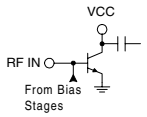
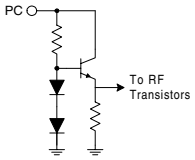
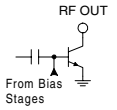
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.8V, V_{PC}=3.3V, Freq=824MHz to 849MHz
Usable Frequency Range	800	824 to 849	950	MHz	
Linear Gain	27	29	31	dB	
Total Linear Efficiency	40	45		%	
Efficiency at Max Output	50	55		%	
OFF Isolation	23	27		dB	V_{PC}=0V,P_{IN}=+6dBm
Second Harmonic		-30		dBc	Including Second Harmonic Trap
Maximum Linear Output Power		28.5	29		IS-95A CDMA Modulation
Adjacent Channel Power Rejection @ 885 kHz		-46	-44	dBc	Pout = 28 dBm ACPR can be improved by trading off efficiency.
Adjacent Channel Power Rejection @ 1.98 MHz		-58	-56	dBc	Pout = 28 dBm
Maximum CW Output Power	31.5	32		dBm	
Operating Case Temperature	-30		110	°C	Pout = 31 dBm, Efficiency = 55%
Ambient Operating Temperature	-30		100	°C	
Junction to Case Thermal Resistance		85		°C/W	
Input VSWR		<2:1			
Output Load VSWR			10:1		No oscillations
Power Down					
Turn On/Off Time			100	ns	
Total Current			10	µA	"OFF" State
V_{PC} "OFF" Voltage	0.2		0.5	V	
V_{PC} "ON" Voltage	3.0	3.3	Vcc	V	
Power Supply					
Power Supply Voltage	4.2	4.8	6.0	V	Operating voltage
Idle Current		40	160	mA	V_{PC}=3.3V
Current into VPC pin		15	20	mA	"ON" State

NOT FOR NEW DESIGNS
See Upgraded Product RF2132

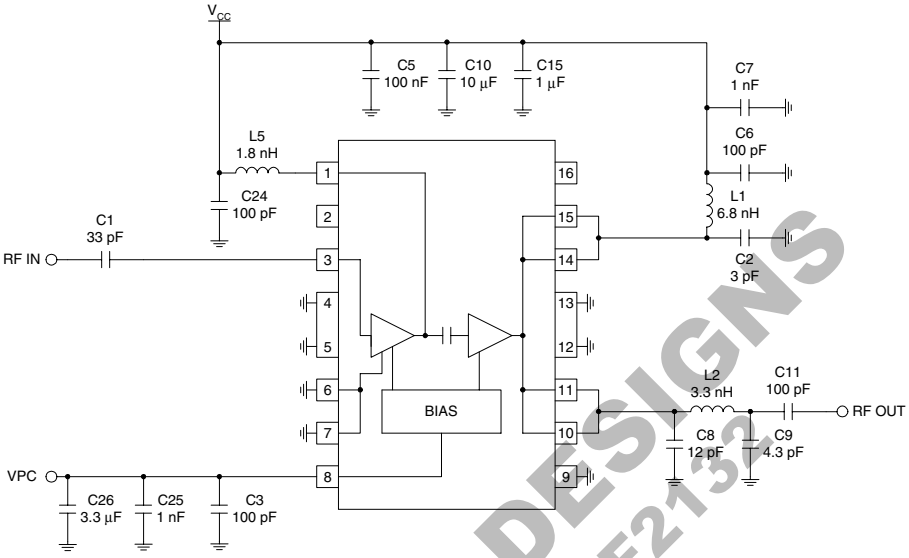
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Pin	Function	Description	Interface Schematic
1	VCC	Power supply for the driver stage, and interstage matching. Shunt inductance is required on this pin, which can be achieved by an inductor to V_{CC}, with a decoupling capacitor on the V_{CC} side. The value of the inductor is frequency dependent, 3.3nH is required for 830MHz, and 1.2nH for 950MHz. Instead of an inductor, a high impedance microstrip line can be used.	
2	NC	Not connected.	
3	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
4	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
5	GND	Same as pin 4.	
6	GND	Same as pin 4.	
7	GND	Same as pin 4.	
8	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V or less at room temperature. During normal operation this pin is the power control. Control range varies from about 2V for 0dBm to V_{CC} for +31dBm RF output power. The maximum power that can be achieved depends on the actual output matching. PC should never exceed 6.0V or V_{CC}, whichever is the lowest.	
9	GND	Same as pin 4.	
10	RF OUT	RF output and power supply for the output stage. The four output pins are combined, and bias voltage for the final stage is provided through these pins. The external path must be kept symmetric until combined to ensure stability. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
11	RF OUT	Same as pin 10.	See pin 10.
12	GND	Same as pin 4.	
13	GND	Same as pin 4.	
14	RF OUT	Same as pin 10.	See pin 10.
15	RF OUT	Same as pin 10.	See pin 10.
16	GND	Same as pin 4.	

NOT FOR NEW DESIGNS
See Upgraded Product RF2132

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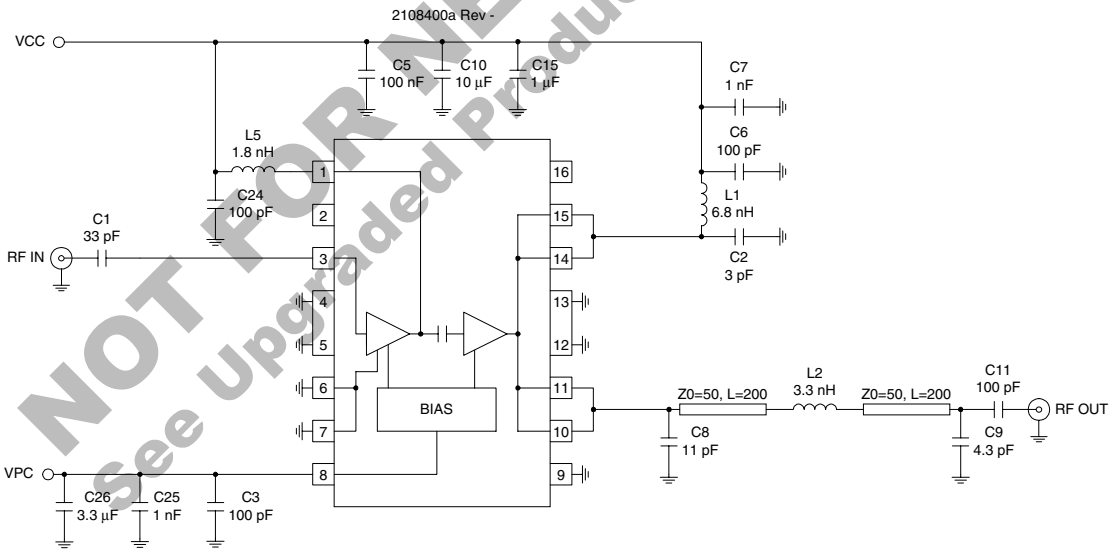
Application Schematic



NOT FOR NEW DESIGNS
See Upgraded Product RF2132

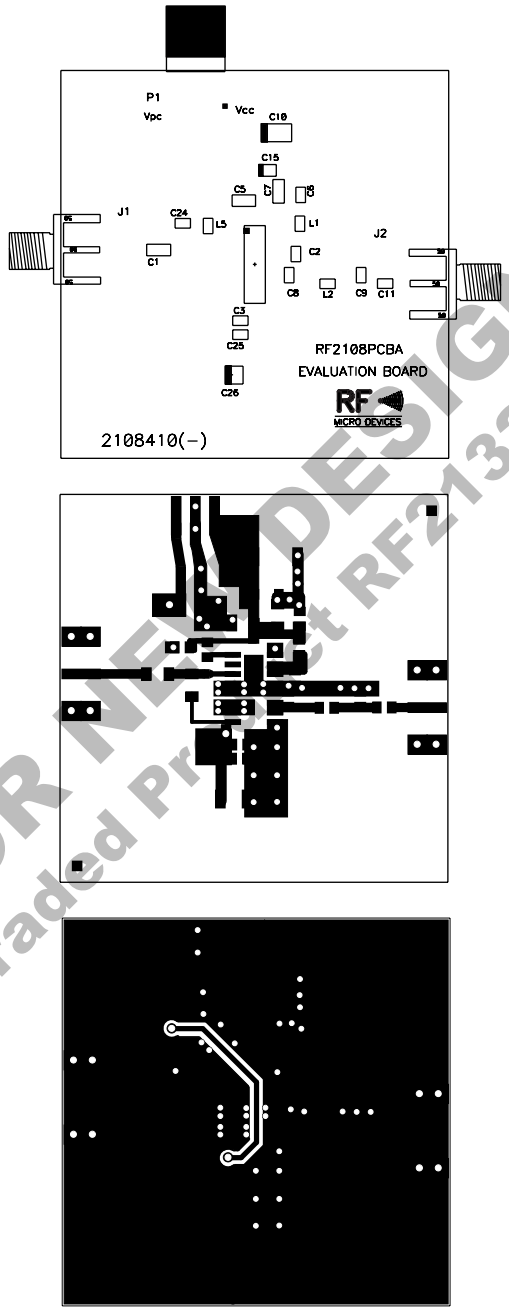
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout



NOT FOR NEW DESIGNS
See Upgraded Product RF2132

RF2108

NOT FOR NEW DESIGNS
See Upgraded Product RF2132

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RF2114

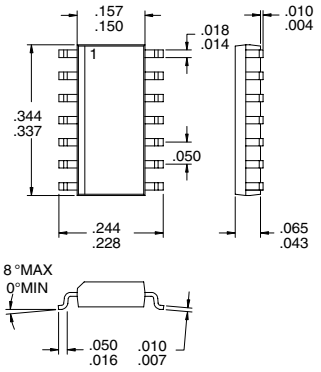
MEDIUM POWER LINEAR AMPLIFIER

Typical Applications

- Digital Communication Systems
- Spread Spectrum Communication Systems
- Driver for Higher Power Linear Applications
- Portable Battery Powered Equipment
- Commercial and Consumer Systems
- Base Station Equipment

Product Description

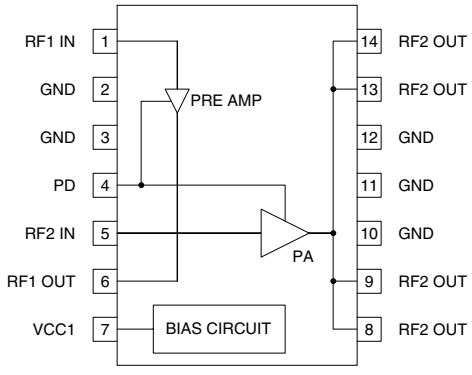
The RF2114 is a medium to high power linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final linear RF amplifier in UHF radio transmitters operating between 1MHz and 600MHz. It may also be used as a driver amplifier in higher power applications. The device is self-contained with the exception of the output matching network, power supply feed line, and bypass capacitors. The device can be used in 3-cell battery applications. The maximum CW output at 3V is 125mW. The unit has a total gain of 35dB, depending upon the output matching network.



Package Style: SOP-14

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 1MHz to 600MHz Operation
- Over 800mW CW Output Power
- 35dB Small Signal Gain
- Single 2.7V to 6.5V Supply
- 45% Efficiency
- Digitally Controlled Power Down Mode

Ordering Information

RF2114	Medium Power Linear Amplifier
RF2114 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2114

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5.0	V
DC Supply Current	350	mA
Input RF Power	+12	dBm
Output Load VSWR	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

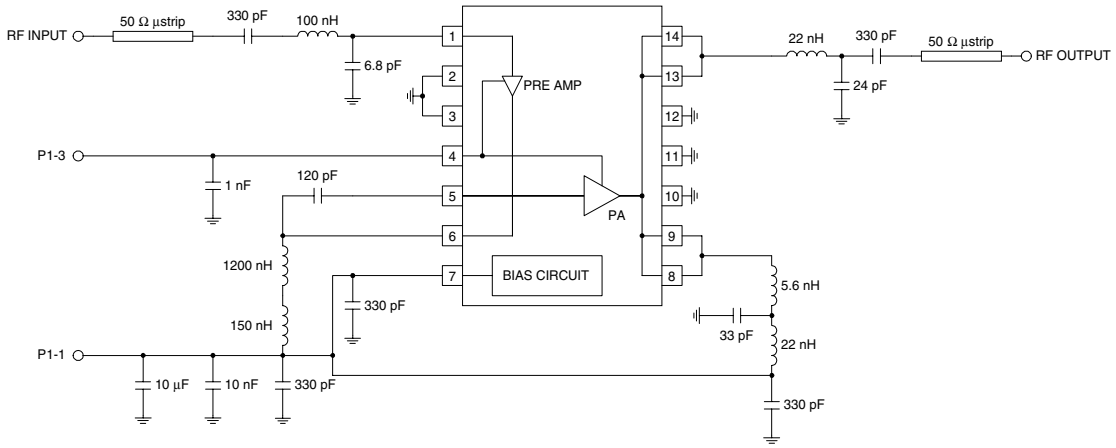
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5.8V, V_{PD}=4.0 V, Z_{LOAD}=18Ω, P_{IN}=0dBm, Freq=150MHz
Frequency Range		1 to 600		MHz	
Saturated Output Power	+28	+28.5	+29.5	dBm	
Output Power		>+27		dBm	Frequency>450MHz
Power Gain	30	36	40	dB	
CW Total Efficiency		45		%	
Two Tone Total Efficiency		26		%	P_{OUT} = +18.5dBm/tone
IM_3	-50	-40	-25	dBc	P_{OUT} = +18.5dBm/tone
IM_5	-70	-43	-30	dBc	P_{OUT} = +18.5dBm/tone
Second Harmonic		-24		dBc	Without external second harmonic trap
Third Harmonic		-30		dBc	
Output Noise Power		<-125		dBm/Hz	
Input VSWR		<3:1			With external matching network; see application schematic
Input Impedance		50		Ω	With external matching network; see application schematic
Load Impedance		18+j0		Ω	Load impedance for optimal match
Power Down Control					
Power Down "ON"		V_{CC}		V	Voltage supplied to the input; Part is "ON"
Power Down "OFF"	0		0.2	V	Voltage supplied to the input; Part is "OFF"
Power Supply					
Power Supply Voltage		2.7 to 6.5		V	
Power Supply Idle Current		45	80	mA	
Supply Current	150	175	250	mA	Total of pins 5 and 6
V_{PD} Current		< 3.5		mA	Into pin 4
Total "OFF" Current Drain			10	µA	V_{PD} < 0.1 V_{DC}
Turn-on Time		<100		ns	V_{PD}=0 to V_{PD}=+4 V_{DC}

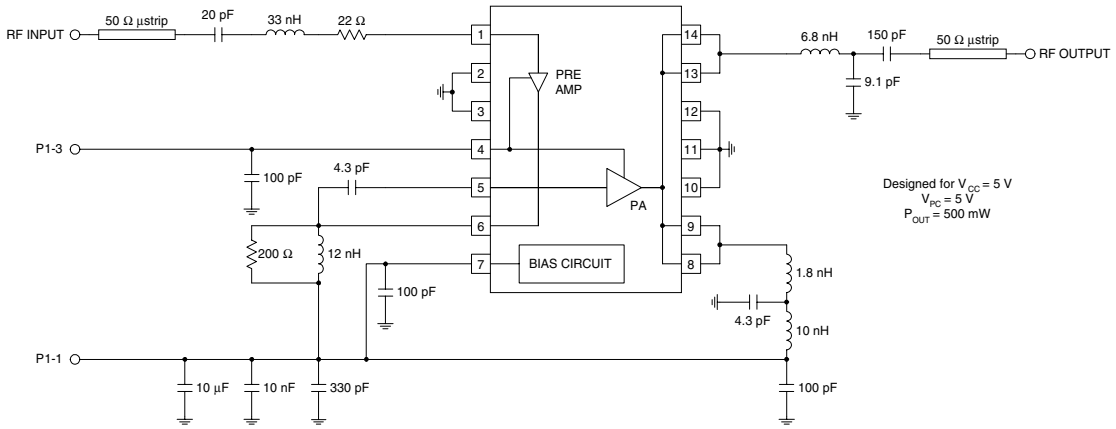
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Pin	Function	Description	Interface Schematic
1	RF1 IN	RF input pin. This pin is internally connected to the bias circuits. An external DC blocking capacitor is required. The value of this capacitor depends on the actual operating frequency.	
2	GND	Ground connection. Keep the connection to the backside ground plane as short as possible, by placing the vias close to the pin.	
3	GND	Same as pin 2.	
4	PD	Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at V_{CC} (but not higher than 5.0V max), the device will be in full power mode delivering maximum gain and output power capability. This pin may also be used to perform some degree of gain control or power control when set to voltages between 0V and V_{CC} or 5.0V, whichever is the lowest. It is not optimized for this function so the transfer function is not linear over a wide range as with other devices specifically designed for analog gain control. However, it may be usable for coarse adjustment or in some closed loop AGC systems. This pin should not, in any circumstance, be higher in voltage than V_{CC}. This pin should also have an external bypassing capacitor.	
5	RF2 IN	RF input of the power stage. This pin is internally connected to the bias circuits. An external DC blocking capacitor is required. This same capacitor can also be used for interstage matching. Typically this capacitor is between RF2 IN (pin 5) and RF1 OUT (pin 6); see the application schematics for details.	
6	RF1 OUT	RF output of the pre-amplifier. Power supply needs to be supplied to this pin through an inductor to V_{CC}. Together with the series capacitor between pin 5 and 6 the interstage matching circuit is formed. See the application schematics for values for different frequencies.	
7	VCC1	Positive supply for the active bias circuits. This needs to be bypassed with a single capacitor, placed as close as possible to the package. Additional bypassing of 1µF is also recommended, but proximity to the package is not as critical.	
8	RF2 OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. Pins 8, 9, 13, and 14 are connected internally. Bias for the final power amplifier output transistor must also be provided through one of these two pins. Typically, pins 8 and 9 are connected to a network that provides the DC bias and also creates a second harmonic trap. A capacitor series resonates with internal bond wires and some additional series inductance, and acts as a trap at two times the operating frequency, effectively shorting out the second harmonic. Shorting out this harmonic serves to increase the amplifier's maximum output power and efficiency, as well as to lower the level of the second harmonic output. Typically, pins 13 and 14 are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output.	
9	RF2 OUT	Same as pin 8.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	GND	Same as pin 2.	
13	RF2 OUT	Same as pin 8.	
14	RF2 OUT	Same as pin 8.	

Application Schematic for 150MHz Operation



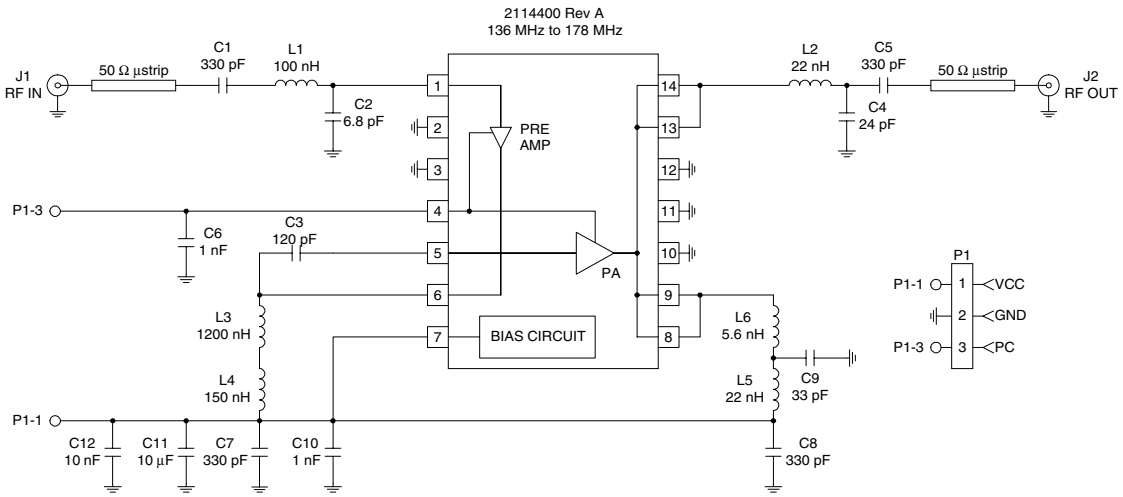
Application Schematic for 450MHz Operation



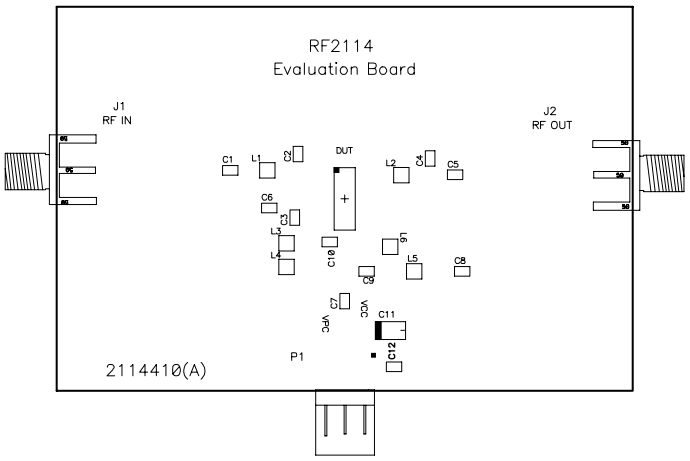
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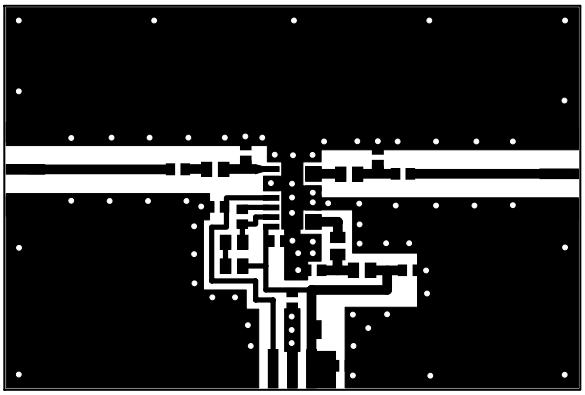
Evaluation Board Schematic (150MHz)

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 3”





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RF2115L

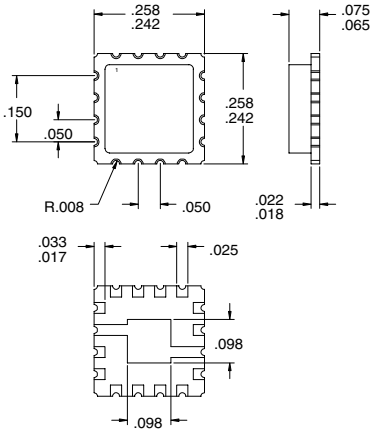
HIGH POWER UHF AMPLIFIER

Typical Applications

- Analog Communication Systems
- Analog Cellular Systems (AMPS & TACS)
- 900MHz Spread Spectrum Systems
- 400MHz Industrial Radios
- Driver Stage for Higher Power Applications
- Portable Battery Powered Equipment

Product Description

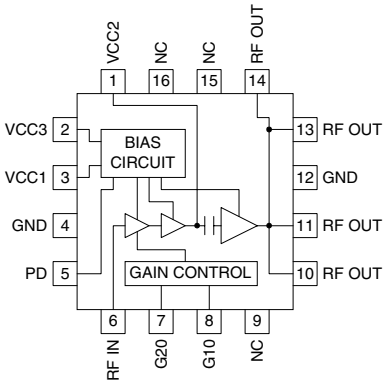
The RF2115L is a high power amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in analog cellular phone transmitters or ISM applications operating at 915MHz. The device is packaged in a 16-lead ceramic quad leadless chip carrier with a backside ground. The device is self-contained with the exception of the output matching network and power supply feed line. A two-bit digital control provides 4 levels of power control, in 10dB steps.



Package Style: QLCC-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 5V to 6.5V Supply
- Up to 1.0W CW Output Power
- 33dB Small Signal Gain
- 48% Efficiency
- Digitally Controlled Output Power
- Small Package Outline (0.25" x 0.25")

Ordering Information

RF2115L	High Power UHF Amplifier
RF2115L PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2115L

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +8.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5.0	V
Control Voltage (G10, G20)	-0.5 to +5.5	V
DC Supply Current	700	mA
Input RF Power	+12	dBm
Output Load	20:1	
Operating Case Temperature	-40 to +100	°C
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition	
	Min.	Typ.	Max.			
Overall					T=25°C, V_{CC}=5.8V, V_{PD}=5.0V, Z_{LOAD}=9Ω, P_{IN}=0dBm, Freq=840MHz	
Frequency Range		430 to 930		MHz		
Maximum CW Output Power		+30.5		dBm	Note that increasing V_{CC} does not result in higher output power; power may actually decrease.	
		+30		dBm	V_{CC}=5.8V, Z_{LOAD}=12Ω	
		+29.5		dBm	V_{CC}=5.0V, Z_{LOAD}=9Ω	
		+28.5		dBm	V_{CC}=5.0V, Z_{LOAD}=12Ω	
Total CW Efficiency at Maximum Output	40	48		%		
Small-signal Gain		33		dB		
Second Harmonic		-23		dBc	Without external second harmonic trap	
Third Harmonic		-36		dBc		
Fourth Harmonic		-35		dBc		
Input VSWR		<2:1				
Input Impedance		50		Ω		
Power Control					G20	G10
Output Power	+30	+30.5	+36	dBm	1	1
	+17	+20	+23	dBm	1	0
	+7	+11	+13	dBm	0	1
	-4	+2.5	+6	dBm	0	0
Power Supply Current	350	415	600	mA	1	1
	75	125	175	mA	1	0
	35	56	90	mA	0	1
	21	38	50	mA	0	0
Idle Current	30	55	80	mA	1	1
Power Down "ON"		5.0		V	Voltage supplied to the input; Part is "ON"	
Power Down "OFF"	0		0.2	V	Voltage supplied to the input; Part is "OFF"	
Power Down Control						
Power Down "ON"		5.0		V	Voltage supplied to the input; Part is "ON"	
Power Down "OFF"	0		0.2	V	Voltage supplied to the input; Part is "OFF"	
Current Drain		1	10	µA	V_{PD} < 0.1 V_{DC}	

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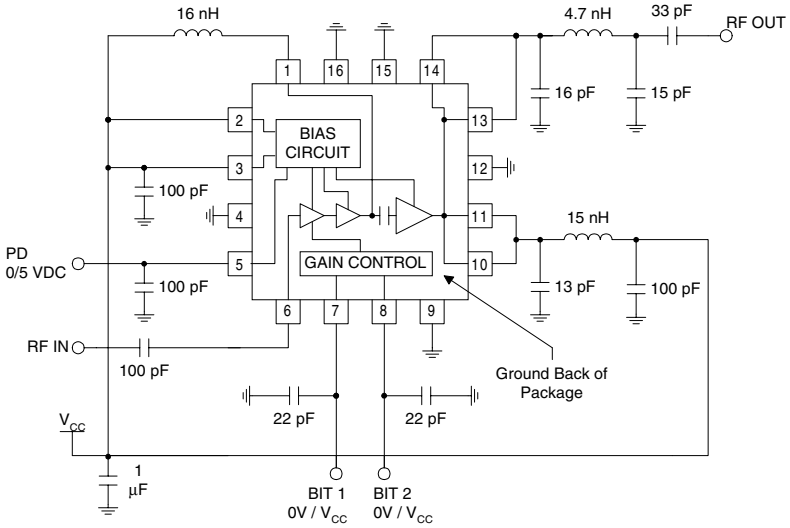
Pin	Function	Description	Interface Schematic
1	VCC2	Positive supply for the second stage (driver) amplifier. This is an unmatched transistor collector output. This pin should see an inductive path to AC ground (V_{CC} with a UHF bypassing capacitor). This inductance can be achieved with a short, thin microstrip line or with a low value chip inductor (approximately 2.7nH). At lower frequencies, the inductance value should be larger (longer microstrip line) and V_{CC} should be bypassed with a larger bypass capacitor (see the application schematic for 430MHz operation). This inductance forms a matching network with the internal series capacitor between the second and third stages, setting the amplifier's frequency of maximum gain. An additional 1μF bypass capacitor in parallel with the UHF bypass capacitor is also recommended, but placement of this component is not as critical. In most applications, pins 1, 2, and 3 can share a single 1μF bypass capacitor.	
2	VCC3	Positive supply for the active bias circuits. This pin can be externally combined with pin 3 (VCC1) and the pair bypassed with a single UHF capacitor, placed as close as possible to the package. Additional bypassing of 1μF is also recommended, but proximity to the package is not as critical. In most applications, pins 1, 2, and 3 can share a single 1μF bypass capacitor.	
3	VCC1	Positive supply for the first stage (input) amplifier. This pin can be externally combined with pin 2 (VCC3) and the pair bypassed with a single UHF capacitor, placed as close as possible to the package. Additional bypassing of 1μF is also recommended, but proximity to the package is not as critical. In most applications, pins 1, 2, and 3 can share a single 1μF bypass capacitor. This pin can also be used for coarse analog gain control, even though it is not optimized for this function.	
4	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. In addition, for specified performance, the package's backside metal should be soldered to ground plane.	
5	PD	Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at 5V the device will be in full power mode delivering maximum available gain and output power capability. This pin may also be used to perform some degree of gain control or power control when set to voltages between 0V and 5V. It is not optimized for this function so the transfer function is not linear over a wide range as with other devices specifically designed for analog gain control; however, it may be usable for coarse adjustment or in some closed loop AGC systems. This pin should not, in any circumstance, be higher in voltage than V_{CC}, nor should it ever be higher than 6.5V. This pin should also have an external UHF bypassing capacitor.	
6	RF IN	Amplifier RF input. This is a 50Ω RF input port to the amplifier. It does not contain internal DC blocking and therefore should be externally DC blocked before connecting to any device which has DC present or which contains a DC path to ground. A series UHF capacitor is recommended for the DC blocking.	
7	G20	RF output power gain control MSB (see specification table for logic). The control voltage at this pin should never exceed V_{CC}. This pin should also have an external UHF bypassing capacitor.	
8	G10	RF output power gain control LSB (see specification table for logic). The control voltage at this pin should never exceed V_{CC}. This pin should also have an external UHF bypassing capacitor.	
9	NC	Not internally connected.	

RF2115L

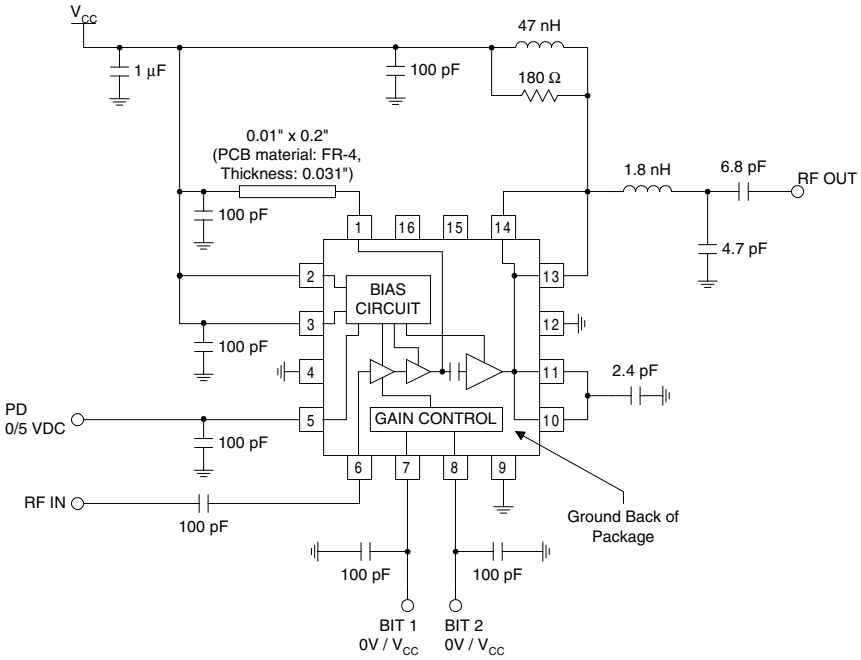
Pin	Function	Description	Interface Schematic
10	RF OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 10, 11, 13, and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through two of these four pins. Typically, pins 10 and 11 are connected to a network that creates a second harmonic trap. For 830MHz operation, this network is simply a single 2.4pF capacitor from both pins to ground. This capacitor series resonates with internal bond wires at two times the operating frequency, effectively shorting out the second harmonic. Shorting out this harmonic serves to increase the amplifier's maximum output power and efficiency, as well as to lower the level of the second harmonic output. Typically, pins 13 and 14 are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output. An additional network of a bias inductor and parallel resistor provides DC bias and helps to protect the output from high voltage swings due to severe load mismatches. Shunt protection diodes are included to clip peak voltage excursions above approximately 15V to prevent voltage breakdown in worst case conditions.	
11	RF OUT	Same as pin 10.	
12	GND	Same as pin 4.	
13	RF OUT	Same as pin 10.	
14	RF OUT	Same as pin 10.	
15	NC	Not internally connected.	
16	NC	Not internally connected.	
Pkg Base	GND	This contact is the main ground contact for the entire device. Care should be taken to ensure that this contact is well soldered in order to prevent performance from being degraded from that indicated in the specifications.	

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Application Schematic 430MHz

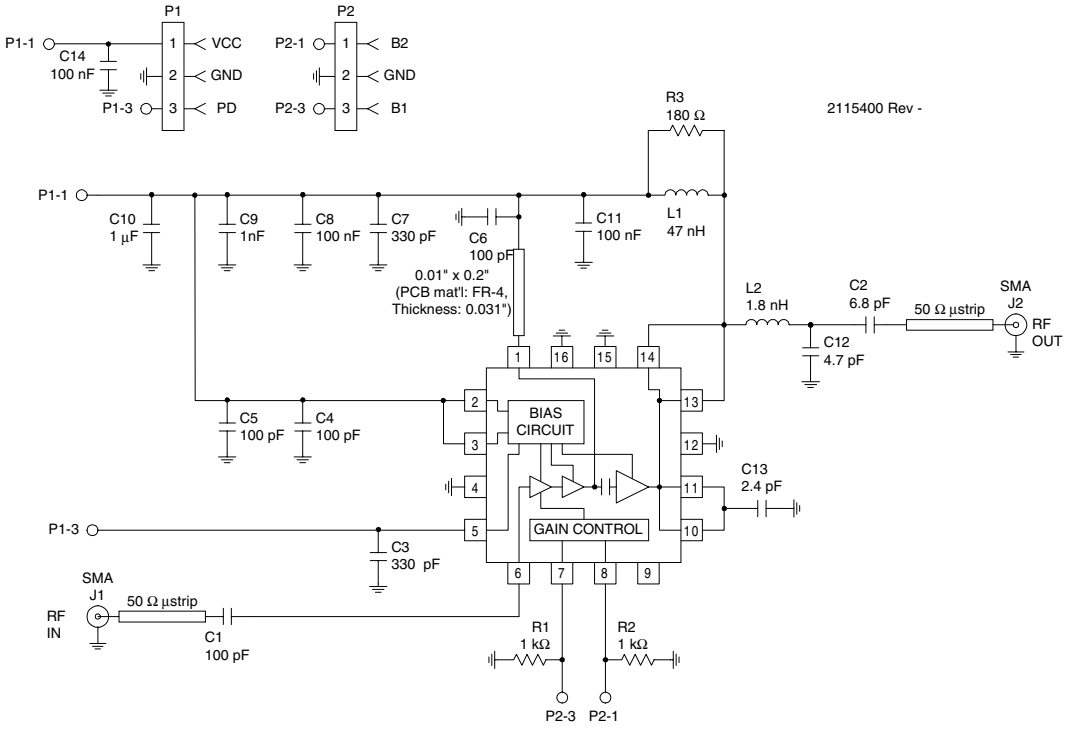


Application Schematic 840MHz

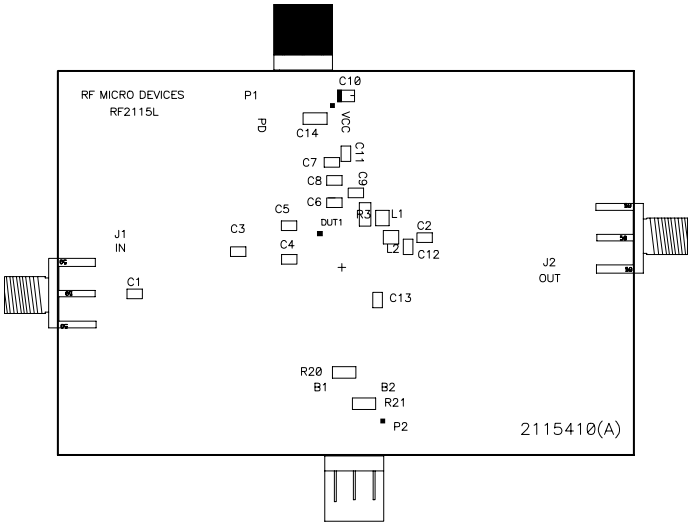


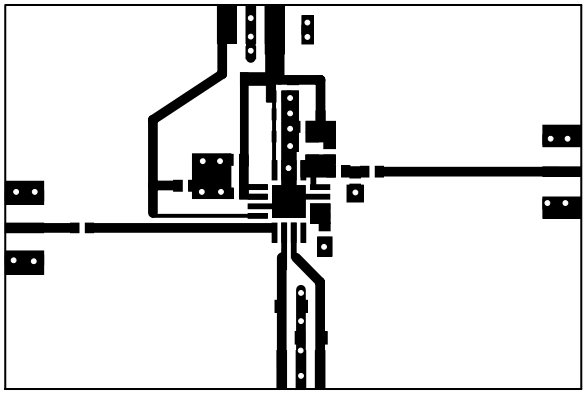
Evaluation Board Schematic
840MHz Operation

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 3”





RF2115L

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Preliminary

RF2117

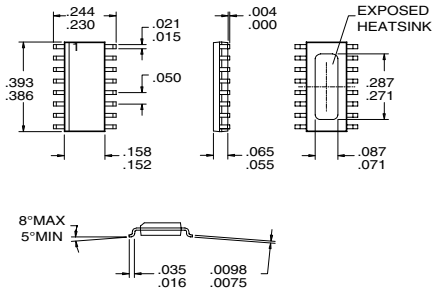
HIGH EFFICIENCY 400MHZ AMPLIFIER

Typical Applications

- 3.6V Analog Handsets
- Analog Communication Systems
- 400MHz Industrial Radios
- Portable Battery Powered Equipment

Product Description

The RF2117 is a high power amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in analog cellular phone transmitters between 400MHz and 500MHz or ISM applications operating at 433MHz. The device is packaged in a low cost 16-lead plastic package with a metal backside. The device is self-contained with the exception of the output matching network and power supply feed line.

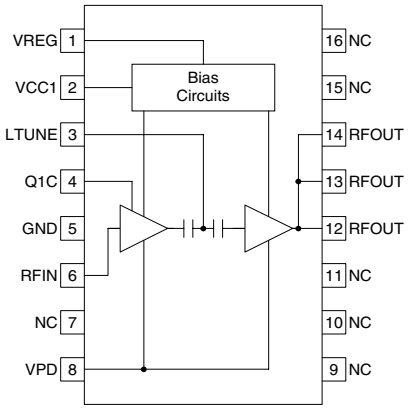


Package Weight
typically 0.22 grams

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: PSOP-16



Functional Block Diagram

Features

- Single 3V to 5.5V Supply
- Up to 2W CW Output Power
- 33dB Small Signal Gain
- >50% Efficiency
- 400MHz to 500MHz Operation

Ordering Information

RF2117	High Efficiency 400MHz Amplifier
RF2117 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +6.0	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +3.0	V
DC Supply Current	1300	mA
Input RF Power	+10	dBm
Output Load	7:1	
Operating Case Temperature	-40 to +100	°C
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

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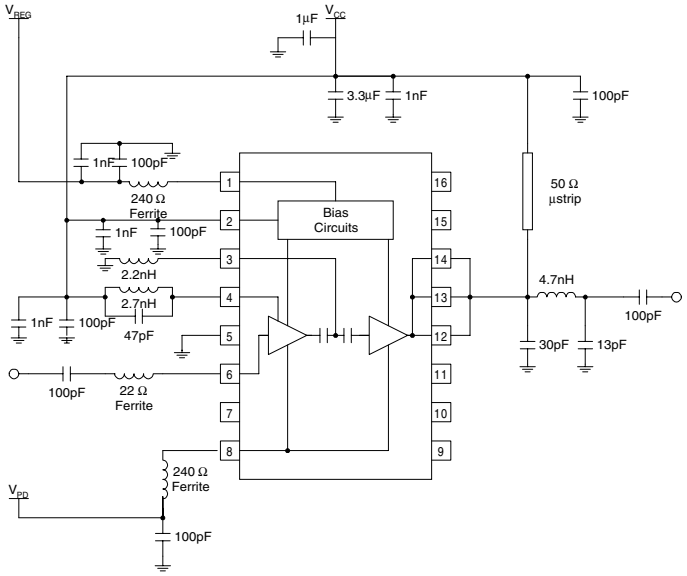
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, V_{PD}=2.2V, Z_{LOAD}=2.7Ω, P_{IN}=4dBm, Freq=450MHz
Frequency Range		400 to 500		MHz	
Maximum CW Output Power		+33		dBm	
	+32.5			dBm	V_{CC}=3.2 to 4.5V Tamb=-25 to +85 °C
	+31.5			dBm	V_{CC}=3.0 to 3.2V and 4.5 to 5.5V
Total CW Efficiency	52	55		%	Vcc=3.0V Pout=+32.5 dBm
		45		%	Vcc=3.6V Pout=+32.5 dBm
Small-signal Gain		33		dB	
Harmonics	-30	-40		dBc	Vcc=3.0 to 5.5V Tamb= -25 to +85 °C
All Other Spurious			-70	dBc	Load VSWR≤6:1 all phase angles, Zs=50 Ω, Vcc=3.0V to 5.5V, Tamb= -30 to +85° C
Input VSWR		<2:1			
Input Power	+2	+4	+6	dBm	
Input Impedance		50		Ω	
Noise Power in Rx Band			-80dBm	dBm	Pout=+32.5 dBm, Freq.= 410 to 485 MHz, Tamb= -30 to +85°C VSWR ≤ 6:1 all phase angles.
Intermodulation Conversion at TX Freq. - 10MHz	12			dB	Pout=+15dBm to +32.5 dBm
Power Down Isolation	45			dB	VPD grounded through 1kΩ resistor Pin=+6dBm
Power Control					
Control Voltage VPD	0		2.4	V	
Control Current			6	mA	
Gain Control	35			dB	
Power Supply					
Power Supply Voltage	3.0	3.6	5.3	V	
Power Supply Current		1100		mA	DC Current at POUT,MAX
Regulated Voltage VREG	2.7	2.8	2.9	V	
Current from VREG			12	mA	

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Pin	Function	Description	Interface Schematic
1	VREG	Regulated Supply for bias circuit. This pin should be connected to the regulated supply with a ferrite of 240 ohms and should have a UHF decoupling capacitor (100pF) to ground at the supply end of the ferrite. An additional capacitor of 1nF can be added with the 100 pF but it's placement is not as critical.	
2	VCC1	Positive supply for the active bias circuits. Bypassing should be accomplished with a single UHF decoupling capacitor, placed close to the Pin. Additional bypassing of 1 nF is also recommended, but proximity to the package is not as critical.	
3	LTUNE	The Inter-stage matching point of the amplifiers. Matching should be performed with a small value inductor connected from the pin to ground.	
4	Q1C	Positive Supply to the first stage collector. The supply should be fed through a parallel LC network, resonant at the centre of the band of interest. A UHF decoupling capacitor should be placed from the supply end of the LC to ground. A 1nF capacitor can also be used but it's placement it not as critical.	
5	GND	Ground Contact for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own via to the groundplane, to minimize any common inductance.	
6	RF IN	Amplifier RF input. This is a 50Ω RF input port to the amplifier. It does not contain internal DC blocking and therefore should be externally DC blocked before connecting to any device which has DC present or which contains a DC path to ground. A series UHF capacitor is recommended for the DC blocking.	
7	NC	Not internally connected.	
8	VPD	Power Down control. When this pin is "low" all circuits are off. A low is typically less than 0.5V at room temperature. This pin affords a measure of power control, however this response is not linear across much of the range. It is recommended that the pin be used in closed loop power control systems if it is to be used across a range of voltages and temperatures for power control.	
9	NC	Not internally connected.	
10	NC	Not internally connected.	
11	NC	Not internally connected.	
12	RF OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 12, 13, and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through two of these three pins. Typically, these pins are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output. An additional network of a bias inductor (or λ/4 line) provides DC bias and helps to protect the output from high voltage swings due to severe load mismatches.	
13	RF OUT	Amplifier RF output, same as pin 12	
14	RF OUT	Amplifier RF output, same as pin 12. Do not feed the supply to this pin alone. If this pin is used as the supply pin it must be connected in parallel with pin 12 and/or 13.	
15	NC	Not internally connected.	
16	NC	Not internally connected.	
Pkg Base	GND	This contact is the main ground contact for the entire device. Care should be taken to ensure that this contact is well soldered in order to prevent performance from being degraded from that indicated in the specifications.	

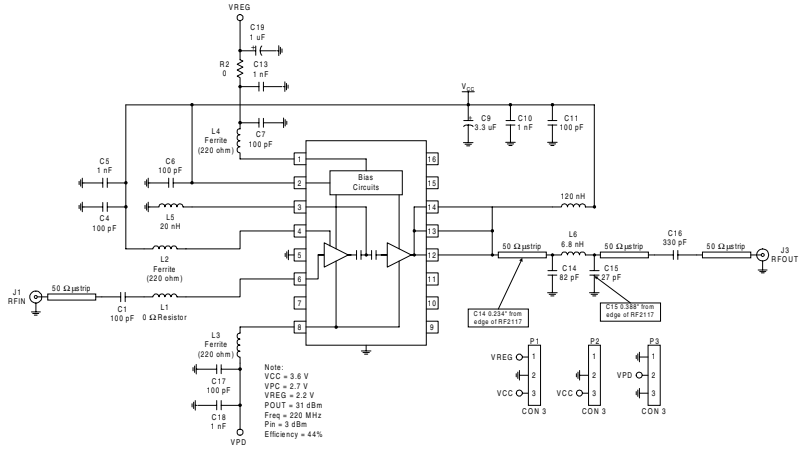
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Application Schematic
450MHz



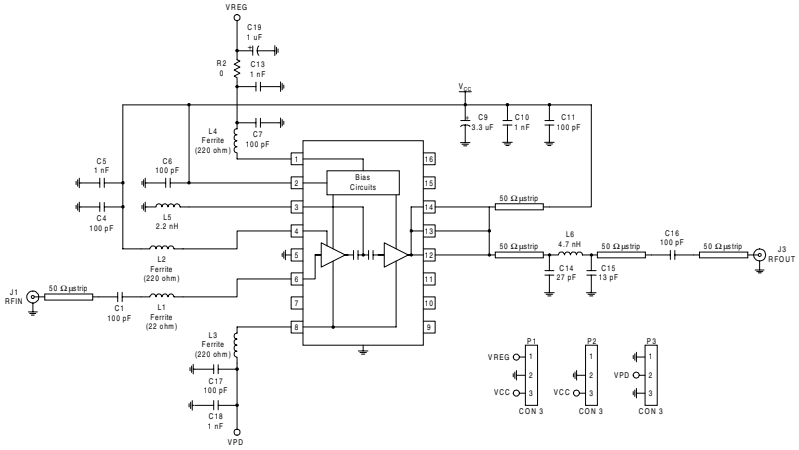
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Application Schematic
220MHz



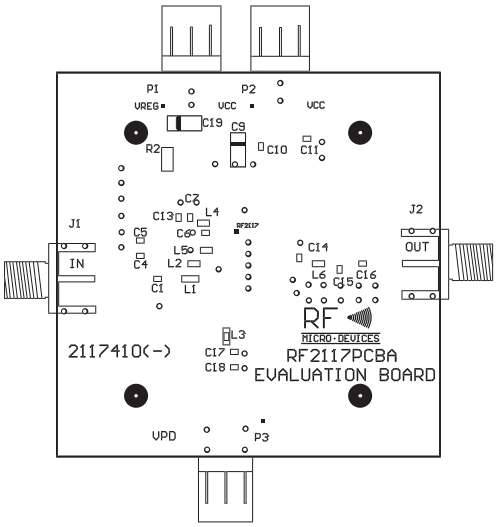
Evaluation Board Schematic

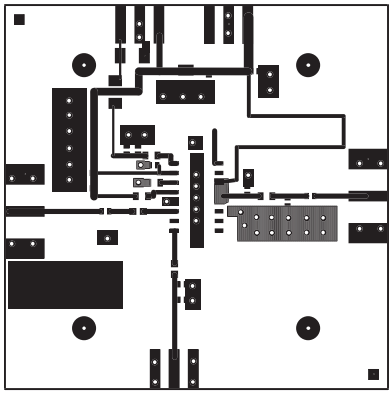
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
2” x 3”





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RF MICRO·DEVICES

Preliminary

RF2119

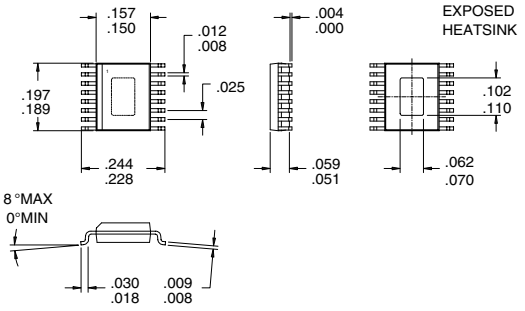
HIGH EFFICIENCY 2V POWER AMPLIFIER

Typical Applications

- Two-Way Pagers
- 915MHz ISM Band Equipment
- Spread Spectrum Systems
- 3V AMPS/ETACS Cellular Handsets
- CDPD Portable Data Cards
- Personal Digital Cellular

Product Description

The RF2119 is a high-power, high-efficiency amplifier IC targeting 2V to 4V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 960MHz band. The device is well suited for either CW or pulsed applications. At 3V, the RF2119 can deliver 29.5dBm of linear output power. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The package is a PSSOP-16 with backside ground.

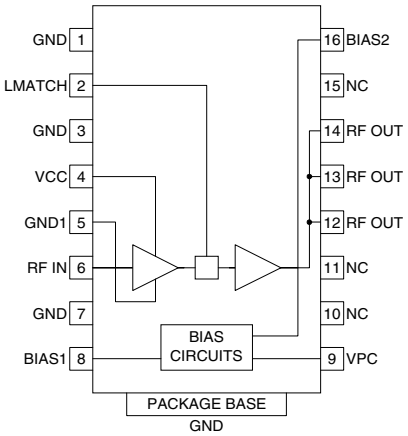


Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Package Style: PSSOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2V to 5V Supply
- 30dBm Output Power at 2.5V
- 30dB Small Signal Gain
- 53% Efficiency
- On-board Power Down Mode
- 800MHz to 960MHz Operation

Ordering Information

RF2119	High Efficiency 2V Power Amplifier
RF2119 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage	+5.2	V_{DC}
Control Voltage (V_{PC})	+3.0	V_{DC}
Input RF Power	+12	dBm
CW Dissipated Power	1.8	W
Peak Dissipated Power	2.5	W
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-30 to +150	°C

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

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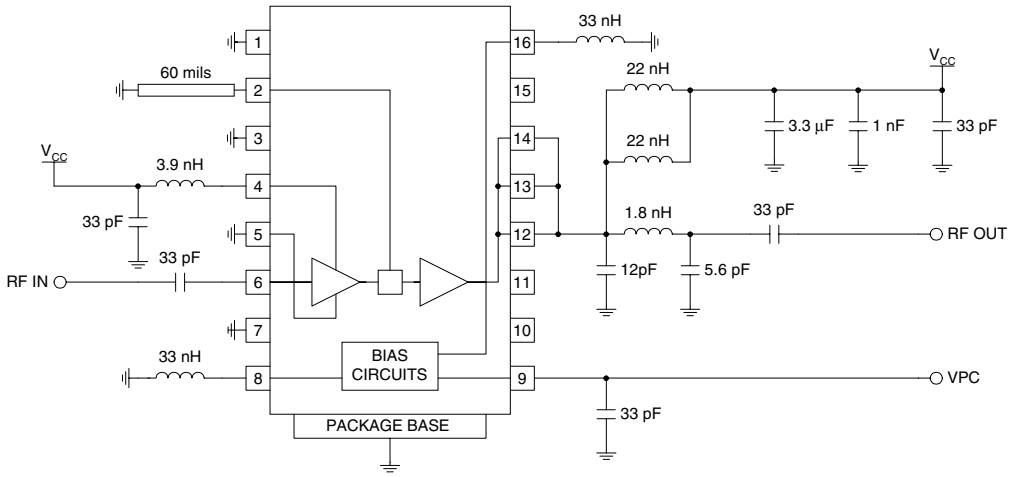
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.5V, V_{PC}=2.2V, Freq=902MHz, P_{IN}=2dBm
Usable Frequency Range	800	902	960	MHz	
Small Signal Gain		30		dB	
Maximum CW Output Power	29.5	30.5	31.5	dBm	Supply Voltage=2.5V
	31	32	34	dBm	Supply Voltage=3.0V
	32.5	33.5	35	dBm	Supply Voltage=3.5V
		29.3		dBm	Supply Voltage=2.0V
Maximum Pulsed Output Power	30	31	32		Supply Voltage=2.5V, 12.5% duty cycle
	31.5	33	34.5		Supply Voltage=3.0V, 12.5% duty cycle
	33	34	35.5		Supply Voltage=3.5V, 12.5% duty cycle
Total CW Efficiency	45	51		%	
Pulsed Efficiency	47	53		%	12.5% duty cycle
Input Power	0	+2	+6	dBm	
OFF Isolation		-25		dBm	V_{PC}=0V, Input Power=+6dBm
Second Harmonic Suppression		45		dBc	
Third Harmonic Suppression		>60		dBc	
Input VSWR			<2:1		With a 50Ω source impedance
Output Load VSWR	10:1				No damage.
AMPS Application					T=25°C, V_{CC}=3.5V, V_{PC}=1.6V, Freq=836MHz, P_{IN}=+8dBm (see AMPS application schematic)
Frequency		824 to 849		MHz	
Maximum Output Power	29.5	30.5		dBm	V_{CC}=2.7V
	30.8	31.5		dBm	V_{CC}=3.0V
	32	33		dBm	V_{CC}=3.5V
Efficiency @ Maximum Output Power	50	55		%	
Idle Current		120		mA	
I_{PC} @ Maximum Output Power		20		mA	
Power Down Control					
Turn On/Off Time			100	ns	
V_{PC} "OFF" Voltage	0.2	0.5		V	
V_{PC} "ON" Voltage	2.0	2.2	2.8	V	
I_{PC} "ON" Current		30		mA	V_{PC} =2.2V
I_{PC} "OFF" Current			10	µA	Standby, V_{PC} =0.5V
Power Supply					
Voltage		2.5		V	Specifications
Voltage	2.0		5.0	V	Operating Limits
Current Total	700	900	1200	mA	V_{CC}=2.5V, V_{PC}=2.2V, P_{IN}=+3dBm, T=25°C

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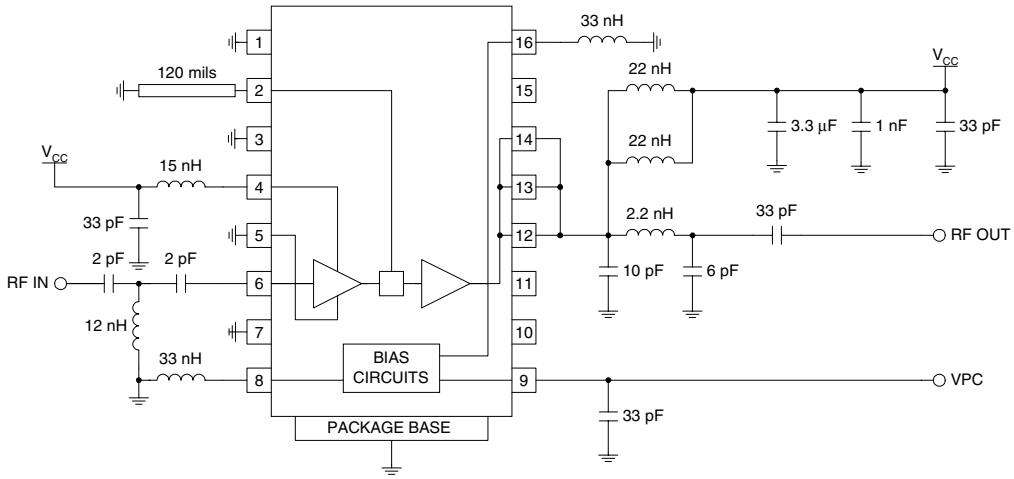
Pin	Function	Description	Interface Schematic
1	GND	Ground externally.	
2	LMATCH	Interstage tuning. This pin is internally DC blocked and will connect to a shunt inductor or microstrip line used for interstage tuning. Length from pin to via should be approximately 60mils for 915MHz and 75mils for 902MHz and 120mils for 836MHz. The lumped element equivalent is 1.2nH to 2.0nH to ground, depending on frequency band of interest.	
3	GND	Ground externally.	
4	VCC1	Power supply for stage 1. V_{CC} should be fed through a 3.9nH inductor with a decoupling capacitor on the V_{CC} side.	
5	GND1	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance.	
6	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
7	GND	Ground externally.	
8	BIAS1	Ground return for the first stage bias. This pin should be connected to a 33nH inductor to ground.	
9	VPC	Power control voltage. For maximum power, this voltage should be at least 2.2V. To turn off, this voltage should be less than 0.6V. This pin should be bypassed as close to the pin as practical.	
10	NC	No connection.	
11	NC	No connection.	
12	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
13	RF OUT	Same as pin 12.	
14	RF OUT	Same as pin 12.	
15	NC	No connection.	
16	BIAS2	Ground return for the second stage bias. This pin should be connected to a 33nH inductor to ground.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

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Application Schematic
902MHz to 928MHz (V_{CC}=2.5V)



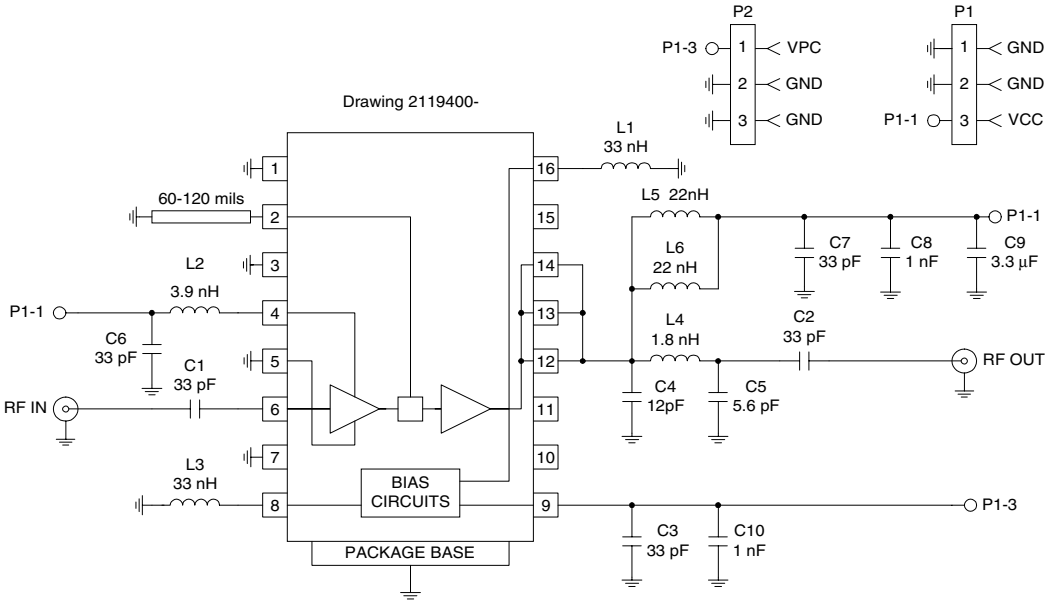
AMPS Application Schematic
824MHz to 849MHz (V_{CC}=3.5V)



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Evaluation Board Schematic 824MHz to 928MHz (V_{CC}=3.5V)

(Download Bill of Materials from www.rfmd.com.)

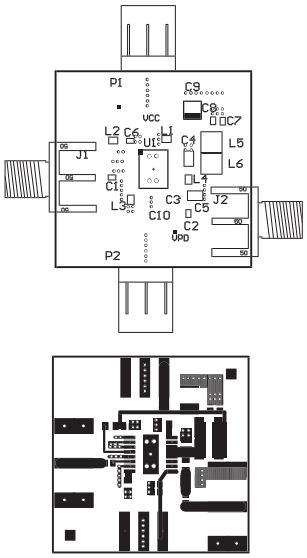


PCB mat'l: FR-4;
Two Layer: (31 mils; w/plating)

Off of Pin 2: 60 mil microstrip line for 902 MHZ to 928 MHz and 75 mil microstrip line for 890 MHZ to 915 MHz and 120 mil for 824 MHz to 849 MHz. Lumped element off of Pin 2 would be 1.2 nH to 2.0 nH to ground depending on frequency band of interest.

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Evaluation Board Layout
1.020” x 1.020”



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RF2125

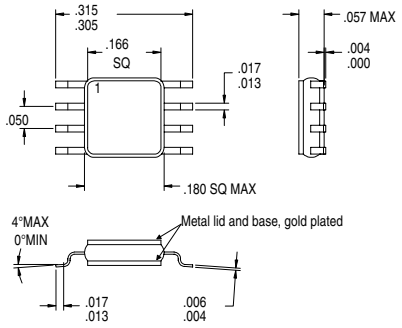
HIGH POWER LINEAR AMPLIFIER

Typical Applications

- PCS Communication Systems
- Digital Communication Systems
- DECT Cordless Applications
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

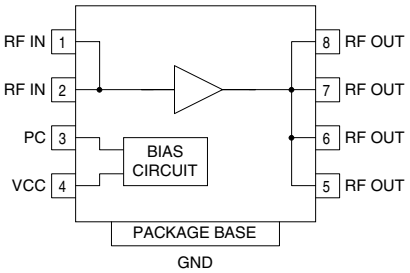
The RF2125 is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in digital PCS phone transmitters and base stations requiring linear amplification operating between 1500MHz and 2200MHz. It will also function as a high efficiency amplifier for constant envelope applications such as DECT. The device is packaged in an 8-lead ceramic package with a backside ground. The device is self-contained with the exception of the output matching network and power supply feed line. It produces a typical output power level of 1W.



Package Style: SOP-8-C

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2.7V to 7.5V Supply
- 1W Output Power
- 14dB Gain
- 45% Efficiency
- Power Down Mode
- 1500MHz to 2200MHz Operation

Ordering Information

RF2125	High Power Linear Amplifier
RF2125 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2125

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +3.6V	V
DC Supply Current	450	mA
Input RF Power	+20	dBm
Output Load	20:1	
Operating Case Temperature	-40 to +100	°C
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

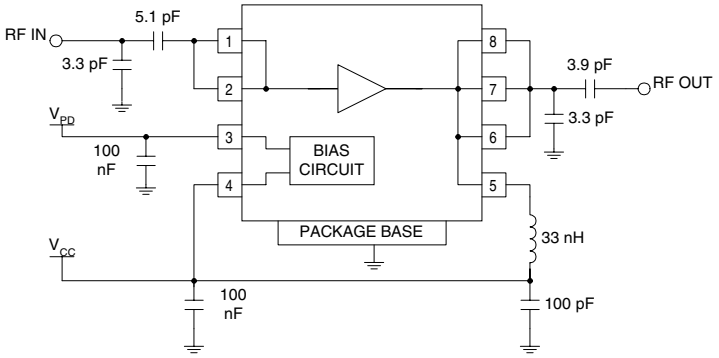
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=6.0V, V_{PC}=3.5V, Z_{LOAD}=12Ω, P_{IN} = 0dBm, Freq=1885MHz, Idle current=180mA
Frequency Range		1500 to 2200		MHz	
Maximum Output Power		+28.5		dBm	V_{CC}=3.6V, P_{IN}=+17dBm
Maximum Output Power		+29.5		dBm	V_{CC}=4.8V, P_{IN}=+17dBm
Maximum Output Power	+29.3	+30		dBm	V_{CC}=6.0V, P_{IN}=+17dBm
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=3.6V
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=4.8V
Total Power Added Efficiency	42	45		%	Maximum output, V_{CC}=6.0V
Small-signal Gain	12	14		dB	
Second Harmonic		-40		dBc	
Third Harmonic		-45		dBc	
Fourth Harmonic		-35		dBc	
Isolation		15		dB	V_{PC}=0.2V
Input VSWR		1.5:1			With external matching network; see application schematic
Two-tone Specification					
IM_3	-25	-30		dBc	P_{OUT}=+23.5dBm for each tone
IM_5		-35		dBc	P_{OUT}=+24dBm for each tone
IM_7		-45		dBc	P_{OUT}=+24dBm for each tone
Power Control					
V_{PC}	1.5	3.3	3.5	V	To obtain 180mA idle current
PC Current		1		mA	V_{PC}=2.0V
		2		mA	V_{PC}=3.5V
Power Control “OFF”	0.2	0.5		V	Threshold voltage at device input
Power Supply					
Power Supply voltage		2.7 to 7.5		V	
Supply Current	270	360	440	mA	P_{OUT}=+30dBm, V_{CC}=6.0V
Power Down Current		0.5	10	µA	V_{PC}=0.2V

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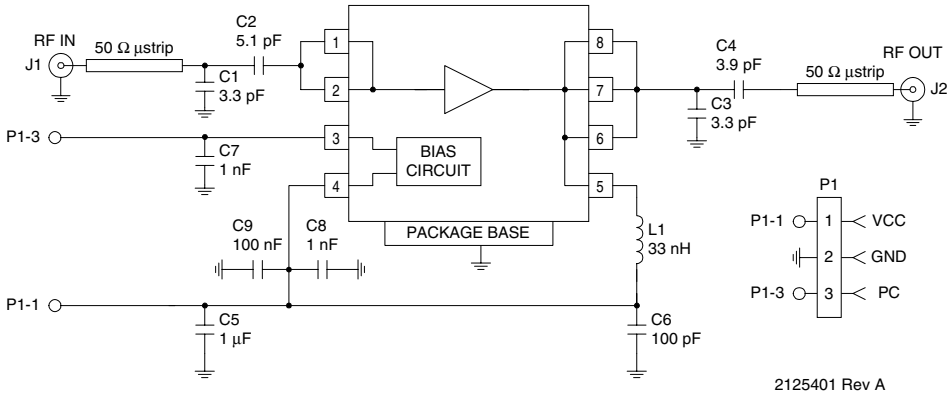
Pin	Function	Description	Interface Schematic
1	RF IN	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path. An optimum match to 50Ω is obtained by providing an external series capacitor of 4.3pF and then a shunt capacitor of 3.3pF; see the application schematic. Those values are typical for 1880MHz; other values may be required for other frequencies.	
2	RF IN	Same as pin 1.	
3	PC	Power control pin. For obtaining maximum performance the voltage on this pin can be used to set correct bias level. In a typical application this is implemented by a feedback loop. The feedback can be based on the actual supply current of the device, i.e., maintaining a fixed current level, or it can be based on the RF output power level to maintain a fixed RF power level (Automatic Level Control loop). A voltage of 0.5V or lower brings the part into power down state.	
4	VCC	Power supply pin for the bias circuits. External low frequency bypass capacitors should be connected if no other low frequency decoupling is nearby.	
5	RF OUT	RF output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through a quarter wave length microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC currents. Optimum load impedance is achieved by providing a shunt capacitor of 3.0pF and a series capacitor of 3.9pF; see the application schematic. Those values are typical for 1880MHz; other values may be required for other frequencies. Since there are several output pins available, which are internally connected, one pin can be used for connecting the bias, another for connecting a (third) harmonic trap filter, and the other pins for the RF output.	
6	RF OUT	Same as pin 5.	
7	RF OUT	Same as pin 5.	
8	RF OUT	Same as pin 5.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

Application Schematic 1880MHz



Evaluation Board Schematic
1880MHz

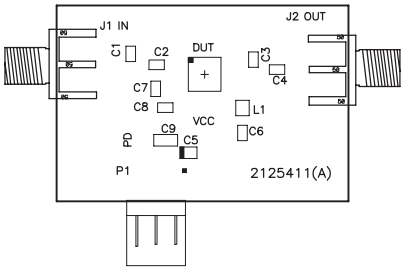
(Download Bill of Materials from www.rfmd.com.)

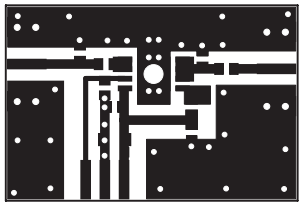


2125401 Rev A
PTI Package

Evaluation Board Layout
1.5” x 1.0”

Board Thickness 0.031”; Board Material FR-4

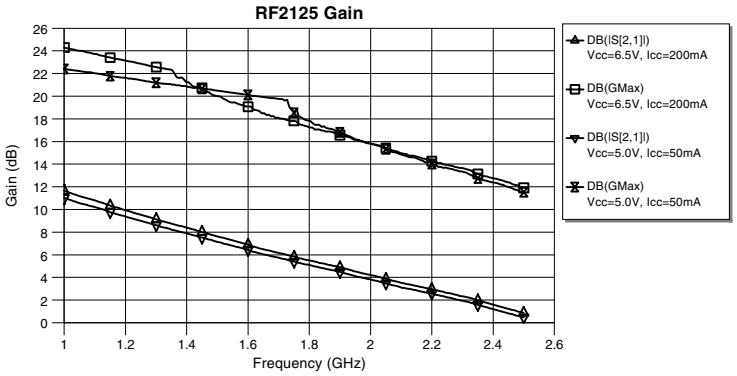




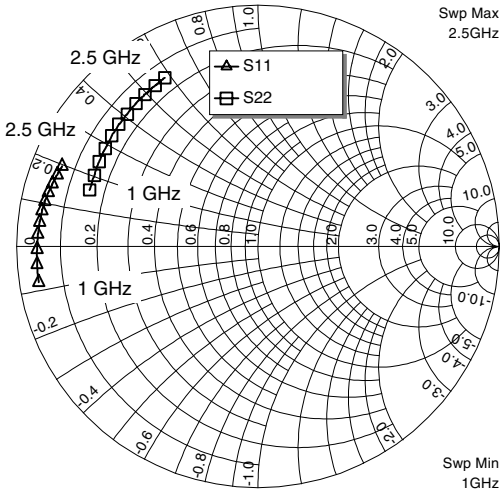
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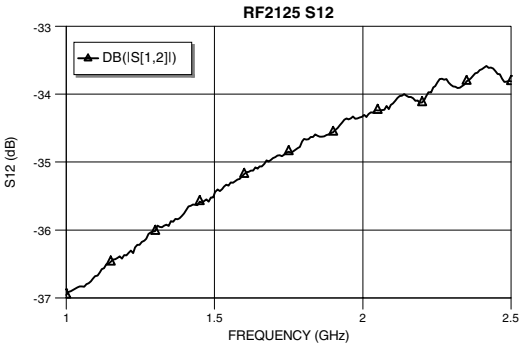
The data below is valid only under small-signal conditions. The device needs to be biased in Class A, with the output power below the 1-dB compression point. For large signal operation this data may be used as a starting point, but further tuning to optimize performance will be required.

Voltage and idle current have only very limited effect on the input and output impedances, hence only one plot is shown, valid for V_{CC}=5 to 7V, and I_{CC}=50 to 250mA.



RF2125 Input / Output Impedance, Class A bias





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MICRO·DEVICES

RF2125P

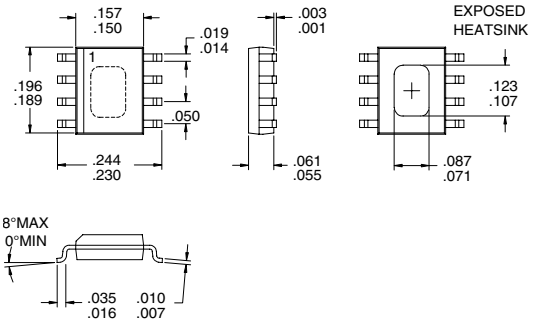
HIGH POWER LINEAR AMPLIFIER

Typical Applications

- PCS Communication Systems
- Digital Communication Systems
- DECT Cordless Applications
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

The RF2125P is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process and has been designed for use as the final RF amplifier in digital PCS phone transmitters and base stations requiring linear amplification operating between 1500MHz and 2200MHz. It will also function as a high efficiency amplifier for constant envelope applications such as DECT. The device is packaged in an 8-lead plastic package with a backside ground. The device is self-contained with the exception of the output matching network and power supply feed line. It produces a typical output power level of 1W.



Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

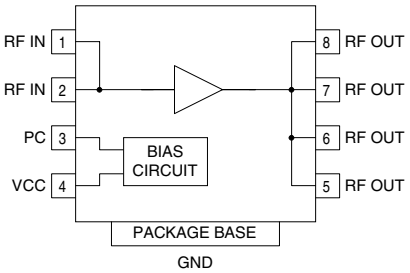
Package Style: PSOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- Single 2.7V to 7.5V Supply
- 1W Output Power
- 14dB Gain
- 45% Efficiency
- Power Down Mode
- 1500MHz to 2200MHz Operation



Functional Block Diagram

Ordering Information

RF2125P	High Power Linear Amplifier
RF2125P PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2125P

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +5	V
DC Supply Current	450	mA
Input RF Power	+20	dBm
Output Load VSWR	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +100	°C

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

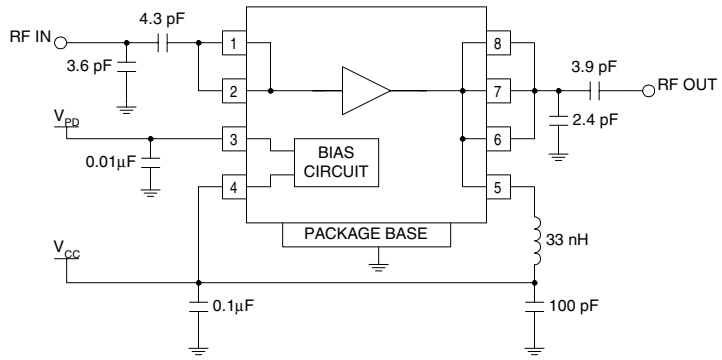
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=6.0V, V_{PC}=5.0V, Z_{LOAD}=12Ω, P_{in} = 0dBm, Freq=1885MHz, Idle current=180mA
Frequency Range		1500 to 2200		MHz	
Maximum Output Power		+28.5		dBm	V_{CC}=3.6V, P_{IN}=+17dBm
Maximum Output Power		+29.5		dBm	V_{CC}=4.8V, P_{IN}=+17dBm
Maximum Output Power	+29.0	+30		dBm	V_{CC}=6.0V, P_{IN}=+17dBm
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=3.6V
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=4.8V
Total Power Added Efficiency	40	45		%	Maximum output, V_{CC}=6.0V
Small-signal Gain	12	14		dB	
Second Harmonic		-40		dBc	
Third Harmonic		-45		dBc	
Fourth Harmonic		-35		dBc	
Isolation		15		dB	V_{PC}=0.2V
Input VSWR		1.5:1			With external matching network; see application schematic
Two-tone Specification					
Average Two-Tone Power		+27		dBm	PEP-3dB
IM_3	-23	-30		dBc	P_{OUT}=+24dBm for each tone
IM_5		-35		dBc	P_{OUT}=+24dBm for each tone
IM_7		-45		dBc	P_{OUT}=+24dBm for each tone
Power Control					
V_{PC}	1.5	3.3	3.5	V	To obtain 180mA idle current
PC Current		1		mA	V_{PC}=2.0V
		2		mA	V_{PC}=3.5V
Power Control "OFF"	0.2	0.5		V	Threshold voltage at device input
Power Supply					
Power Supply voltage		2.7 to 7.5		V	
Supply Current	200	360	500	mA	P_{OUT}=+30dBm, V_{CC}=6.0V
Power Down Current		0.5	10	µA	V_{PC}=0.2V

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path. An optimum match to 50Ω is obtained by providing an external series capacitor of 4.3pF and then a shunt capacitor of 3.3pF; see the application schematic. Those values are typical for 1880MHz; other values may be required for other frequencies.	
2	RF IN	Same as pin 1.	
3	PC	Power control pin. For obtaining maximum performance the voltage on this pin can be used to set correct bias level. In a typical application this is implemented by a feedback loop. The feedback can be based on the actual supply current of the device, i.e. maintaining a fixed current level, or it can be based on the RF output power level to maintain a fixed RF power level (Automatic Level Control loop). A voltage of 0.5V or lower brings the part into power down state.	
4	VCC	Power supply pin for the bias circuits. External low frequency bypass capacitors should be connected if no other low frequency decoupling is nearby.	
5	RF OUT	RF output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through a quarter wave length microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC currents. Optimum load impedance is achieved by providing a shunt capacitor of 3.0pF and a series capacitor of 3.9pF; see the application schematic. Those values are typical for 1880MHz; other values may be required for other frequencies. Since there are several output pins available, which are internally connected, one pin can be used for connecting the bias, another for connecting a (third) harmonic trap filter, and the other pins for the RF output.	
6	RF OUT	Same as pin 5.	
7	RF OUT	Same as pin 5.	
8	RF OUT	Same as pin 5.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

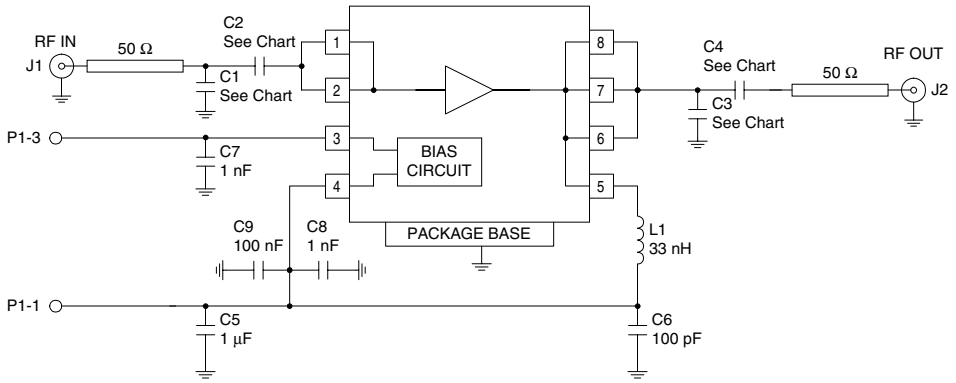
Application Schematic
1880MHz Operation

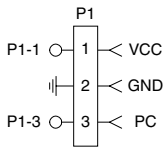


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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)





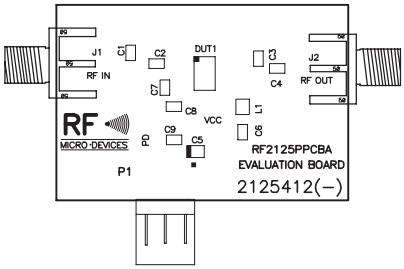
2125402 Rev -

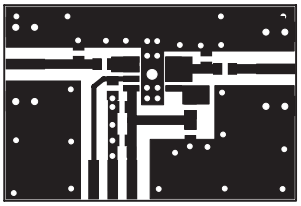
Capacitors are ATC type.
The 2.7 pF capacitor is 2.4 pF in parallel with 0.3 pF.

APPLICATION	C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)
DCS1800 (1710 to 1785 MHz)	3.3	7.5	3.6	3.9
DECT (1880 to 1990 MHz)	3.0	3.9	2.7	3.6
Broadband and Unlicensed PCS (1850 to 1910 MHz)	3.6	4.3	2.4	3.9
Broadband and Unlicensed PCS (1910 to 1970 MHz)	3.0	3.9	2.7	3.6

Evaluation Board Layout
1.0” x 1.5”

Board Thickness 0.031”; Board Material FR-4





RF2126

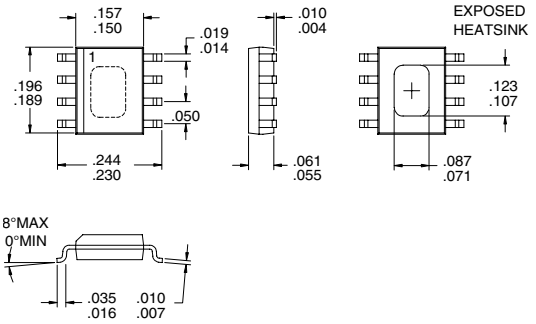
HIGH POWER LINEAR AMPLIFIER

Typical Applications

- 2.5GHz ISM Band Applications
- Digital Communication Systems
- PCS Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

The RF2126 is a high-power, high-efficiency, linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process and has been designed for use as the final RF amplifier in 2.45 GHz ISM applications such as WLAN and POS terminals. The part will also function as the final stage in digital PCS phone transmitters requiring linear amplification operating between 1800MHz and 2500MHz. The device is packaged in an 8-lead plastic package with a backside ground. The device is self-contained with the exception of the output matching network and power supply feed line. It produces a typical output power level of 1W.



Refer to “Handling of PSOP and PSSOP Products” on page 16-15 for special handling information.

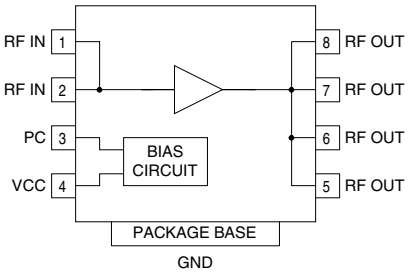
Package Style: PSOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- Single 3V to 6.5V Supply
- 1.3W Output Power
- 12dB Gain
- 45% Efficiency
- Power Down Mode
- 1800MHz to 2500MHz Operation



Functional Block Diagram

Ordering Information

RF2126	High Power Linear Amplifier
RF2126 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2126

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +5	V
DC Supply Current	450	mA
Input RF Power	+20	dBm
Output Load VSWR	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +100	°C

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

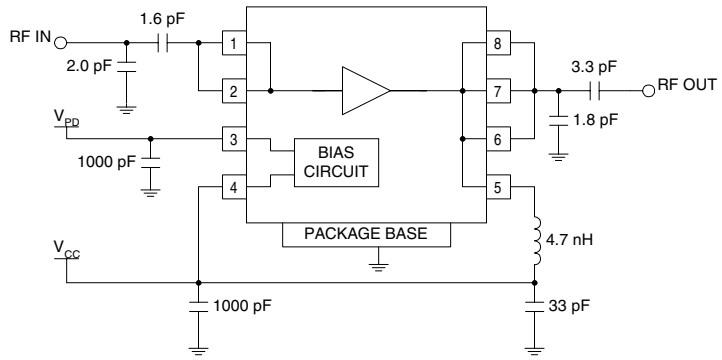
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=6.0V, V_{PC}=3.0V, Z_{LOAD}=12Ω, P_{in} = 0dBm, Freq=2450MHz, Idle current=180mA
Frequency Range	1800		2500	MHz	
Maximum Output Power		+27.0		dBm	V_{CC}=3.6V, P_{IN}=+19dBm
Maximum Output Power		+29		dBm	V_{CC}=4.8V, P_{IN}=+19dBm
Maximum Output Power	+30.0	+31.0		dBm	V_{CC}=6.0V, P_{IN}=+19dBm
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=3.6V
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=4.8V
Total Power Added Efficiency		45		%	Maximum output, V_{CC}=6.0V
Small-signal Gain		12		dB	
Second Harmonic		-55		dBc	See Application Schematic, P_{IN}=+17dBm
Third Harmonic		-60		dBc	
Input VSWR		1.5:1			With external matching network; see application schematic
Two-tone Specification					
Average Two-Tone Power		+27		dBm	PEP-3dB
IM_3	-24	-25		dBc	P_{OUT}=+24dBm for each tone
IM_5		-35		dBc	P_{OUT}=+24dBm for each tone
IM_7		-55		dBc	P_{OUT}=+24dBm for each tone
Power Control					
V_{PC}	1.5	3.0	3.5	V	To obtain 180mA idle current
Power Control "OFF"	0.2	0.5		V	Threshold voltage at device input
Power Supply					
Power Supply Voltage	3.0		6.5	V	
Supply Current	270	350	410	mA	P_{OUT}=+30dBm, V_{CC}=6.0V
Power Down Current		0.5	10	µA	V_{PC}=0.2V

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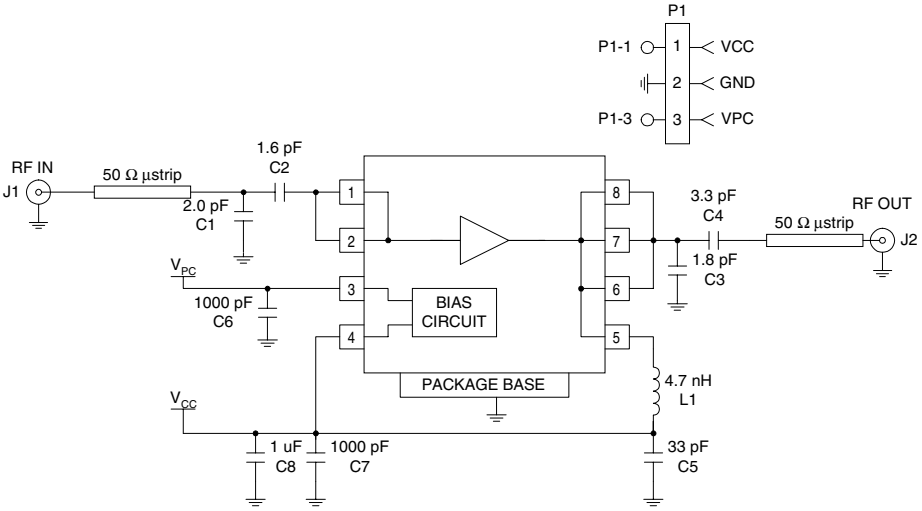
Pin	Function	Description	Interface Schematic
1	RF IN	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path. An optimum match to 50Ω is obtained by providing an external series capacitor of 1.6pF and then a shunt capacitor of 2.0pF; see the Application Schematic. Those values are typical for 2450MHz; other values may be required for other frequencies.	
2	RF IN	Same as pin 1.	
3	PC	Power control pin. For obtaining maximum performance the voltage on this pin can be used to set correct bias level. In a typical application this is implemented by a feedback loop. The feedback can be based on the actual supply current of the device, i.e. maintaining a fixed current level, or it can be based on the RF output power level to maintain a fixed RF power level (Automatic Level Control loop). A voltage of 0.5V or lower brings the part into power down state.	
4	VCC	Power supply pin for the bias circuits. External low frequency bypass capacitors should be connected if no other low frequency decoupling is nearby.	
5	RF OUT	RF output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through a quarter-wavelength microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC currents. Optimum load impedance is achieved by providing a shunt capacitor of 1.8pF and a series capacitor of 3.3pF; see the Application Schematic. Those values are typical for 2450MHz; other values may be required for other frequencies. Since there are several output pins available, which are internally connected, one pin can be used for connecting the bias, another for connecting a (third) harmonic trap filter, and the other pins for the RF output.	
6	RF OUT	Same as pin 5.	
7	RF OUT	Same as pin 5.	
8	RF OUT	Same as pin 5.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

Application Schematic
2450MHz Operation



Evaluation Board Schematic
2450 MHz Operation

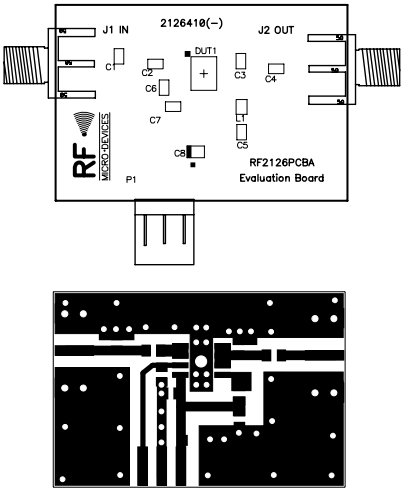
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
1.5" x 1.0"

Board Thickness 0.031", Board Material FR-4



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RF2127

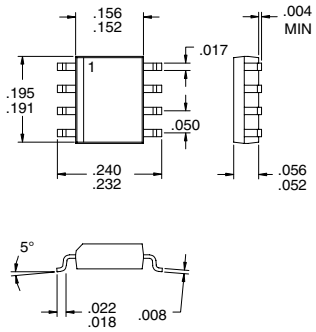
MEDIUM POWER LINEAR AMPLIFIER

Typical Applications

- DECT Cordless Applications
- PCS Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

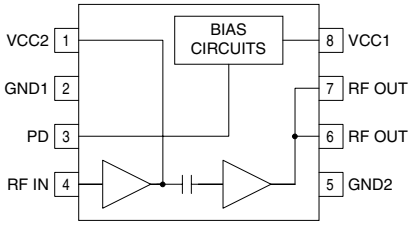
The RF2127 is a medium-power, high-efficiency, linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 1800MHz digital PCS phone transmitters requiring linear amplification operating between 1800MHz and 1900MHz, with over 100mW transmitted power. It will also function as the driver stage for the RF2125 high power amplifier. A simple power down function is included for TDD operation.



Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3.0V to 6.5V Supply
- 100mW Linear Output Power
- 25dB Small Signal Gain
- 30% Efficiency
- Digitally Controlled Power Down Mode
- 1500MHz to 1900MHz Operation

Ordering Information

RF2127	Medium Power Linear Amplifier
RF2127 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2127

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +7.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5.5	V
DC Supply Current	125	mA
Input RF Power	+12	dBm
Output Load VSWR	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

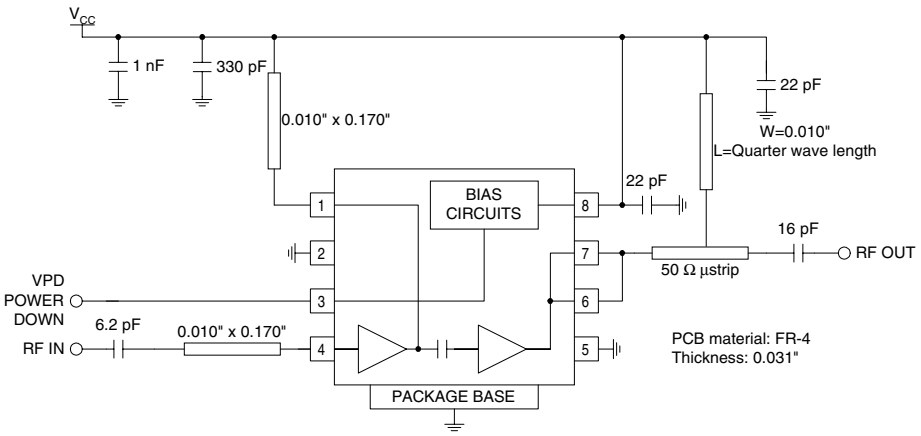
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, V_{PD}=5V, Z_{LOAD}=106Ω, P_{IN}=-3dBm, Freq=1800MHz
Frequency Range		1500 to 1900		MHz	
Maximum Output Power		+20		dBm	V_{CC}=5V, Pin=-3dBm
Maximum Output Power		+23		dBm	V_{CC}=6V, Pin=0dBm
Total CW Efficiency		30		%	Maximum output, V_{CC}=V_{PD}=5V
Small-signal Gain	23	25		dB	
Second Harmonic		-25		dBc	P_{OUT}=20dBm
Third Harmonic		-22		dBc	P_{OUT}=20dBm
Input VSWR		2:1			
Input Impedance		50		Ω	
Noise Figure		7		dB	
Two-Tone Specification					
Average Two-Tone Power		+17		dBm	PEP-3dB
IM_3		-40		dBc	P_{OUT}=+14dBM for each tone
IM_5		-45		dBc	P_{OUT}=+14dBM for each tone
IM_7		-44		dBc	P_{OUT}=+14dBM for each tone
Two-Tone Power-Added Efficiency		36		%	
Power Control					
Power Down "ON"		V_{CC}		V	Voltage supplied to the input; Part is "ON"
Power Down "OFF"	0		1.2	V	Voltage supplied to the input; Part is "OFF"
Power Supply					
Voltage		5		V	Specifications
		3.0 to 6.5		V	Operating Limits
Current		50	65	mA	Operating Idle
		80		mA	Maximum output
			10	µA	Power Down

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Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for the driver stage and interstage matching. Matching is typically done by a microstrip line to V_{CC} that is RF grounded at the V_{CC} side. See the application information for details.	
2	GND1	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance. This connection should be separated from the ground connection for the output stage, i.e., using separate traces and vias.	
3	PD	Power Down control. When this pin is "low", all circuits are shut off. A "low" is typically 1.2V or less at room temperature. When this pin is "high", all circuits are operating normally. A "high" is V_{CC}. If V_{PD} is below V_{CC}, output power and performance will be degraded. This could be used to obtain some gain control, but results are not guaranteed.	
4	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the matching provided on pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground.	
5	GND2	Ground connection for the output stage. Keep traces physically short and connect immediately to the ground plane for best performance. This connection should be separated from the ground connection for the driver stage, i.e., using separate traces and vias.	
6	RF OUT	RF Output and power supply for the output stage. Bias for the output stage needs to be provided on this pin. This can be done through a quarter-wave microstrip that is RF grounded on the other end. For matching to 50Ω, an external series microstrip line is required.	
7	RF OUT	Same as pin 6.	
8	VCC1	Power supply for the bias circuits. An external RF bypass capacitor of 22 pF is required. Keep the traces to the capacitor as short as possible, and connect the capacitor immediately to the ground plane.	

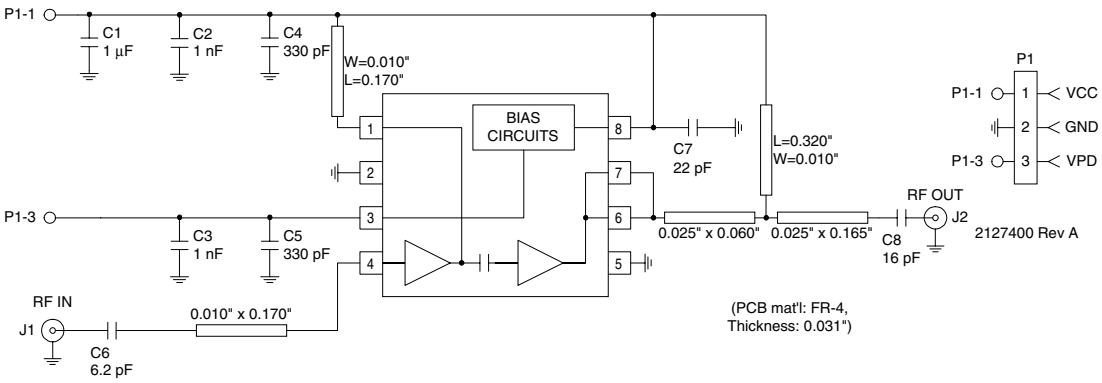
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Application Schematic
1850MHz



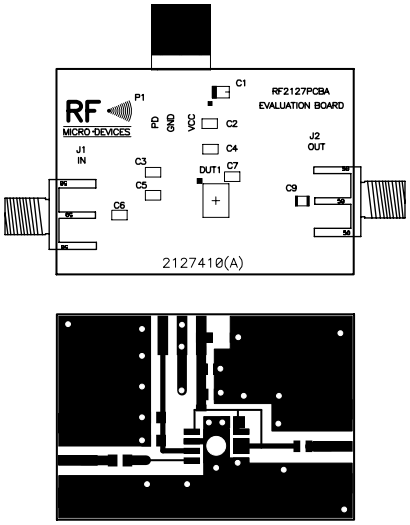
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
1.55” x 1.07”



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RF2128

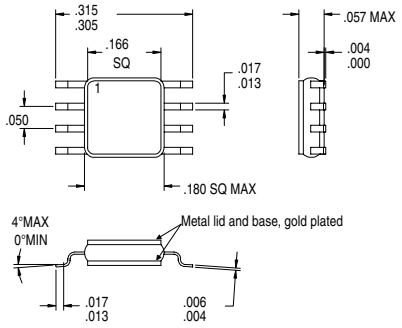
MEDIUM POWER LINEAR AMPLIFIER

Typical Applications

- PCS Communication Systems
- 2.5GHz ISM Band Applications
- Wireless LANs
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

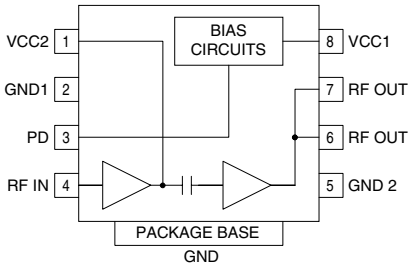
The RF2128 is a medium-power, high-efficiency, linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.45GHz ISM applications such as WLAN and POS terminals. The part also will function as the final stage in digital PCS phone transmitters requiring linear amplification operating between 1900MHz and 2200MHz, with over 100mW transmitted power, or as the driver stage for the RF2125 high power amplifier. A simple power down function is included for TDD operation.



Package Style: SOP-8-C

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3.0V to 6.5V Supply
- 100mW Linear Output Power
- 25dB Small Signal Gain
- 30% Efficiency
- Digitally Controlled Power Down Mode
- 1900MHz to 2500MHz Operation

Ordering Information

RF2128	Medium Power Linear Amplifier
RF2128 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	+7.5	V_{DC}
Power Down Voltage (V_{PD})	+5.5	V
DC Supply Current	125	mA
Input RF Power	+12	dBm
Output Load VSWR	20:1	
Operating Case Temperature	-40 to +100	°C
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

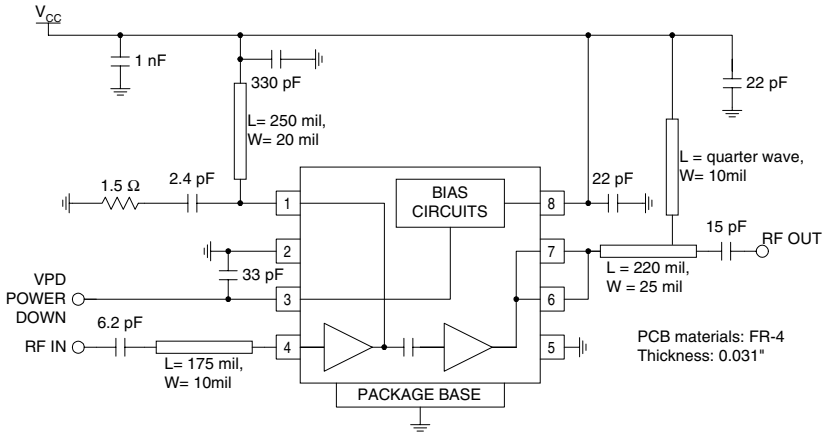
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, V_{PD}=5.0V, Freq=2400MHz
Frequency Range		1900 to 2500		MHz	
Maximum Output Power		>+20		dBm	V_{CC}=5.0V, V_{PD}=5.0V, P_{IN}=-3.0dBm
Maximum Output Power		>+23		dBm	V_{CC}=6.0V, V_{PD}=5.5V, P_{IN}=0dBm
Total CW Efficiency		30		%	Maximum output
Small-signal Gain		25		dB	
Second Harmonic		-25		dBc	
Third Harmonic		-22		dBc	
Isolation		15		dB	V_{PD}=0.2V
Input VSWR		2:1			
Input Impedance		50		Ω	
Noise Figure		7		dB	
Two-tone Specification					
Average Two-Tone Power		+17		dBm	PEP-3dB
IM_3		-24		dBc	P_{OUT}=+14dBm for each tone
IM_5		-36		dBc	P_{OUT}=+14dBm for each tone
IM7		-44		dBc	P_{OUT}=+14dBm for each tone
Two-Tone Power-Added Efficiency		36		%	
Power Down Control					
Power Down "ON"		V_{CC}		V	Voltage supplied to the input; device is "on"
Power Down "OFF"	0		1.2	V	Voltage supplied to the input; device is "off"
Power Supply					
Voltage		5		V	Specifications
		3.0 to 6.5		V	Operating
Current		50	65	mA	Operating Idle
		85		mA	At maximum output power
Current			10	μA	Power Down

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Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for the driver stage and interstage matching. External matching on this pin is required to optimize the gain. The matching on this port also greatly affects the input impedance. A decoupling capacitor of 330pF is required, together with a series RC for tuning for maximum gain at the desired frequency. See the application information for details.	
2	GND1	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	PD	Power Down control. When this pin is "low", all circuits are shut off. A "low" is typical 1.2V or less at room temperature. When this pin is "high", all circuits are operating normally. A "high" is V_{CC}. If PD is below V_{CC}, output power and performance will be degraded. This could be used to obtain some gain control, but results are not guaranteed.	
4	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the matching provided on pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground.	
5	GND2	Ground connection for the output stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
6	RF OUT	RF Output and power supply for the output stage. Bias for the output stage needs to be provided on this pin. This can be done through a quarter-wave microstrip that is RF grounded on the other end. For matching to 50Ω, an external series microstrip line is required.	
7	RF OUT	Same as pin 6.	
8	VCC1	Power supply for the bias circuits. An external RF bypass capacitor of 22pF is required. Keep the traces to the capacitor as short as possible, and connect the capacitor immediately to the ground plane.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

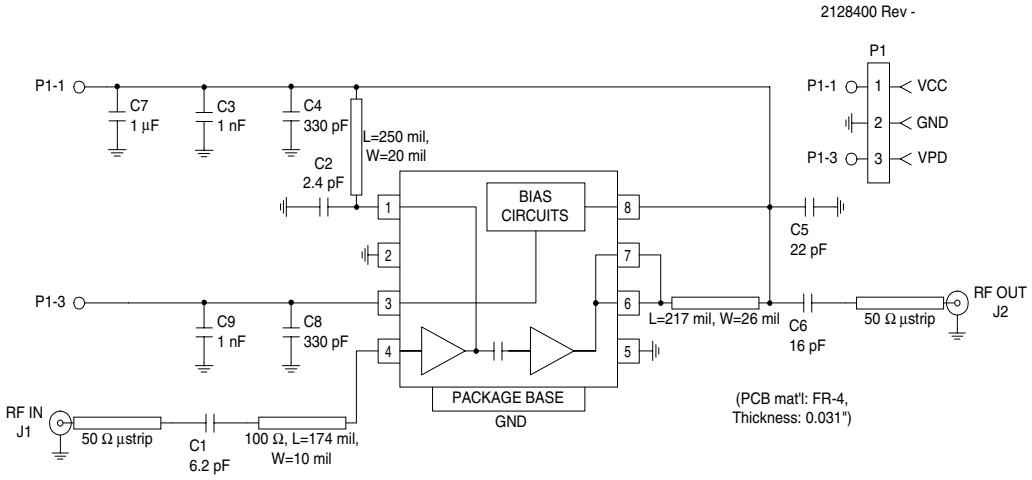
Application Schematic 2450MHz



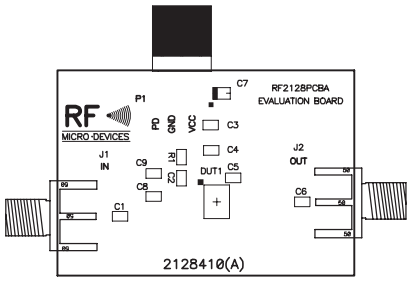
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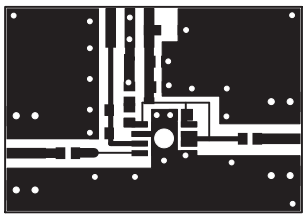
Evaluation Board Schematic
2450MHz Operation

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
1.547" x 1.068"





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RF2128P

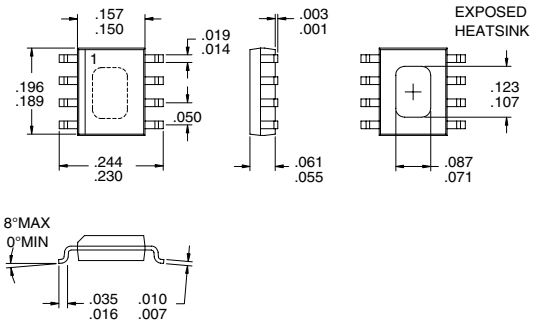
MEDIUM POWER LINEAR AMPLIFIER

Typical Applications

- PCS Communication Systems
- 2.5GHz ISM Band Applications
- Wireless LANs
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

The RF2128P is a medium-power, high-efficiency, linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.45GHz ISM applications such as WLAN and POS terminals. The part also will function as the final stage in digital PCS phone transmitters requiring linear amplification operating between 1900MHz and 2200MHz, with over 100mW transmitted power, or as the driver stage for the RF2125 high power amplifier. A simple power down function is included for TDD operation. The part is packaged in a low-cost plastic package with a metal backside.

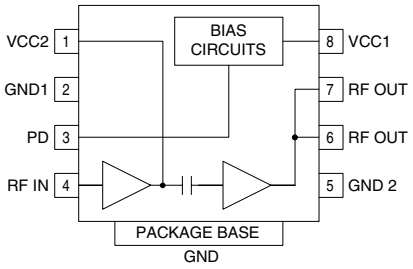


Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Package Style: PSOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3.0V to 6.5V Supply
- 100mW Linear Output Power
- 28dB Small Signal Gain
- 33% Efficiency
- Digitally Controlled Power Down Mode
- 1900MHz to 2500MHz Operation

Ordering Information

RF2128P	Medium Power Linear Amplifier
RF2128P PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2128P

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +7.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5.5	V
DC Supply Current	125	mA
Input RF Power	+12	dBm
Output Load	20:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

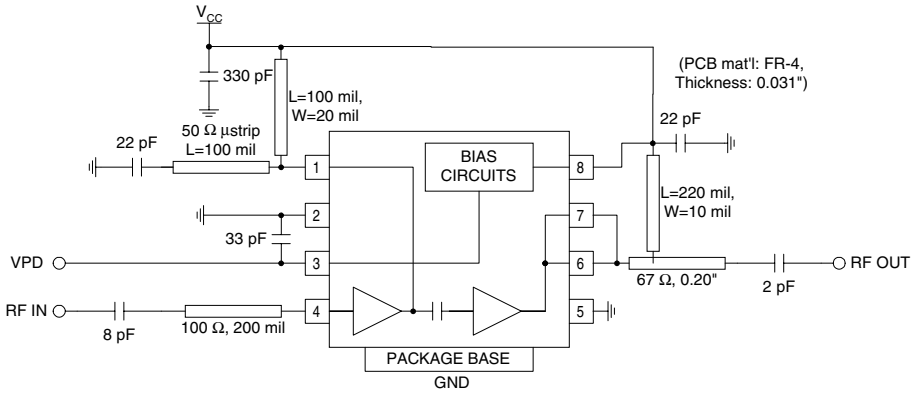
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, V_{PD}=5.0V, Freq=2400MHz
Frequency Range		1900 to 2500		MHz	
Maximum Output Power		+22		dBm	V_{CC}=5.0V, V_{PD}=5.0V, P_{IN}=-3.0dBm
		>+24		dBm	V_{CC}=6.0V, V_{PD}=5.5V, P_{IN}=0dBm
1dB Compression Output Power		+21		dBm	
Total CW Efficiency		33		%	Maximum output
Small-signal Gain		28		dB	
Second Harmonic		-23		dBc	
Third Harmonic		-19		dBc	
Isolation		15		dB	V_{PC}=0.2V
Input VSWR		2:1			
Input Impedance		50		Ω	
Noise Figure		7		dB	
Two-tone Specification					
Average Two-Tone Power		+17		dBm	PEP-3dB
IM_3		-27		dBc	P_{OUT}=+14dBm for each tone
IM_5		-40		dBc	P_{OUT}=+14dBm for each tone
IM7		-44		dBc	P_{OUT}=+14dBm for each tone
Two-Tone Power-Added Efficiency		30		%	
Power Down Control					
Power Down "ON"		V_{CC}		V	Voltage supplied to the input; device is "on"
Power Down "OFF"	0		1.2	V	Voltage supplied to the input; device is "off"
Power Supply					
Voltage		5		V	Specifications
		3.0 to 6.5		V	Operating
Current		50	65	mA	Operating Idle
		85		mA	At maximum output power
Current			10	µA	Power Down

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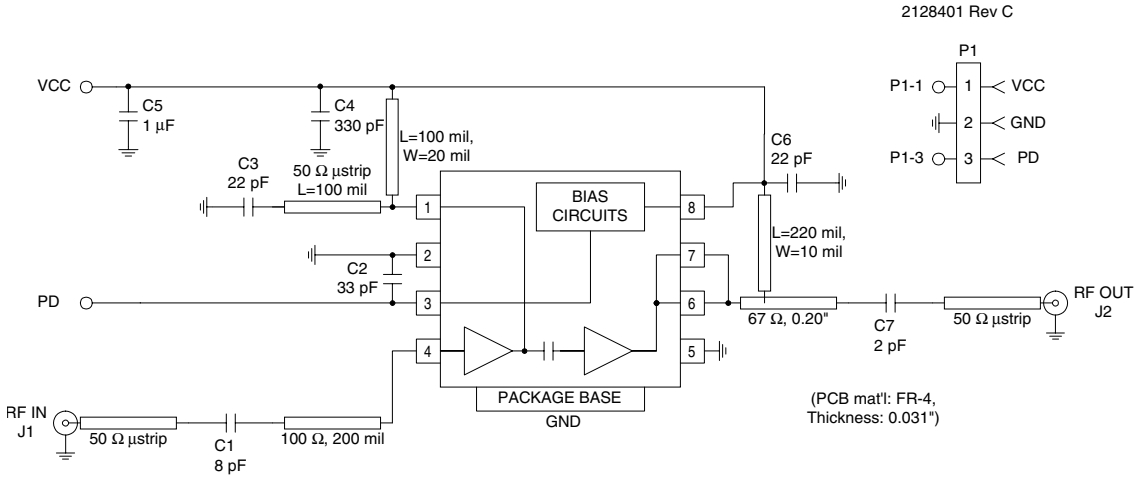
Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for the driver stage and interstage matching. External matching on this pin is required to optimize the gain. The matching on this port also greatly affects the input impedance. A decoupling capacitor of 330pF is required, together with a series RC for tuning for maximum gain at the desired frequency. See the application information for details.	
2	GND1	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	PD	Power Down control. When this pin is "low", all circuits are shut off. A "low" is typical 1.2V or less at room temperature. When this pin is "high", all circuits are operating normally. A "high" is V_{CC}. If PD is below V_{CC} output power and performance will be degraded. This could be used to obtain some gain control, but results are not guaranteed.	
4	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the matching provided on pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground.	
5	GND2	Ground connection for the output stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
6	RF OUT	RF Output and power supply for the output stage. Bias for the output stage needs to be provided on this pin. This can be done through a quarter-wave microstrip that is RF grounded on the other end. For matching to 50Ω, an external series microstrip line is required.	
7	RF OUT	Same as pin 6.	
8	VCC1	Power supply for the bias circuits. An external RF bypass capacitor of 22pF is required. Keep the traces to the capacitor as short as possible, and connect the capacitor immediately to the ground plane.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

Application Schematic 2450MHz Operation

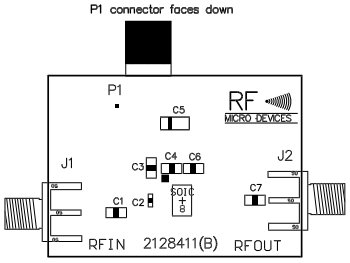


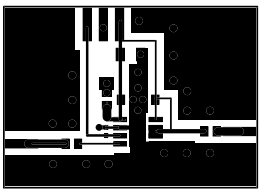
Evaluation Board Schematic
2450MHz Operation

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
1.572" X 1.121"





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RF2129

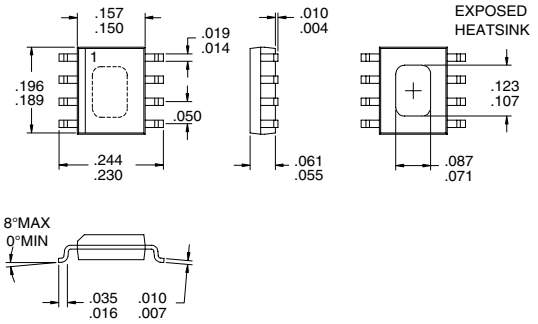
3V, 2.5GHZ LINEAR POWER AMPLIFIER

Typical Applications

- 2.5GHz ISM Band Applications
- PCS Communication Systems
- Wireless LAN Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- Broadband Spread Spectrum Systems

Product Description

The RF2129 is a linear, medium power, high efficiency amplifier IC designed specifically for low voltage operation. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz spread spectrum transmitters. The device is packaged in an 8-lead plastic package with a backside ground and is self-contained with the exception of the output matching network and power supply feed line.



Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

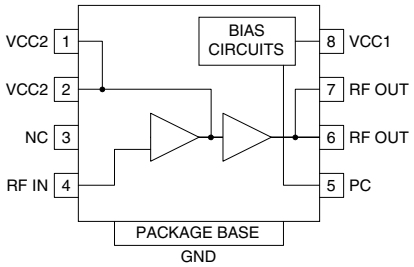
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: PSOP-8

Features

- Single 3.3V Power Supply
- +26dBm Saturated Output Power
- 27dB Small Signal Gain
- High Power Added Efficiency
- Power Down Mode
- 1800MHz to 2500MHz Frequency Range



Functional Block Diagram

Ordering Information

RF2129	3V, 2.5GHz Linear Power Amplifier
RF2129 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to 3.3	V
DC Supply Current	350	mA
Input RF Power	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture sensitivity	JEDEC Level 3	

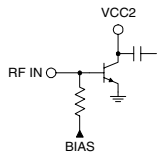
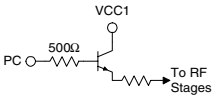
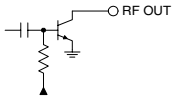
Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

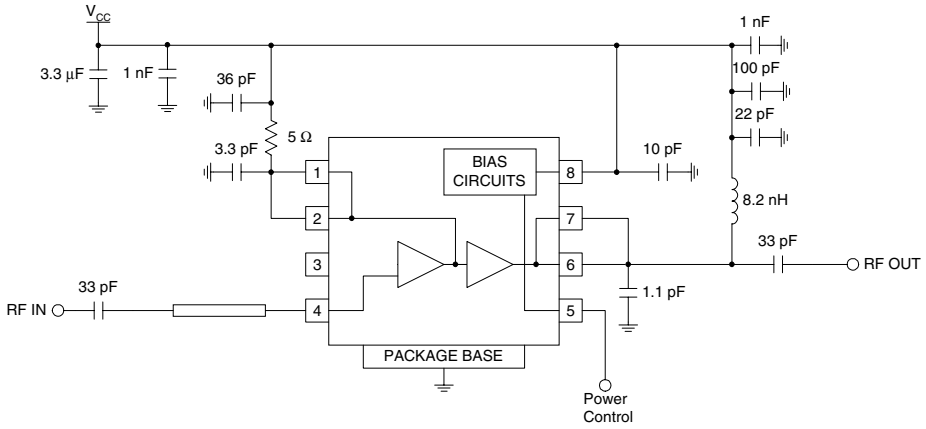
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.3V, V_{PC}=3.0V, P_{IN}=0dBm, Freq=2450MHz
Frequency Range		1800 to 2500		MHz	
Maximum Saturated Output Power	+24.5	+26	+27	dBm	P_{IN}=+6dBm
Efficiency at max output power		42		%	
Small Signal Gain	24.5	26.5		dB	
Reverse Isolation		30		dB	In "ON" state
		30		dB	In "OFF" state
Second Harmonic		-50		dBc	Including second harmonic trap, see application circuit
IM_3		-30	-23		P_{OUT}=+17dBm in each tone
IM_5		-35	-30		P_{OUT}=+17dBm in each tone
IM_7		-48	-35		P_{OUT}=+17dBm in each tone
Isolation	-20	-30		dBm	In "OFF" state, P_{IN}=0dBm
Input Impedance		50		Ω	
Input VSWR		2:1			
Noise Figure		7		dB	
Power Down					
Power Control "ON"	2.7		3.0	V	Voltage supplied to control input; device is "ON"
Power Control "OFF"		0	0.5	V	Voltage supplied to control input; device is "OFF"
PC Input Impedance	5			kΩ	
Power Supply					
Operating Voltage		3.0 to 5.0		V	
Current Consumption	180	260	320	mA	Power Down "ON", at max output power
	95	150	175	mA	Power Down "ON", two-tone test +20dBm average output power
	50	100	150	mA	Idle current
Current Consumption		<1	10	μA	Power Down "OFF"

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Pin	Function	Description	Interface Schematic
1	VCC2	Bias supply pin for the first stage. A small tuning capacitor is required to set the desired frequency response. External low frequency bypass capacitors should be connected as shown in the application schematic if no other low frequency decoupling is nearby.	
2	VCC2	Connected internally to pin 1.	See pin 1.
3	NC	Not internally connected.	
4	RF IN	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path.	See pin 1.
5	PC	Power control pin. For maximum power this pin should be 3.3V. A higher voltage is not recommended. For less output power and reduced idle current this voltage may be reduced.	
6	RF OUT	RF output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through a quarter-wave length microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC currents.	
7	RF OUT	Same as pin 6.	See pin 6.
8	VCC1	Power supply pin for the bias circuits. External low frequency bypass capacitors should be connected if no other low frequency decoupling is nearby.	See pin 5.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	See pin 1 and 6.

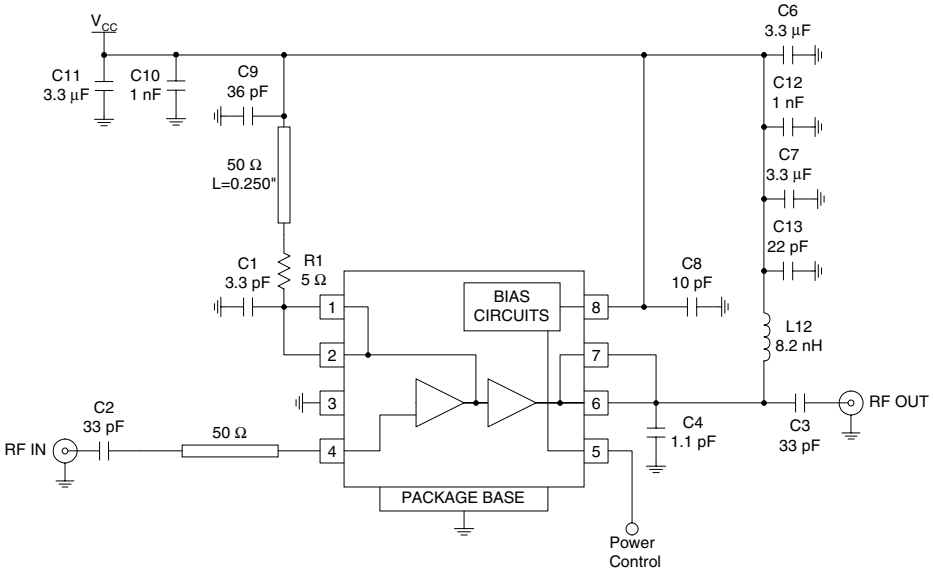
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Application Schematic
2.45GHz Operation



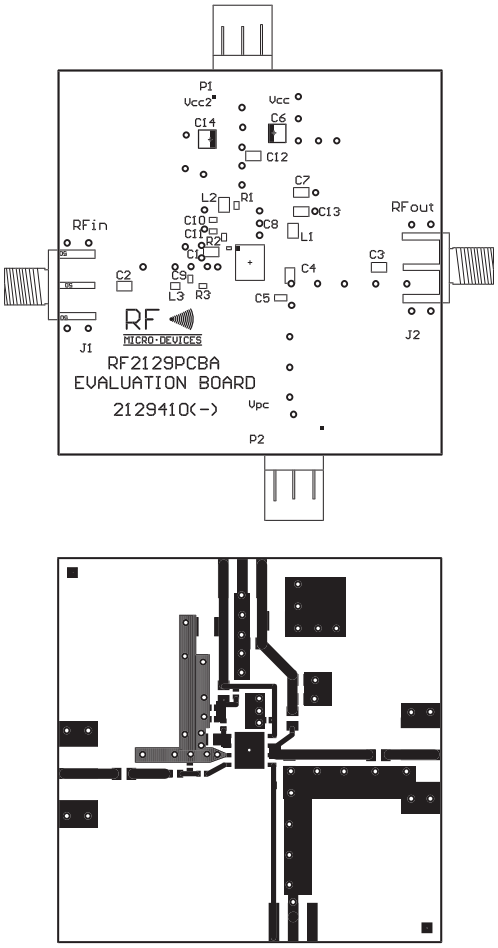
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
2” x 2”



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RF2131

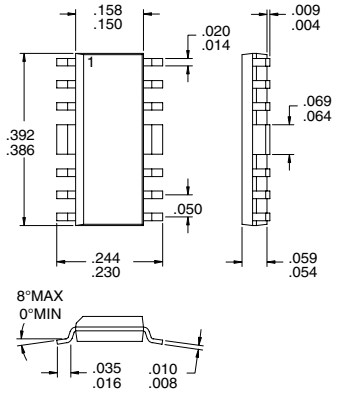
HIGH EFFICIENCY AMPS/ETACS AMPLIFIER

Typical Applications

- AMPS/ETACS Cellular Handsets
- CDPD Portable Data Cards
- 900MHz ISM Band Equipment
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

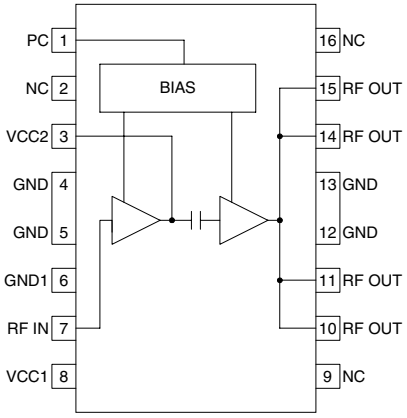
The RF2131 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in AMPS and ETACS hand held equipment, spread spectrum systems, CDPD, and other applications in the 800MHz to 950MHz band. On-board power control provides over 30dB of control range with an analog voltage input, and provides power down with a logic "low" for standby operation. Although it is intended for class C operation, linear class AB operation can be achieved by raising the bias level. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics.



Package Style: SOP-16 BW

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 4.0V to 7.0V Supply
- 1.2W Output Power
- 25dB Gain With Analog Gain Control
- 64% Efficiency
- Digitally Controlled Power Down Mode
- 800MHz to 950MHz Operation

Ordering Information

RF2131	High Efficiency AMPS/ETACS Amplifier
RF2131 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2131

Absolute Maximum Ratings

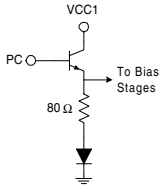
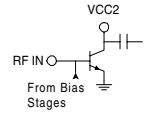
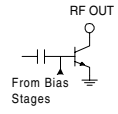
Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +4.5	V
DC Supply Current	570	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +100	°C
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.8V, V_{PC} set for P_{OUT}=+31dBm, Freq=836MHz
Operating Frequency Range		824 to 849		MHz	As configured in Application schematics
Usable Frequency Range		800 to 950		MHz	
Maximum CW Output Power	+30.5	+31		dBm	Depends on output matching
Total CW Efficiency	55	64		%	At Max Output
DC Current at 1.2W Output		400		mA	As configured in Application Circuit #1
Input Power for 1.2W output		+6	+8	dBm	
Noise Power Output		-90	-85	dBm/30kHz	In 869 - 894 MHz band (any gain or input power setting)
OFF Isolation	20	25		dB	V_{PC}=0V, Input Power=+6dBm
Second Harmonic		-30	-25	dBc	Depends upon external matching. Second harmonic levels directly from the IC are approximately 20 to 25dBc
Input VSWR			<2:1		
Input Impedance		50		Ω	
Power Down Control					
Turn On/Off Time			100	ns	
V_{PC} "OFF" Voltage	0.2	0.5		V	
V_{PC} "ON" Voltage		3.6	4.0	V	
Power Supply					
Voltage		4.8		V	Specifications
Voltage	4.0		7.0	V	Operating Limits

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Pin	Function	Description	Interface Schematic
1	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V or less at room temperature. During normal operation this pin is the power control. Control range varies from about 2V for 0dBm to 3.6V for +31dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details.	
2	NC	Not connected.	
3	VCC2	Power supply for the driver stage and interstage matching. A shunt capacitor is required for tuning the interstage to the proper frequency. The value of this capacitor depends on the operating frequency and power level. See the application information for details.	
4	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
5	GND	Same as pin 4.	
6	GND1	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is recommended to use separate vias to the ground plane for this return path.	See pin 1 schematic.
7	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 3. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 3 schematic.
8	VCC1	Power supply for the bias circuits. An external RF bypass capacitor is required. Keep the traces to the capacitor as short as possible, and connect the capacitor immediately to the ground plane.	See pin 1 schematic.
9	NC	This pin is not connected internally; however it needs to be connected to ground externally. This will improve performance by reducing coupling between pins.	
10	RF OUT	RF Output and power supply for the output stage. The four output pins are combined, and bias voltage for the final stage is provided through these pins. The external path must be kept symmetric until combined to ensure stability. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
11	RF OUT	Same as pin 10.	See pin 10 schematic.
12	GND	Ground connection for the output stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
13	GND	Ground connection for the output stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
14	RF OUT	Same as pin 10.	See pin 10 schematic.
15	RF OUT	Same as pin 10.	See pin 10 schematic.
16	NC	This pin is not connected internally, however it needs to be connected to ground externally. This will improve performance by reducing coupling between pins.	

Theory of Operation and Application Information

The RF2131 is a two-stage device with 25dB gain at full power. Therefore, for +31dBm output power, the drive required to fully saturate the output is +6dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 4.8V supply to operate to full specification. Bias control is provided through a single pin interface, and the final stage ground is achieved through the large pins on both sides of the package. First stage ground is brought out through a separate ground pin for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane. The output is brought out through the 4 output pins, and combined off-chip to form the RF output signal path.

The amplifier operates in Class AB bias mode. The final stage is "deep AB", meaning the quiescent current is very low, around 40mA. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 340mA. The optimum load for the output stage is approximately 10Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, leads, and microstrip, and a shunt capacitor external to the part. With this match, a 50Ω terminal impedance is achieved. The input is matched to 50Ω with just a blocking capacitor needed. This data sheet defines the configuration for AMPS operation, but the output load may be modified slightly for ETACS operation. In any case the optimum load for 1.2W is the same at the device, and only the reactive elements must change to perform the transformation from 50Ω down to 10Ω.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

V_{CC2} provides supply voltage to the first stage, as well as provides some frequency selectivity to tune to the operating band. Essentially, the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. For ETACS, the capacitor placement is slightly different than for AMPS due to the frequency shift. This supply should be bypassed individually with 33pF or 100pF capacitors before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RF OUT pins provide the output power. Pins 10 and 11 should be combined externally with pins 14 and 15 with a symmetric combiner, as shown in the PCB layout. Care should be taken to ensure that the output paths are symmetric up to the point of combining. This prevents "odd-mode" cancellation from occurring wherein one side may get out-of-phase with the other, affecting efficiency and stability. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 400mA of current required. Care should also be taken to keep the losses low in the bias feed and output components. DC losses in the bias choke will degrade efficiency and power.

The part will operate over a 4.0V to 4.8V range. If, for example, the full power is desired at minimum voltage, then the load can be optimized at that point. This is illustrated in Application Schematic 2. At that point, the specified efficiency and power should be attainable. As the voltage is increased, however, the output power will increase. Thus, in a system design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This will occur at a less-than-optimum efficiency, since the load is optimized for minimum voltage. If the load is set up to optimize power and efficiency at nominal operating voltage, then max efficiency should be attainable there. This case is illustrated in Application Schematic 1. As the voltage drops to minimum, power will degrade, but the efficiency tends to be maintained. For nominal 31.5dBm at 4.8V setup, as the voltage drops to 4.0V, the output power drops to 30.5dBm with a constant V_{PC}.

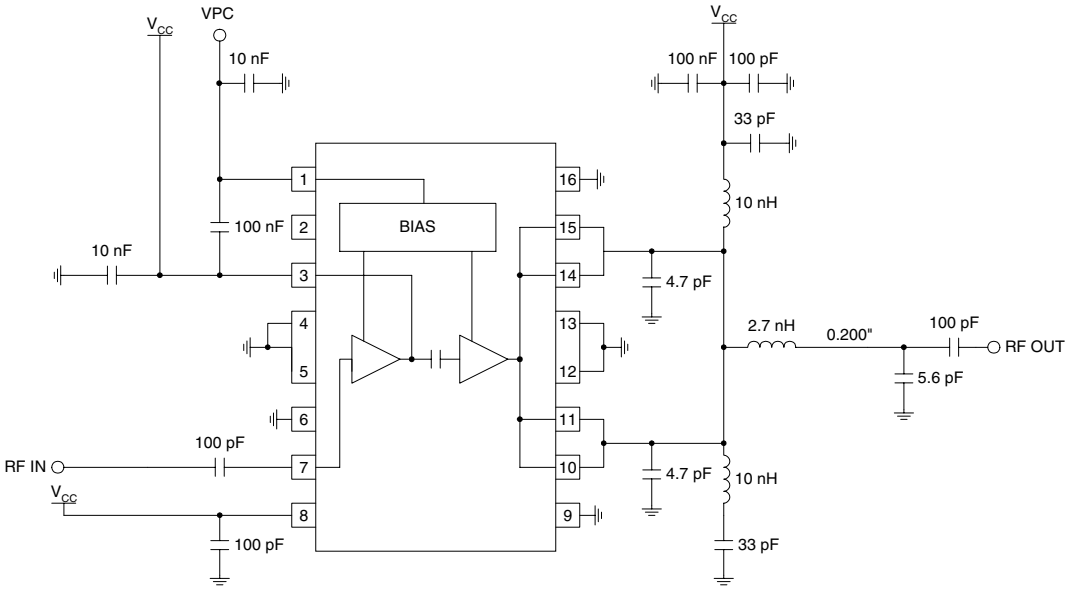
The HBT breakdown voltage is >20V, so nominally at 4.8V there should be no issue with overvoltage. Under extreme conditions, however, which can occur in a cellular handset environment, the supply voltage could be as high as 7.5V to 8.5V. These conditions may correspond to operation in a battery charger, especially with the battery removed, which "unloads" the supply circuit. To add to this worst-case scenario, the RF drive may be at full power during transmit, and the output VSWR could be extremely high, corresponding to a broken or removed antenna. Under all of the above conditions, the peak RF voltages could well exceed two times the supply voltage, forcing the device into breakdown. The RF2131 includes overvoltage protection diodes at the output, which begin clipping the waveform peaks at approximately 15V. This protects the device's output from breaking down under these worst-

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case conditions, and provides a rugged, robust component for the system designer.

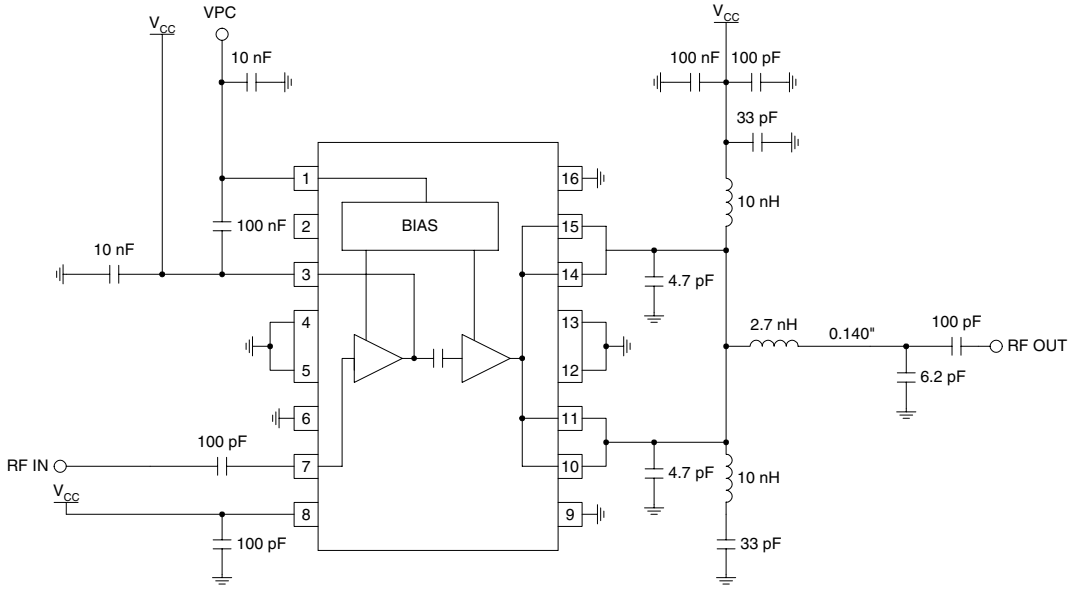
High current conditions are also potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2131 includes temperature compensation circuits in the bias network to stabilize the RF transistors, thus limiting the current through the amplifier and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations.

Application Schematic 1
Optimized for Efficiency at 4.8V



This schematic defines the optimum configuration for maximum efficiency at 4.8V. Under these conditions, as can be seen in the data plots, the power drops at 4.0V. Over 70% power-added efficiency can be achieved at +30.8dBm with 4.8V and +8dBm input level with this implementation.

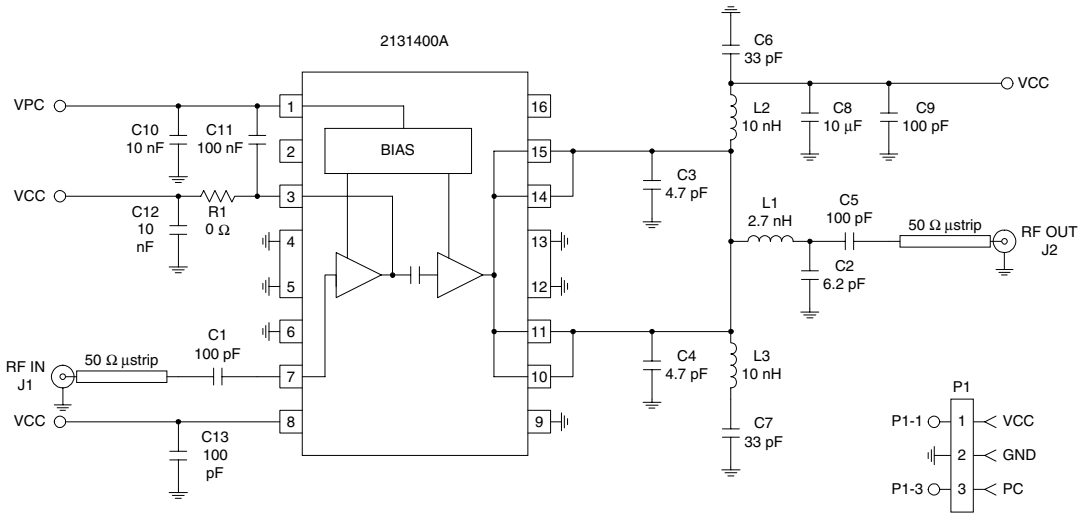
Application Schematic 2
Optimized for Power and Efficiency over 4.0V to 4.8V



This application circuit differs from Application schematic 1 only slightly in the output tuning. The output shunt capacitor has been moved 0.060" closer to the device, and has increased from 5.6pF to 6.2pF. This retuning allows over +30.8dBm of output power to be achieved down to 4.0V, however a couple of percent points of efficiency are sacrificed. This implementation is recommended for some additional margin on output power.

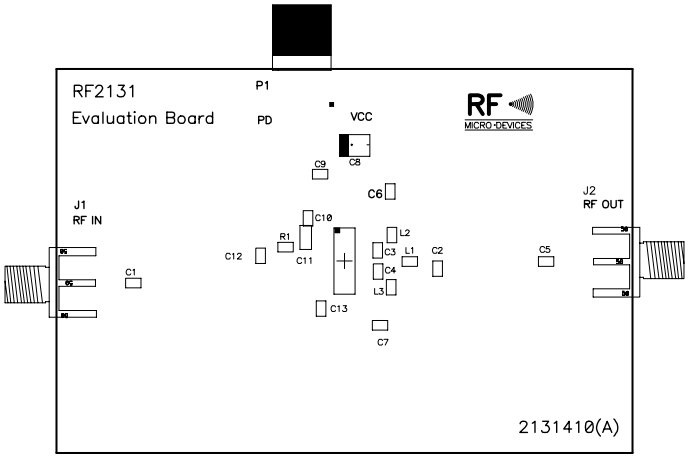
Evaluation Board Schematic

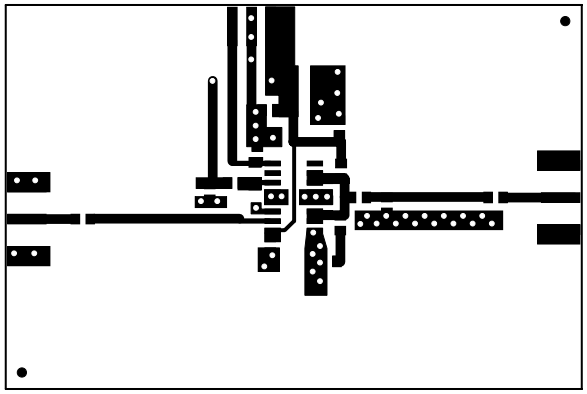
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
3” x 2”





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RF2132

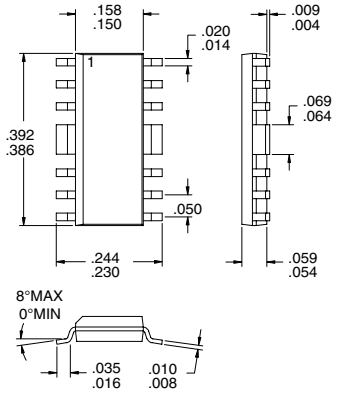
LINEAR POWER AMPLIFIER

Typical Applications

- 4.8V AMPS Cellular Handsets
- 4.8V CDMA/AMPS Handsets
- 4.8V JCDMA/TACS Handsets
- Driver Amplifier in Cellular Base Stations
- Portable Battery Powered Equipment

Product Description

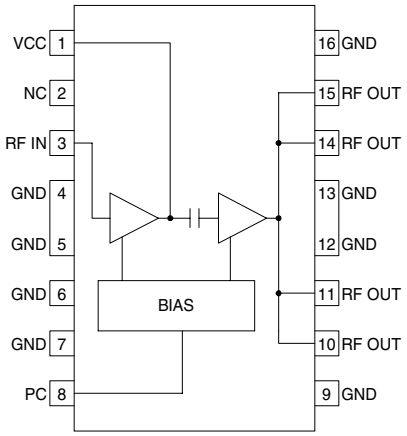
The RF2132 is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 4-cell CDMA/AMPS hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 950MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics over varying supply and control voltages.



Package Style: SOP-16 BW

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 4.2V to 6.0V Supply
- Up to 29 dBm Linear Output Power
- 29dB Gain With Analog Gain Control
- 45% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 950MHz Operation

Ordering Information

RF2132	Linear Power Amplifier
RF2132 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2132

Absolute Maximum Ratings

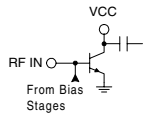
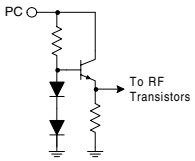
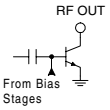
Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V_{DC}
Supply Voltage (P_{OUT}<32dBm)	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +6.0 or V_{CC}	V
DC Supply Current	800	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Storage Temperature	-40 to +150	°C
Junction Temperature	200	°C

Caution! ESD sensitive device.

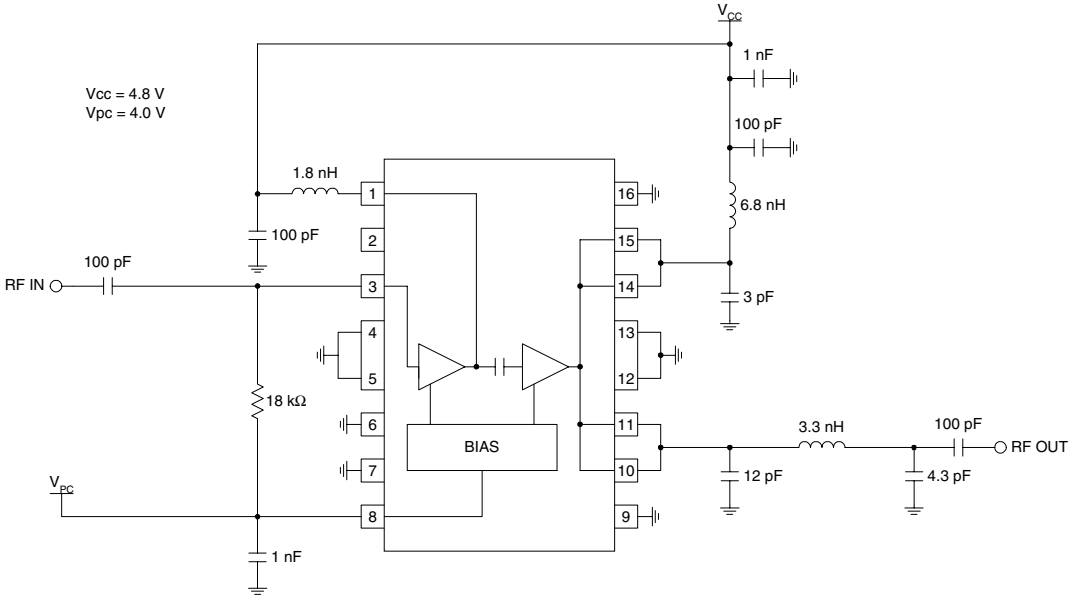
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.8V, V_{PC}=4.0V, Freq=824MHz to 849MHz
Usable Frequency Range	800	824 to 849	950	MHz	
Linear Gain	27	29	31	dB	
Total Linear Efficiency	40	45		%	
Efficiency at Max Output	50	55		%	
OFF Isolation	23	27		dB	V_{PC}=0V,P_{IN}=+6dBm
Second Harmonic		-30		dBc	Including Second Harmonic Trap
Maximum Linear Output Power		28.5	29		IS-95A CDMA Modulation
Adjacent Channel Power Rejection @ 885 kHz		-46	-44	dBc	Pout = 28 dBm ACPR can be improved by trading off efficiency.
Adjacent Channel Power Rejection @ 1.98 MHz		-58	-56	dBc	Pout = 28 dBm
Maximum CW Output Power	31.5	32		dBm	
Operating Case Temperature	-30		110	°C	Pout = 31 dBm, Efficiency = 55%
Ambient Operating Temperature	-30		100	°C	
Junction to Case Thermal Resistance		85		°C/W	
Input VSWR		<2:1			
Output Load VSWR			10:1		No oscillations
Power Down					
Turn On/Off Time			100	ns	
Total Current			10	µA	"OFF" State
V_{PC} "OFF" Voltage	0.2		0.5	V	
V_{PC} "ON" Voltage	3.6	4.0	Vcc	V	
Power Supply					
Power Supply Voltage	4.2	4.8	6.0	V	Operating voltage
Idle Current		40	100	mA	V_{PC}=4.0V
Current into VPC pin		15	20	mA	"ON" State

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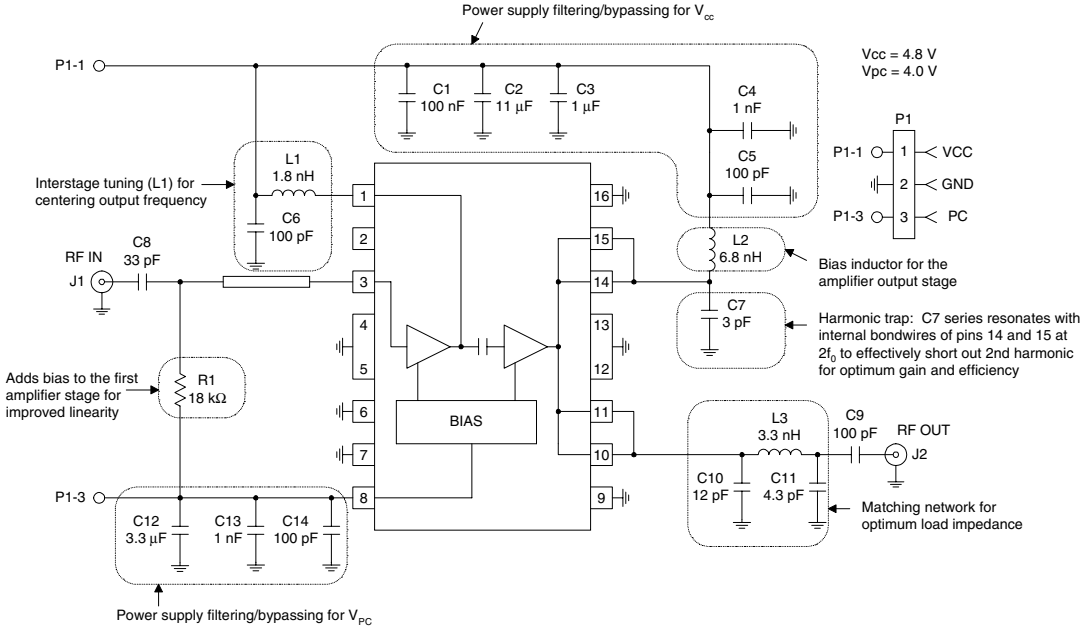
Pin	Function	Description	Interface Schematic
1	VCC1	Power supply for the driver stage, and interstage matching. Shunt inductance is required on this pin, which can be achieved by an inductor to V_{CC}, with a decoupling capacitor on the V_{CC} side. The value of the inductor is frequency dependent; 3.3nH is required for 830MHz, and 1.2nH for 950MHz. Instead of an inductor, a high impedance microstrip line can be used.	
2	NC	Not Connected.	
3	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
4	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
5	GND	Same as pin 4.	
6	GND	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the batwing and other ground contacts. See evaluation board layout.	
7	GND	Same as pin 6.	
8	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V or less at room temperature. During normal operation this pin is the power control. Control range varies from about 2V for 0dBm to V_{CC} for +31dBm RF output power. The maximum power that can be achieved depends on the actual output matching. PC should never exceed 6.0V or V_{CC}, whichever is the lowest.	
9	GND	Same as pin 4.	
10	RF OUT	RF Output and power supply for the output stage. The four output pins are combined, and bias voltage for the final stage is provided through these pins. The external path must be kept symmetric until combined to ensure stability. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
11	RF OUT	Same as pin 10.	See pin 10.
12	GND	Same as pin 4.	
13	GND	Same as pin 4.	
14	RF OUT	Same as pin 10.	See pin 10.
15	RF OUT	Same as pin 10.	See pin 10.
16	GND	Same as pin 4.	

Application Schematic



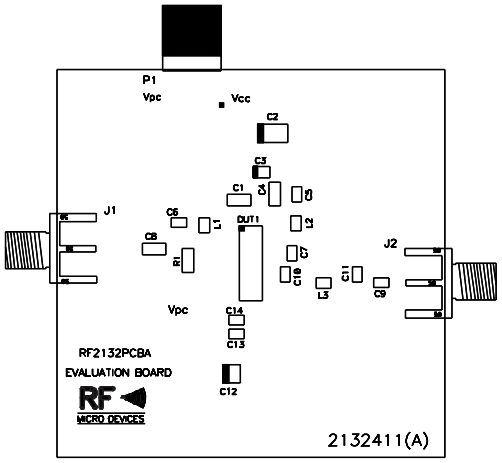
Evaluation Board Schematic

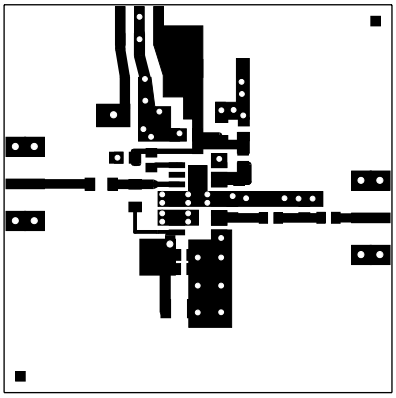
(Download Bill of Materials from www.rfmd.com.)

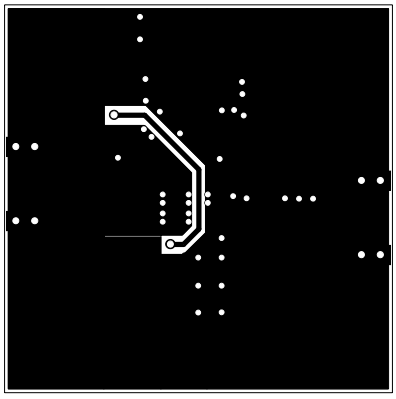


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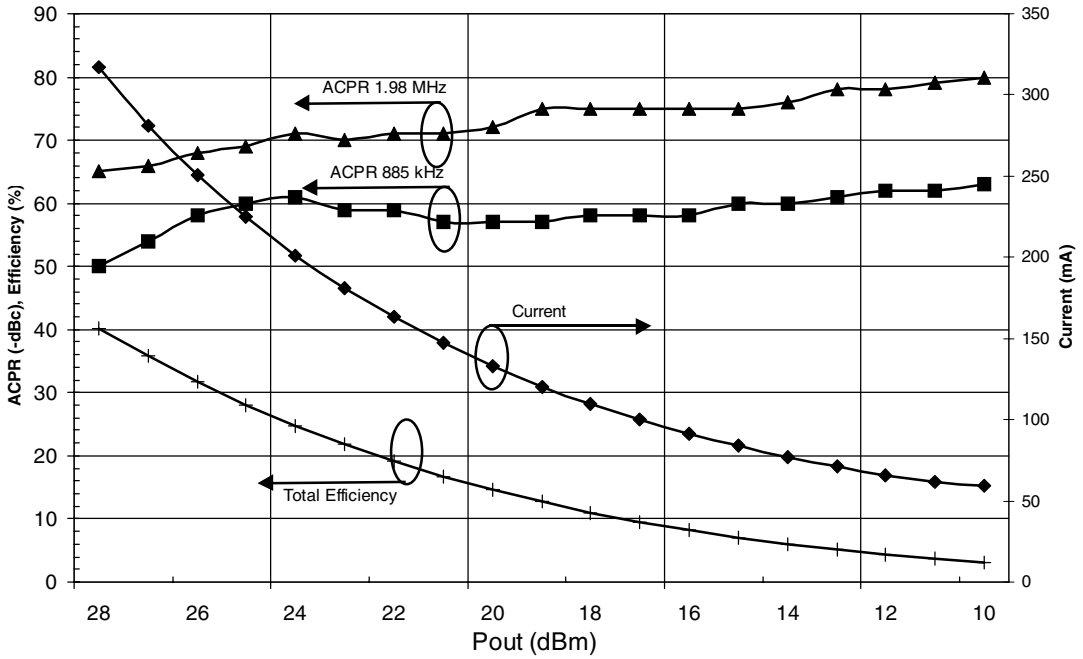
Evaluation Board Layout
2” x 2”







RF2132 Evaluation Board
Vcc = 4.8 V, Vpc = 4.0 V, Frequency = 836 MHz, IS-95A CDMA



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RF2137

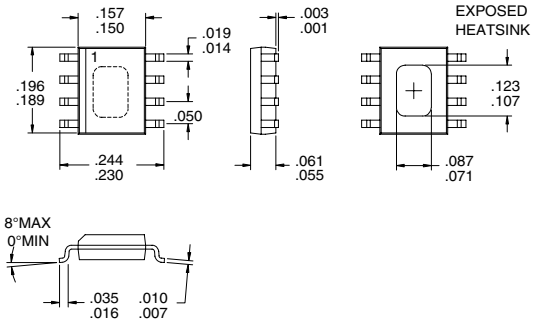
LINEAR POWER AMPLIFIER

Typical Applications

- 4.8V AMPS Cellular Handsets
- 4.8V CDMA/AMPS Handsets
- 4.8V JCDMA/TACS Handsets
- Driver Amplifier in Cellular Base Stations
- Portable Battery Powered Equipment

Product Description

The RF2137 is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 4-cell CDMA/AMPS hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 950MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics at all recommended supply voltages.



Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

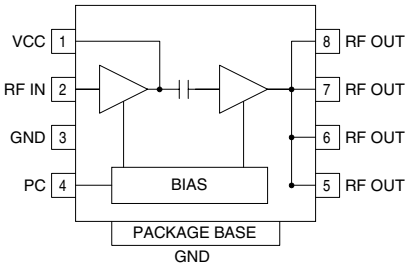
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: PSOP-8

Features

- Single 4.2V to 6.0V Supply
- Up to 29 dBm Linear Output Power
- 27dB Gain With Analog Gain Control
- 45% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 950MHz Operation



Functional Block Diagram

Ordering Information

RF2137	Linear Power Amplifier
RF2137 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2137

Absolute Maximum Ratings

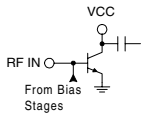
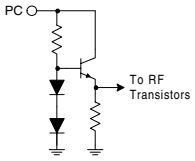
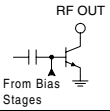
Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V_{DC}
Supply Voltage (P_{OUT}<31dBm)	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +6.0 or V_{CC}	V
DC Supply Current	800	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Ambient Operating Temperature	-30 to +90	°C
Storage Temperature	-40 to +150	°C

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

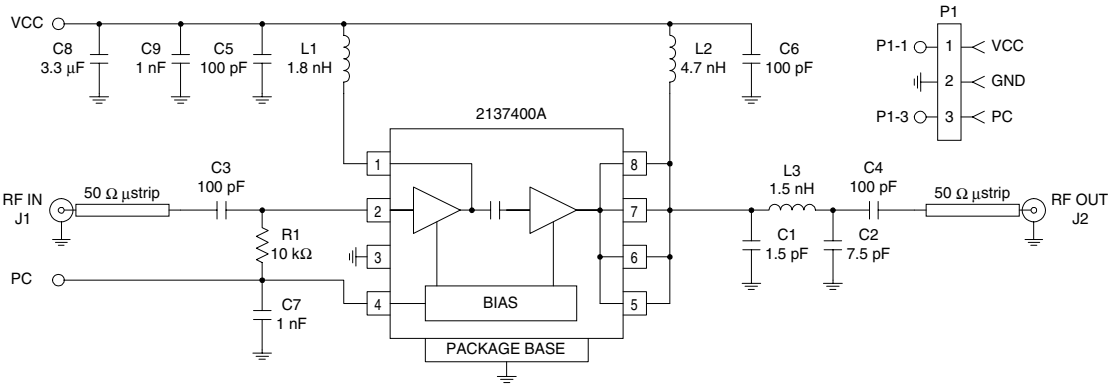
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5.0 V, V_{PC}=3.6V, Freq=824MHz to 849MHz
Usable Frequency Range	800	824 to 849	950	MHz	
Linear Gain	25	27	29	dB	
Total Linear Efficiency	40	45		%	
Efficiency at Max Output	50	55		%	
OFF Isolation		27		dB	V_{PC}=0V,P_{IN}=+6dBm
Second Harmonic		-30		dBc	Including Second Harmonic Trap
Maximum Linear Output Power		28.5	29	dBm	IS-95A CDMA Modulation
Adjacent Channel Power @ 885kHz offset		-46	-44	dBc	Pout = 28 dBm ACPR can be improved by trading off efficiency.
Adjacent Channel Power @ 1.98MHz offset		-58	-56	dBc	Pout = 28 dBm
Max CW Output Power	31.5	+32.0		dBm	
Input VSWR		<2:1			
Output Load VSWR			10:1		No oscillations
Power Down					
Turn On/Off Time			100	ns	
Total Current			10	µA	"OFF" State
V_{PC} "OFF" Voltage	0.2		0.5	V	Threshold Voltage at Input
V_{PC} "ON" Voltage	3.6		Vcc	V	Threshold Voltage at Input
Power Supply					
Power Supply Voltage	4.2	5.0	6.0	V	Operating voltage
Idle Current		40	100	mA	V_{PC}=4.0V
Current into VPC pin		15	20	mA	

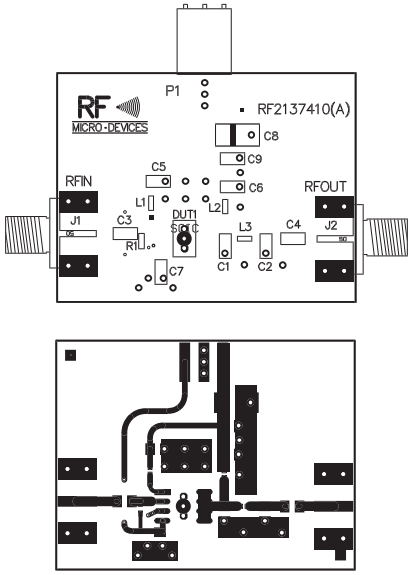
Pin	Function	Description	Interface Schematic
1	VCC	Power supply for the driver stage, and interstage matching. Shunt inductance is required on this pin, which can be achieved by an inductor to V_{CC}, with a decoupling capacitor on the V_{CC} side. The value of the inductor is frequency dependent; 3.3nH is required for 830MHz, and 1.2nH for 950MHz. Instead of an inductor, a high impedance microstrip line can be used.	
2	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
4	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V or less at room temperature. During normal operation this pin is the power control. Control range varies from about 2V for 0dBm to V_{CC} for +31dBm RF output power. The maximum power that can be achieved depends on the actual output matching. PC should never exceed 6.0V or V_{CC}, whichever is lowest.	
5	RF OUT	RF Output and power supply for the output stage. The three output pins are combined, and bias voltage for the final stage is provided through these pins. The external path must be kept symmetric until combined to ensure stability. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
6	RF OUT	Same as pin 5.	See pin 5.
7	RF OUT	Same as pin 5.	See pin 5.
8	RF OUT	Same as pin 5.	See pin 5.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
1.559" X 1.191"



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RF2138

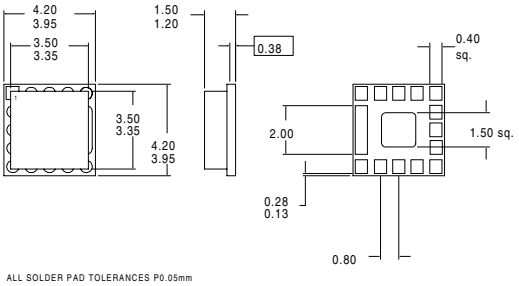
3V GSM POWER AMPLIFIER

Typical Applications

- 3V GSM Cellular Handsets
- 3V Dual-Band/Triple-Band Handsets
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

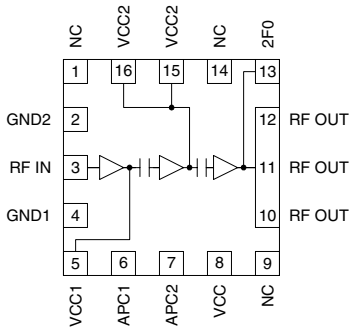
The RF2138 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in GSM hand held-digital cellular equipment and other applications in the 800MHz to 950MHz band. On-board power control provides over 70dB of control range with an analog voltage input, and provides power down with a logic "low" for standby operation. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics. The RF2138 can be used together with the RF2140 for dual-band operation. The device is packaged in an ultra-small ceramic package, minimizing the required board space.



Package Style: MP16K01A

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2.7V to 4.8V Supply Voltage
- +36dBm Output Power at 3.5V
- 32dB Gain with Analog Gain Control
- 58% Efficiency
- 800MHz to 950MHz Operation
- Supports GSM and E-GSM

Ordering Information

RF2138	3V GSM Power Amplifier
RF2138 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2138

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage ($V_{APC1,2}$)	-0.5 to +3.0	V
DC Supply Current	2400	mA
Input RF Power	+13	dBm
Duty Cycle at Max Power	37.5	%
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

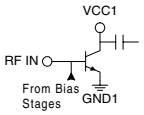
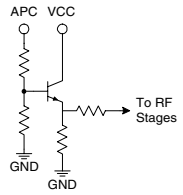
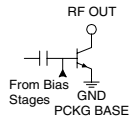
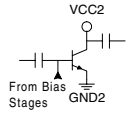
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V, P_{IN}=+6dBm, Freq=880MHz to 915MHz, 12.5% Duty Cycle, pulse width=577µs
Operating Frequency Range		880 to 915		MHz	See evaluation board schematic.
Usable Frequency Range		800 to 950		MHz	
Maximum Output Power	+35.0	+36		dBm	Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V
	+34.1	+35.2		dBm	Temp=+25°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
	+34.0			dBm	Temp=+85°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
	+33.0	+34.0		dBm	Temp=25°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
	+32.5			dBm	Temp=+85°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
Total Efficiency	50	58		%	At $P_{OUT,MAX}$, V_{CC}=3.2V
		58		%	At $P_{OUT,MAX}$, V_{CC}=3.0V
		12		%	P_{OUT}=+20dBm
		5		%	P_{OUT}=+10dBm
Input Power for Max Output	+4	+6	+8	dBm	
Output Noise Power			-72	dBm	RBW=100kHz, 925MHz to 935MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.0V to 5.0V
			-81	dBm	RBW=100kHz, 935MHz to 960MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.0V to 5.0V
Forward Isolation		-45	-40	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+6dBm
			-30	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+10dBm
Second Harmonic		-50	-38	dBc	P_{OUT}=$P_{OUT,MAX}$
Third Harmonic		-65	-43	dBc	P_{OUT}=$P_{OUT,MAX}$
Fourth Harmonic		-65	-55	dBc	P_{OUT}=$P_{OUT,MAX}$
Fifth Harmonic		-65	-50	dBc	P_{OUT}=$P_{OUT,MAX}$
Sixth Harmonic		-65	-40	dBc	P_{OUT}=$P_{OUT,MAX}$
All Non-Harmonic Spurious			-36	dBm	<1GHz
			-30	dBm	>1GHz
Input Impedance		50		Ω	
Optimum Source Impedance		40+j10		Ω	For best noise performance
Input VSWR			2.5:1		$P_{OUT,MAX}$-5dB<P_{OUT}<$P_{OUT,MAX}$
			4:1		P_{OUT}<$P_{OUT,MAX}$-5dB
Output Load VSWR	10:1				Spurious<-36dBm, $V_{APC1,2}$=0.2V to 2.6V, RBW=3MHz
Output Load Impedance		1.5-j1.7		Ω	Load Impedance presented at RF OUT pad

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Control V_{APC1} V_{APC2}					
Power Control "ON"	2.6			V	Maximum P_{OUT}, Voltage supplied to the input
Power Control "OFF"	0.2	0.5		V	Minimum P_{OUT}, Voltage supplied to the input
Power Control Range	75			dB	$V_{APC1,2}$=0.2V to 2.6V
Gain Control Slope	5	100	150	dB/V	P_{OUT}=-10dBm to +35dBm
APC Input Capacitance			10	pF	DC to 2MHz
APC Input Current		4.5	5	mA	$V_{APC1,2}$=2.6V
			10	µA	$V_{APC1,2}$=0V
Turn On/Off Time			100	ns	$V_{APC1,2}$=0 to 2.6V
Power Supply					
Power Supply Voltage		3.5		V	Specifications
	2.7		4.8	V	Nominal operating limits, P_{OUT}<+35dBm
			5.5	V	With maximum output load VSWR 6:1, P_{OUT}<+35dBm
Power Supply Current		2		A	DC Current at $P_{OUT,MAX}$
	50	200	375	mA	Idle Current, P_{IN}<-30dBm
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V, Temp=+85°C

RF2138

Pin	Function	Description	Interface Schematic
1	NC	Not connected. Connect this pin to the ground plane for compatibility with future packages.	
2	GND2	Ground connection for the driver stage. To minimize the noise power at the output, it is recommended to connect this pin with a trace of about 40mil to the ground plane. This will slightly reduce the small signal gain, and lower the noise power. It is important for stability that this pin have it's own vias to the ground plane, minimizing common inductance.	See pin 15.
3	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 5. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
4	GND1	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance.	See pin 3.
5	VCC1	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Refer to the application schematic for proper configuration. Note that position and value of the components are important.	See pin 3.
6	APC1	Power Control for the driver stage and pre-amplifier. When this pin is "low," all circuits are shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. During normal operation this pin is the power control. Control range varies from about 1.0V for -10dBm to 2.6V for +35dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details. The maximum current into this pin is 5mA when V_{APC1}=2.6V, and 0mA when V_{APC}=0V.	
7	APC2	Power Control for the output stage. See pin 6 for more details.	See pin 6.
8	VCC	Power supply for the bias circuits.	See pin 6.
9	NC	Not connected. Connect this pin to the ground plane for compatibility with future packages.	
10	RF OUT	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pin. An external matching network is required to provide the optimum load impedance.	
11	RF OUT	Same as pin 10.	Same as pin 10.
12	RF OUT	Same as pin 10.	Same as pin 10.
13	2F0	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. The bonding wire together with an external capacitor form a series resonator that should be tuned to the second harmonic frequency in order to increase efficiency and reduce spurious outputs.	Same as pin 10.
14	NC	Not connected.	
15	VCC2	Power supply for the driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	
16	VCC2	Same as pin 15.	Same as pin 15.
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the ground plane by vias directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

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Theory of Operation and Application Information

The RF2138 is a three-stage device with 32 dB gain at full power. Therefore, the drive required to fully saturate the output is +3dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 3V supply to operate to full specification. Power control is provided through a single pin interface, with a separate Power Down control pin. The final stage ground is achieved through the large pad in the middle of the backside of the package. First and second stage grounds are brought out through separate ground pins for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane, and not connected with the output ground to form a so called “local ground plane” on the top layer of the PCB. The output is brought out through the wide output pad, and forms the RF output signal path.

The amplifier operates in near Class C bias mode. The final stage is "deep AB", meaning the quiescent current is very low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 2000mA. The optimum load for the output stage is approximately 1.2Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, vias, and microstrip, and 2 shunt capacitors external to the part. The optimum load impedance at the RF Output pad is 1.2-j1.7Ω. With this match, a 50Ω terminal impedance is achieved. The input is internally matched to 50Ω with just a blocking capacitor needed. This data sheet defines the configuration for GSM operation.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

VCC1 and VCC2 provide supply voltage to the first and second stage, as well as provides some frequency selectivity to tune to the operating band. Essentially, the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be bypassed individually with 100pF capacitors before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RF OUT pin provides the output power. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 2A of current required. Care should be taken to keep the losses low in the bias feed and output components. A narrow microstrip line is recommended because DC losses in a bias choke will degrade efficiency and power.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in this data sheet is based on a 12.5% duty cycle and a 600μs pulse, unless specified otherwise.

The part will operate over a 3.0V to 5.0V range. Under nominal conditions, the power at 3.5V will be greater than +34.5dBm at +90°C. As the voltage is increased, however, the output power will increase. Thus, in a system design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This must occur during operation, or the device may be damaged from too much power dissipation. At 5.0V, over +38dBm may be produced; however, this level of power is not recommended, and can cause damage to the device.

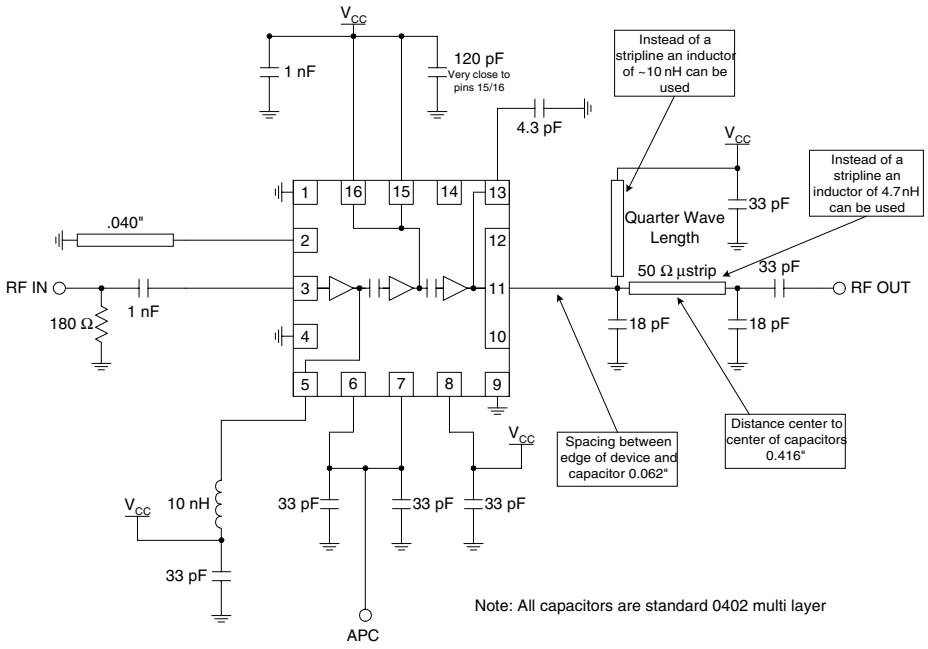
The HBT breakdown voltage is >20V, so there are no issue with overvoltage. However, under worst-case conditions, with the RF drive at full power during transmit, and the output VSWR extremely high, a low load impedance at the collector of the output transistors can cause currents much higher than normal. Due to the bipolar nature of the devices, there is no limitation on the amount of current de device will sink, and the safe current densities could be exceeded.

High current conditions are potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2138 includes temperature compensation circuits in the bias network to stabilize the RF transistors, thus limiting the current through the amplifier and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations.

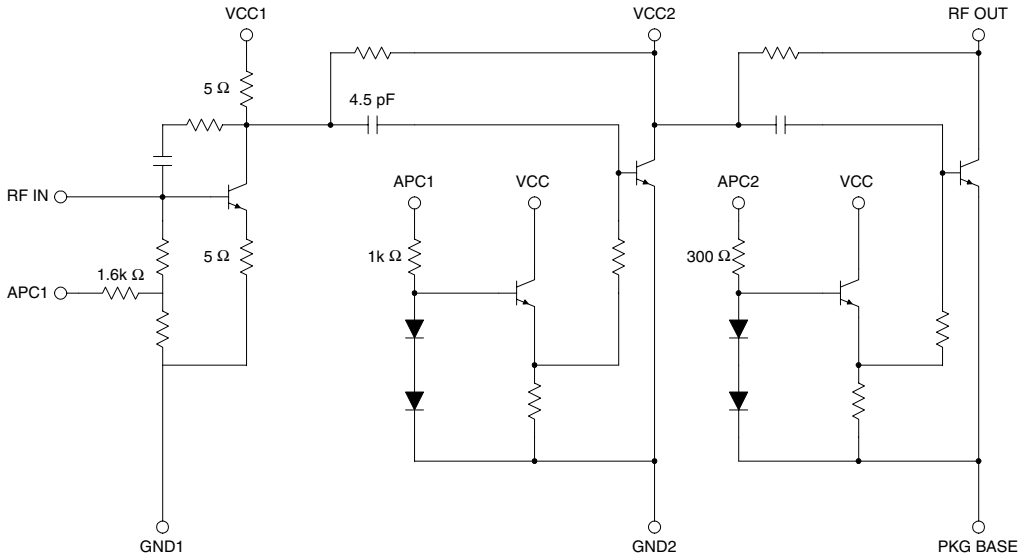
To avoid excessively high currents it is important to control the V_{APC} when operating at supply voltages higher than 4.0V, such that the maximum output power is not exceeded.

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Application Schematic



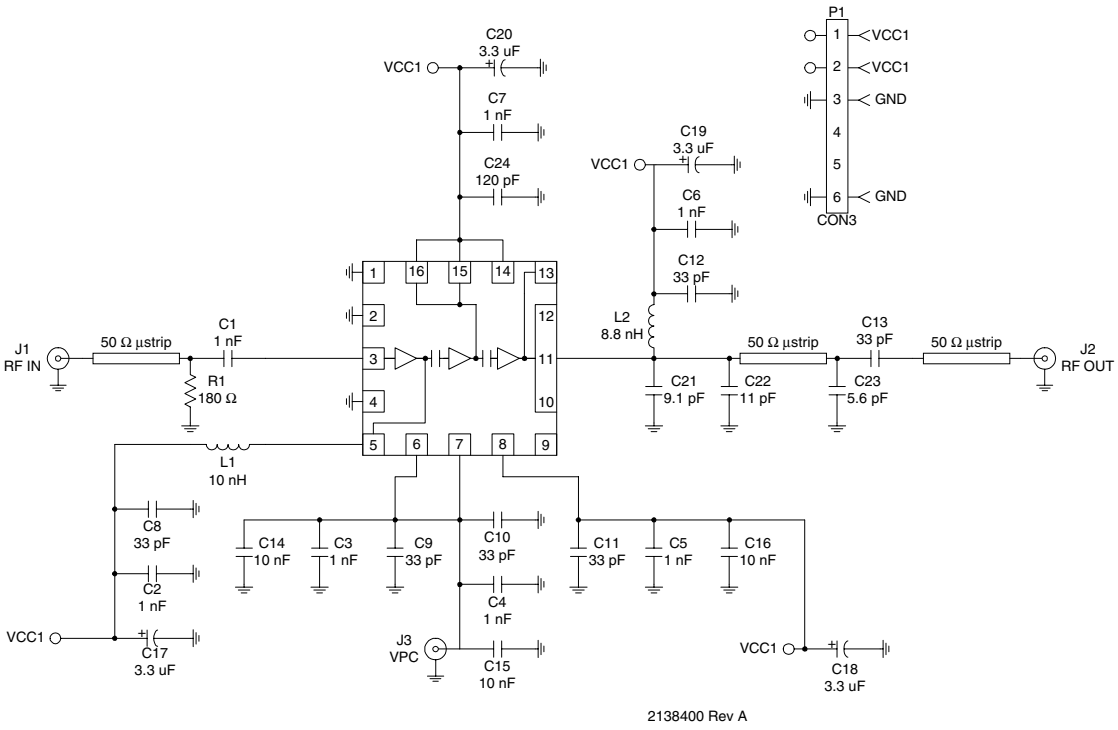
Internal Schematic



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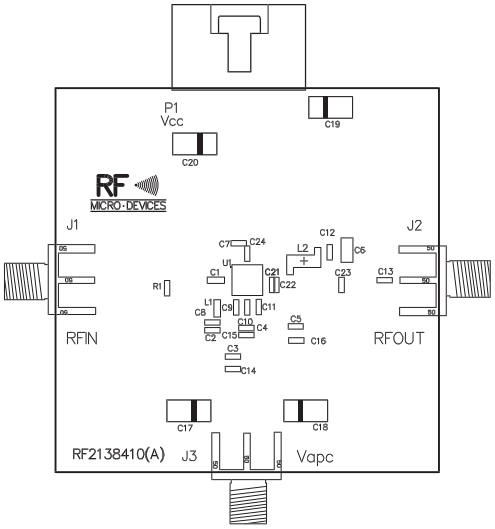
Evaluation Board Schematic

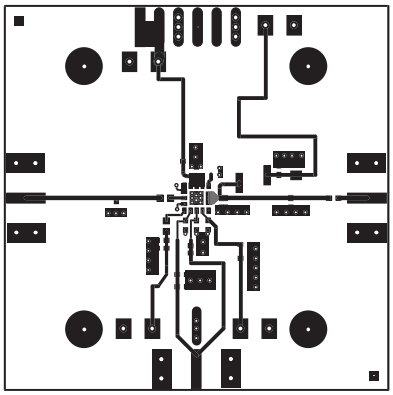
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board size 2.0” x 2.0”

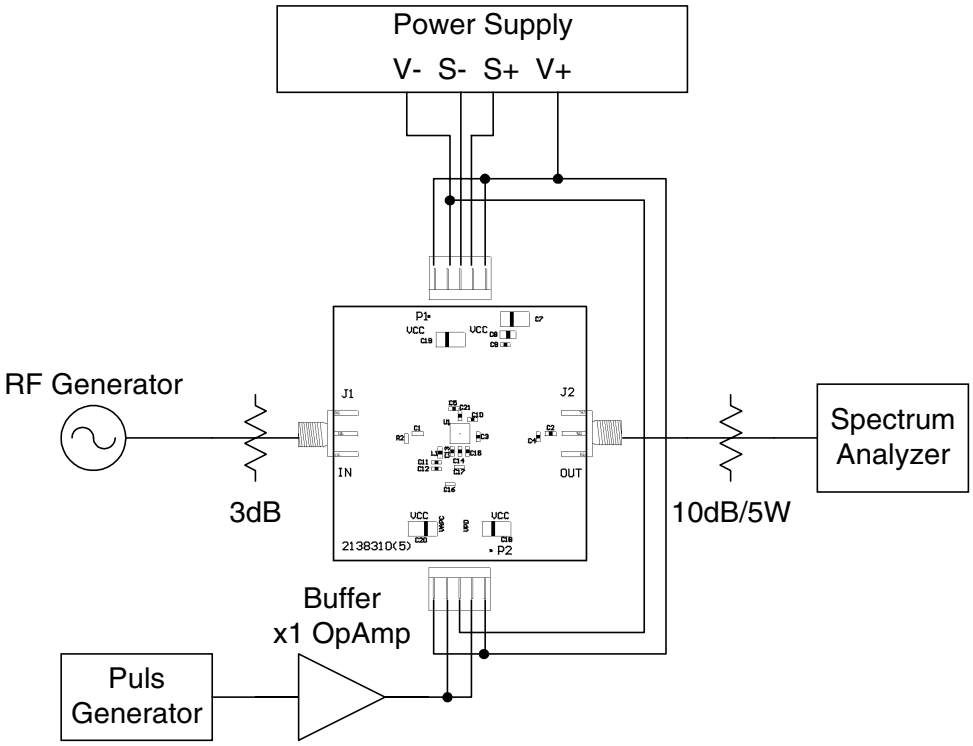
Board Thickness 0.014”; Board Material FR-4; Multi-Layer





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Typical Test Setup



A buffer amplifier is recommended because the current into the Vapc changes with voltage. As an alternative, the voltage may be monitored with an oscilloscope.

Notes about testing the RF2138

The test setup shown above includes two attenuators. The 3dB pad at the input is to minimize the effects that the switching of the input impedance of the PA has on the signal generator. When Vapc is switched quickly, the resulting input impedance change can cause the signal generator to vary its output signal, either in output level or in frequency. Instead of an attenuator an isolator may also be used. The attenuator at the output is to prevent damage to the spectrum analyzer, and should be able to handle the power.

It is important not to exceed the rated supply current and output power. When testing the device at higher than nominal supply voltage, the V_{APC} should be adjusted to avoid the output power exceeding +36dBm. During load-pull testing at the output it is important to monitor the forward power through a directional coupler. The forward power should not exceed +36dBm, and V_{APC} needs to be adjusted accordingly. This simulates the behavior for the power control loop in this respect. To avoid damage, it is recommended to set the power supply to limiting the current during the burst, not to exceed the maximum current rating.

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RF2140

3V DCS POWER AMPLIFIER

Typical Applications

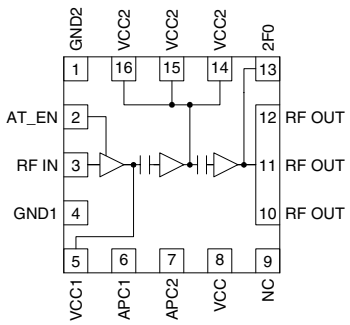
- 3V DCS1800 (PCN) Cellular Handsets
- 3V DCS1900 (PCS) Cellular Handsets
- 3V Dual-Band/Triple-Band Handsets
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

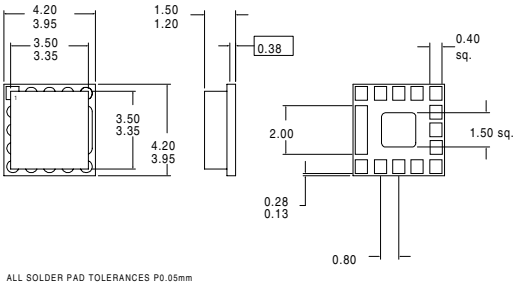
The RF2140 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in DCS1800/1900 hand held-digital cellular equipment and other applications in the 1700MHz to 2000MHz band. On-board power control provides over 65dB of control range with an analog voltage input, and provides power down with a logic "low" for standby operation. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics.The RF2140 can be used together with the RF2138 for dual-band operation. The device is packaged in an ultra-small ceramic package, minimizing the required board space.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: MP16K01A

Features

- Single 2.7V to 4.8V Supply Voltage
- +33dBm Output Power at 3.5V
- 27dB Gain with Analog Gain Control
- 51% Efficiency
- 1700MHz to 1950MHz Operation
- Supports DCS1800 and PCS1900

Ordering Information

RF2140	3V DCS Power Amplifier
RF2140 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2140

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{APC})	-0.5 to +3.0	V
Enable Voltage (V_{AT_EN})	-0.5 to +3.0	V
DC Supply Current	1500	mA
Input RF Power	+13	dBm
Duty Cycle at Max Power	37.5	%
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

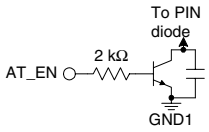
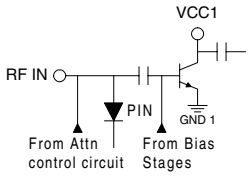
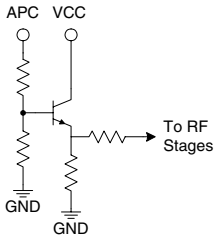
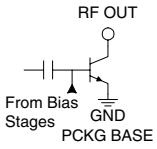
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V, V_{AT_EN}=2.6V, P_{IN}=+6dBm, Freq=1710MHz to 1910MHz, 12.5% Duty Cycle, pulse width=577µs
Operating Frequency Range		1710 to 1785		MHz	See application schematic for tuning details.
		1850 to 1910		MHz	A different tuning is required.
Usable Frequency Range		1700 to 2000		MHz	
Maximum Output Power	+32	+33		dBm	Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V
	+31.5	+32.8		dBm	Temp=+25°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
		+31.5		dBm	Temp=+85°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
		+31		dBm	Temp=25°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
	+29.5	+30		dBm	Temp=+85°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
Total Efficiency	45	51		%	At $P_{OUT,MAX}$, V_{CC}=3.5V
		51		%	At $P_{OUT,MAX}$, V_{CC}=3.0V
		15		%	P_{OUT}=+20dBm
		10		%	P_{OUT}=+10dBm
Recommended Input Power Range	+5	+7	+9	dBm	
Output Noise Power			-79	dBm	RBW=100kHz, 1805MHz to 1880MHz and 1930MHz to 1990MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.0V to 5.0V
Forward Isolation		-37	-30	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+10dBm
		-40	-35	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+6dBm
Second Harmonic		-60	-45	dBc	
Third Harmonic		-65	-50	dBc	
Fourth Harmonic		-50	-45	dBc	
Fifth Harmonic		-50	-45	dBc	
Sixth Harmonic		-50	-45	dBc	
All Other Non-Harmonic Spurious			-36	dBm	
Input Impedance		50		Ω	
Input VSWR			2.2:1		$P_{OUT,MAX}$-5dB<P_{OUT}<$P_{OUT,MAX}$
			3:1		P_{OUT}<$P_{OUT,MAX}$-5dB
Output Load VSWR	10:1				Spurious<-36dBm, $V_{APC1,2}$=0.2V to 2.6V, RBW=3MHz
Output Load Impedance		4.5-j3.9		Ω	Load Impedance presented at RF OUT pin

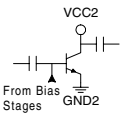
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Control					
Power Control "ON"			2.6	V	Maximum P_{OUT}, Voltage supplied to the input
Power Control "OFF"	0.2	0.5		V	Minimum P_{OUT}, Voltage supplied to the input
Attenuator Enable "ON"	2.5	2.6	2.85	V	For maximum isolation when V_{APC} is low
Attenuator Enable "OFF"	0.2	0.5		V	For power down mode
Power Control Range	62	68		dB	$V_{APC1,2}$=0.2V to 2.6V, V_{AT_EN}=2.6V, P_{IN}=+10dBm
Gain Control Slope		100		dB/V	P_{OUT}=-10dBm to +33dBm
APC Input Capacitance			10	pF	DC to 2MHz
APC Input Current		4.5	5	mA	$V_{APC1,2}$=2.6V
			10	µA	$V_{APC1,2}$=0V
AT_EN Input Current			500	µA	V_{AT_EN}=2.6V, $V_{APC1,2}$=0V
			10	µA	V_{AT_EN}=0V, $V_{APC1,2}$=0V
Turn On/Off Time			100	ns	
Power Supply					
Power Supply Voltage		3.5		V	Specifications
	2.7		4.8	V	Nominal operating limits, P_{OUT}<+33dBm
			5.5	V	With maximum output load VSWR 6:1, P_{OUT}<+33dBm
Power Supply Current		1.3		A	DC Current at $P_{OUT,MAX}$
	55		295	mA	Idle Current, P_{IN}<-30dBm
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V, Temp=+85°C

RF2140

Pin	Function	Description	Interface Schematic
1	GND2	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance. This pin is internally connected to the ground slug.	See pin 15.
2	AT_EN	Control input for the PIN diode. The purpose of the PIN diode is to attenuate the RF input drive level when the V_{APC} is low. This serves both to reduce the leakage through the device cause by self biasing when driving with high level at the RF input, as well as to maintain a good input match when the bias of the input stage is turned off. When this pin is "high" the PIN diode control is turned on. See the Theory of Operation for more details.	
3	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 5. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
4	GND1	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance.	See pin 3.
5	VCC1	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	See pin 3.
6	APC1	Power Control for the driver stage and pre-amplifier. When this pin is "low," all circuits are shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. During normal operation this pin is the power control. Control range varies from about 1.0V for -10dBm to 2.6V for +33dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details. The maximum current into this pin is 5mA when V_{APC1}=2.6V, and 0mA when V_{APC}=0V.	
7	APC2	Power Control for the output stage. See pin 6 for more details.	See pin 6.
8	VCC	Power supply for the bias circuits.	See pin 6.
9	NC	Not connected. Connect this pin to the ground plane for compatibility with future packages.	
10	RF OUT	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pin. An external matching network is required to provide the optimum load impedance.	
11	RF OUT	Same as pin 10.	Same as pin 10.
12	RF OUT	Same as pin 10.	Same as pin 10.
13	2F0	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. The bonding wire together with an external capacitor form a series resonator that should be tuned to the second harmonic frequency in order to increase efficiency and reduce spurious outputs.	Same as pin 10.
14	VCC2	Same as pin 15.	

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Pin	Function	Description	Interface Schematic
15	VCC2	Power supply for the driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	
16	VCC2	Same as pin 15.	Same as pin 15.
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the groundplane by vias directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

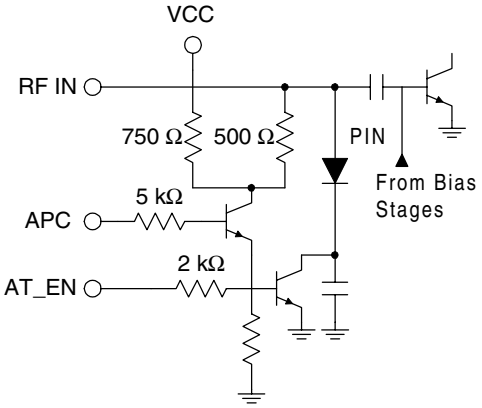
Theory of Operation and Application Information

The RF2140 is a three-stage device with 28 dB gain at full power. Therefore, the drive required to fully saturate the output is +5dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 3V supply to operate to full specification. Power control is provided through a single pin interface, with a separate Power Down control pin. The final stage ground is achieved through the large pad in the middle of the backside of the package. First and second stage grounds are brought out through separate ground pins for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane, and not connected with the output ground to form a so called “local ground plane” on the top layer of the PCB. The output is brought out through the wide output pad, and forms the RF output signal path.

The amplifier operates in near Class C bias mode. The final stage is "deep AB", meaning the quiescent current is very low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 1500mA. The optimum load for the output stage is approximately 4.5Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, vias, and microstrip, and 2 shunt capacitors external to the part. The optimum load impedance at the RF Output pad is 4.5-j3.9Ω. With this match, a 50Ω terminal impedance is achieved. The input is internally matched to 50Ω with just a blocking capacitor needed. This data sheet defines the configuration for GSM operation.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

When the device is driven at maximum input power self biasing would occur. This results in less isolation than one would expect, and the maximum output power would be about -15dBm. If the drive power to the PA is turned on before the GSM ramp-up, higher isolation is required. In order to meet the GSM system specs under those conditions, a PIN diode attenuator connected to the input can be turned on. The figure below shows how the attenuator and its controls are connected.



The current through the PIN diode is controlled by two signals: AT_EN and APC. The AT_EN signal allows current through the PIN diode and is an on/off function. The APC signal controls the amount of current through the PIN diode. Normally, the AT_EN signal will be derived from the VCO ENABLE signal available in most GSM handset designs. If maximum isolation is needed before the ramp-up, the AT_EN signal needs to be turned on before the RF power is applied to the device input. The current into this pin is not critical, and can be reduced to a few hundred micro amps with an external series resistor. Without the resistor, the pin will draw about 700μA.

Because of the inverting stage at the APC input, the current through the PIN diode is inverted from the APC voltage. Thus, when V_{APC} is high for maximum output power, the attenuator is turned off to obtain maximum drive level for the first RF stage. When V_{APC} is low for maximum isolation, the attenuator is be turned on to reduce the drive level and to avoid self-biasing.

The PIN diode is dimensioned such that a low V_{APC} the impedance of the diode is about 50 Ohm. Since the input impedance of the first RF stage become very high when the bias is turned off, this topology will maintain a good input impedance over the entire V_{APC} control range.

VCC1 and VCC2 provide supply voltage to the first and second stage, as well as provides some frequency selectivity to tune to the operating band. Essentially,

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the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be bypassed individually with 100pF capacitors before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RF OUT pin provides the output power. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 1.5A of current required. Care should be taken to keep the losses low in the bias feed and output components. A narrow microstrip line is recommended because DC losses in a bias choke will degrade efficiency and power.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in this data sheet is based on a 12.5% duty cycle and a 600µs pulse, unless specified otherwise.

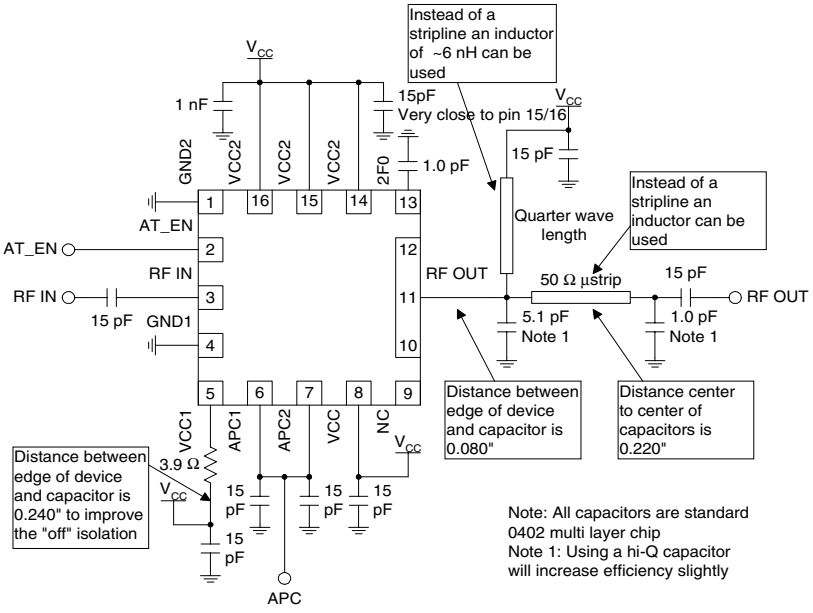
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The HBT breakdown voltage is >20V, so there is no issue with overvoltage. However, under worst-case conditions, with the RF drive at full power during transmit, and the output VSWR extremely high, a low load impedance at the collector of the output transistors can cause currents much higher than normal. Due to the bipolar nature of the devices, there is no limitation on the amount of current the device will sink, and the safe current densities could be exceeded.

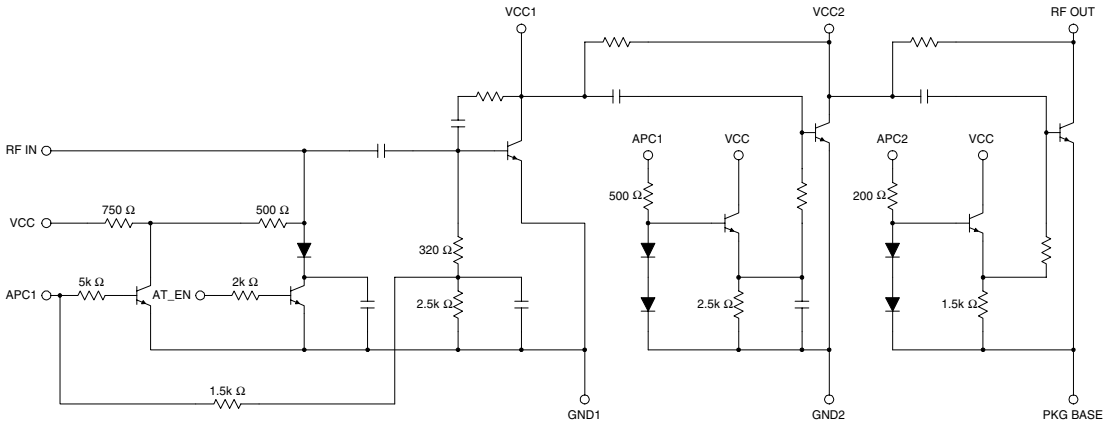
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To avoid excessively high currents it is important to control the V_{APC} when operating at supply voltages higher than 4.0V, such that the maximum output power is not exceeded.

Application Schematic

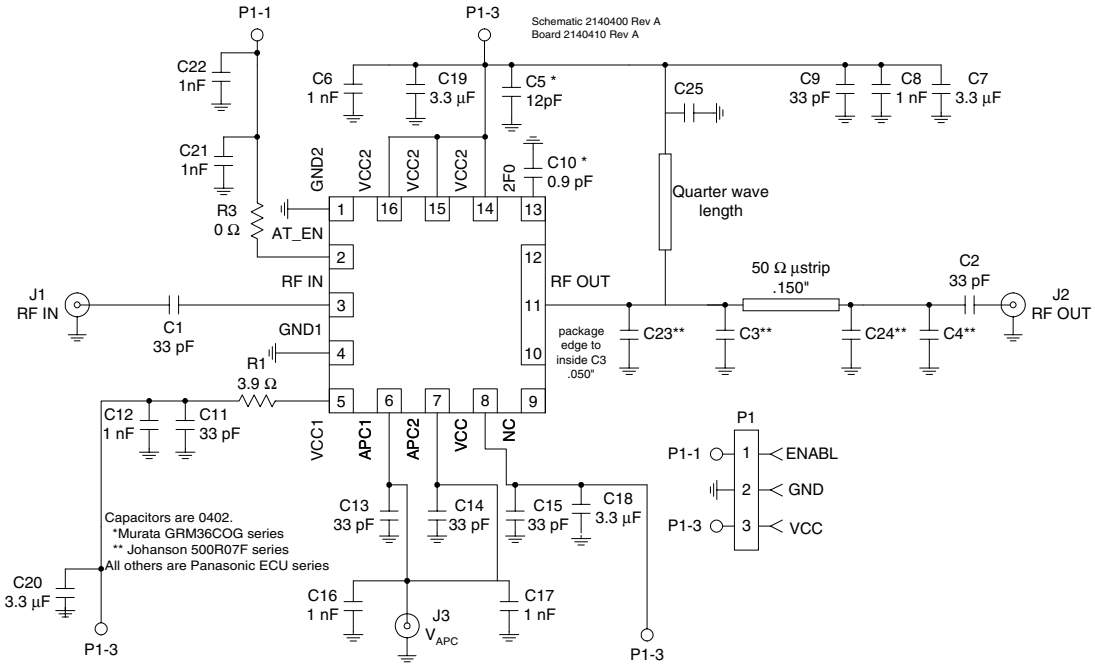


Internal Schematic



Evaluation Board Schematic

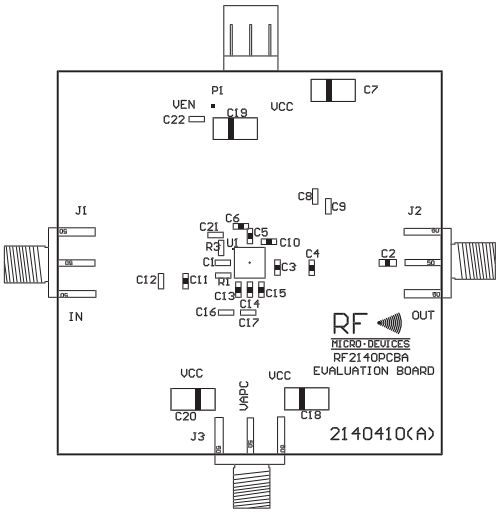
(Download Bill of Materials from www.rfmd.com.)

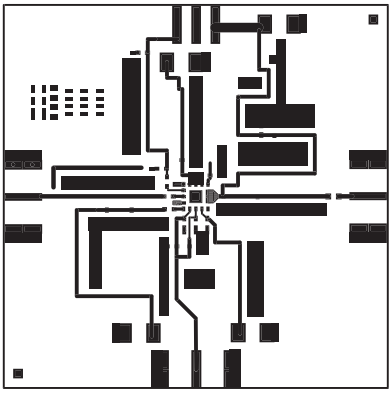


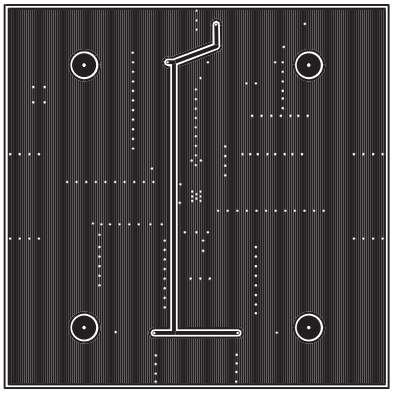
Band	C3 (pF)	C4 (pF)	C23 (pF)	C24 (pF)	C25 (pF)
DCS	5.1	1.8	N/I	N/I	N/I
PCS	3.9	1.2	0.5	0.6	0.5

Evaluation Board Layout
Board size 2.0” x 2.0”

Board Thickness 0.014”; Board Material FR-4; Multi-Layer

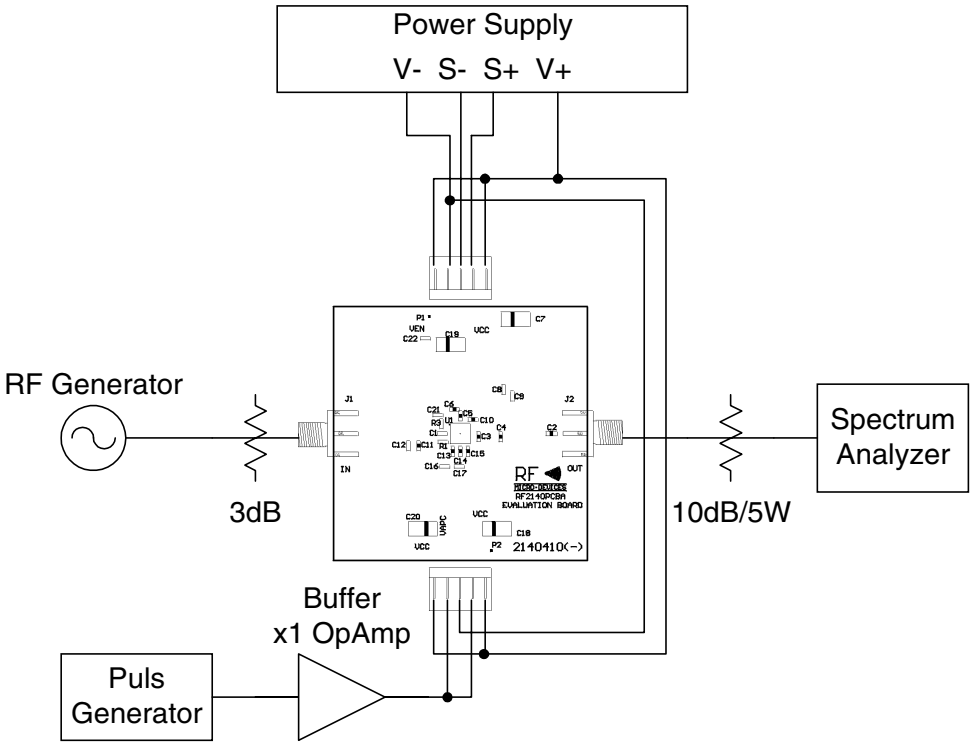






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Typical Test Setup



A buffer amplifier is recommended because the current into the Vapc changes with voltage. As an alternative, the voltage may be monitored with an oscilloscope.

Notes about testing the RF2140

The test setup shown above includes two attenuators. The 3dB pad at the input is to minimize the effects that the switching of the input impedance of the PA has on the signal generator. When Vapc is switched quickly, the resulting input impedance change can cause the signal generator to vary its output signal, either in output level or in frequency. Instead of an attenuator an isolator may also be used. The attenuator at the output is to prevent damage to the spectrum analyzer, and should be able to handle the power.

It is important not to exceed the rated supply current and output power. When testing the device at higher than nominal supply voltage, the V_{APC} should be adjusted to avoid the output power exceeding +36dBm. During load-pull testing at the output it is important to monitor the forward power through a directional coupler. The forward power should not exceed +36dBm, and V_{APC} needs to be adjusted accordingly. This simulates the behavior for the power control loop in this respect. To avoid damage, it is recommended to set the power supply to limiting the current during the burst, not to exceed the maximum current rating.

RF2140

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RF2145

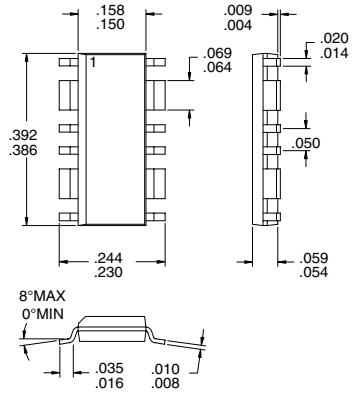
DCS1800/1900 POWER AMPLIFIER

Typical Applications

- 4.8V DCS1800/1900 Handsets
- 3V DECT Handsets and Base Stations
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

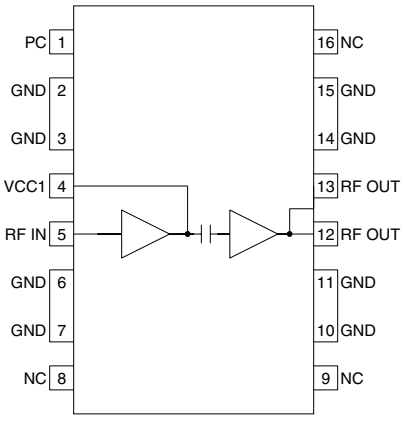
The RF2145 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in a 4-cell DCS1800 or DCS1900 handset. The device is packaged in a 16-lead plastic package with wide ground leads, and is self-contained with the exception of the output matching network and power supply feed line. Only a single positive voltage is required to operate with full power and efficiency, and on-board power control and power-down functions are provided.



Package Style: SOP-16 QBW1

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 4.8V Power Supply
- +32dBm Output Power
- 28dB Small Signal Gain
- 55% Power Added Efficiency
- Power Control
- 1700MHz to 1900MHz Frequency Range

Ordering Information

RF2145	DCS1800/1900 Power Amplifier
RF2145 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2145

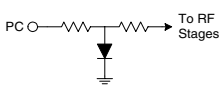
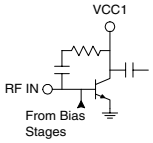
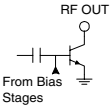
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +3.0	V
DC Supply Current	675	mA
Input RF Power	+12	dBm
Output Load VSWR	5:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

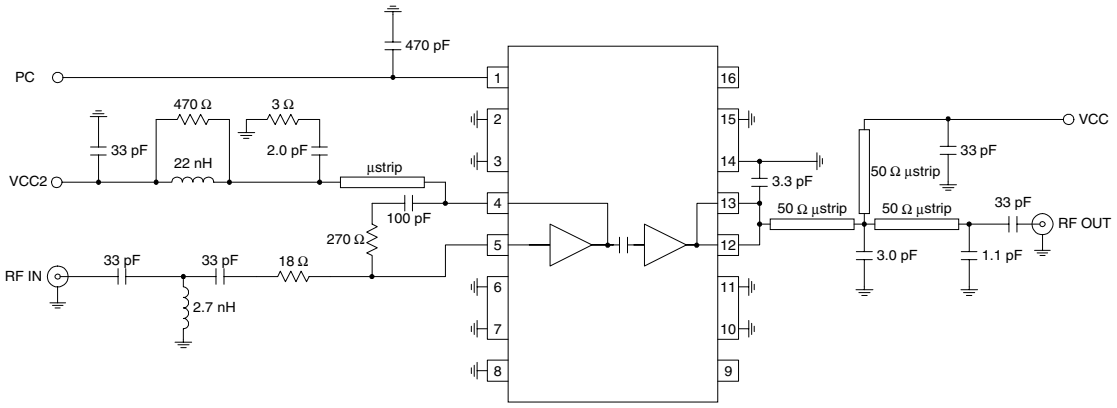
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.8V, V_{PC}=2.5V, P_{IN}=+8dBm, Freq=1750MHz
Operating Frequency Range		1710 to 1785 1850 to 1910		MHz	
Usable Frequency Range		1700 to 1990		MHz	
Maximum Output Power		+32		dBm	1/8 Duty cycle with 600µs pulse width
Total Efficiency		55		%	At maximum output power
Input Power for Max Output		+8		dBm	
Input Intermodulation Distortion		-57		dBc	Input signal consists of F_1 at 1785MHz at +8dBm, F_2 at 1765MHz at -42dBm. Output power at F_1 is set to +32.5dBm. Specified power level at 1805MHz relative to F_1. This refers to the amount of TX band noise which converts into the receive band.
		-48		dBc	Input signal consists of F_1 at 1785MHz at +8dBm, F_2 at 1765MHz at -32dBm. Output power at F_1 is set to +32.5dBm. Specified power level at 1805MHz relative to F_1. This refers to the amount of TX band noise which converts into the receive band.
Output Noise Power in Receive Band		-137		dBm/Hz	Any gain setting
Isolation		-25		dBm	In "OFF" state, P_{IN}=+8dBm
Second Harmonic		-48		dBc	
Third Harmonic		<-60		dBc	
Input Impedance		50		Ω	
Input VSWR			3.8:1		Worst-case across the band. Using evaluation board; can be different with other layouts
Output Load VSWR	3:1				Spurious<-60dBc
Power Control					
Power Control "ON"		2.5	3.0	V	Threshold voltage
Power Control "OFF"	0.2	0.5		V	Threshold voltage
Current into PC Input		15		mA	In "ON" state
			10	µA	In "OFF" state
Power Control Range	45			dB	
Turn On/Off TIme			100	ns	
Power Supply					
Power Supply Voltage		4.8		V	Specifications
	2.7		6.5	V	Operating limits
Power Supply Current		550		mA	DC Current at maximum output power
			10	µA	V_{PC}=0.5V

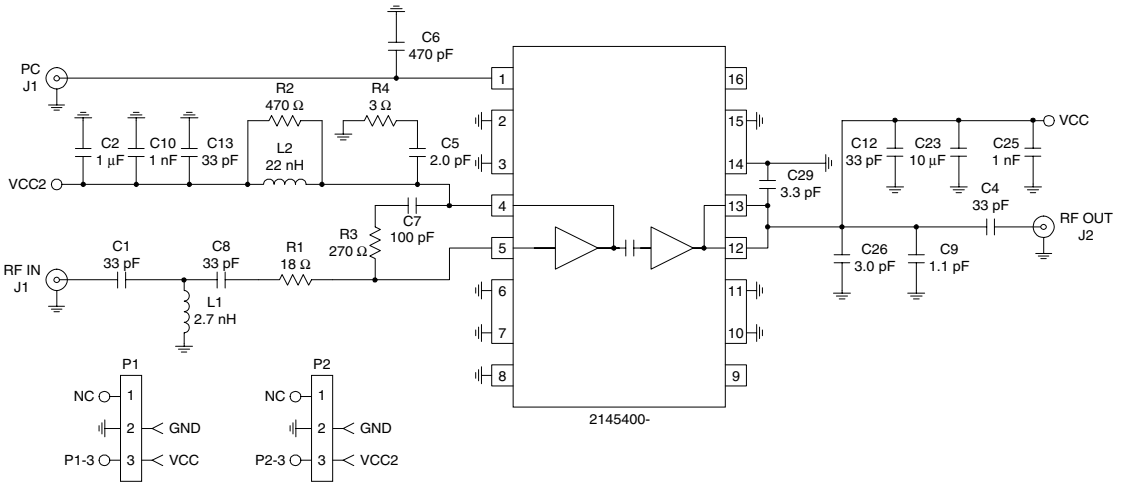
Pin	Function	Description	Interface Schematic
1	PC	Power control pin. This also provides power down when V_{PC} is less than +0.5V. Full power is achieved at 2.5V, and >45dB of gain control is obtainable over the full range. Approximately 15mA current is drawn into this pin at full power.	
2	GND	Ground connection. This pin should be connected to the ground plane through a short path and may be combined with the ground plane from Pins 3, 6, 7, 10, 11, 14, and 15. All four of these wide leads are tied together internally to provide a low-inductance and low thermal resistance path to external ground. Ground vias should be placed as close as possible to each ground lead.	
3	GND	Same as pin 2.	
4	VCC1	Power supply pin for the first stage. Also provides tuning for interstage match.	
5	RF IN	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path.	See pin 4 schematic.
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	NC	No connection.	
9	NC	No connection.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	RF OUT	RF output pin. Bias is also fed to the final stage through this wide lead. External matching is most easily achieved with a series transmission line and shunt capacitors, as shown in the application schematic.	
13	RF OUT	Same as pin 12.	
14	GND	Same as pin 2.	
15	GND	Same as pin 2.	
16	NC	No connection.	

Application Schematic
DCS 1800



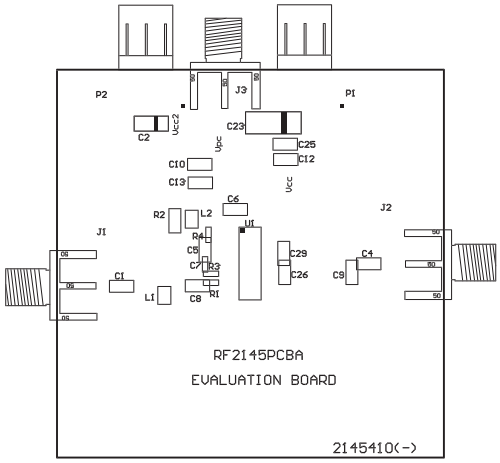
Evaluation Board Schematic

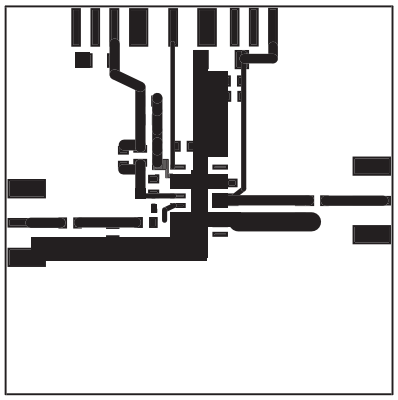
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
2” x 2”





RF2145

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RF2146

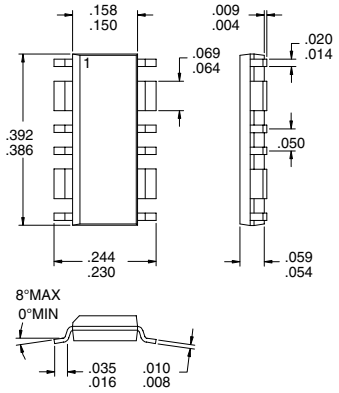
PCS LINEAR POWER AMPLIFIER

Typical Applications

- 4.8V CDMA PCS Handsets
- 4.8V TDMA PCS Handsets
- 4.8V PACS PCS Handsets
- Driver Amplifier in Cellular Base Stations
- Portable Battery Powered Equipment

Product Description

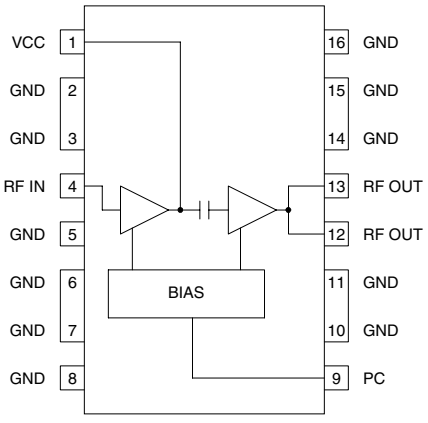
The RF2146 is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 4-cell CDMA hand-held digital cellular equipment, spread spectrum systems, and other applications in the 1500 to 2000 MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics.



Package Style: SOP-16 QBW1

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 4V to 6.5V Supply
- 28.5dBm Linear Output Power
- 18.5dB Gain With Analog Gain Control
- 37% Linear Efficiency
- On-board Power Down Mode
- 1500MHz to 2000MHz Operation

Ordering Information

RF2146	PCS Linear Power Amplifier
RF2146 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2146

Absolute Maximum Ratings

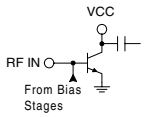
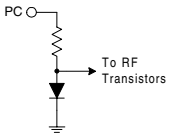
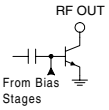
Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V_{DC}
Supply Voltage (P_{OUT}<30dBm)	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +5.0 or V_{CC}	V
DC Supply Current	500	mA
Input RF Power	+15	dBm
Output Load VSWR	10:1	
Ambient Operating Temperature	-30 to +90	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

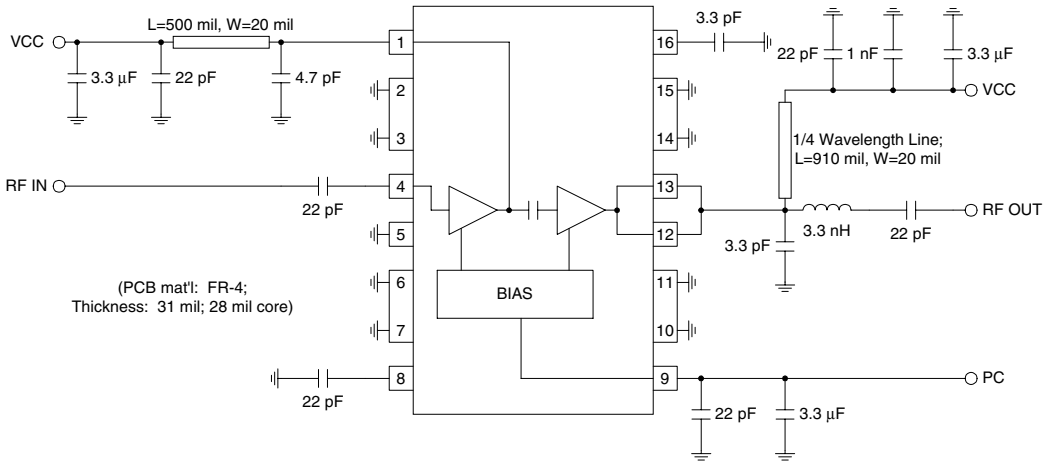
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.8V, V_{PC}=3.6V, P_{IN}=+10dBm, Freq=1880MHz
Usable Frequency Range		1500 to 2000		MHz	
Linear Gain		18.5	19	dB	
Maximum Linear Output Power		28.5			CDMA Modulation
Total Linear Efficiency		37		%	
Input Power for 28 dBm Output		+10		dBm	
Adjacent Channel Power Rejection	-45			dBc	CDMA Modulation, +28 dBm Output, At 1.25MHz Offset
Input VSWR		<2:1			
Second Harmonic		-35		dBc	Including Second Harmonic Trap
Power Down					
Off Isolation		25		dB	
Turn On Time		200		ns	Up to -0.5 dB of Final Power
Turn Off Time		350		ns	Down to +0.5 dB of Final Power
Total Current			TBD	µA	"OFF" State
V_{PC} "OFF" Voltage		0	0.2	V	Threshold Voltage at Input
V_{PC} "ON" Voltage	3.4	3.6		V	Threshold Voltage at Input
Power Supply					
Power Supply Voltage		4.0 to 6.5		V	Operating voltage
Current into V_{PC} pin		13		mA	"ON" State
Idle Current		70		mA	V_{PC}=3.6V, No RF Applied

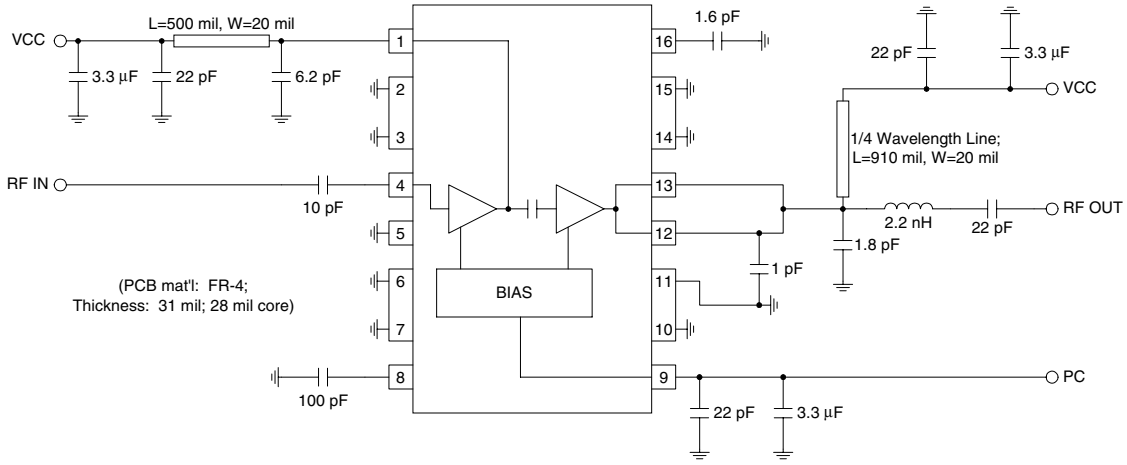
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Pin	Function	Description	Interface Schematic
1	VCC	Power supply for the driver stage, and interstage matching. Shunt capacitance is required on this pin. The value of the capacitance is frequency dependent. 4.7pF centers the gain at 1880 MHz.	
2	GND	Ground connection for final stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	GND	Same as pin 2.	
4	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
5	GND	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	BYP1	Bypass Pin. Part of the matching circuit for interstage match. DC connected to VCC1. Use a suitable bypass capacitor to ground. Keep capacitor as close to pin as possible.	See pin 1.
9	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V. When this pin is "high", the part operates normally, and the pin consumes approximately 13mA during normal operation. This pin should never exceed 5V.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	RF OUT	RF Output and power supply for the output stage. The two output pins are combined, and bias voltage for the final stage is provided through these pins. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
13	RF OUT	Same as pin 12.	See pin 12.
14	GND	Same as pin 2.	
15	GND	Same as pin 2.	
16	BYP2	Bypass Pin. Part of the matching circuit for interstage match. DC connected to VCC1. For 1880 MHz operation, use a 3.3pF capacitor to ground. Keep capacitor as close to pin as possible.	See pin 1.

Application Schematic
1880MHz



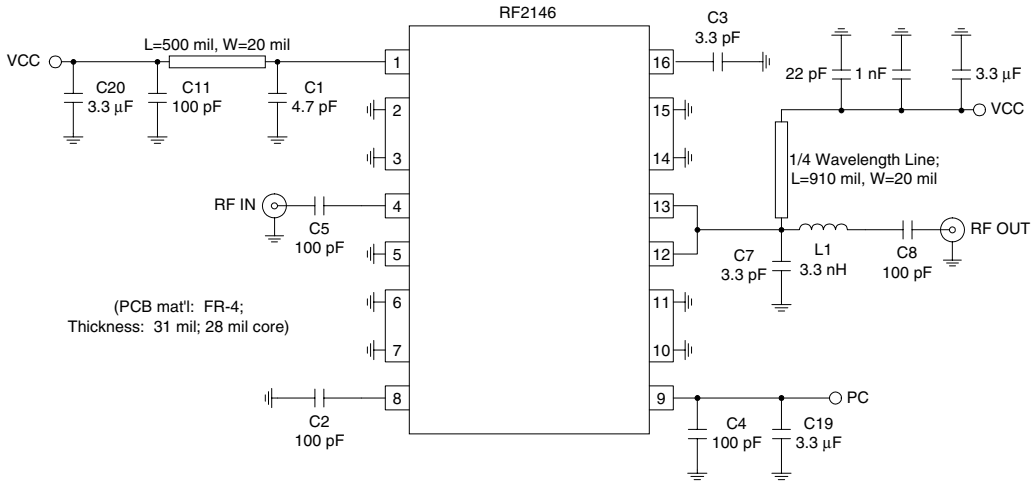
Application Schematic
2150MHz



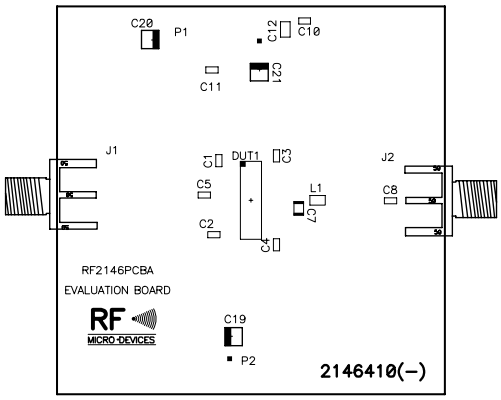
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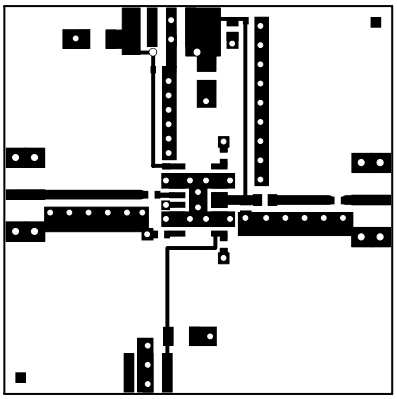
Evaluation Board Schematic

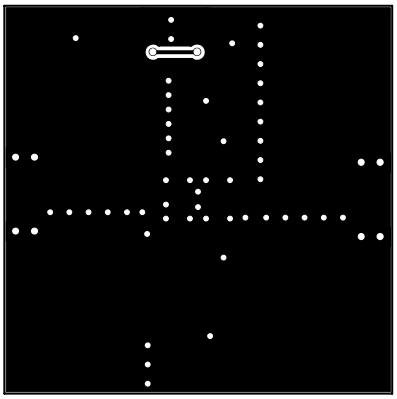
(Download Bill of Materials from www.rfmd.com.)



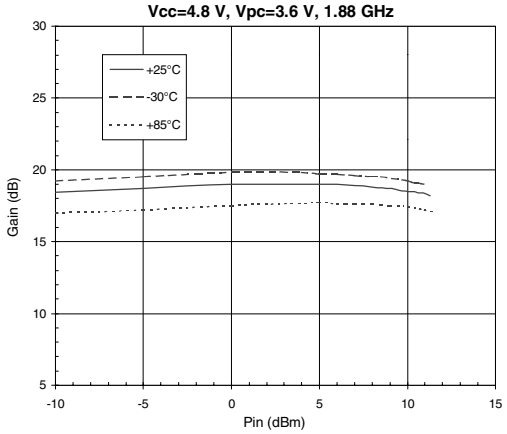
Evaluation Board Layout
2” x 2”



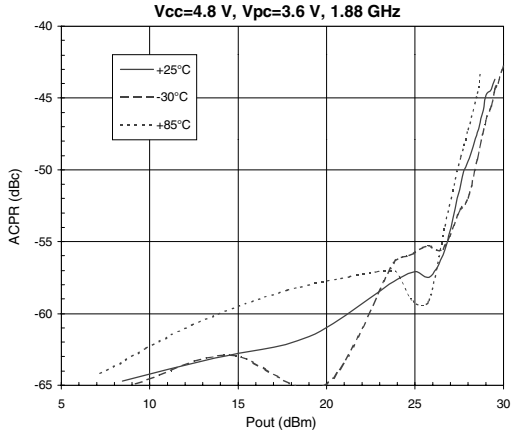




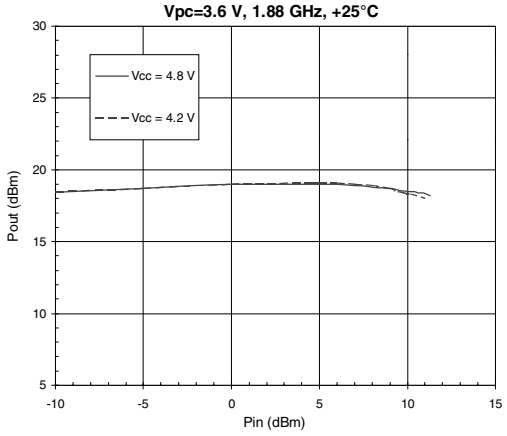
Gain vs. Pin
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



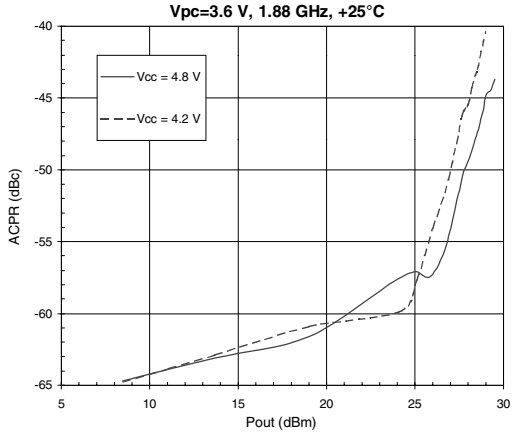
ACPR @ 1.25 MHz Offset vs. Pout
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



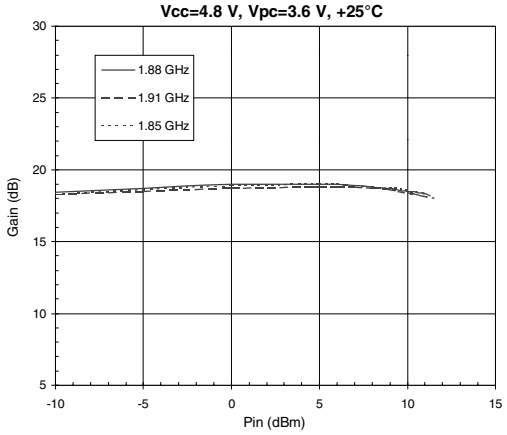
Gain vs. Pin
Vpc=3.6 V, 1.88 GHz, +25°C



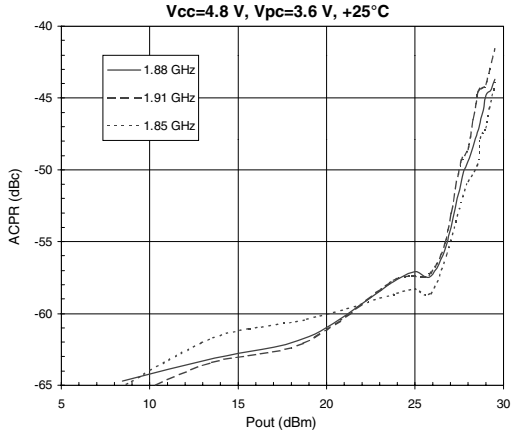
ACPR @ 1.25 MHz Offset vs. Pout
Vpc=3.6 V, 1.88 GHz, +25°C



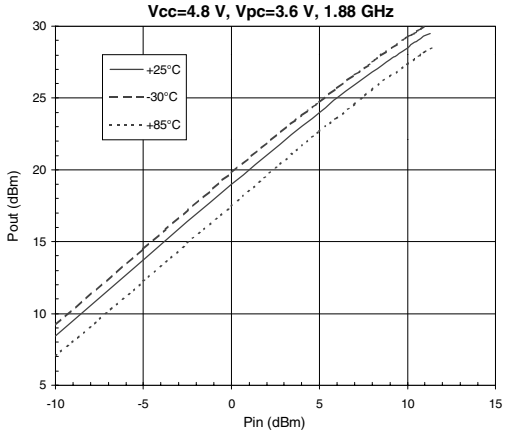
Gain vs. Pin
Vcc=4.8 V, Vpc=3.6 V, +25°C



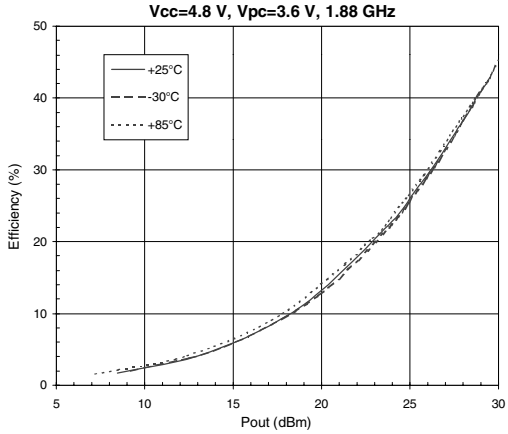
ACPR @ 1.25 MHz Offset vs. Pout
Vcc=4.8 V, Vpc=3.6 V, +25°C



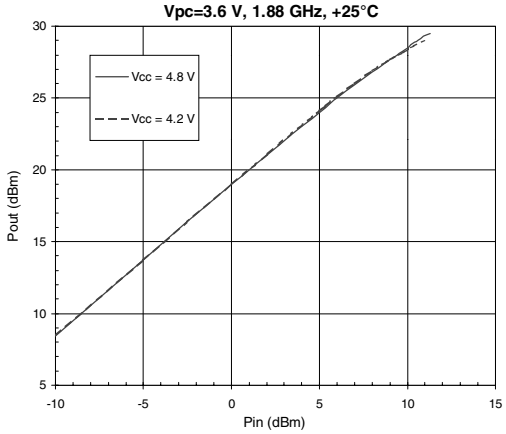
Pout vs. Pin
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



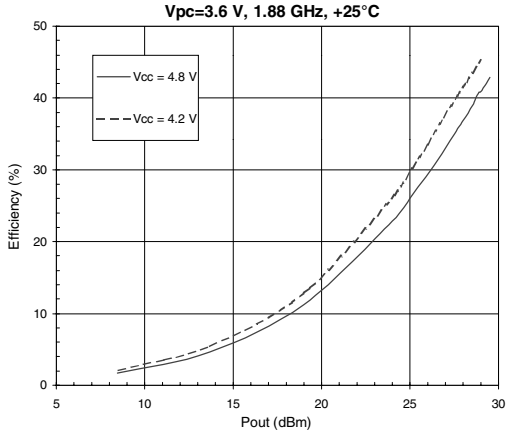
Efficiency vs. Pout
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



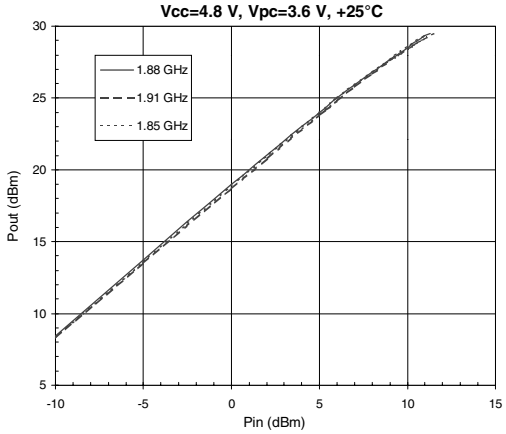
Pout vs. Pin
Vpc=3.6 V, 1.88 GHz, +25°C



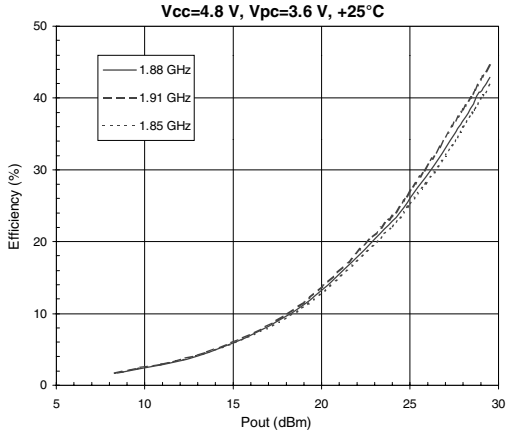
Efficiency vs. Pout
Vpc=3.6 V, 1.88 GHz, +25°C



Pout vs. Pin
Vcc=4.8 V, Vpc=3.6 V, +25°C



Efficiency vs. Pout
Vcc=4.8 V, Vpc=3.6 V, +25°C



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RF MICRO·DEVICES

Preliminary

RF2152

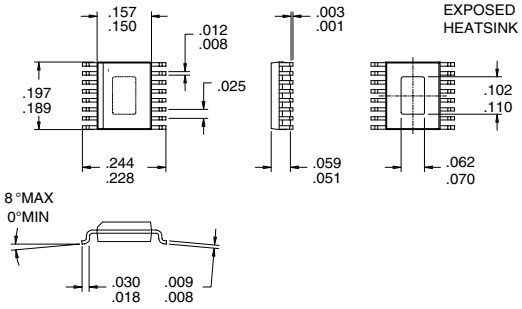
DUAL-MODE CDMA/AMPS OR TDMA/AMPS 3V POWER AMPLIFIER

Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA/TACS Cellular Handsets
- 3V TDMA/AMPS Cellular Handsets
- Spread Spectrum Systems
- CDPD Portable Data Cards
- Portable Battery-Powered Equipment

Product Description

The RF2152 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 950MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The package is a PSSOP-16 with backside ground.

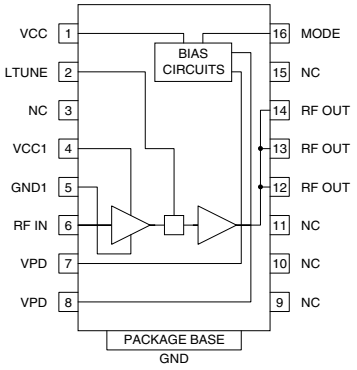


Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: PSSOP-16



Functional Block Diagram

Features

- Single 3V Supply
- 28dBm Linear Output Power
- 30dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 960MHz Operation

Ordering Information

RF2152	Dual-Mode CDMA/AMPS or TDMA/AMPS 3V Power Amplifier
RF2152 PCBA-N	Fully Assembled Evaluation Board 824-849MHz
RF2152 PCBA-J	Fully Assembled Evaluation Board 877-924MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+5.2	V_{DC}
DC Supply Current	1.0	A
Mode Voltage (V_{MODE})	+3.0	V_{DC}
Control Voltage (V_{PD})	+3.0	V_{DC}
Input RF Power	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC LEVEL 5	

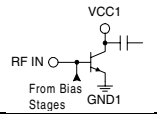
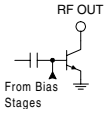
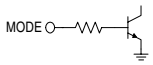
Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

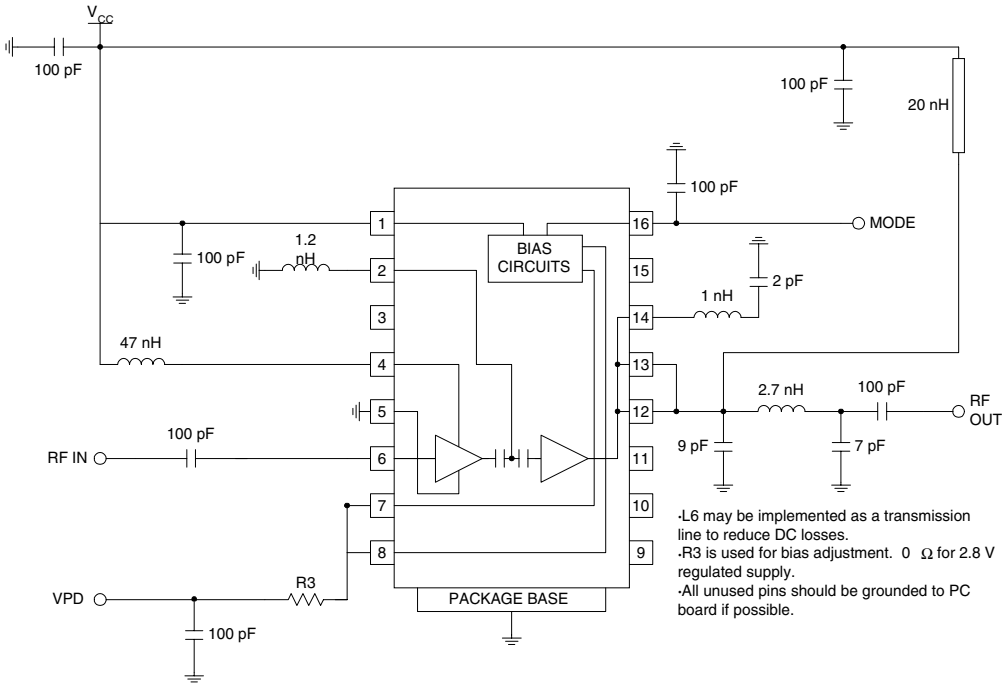
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, V_{PD}=2.8V, Freq=824MHz to 849MHz, unless otherwise specified
Usable Frequency Range	800		960	MHz	
Typical Frequency Range		824-849 877-925		MHz MHz	
Linear Gain	28	30	33	dB	Pout=28dBm
Second Harmonic (including second harmonic trap)	-32	-38	-42	dBc	
Max CW Output Power	31	31.5	32	dBm	Tuned for CDMA
Total Efficiency (AMPS mode)	40	45	55	%	
Maximum Linear Output Power (CDMA Modulation)	28	28.5	29	dBm	Tuned for CDMA
Total Linear Efficiency	30	35	38	%	
Adjacent Channel Power Rejection	-44	-46	-50	dBc	ACPR@885kHz
Adjacent Channel Power Rejection	-56	-58	-62	dBc	ACPR@1980kHz
Input VSWR		< 2:1			
Output Load VSWR			10:1		No oscillations
Noise Figure	5.9	6.0	6.1	dB	V_{CC}=3.4V
Noise Power P_{OUT}=15dBm P_{OUT}=28dBm P_{OUT}=31dBm		86.5 89.3 92.3		dBm dBm dBm	V_{CC}=3.4V; 30KHz BW; RX Band NP measured from TX center band to RX center band
Power Supply					
Power Supply Voltage	3.0	3.4	5.2	V	
Idle current		90		mA	MODE = low Pin 16=Ground AMPS/Low Power CDMA Modes
Idle current		200		mA	MODE = high Pin 16=2.8V High Power CDMA Mode (Pout>20dBm)
V_{PD} current		10		mA	Pins7,8, Vpd=2.8V (Pin 7 typ. not connected, I=5mA for Pin 8)
Turn On/Off time			<100	ns	
Total Current (Power down)			10	µA	V_{PD} = low
V_{PD} "Low" Voltage		0	0.2	V	
V_{PD} "High" Voltage	2.7	2.8	2.9	V	
MODE "High" Voltage	2.1	2.8	2.9		
MODE "Low" Voltage		0	0.5		

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Pin	Function	Description	Interface Schematic
1	VCC	Power supply for input bias circuitry. A 100 pF high frequency bypass capacitor is recommended.	
2	LTUNE	Interstage tuning. This pin will connect to a shunt inductor used for interstage tuning. For 824MHz to 849MHz a 1.5nH discrete inductor is used; for 877MHz to 925MHz a shorted transmission line presenting 0.7 nH of inductance or discrete inductor may be used. This inductor should be placed as close to the pin as possible.	
3	NC	No connection. Grounding pin is recommended.	
4	VCC1	Power supply for stage 1. V_{CC} should be fed through a 25nH or greater inductor with a decoupling capacitor on the V_{CC} side.	See pin 6.
5	GND1	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact.	See pin 6.
6	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
7	VPD	Power Down control. When this pin is “low”, all circuits are shut off. When this pin is 2.8 volts, all circuits are operating normally. V_{PD} requires a regulated 2.8 V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8 V. A 100 pF high frequency bypass capacitor is recommended.	
8	VPD	Connect to pin 7.	
9	NC	No connection. Grounding pin is recommended.	
10	NC	No connection. Grounding pin is recommended.	
11	NC	No connection. Grounding pin is recommended.	
12	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details. The first shunt cap of the matching circuit should be placed as close to the pin as possible.	
13	RF OUT	Same as pin 12.	See pin 12.
14	RF OUT	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with a shunt capacitor at $2f_0$ is connected to this pin.	See pin 12.
15	NC	No connection. Grounding pin is recommended.	
16	MODE	The mode pin allows higher efficiency operation in AMPS and low power CDMA modes. MODE should be set “low” for highest efficiency in AMPS/TACS and in low power (<+15 dBm) CDMA operation. MODE should be set “high” for best linearity in high power CDMA operation.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

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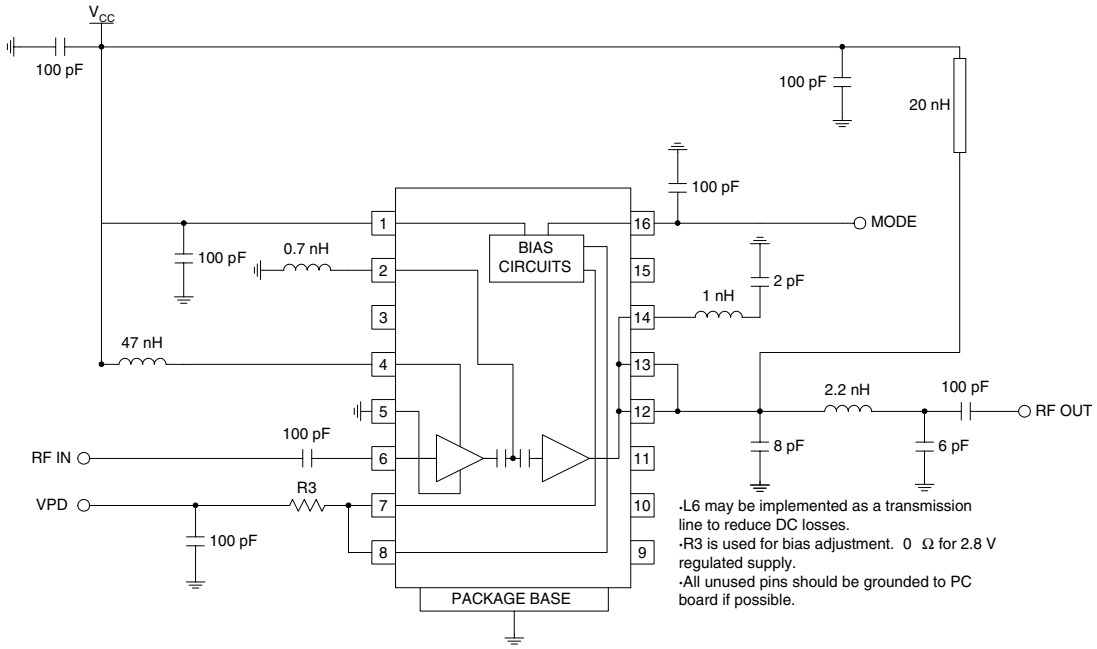
Application Schematic
824MHz to 849MHz



- L6 may be implemented as a transmission line to reduce DC losses.
- R3 is used for bias adjustment. 0 Ω for 2.8 V regulated supply.
- All unused pins should be grounded to PC board if possible.

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Application Schematic
877MHz to 924MHz

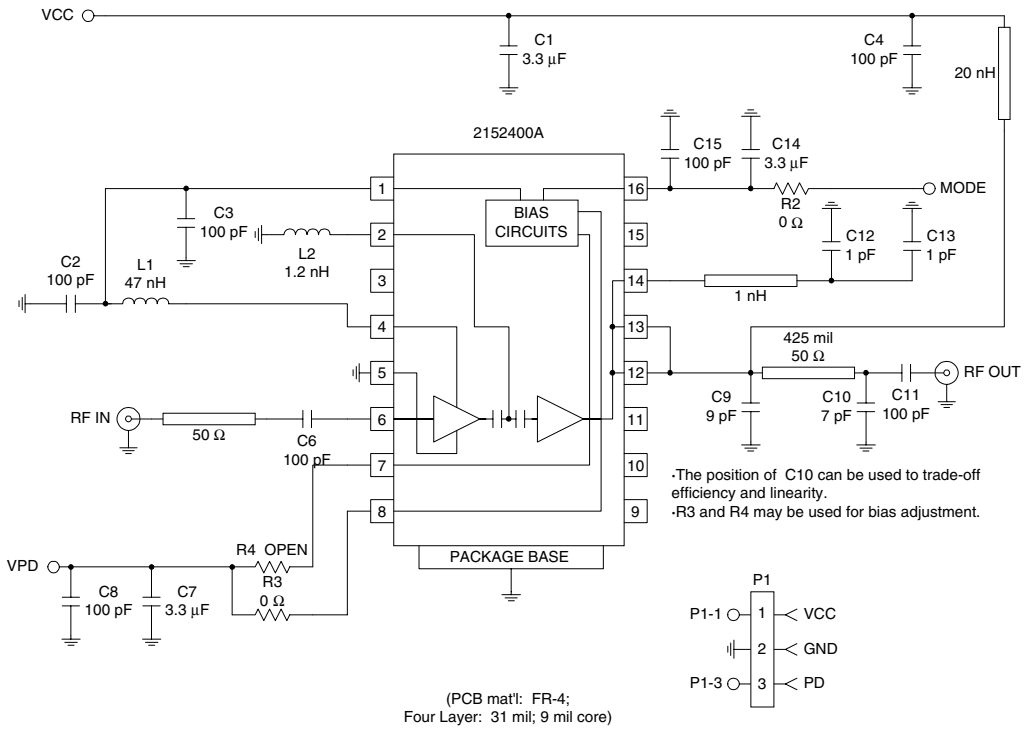


- L6 may be implemented as a transmission line to reduce DC losses.
- R3 is used for bias adjustment. 0 Ω for 2.8 V regulated supply.
- All unused pins should be grounded to PC board if possible.

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Evaluation Board Schematic
824MHz to 849MHz

(Download Bill of Materials from www.rfmd.com.)



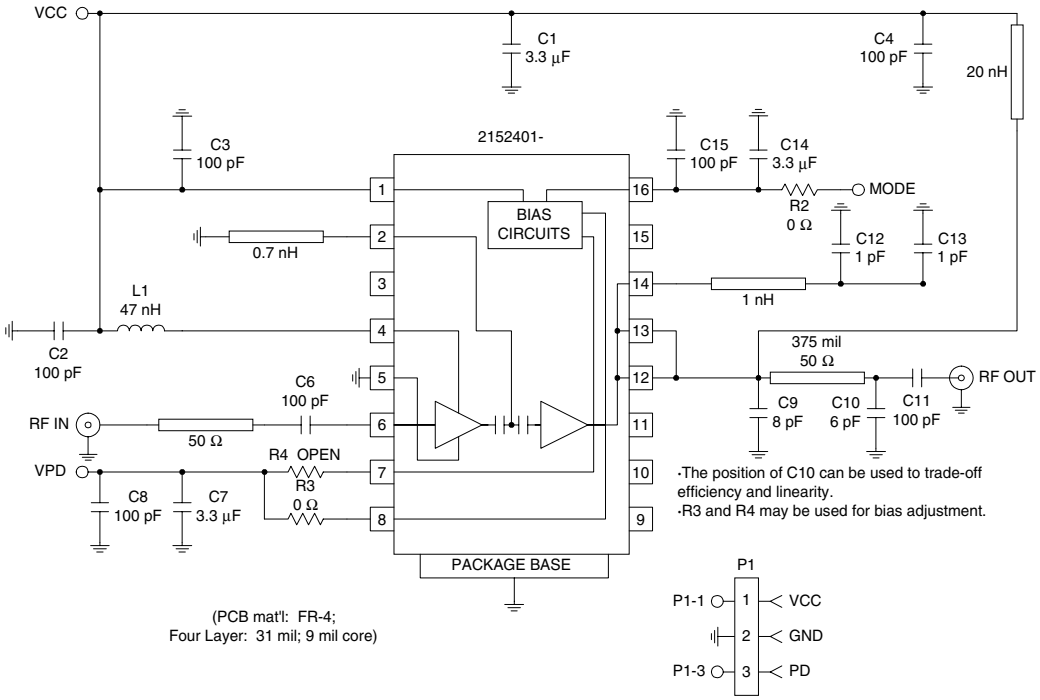
·The position of C10 can be used to trade-off efficiency and linearity.
·R3 and R4 may be used for bias adjustment.

(PCB mat'l: FR-4;
Four Layer: 31 mil; 9 mil core)

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Evaluation Board Schematic
877MHz to 924MHz

(Download Bill of Materials from www.rfmd.com.)

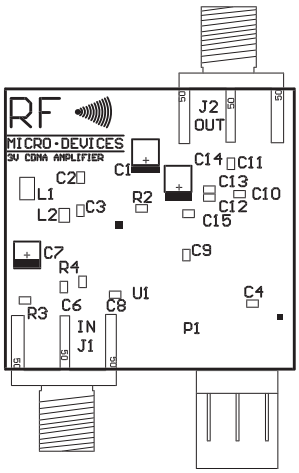


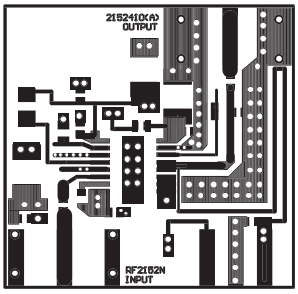
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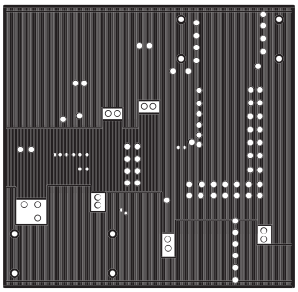
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Evaluation Board Layout 824MHz to 849MHz
1" x 1"

Board Thickness 0.034", Board Material FR-4, Multi-Layer

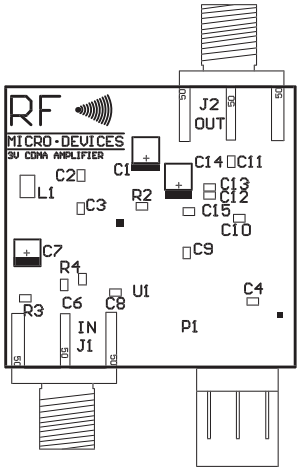


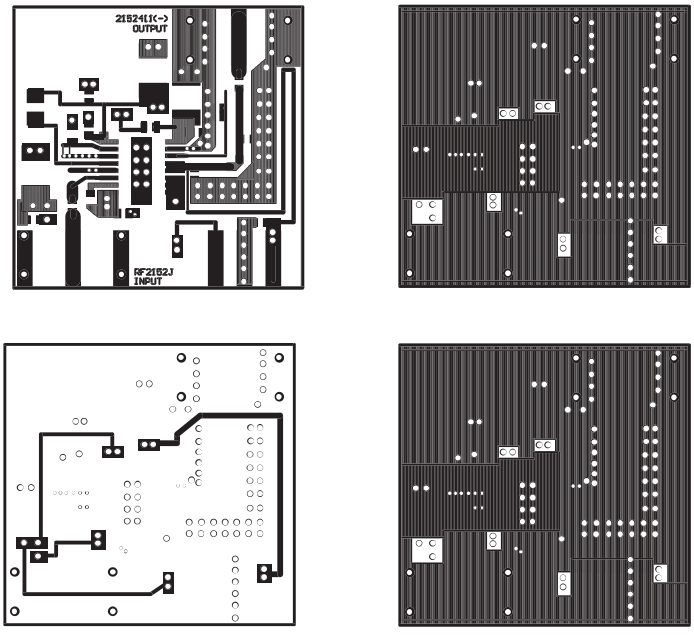




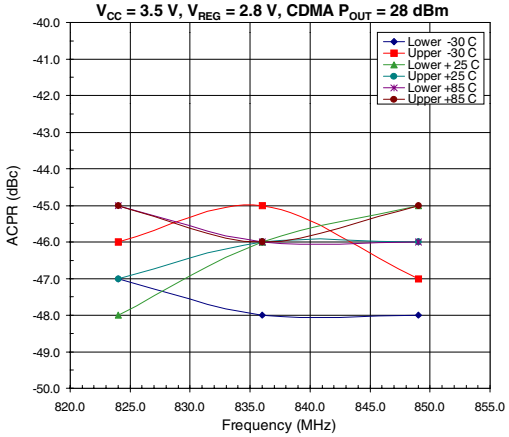
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Evaluation Board Layout 877MHz to 924MHz
1" x 1"

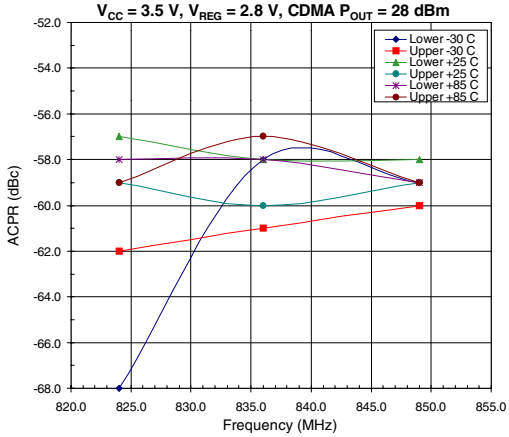




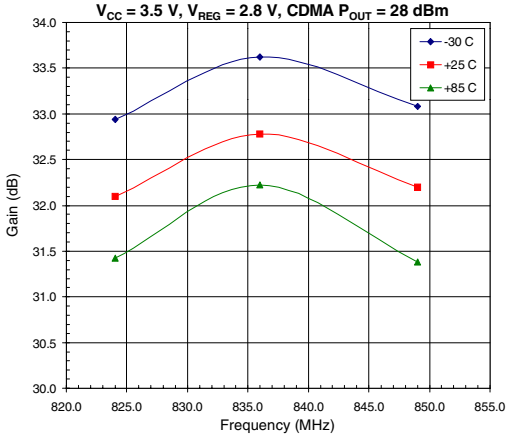
ACPR (@885 kHz offset) versus Frequency
V_{CC} = 3.5 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



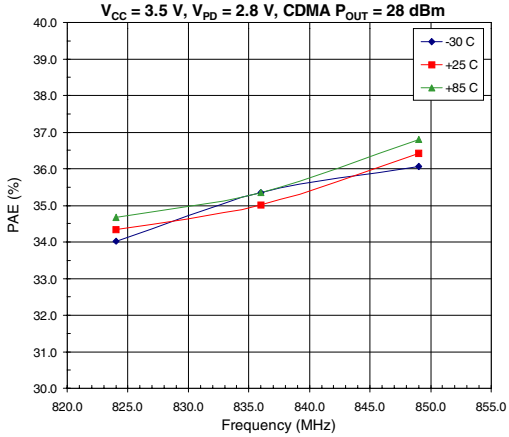
ACPR (@1980 kHz offset) versus Frequency
V_{CC} = 3.5 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



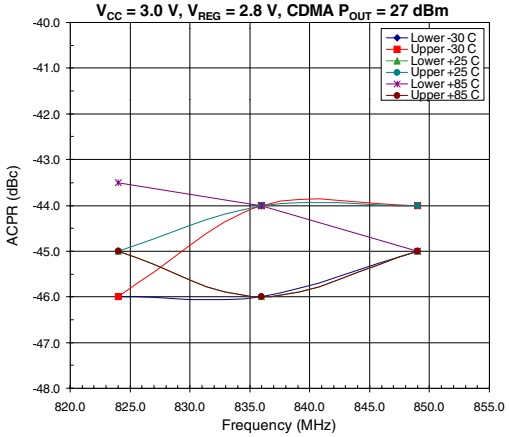
Gain versus Frequency
V_{CC} = 3.5 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



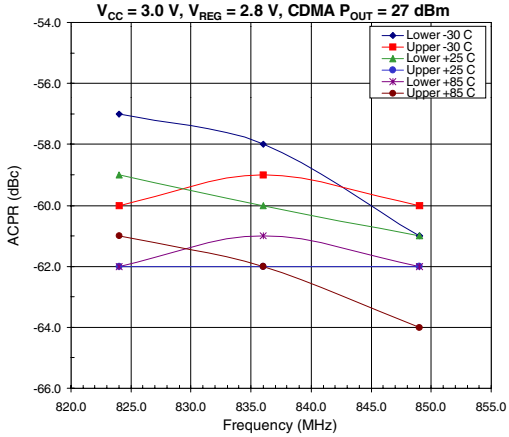
PAE versus Frequency
V_{CC} = 3.5 V, V_{PD} = 2.8 V, CDMA P_{OUT} = 28 dBm



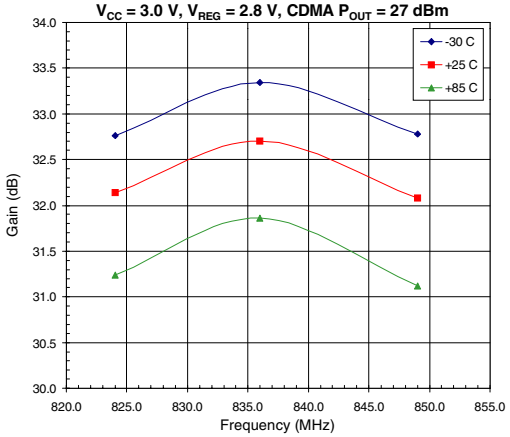
ACPR (@885 kHz offset) versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



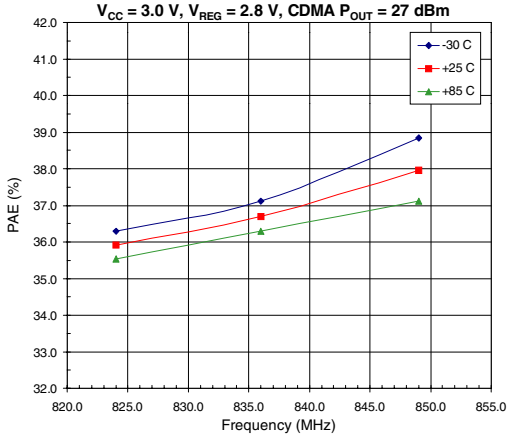
ACPR (@1908 kHz offset) versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



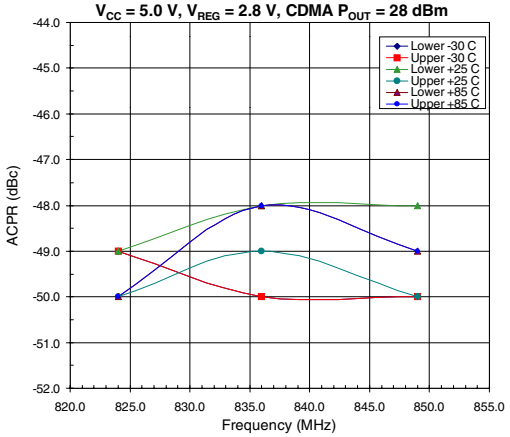
Gain versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



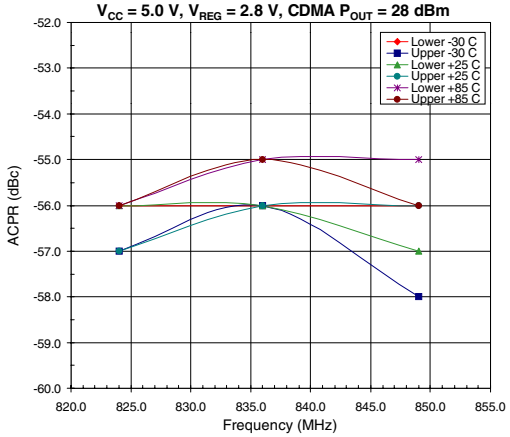
PAE versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



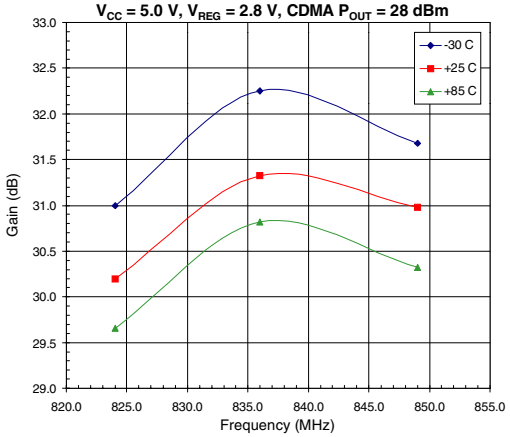
ACPR (@885 kHz offset) versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



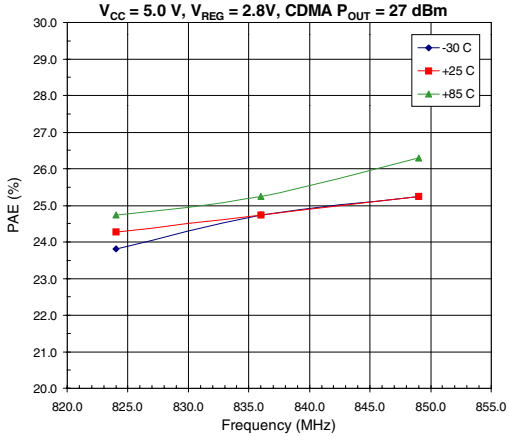
ACPR (@1908 kHz offset) versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm

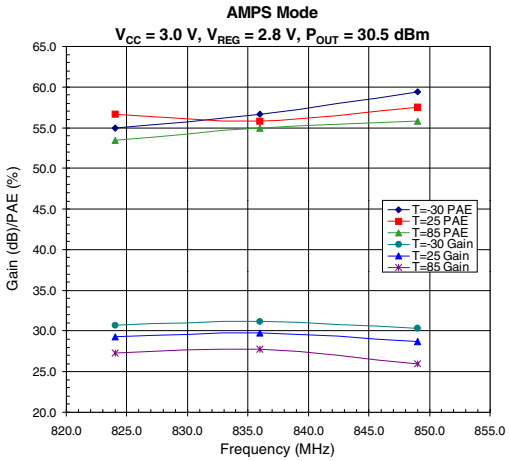


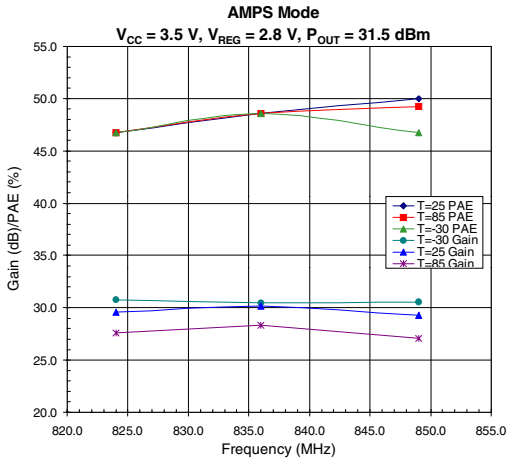
Gain versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm

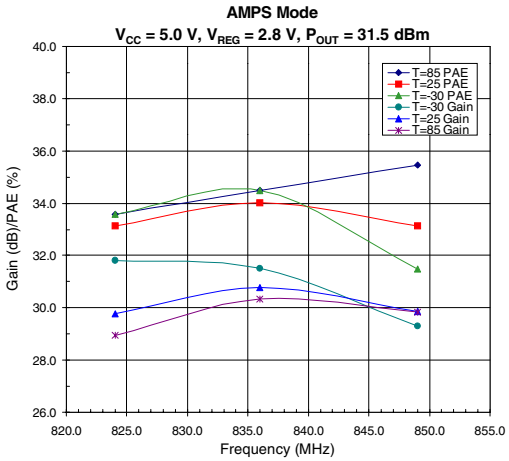


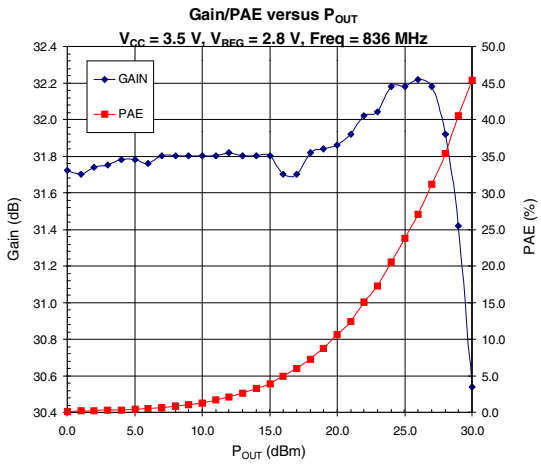
PAE versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8V, CDMA P_{OUT} = 27 dBm




AMPS Mode
VCC = 3.0 V, VREG = 2.8 V, POUT = 30.5 dBm
Gain (dB)/PAE (%)
Frequency (MHz)
T=-30 PAE
T=25 PAE
T=85 PAE
T=-30 Gain
T=25 Gain
T=85 Gain


AMPS Mode
VCC = 3.5 V, VREG = 2.8 V, POUT = 31.5 dBm
Gain (dB)/PAE (%)
Frequency (MHz)
T=25 PAE
T=85 PAE
T=-30 PAE
T=-30 Gain
T=25 Gain
T=85 Gain


AMPS Mode
VCC = 5.0 V, VREG = 2.8 V, POUT = 31.5 dBm
Gain (dB)/PAE (%)
Frequency (MHz)
T=85 PAE
T=25 PAE
T=-30 PAE
T=-30 Gain
T=25 Gain
T=85 Gain


Gain/PAE versus POUT
VCC = 3.5 V, VREG = 2.8 V, Freq = 836 MHz
Gain (dB)
PAE (%)
POUT (dBm)
GAIN
PAE

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RF2153

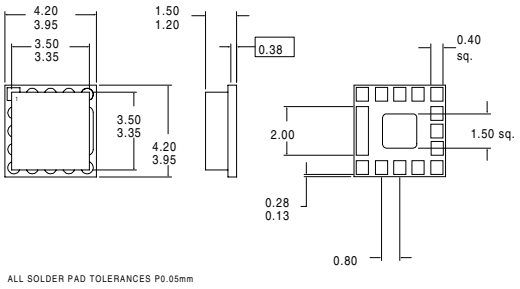
CDMA/TDMA/PACS 1900MHZ 3V POWER AMPLIFIER

Typical Applications

- PACS Handsets and Base Stations
- 3V 1850-1910MHz CDMA PCS Handsets
- 3V 1750-1780MHz CDMA PCS Handsets
- 3V TDMA PCS Handsets
- Spread Spectrum Systems
- Commercial and Consumer Systems

Product Description

The RF2153 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 3V CDMA and TDMA hand-held digital equipment, spread spectrum systems, and other applications in the 1750MHz to 1910MHz band. The device is packaged in a compact 4mmx4mm (LCC). The device's frequency response can be optimized for linear performance in the 1750MHz to 1910MHz band.



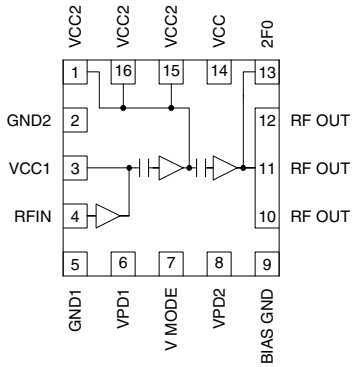
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MP16KO1A

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 30dB Linear Gain
- 33% Linear Efficiency CDMA
- 40% Linear Efficiency TDMA
- On-board Power Down Mode



Functional Block Diagram

Ordering Information

RF2153	CDMA/TDMA/PACS 1900MHz 3V Power Amplifier
RF2153 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2153

Absolute Maximum Ratings

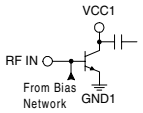
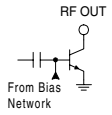
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+4.5	V_{DC}
Mode Voltage (V_{MODE})	+3.5	V_{DC}
Control Voltage (V_{PD})	+3.5	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +85	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

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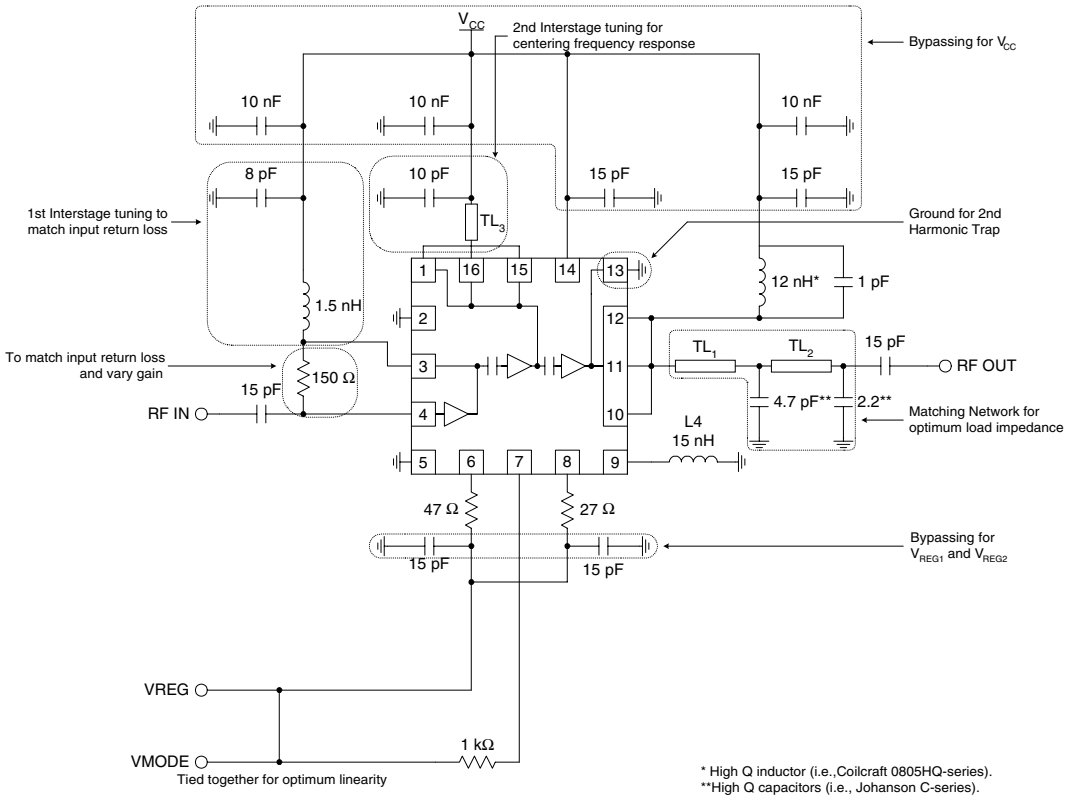
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall - CDMA					T=25°C, V_{CC}=3.4V unless otherwise specified
Usable Frequency Range	1750		1910	MHz	
Typical Frequency Range		1750-1780		MHz	Output Matching Network Tune
		1850-1910		MHz	Output Matching Network Tune
Small Signal Gain	30	32	34	dB	V_{MODE}=Low 0V to 0.5V
Linear Gain	28	30		dB	V_{MODE}=High 2.5V to 3V
					P_{OUT}=29dBm, V_{CC}=3.4V, V_{REG}=2.8V
Second Harmonic (including second harmonic trap)		-35		dBc	
Third Harmonic		-40		dBc	
Fourth Harmonic		-45		dBc	
Minimum Linear Output Power (CDMA or TDMA Modulation)	29			dBm	
Idle Current		100		mA	V_{MODE}=>2.5V
CDMA Linear Efficiency	30	33			P_{OUT}=29dBm, V_{CC}=3.4V, V_{REG}=2.8V
CDMA Adjacent Channel Power Rejection @ 1.25MHz		-46	-44	dBc	P_{OUT}=29dBm, V_{CC}=3.4V, V_{REG}=2.8V
Minimum Linear Output Power (CDMA Modulation)	28	+29		dBm	V_{CC}=3.0V, V_{REG}=2.8V
Input VSWR		< 2:1			
Output Load VSWR	5:1				
Overall - TDMA					T=25°C, V_{CC}=3.4V unless otherwise specified
Idle Current		250	500	mA	V_{MODE}=0V to 0.5V
TDMA Linear Efficiency	30	40		%	P_{OUT}=30dBm, V_{CC}=3.4V, V_{REG}=2.8V
TDMA ACP @ 30kHz		-29	-28	dBc	P_{OUT}=30dBm
TDMA ALT @ 60kHz		-49	-48	dBc	P_{OUT}=30dBm
Power Supply					
Power Supply Voltage	3.0	3.4	4.5	V	
V_{PD} Current		10	15	mA	Total pins 7 and 8
Turn On/Off time			100	ns	
Total Current (Power down)			10	µA	V_{PD} = low
V_{PD} "Low" Voltage		0	0.2	V	
V_{PD} "High" Voltage	2.7	2.8	2.9	V	
MODE "High" Voltage	2.5	2.8		V	
MODE "Low" Voltage		0	0.5	V	
Stability		3:1			Inband
		20:1			Outband
Spurious		<-60		dBc	
Noise Power		-136		dB/Hz	@ 80MHz offset

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Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for second stage and interstage match. Pins 1, 15 and 16 should be connected by a common trace where the pins contact the printed circuit board.	
2	GND2	Ground for second stage. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact on top metal layer.	
3	VCC1	Power supply for first stage and interstage match. V_{CC} should be fed through a 1.5nH inductor terminated with a 15pF capacitor on the supply side.	See pin 4.
4	RF IN	RF input. An external 15pF series capacitor is required as a DC block and also provides for an input VSWR of <2:1 typical.	
5	GND1	Ground for first stage. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact on top metal layer.	See pin 4.
6	VPD1	Power Down control for first and second stages. When this pin is “low”, all first and second stage circuits are shut off. When this pin is 2.8V, all first stage circuits are operating normally. V_{PD1} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V.	
7	VMODE	For full power operation, MODE is set low. VMODE will reduce the bias current by up to 50% when set HIGH. Large Signal Gain is reduced approximately 1.5dB at 29dBm P_{OUT} and Small Signal Gain is reduced approximately 6dB. An external series resistor is optional to limit the amount of current required by the V_{MODE} pin.	
8	VPD2	Power Down control for the third stage. When this pin is “low”, the third stage circuit is shut off. When this pin is 2.8V, the third stage circuit is operating normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 15pF high frequency bypass capacitor is recommended.	
9	BIAS GND	Requires a 15nH inductor.	
10	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the third stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1850MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	RF OUT	Same as pin 12.	See pin 10.
12	RF OUT	Same as pin 12.	See pin 10.
13	2FO	Second harmonic trap. Keep traces physically short and connect immediately to ground plane. This ground should be isolated from backside ground contact.	
14	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
15	VCC2	Same as pin 1.	
16	VCC2	Same as pin 1.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

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Application Schematic
US - CDMA

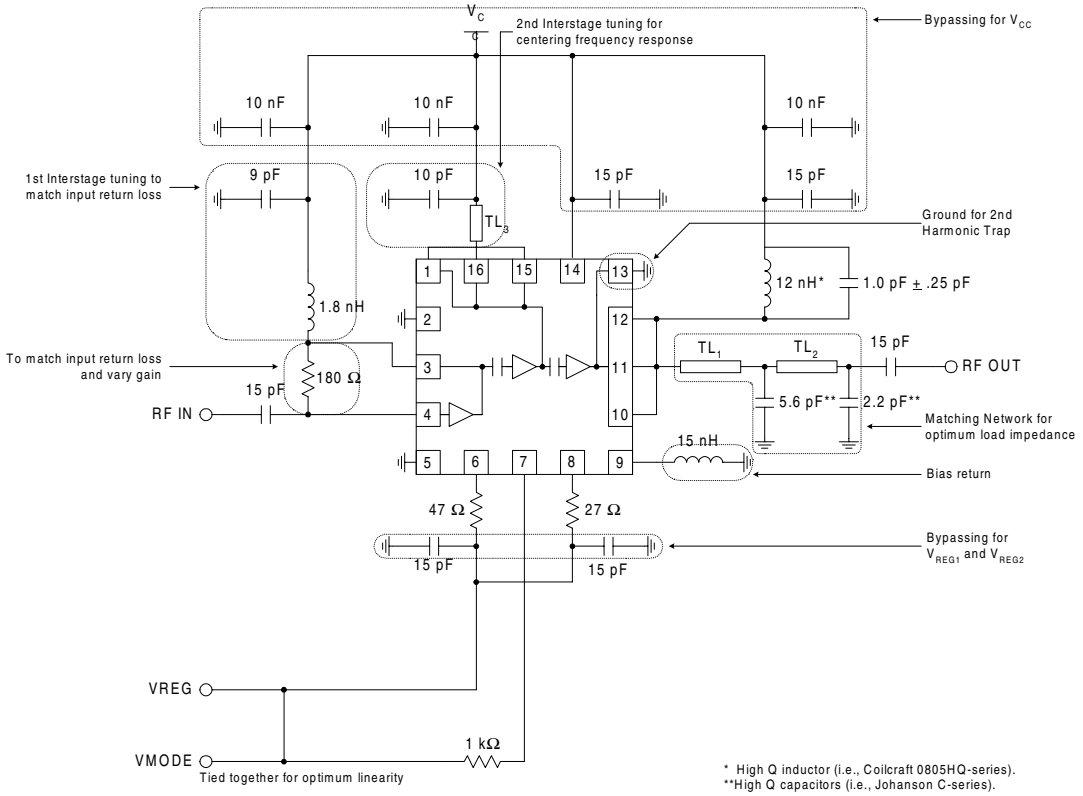


* High Q inductor (i.e.,Coilcraft 0805HQ-series).
**High Q capacitors (i.e., Johanson C-series).

Transmission Line Length	TL_1	TL_2	TL_3
CDMA (US)	20 mils	100 mils	20 mils

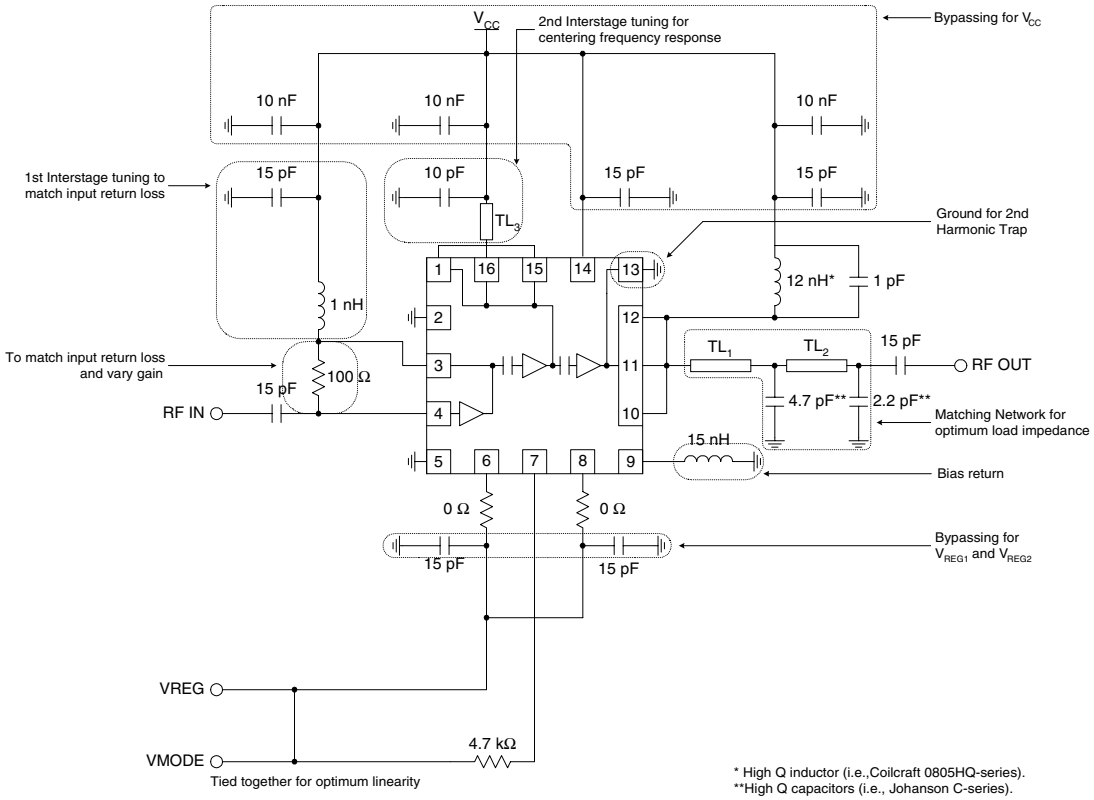
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Application Schematic
Korea - CDMA



Transmission Line Length	TL_1	TL_2	TL_3
CDMA (Korea)	30 mils	100 mils	30 mils

Application Schematic
US - TDMA

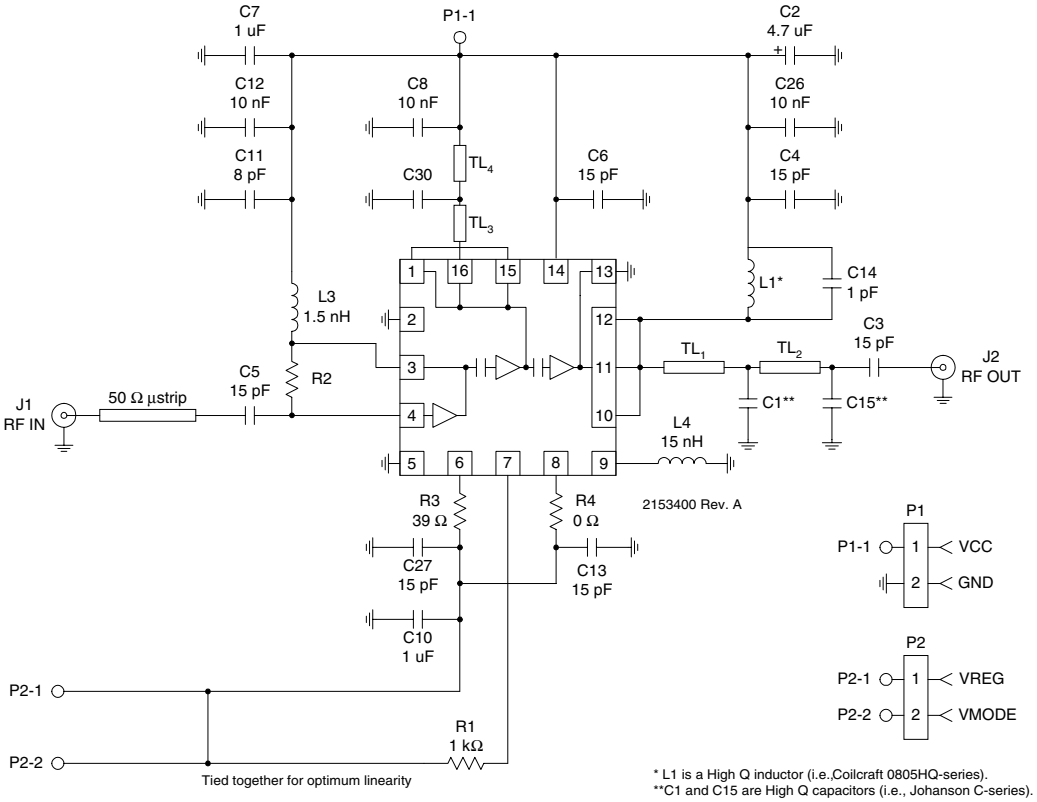


* High Q inductor (i.e.,Coilcraft 0805HQ-series).
**High Q capacitors (i.e., Johanson C-series).

Transmission Line Length	TL_1	TL_2	TL_3
TDMA (US)	20 mils	160 mils	10 mils

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Evaluation Board Schematic
US - CDMA



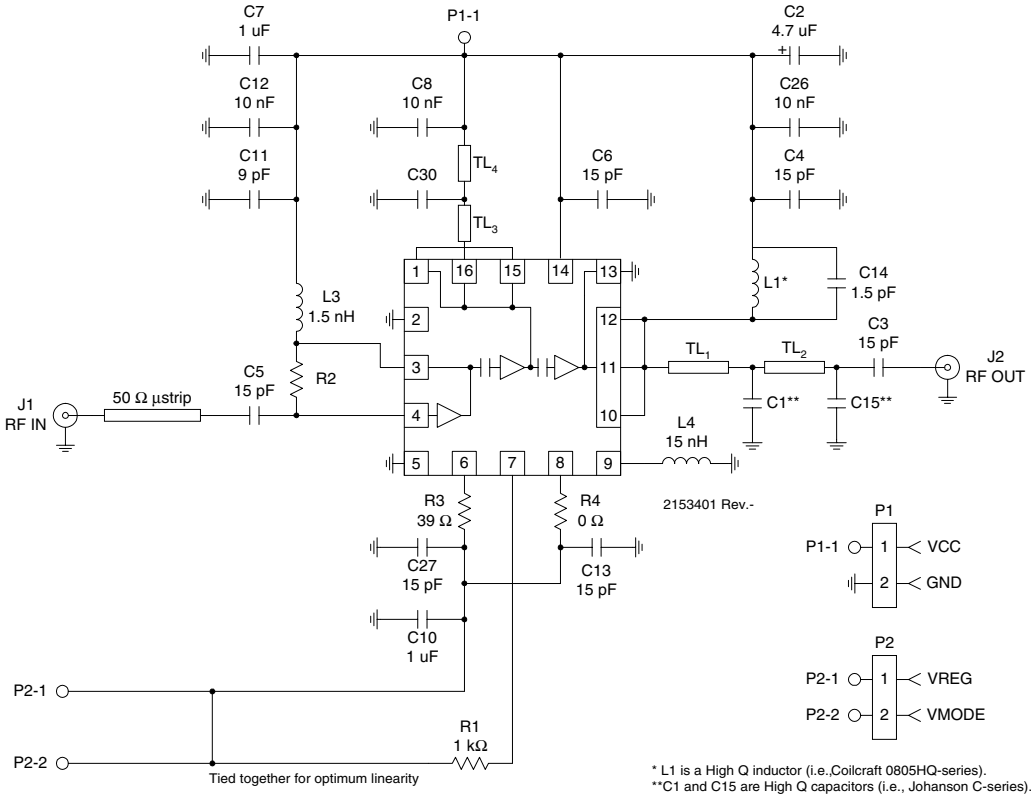
* L1 is a High Q inductor (i.e.,Coilcraft 0805HQ-series).
**C1 and C15 are High Q capacitors (i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C15 (pF)
CDMA (US)	150	10	4.7	12	2.2

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (US)	20 mils	100 mils	20 mils	100 mils or ≥ 2.7 nH inductor

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Evaluation Board Schematic
Korea - CDMA



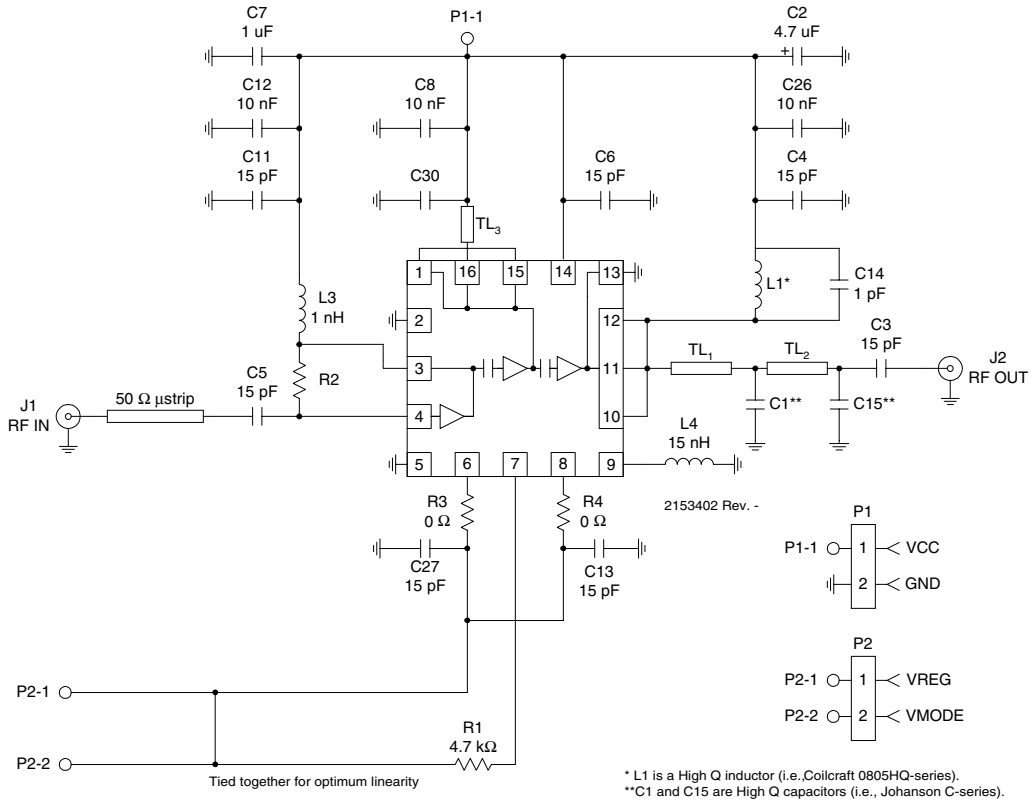
* L1 is a High Q inductor (i.e.,Coilcraft 0805HQ-series).
**C1 and C15 are High Q capacitors (i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C15 (pF)
CDMA (Korea)	180	11	5.6	12	2.2

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (Korea)	30 mils	100 mils	30 mils	100 mils or ≥ 2.7 nH inductor

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Evaluation Board Schematic
US - TDMA



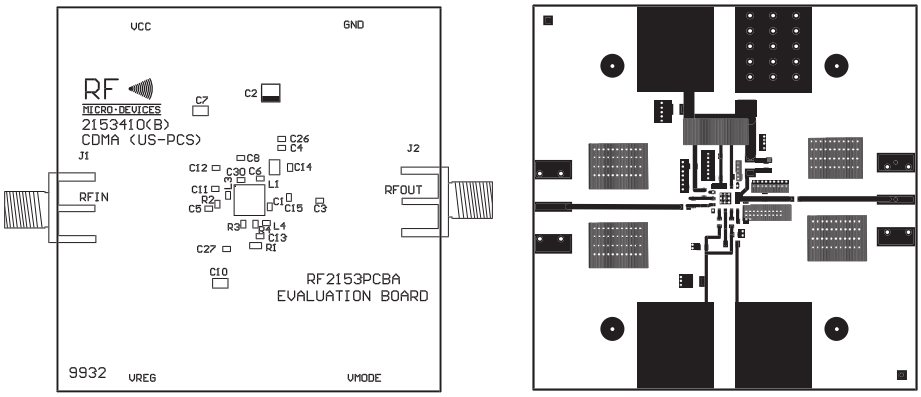
* L1 is a High Q inductor (i.e.,Coilcraft 0805HQ-series).
**C1 and C15 are High Q capacitors (i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C15 (pF)
TDMA (US)	100	10	4.7	12	2.2

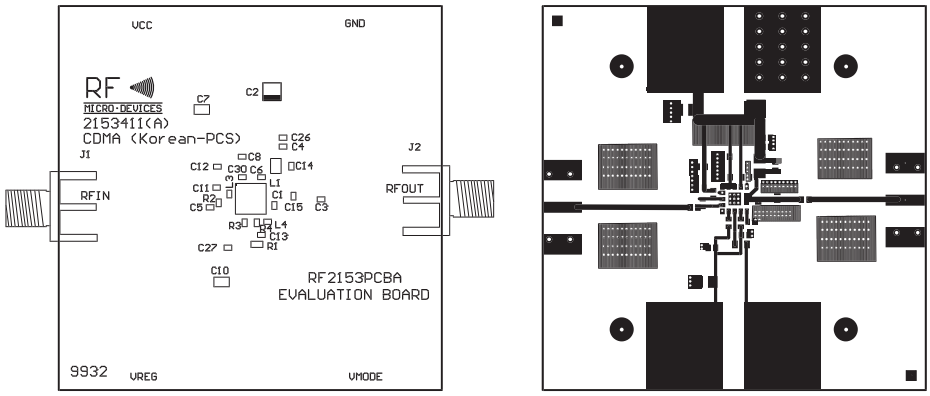
Transmission Line Length	TL_1	TL_2	TL_3
TDMA (US)	20 mils	160 mils	10 mils

Evaluation Board Layout
US - CDMA
Board Size 2.0" x 2.0"

Board Thickness 0.031", Board Material FR-4

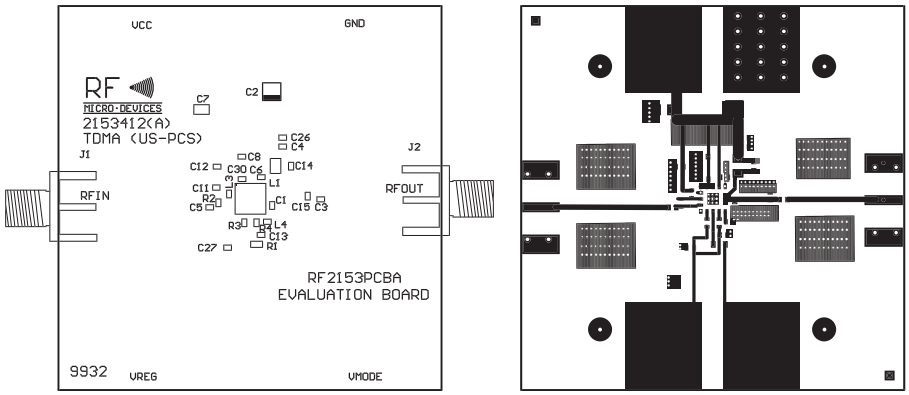


Evaluation Board Layout
Korea - CDMA



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Evaluation Board Layout
US - TDMA



RF2153

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RF2155

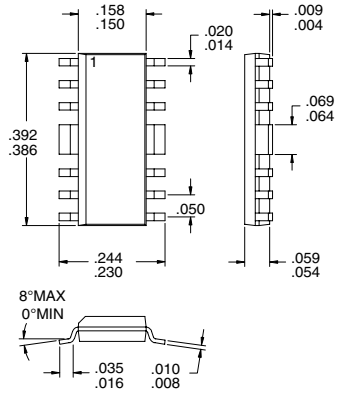
3V PROGRAMMABLE GAIN POWER AMPLIFIER

Typical Applications

- Analog Communication Systems
- 900MHz Spread Spectrum Systems
- 400MHz Industrial Radios
- Driver Stage for Higher Power Applications
- 3V Applications

Product Description

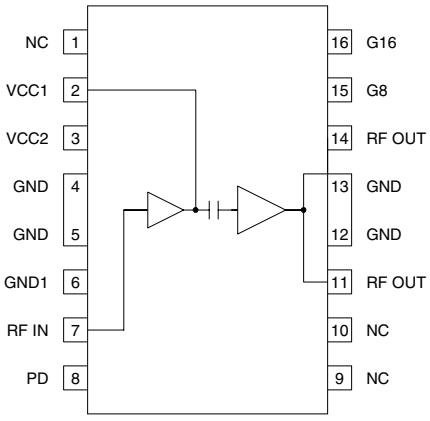
The RF2155 is a 3V medium power programmable gain amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in analog cellular phone transmitters or ISM applications operating at 915MHz. The device is self-contained with the exception of the output matching network and power supply feed line. A two-bit digital control provides 4 levels of power control, in 8dB steps.



Package Style: SOP-16 BW

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 500mW CW Output Power
- 31dB Small Signal Gain
- Up to 60% Efficiency
- Digitally Controlled Output Power
- 430MHz to 930MHz Frequency Range

Ordering Information

RF2155	3V Programmable Gain Power Amplifier
RF2155 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2155

Absolute Maximum Ratings

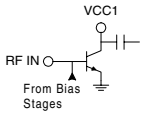
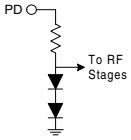
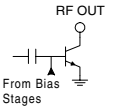
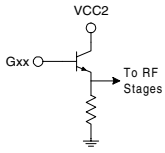
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +3.3	V
DC Supply Current	500	mA
Input RF Power	+10	dBm
Output Load VSWR	10:1	
Ambient Operating Temperature	-30 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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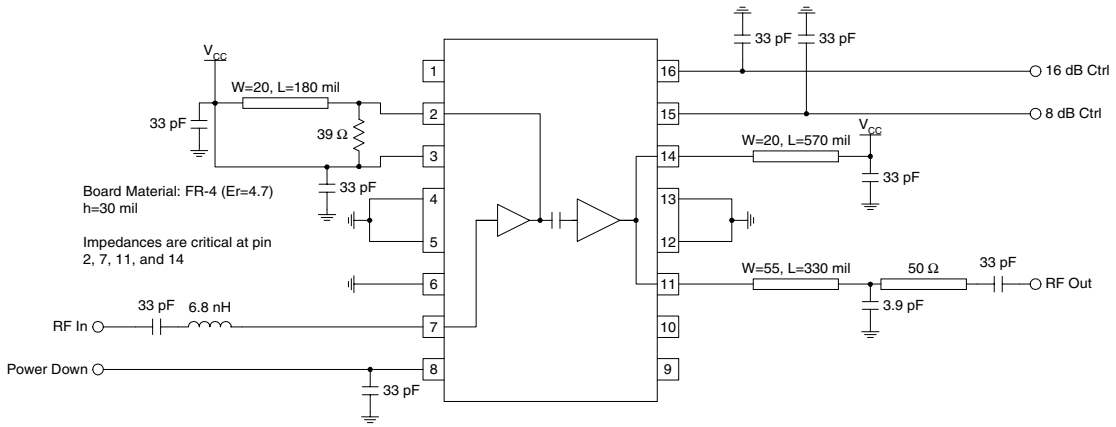
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, V_{PD}=3.0V, Z_{LOAD}=13Ω, P_{IN}=0dBm, Freq=915MHz
Frequency Range		430 to 930		MHz	
Maximum CW Output Power		450		mW	V_{CC}=3.6V
		300		mW	V_{CC}=3.0V
Small Signal Gain		31		dB	
Second Harmonic		-30		dBc	Without external second harmonic trap
Third Harmonic		-40		dBc	
Fourth Harmonic		-36		dBc	
Input VSWR		2:1			All gain settings
CW Efficiency	50	56		%	G16="high", G8="high", P_{IN}=0dBm
Output Load VSWR	6:1				Spurious<-60dBc
Power Control					
Power Down "ON"	2.7	2.8	3.0	V	Voltage supplied to the input
Power Down "OFF"	0	0.5	0.8	V	Voltage supplied to the input
PD Input Current		3.7	5.0	mA	Only in "ON" state
G16, G8 "ON"	2.2	2.5	3.0	V	Voltage supplied to the input
G16, G8 "OFF"	0	0.3	0.5	V	Voltage supplied to the input
G16, G8 Input Current	0.8	1.0	1.6	mA	Only in "ON" state
Output Power	+25.5	+26.5	+28.0	dBm	G16="high", G8="high", P_{IN}=0dBm
	+16.0	+18.5	+21.0	dBm	G16="high", G8="low", P_{IN}=0dBm
	+8.0	+10.5	+13.0	dBm	G16="low", G8="high", P_{IN}=0dBm
	-1.0	+1.5	+4.0	dBm	G16="low", G8="low", P_{IN}=0dBm
Turn On/Off Time			100	ns	
Power Supply					
Power Supply Voltage		3.6		V	Specifications
	3.0		5.0	V	Operating limits
Power Supply Current		225	300	mA	G16="high", G8="high", P_{IN}=0dBm
		90	115	mA	G16="high", G8="low", P_{IN}=0dBm
		37	55	mA	G16="low", G8="high", P_{IN}=0dBm
		25	35	mA	G16="low", G8="low", P_{IN}=0dBm
	20	50	110	mA	G16="high", G8="high", No RF In
		1	10	μA	G16="low", G8="low", PD="low"

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Pin	Function	Description	Interface Schematic
1	NC	Not internally connected.	
2	VCC1	Positive supply for the first stage (driver) amplifier. This is an unmatched transistor collector output. This pin should see an inductive path to AC ground (V_{CC} with a UHF bypassing capacitor). This inductance can be achieved with a short, thin microstrip line (approximately equivalent to 0.4nH). At lower frequencies, the inductance value should be larger (longer microstrip line) and V_{CC} should be bypassed with a larger bypass capacitor. This inductance forms a matching network with the amplifier stages, setting the amplifier's frequency of maximum gain. An additional 1µF bypass capacitor in parallel with the UHF bypass capacitor is also recommended, but placement of this component is not as critical. A resistor of 39Ω from this pin to pin 3 is necessary to ensure stability under extreme output VSWR conditions.	
3	VCC2	Positive supply for the bias circuits. This pin should be bypassed with a single UHF capacitor, placed as close as possible to the package.	
4	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
5	GND	Same as pin 4.	
6	GND1	Ground return for the first stage; this should be connected to a via very close to the device.	
7	RF IN	Amplifier RF input. This is a 50Ω RF input port to the amplifier. To improve the input match over all four gain control settings, an input inductor of 6.8nH should be added. The amplifier does not contain internal DC blocking and, therefore, should be externally DC blocked before connecting to any device which has DC present or which contains a DC path to ground. A series UHF capacitor is recommended for the DC blocking.	See pin 2.
8	PD	Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at 3V the device will be in full power mode delivering maximum available gain and output power capability. This pin should not, in any circumstance, be higher than 3.3V. This pin should also have an external UHF and HF bypassing capacitor.	
9	NC	Not internally connected.	
10	NC	Not internally connected.	
11	RF OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 11 and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through one of these pins. Typically, pin 14 is used to supply bias. A transmission line of approximately 500 mils length, followed by a bypass capacitor, is adequate. This pin can also be used to create a second harmonic trap. A UHF and large tantalum (1µF) capacitor should be placed on the power supply side of the bias inductor. Pin 11 should be used for the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC blocking at the output.	
12	GND	Same as pin 4.	
13	GND	Same as pin 4.	
14	RF OUT	Same as pin 11.	
15	G8	RF output power gain control 8dB bit (see specification table for logic). The control voltage at this pin should never exceed 3.3V and a logic high should be at least 2.7V. This pin should also have an external UHF bypassing capacitor.	

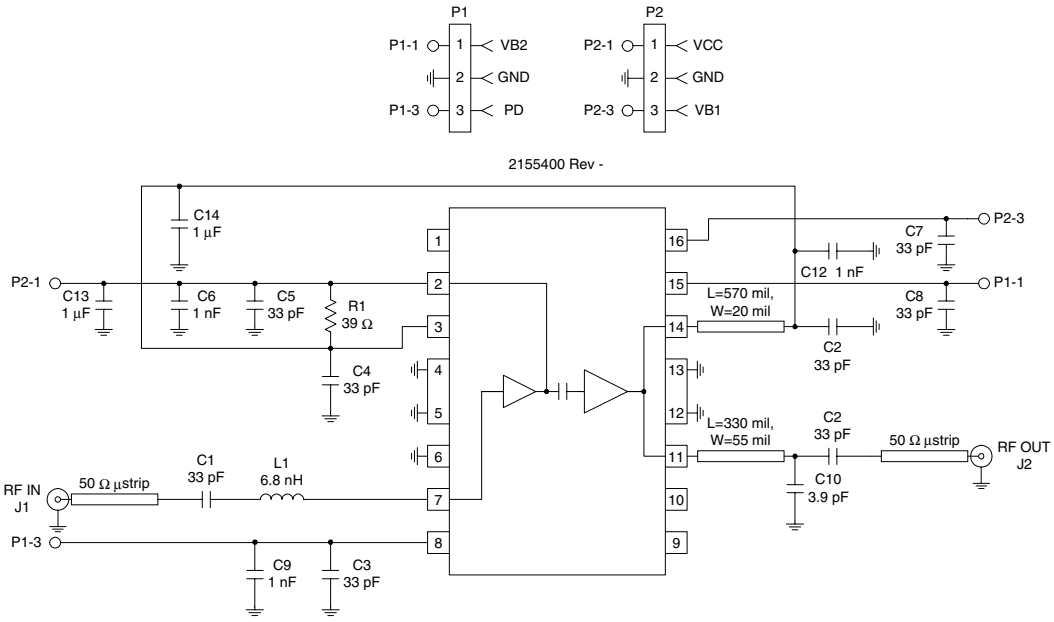
Pin	Function	Description	Interface Schematic
16	G16	RF output power gain control 16 dB bit (see specification table for logic). The control voltage at this pin should never exceed 3.3V and a logic high should be at least 2.7V. This pin should also have an external UHF bypassing capacitor.	Same as pin 15.

Application Schematic
915 MHz

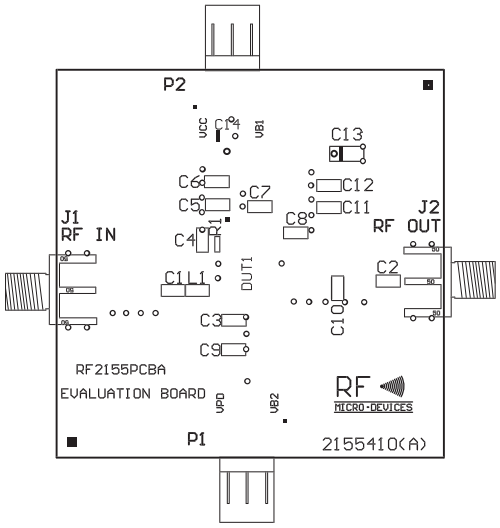


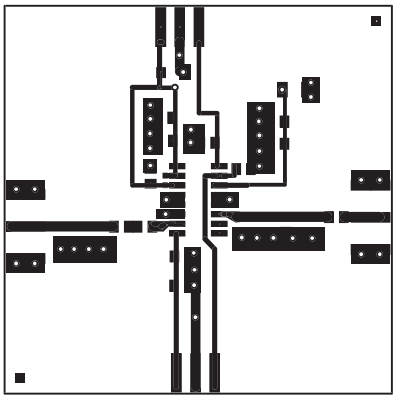
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

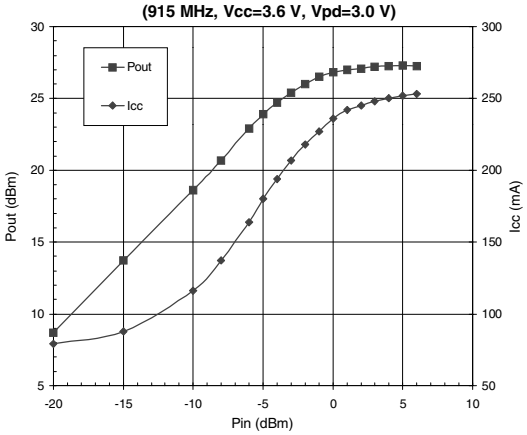


Evaluation Board Layout
Board Size 2.0” x 2.0”

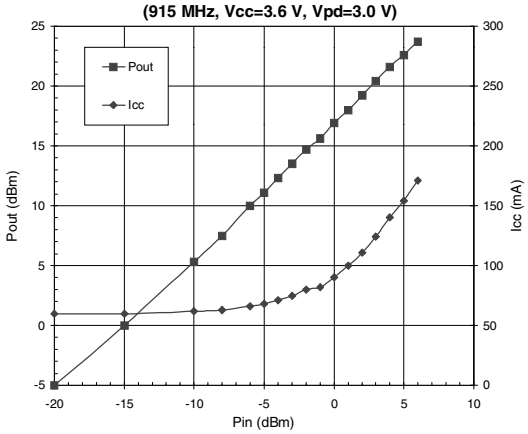




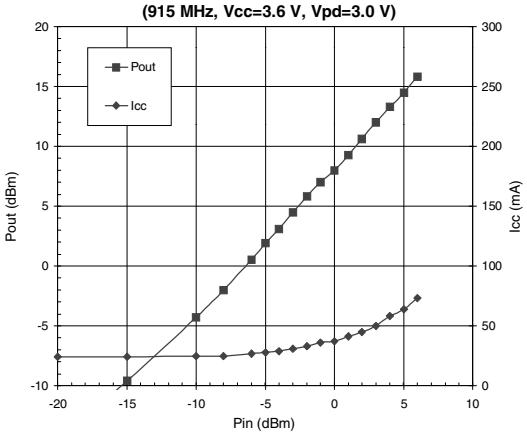
Pout and Icc vs. Pin, State 11
(915 MHz, Vcc=3.6 V, Vpd=3.0 V)



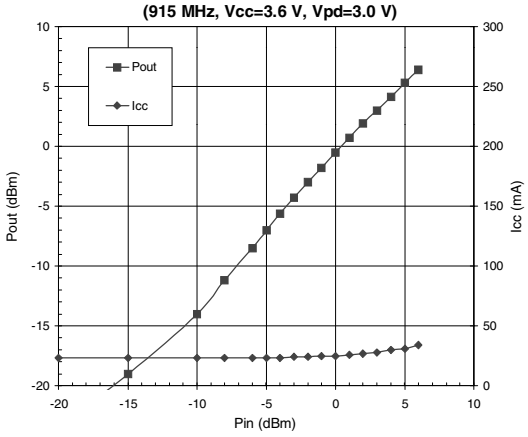
Pout and Icc vs. Pin, State 10
(915 MHz, Vcc=3.6 V, Vpd=3.0 V)



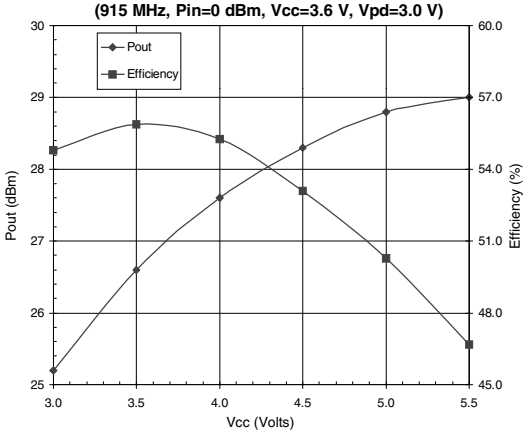
Pout and Icc vs. Pin, State 01
(915 MHz, Vcc=3.6 V, Vpd=3.0 V)



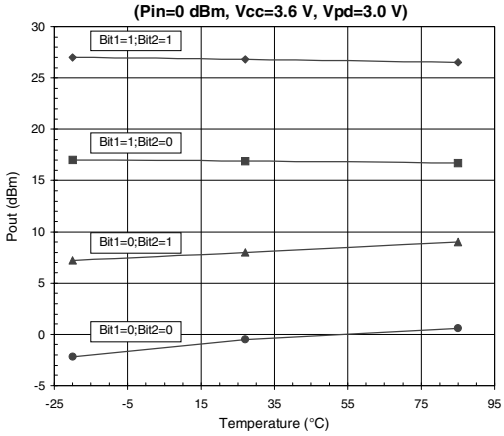
Pout and Icc vs. Pin, State 01
(915 MHz, Vcc=3.6 V, Vpd=3.0 V)



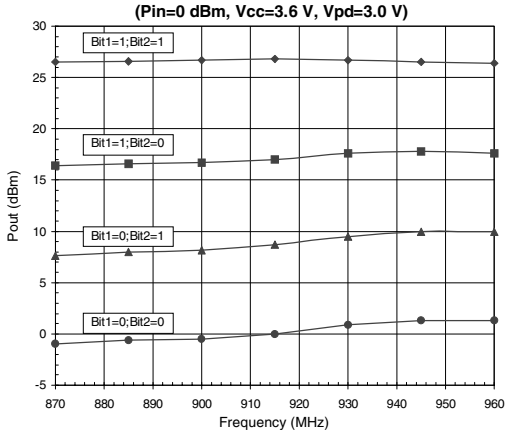
Pout and Efficiency vs. Vcc, Full Gain
(915 MHz, Pin=0 dBm, Vcc=3.6 V, Vpd=3.0 V)



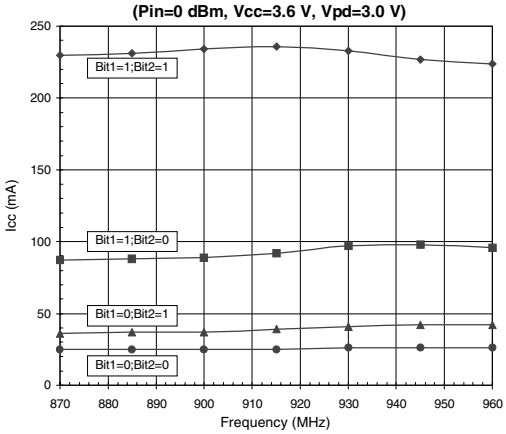
Pout vs. Temperature, All Gain Settings
(Pin=0 dBm, Vcc=3.6 V, Vpd=3.0 V)



Pout vs. Frequency, All Gain Settings
(Pin=0 dBm, Vcc=3.6 V, Vpd=3.0 V)



Icc vs. Frequency, All Gain Settings
(Pin=0 dBm, Vcc=3.6 V, Vpd=3.0 V)



RF2157

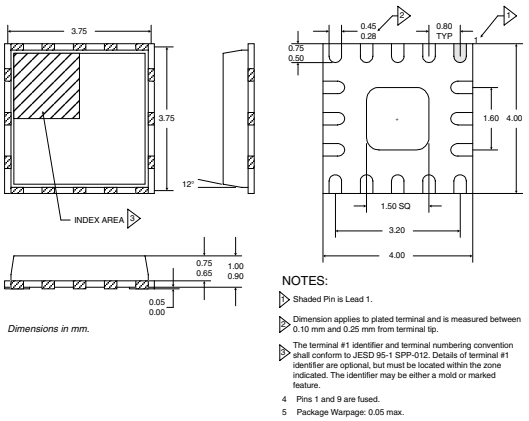
PCS CDMA/TDMA 3V POWER AMPLIFIER

Typical Applications

- 3V 1850-1910MHz CDMA PCS Handsets
- 3V 1750-1780MHz CDMA PCS Handsets
- 3V TDMA PCS Handsets
- Spread Spectrum Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF2157 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA and TDMA hand-held digital equipment, spread spectrum systems, and other applications in the 1710MHz to 1910MHz band. The device is packaged in a compact 4mmx4mm LCC, as well as a 4mmx4mm MLF (micro leaded package). The frequency response can be optimized for linear performance over 1710MHz to 1910MHz. The device features a digital mode switch which can be used to minimize operating current under low output power conditions.

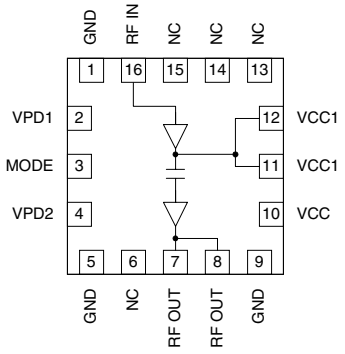


Dimensions in mm.

Package Style: MLF16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 24dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode
- 1750MHz to 1910MHz Operation

Ordering Information

RF2157	PCS CDMA Power Amplifier
RF2157 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2157

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+4.5	V_{DC}
Mode Voltage (V_{MODE})	+3.5	V_{DC}
Control Voltage (V_{PD})	+3.5	V_{DC}
Input RF Power	+12	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-65 to +150	°C

Caution! ESD sensitive device.

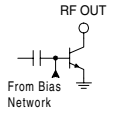
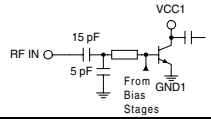
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, V_{PD}=2.8V, V_{MODE}≤0.5V unless otherwise specified
Usable Frequency Range	1750		1910	MHz	
Typical Frequency Range		1750-1780		MHz	Tuned Matching Network
		1850-1910		MHz	Tuned Matching Network
Linear Gain	23	25	28	dB	P_{OUT}=29dBm, V_{MODE}≤0.5V
	22	24	26	dB	P_{OUT}=29dBm, V_{MODE}≥2.5V
Small Signal Gain	24	27	29	dB	P_{IN}≤-20dBm
Second Harmonic (Including second harmonic trap)		-35		dBc	
Third Harmonic		-40		dBc	
Fourth Harmonic		-45		dBc	
Linear Output Power (CDMA/ TDMA Modulation)	29			dBm	V_{MODE}≤0.5V
CDMA Linear Efficiency	30	35		%	P_{OUT}=29dBm
CDMA ACPR @ 1.25MHz		-46	-44	dBc	
Noise Power @ 80MHz Offset		-139		dBm/Hz	
Linear Output Power (CDMA/ TDMA Modulation)	29			dBm	V_{MODE}≥2.5V
CDMA Linear Efficiency	33	37		%	P_{OUT}=29dBm
		6		%	P_{OUT}=16dBm, V_{MODE}≥2.5V
CDMA ACPR @ 1.25MHz		-46	-44	dBc	P_{OUT}=29dBm
Noise Power @ 80MHz Offset		-139		dBm/Hz	P_{OUT}=29dBm
TDMA Linear Efficiency	30	37		%	P_{OUT}=29dBm
TDMA ACPR (30kHz Offset)		-31	-28	dBc	P_{OUT}=29dBm
TDMA ACPR (60kHz Offset)		-52	-48	dBc	P_{OUT}=29dBm
Linear Output Power (CDMA Modulation)	28			dBm	V_{CC}=3.0V
Input VSWR		< 2:1			
Output Load VSWR			10:1		No damage.
Stability	5:1				
Junction to Case Thermal Resistance		25		°C/W	

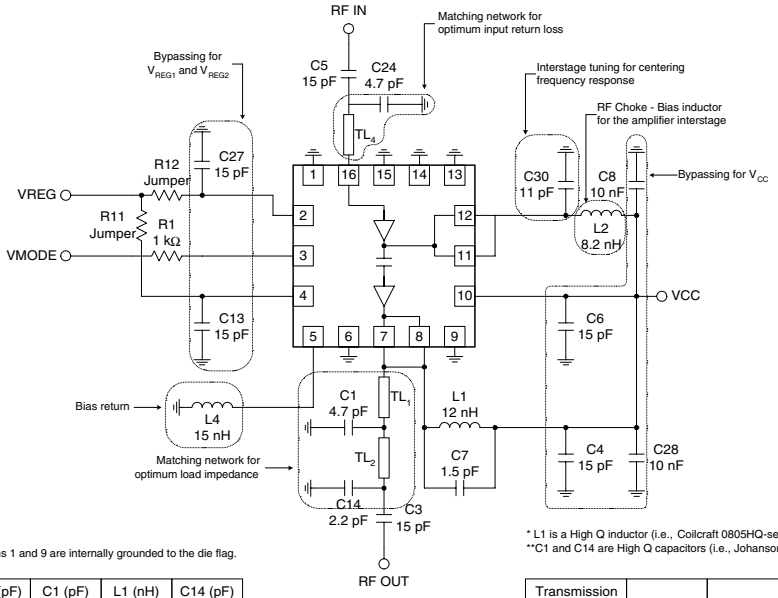
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Power Supply Voltage		3.4	4.5	V	
Idle Current		325		mA	$V_{MODE} \leq 0.5V$
	110	140	175	mA	$V_{MODE} = 2.8V$
V_{PD} Current		10		mA	$V_{PD} = 2.8V$
Turn On/Off time			100	ns	
Total Current (Power down)			10	µA	$V_{PD} \leq 0.2dBm$
V_{PD} Low Voltage		0	0.2	V	
V_{PD} High Voltage	2.7	2.8	2.9	V	
MODE High Voltage	2.5	2.8			$R_1 = 1k\Omega$
MODE Low Voltage		0	0.5		

RF2157

Pin	Function	Description	Interface Schematic
1	GND	This pin is internally grounded to the die flag.	
2	VPD1	Power Down control for first stage. When this pin is “low”, first stage circuits are shut off. When this pin is 2.8V, all first stage circuits are operating normally. V_{PD1} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V.	
3	MODE	For full power operation, VMODE is set low. VMODE will reduce the bias current by approximately 50% when set HIGH. Large Signal Gain is reduced approximately 1.5dB at 29dBm P_{OUT}. Small Signal Gain is reduced by approximately 6dB at lower temperatures. An external series resistor is optional to limit the amount of current required.	
4	VPD2	Power Down control for the second stage. When this pin is “low”, the second stage circuit is shut off. When this pin is 2.8V, the second stage circuit is operating normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 15pF high frequency bypass capacitor is recommended.	
5	GND	Connect to ground plane via 15nH inductor. DC return for the second stage bias circuit.	
6	NC	It is recommended that this pin be connected to the ground plane. This should be isolated from the backside ground contact on the top metal layer.	
7	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1710MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
8	RF OUT	Same as pin 7.	See pin 7.
9	GND	This pin is internally grounded to the die flag.	
10	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
11	VCC1	Power supply for first stage and interstage match. Pins 11 and 12 should be connected by a common trace where the pins contact the printed circuit board.	
12	VCC1	Same as pin 11.	
13	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
14	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
15	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
16	RF IN	RF input. An external 15pF series capacitor is required as a DC block. In addition, a series transmission line and shunt capacitor, 5pF, are required to provide 2:1 VSWR.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic
Korea - CDMA



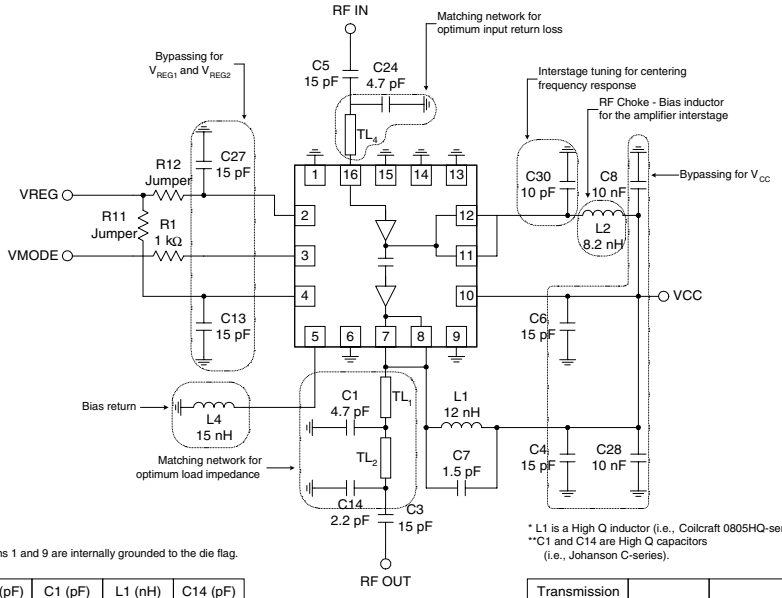
Pins 1 and 9 are internally grounded to the die flag.

Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (Korea)	10	4.7	12	2.2

* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors (i.e., Johanson C-series).

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (Korea)	30-40 mils	150 mils	20-30 mils	200 mils

Application Schematic
US - CDMA



Pins 1 and 9 are internally grounded to the die flag.

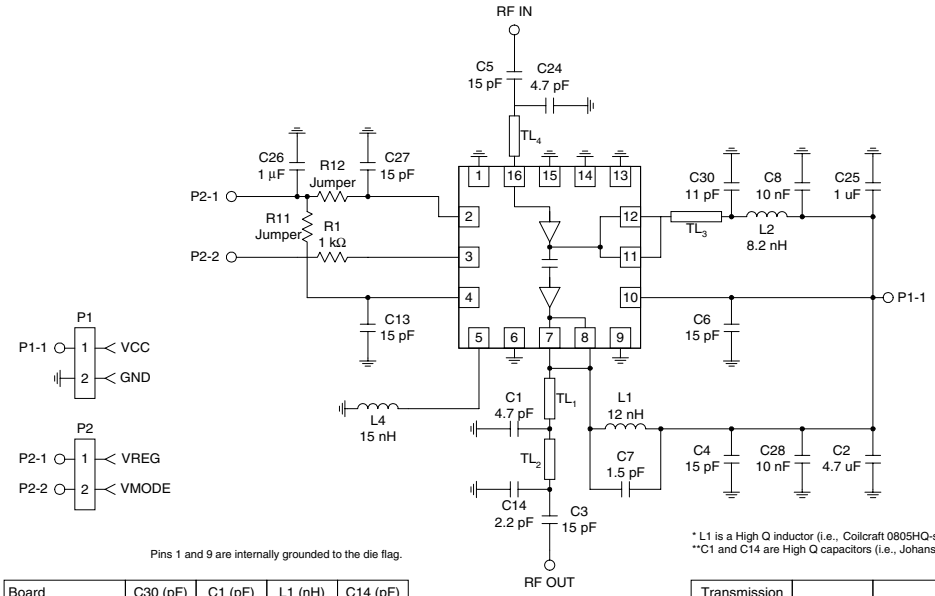
Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	10	4.7	12	2.2

* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors (i.e., Johanson C-series).

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (US)	30-40 mils	150 mils	20-30 mils	200 mils

Evaluation Board Schematic
Korea - CDMA

(Download Bill of Materials from www.rfmd.com.)



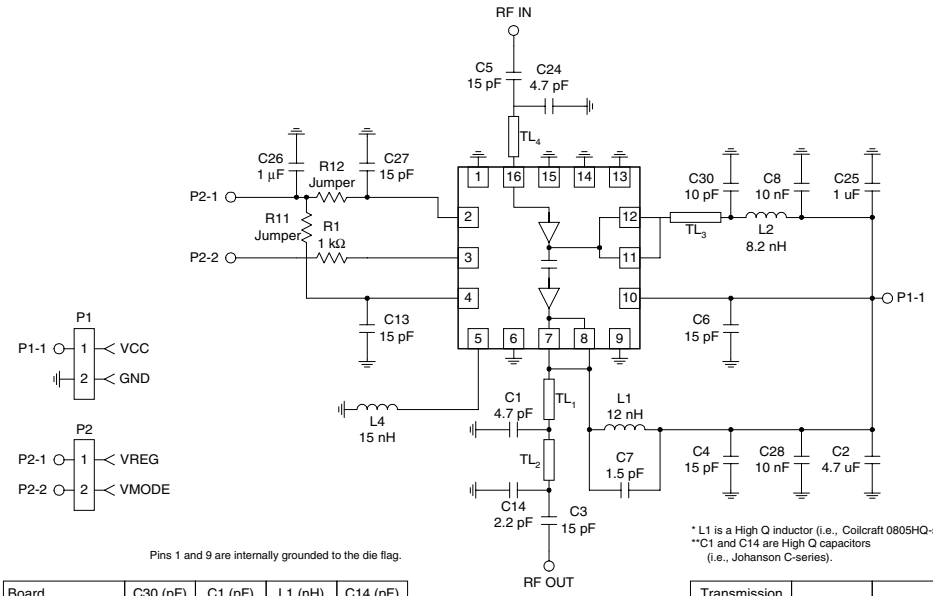
Pins 1 and 9 are internally grounded to the die flag.

Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (Korea)	10	4.7	12	2.2

* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors (i.e., Johanson C-series).

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (Korea)	30-40 mils	150 mils	20-30 mils	200 mils

Evaluation Board Schematic
US - CDMA



Pins 1 and 9 are internally grounded to the die flag.

Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	10	4.7	12	2.2

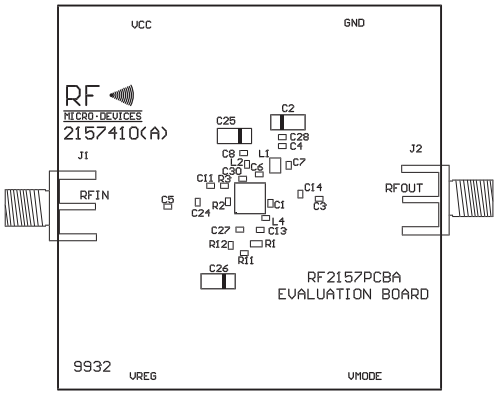
* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

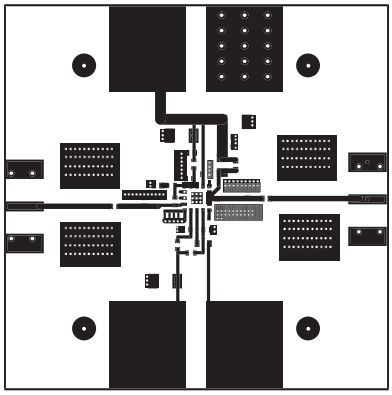
Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (US)	30-40 mils	150 mils	20-30 mils	200 mils

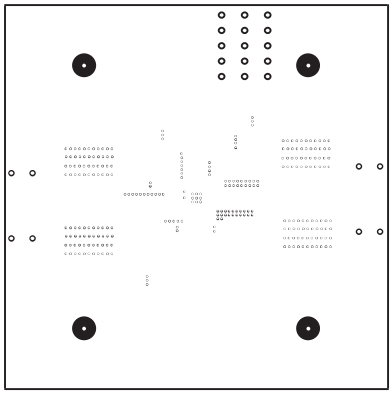
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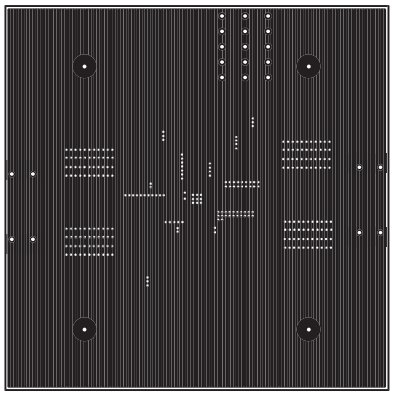
Evaluation Board Layout
Board Size 2" x 2"

Board Thickness 0.031", Board Material FR-4, Multi-Layer









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Preliminary

RF2161

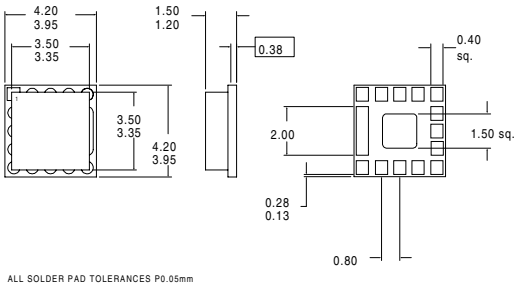
3V WCDMA POWER 1900MHZ 3V LINEAR POWER AMPLIFIER

Typical Applications

- 3V 1850-1910 CDMA-2000 Handsets
- 3V 1920-1980 WCDMA Handsets
- Spread Spectrum Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

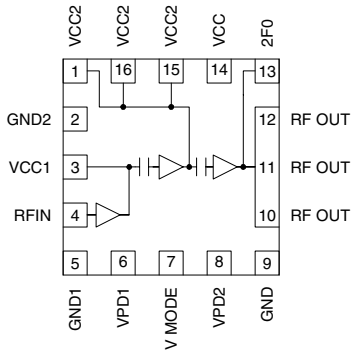
The RF2161 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 3V CDMA-2000 and WCDMA handsets, spread spectrum systems, and other applications in the 1920MHz to 1980MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics over all recommended supply voltages.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MP16KO1A



Functional Block Diagram

Features

- Single 3V Supply
- 27dBm Linear Output Power
- 30dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode

Ordering Information

RF2161	3V WCDMA Power 1900MHZ 3V Linear Power Amplifier
RF2161 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

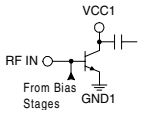
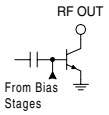
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+5.0	V_{DC}
Mode Voltage (V_{MODE})	+3.0	V_{DC}
Control Voltage (V_{PD})	+3.0	V_{DC}
Input RF Power	+6	dBm
Operating Case Temperature	-30 to +100	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V unless otherwise specified
Usable Frequency Range	1850		2000	MHz	
Typical Frequency Range		1850 to 1910 1920 to 1980		MHz	
Linear Gain	28	30		dB	Mode=Low
	26	28		dB	Mode=High
Second Harmonic (including second harmonic trap)		-35		dBc	
Third Harmonic		-40		dBc	
Fourth Harmonic		-45		dBc	
Maximum Linear Output Power (WCDMA Modulation)	27			dBm	
Total Linear Efficiency	30	35		%	
Adjacent Channel Power Rejection @ 5MHz	-45	-40	-38	dBc	P_{OUT}=27dBm, WCDMA Modulation
Adjacent Channel Power Rejection @ 10MHz	-60	-50	-48	dBc	P_{OUT}=27dBm, WCDMA Modulation
Noise Power		-92		dBc	P_{OUT}=+27dBm, 30kHz BW Rx Band 2110MHz to 2170MHz
Maximum Linear Output Power (WCDMA Modulation)	27			dBm	V_{CC}=3.0V
Total Linear Efficiency		36		%	
Input VSWR		< 2:1			
Output Load VSWR			5:1		No oscillations
Power Supply					
Power Supply Voltage	3.0	3.4	5.0	V	
Idle Current		120		mA	MODE = high
V_{PD} Current		10		mA	Total pins 7 and 8, V_{PD} = 2.8 V
Turn On/Off time			100	ns	
Total Current (Power down)			10	µA	V_{PD} = low
V_{PD} "Low" Voltage		0	0.2	V	
V_{PD} "High" Voltage	2.7	2.8	2.9	V	
MODE "High" Voltage	2.5	2.8			
MODE "Low" Voltage		0	0.5		

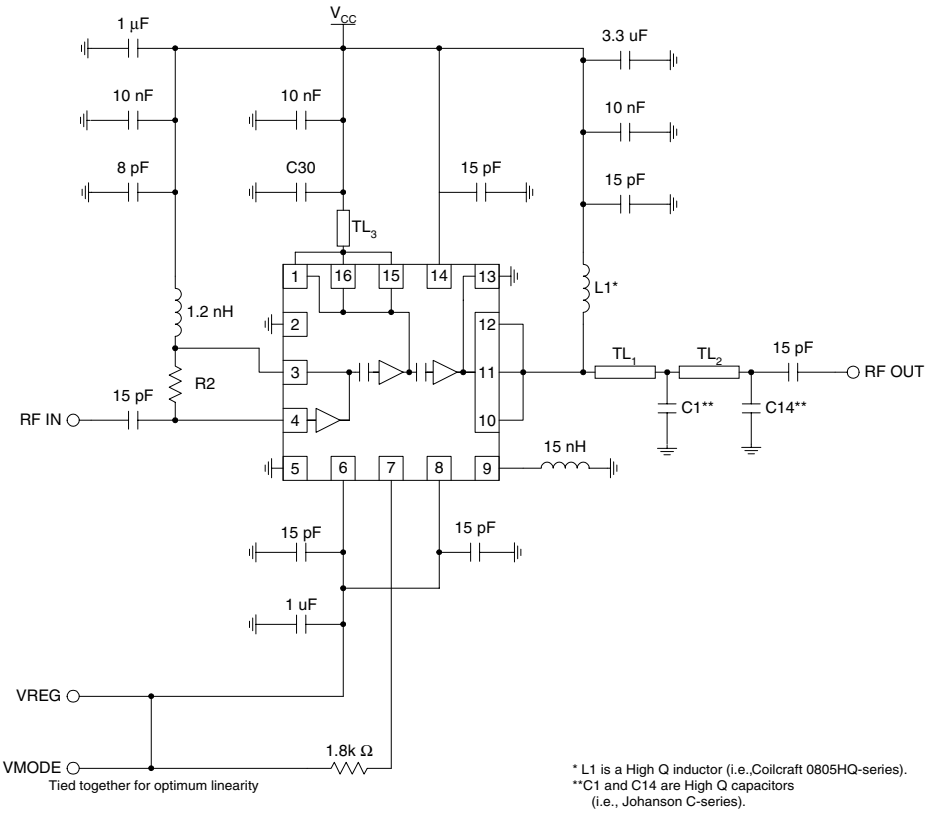
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Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for second stage and interstage match. Pins 1, 15 and 16 should be connected by a common trace where the pins contact the printed circuit board.	
2	GND2	Ground for second stage. For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	
3	VCC1	Power supply for first stage and interstage match. V_{CC} should be fed through a 1.2nH inductor terminated with a 8.2pF capacitor on the supply side. The inductor should be as close to the pin as possible.	See pin 4.
4	RF IN	RF input. An external series capacitor is required as a DC block. The input match can be improved to <2:1 by using a series capacitor and shunt inductor.	
5	GND1	Ground for first stage. For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	See pin 4.
6	VPD1	Power Down control for first and second stages. When this pin is “low”, all first and second stage circuits are shut off. When this pin is 2.8V, all first and second stage circuits operate normally. V_{PD1} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V.	
7	VMODE	V_{MODE} adjusts the bias to the 2nd and 3rd stages. For full power operation, MODE is set low. When operating in a lower output power mode (<+25dBm) this pin is set high to reduce bias current by up to 50%. An external series resistor is optional to limit the amount of current required. At low temperature (-30°C), it is recommended to set V_{MODE} low to maintain correct operation.	
8	VPD2	Power Down control for third stage. When this pin is “low”, all and third stage circuits are shut off. When this pin is 2.8V, all and third stage circuits operate normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 12pF high frequency bypass capacitor is recommended.	
9	GND	For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	
10	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the third stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1920MHz to 1980MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT	Same as pin 10.	See pin 10.
13	2FO	Second harmonic trap. Keep traces physically short and connect immediately to ground plane. This ground should be isolated from backside ground contact.	
14	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
15	VCC2	Same as Pin 1.	
16	VCC2	Same as Pin 1.	

Pin	Function	Description	Interface Schematic
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

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Application Schematic
WCDMA (1920MHz to 1980MHz)



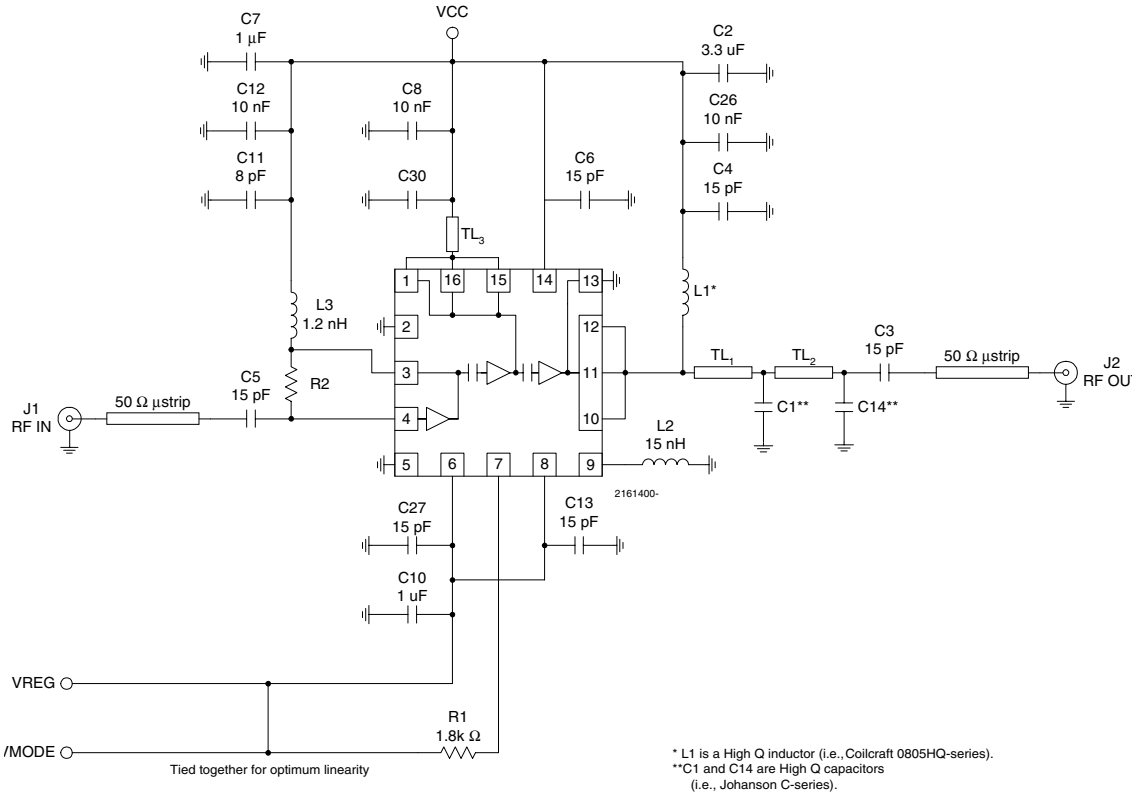
* L1 is a High Q inductor (i.e.,Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
WCDMA	150	10	4.7	16	2.2

Transmission Line Length	TL_1	TL_2	TL_3
WCDMA	0.067"	0.130"	0.022"

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Evaluation Board Schematic
WCDMA (1920MHz to 1980MHz)



* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

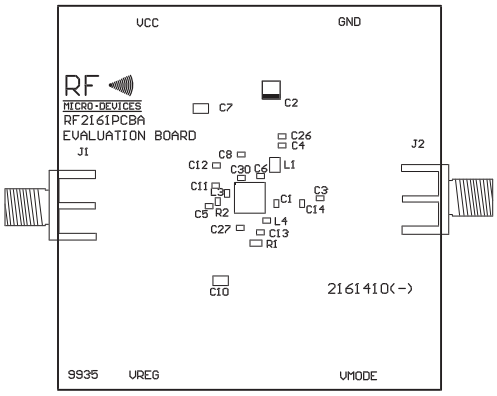
Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
WCDMA	150	10	4.7	16	2.2

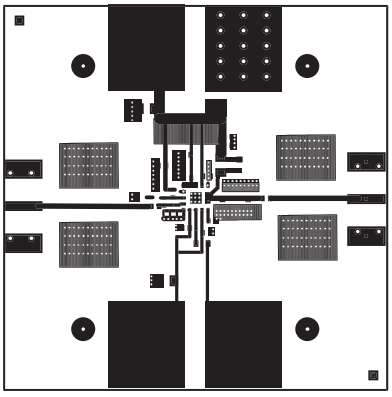
Transmission Line Length	TL_1	TL_2	TL_3
WCDMA	0.067"	0.130"	0.022"

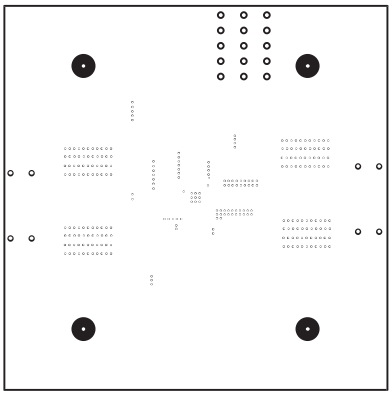
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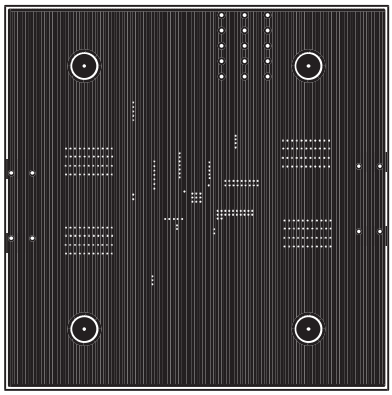
Evaluation Board Layout
Board Size 2.00” x 2.00”

Board Thickness 0.28”, Board Material FR-4, Multi-Layer









RF MICRO·DEVICES

Preliminary

RF2162

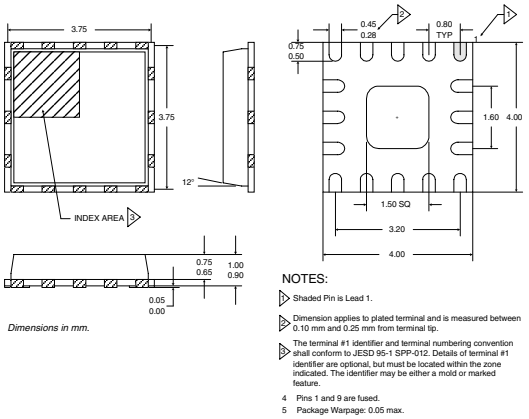
3V 900MHZ LINEAR AMPLIFIER

Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA/TACS Cellular Handsets
- 3V TDMA/AMPS Cellular Handsets
- Spread Spectrum Systems
- CDPD Portable Data Cards
- Portable Battery-Powered Equipment

Product Description

The RF2162 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 960MHz band. The RF2162 has an analog bias control voltage to maximize efficiency. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The device is packaged in a compact 4mmx4mm MLF (micro leaded package).



Dimensions in mm.

NOTES:

Shaded Pin is Lead 1.

Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.

The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.

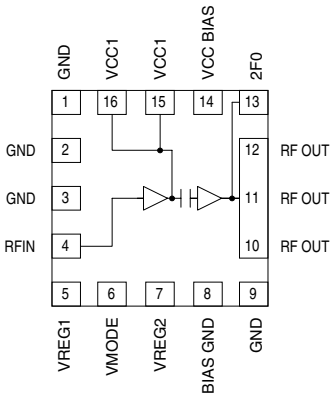
4 Pins 1 and 9 are fused.

5 Package Warpage: 0.05 max.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MLF16



Functional Block Diagram

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 29dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 960MHz Operation

Ordering Information

RF2162	3V 900MHz Linear Amplifier
RF2162 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

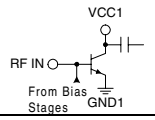
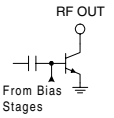
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+4.5	V_{DC}
Mode Voltage (V_{MODE})	+3.0	V_{DC}
Control Voltage (V_{PD})	+3.0	V_{DC}
Input RF Power	+12	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-30 to +150	°C
Moisture Sensitivity	Modified JEDEC Level 2	

Caution! ESD sensitive device.

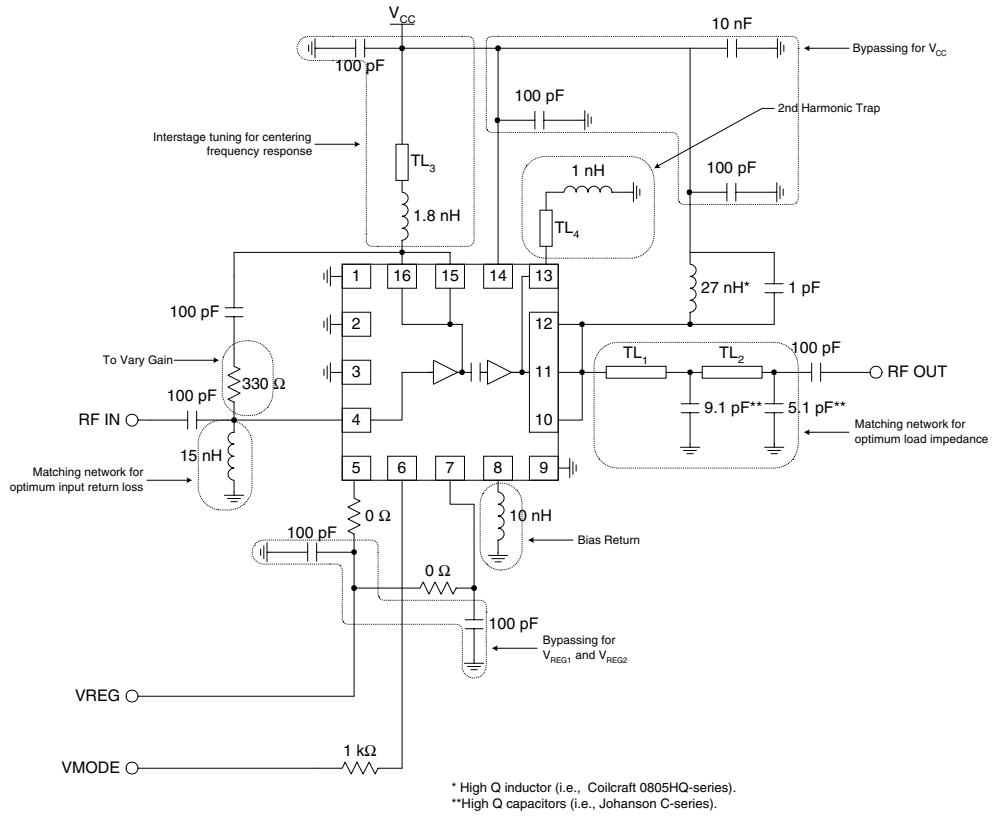
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, Freq=824MHz to 849MHz unless otherwise specified
Usable Frequency Range	800		960	MHz	
Typical Frequency Range		824-849		MHz	
Linear Gain	28	29	31	dB	
Second Harmonic (including second harmonic trap)		-30		dBc	
Max CW Output Power		31.5		dBm	
Total Efficiency (AMPS mode)		50		%	
Maximum Linear Output Power (CDMA Modulation)		29		dBm	
Total Linear Efficiency	30	35		%	
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR @ 885kHz
		-58	-56	dBc	ACPR @1980kHz
Noise Power		-90	-89	dBm	V_{CC}=3.4V; BW=30kHz; RX Band NF measure from TX center band to RX center band.
Maximum Linear Output Power (CDMA Modulation)		29		dBm	V_{CC}=3.0V
Total Efficiency (AMPS mode)		50		%	
Max CW Output Power	30	30.5	31	dBm	
Total Linear Efficiency	30	36		%	
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR @ 885kHz
		-58	-56	dBc	ACPR @ 1980kHz
Input VSWR		<2:1			
Output Load VSWR			10:1		No damage.
Power Supply					
Power Supply Voltage	3.0	3.4	4.5	V	
Idle Current		135	200	mA	V_{MODE}=0V to 0.5V
V_{REG} Current		10	15	mA	Total pins 6 and 7, V_{REG}=2.8V
Turn On/Off time			<100	ns	
Total Current (Power down)			10	µA	V_{PD}=Low
V_{REG} "Low" Voltage		0	0.2	V	
V_{REG} "High" Voltage	2.7	2.8	2.9	V	
VMODE Bias Control Voltage Range		0 to 2.5		V	

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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Connect to package base ground. This ground should be isolated from the backside ground contact on top metal layer.	
2	GND1	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact on top metal layer.	
3	GND1	Same as Pin 2.	
4	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
5	VREG1	Enable voltage for first stage. When this pin is "low", all circuits are shut off. When this pin is 2.8V, all circuits are operating normally. V_{REG} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 100pF high frequency bypass capacitor is recommended.	
6	VMODE	This is an analog bias current control pin. The range is 0V for minimum bias to 3.0 for maximum bias.	
7	VREG2	Enable voltage for second or output stage. When this pin is "low", all circuits are shut off. When this pin is 2.8V, all circuits are operating normally. V_{REG} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 100pF high frequency bypass capacitor is recommended.	
8	GND	Bias circuitry ground. See application schematic.	
9	GND	Ground connection. Connect to package base ground. This ground should be isolated from the backside ground contact on top metal layer.	
10	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT	Same as pin 10.	
13	2FO	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with an on chip capacitor at 2fo is required at this pin.	
14	VCC BIAS	Power supply for bias circuitry. A 100pF high frequency bypass capacitor is recommended.	
15	VCC1	Interstage tuning and bias supply for first stage.	
16	VCC1	Interstage tuning and bias supply for first stage.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

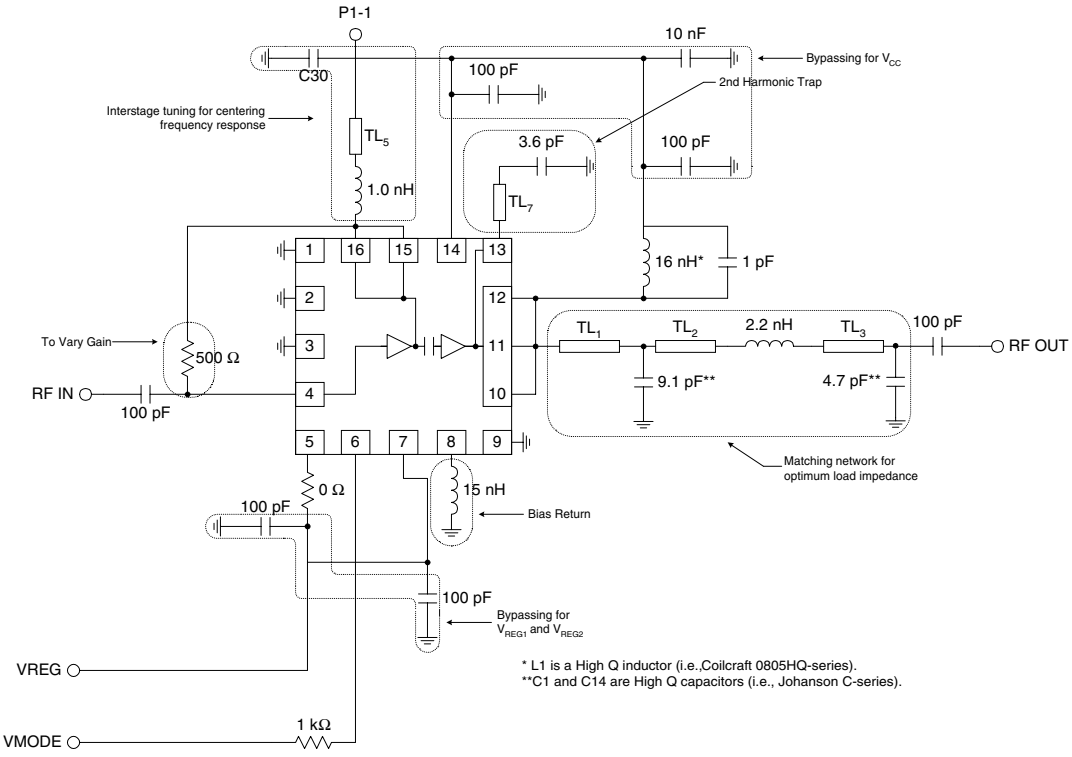
Application Schematic - US CDMA



* High Q inductor (i.e., Coilcraft 0805HQ-series).
**High Q capacitors (i.e., Johanson C-series).

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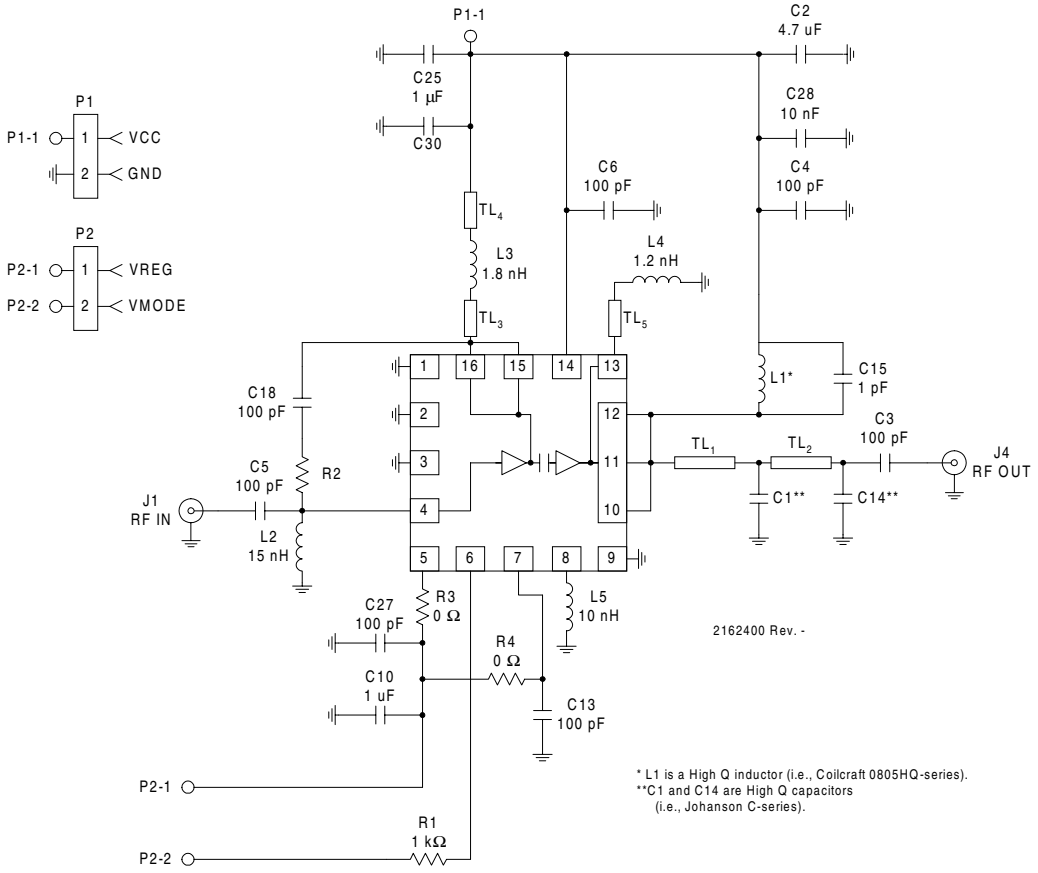
Application Schematic - US TDMA



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Evaluation Board Schematic - US CDMA

(Download Bill of Materials from www.rfmd.com.)

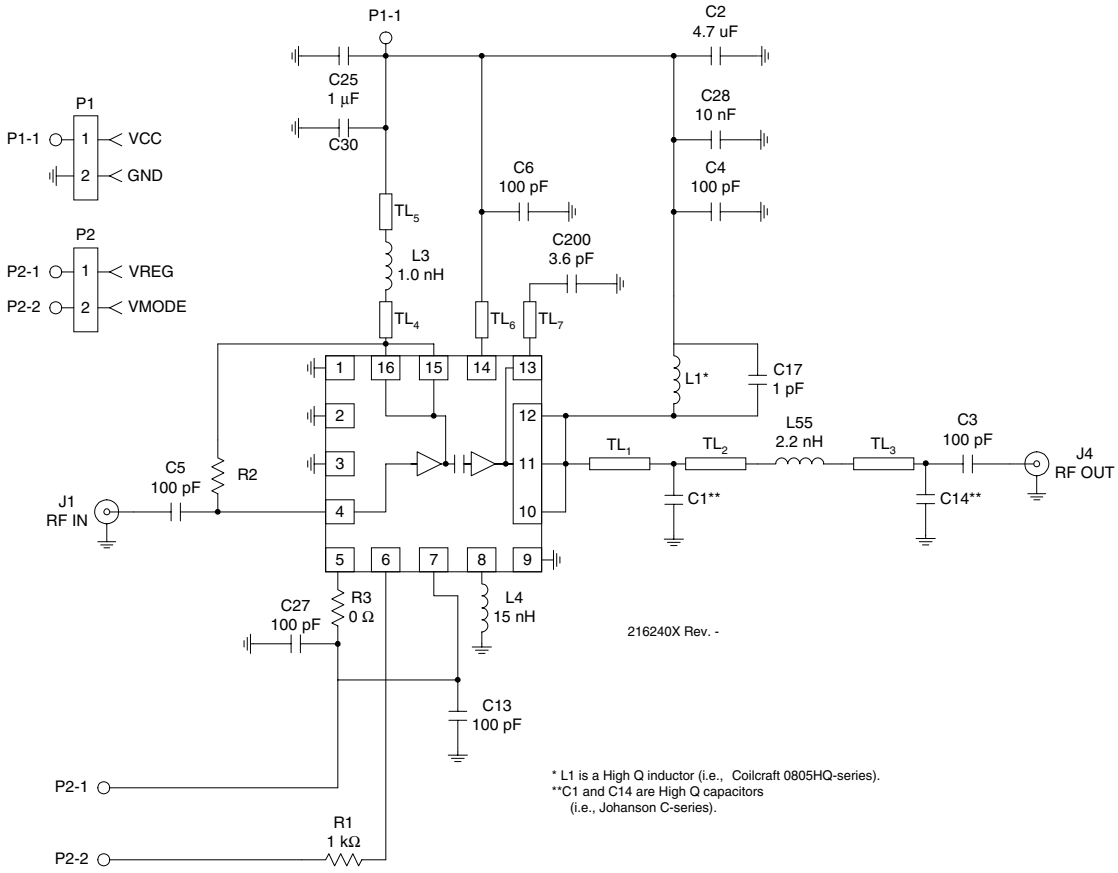


Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	330	100	9.1	27	5.1

Transmission Line Length	TL_1	TL_2	TL_3	TL_4	TL_5
CDMA (US)	200 mils	150 mils	L=15 mils W=16 mils	L=40-45 mils from L3 W=16 mils	L=15-20 mils W=14 mils

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Evaluation Board Schematic - US TDMA

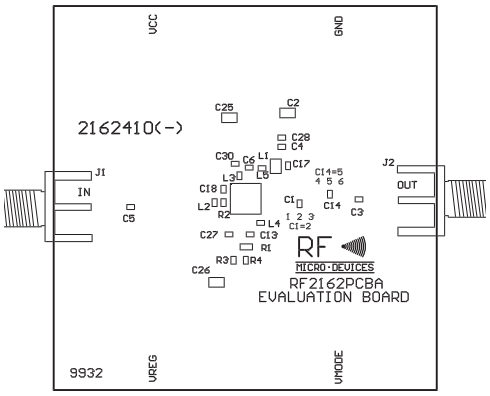


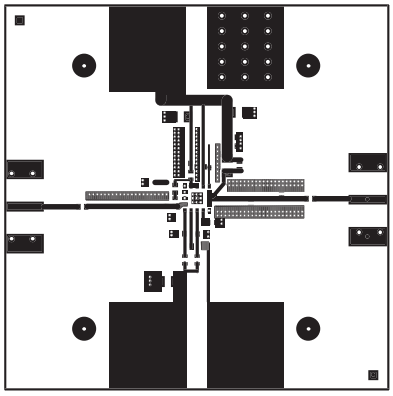
Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
TDMA (US)	500	56	9.1	16	4.7

Transmission Line Length	TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7
TDMA (US)	155 mils	47 mils	L=44 mils	L=12 mils W=16 mils	L=49 mils W=16 mils	L=12 mils	L=12 mils W=14 mils

Evaluation Board Layout
2.0" x 2.0"

Board Thickness 0.031", Board Material FR-4





RF MICRO·DEVICES

Preliminary

RF2172

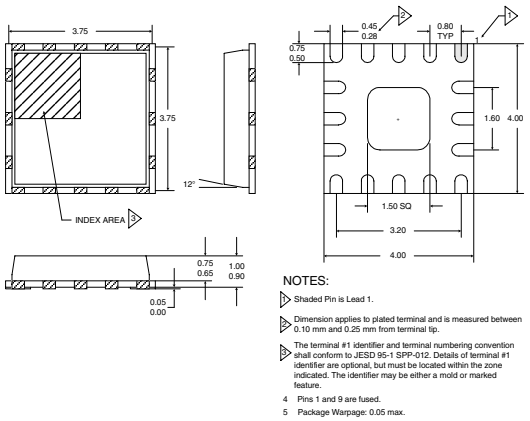
900MHZ ISM BAND 3.6V, 250MW AMP WITH ANALOG GAIN CONTROL

Typical Applications

- 3.6V Spread Spectrum Cordless Phones
- 902MHz to 928MHz ISM Band Systems
- Spread Spectrum Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

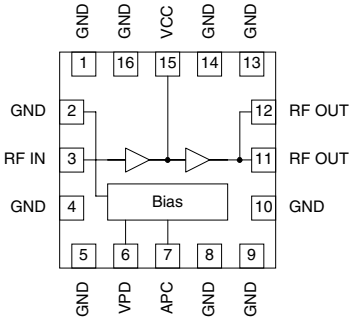
The RF2172 is a medium-power high efficiency amplifier IC targeting 3.6V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in frequency hopping/direct sequence spread spectrum cordless telephones or other applications in the 902MHz to 928MHz ISM band. The device is packaged in a compact 4mm x 4mm LCC. The device features analog gain control to optimize transmit power while maximizing battery life in portable equipment requiring up to 100mW transmit power at the antenna port.



Package Style: MLF16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 24dBm Typical Output Power
- 0dB to 28dB Variable Gain with Analog Control
- 58% Efficiency at Max Output
- On-Board Power Down Mode
- 902MHz to 928MHz Operation

Ordering Information

RF2172	900MHz ISM Band 3.6V, 250mW Amp with Analog Gain Control
RF2172 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

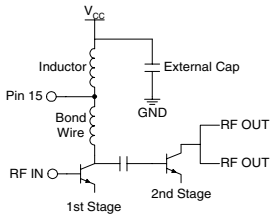
Parameter	Rating	Unit
Supply Voltage (RF off)	-0.5 to +6.0	V_{DC}
APC Voltage (V_{MODE})	-0.5 to +6.0	V_{DC}
Control Voltage (V_{PD})	-0.5 to +6.0	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +155	°C

Caution! ESD sensitive device.

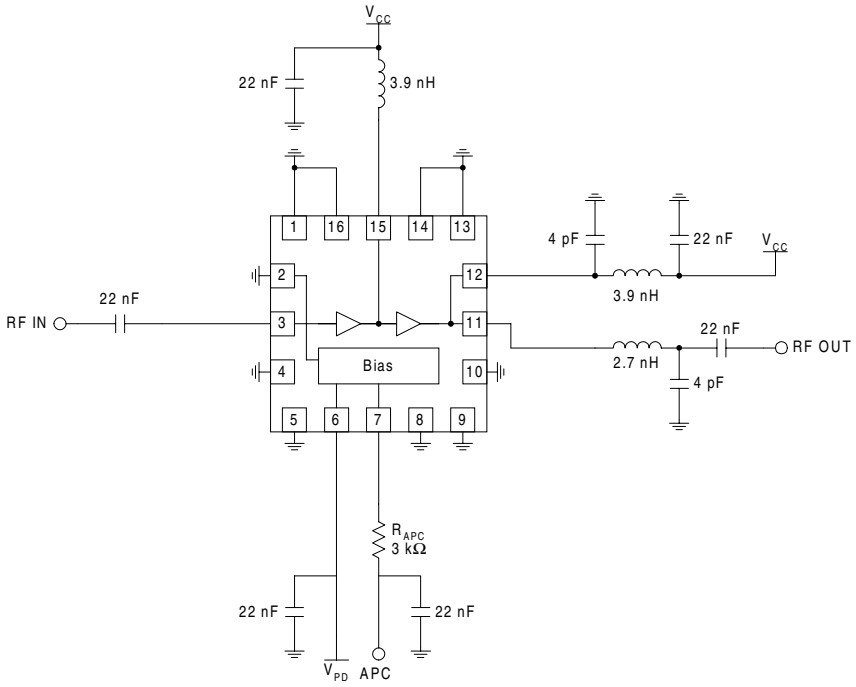
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, V_{PD}=3.6V, V_{APC}=2.5V, Freq=902MHz to 928MHz, P_{IN}=-3.0dBm
Operating Frequency		902 to 928		MHz	
Usable Frequency Range		500 to 1000		MHz	
Maximum Output Power		+24.0		dBm	
Total Efficiency		58		%	
Forward Isolation		-35		dBm	
Second Harmonic		-40		dBc	With External Harmonic Trap
Third Harmonic		-40		dBc	
All other spurious		-50		dBc	
Input Impedance		50		Ω	
Input VSWR		1.8:1			Without Input Match
Output Load VSWR	<10:1				$0 \leq V_{APC} \leq 3.0$
	<6:1				$0 \leq V_{APC} \leq 3.6$
Output Load Impedance		20-j1.6		Ω	Without Second Harmonic Trap
Gain Control Voltage		0 to V_{CC}		V	
Gain Control Slope		20		dB/V	
Gain		0 to 28		dB	
Power Supply					
Power Supply Voltage		3.6		V	
Power Supply Current		145		mA	V_{CC}=3.6V, V_{APC}=3.6V, P_{IN}=-3dBm, V_{PD}=3.6
Idle Current		35		mA	V_{PD}=3.6V, V_{APC}=3.6V, RF $P_{IN} \leq$-30dBm

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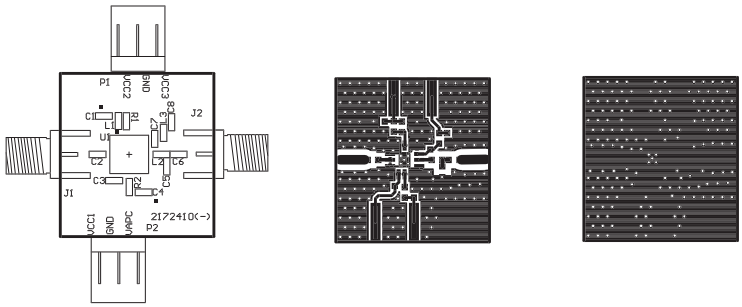
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
2	GND	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	RF IN	RF input. This is a 50Ω input. No external matching is needed. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 15.
4	GND	See Pin 1.	
5	GND	See Pin 1.	
6	VPD	Power down pin. when this pin is 0V, the device will be in power down mode, dissipating minimum DC power. This pin also serves as the VCC supply pin for the bias circuitry. VPD should be at the supply voltage when the part is not in power down mode.	
7	APC	Analog power control. Output power varies as a function of the voltage on this pin. See graph. This pin can be driven with a voltage between 0 and VCC. Series Resistor determines dynamic range of power control. See plot "P_{OUT} versus Gain Control versus Gain Control Resistor".	
8	GND	See Pin 1.	
9	GND	See Pin 1.	
10	GND	See Pin 1.	
11	RF OUT	RF output. An external matching network is required to provide the optimum load impedance at this pin.	See pin 15.
12	RF OUT	RF output and power supply for the output stage. Bias voltage for the output stage is provided through this pin. A shunt cap resonating with the bond wire inductance at $2xf_0$ can also be used at this pin to provide a second harmonic trap.	See pin 15.
13	GND	See Pin 1.	
14	GND	See Pin 1.	
15	VCC	Power supply for driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage. Refer to the application schematic for the proper configuration. Note: Position and value of the components are important.	
16	GND	See Pin 1.	
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the groundplane by vias directly under the device. A short path is required to obtain optimum performance, as well as provide a good thermal path to the PCB for maximum heat dissipation.	

Application Schematic

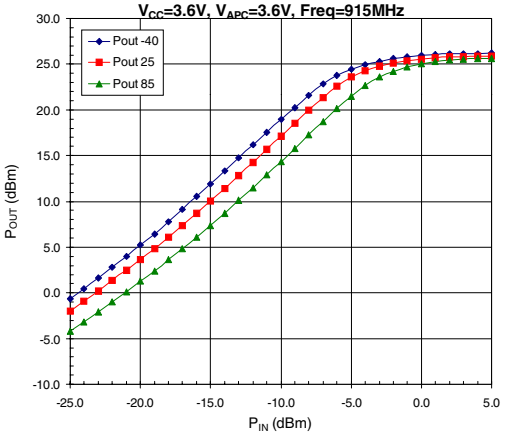


Evaluation Board Layout
Board Size 0.800" x 0.850"

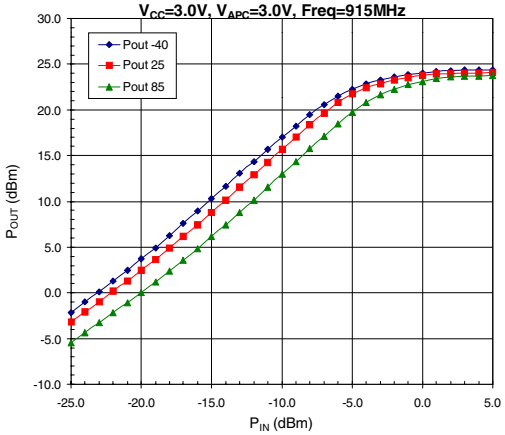
Board Thickness 0.031”, Board Material FR-4



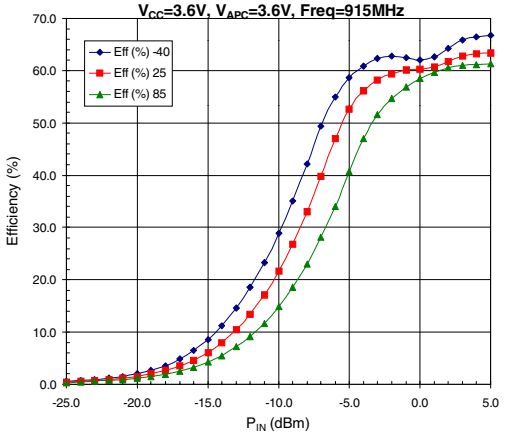
P_{OUT} versus P_{IN}
V_{CC}=3.6V, V_{APC}=3.6V, Freq=915MHz



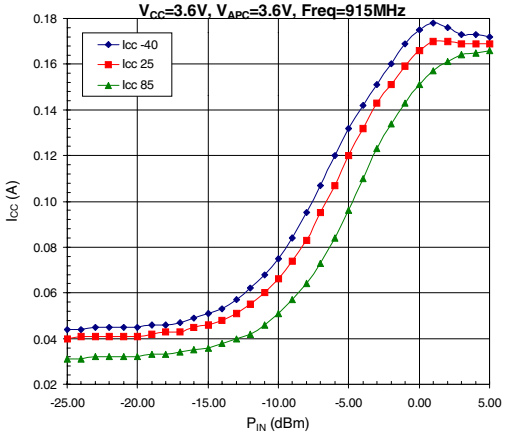
P_{OUT} versus P_{IN}
V_{CC}=3.0V, V_{APC}=3.0V, Freq=915MHz



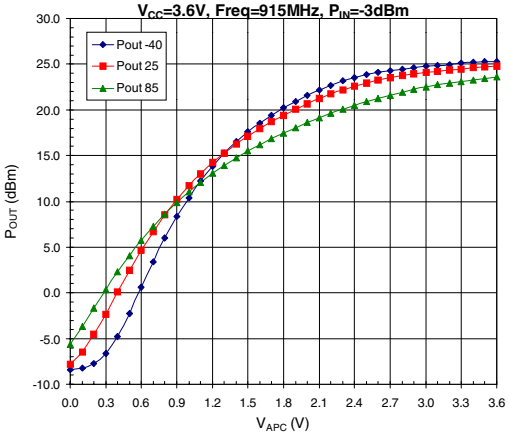
Efficiency versus P_{IN}
V_{CC}=3.6V, V_{APC}=3.6V, Freq=915MHz



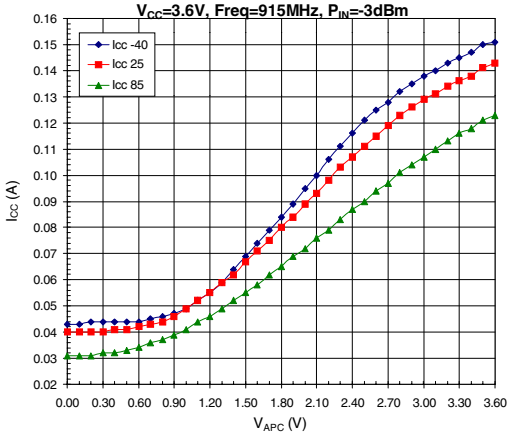
ICC versus P_{IN}
V_{CC}=3.6V, V_{APC}=3.6V, Freq=915MHz

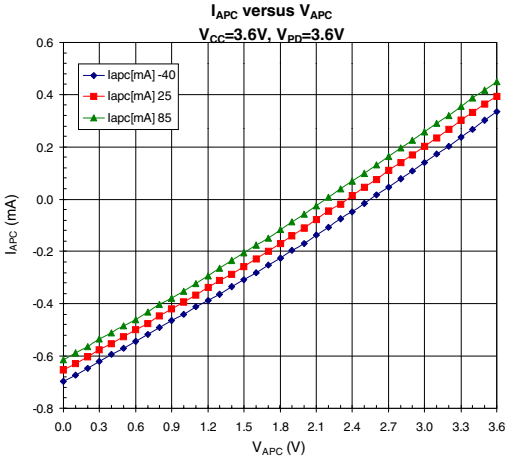


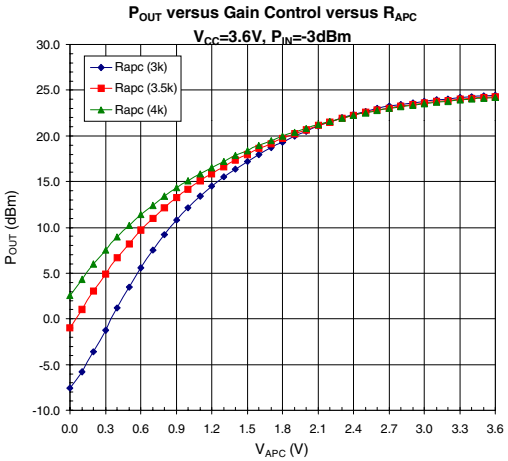
POUT versus V_{APC}
V_{CC}=3.6V, Freq=915MHz, P_{IN}=-3dBm

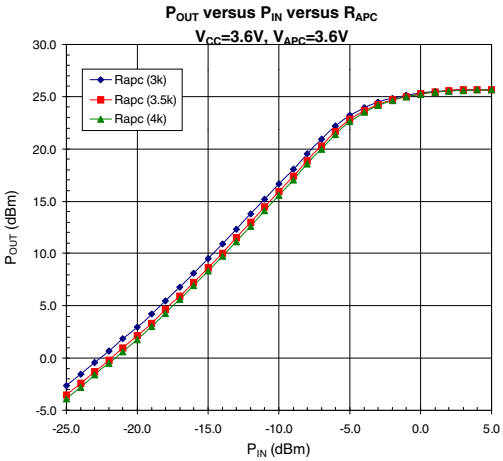


ICC versus V_{APC}
V_{CC}=3.6V, Freq=915MHz, P_{IN}=-3dBm









2 POWER AMPLIFIERS

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Preliminary

RF2173

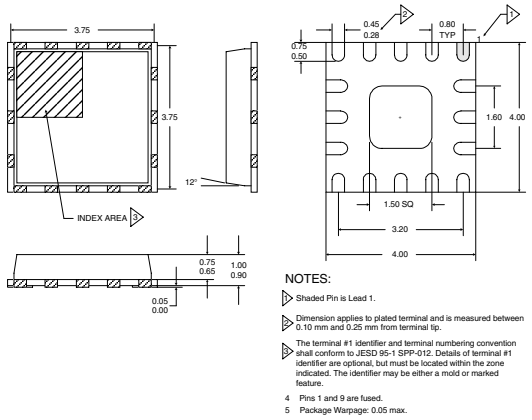
3V GSM POWER AMPLIFIER

Typical Applications

- 3V GSM Cellular Handsets
- 3V Dual-Band/Triple-Band Handsets
- GPRS Compatible
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

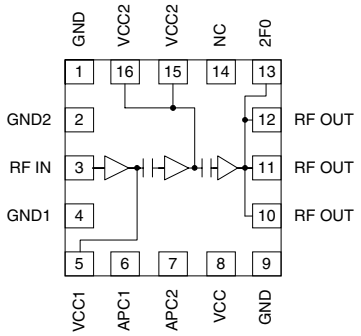
The RF2173 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in GSM hand-held digital cellular equipment and other applications in the 800MHz to 950MHz band. On-board power control provides over 70dB of control range with an analog voltage input, and provides power down with a logic "low" for standby operation. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics. The RF2173 can be used together with the RF2174 for dual-band operation. The device is packaged in an ultra-small plastic package, minimizing the required board space.



Package Style: MLF16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2.7V to 4.8V Supply Voltage
- +36dBm Output Power at 3.5V
- 32dB Gain with Analog Gain Control
- 56% Efficiency
- 800MHz to 950MHz Operation
- Supports GSM and E-GSM

Ordering Information

RF2173	3V GSM Power Amplifier
RF2173 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage ($V_{APC1,2}$)	-0.5 to +3.0	V
DC Supply Current	2400	mA
Input RF Power	+13	dBm
Duty Cycle at Max Power	37.5	%
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

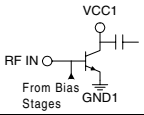
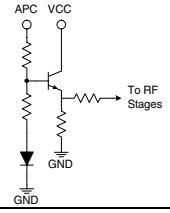
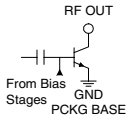
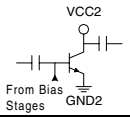
Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V, P_{IN}=+6dBm, Freq=880MHz to 915MHz, 12.5% Duty Cycle, pulse width=577µs
Operating Frequency Range		880 to 915		MHz	See evaluation board schematic.
Usable Frequency Range		800 to 950		MHz	
Maximum Output Power	+35.0	+36		dBm	Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V
	+34.1	+35.2		dBm	Temp=+25°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
	+34.0			dBm	Temp=+85°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
	+33.0	+34.0		dBm	Temp=25°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
	+32.5			dBm	Temp=+85°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
Total Efficiency	50	56		%	At $P_{OUT,MAX}$, V_{CC}=3.2V
		56		%	At $P_{OUT,MAX}$, V_{CC}=3.0V
		12		%	P_{OUT}=+20dBm
		5		%	P_{OUT}=+10dBm
Input Power for Max Output	+4	+6	+8	dBm	
Output Noise Power			-72	dBm	RBW=100kHz, 925MHz to 935MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.0V to 5.0V
			-81	dBm	RBW=100kHz, 935MHz to 960MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.0V to 5.0V
Forward Isolation		-45	-40	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+6dBm
			-30	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+8dBm
Second Harmonic		-50	-38	dBc	
Third Harmonic		-65	-43	dBc	
All Other Non-Harmonic Spurious			-36	dBm	
Input Impedance		50		Ω	
Optimum Source Impedance		40+j10		Ω	For best noise performance
Input VSWR			2.5:1		$P_{OUT,MAX}$-5dB<P_{OUT}<$P_{OUT,MAX}$
			4:1		P_{OUT}<$P_{OUT,MAX}$-5dB
Output Load VSWR	10:1				Spurious<-36dBm, $V_{APC1,2}$=0.2V to 2.6V, RBW=3MHz
Output Load Impedance		1.5-j1.7		Ω	Load Impedance presented at RF OUT pad

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Control V_{APC1} V_{APC2}					
Power Control "ON"	2.6			V	Maximum P_{OUT}, Voltage supplied to the input
Power Control "OFF"	0.2	0.5		V	Minimum P_{OUT}, Voltage supplied to the input
Power Control Range	75			dB	$V_{APC1,2}$=0.2V to 2.6V
Gain Control Slope	5	100	150	dB/V	P_{OUT}=-10dBm to +35dBm
APC Input Capacitance			10	pF	DC to 2MHz
APC Input Current		4.5	5	mA	$V_{APC1,2}$=2.6V
			10	µA	$V_{APC1,2}$=0V
Turn On/Off Time			100	ns	$V_{APC1,2}$=0 to 2.6V
Power Supply					
Power Supply Voltage		3.5		V	Specifications
	2.7		4.8	V	Nominal operating limits, P_{OUT}<+35dBm
			5.5	V	With maximum output load VSWR 6:1, P_{OUT}<+35dBm
Power Supply Current		2		A	DC Current at $P_{OUT,MAX}$
	50	200	375	mA	Idle Current, P_{IN}<-30dBm
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V, Temp=+85°C

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Pin	Function	Description	Interface Schematic
1	GND	Internally connected to the ground slug.	
2	GND2	Ground connection for the driver stage. To minimize the noise power at the output, it is recommended to connect this pin with a trace of about 40mil to the ground plane. This will slightly reduce the small signal gain, and lower the noise power. It is important for stability that this pin have it's own vias to the ground plane, minimizing common inductance.	See pin 15.
3	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 5. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
4	GND1	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance.	See pin 3.
5	VCC1	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Refer to the application schematic for proper configuration. Note that position and value of the components are important.	See pin 3.
6	APC1	Power Control for the driver stage and pre-amplifier. When this pin is "low," all circuits are shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. During normal operation this pin is the power control. Control range varies from about 1.0V for -10dBm to 2.6V for +35dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details. The maximum current into this pin is 5mA when V_{APC1}=2.6V, and 0mA when V_{APC}=0V.	
7	APC2	Power Control for the output stage. See pin 6 for more details.	See pin 6.
8	VCC	Power supply for the bias circuits.	See pin 6.
9	GND	Internally connected to the ground slug.	
10	RF OUT	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pin. An external matching network is required to provide the optimum load impedance.	
11	RF OUT	Same as pin 10.	Same as pin 10.
12	RF OUT	Same as pin 10.	Same as pin 10.
13	2F0	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. The bonding wire together with an external capacitor form a series resonator that should be tuned to the second harmonic frequency in order to increase efficiency and reduce spurious outputs.	Same as pin 10.
14	NC	Not connected.	
15	VCC2	Power supply for the driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	
16	VCC2	Same as pin 15.	Same as pin 15.
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the ground plane by vias directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

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Theory of Operation and Application Information

The RF2173 is a three-stage device with 32 dB gain at full power. Therefore, the drive required to fully saturate the output is +3dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 3V supply to operate to full specification. Power control is provided through a single pin interface, with a separate Power Down control pin. The final stage ground is achieved through the large pad in the middle of the backside of the package. First and second stage grounds are brought out through separate ground pins for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane, and not connected with the output ground to form a so called “local ground plane” on the top layer of the PCB. The output is brought out through the wide output pad, and forms the RF output signal path.

The amplifier operates in near Class C bias mode. The final stage is "deep AB", meaning the quiescent current is very low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 2000mA. The optimum load for the output stage is approximately 1.2Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, vias, and microstrip, and 2 shunt capacitors external to the part. The optimum load impedance at the RF Output pad is 1.5-j1.7Ω. With this match, a 50Ω terminal impedance is achieved. The input is internally matched to 50Ω with just a blocking capacitor needed. This data sheet defines the configuration for GSM operation.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

VCC1 and VCC2 provide supply voltage to the first and second stage, as well as provides some frequency selectivity to tune to the operating band. Essentially, the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be bypassed individually with 100pF capacitors before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RF OUT pin provides the output power. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 2A of current required. Care should be taken to keep the losses low in the bias feed and output components. A narrow microstrip line is recommended because DC losses in a bias choke will degrade efficiency and power.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in this data sheet is based on a 12.5% duty cycle and a 600µs pulse, unless specified otherwise.

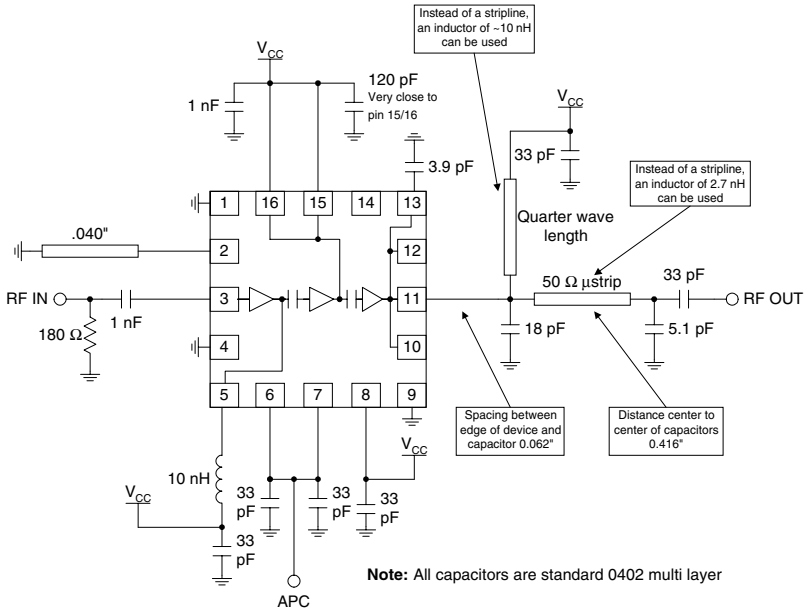
The part will operate over a 3.0V to 5.0V range. Under nominal conditions, the power at 3.5V will be greater than +34.5dBm at +90°C. As the voltage is increased, however, the output power will increase. Thus, in a system design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This must occur during operation, or the device may be damaged from too much power dissipation. At 5.0V, over +38dBm may be produced; however, this level of power is not recommended, and can cause damage to the device.

The HBT breakdown voltage is >20V, so there are no issue with overvoltage. However, under worst-case conditions, with the RF drive at full power during transmit, and the output VSWR extremely high, a low load impedance at the collector of the output transistors can cause currents much higher than normal. Due to the bipolar nature of the devices, there is no limitation on the amount of current de device will sink, and the safe current densities could be exceeded.

High current conditions are potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2173 includes temperature compensation circuits in the bias network to stabilize the RF transistors, thus limiting the current through the amplifier and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations.

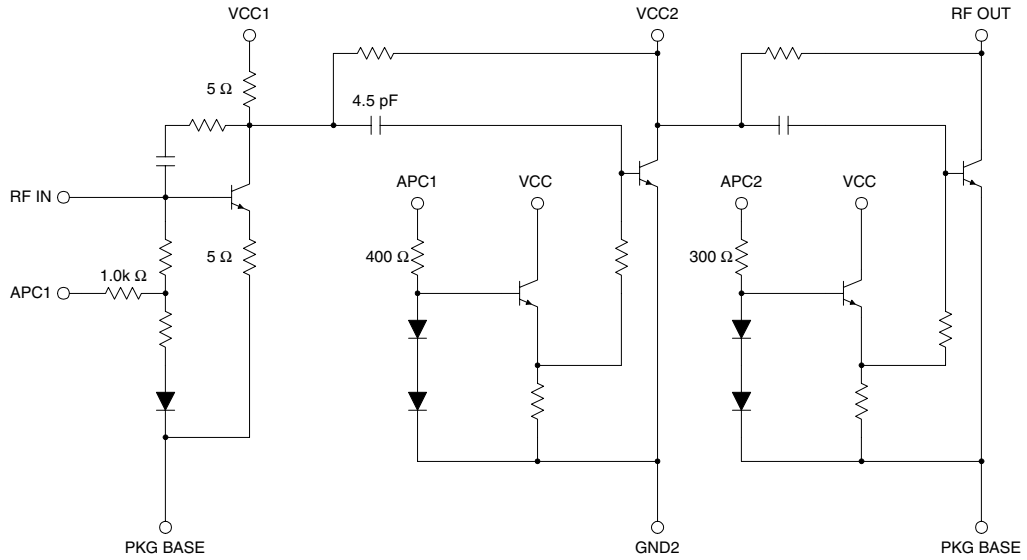
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Application Schematic



Note: All capacitors are standard 0402 multi layer

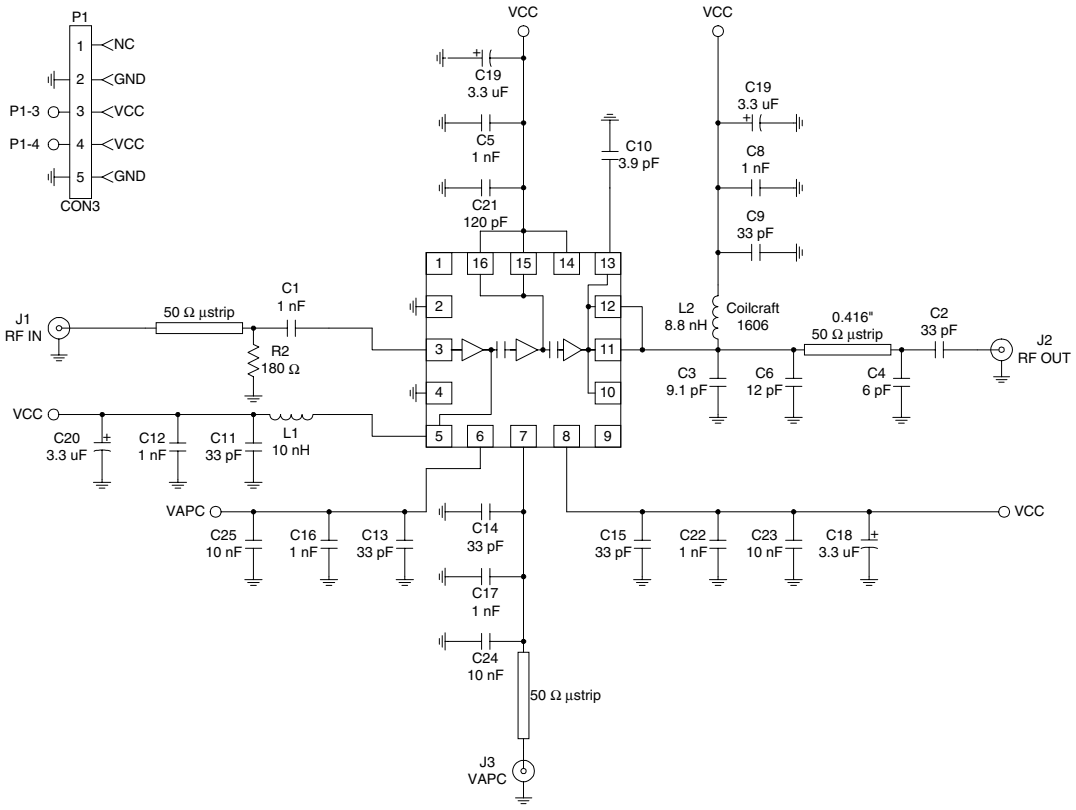
Internal Schematic



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Evaluation Board Schematic

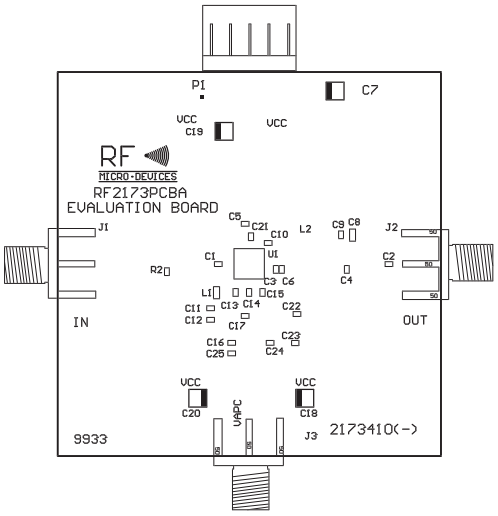
(Download Bill of Materials from www.rfmd.com.)

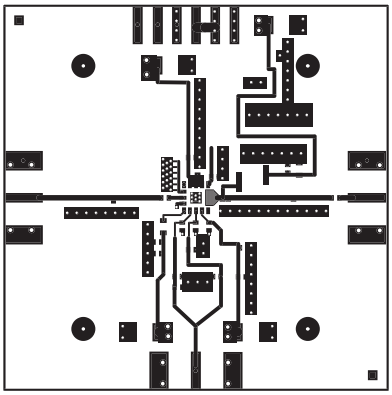


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Evaluation Board Layout
Board Size 2.0” x 2.0”

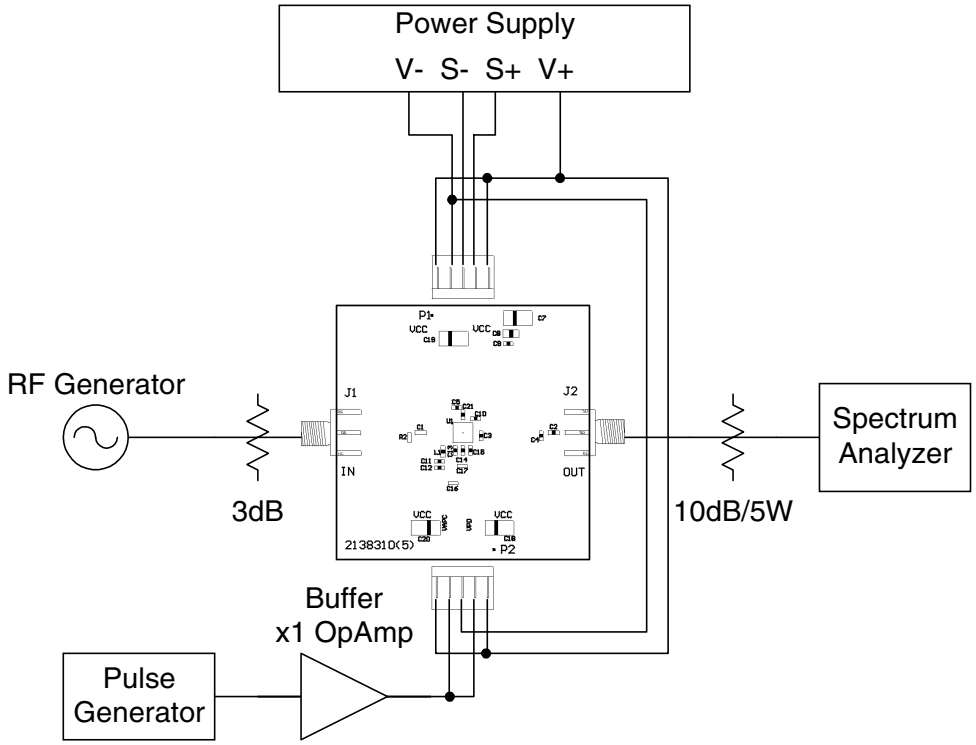
Board Thickness 0.032”; Board Material FR-4; Multi-Layer





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Typical Test Setup



A buffer amplifier is recommended because the current into the V_{APC} changes with voltage. As an alternative, the voltage may be monitored with an oscilloscope.

Notes about testing the RF2173

The test setup shown above includes two attenuators. The 3dB pad at the input is to minimize the effects that the switching of the input impedance of the PA has on the signal generator. When V_{APC} is switched quickly, the resulting input impedance change can cause the signal generator to vary its output signal, either in output level or in frequency. Instead of an attenuator an isolator may also be used. The attenuator at the output is to prevent damage to the spectrum analyzer, and should be able to handle the power.

It is important not to exceed the rated supply current and output power. When testing the device at higher than nominal supply voltage, the V_{APC} should be adjusted to avoid the output power exceeding +36dBm. During load-pull testing at the output it is important to monitor the forward power through a directional coupler. The forward power should not exceed +36dBm, and V_{APC} needs to be adjusted accordingly. This simulates the behavior for the power control loop in this respect. To avoid damage, it is recommended to set the power supply to limiting the current during the burst, not to exceed the maximum current rating.

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MICRO·DEVICES

Preliminary

RF2174

3V DCS POWER AMPLIFIER

Typical Applications

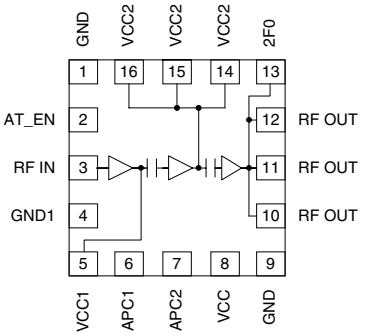
- 3V DCS1800 (PCN) Cellular Handsets
- 3V DCS1900 (PCS) Cellular Handsets
- 3V Dual-Band/Triple-Band Handsets
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- GPRS Compatible

Product Description

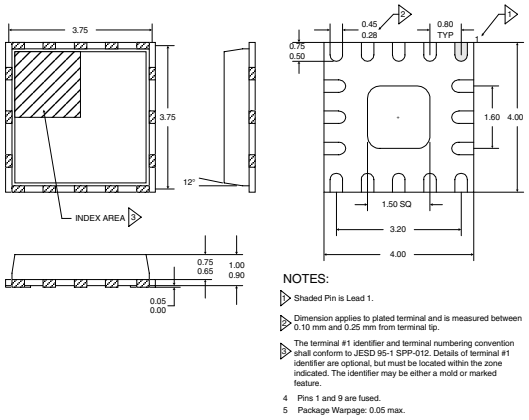
The RF2174 is a high power, high efficiency amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in DCS1800/1900 hand-held digital cellular equipment and other applications in the 1700MHz to 2000MHz band. On-board power control provides over 65dB of control range with an analog voltage input, and provides power down with a logic "low" for standby operation. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics. The RF2174 can be used together with the RF2173 for dual-band operation. The device is packaged in an ultra-small plastic package, minimizing the required board space.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: MLF16

Features

- Single 2.7V to 4.8V Supply Voltage
- +33dBm Output Power at 3.5V
- 27dB Gain with Analog Gain Control
- 51% Efficiency
- 1700MHz to 1950MHz Operation
- Supports DCS1800 and PCS1900

Ordering Information

RF2174	3V DCS Power Amplifier
RF2174 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{APC})	-0.5 to +3.0	V
Enable Voltage (V_{AT_EN})	-0.5 to +3.0	V
DC Supply Current	1500	mA
Input RF Power	+13	dBm
Duty Cycle at Max Power	37.5	%
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

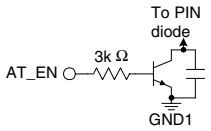
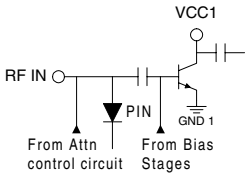
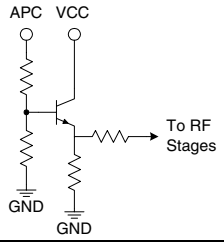
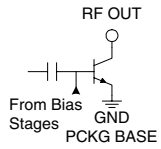
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

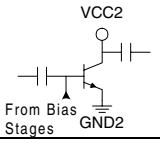
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V, V_{AT_EN}=2.6V, P_{IN}=+6dBm, Freq=1710MHz to 1910MHz, 12.5% Duty Cycle, pulse width=577µs
Operating Frequency Range		1710 to 1785		MHz	See application schematic for tuning details.
		1850 to 1910		MHz	A different tuning is required.
Usable Frequency Range		1700 to 2000		MHz	
Maximum Output Power	+32	+33		dBm	Temp=25°C, V_{CC}=3.5V, $V_{APC1,2}$=2.6V
	+31.5	+32.8		dBm	Temp=+25°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
		+31.5		dBm	Temp=+85°C, V_{CC}=3.2V, $V_{APC1,2}$=2.6V
		+31		dBm	Temp=25°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
	+29.5	+30		dBm	Temp=+85°C, V_{CC}=2.7V, $V_{APC1,2}$=2.6V
Total Efficiency	45	51		%	At $P_{OUT,MAX}$, V_{CC}=3.5V
		51		%	At $P_{OUT,MAX}$, V_{CC}=3.0V
		15		%	P_{OUT}=+20dBm
		10		%	P_{OUT}=+10dBm
Recommended Input Power Range	+5	+7	+9	dBm	
Output Noise Power			-79	dBm	RBW=100kHz, 1805MHz to 1880MHz and 1930MHz to 1990MHz, $P_{OUT,MIN}$<P_{OUT}<$P_{OUT,MAX}$, $P_{IN,MIN}$<P_{IN}<$P_{IN,MAX}$, V_{CC}=3.0V to 5.0V
Forward Isolation		-37	-30	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+9dBm
		-40	-35	dBm	$V_{APC1,2}$=0.2V, P_{IN}=+6dBm
Second Harmonic		-60	-45	dBc	P_{OUT}≤+32.5dBm
Third Harmonic		-65	-50	dBc	
All Other Non-Harmonic Spurious			-36	dBm	
Input Impedance		50		Ω	
Input VSWR			2.2:1		$P_{OUT,MAX}$-5dB<P_{OUT}<$P_{OUT,MAX}$
			3:1		P_{OUT}<$P_{OUT,MAX}$-5dB
Output Load VSWR	10:1				Spurious<-36dBm, $V_{APC1,2}$=0.2V to 2.6V, RBW=3MHz
Output Load Impedance		4.5-j3.9		Ω	Load Impedance presented at RF OUT pin
Power Control					
Power Control "ON"			2.6	V	Maximum P_{OUT}, Voltage supplied to the input
Power Control "OFF"	0.2	0.5		V	Minimum P_{OUT}, Voltage supplied to the input
Attenuator Enable "ON"	2.5	2.6	2.85	V	For maximum isolation when $V_{APC}$is low
Attenuator Enable "OFF"	0.2	0.5		V	For power down mode

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Control Range	62	68		dB	$V_{APC1,2}$=0.2V to 2.6V, V_{AT_EN}=2.6V, P_{IN}=+9dBm
Gain Control Slope		100		dB/V	P_{OUT}=-10dBm to +33dBm
APC Input Capacitance			10	pF	DC to 2MHz
APC Input Current		4.5	5	mA	$V_{APC1,2}$=2.6V
			10	µA	$V_{APC1,2}$=0V
AT_EN Input Current			500	µA	V_{AT_EN}=2.6V, $V_{APC1,2}$=0V
			10	µA	V_{AT_EN}=0V, $V_{APC1,2}$=0V
Turn On/Off Time			100	ns	
Power Supply					
Power Supply Voltage		3.5		V	Specifications
	2.7		4.8	V	Nominal operating limits, P_{OUT}<+33dBm
			5.5	V	With maximum output load VSWR 6:1, P_{OUT}<+33dBm
Power Supply Current		1.3		A	DC Current at $P_{OUT,MAX}$
	50		300	mA	Idle Current, P_{IN}<-30dBm
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V
		1	10	µA	P_{IN}<-30dBm, $V_{APC1,2}$=0.2V, Temp=+85°C

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Pin	Function	Description	Interface Schematic
1	GND	Internally connected to the ground slug.	See pin 15.
2	AT_EN	Control input for the PIN diode. The purpose of the PIN diode is to attenuate the RF input drive level when the V_{APC} is low. This serves both to reduce the leakage through the device cause by self biasing when driving with high level at the RF input, as well as to maintain a good input match when the bias of the input stage is turned off. When this pin is "high" the PIN diode control is turned on. See the Theory of Operation for more details.	
3	RF IN	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 5. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
4	GND1	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance.	See pin 3.
5	VCC1	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	See pin 3.
6	APC1	Power Control for the driver stage and pre-amplifier. When this pin is "low," all circuits are shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. During normal operation this pin is the power control. Control range varies from about 1.0V for -10dBm to 2.6V for +33dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details. The maximum current into this pin is 5mA when V_{APC1}=2.6V, and 0mA when V_{APC}=0V.	
7	APC2	Power Control for the output stage. See pin 6 for more details.	See pin 6.
8	VCC	Power supply for the bias circuits.	See pin 6.
9	GND	Internally connected to the ground slug.	
10	RF OUT	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pin. An external matching network is required to provide the optimum load impedance.	
11	RF OUT	Same as pin 10.	Same as pin 10.
12	RF OUT	Same as pin 10.	Same as pin 10.
13	2F0	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. The bonding wire together with an external capacitor form a series resonator that should be tuned to the second harmonic frequency in order to increase efficiency and reduce spurious outputs.	Same as pin 10.
14	VCC2	Same as pin 15.	

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Pin	Function	Description	Interface Schematic
15	**VCC2**	Power supply for the driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	
16	**VCC2**	Same as pin 15.	Same as pin 15.
Pkg Base	**GND**	Ground connection for the output stage. This pad should be connected to the groundplane by vias directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

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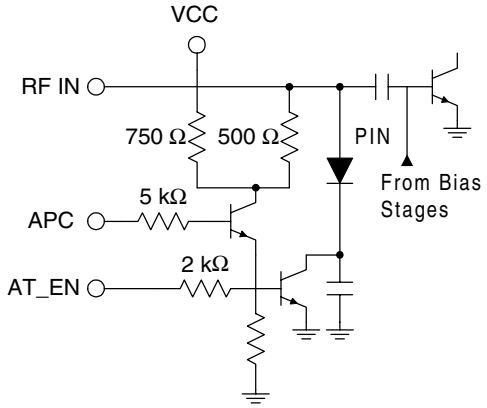
Theory of Operation and Application Information

The RF2174 is a three-stage device with 28 dB gain at full power. Therefore, the drive required to fully saturate the output is +5dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 3V supply to operate to full specification. Power control is provided through a single pin interface, with a separate Power Down control pin. The final stage ground is achieved through the large pad in the middle of the backside of the package. First and second stage grounds are brought out through separate ground pins for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane, and not connected with the output ground to form a so called “local ground plane” on the top layer of the PCB. The output is brought out through the wide output pad, and forms the RF output signal path.

The amplifier operates in near Class C bias mode. The final stage is "deep AB", meaning the quiescent current is very low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 1500mA. The optimum load for the output stage is approximately 4.5Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, vias, and microstrip, and 2 shunt capacitors external to the part. The optimum load impedance at the RF Output pad is 4.5-j3.9Ω. With this match, a 50Ω terminal impedance is achieved. The input is internally matched to 50Ω with just a blocking capacitor needed. This data sheet defines the configuration for GSM operation.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

When the device is driven at maximum input power self biasing would occur. This results in less isolation than one would expect, and the maximum output power would be about -15dBm. If the drive power to the PA is turned on before the GSM ramp-up, higher isolation is required. In order to meet the GSM system specs under those conditions, a PIN diode attenuator connected to the input can be turned on. The figure below shows how the attenuator and its controls are connected.



The current through the PIN diode is controlled by two signals: AT_EN and APC. The AT_EN signal allows current through the PIN diode and is an on/off function. The APC signal controls the amount of current through the PIN diode. Normally, the AT_EN signal will be derived from the VCO ENABLE signal available in most GSM handset designs. If maximum isolation is needed before the ramp-up, the AT_EN signal needs to be turned on before the RF power is applied to the device input. The current into this pin is not critical, and can be reduced to a few hundred micro amps with an external series resistor. Without the resistor, the pin will draw about 700µA.

Because of the inverting stage at the APC input, the current through the PIN diode is inverted from the APC voltage. Thus, when V_{APC} is high for maximum output power, the attenuator is turned off to obtain maximum drive level for the first RF stage. When V_{APC} is low for maximum isolation, the attenuator is be turned on to reduce the drive level and to avoid self-biasing.

The PIN diode is dimensioned such that a low V_{APC} the impedance of the diode is about 50 Ohm. Since the input impedance of the first RF stage become very high when the bias is turned off, this topology will maintain a good input impedance over the entire V_{APC} control range.

VCC1 and VCC2 provide supply voltage to the first and second stage, as well as provides some frequency selectivity to tune to the operating band. Essentially,

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the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be bypassed individually with 100pF capacitors before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RF OUT pin provides the output power. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 1.5A of current required. Care should be taken to keep the losses low in the bias feed and output components. A narrow microstrip line is recommended because DC losses in a bias choke will degrade efficiency and power.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in this data sheet is based on a 12.5% duty cycle and a 600µs pulse, unless specified otherwise.

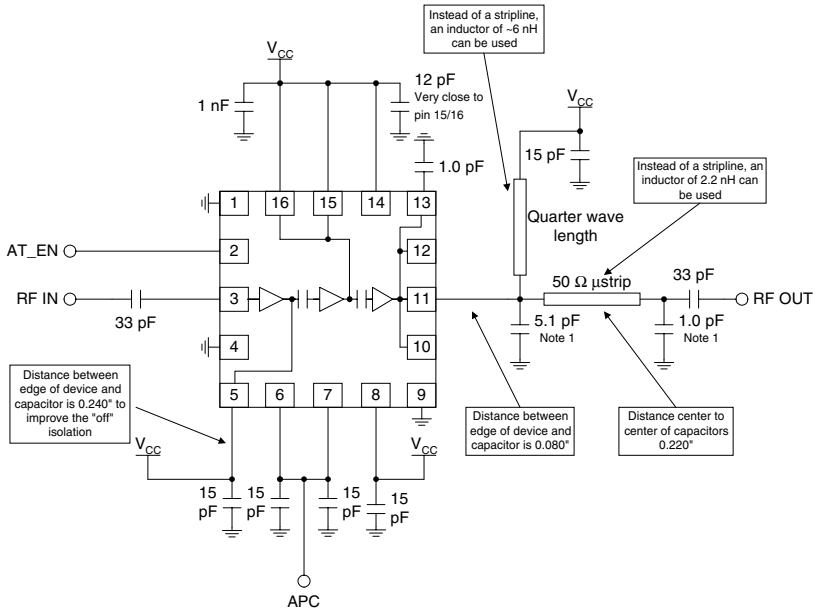
The part will operate over a 3.0V to 5.0V range. Under nominal conditions, the power at 3.5V will be greater than +32dBm at +85°C. As the voltage is increased, however, the output power will increase. Thus, in a system design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This must occur during operation, or the device may be damaged from too much power dissipation. At 5.0V, over +36dBm may be produced; however, this level of power is not recommended, and can cause damage to the device.

The HBT breakdown voltage is >20V, so there is no issue with overvoltage. However, under worst-case conditions, with the RF drive at full power during transmit, and the output VSWR extremely high, a low load impedance at the collector of the output transistors can cause currents much higher than normal. Due to the bipolar nature of the devices, there is no limitation on the amount of current the device will sink, and the safe current densities could be exceeded.

High current conditions are potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2174 includes temperature compensation circuits in the bias network to stabilize the RF transistors, thus limiting the current through the amplifier and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations.

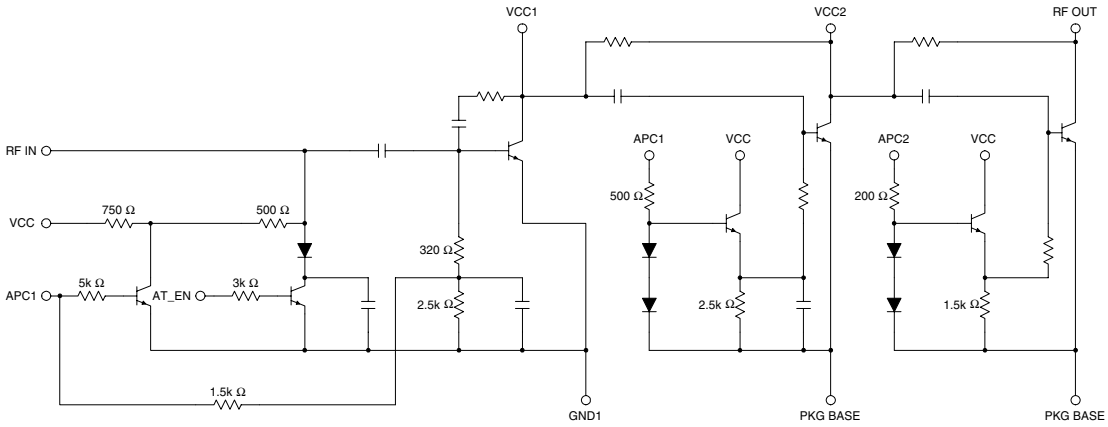
To avoid excessively high currents it is important to control the V_{APC} when operating at supply voltages higher than 4.0V, such that the maximum output power is not exceeded.

Application Schematic



Note: All capacitors are standard 0402 multi layer chip
Note 1: Using a hi-Q capacitor will increase efficiency slightly

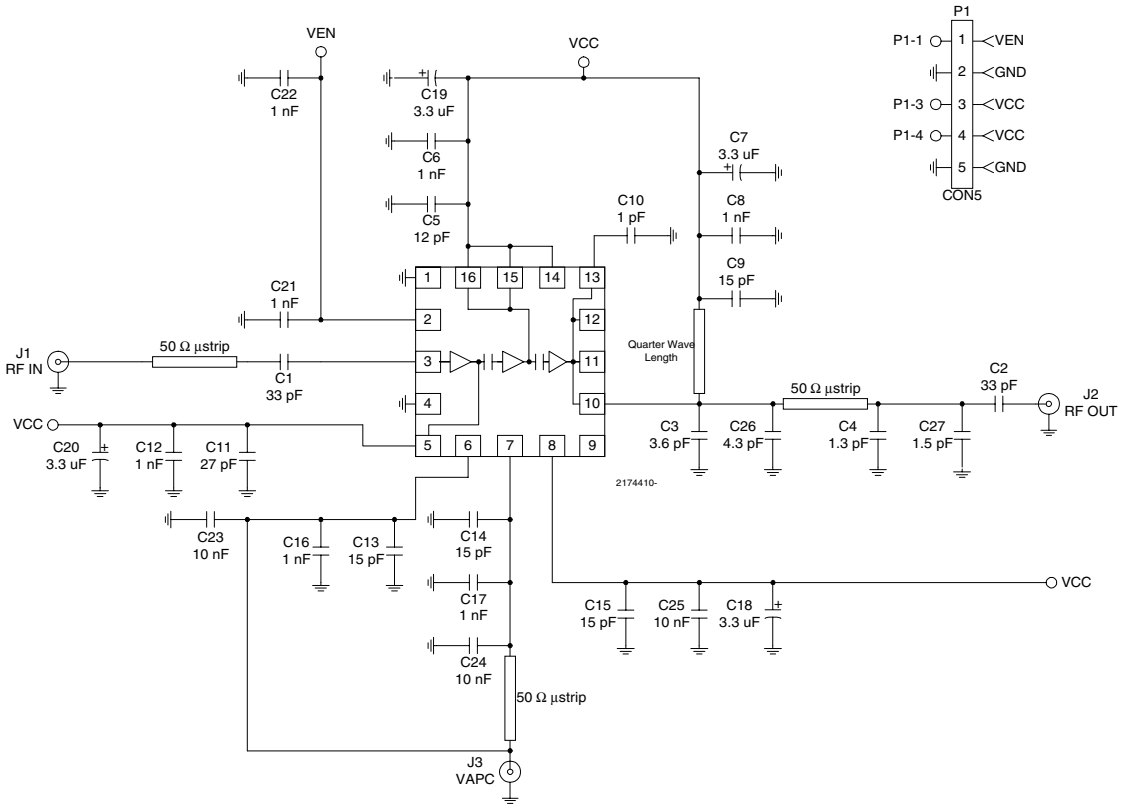
Internal Schematic



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Evaluation Board Schematic

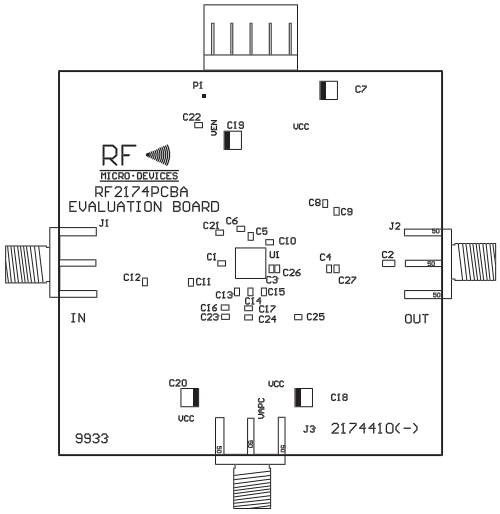
(Download Bill of Materials from www.rfmd.com.)

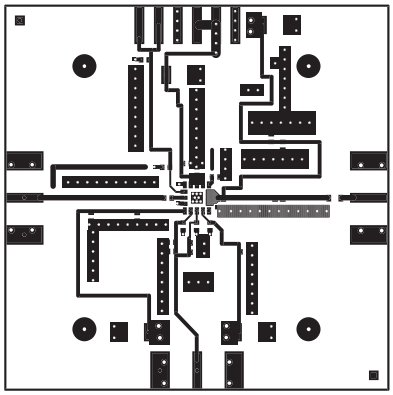


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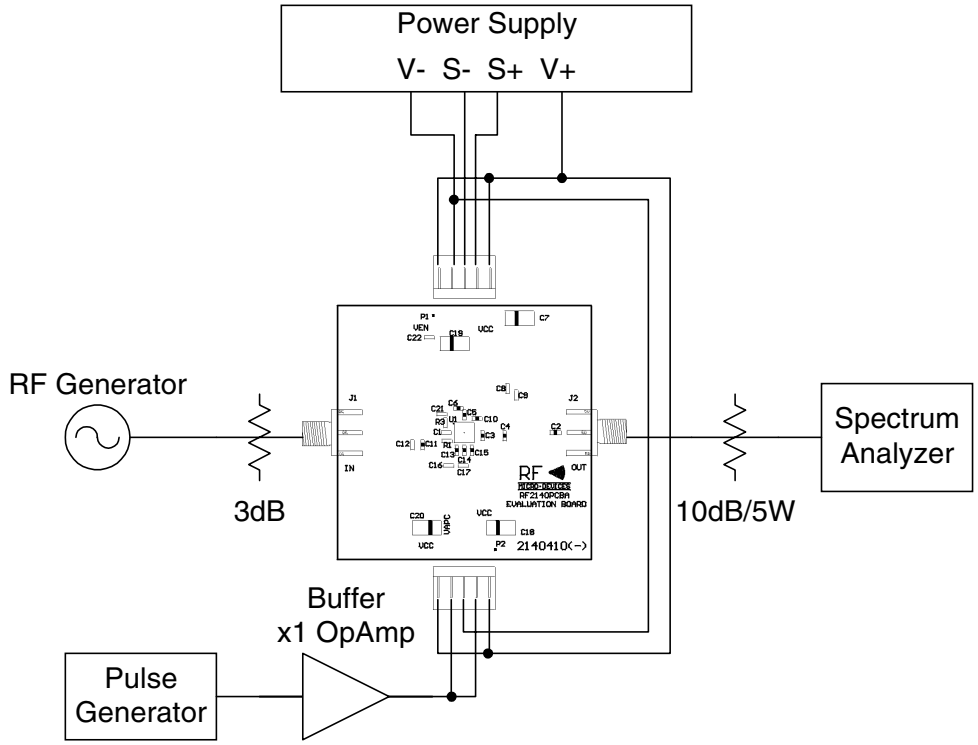
Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.032”; Board Material FR-4; Multi-Layer





Typical Test Setup



A buffer amplifier is recommended because the current into the V_{APC} changes with voltage. As an alternative, the voltage may be monitored with an oscilloscope.

Notes about testing the RF2174

The test setup shown above includes two attenuators. The 3dB pad at the input is to minimize the effects that the switching of the input impedance of the PA has on the signal generator. When V_{APC} is switched quickly, the resulting input impedance change can cause the signal generator to vary its output signal, either in output level or in frequency. Instead of an attenuator an isolator may also be used. The attenuator at the output is to prevent damage to the spectrum analyzer, and should be able to handle the power.

It is important not to exceed the rated supply current and output power. When testing the device at higher than nominal supply voltage, the V_{APC} should be adjusted to avoid the output power exceeding +36dBm. During load-pull testing at the output it is important to monitor the forward power through a directional coupler. The forward power should not exceed +36dBm, and V_{APC} needs to be adjusted accordingly. This simulates the behavior for the power control loop in this respect. To avoid damage, it is recommended to set the power supply to limiting the current during the burst, not to exceed the maximum current rating.

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RF MICRO·DEVICES

Preliminary

RF2175

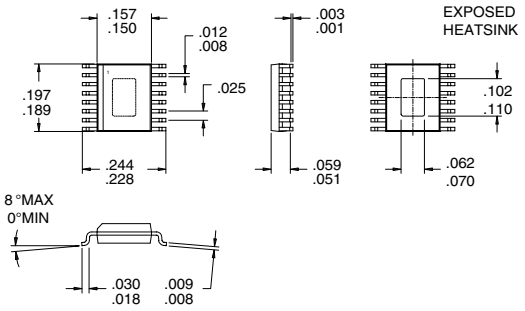
3V 400MHZ LINEAR AMPLIFIER

Typical Applications

- 3V TETRA Cellular Handsets
- 3V CDMA Cellular Handsets
- Portable Battery-Powered Equipment

Product Description

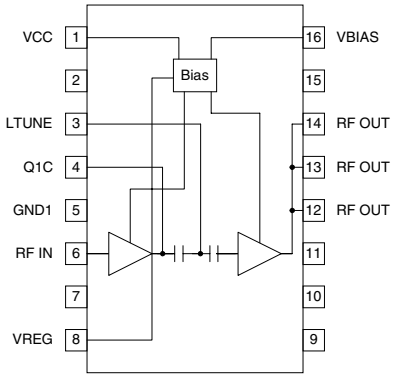
The RF2175 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in TETRA handheld digital cellular equipment, spread spectrum systems, and other applications in the 380MHz to 512MHz band. The RF2175 has an analog bias control voltage to maximize efficiency. The device is self-contained with 50Ω input, and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The package is a small PSSOP-16 plastic with backside ground.



Package Style: PSSOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 30dBm Linear Output Power
- 34.5dB Linear Gain
- 30% Linear Efficiency
- On-Board Power Down Mode
- 380MHz to 512MHz Operation

Ordering Information

RF2175	3V 400MHz Linear Amplifier
RF2175 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF Off)	+8.0	V_{DC}
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V_{DC}
Mode Voltage (V_{MODE})	+5.7	V_{DC}
Control Voltage (V_{PD})	+5.7	V_{DC}
Input RF Power	+5	dBm
Output VSWR - Inband	10:1	
Output VSWR - Out of Band	20:1	
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

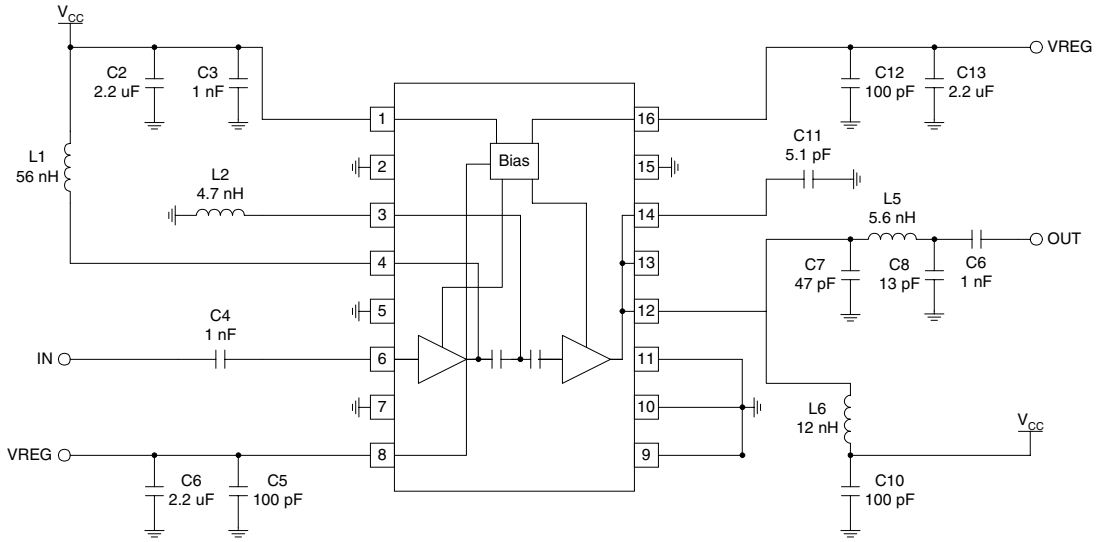
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=410MHz to 420MHz unless otherwise specified, 50% duty cycle.
Usable Frequency Range	380		512	MHz	
Typical Frequency Range		410 to 420		MHz	
Linear Gain	35.5	37.5	39.5	dB	
Second Harmonic (including Second Harmonic Trap)			-40	dBc	
P3dB Output Power		34		dBm	
Maximum Linear Output Power (TETRA Modulation)		30		dBm	
Total Linear Efficiency	25	30		%	
Adjacent Channel Power Rejection	-35			dBc	ACPR@25kHz, TETRA modulation
	-45			dBc	ACPR@50kHz, TETRA modulation
Power Supply					
Power Supply Voltage	3.0	3.6	5.2	V	
Idle Current		230		mA	
V_{REG} Current		820		mA	Total pins 6 and 7, V_{REG}=2.8V
Turn On/Off Time			<100	ns	
Total Current (Power Down)			10	µA	V_{PD}=Low
V_{REG} "Low" Voltage		0	0.2	V	
V_{REG} "High" Voltage	2.7	2.8	2.9	V	
VMODE Bias Control Voltage Range		0 to 2.5		V	

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Pin	Function	Description	Interface Schematic
1	VCC	Power supply for input bias circuitry. A 100 pF high frequency bypass capacitor is recommended.	
2	NC	No Connection.	
3	L TUNE	Interstage Tuning. A shunt inductor to GND is required to optimize the match.	
4	Q1C	Power supply for stage 1. V_{CC} should be fed through a 25nH or greater inductor with a decoupling capacitor on the V_{CC} side.	
5	GND1	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact.	
6	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
7	NC	No Connection.	
8	VREG	Power Down control. When this pin is “low”, all circuits are shut off. When this pin is 2.8V, all circuits are operating normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 100pF high frequency bypass capacitor is recommended.	
9	NC	No Connection.	
10	NC	No Connection.	
11	NC	No Connection.	
12	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
13	RF OUT	Same as pin 12.	
14	RF OUT	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with a shunt capacitor at $2f_0$ is connected to this pin.	
15	NC	No Connection.	
16	VBIAS	The bias pin allows higher efficiency in low power power modes. When operating at full output, VBIAS should be 2.8V.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad, which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

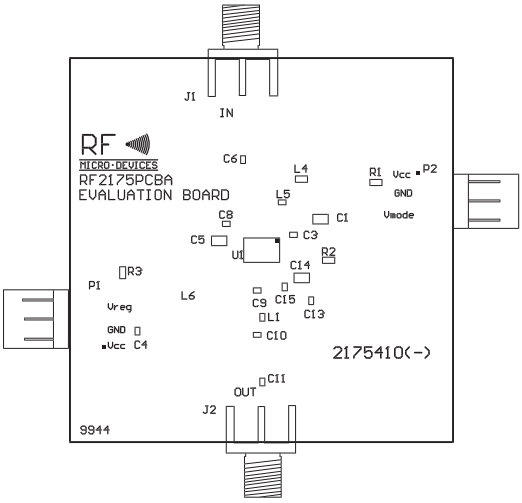
Application Schematic

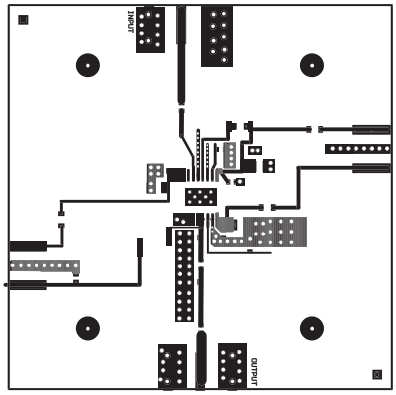


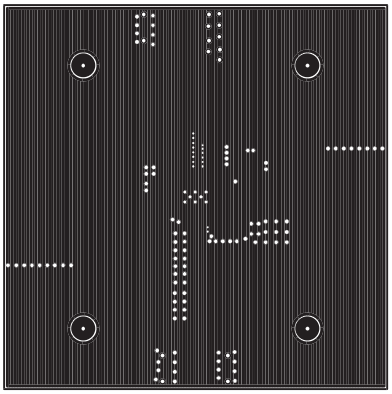
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Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.032”, Board Material FR-4







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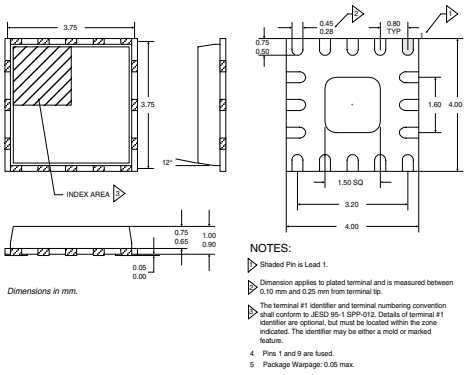
3V, 2.5GHZ LINEAR POWER AMPLIFIER

Typical Applications

- 2.5GHz ISM Band Applications
- PCS Communication Systems
- Wireless LAN Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- Broadband Spread Spectrum Systems

Product Description

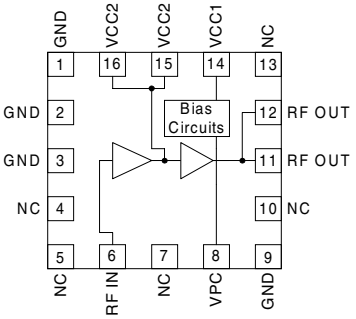
The RF2189 is a linear, medium power, high efficiency amplifier IC designed specifically for low voltage operation. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz spread spectrum transmitters. The device is provided in a 16-pin MLF16 package with a backside ground and is self-contained with the exception of the output matching network and power supply feed line.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MLF16



Functional Block Diagram

Features

- Single 3.3V Power Supply
- +26dBm Saturated Output Power
- 27dB Small Signal Gain
- High Power Added Efficiency
- Power Down Mode
- 1800MHz to 2500MHz Frequency Range

Ordering Information

RF2189	3V, 2.5GHz Linear Power Amplifier
RF2189 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to 3.3	V
DC Supply Current	350	mA
Input RF Power	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture sensitivity	JEDEC Level 3	

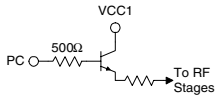
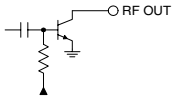
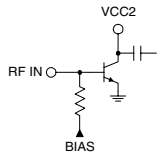
Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

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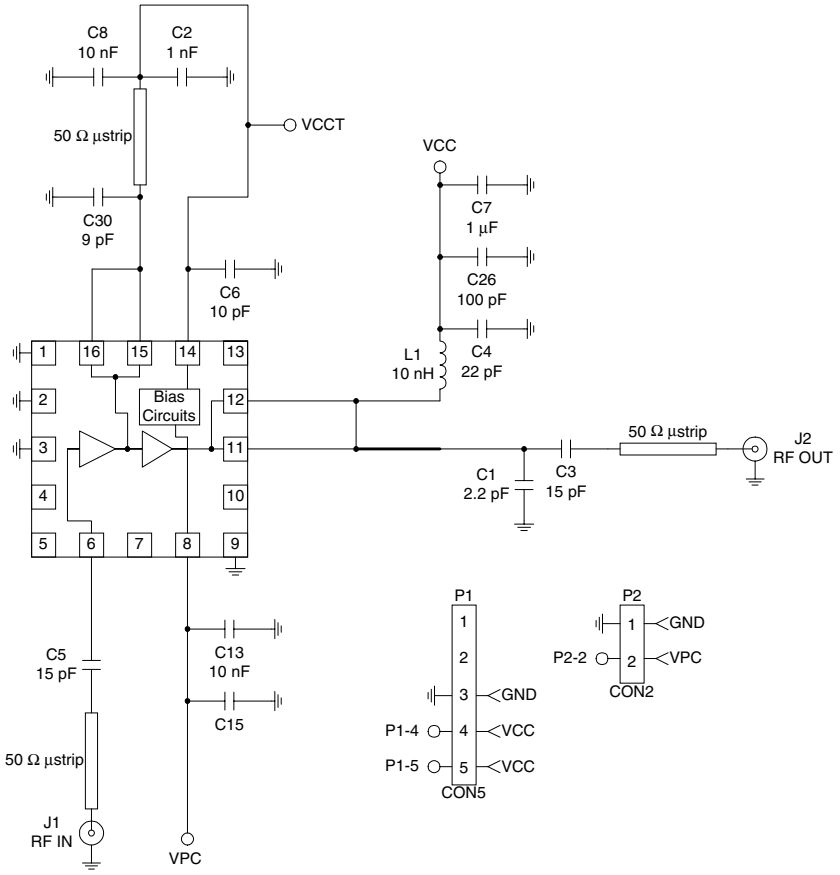
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.3V, V_{PC}=3.0V, P_{IN}=0dBm, Freq=2450MHz
Frequency Range		1800 to 2500		MHz	
Maximum Saturated Output Power	+24.5	+26	+27	dBm	P_{IN}=+6dBm
Efficiency at Max Output Power		42		%	
Small Signal Gain	24.5	26.5		dB	
Reverse Isolation		30		dB	In "ON" state
		30		dB	In "OFF" state
Second Harmonic		-50		dBc	Including second harmonic trap, see application circuit
IM_3		-30	-23		P_{OUT}=+17dBm in each tone
IM_5		-35	-30		P_{OUT}=+17dBm in each tone
IM_7		-48	-35		P_{OUT}=+17dBm in each tone
Isolation	-20	-30		dBm	In "OFF" state, P_{IN}=0dBm
Input Impedance		50		Ω	
Input VSWR		2:1			
Noise Figure		7		dB	
Power Down					
Power Control "ON"	2.7		3.0	V	Voltage supplied to control input; device is "ON"
Power Control "OFF"		0	0.5	V	Voltage supplied to control input; device is "OFF"
PC Input Impedance	5			kΩ	
Power Supply					
Operating Voltage		3.0 to 5.0		V	
Current Consumption	180	260	320	mA	Power Down "ON", at max output power
	95	150	175	mA	Power Down "ON", two-tone test +20dBm average output power
	50	100	150	mA	Idle current
Current Consumption		<1	10	μA	Power Down "OFF"

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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	GND	Same as pin 1.	
4	NC	Not connected.	
5	NC	Not connected.	
6	RF IN	RF input. This input is DC coupled, so an external blocking capacitor is required if this pin is connected to a DC path.	See pin 1.
7	NC	Not connected.	
8	PC	Power control pin. For maximum power this pin should be 3.3V. A higher voltage is not recommended. For less output power and reduced idle current this voltage may be reduced.	
9	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
10	NC	Not internally connected.	
11	RF OUT	RF output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through a quarter-wave length microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC currents.	
12	RF OUT	Same as pin 11.	See pin 11.
13	NC	Not connected.	
14	VCC1	Power supply pin for the bias circuits. External low frequency bypass capacitors should be connected if no other low frequency decoupling is nearby.	See pin 5.
15	VCC2	Bias supply pin for the first stage. A small tuning capacitor is required to set the desired frequency response. External low frequency bypass capacitors should be connected as shown in the application schematic if no other low frequency decoupling is nearby.	
16	VCC2	Connected internally to pin 15.	See pin 15.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	See pin 1 and 6.

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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3 Linear CATV Amplifiers

Part	Description	Frequency (GHz)	Vcc (Volts)	Icc (mA)	Isolation (dB)	Gain (dB)	NF (dB)	P1dB (dBm)	Package	Page
RF2312	Linear General Purpose Amplifier	DC to 2.5	5 to 12	40 to 115	20	15	3.8	+22	SOP-8	3-1
RF2317	Linear CATV Amplifier	DC to 3.0	12to15	100 to 200	20	14.5	4.9	+26	SOP-16 QBW1	3-13
RF2318	Linear Broadband Amplifier	DC to 5.0	9 to 12	50 to 65	15	8	6		SOP-8	3-21
RF2320	Linear General Purpose Amplifier	0.005 to 2.5	6 to 9	75 to 100	20	16	1.6	+22.5	SOP-16BW	3-27
RF2360	Linear General Purpose Amplifier	0.005 to 1.5	6 to 9	100	24	20	1.2	+24	SOP-16BW	3-37

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RF2312

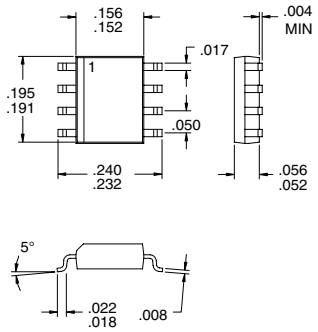
LINEAR GENERAL PURPOSE AMPLIFIER

Typical Applications

- CATV Distribution Amplifiers
- Cable Modems
- Broadband Gain Blocks
- Laser Diode Driver
- Return Channel Amplifier
- Base Stations

Product Description

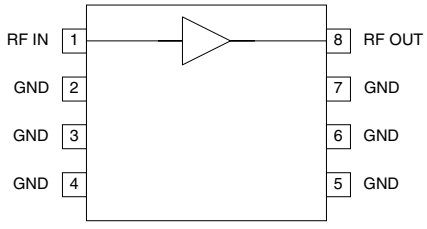
The RF2312 is a general purpose, low cost high linearity RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily cascadable 75Ω gain block. The gain flatness of better than 0.5dB from 5MHz to 1000MHz, and the high linearity, make this part ideal for cable TV applications. Other applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 2500MHz. The device is self-contained with 75Ω input and output impedances, and requires only two external DC biasing elements to operate as specified.



Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to well over 2500MHz Operation
- Internally Matched Input and Output
- 15dB Small Signal Gain
- 3.8dB Noise Figure
- +20dBm Output Power
- Single 5V to 12V Positive Power Supply

Ordering Information

RF2312	Linear General Purpose Amplifier
RF2312 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2312

Absolute Maximum Ratings

Parameter	Rating	Unit
Device Current	125	mA
Input RF Power	+18	dBm
Output Load VSWR	20:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

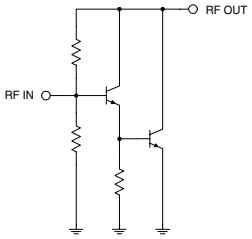
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (50Ω)					T=25 °C, V_{CC}=9V, Freq=900 MHz, R_C=30Ω, 50Ω System, P_{IN}=-4dBm
Frequency Range		DC to 2500		MHz	3dB Bandwidth
Gain	14.5	15.1		dB	
Noise Figure		3.8	4.3	dB	From 50MHz to 300MHz, -30 to +70 °C
		4.2	4.8	dB	From 300MHz to 1000MHz, -30 to +70 °C
Input VSWR			1.7:1		Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output VSWR			1.4:1		Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output IP_3	+40	+42		dBm	At 100MHz
Output IP_3	+33	+36		dBm	At 500MHz
Output IP_3	+30	+33		dBm	At 900MHz
Output P_{1dB}	+21	+22		dBm	At 100MHz
Output P_{1dB}	+20	+21		dBm	At 500MHz
Output P_{1dB}	+17	+18.5		dBm	At 900MHz
Saturated Output Power		+23		dBm	At 100MHz
Saturated Output Power		+22.5		dBm	At 500MHz
Saturated Output Power		+20.5		dBm	At 900MHz
Reverse Isolation		20		dB	
Thermal					
$Theta_{JC}$		73		°C/W	P_{DISS}=0.6W, T_{AMB}=85°C
Maximum junction temperature		138		°C	
Mean Time Between Failures		$1.1x10^6$		years	T_{AMB}=+85°C
Mean Time Between Failures		$3.2x10^3$		years	T_{AMB}=+25°C
Power Supply					
Device Voltage (V_D)		6.0		V	On pin 8, I_{CC}=100mA
		5.0		V	On pin 8, I_{CC}=40mA
Operating Current Range	85	100	115	mA	V_{CC}=9.0V, R_C=30Ω

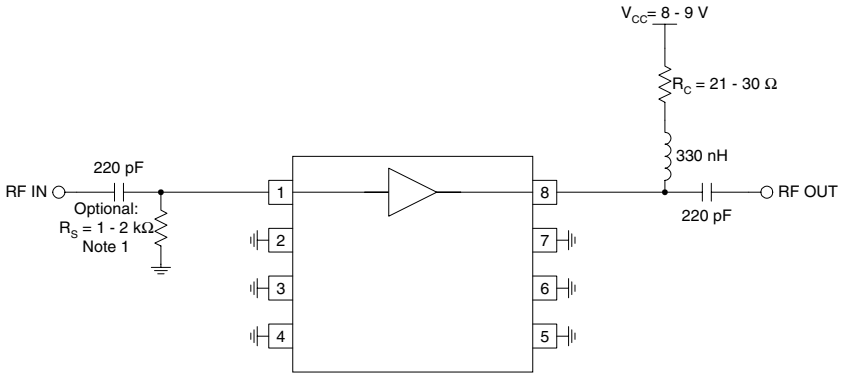
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (75Ω)					T=25 °C, V_{CC}=9V, Freq=900MHz, R_C=30Ω, 75Ω System
Frequency Range		DC to 2500		MHz	3dB Bandwidth
Gain	15.5	16		dB	
Noise Figure		3.8	4.3	dB	From 50MHz to 300MHz, -30 to +70 °C
		4.2	4.8	dB	From 300MHz to 1000MHz, -30 to +70 °C
Input VSWR		1.3:1	1.4:1		From 50MHz to 900MHz, -30 to +70 °C. Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output VSWR			1.25:1		From 50MHz to 300MHz, -30 to +70 °C. Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
			1.4:1		From 300MHz to 500MHz, -30 to +70 °C.
		1.5:1	1.7:1		From 500MHz to 900MHz, -30 to +70 °C.
Output IP_3	+36	+38		dBm	At 100MHz
Output IP_3	+33	+36		dBm	At 500MHz
Output IP_3	+28	+30		dBm	At 900MHz
Output P_{1dB}	+21	+22		dBm	At 100MHz
Output P_{1dB}	+20	+21		dBm	At 500MHz
Output P_{1dB}	+17	+18.5		dBm	At 900MHz
Saturated Output Power		+23		dBm	At 100MHz
Saturated Output Power		+22.5		dBm	At 500MHz
Saturated Output Power		+20.5		dBm	At 900MHz
Reverse Isolation		20		dB	
CATV					110 Channels, 10dBmV/channel at input
CSO		>86		dBc	61.25MHz
		>86		dBc	83.25MHz
		76		dBc	193.25MHz
		70		dBc	313.2625MHz
		64		dBc	547.25MHz
CTB		84		dBc	61.25MHz
		86		dBc	83.25MHz
		85		dBc	193.25MHz
		81		dBc	313.2625MHz
		80		dBc	547.25MHz
Cross Modulation		77		dBc	61.25MHz
		74		dBc	445.25MHz
CNR	65	66		dB	
					77 Channels to 550MHz at 10dBmV, 33 channels to 760MHz at 0dBmV flat at DUT input
CSO		>86		dBc	61.25MHz
		>86		dBc	83.25MHz
		76		dBc	193.25MHz
		72		dBc	313.2625MHz
		64		dBc	547.25MHz
CTB		>86		dBc	61.25MHz
		>86		dBc	83.25MHz
		86		dBc	193.25MHz
		84		dBc	313.2625MHz
		83		dBc	547.25MHz
CNR	65	66		dB	

RF2312

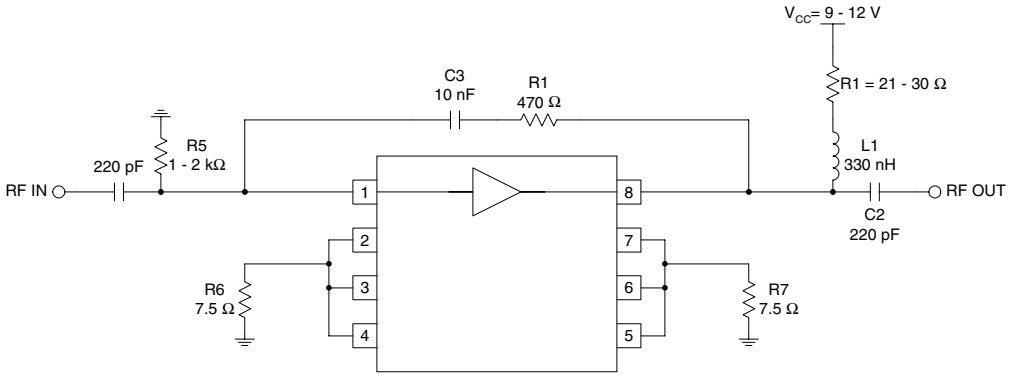
Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in all applications. The device has internal feedback, and not using a DC blocking capacitor will disable the temperature compensation.The bias of the device can be controlled by this pin. Adding an optional 1kΩ resistor to ground on this pin reduces the bias level, which may be compensated for by a higher supply voltage to maintain the appropriate bias level. The net effect of this is an increased output power capability, as well as higher linearity for signals with high crest factors. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Each ground pin should have a via to the ground plane.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output and bias pin. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. For biasing, an RF choke in series with a resistor is needed. The value for the resistor R_C is 30Ω (0.5W) for V_{CC}=9V and 21Ω for V_{CC}=8V. The DC voltage on this pin is typically 6.0V with a current of 100mA. In lower power applications the value of R_C can be increased to lower the current and V_D on this pin.	

Application Schematic
5MHz to 50MHz Reverse Path



NOTE 1:
Optional resistor R_S can be used to maintain the correct bias level at higher supply voltages. This is useful to increase output capability or linearity for signals with high crest factors.

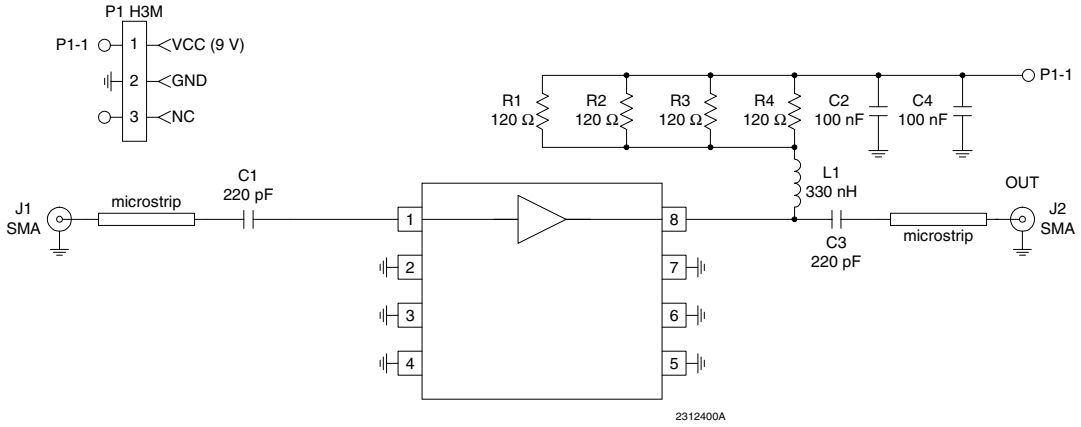
Application Schematic
10dB Gain



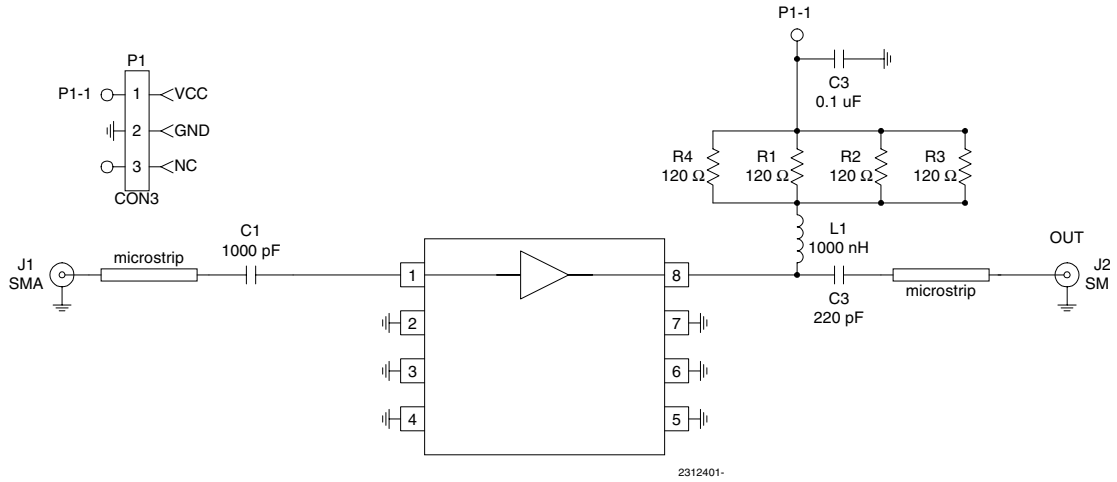
R5 is used to maintain the correct bias level at higher supply voltages and is also required in this configuration. The RC feedback network of R1 and C3 should be kept physically as short as possible. R1 can be adjusted as required to improve the input and output impedance matching. R6 and R7 reduce the typical gain by increasing the emitter resistance. L1 should be at least 200 Ω reactive at the lowest operating frequency. C1 and C2 should be less than 10 Ω at the lowest operating frequency.

Evaluation Board Schematic - 50Ω

(Download Bill of Materials from www.rfmd.com.)



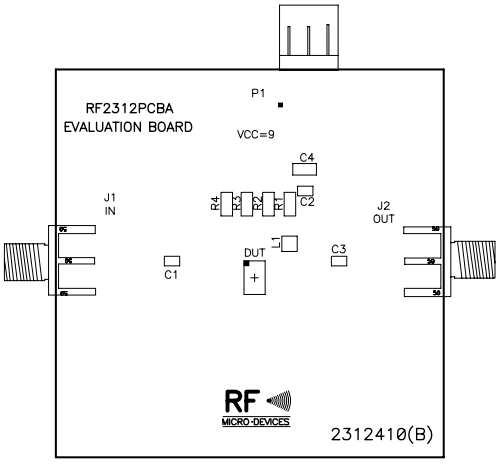
Evaluation Board Schematic - 75Ω

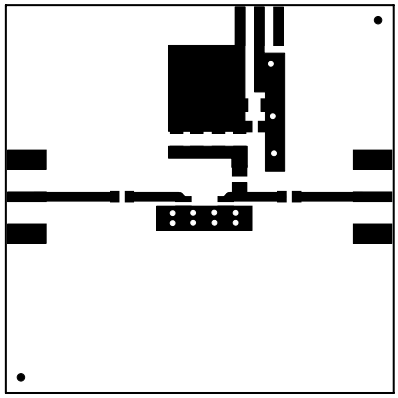


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Evaluation Board Layout - 50Ω
2.02" x 2.02"

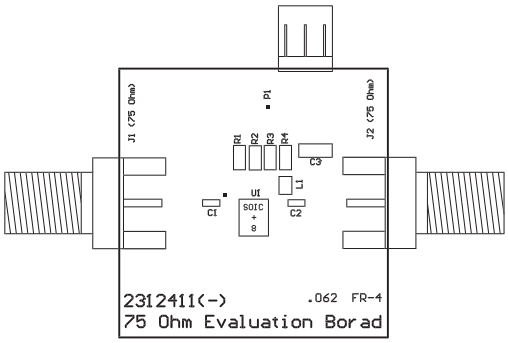
Board Thickness 0.031", Board Material FR-4

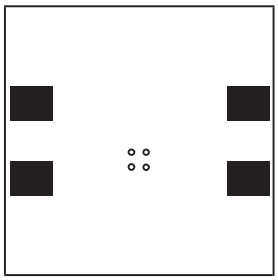




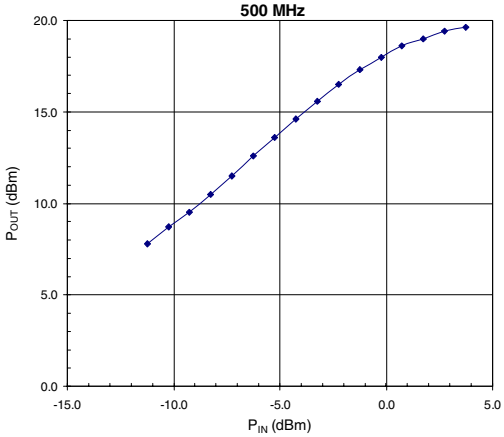
Evaluation Board Layout - 75Ω
2.02" x 2.02"

Board Thickness 0.062", Board Material FR-4

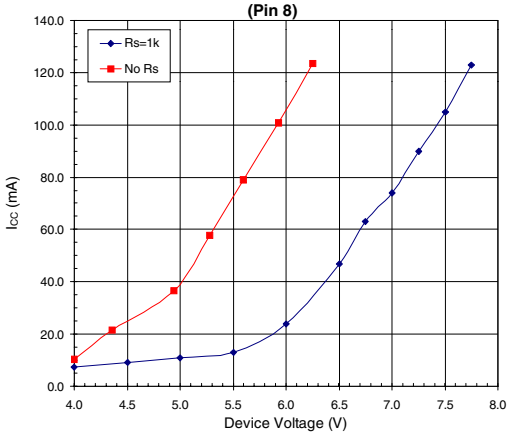




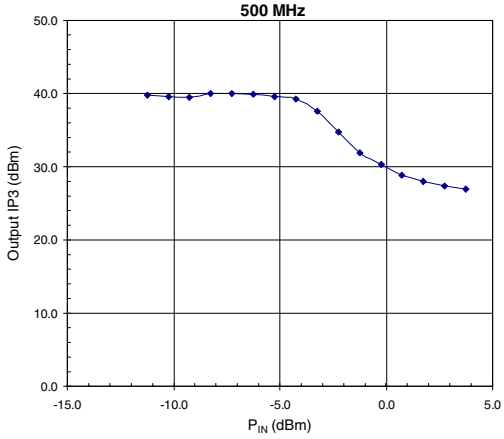
P_{OUT} versus P_{IN}
500 MHz



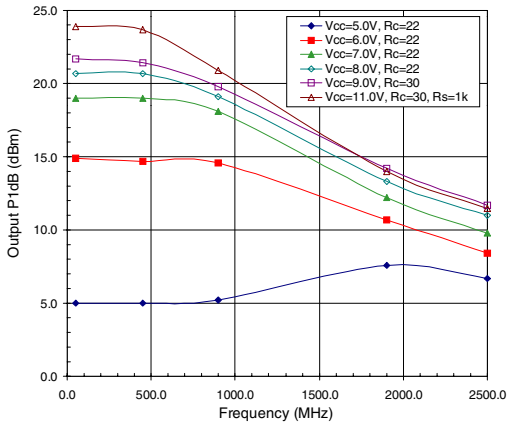
I_{CC} versus Device Voltage
(Pin 8)



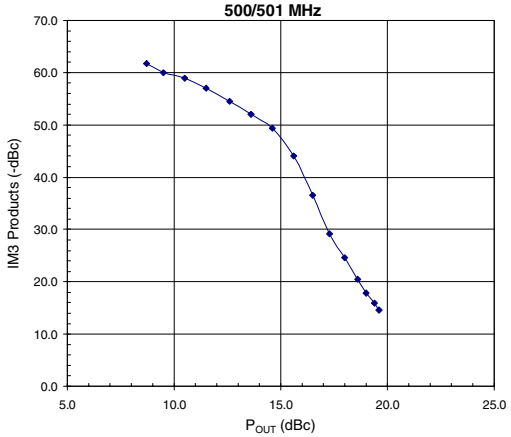
Output Third Order Intercept Point (OIP3) versus P_{IN}
500 MHz



Output P1dB versus Frequency

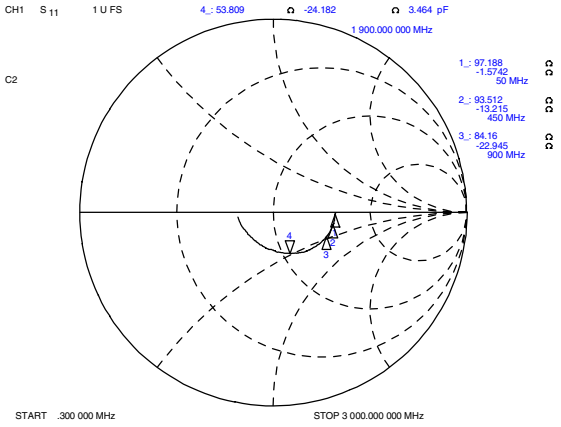


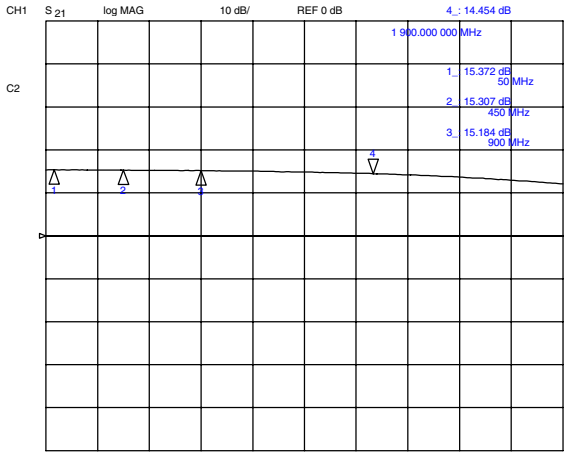
IM3 Products versus P_{OUT}
500/501 MHz

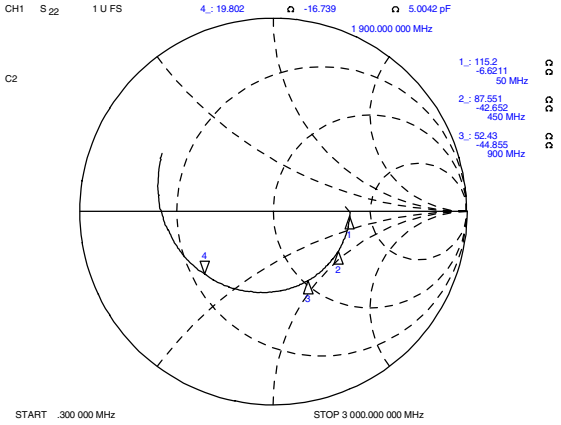


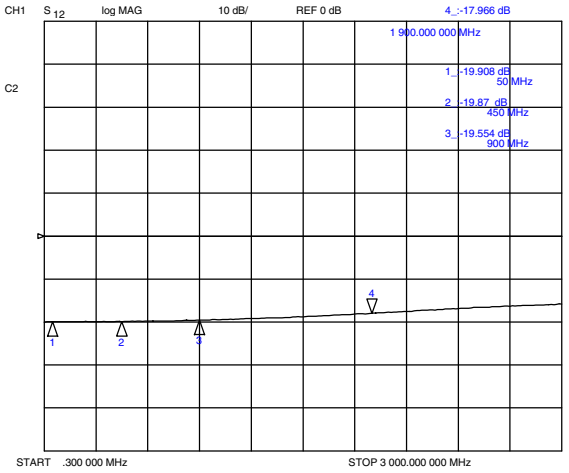
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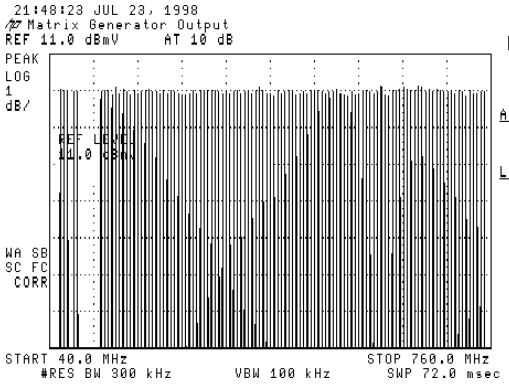
LINEAR CATV AMPLIFIERS

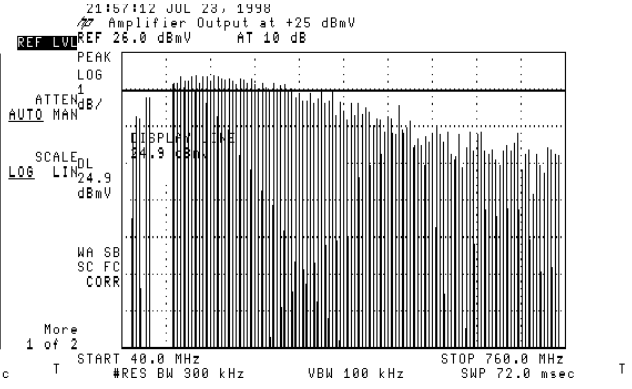

CH1 S 11 1 U FS
4_: 53.809 -24.182 3.464 pF
1 900.000 000 MHz
1_: 97.188 -1.5742 50 MHz
2_: 93.512 -13.215 450 MHz
3_: 84.16 -22.945 900 MHz
C2
START .300 000 MHz
STOP 3 000.000 000 MHz


CH1 S 21 log MAG 10 dB/ REF 0 dB
4_: 14.454 dB
1 900.000 000 MHz
1_: 15.372 dB 50 MHz
2_: 15.307 dB 450 MHz
3_: 15.184 dB 900 MHz
C2
START .300 000 MHz
STOP 3 000.000 000 MHz

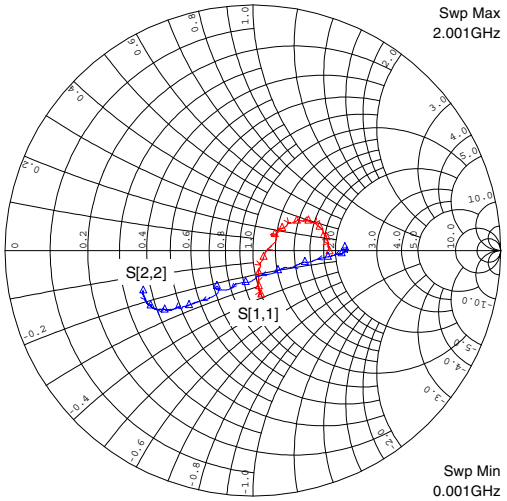

CH1 S 22 1 U FS
4_: 19.802 -16.739 5.0042 pF
1 900.000 000 MHz
1_: 115.2 -6.6211 50 MHz
2_: 87.551 -42.652 450 MHz
3_: 52.43 -44.855 900 MHz
C2
START .300 000 MHz
STOP 3 000.000 000 MHz


CH1 S 12 log MAG 10 dB/ REF 0 dB
4_: -17.966 dB
1 900.000 000 MHz
1_: -19.908 dB 50 MHz
2_: -19.87 dB 450 MHz
3_: -19.554 dB 900 MHz
C2
START .300 000 MHz
STOP 3 000.000 000 MHz

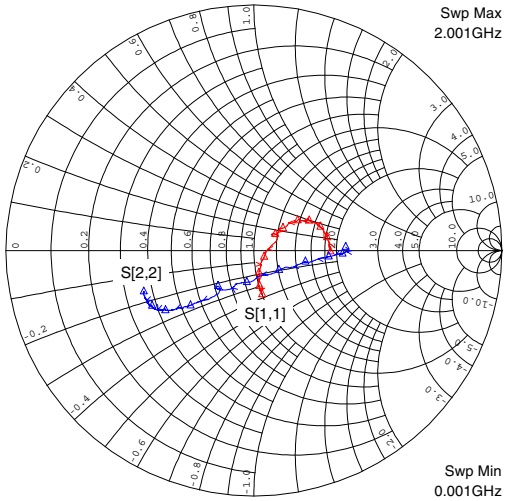

21:48:23 JUL 23, 1998
Matrix Generator Output
REF 11.0 dBmV AT 10 dB
PEAK
LOG
1
dB/
REF LEVEL
11.0 dBmV
WA SB
SC FC
CORR
START 40.0 MHz
STOP 760.0 MHz
#RES BW 300 kHz
VBW 100 kHz
SWP 72.0 msec


21:57:12 JUL 23, 1998
Amplifier Output at +25 dBmV
REF 26.0 dBmV AT 10 dB
REF LVL
PEAK
LOG
1
dB/
ATTEN
AUTO MAN
SCALE
LOG LIN
DISPLAY LVL
24.9 dBmV
WA SB
SC FC
CORR
More
1 of 2
START 40.0 MHz
STOP 760.0 MHz
#RES BW 300 kHz
VBW 100 kHz
SWP 72.0 msec

75 Ohms, ICC = 100 mA, Temp = 25°C



75 Ohms, ICC = 110 mA, Temp = 25°C



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RF2317

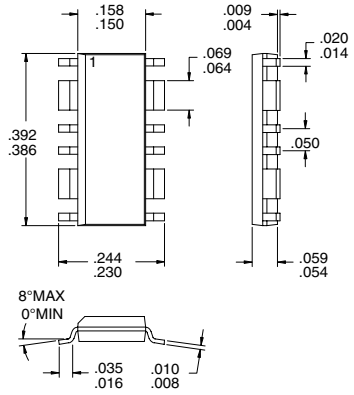
LINEAR CATV AMPLIFIER

Typical Applications

- CATV Distribution Amplifiers
- Cable Modems
- Broadband Gain Blocks
- Laser Diode Driver
- Return Channel Amplifier
- Base Stations

Product Description

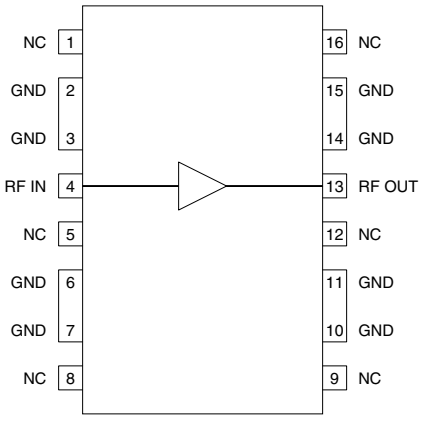
The RF2317 is a general purpose, low cost high linearity RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily cascadable 75Ω gain block. The gain flatness of better than ±0.4dB from 50MHz to 1000MHz, and the high linearity, make this part ideal for cable TV applications. Other applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 3GHz. The device is self-contained with 75Ω input and output impedances and requires only two external DC biasing elements to operate as specified.



Package Style: SOP-16 QBW1

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to 3.0GHz Operation
- Internally Matched Input and Output
- 15dB Small Signal Gain
- 4.9dB Noise Figure
- +26dBm Output Power
- Single 9V to 12V Power Supply

Ordering Information

RF2317	Linear CATV Amplifier
RF2317 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2317

Absolute Maximum Ratings

Parameter	Rating	Unit
Device Current	250	mA
Input RF Power	+18	dBm
Output Load VSWR	20:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

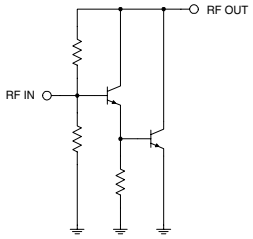
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (50Ω)					T=25 °C, I_{CC}=180mA, R_C=11Ω, 50Ω System
Frequency Range		DC to 3000		MHz	3dB Bandwidth
Gain	14.0	14.5		dB	
Noise Figure		4.9		dB	From 100MHz to 1000MHz
Input VSWR		1.7			Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output VSWR		2.2			Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output IP_3				dBm	At 100MHz
Output IP_3		+42		dBm	At 500MHz
Output IP_3				dBm	At 900MHz
Output IP_2		+63		dBm	F_1=400MHz, F_2=500MHz, F_{OUT}=100MHz
Output P_{1dB}				dBm	At 100MHz
Output P_{1dB}		+26		dBm	At 500MHz
Output P_{1dB}				dBm	At 900MHz
Saturated Output Power				dBm	At 100MHz
Saturated Output Power		+27		dBm	At 500MHz
Saturated Output Power				dBm	At 900MHz
Reverse Isolation		20		dB	
Thermal					
$Theta_{JC}$		47		°C/W	I_{CC}=150mA, P_{DISS} =1.3W, T_{AMB}=85°C
Maximum junction temperature		153		°C	
Mean Time Between Failures		$8.6x10^2$		years	T_{AMB}=+85°C
Mean Time Between Failures		$1.8x10^5$		years	T_{AMB}=+25°C
$Theta_{JC}$		54		°C/W	I_{CC}=180mA, P_{DISS} =1.7W, T_{AMB}=85°C
Maximum Junction Temperature		177		°C	
Mean Time Between Failures		99		years	T_{AMB}=+85°C
Mean Time Between Failures		$9.4x10^3$		years	T_{AMB}=+25°C
Power Supply					
Device Voltage		8.3		V	On pin 13, I_{CC}=150mA
Device Voltage		8.7		V	On pin 13, I_{CC}=180mA
Operating Current Range	100		200	mA	Actual current determined by V_{CC} and R_S

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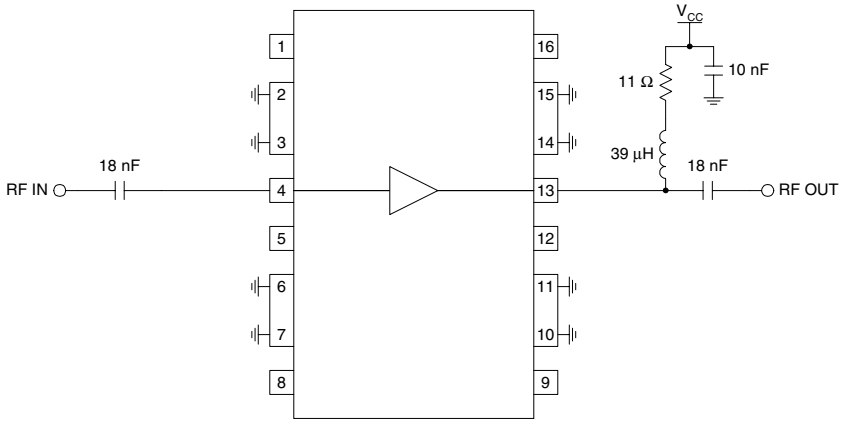
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (75Ω)					T=25°C, I_{CC}=180mA, R_C=11Ω, 75Ω System
Frequency Range		DC to 3000		MHz	3dB Bandwidth
Gain	14.5	15.0		dB	
Noise Figure		5.3		dB	From 100MHz to 1000MHz
Input VSWR		1.1:1			Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output VSWR		1.5:1			Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output IP_3				dBm	At 100MHz
Output IP_3		+42		dBm	At 500MHz
Output IP_3				dBm	At 900MHz
Output IP_2		+63		dBm	F_1=400MHz, F_2=500MHz, F_{OUT}=100MHz
Output P_{1dB}				dBm	At 100MHz
Output P_{1dB}		+26		dBm	At 500MHz
Output P_{1dB}				dBm	At 900MHz
Saturated Output Power				dBm	At 100MHz
Saturated Output Power		+27		dBm	At 500MHz
Saturated Output Power				dBm	At 900MHz
Reverse Isolation		20		dB	
79 Channels					10dBmV per channel, flat, at the input of the amplifier; I_{CC}=150mA, V_{CC}=10.6V
XMOD		-110		dBc	At 55.25MHz
		-78		dBc	At 331.25MHz
		-75		dBc	At 547.25MHz
CTB		-88		dBc	At 55.25MHz
		-88		dBc	At 331.25MHz
		-88		dBc	At 547.25MHz
CSO+1.25MHz		-93		dBc	At 55.25MHz
		-78		dBc	At 331.25MHz
		-70		dBc	At 547.25MHz
CSO-1.25MHz		-68		dBc	At 55.25MHz
		-78		dBc	At 331.25MHz
		-85		dBc	At 547.25MHz
110 Channels					10dBmV per channel, flat, at the input of the amplifier; I_{CC}=150mA, V_{CC}=10.6V
XMOD		-91		dBc	At 55.25MHz
		-77		dBc	At 331.25MHz
		-75		dBc	At 547.25MHz
CTB		-86		dBc	At 55.25MHz
		-85		dBc	At 331.25MHz
		-85		dBc	At 547.25MHz
CSO+1.25MHz		-92		dBc	At 55.25MHz
		-78		dBc	At 331.25MHz
		-71		dBc	At 547.25MHz
CSO-1.25MHz		-63		dBc	At 55.25MHz
		-68		dBc	At 331.25MHz
		-81		dBc	At 547.25MHz

RF2317

Pin	Function	Description	Interface Schematic
1	NC	This pin is internally not connected.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Each ground pin should have a via to the ground plane.	
3	GND	Same as pin 2.	
4	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
5	NC	This pin is internally not connected.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	NC	This pin is internally not connected.	
9	NC	This pin is internally not connected.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	NC	This pin is internally not connected.	
13	RF OUT	RF output and bias pin. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. For biasing, an RF choke in series with a resistor is needed. The DC voltage on this pin is typically 8.3V with a current of 150mA. See device voltage versus device current plot. In lower power applications the value of R_C can be increased to lower the current and V_D on this pin.	
14	GND	Same as pin 2.	
15	GND	Same as pin 2.	
16	NC	This pin is internally not connected.	

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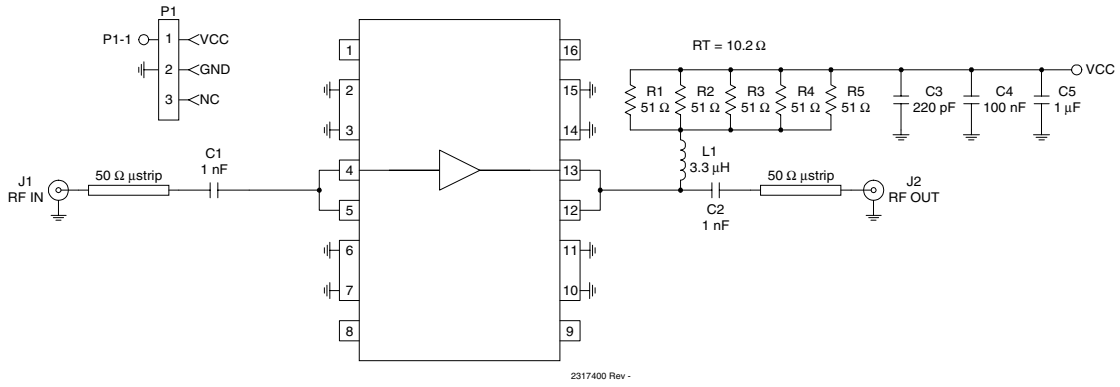
Application Schematic
5MHz to 50MHz Reverse Path



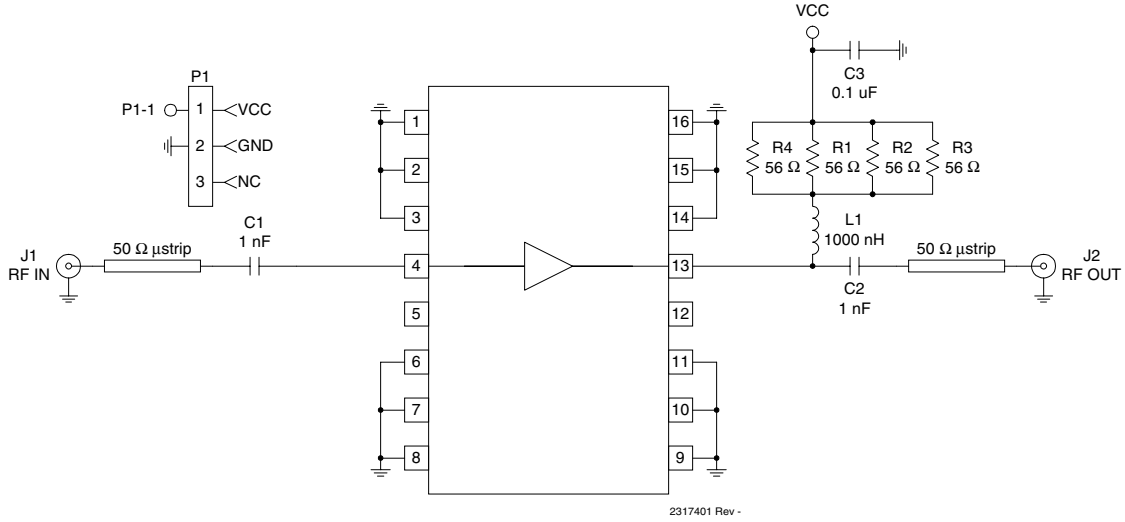
NOTES:
Gain Flatness <0.5 dB
Input and Output Return Loss >20 dB in 75 Ω system

Evaluation Board Schematic - 50 Ω

(Download Bill of Materials from www.rfmd.com.)

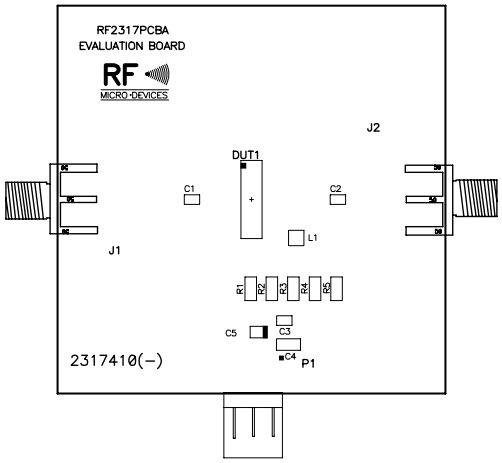


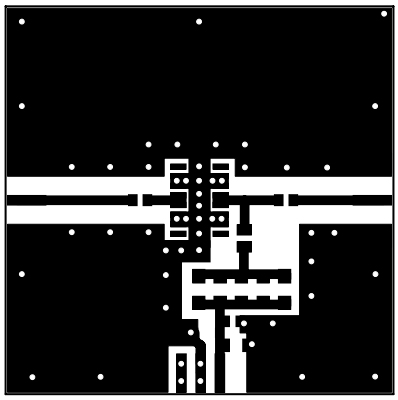
Evaluation Board Schematic - 75 Ω



Evaluation Board Layout - 50 Ω
2" x 2"

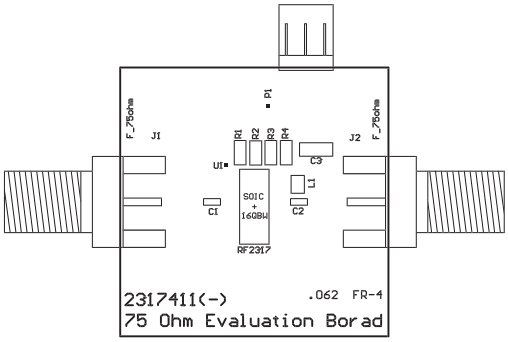
Board Thickness 0.031", Board Material FR-4

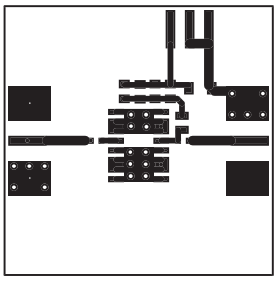




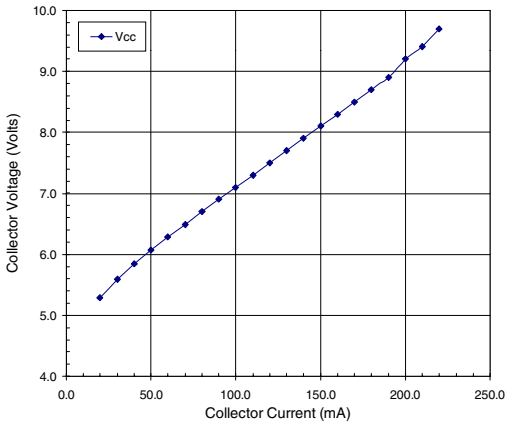
Evaluation Board Layout - 75 Ω
1.40" x 1.40"

Board Thickness 0.062", Board Material FR-4

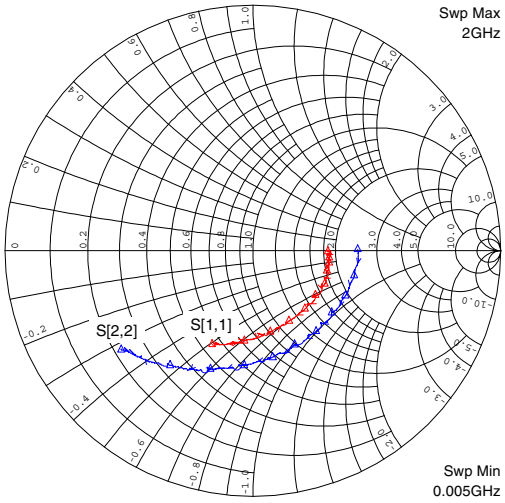




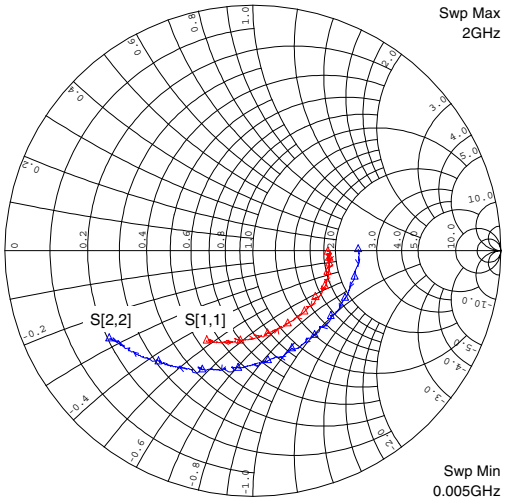
Collector Voltage versus Current



75 Ohms, ICC = 150 mA, Temp = 25°C



75 Ohms, ICC = 180 mA, Temp = 25°C



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RF MICRO·DEVICES

Preliminary

RF2318

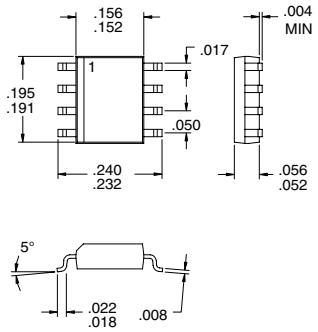
LINEAR BROADBAND AMPLIFIER

Typical Applications

- CATV Amplifiers
- Cable Modems
- Broadband Gain Blocks
- Return Channel Amplifier
- Base Stations

Product Description

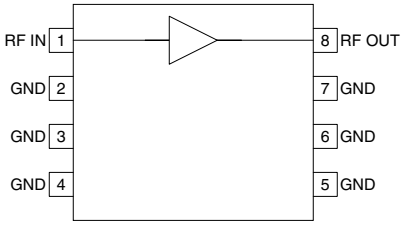
The RF2318 is a broadband general purpose, low cost high linearity RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily cascadable 75Ω gain block. The gain flatness of better than 1.0dB from 5MHz to 1000MHz, and the high linearity, make this part ideal for cable TV applications. Other applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 5000MHz. The device is self-contained with 75Ω input and output impedances, and requires only two external DC biasing elements to operate as specified.



Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to over 5000MHz Operation
- Internally Matched Input and Output
- 8dB Small Signal Gain
- 6dB Noise Figure
- +18dBm Output Power
- Single 9V to 12V Positive Power Supply

Ordering Information

RF2318	Linear Broadband Amplifier
RF2318 PCBA-L	Fully Assembled Evaluation Board (DC to 3GHz)
RF2318 PCBA-H	Fully Assembled Evaluation Board (3GHz to 6GHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Device Current	70	mA
Input RF Power	+13	dBm
Output Load VSWR	20:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

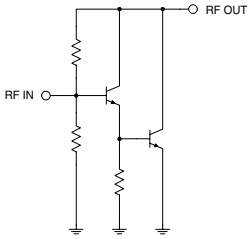
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (50Ω)					T=27°C, V_{CC}=9V, Icc=60mA, R_C=30Ω
Frequency Range		DC to 5000		MHz	1dB Bandwidth
Gain	8	8	9	dB	From 10MHz to 1000MHz
	8	9	10	dB	From 1000MHz to 2000MHz
	10	11	12	dB	From 2000MHz to 5000MHz
Noise Figure		6		dB	From 50MHz to 300MHz, -30°C to +70°C
		6		dB	From 300MHz to 1000MHz, -30°C to +70°C
Input VSWR		1.6:1	1.9:1		From 10MHz to 1800MHz
			1.4:1		From 1800MHz to 5000MHz
					Appropriate values for the DC blocking capacitors and bias inductor are required to maintain these VSWRs at the intended operating frequency range.
Output VSWR		2.0:1	3.0:1		From 10MHz to 1800MHz
			1.9:1		From 1800MHz to 4000MHz
			3.0:1		From 4000MHz to 5000MHz
					Appropriate values for the DC blocking capacitors and bias inductor are required to maintain these VSWRs at the intended operating frequency range.
Output IP_2		+50		dBm	Tones at 500MHz and 900MHz
Output IP_3	+30			dBm	At 100MHz
	+33	+35		dBm	At 500MHz
	+30	+33		dBm	At 900MHz
Output P_{1dB}		TBD		dBm	At 100MHz
		TBD		dBm	At 500MHz
		TBD		dBm	At 900MHz
Saturated Output Power		TBD		dBm	At 100MHz
Saturated Output Power		18		dBm	At 500MHz
Saturated Output Power		TBD		dBm	At 900MHz
Reverse Isolation		15		dB	From 30MHz to 4000MHz
			20	dB	From 4000MHz to 5000MHz
Power Supply					
Device Voltage (V_D)		7.0		V	On pin 8, I_{CC}=63mA
		6.5		V	On pin 8, I_{CC}=49mA
Operating Current Range		63	65	mA	V_D=7.0V

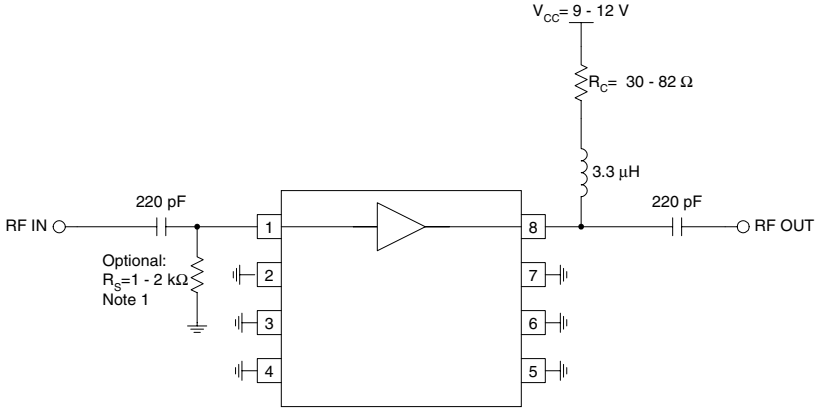
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (75Ω)					T=25°C, V_{CC}=9V, Icc=63mA, R_C=30Ω, 75Ω System
Frequency Range		DC to 5000		MHz	1dB Bandwidth
Gain		8		dB	
Noise Figure		6		dB	From 30MHz to 2000MHz, -30°C to +70°C
Input VSWR		1.3:1			From 30MHz to 2000MHz, -30°C to +70°C
		1.4:1			From 2000MHz to 4000MHz
		1.6:1			From 4000MHz to 5000MHz Appropriate values for the DC blocking capacitors and bias inductor are required to maintain these VSWRs at the intended operating frequency range.
Output VSWR		2.0:1			From 30MHz to 1000MHz, -30°C to +70°C
			2.6:1		From 1000MHz to 5000MHz Appropriate values for the DC blocking capacitors and bias inductor are required to maintain these VSWRs at the intended operating frequency range.
Output IP_2		+54		dBm	Tones at 500MHz and 900MHz
Output IP_3		TBD		dBm	At 100MHz
	+36	+37		dBm	At 500MHz
		TBD		dBm	At 900MHz
Output P_{1dB}		TBD		dBm	At 100MHz
		18		dBm	At 500MHz
		18		dBm	At 900MHz
Saturated Output Power		TBD		dBm	At 100MHz
		19		dBm	At 500MHz
		18.5		dBm	At 900MHz
Reverse Isolation		15		dB	From 30MHz to 4000MHz
			20	dB	From 4000MHz to 5000MHz
CSO		TBD		dB	77 Channels, 36dBmV output/channel
		TBD		dB	110 Channels, 36dBmV output/channel
CTB		TBD		dB	77 Channels, 36dBmV output/channel
		TBD		dB	110 Channels, 36dBmV output/channel
Cross Modulation		TBD		dB	77 Channels, 36dBmV output/channel
		TBD		dB	110 Channels, 36dBmV output/channel

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in all applications. The device has internal feedback, and not using a DC blocking capacitor will disable the temperature compensation.The bias of the device can be controlled by this pin. Adding an optional 1kΩ resistor to ground on this pin reduces the bias level, which may be compensated for by a higher supply voltage to maintain the appropriate bias level. The net effect of this is an increased output power capability, as well as higher linearity for signals with high crest factors. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Each ground pin should have a via to the ground plane.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output and bias pin. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. For biasing, an RF choke in series with a resistor is needed. The value for the resistor R_C is 30Ω (0.5W) for V_{CC}=9V and 82Ω for V_{CC}=12V. The DC voltage on this pin is typically 7V with a current of 63mA. In lower power applications the value of R_C can be increased to lower the current and V_D on this pin.	

Application Schematic

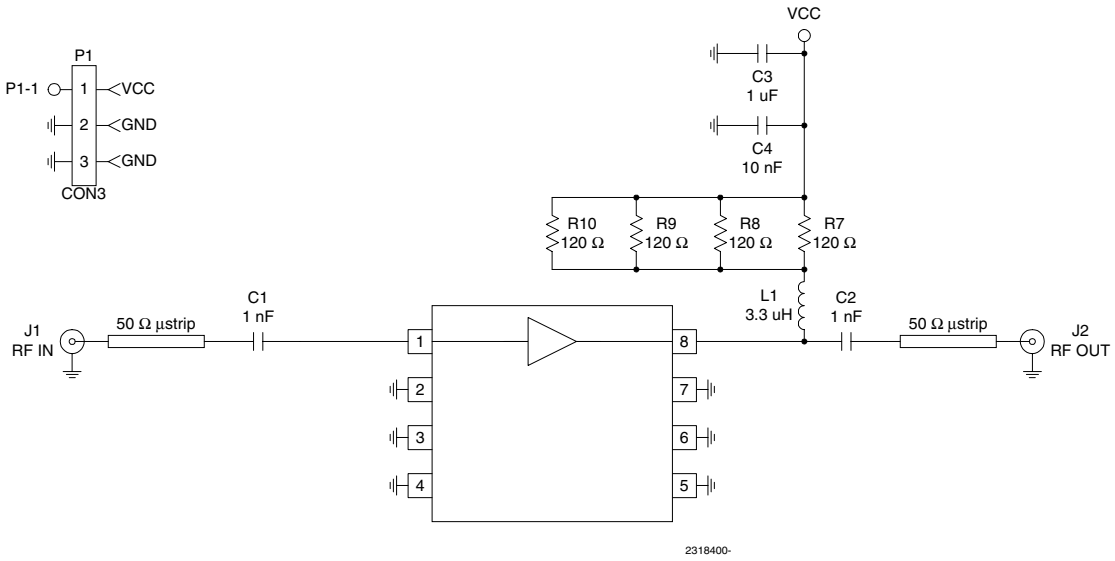


Note 1:
Optional resistor Rs can be used to maintain the correct bias level at higher supply voltages. This is useful to increase output capability or linearity for signals with high crest factors.

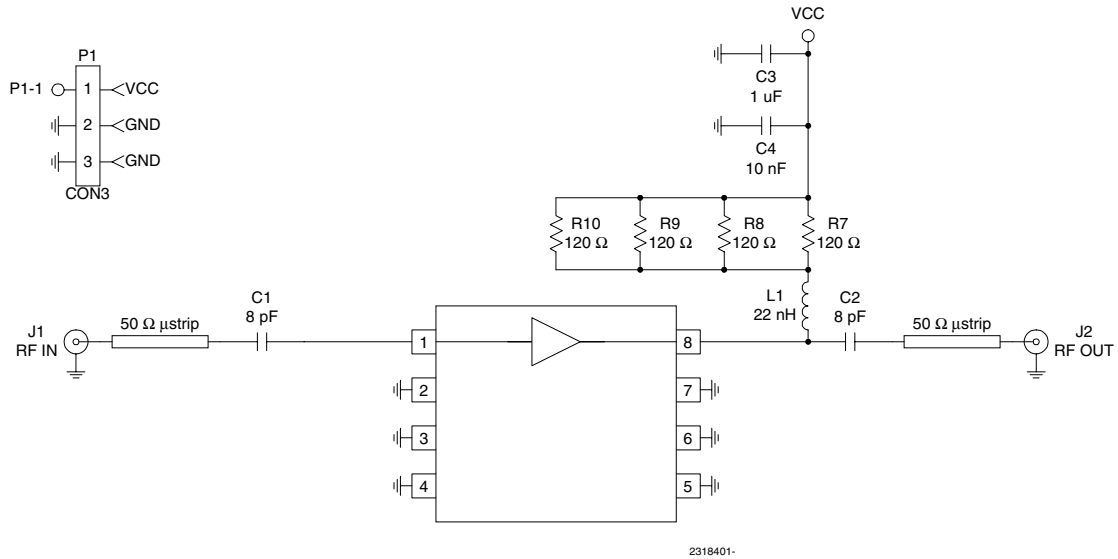
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Evaluation Board Schematic - DC to 3GHz

(Download Bill of Materials from www.rfmd.com.)

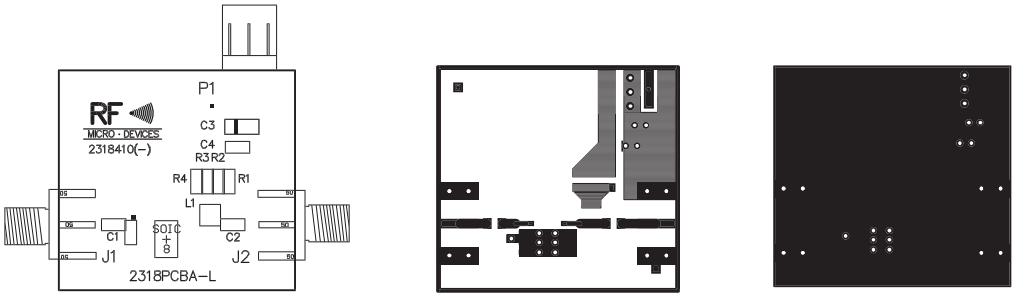


Evaluation Board Schematic - 3GHz to 6GHz

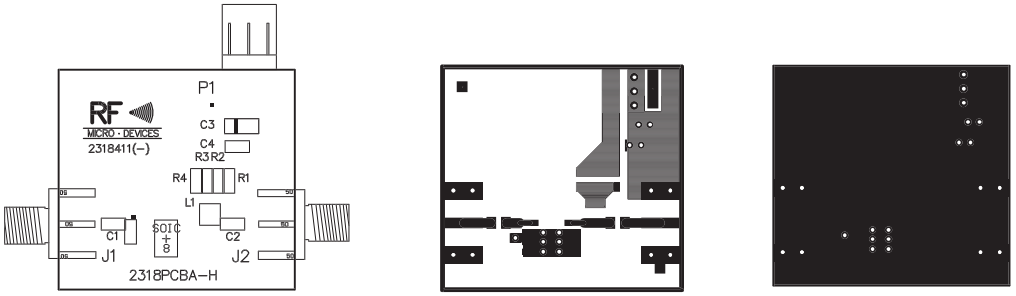


Evaluation Board Layout - DC to 3GHz
Board Size 1.233" x 1.145"

Board Thickness 0.031", Board Material FR-4



Evaluation Board Layout - 3GHz to 6GHz



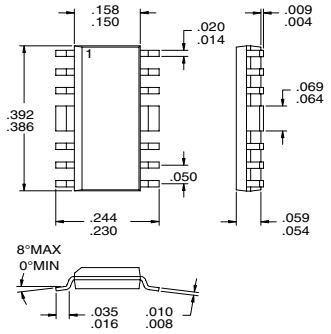
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Typical Applications

- CATV Distribution Amplifiers
- Cable Modems
- Broadband Gain Blocks
- Laser Diode Driver
- Return Channel Amplifier
- Base Stations

Product Description

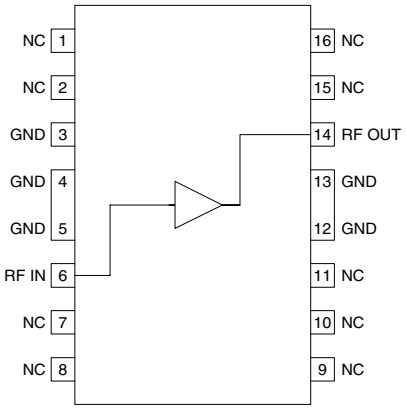
The RF2320 is a general purpose, low-cost, high-linearity RF amplifier IC. The device is manufactured on a Gallium Arsenide process and is featured in an SOP-16 batwing package. It has been designed for use as an easily cascadable 75Ω gain block with a Noise Figure of less than 2dB. Gain flatness better than 0.5dB from 5MHz to 1000MHz, and high linearity make this part ideal for cable TV applications. Other applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 2500MHz. The device is self-contained with 75Ω input and output impedances providing 2:1 VSWR matching. For higher input and output return losses, see the evaluation schematic.



Package Style: SOP-16 BW

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 5MHz to 2500MHz Operation
- Internally Matched Input and Output
- 16dB Small Signal Gain
- 1.6dB Noise Figure
- +22dBm Output Power
- Single 6V to 9V Positive Power Supply

Ordering Information

RF2320	Linear General Purpose Amplifier
RF2320 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Device Current	175	mA
Device Voltage	9	V
Input RF Power	+10	dBm
Output Load VSWR	20:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

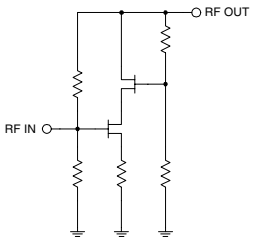
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (50Ω)					T=25 °C, V_{DD}=7V, Freq= 1000MHz, 50Ω System, P_{IN}=-10dBm
Frequency Range		5 to 2500		MHz	3dB Bandwidth
Input VSWR		2:1			Appropriate values for the DC blocking capacitor and bias inductor are required to maintain this VSWR at the intended operating frequency range.
Output VSWR		1.3:1			See note for Input VSWR.
Gain		15		dB	At 100MHz
Gain		16		dB	At 2000MHz
Gain Flatness		+/-1		dB	From 5MHz to 2500MHz
Noise Figure		1.8		dB	From 5MHz to 900MHz, -30 to +70 °C
Noise Figure		1.6		dB	From 900MHz to 2500MHz,
Output IP_3		35		dBm	At 100MHz
Output IP_3		36		dBm	At 1000MHz
Output IP_2		39.6		dBm	At 1000MHz
Output P_{1dB}		21.5		dBm	At 100MHz
Output P_{1dB}		22.5		dBm	At 1000MHz
Output P_{1dB}		18		dBm	At 2000MHz
Reverse Isolation		20		dB	
					T=25 °C, V_{DD}=9V, Freq= 500MHz, 50Ω System, P_{IN}=-10dBm
Gain		16.5		dB	At 100MHz
Gain		16.7		dB	At 1000MHz
Noise Figure		2.0		dB	From 5MHz to 900MHz,
Noise Figure		1.8		dB	From 900MHz to 2500MHz,
Output IP_3		36		dBm	At 100MHz
Output IP_3		36.3		dBm	At 1000MHz
Output IP_2		39.8		dBm	At 1000MHz
Output P_{1dB}		23		dBm	At 100MHz
Output P_{1dB}		24.7		dBm	At 1000MHz
Output P_{1dB}		19.5		dBm	At 2000MHz
Power Supply					
Supply Voltage (V_{DD})	6	7	9	V	
Operating Current Range	75	85	100	mA	

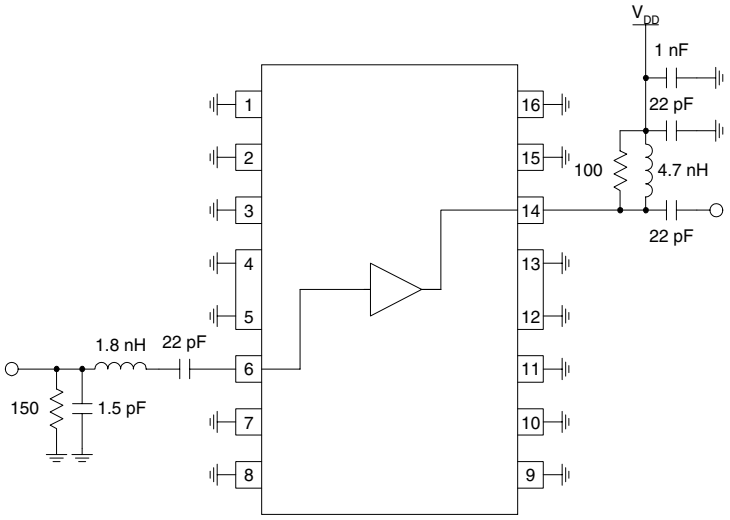
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (75Ω)					T=25°C, V_{DD}=7V, 75Ω System, P_{IN}=-8dBm
Frequency Range		5 to 2500		MHz	3dB Bandwidth
Input VSWR		1.6:1			Appropriate values for the output DC blocking capacitor and bias inductor are required to maintain this VSWR over the intended operating frequency range.
Output VSWR		1.3:1			See note for input VSWR.
Gain		15		dB	At 500MHz
Gain Flatness		+1-0.5		dB	5MHz to 1000MHz
Output IP_3		34.6		dBm	At 10MHz, Delta F1 and F2 = 1MHz
		36.1		dBm	At 500MHz
		33.1		dBm	At 1000MHz
Output IP_2		49.9		dBm	At 100MHz, Delta F1 and F2 = 156MHz
		48.5		dBm	At 1000MHz
Output IP_{1dB}		21		dBm	At 10MHz
		23		dBm	At 500MHz
		22		dBm	At 1000MHz
Power Supply					
Supply Voltage (V_{DD})	6	7	9	V	
Operating Current Range	75	85	100	mA	

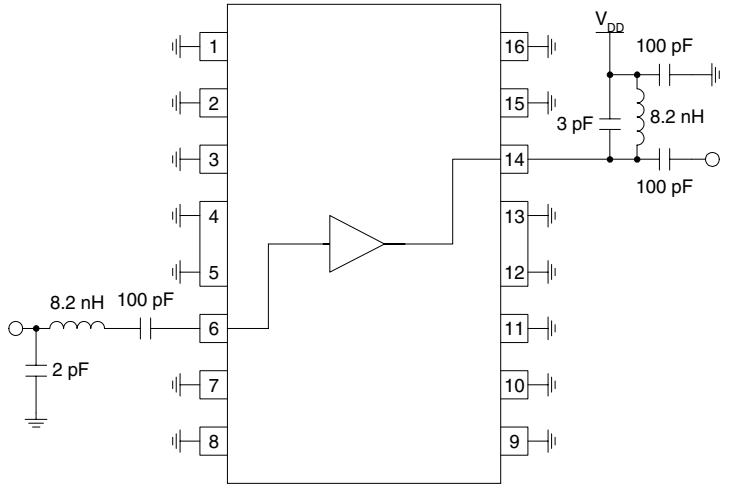
Pin	Function	Description	Interface Schematic
1	NC	No connection. This pin should be connected to the ground plane.	
2	NC	Same as pin 1.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Each ground pin should have a via to the ground plane.	
4	GND	Same as pin 3.	
5	GND	Same as pin 3.	
6	RF IN	RF input pin. This pin is not internally DC blocked. A DC blocking capacitor suitable for the frequency of operation is required if DC is present from the previous stage. The gate voltage is nominally 0V but can be raised externally to increase the bias level. This will increase the current drain but improve linearity.	
7	NC	Same as pin 1.	
8	NC	Same as pin 1.	
9	NC	Same as pin 1.	
10	NC	Same as pin 1.	
11	NC	Same as pin 1.	
12	GND	Same as pin 3.	
13	GND	Same as pin 3.	
14	RF OUT	RF output and bias pin. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. For biasing, only an RF choke is needed.	
15	NC	Same as pin 1.	
16	NC	Same as pin 1.	

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Application Schematic 1930-1990MHz Narrowband Operation



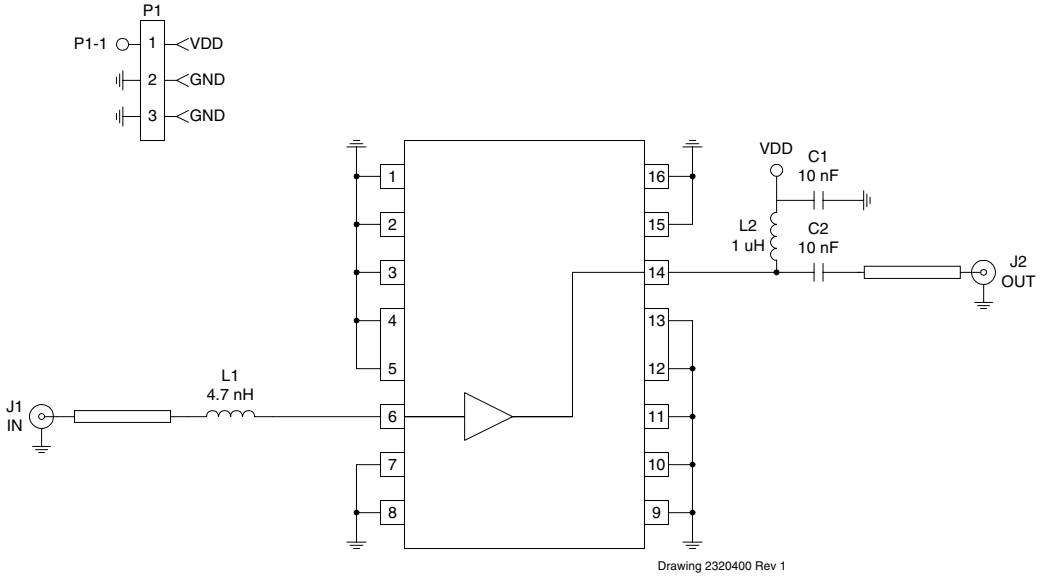
Application Schematic 869-894MHz Narrowband Operation



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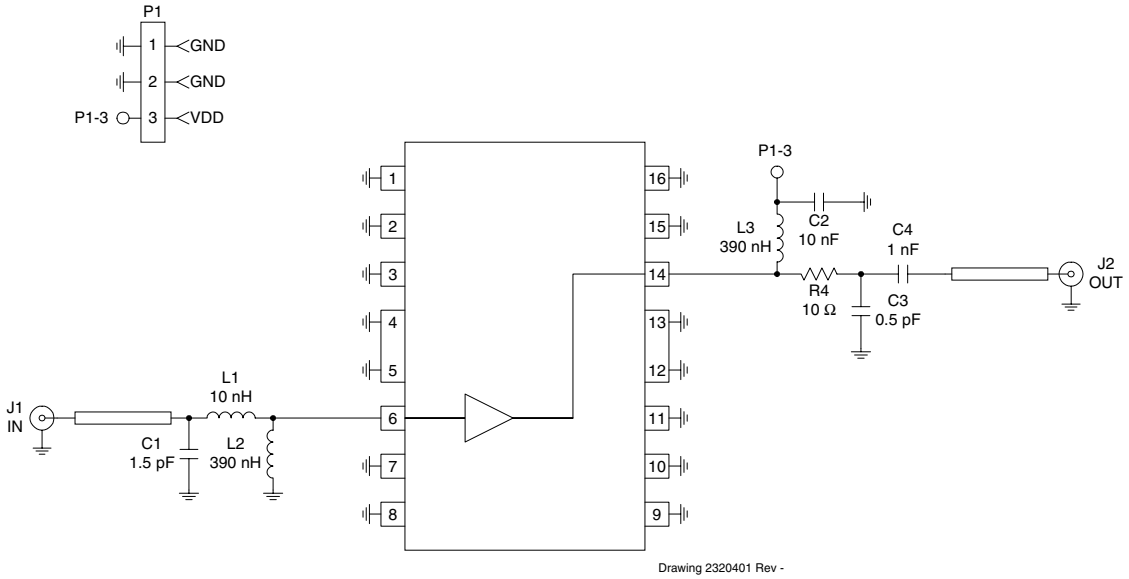
Evaluation Board Schematic - 50Ω

(Download Bill of Materials from www.rfmd.com.)



Drawing 2320400 Rev 1

Evaluation Board Schematic - 75Ω

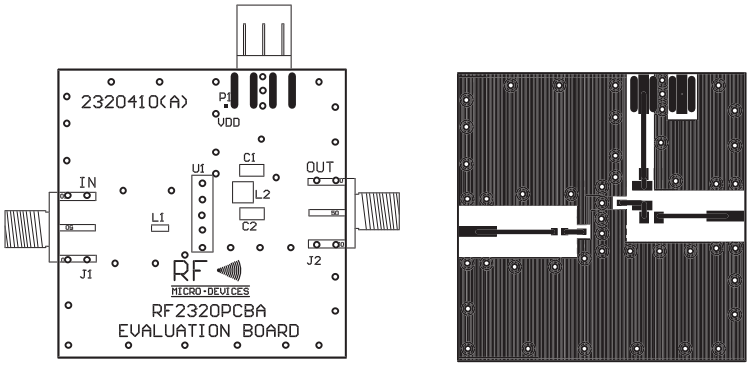


Drawing 2320401 Rev -

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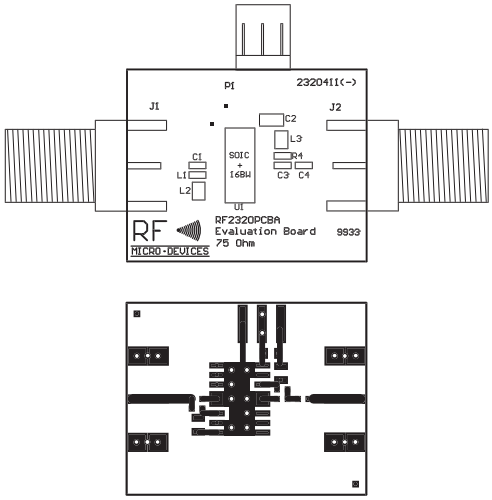
Evaluation Board Layout - 50Ω
Board Size 1.5” x 1.5”

Board Thickness 0.031”, Board Material FR-4

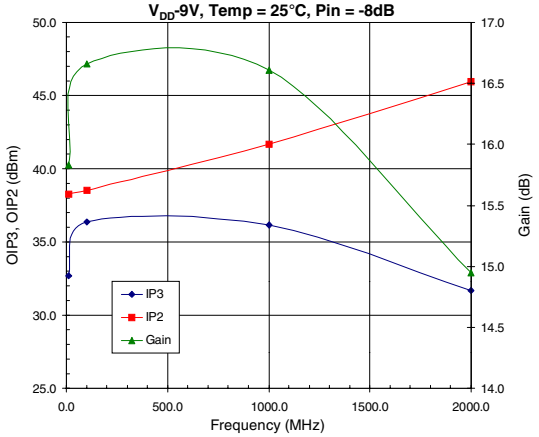


Evaluation Board Layout - 75Ω

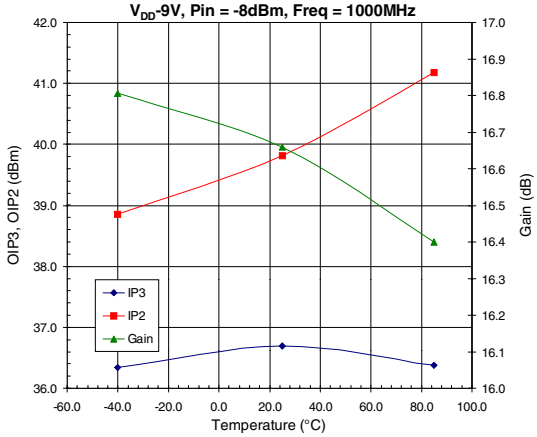
Board Thickness 0.062”, Board Material FR-4



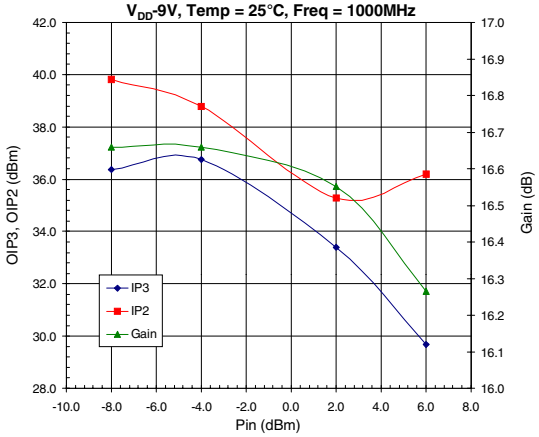
Gain, OIP3, and OIP2 versus Frequency
V_{DD}-9V, Temp = 25°C, Pin = -8dB



Gain, OIP3, and OIP2 versus Temperature
V_{DD}-9V, Pin = -8dBm, Freq = 1000MHz

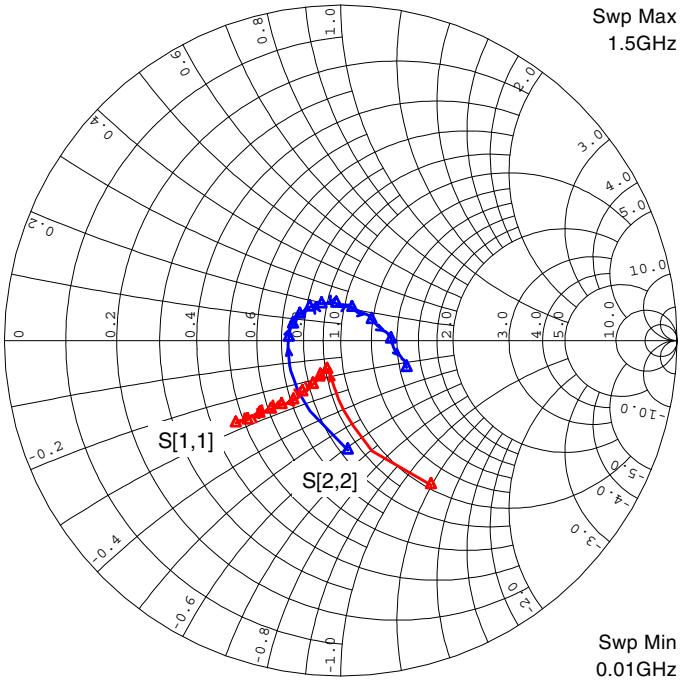


Gain, OIP3, and OIP2 versus Pin
V_{DD}-9V, Temp = 25°C, Freq = 1000MHz



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75 Ohm, 8V, 25°C



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RF MICRO·DEVICES

Preliminary

RF2360

LINEAR GENERAL PURPOSE AMPLIFIER

Typical Applications

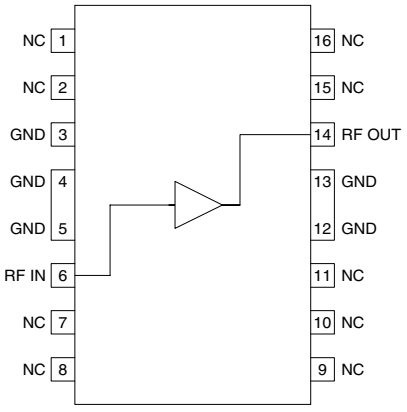
- CATV Distribution Amplifiers
- Cable Modems
- Broadband Gain Blocks
- Laser Diode Driver
- Return Channel Amplifier
- Base Stations

Product Description

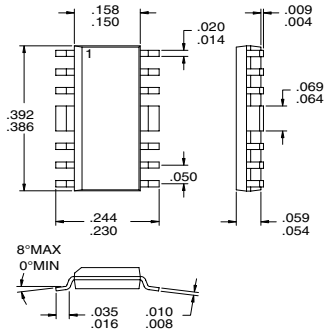
The RF2360 is a general purpose, low-cost, high-linearity RF amplifier IC. The device is manufactured on a Gallium Arsenide process and is featured in an SOP-16 batwing package. It has been designed for use as an easily cascadable 75Ω gain block with a Noise Figure of less than 2dB. Gain flatness better than 0.5dB from 5MHz to 1000MHz, and high linearity make this part ideal for cable TV applications. Other applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 1000MHz. The device is self-contained with 75Ω input and output impedances providing less than 2:1 VSWR matching. For higher input and output return losses, see the evaluation schematic.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-16 BW

Features

- 5MHz to 1500MHz Operation
- Internally Matched Input and Output
- 20dB Small Signal Gain
- 1.2dB Noise Figure
- +24dBm Output Power
- Single 6V to 9V Positive Power Supply

Ordering Information

RF2360	Linear General Purpose Amplifier
RF2360 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

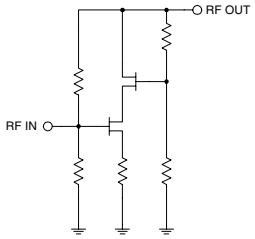
Parameter	Rating	Unit
Device Current	175	mA
Device Voltage	9	V
Input RF Power	+10	dBm
Output Load VSWR	20:1	
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

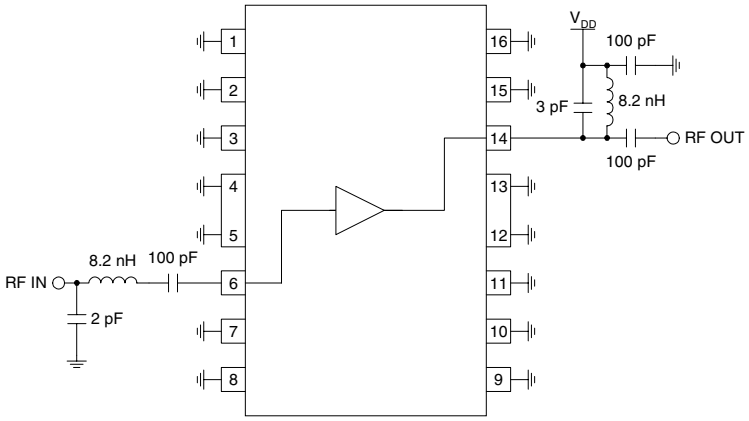
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (50Ω)					T=25 °C, V_{DD}=7V, 50Ω System, P_{IN}=-8dBm
Frequency Range		5 to 1500		MHz	3dB Bandwidth
Input VSWR		1.6:1			Appropriate values for the output DC blocking capacitor and bias inductor are required to maintain this VSWR over the intended operating frequency range.
Output VSWR		1.2:1			See note for Input VSWR.
Gain		20		dB	At 500MHz
Gain Flatness		+/-0.9		dB	5MHz to 1000MHz
Noise Figure		1.2		dB	At 500MHz
Noise Figure		1.5		dB	From 5MHz to 1000MHz
Output IP_3		33.7		dBm	At 10MHz, Delta F1 and F2 = 1MHz
Output IP_3		37.2		dBm	At 500MHz
Output IP_3		36.4		dBm	At 1000MHz
Output IP_2		46.3		dBm	At 100MHz, Delta F1 and F2 = 156MHz
Output IP_2		44.4		dBm	At 1000MHz
Output P_{1dB}		21		dBm	At 10MHz
Output P_{1dB}		24		dBm	At 500MHz
Output P_{1dB}		23.7		dBm	At 1000MHz
Reverse Isolation		24		dB	At 500MHz
					T=25 °C, V_{DD}=9V, P_{IN}=-8dBm
Gain		20		dB	At 500MHz
Gain Flatness		+/-0.9		dB	5MHz to 1000MHz
Noise Figure		1.1		dB	At 500MHz
Noise Figure		1.5		dB	From 5MHz to 1000MHz,
Output IP_3		34.8		dBm	At 10MHz, Delta F1 and F2 = 1MHz
Output IP_3		38.1		dBm	At 500MHz
Output IP_3		38.7		dBm	At 1000MHz
Output IP_2		44.1		dBm	At 100MHz, Delta F1 and F2 = 156MHz
Output IP_2		48.6		dBm	At 1000MHz
Output P_{1dB}		22.5		dBm	At 10MHz
Output P_{1dB}		25.1		dBm	At 500MHz
Output P_{1dB}		25.3		dBm	At 1000MHz
Power Supply					
Supply Voltage (V_{DD})	6	7	9	V	
Operating Current Range	100	104	109	mA	

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Pin	Function	Description	Interface Schematic
1	NC	No connection. This pin should be connected to the ground plane.	
2	NC	Same as pin 1.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Each ground pin should have a via to the ground plane.	
4	GND	Same as pin 3.	
5	GND	Same as pin 3.	
6	RF IN	RF input pin. This pin is internally DC blocked. An external DC blocking capacitor is not required.	
7	NC	Same as pin 1.	
8	NC	Same as pin 1.	
9	NC	Same as pin 1.	
10	NC	Same as pin 1.	
11	NC	Same as pin 1.	
12	GND	Same as pin 3.	
13	GND	Same as pin 3.	
14	RF OUT	RF output and bias pin. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. For biasing, only an RF choke is needed.	
15	NC	Same as pin 1.	
16	NC	Same as pin 1.	

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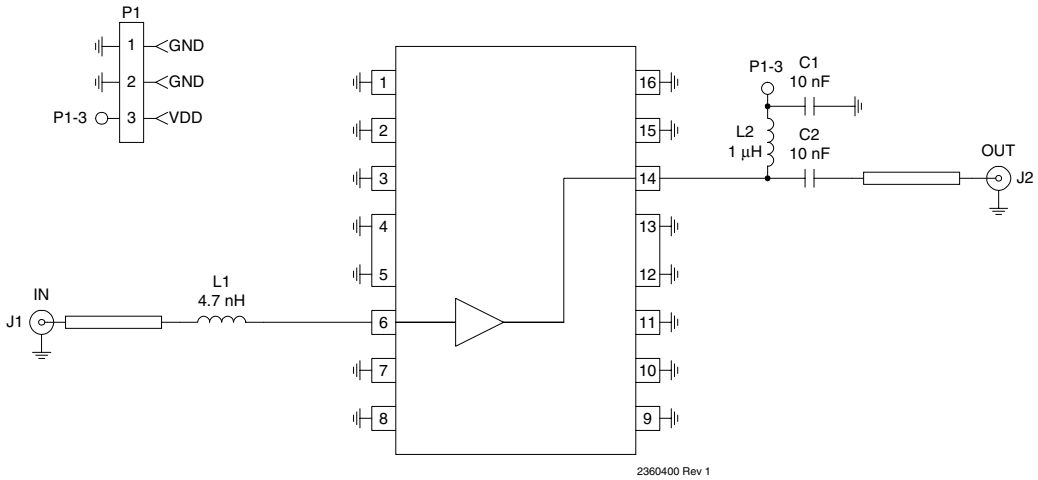
Application Schematic
869-894MHz Narrowband Operation



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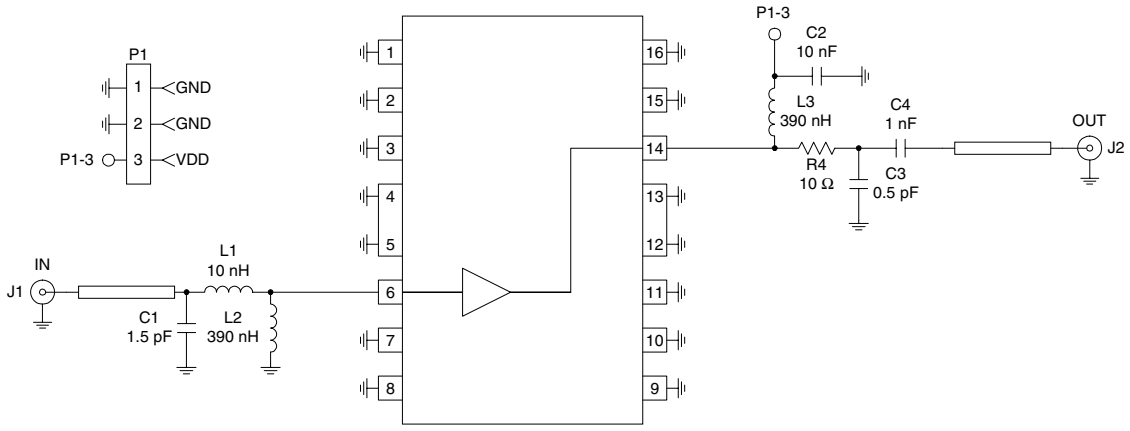
Evaluation Board Schematic - 50Ω

(Download Bill of Materials from www.rfmd.com.)



2360400 Rev 1

Evaluation Board Schematic - 75Ω

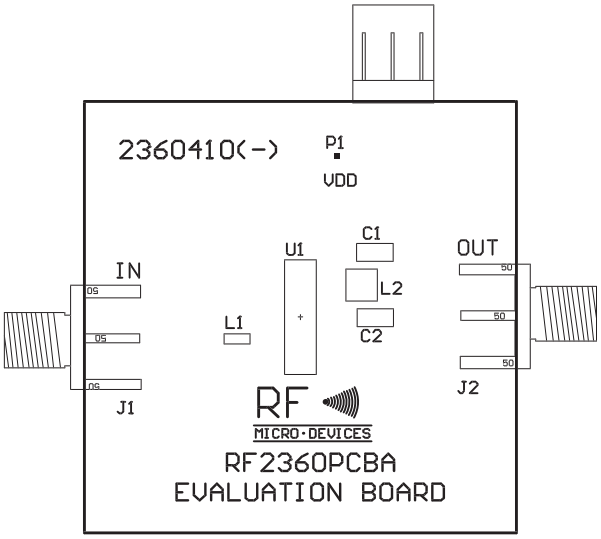


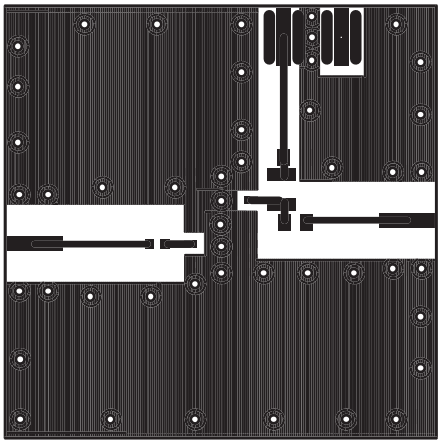
2360401 Rev-

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Evaluation Board Layout - 50Ω
Board Size 1.5" x 1.5"

Board Thickness 0.031", Board Material FR-4

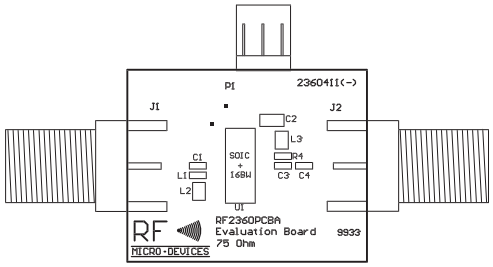


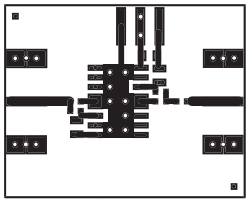


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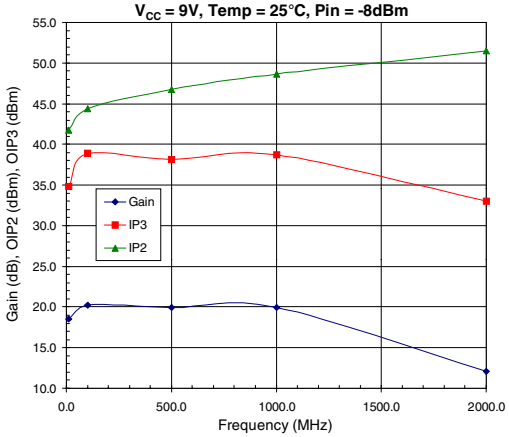
Evaluation Board Layout - 75Ω

Board Thickness 0.062", Board Material FR-4

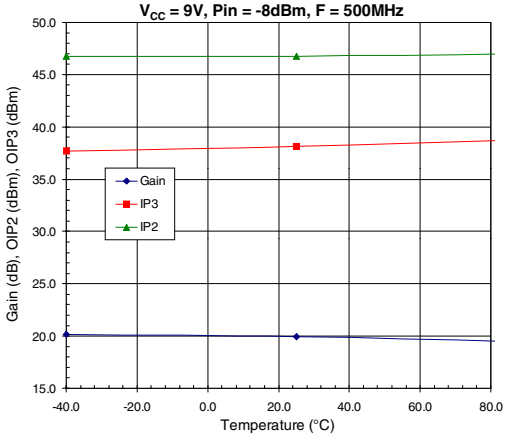




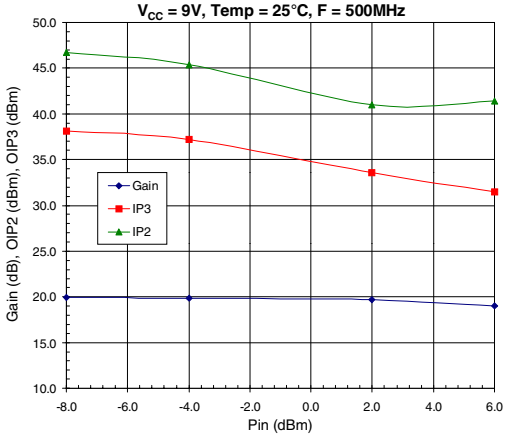
Gain, OIP2 and OIP3 versus Frequency
V_{CC} = 9V, Temp = 25°C, Pin = -8dBm



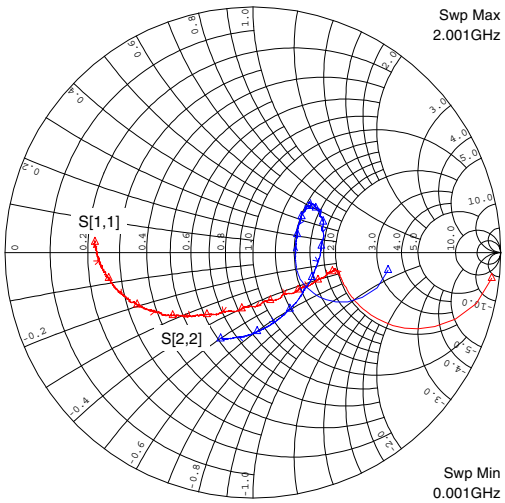
Gain, OIP2 and OIP3 versus Temperature
V_{CC} = 9V, Pin = -8dBm, F = 500MHz



Gain, OIP2 and OIP3 versus Pin
V_{CC} = 9V, Temp = 25°C, F = 500MHz



75 Ohm, 8V, 25°C



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4 General Purpose Amplifiers

Part	Description	Frequency (GHz)	Vcc (Volts)	Icc (mA)	Isolation (dB)	Gain (dB)	NF (dB)	P1dB (dBm)	Package	Page
RF2043	General Purpose Amplifier	DC to 6	5 to 6	70	16.5	11	7.6	+18.5	MicroX-CF	4-1
RF2044	General Purpose Amplifier	DC to 6	4.3 to 5.3	65	22	20	4.1	+18.5	MicroX-CF	4-7
RF2045	General Purpose Amplifier	DC to 6	4.6 to 5.6	65	18	14	5.0	+18	MicroX-CF	4-13
RF2046	General Purpose Amplifier	DC to 3	3 to 4	35	23	22	3.8	+12	MicroX-CF	4-19
RF2047	General Purpose Amplifier	DC to 6	3 to 4	40	19	16	4.2	+12	MicroX-CF	4-25
RF2048	General Purpose Amplifier	DC to 8	3 to 4	40	16.5	12	5.3	+12	MicroX-CF	4-31
RF2301	High Isolation Buffer Amplifier	0.3 to 2.5	2.7 to 6	18	50	21	8.0	+4	SOP-8	4-37
RF2302	Broadband Linear Variable Gain Amplifier	0.1 to 2.0	3.0 to 6.0	35		-11to14	4	+14	MSOP-8	4-43
RF2303	Broadband Linear Variable Gain Amplifier	0.1 to 2.0	3.0 to 6.0	25	35	-2 to 23	4	+16	MLF16	4-51
RF2304	General Purpose Low-Noise Amplifier	0.3 to 2.5	2.7 to 6.0	5 to 26	18	8	1.8	+6	SOP-8	4-57
RF2306	General Purpose Amplifier	DC to 2	>3.7	20 to 65	20	20	3.5	+12	SOP-8	4-63
RF2307	General Purpose Amplifier	DC to 3	>3.7	20 to 65	18	15	4.0	+14	SOP-8	4-67
RF2308	General Purpose Amplifier	DC to 4	>3.7	20 to 65	15	12	5.0	+13	SOP-8	4-71
RF2310	Wideband General Purpose Amplifier	DC to 2.5	3.5 to 6.0	20 to 65	20	15	5.0	+19	SOP-8	4-75
RF2311	General Purpose Amplifier	DC to 1.6	2.7 to 6.0	8 to 17	20	14	4.0	+8	SOP-8	4-81
RF2314	General Purpose Low Noise Amplifier	0.15 to 2.5	2.7 to 6.0	5 to 25	20	14	1.4	+8	SOT-23-5	4-87
RF2321	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	8	36	12	3.7	-7	SOT-23-5	4-91
RF2322	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	8	38	19	3.3	-7	SOT-23-5	4-99
RF2323	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	7	33	21	2.3	-7	SOT-23-5	4-107
RF2324	PCS CDMA/TDMA 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	24 to 43	36	22	1.8	+16	MSOP-8	4-115
RF2325	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	27	22	16	5.0	+7	SOT-23-5	4-121
RF2326	3V General Purpose Amplifier	DC to 2.5	2.7 to 3.3	25	18	12	5.7	+7	SOT-23-5	4-129
RF2333	General Purpose Amplifier	DC to 6	5 to 6	70	17	10	8.2	+18.5	SOT-23-5	4-137
RF2334	General Purpose Amplifier	DC to 4	>4.8	65	20	16	5	+18.5	SOT-23-5	4-143
RF2335	General Purpose Amplifier	DC to 6	>5.0	65	17	12	5.6	+17	SOT-23-5	4-147
RF2336	General Purpose Amplifier	DC to 3	>3.5	35	21	20	3.8	+11	SOT-23-5	4-151
RF2337	General Purpose Amplifier	DC to 6	>3.6	40	17	15	4.5	+12	SOT-23-5	4-155
RF2338	General Purpose Amplifier	DC to 6	>3.6	40	16	12		+10.5	SOT-23-5	4-159
RF2347	3V Low Noise Amplifier/ 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	22	26	20.5	1.4	+15.5	MSOP-8	4-163
RF2351	3V PCS CDMA Split Band PA Driver	1.71 to 1.91	3.0 to 6.0	48	30	21	2.5	+16	MLF16	4-171
RF2352	3V CDMA Driver Amplifier	0.8 to 0.9	2.7 to 3.6	15		19.5	2.3		MLF16	4-177
RF2361	3V Low Noise Amplifier/ 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	22	26	20.5	1.4	+15.5	SOT23-5	4-183
RF2362	PCS CDMA/TDMA 3V PA Driver Amplifier	0.15 to 2.5	2.5 to 6.0	38	32	20.1	2.2	+14.5	SOT23-5	4-193
RF2363	Dual-Band 3V Low Noise Amplifier	800 to 1000/ 1800 to 2000	2.5 to 5.0	5/ 7.5	20/ 30	18/ 21.5	1.3/ 1.4	-10/ -12	SOT23-8	4-199
RF2364	3V PCS Low Noise Amplifier	1.8 to 2.5	2.7 to 3.3	17	27	18	1.7	8.5	SOT23-5	4-209
RF2365	3V Low Noise Amplifier	1.5 to 2.5	3.0	5.0 to 8.0	25	18	1.6		SOT23-5	4-215
RF2371	3V Low Noise Amplifier	0.7 to 2.0	2.7 to 3.6	2.9		17	1.6		SOT23-8	4-221
RF2375	3V DCS Low Noise Amplifier	0.7 to 2.0	2.7 to 3.6	5.3		18	2.5		SOT23-8	4-227
RF2442	High-Linearity Low Noise Amplifier	0.50 to 2.5	2.5 to 5.0	16	24	20	1.5	+13	MSOP-8	4-231
RF2445	3V DCS Low Noise Amplifier	1700 to 2200	2.7 to 3.6	5	7	20	2.2	+2	MSOP-8	4-241
RF2451	3V Low Noise Amplifier	0.70 to 2.0	2.7 to 3.6	2.9		12	1.7	-3	MSOP-8	4-247

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RF2043

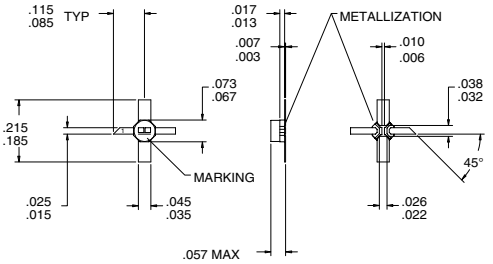
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- High Reliability Applications
- Broadband Test Equipment

Product Description

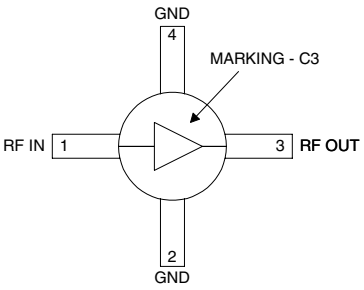
The RF2043 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. With a goal of enhanced reliability, the extremely small Micro-X-CF ceramic package offers significantly lower thermal resistance than similar size plastic packages.



Package Style: Micro-X-CF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to >6000MHz Operation
- Internally matched Input and Output
- 11dB Small Signal Gain
- +35dBm Output IP3
- +18.5dBm Output Power
- Extremely Flat Gain Response

Ordering Information

RF2043	General Purpose Amplifier
RF204X PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2043

Absolute Maximum Ratings

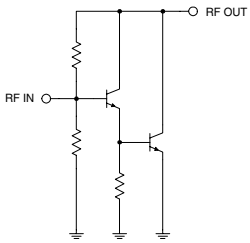
Parameter	Rating	Unit
Supply Current	120	mA
Input RF Power	+20	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

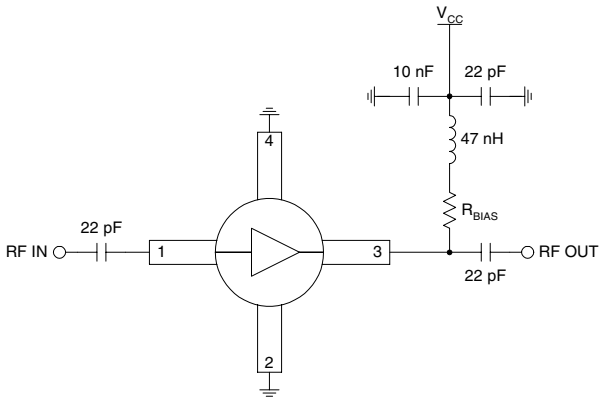
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_D=5.5V, I_{CC}=70mA
Frequency Range		DC to >6000		MHz	
1dB Bandwidth		5.5		GHz	
Gain		11.3		dB	Freq=100MHz
		11.3		dB	Freq=1000MHz
	10.2	11.4		dB	Freq=2000MHz
		11.5		dB	Freq=3000MHz
		11.5			Freq=4000MHz
		9.9			Freq=6000MHz
Gain Flatness		±0.05		dB	100MHz to 2000MHz
Noise Figure		7.6		dB	Freq=1000MHz
Input VSWR		<1.8:1			In a 50Ω system, DC to 3000MHz
		<2.5:1			In a 50Ω system, 3000MHz to 6000MHz
Output VSWR		<1.8:1			In a 50Ω system, DC to 3000MHz
		<2.6:1			In a 50Ω system, 3000MHz to 6000MHz
Output IP_3		+34.5		dBm	Freq=1000MHz
Output P_{1dB}		+18.5		dBm	Freq=1000MHz
Reverse Isolation		16.5		dB	Freq=1000MHz
Thermal					I_{CC}=70mA, P_{DISS}=370mW
$Theta_{JC}$		149		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		142		°C	T_{AMB}=+85°C
Mean Time Between Failures		$1.4x10^3$		years	T_{AMB}=+85°C
		$3.4x10^5$		years	T_{AMB}=+25°C
		$1.8x10^9$		years	T_{AMB}=-40°C
Power Supply					With 22Ω bias resistor
Device Operating Voltage	5.0	5.5	6.0	V	At pin 3 with I_{CC}=70mA
Operating Current		70		mA	

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 120 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 5.5V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
4	GND	Same as pin 2.	

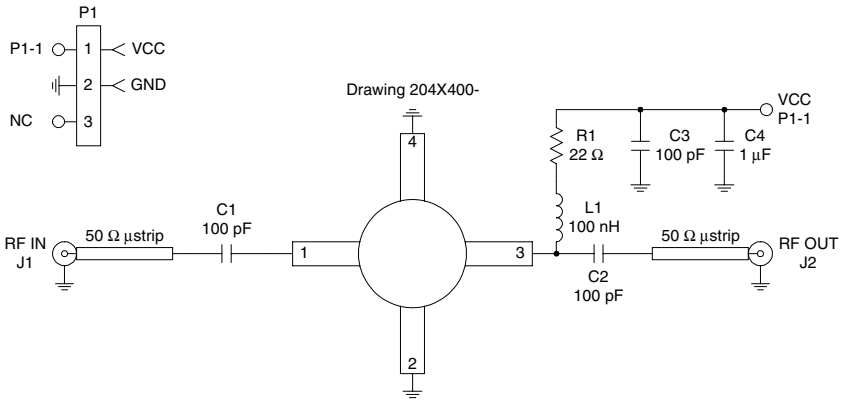
Application Schematic



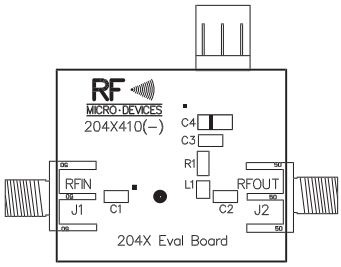
Db00.bk Page 4 Thursday, January 6, 2000 6:50 PM

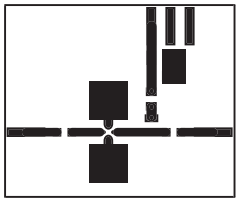
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

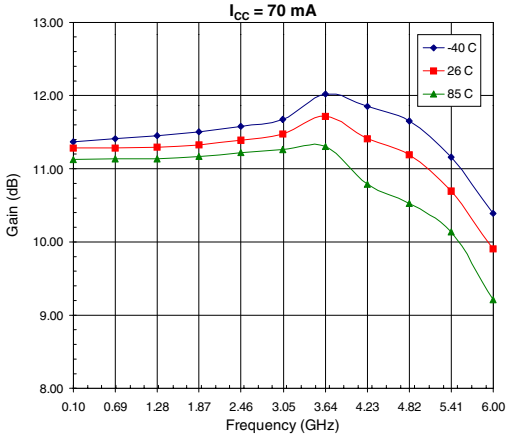


Evaluation Board Layout
Board Size 1.195" x 1.000"

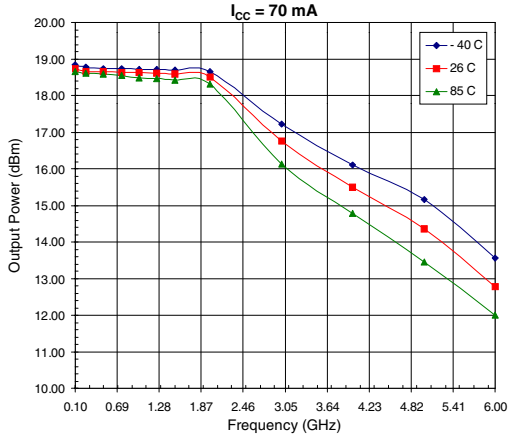




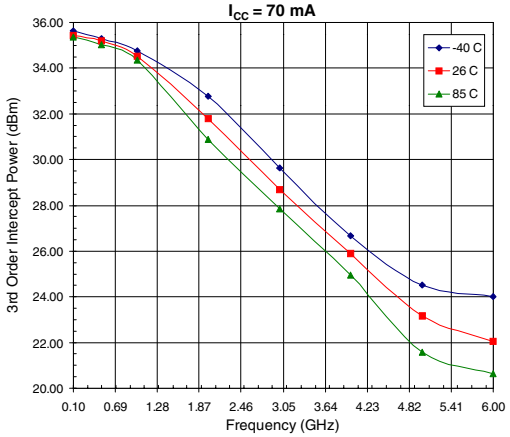
Gain versus Frequency Across Temperature
I_{CC} = 70 mA



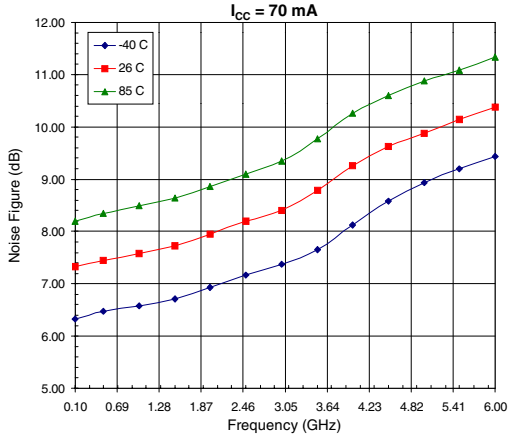
Output P1dB versus Frequency Across Temperature
I_{CC} = 70 mA



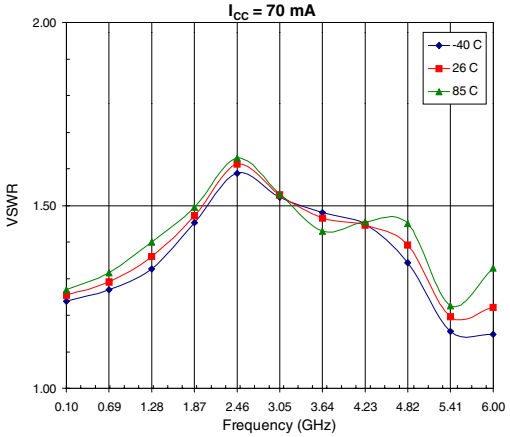
Output IP3 versus Frequency Across Temperature
I_{CC} = 70 mA



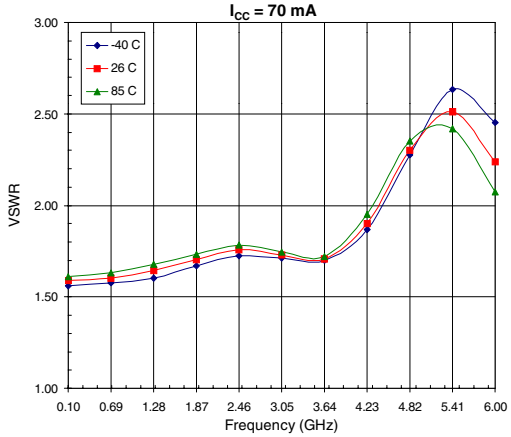
Noise Figure versus Frequency Across Temperature
I_{CC} = 70 mA

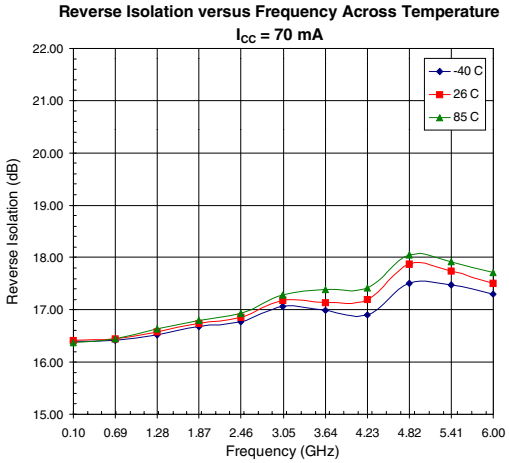


Input VSWR versus Frequency Across Temperature
I_{CC} = 70 mA



Output VSWR versus Frequency Across Temperature
I_{CC} = 70 mA




Reverse Isolation versus Frequency Across Temperature
I_{CC} = 70 mA
-40 C
26 C
85 C
Reverse Isolation (dB)
22.00
21.00
20.00
19.00
18.00
17.00
16.00
15.00
0.10
0.69
1.28
1.87
2.46
3.05
3.64
4.23
4.82
5.41
6.00
Frequency (GHz)

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RF2044

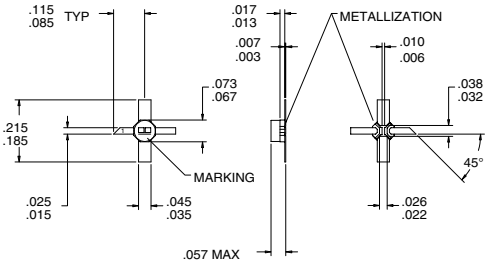
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- High Reliability Applications
- Broadband Test Equipment

Product Description

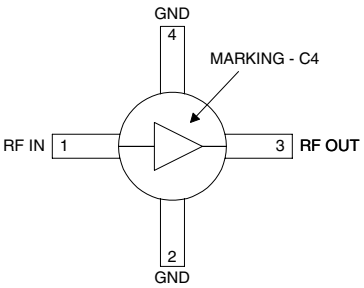
The RF2044 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. With a goal of enhanced reliability, the extremely small Micro-X-CF ceramic package offers significantly lower thermal resistance than similar size plastic packages.



Package Style: Micro-X-CF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to >6000MHz Operation
- Internally matched Input and Output
- 20dB Small Signal Gain
- 4.0dB Noise Figure
- 50mW Linear Output Power
- Single Positive Power Supply

Ordering Information

RF2044	General Purpose Amplifier
RF204X PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2044

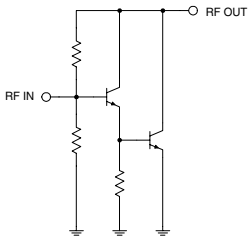
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	120	mA
Input RF Power	+13	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

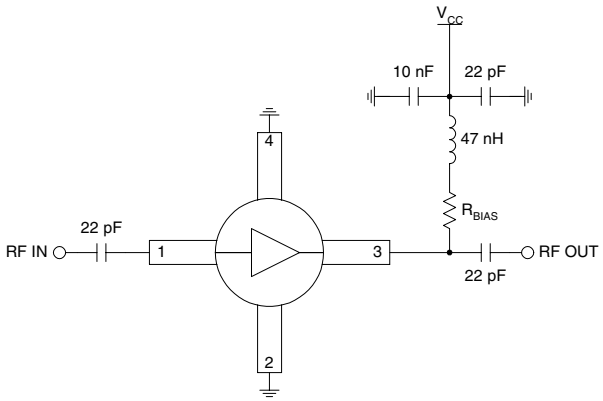
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=65mA
Frequency Range		DC to >6000		MHz	
3dB Bandwidth		3		GHz	
Gain		20.4		dB	Freq=100MHz
		19.9		dB	Freq=1000MHz
	16.5	19.0		dB	Freq=2000MHz
		17.5		dB	Freq=3000MHz
		16.6			Freq=4000MHz
		14.3			Freq=6000MHz
Gain Flatness		±0.7		dB	100MHz to 2000MHz
Noise Figure		4.1		dB	Freq=1000MHz
Input VSWR		<1.4:1			In a 50Ω system, DC to 5000MHz
		<1.7:1			In a 50Ω system, 5000MHz to 6000MHz
Output VSWR		<1.2:1			In a 50Ω system, DC to 3000MHz
		<1.8:1			In a 50Ω system, 3000MHz to 6000MHz
Output IP_3		+33.5		dBm	Freq=1000MHz
Output P_{1dB}		+18.5		dBm	Freq=1000MHz
Reverse Isolation		22.3		dB	Freq=1000MHz
Thermal					I_{CC}=65mA, P_{DISS}=300mW
$Theta_{JC}$		188		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		143		°C	T_{AMB}=+85°C
Mean Time Between Failures		$1.3x10^3$		years	T_{AMB}=+85°C
		$3.1x10^5$		years	T_{AMB}=+25°C
		$1.6x10^9$		years	T_{AMB}=-40°C
Power Supply					With 22Ω bias resistor
Device Operating Voltage	4.3	4.8	5.3	V	At pin 3 with I_{CC}=65mA
Operating Current		65		mA	

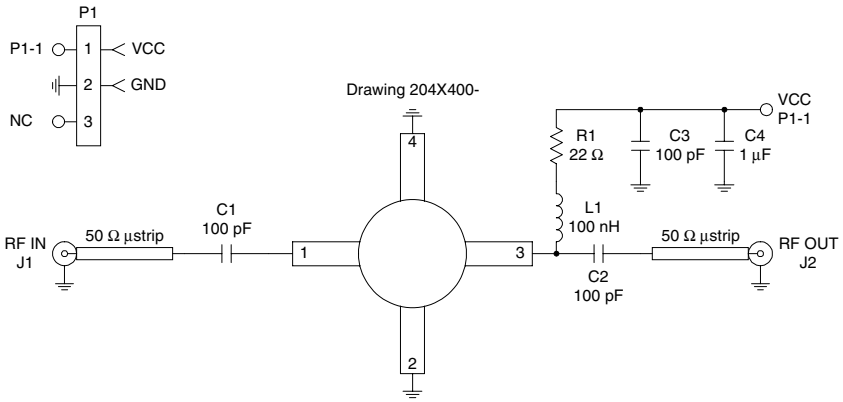
Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 120 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 4.9V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
4	GND	Same as pin 2.	

Application Schematic

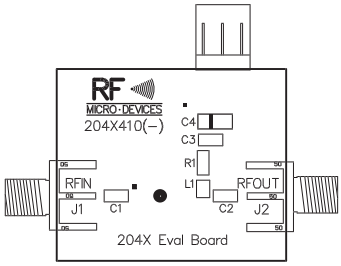


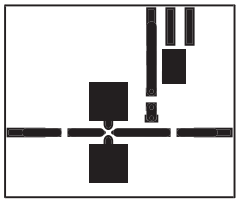
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

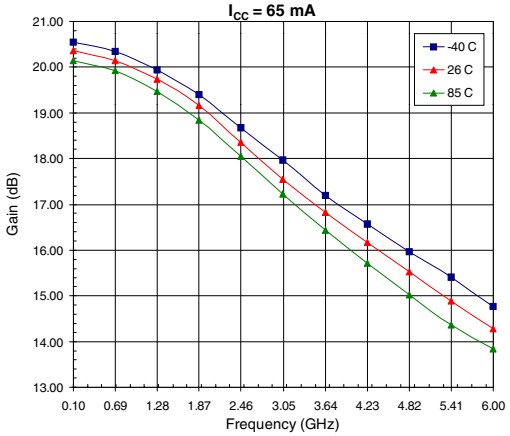


Evaluation Board Layout
Board Size 1.195" x 1.000"

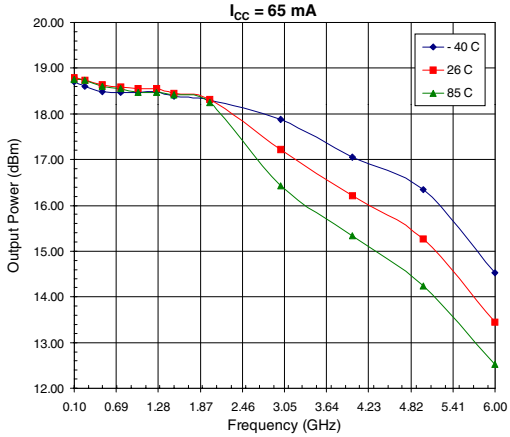




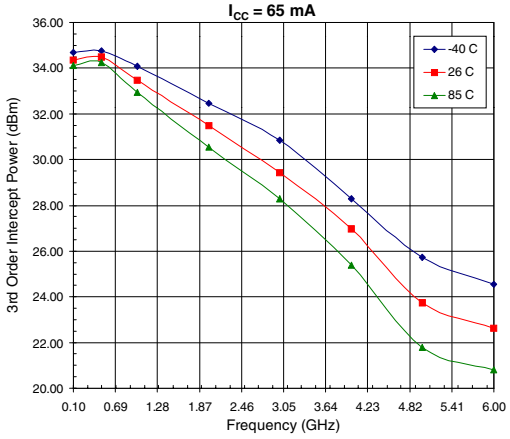
Gain versus Frequency Across Temperature
I_{CC} = 65 mA



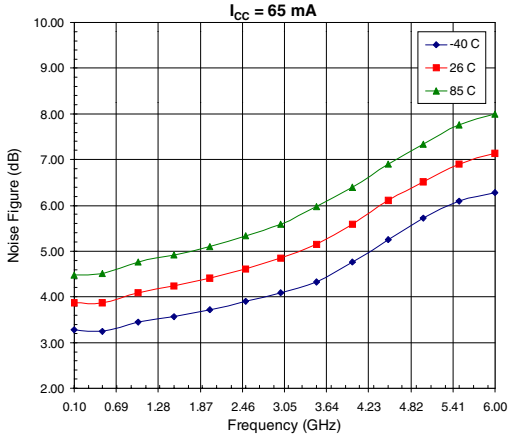
Output P1dB versus Frequency Across Temperature
I_{CC} = 65 mA



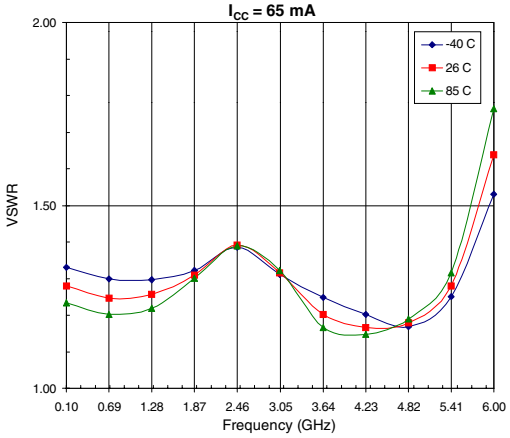
Output IP3 versus Frequency Across Temperature
I_{CC} = 65 mA



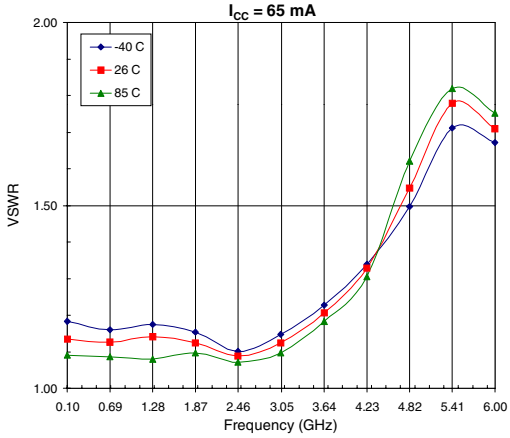
Noise Figure versus Frequency Across Temperature
I_{CC} = 65 mA



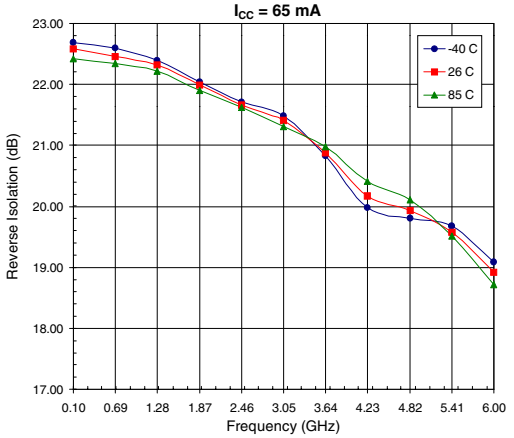
Input VSWR versus Frequency Across Temperature
I_{CC} = 65 mA



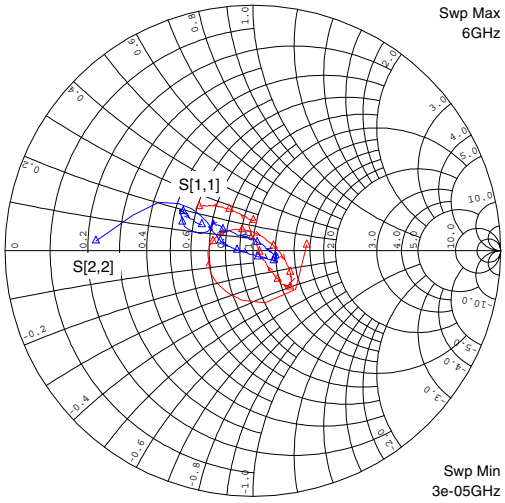
Output VSWR versus Frequency Across Temperature
I_{CC} = 65 mA



Reverse Isolation versus Frequency Across Temperature
I_{CC} = 65 mA



50 Ohms, 65 mA



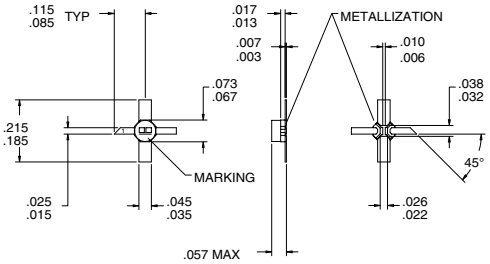
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Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- High Reliability Applications
- Broadband Test Equipment

Product Description

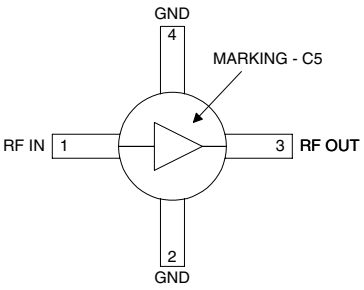
The RF2045 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. With a goal of enhanced reliability, the extremely small Micro-X-CF ceramic package offers significantly lower thermal resistance than similar size plastic packages.



Package Style: Micro-X-CF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to 6000MHz Operation
- Internally matched Input and Output
- 13dB Small Signal Gain
- +32dBm Output IP3
- +18dBm Output Power
- Excellent Gain Flatness

Ordering Information

RF2045	General Purpose Amplifier
RF2045 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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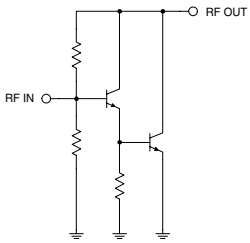
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	120	mA
Input RF Power	+20	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

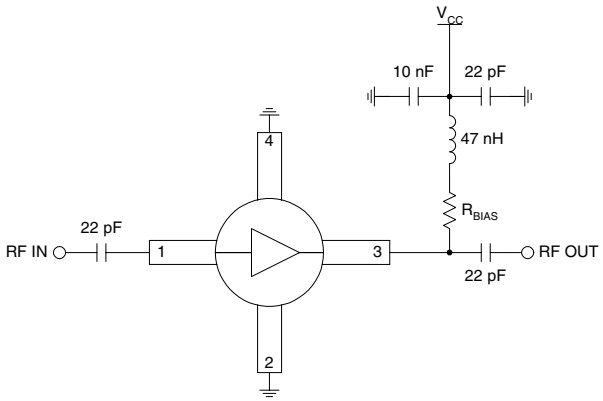
Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=65mA
Frequency Range		DC to 6000		MHz	
3dB Bandwidth		6		GHz	
Gain		13.8		dB	Freq=100MHz
		13.7		dB	Freq=1000MHz
	11	13.6		dB	Freq=2000MHz
		13.4		dB	Freq=3000MHz
		13			Freq=4000MHz
Gain Flatness		±0.2		dB	100MHz to 2000MHz
Noise Figure		5.0		dB	Freq=1000MHz
Input VSWR		1.7:1			In a 50Ω system, DC to 4000MHz
Output VSWR		1.7:1			In a 50Ω system, DC to 4000MHz
Output IP_3		+33		dBm	Freq=1000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+17.8		dBm	Freq=1000MHz
Reverse Isolation		18.4		dB	Freq=2000MHz
Thermal					I_{CC}=65mA, P_{DISS}=310mW
$Theta_{JC}$		173		°C/W	
Maximum junction temperature		142		°C	
Mean Time Between Failures		$1.5x10^3$		years	T_{AMB}=+85°C
Mean Time Between Failures		$3.7x10^5$		years	T_{AMB}=+25°C
Mean Time Between Failures		$2.0x10^9$		years	T_{AMB}=-40°C
Power Supply					With 22Ω bias resistor
Device Operating Voltage	4.6	5.0	5.6	V	At pin 3 with I_{CC}=65mA
Operating Current		65		mA	

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 120mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 5.0V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
4	GND	Same as pin 2.	

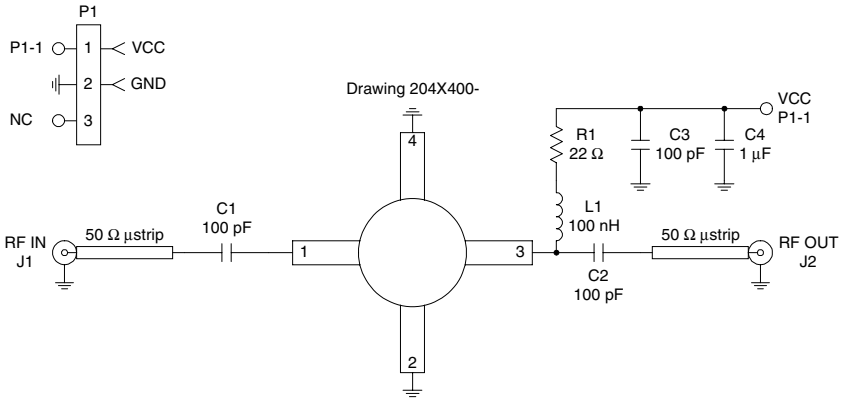
Application Schematic



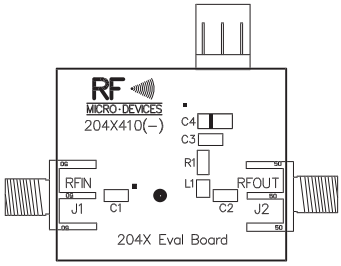
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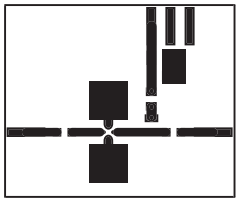
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

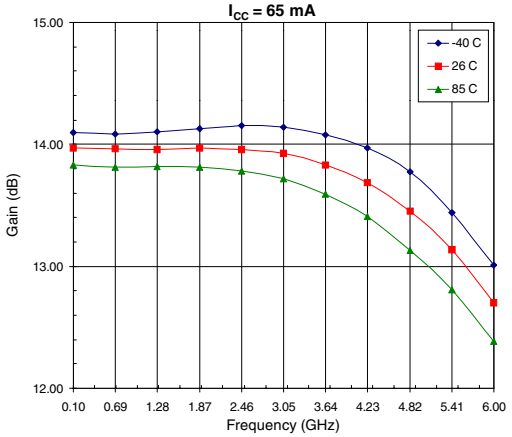


Evaluation Board Layout
Board Size 1.195" x 1.000"

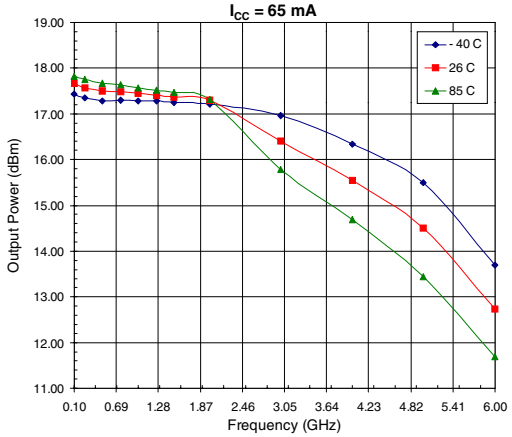




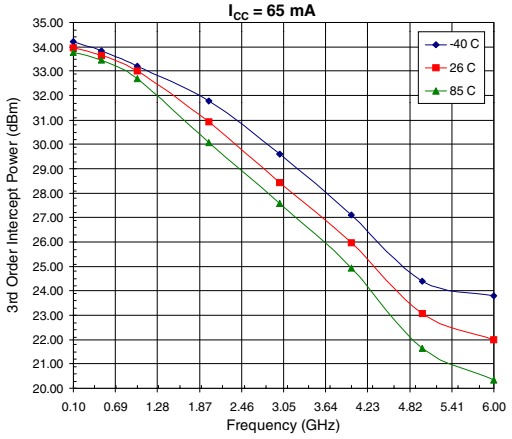
Gain versus Frequency Across Temperature
I_{CC} = 65 mA



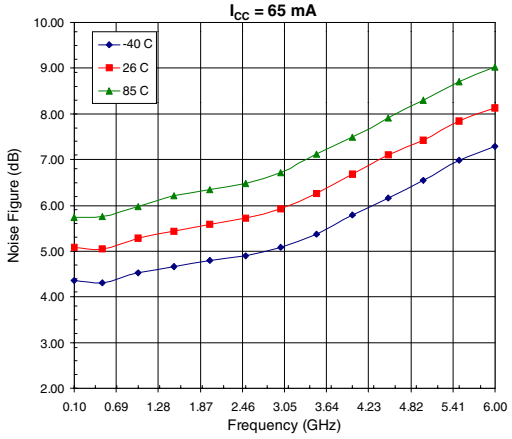
Output P1dB versus Frequency Across Temperature
I_{CC} = 65 mA



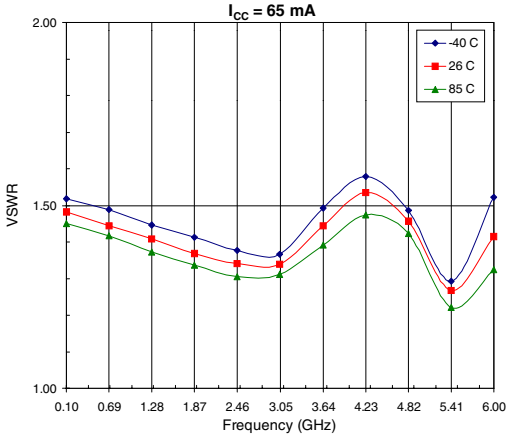
Output IP3 versus Frequency Across Temperature
I_{CC} = 65 mA



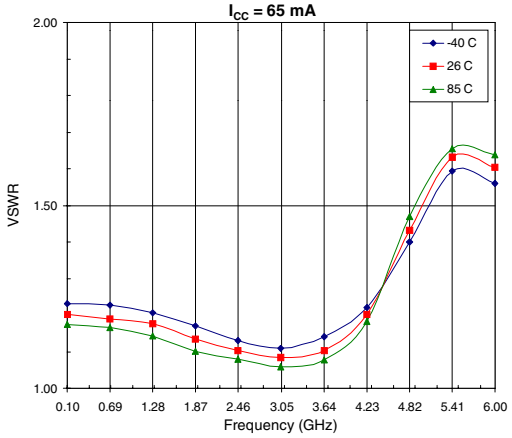
Noise Figure versus Frequency Across Temperature
I_{CC} = 65 mA



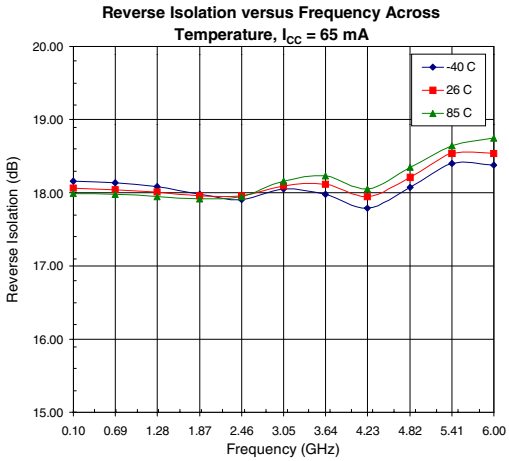
Input VSWR versus Frequency Across Temperature
I_{CC} = 65 mA



Output VSWR versus Frequency Across Temperature
I_{CC} = 65 mA



4
GENERAL PURPOSE AMPLIFIERS


Reverse Isolation versus Frequency Across Temperature, I_{CC} = 65 mA
20.00
19.00
18.00
17.00
16.00
15.00
Reverse Isolation (dB)
0.10
0.69
1.28
1.87
2.46
3.05
3.64
4.23
4.82
5.41
6.00
Frequency (GHz)
-40 C
26 C
85 C

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RF MICRO·DEVICES

Preliminary

RF2046

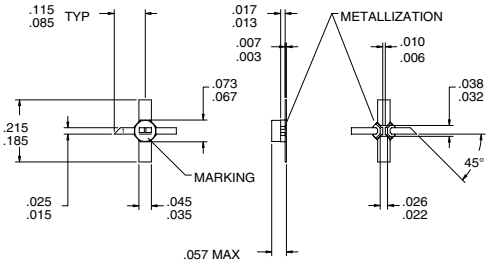
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- High Reliability Applications
- Broadband Test Equipment

Product Description

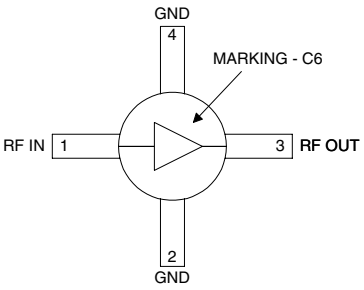
The RF2046 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 3000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. With a goal of enhanced reliability, the extremely small Micro-X-CF ceramic package offers significantly lower thermal resistance than similar size plastic packages.



Package Style: Micro-X-CF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to 3000MHz Operation
- Internally matched Input and Output
- 22dB Small Signal Gain
- 3.8dB Noise Figure
- 10mW Linear Output Power
- Single Positive Power Supply

Ordering Information

RF2046	General Purpose Amplifier
RF2046 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

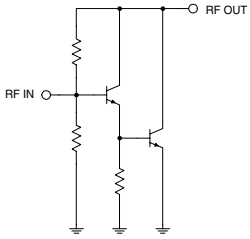
Parameter	Rating	Unit
Supply Current	75	mA
Input RF Power	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

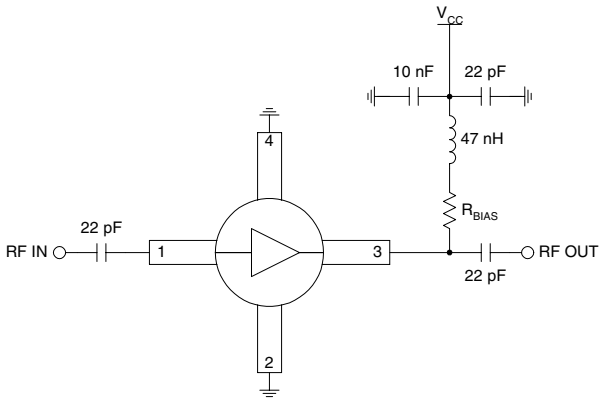
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_D=3.5V, I_{CC}=35mA
Frequency Range		DC to 3000		MHz	
Gain		22.9		dB	Freq=100MHz
		22.2		dB	Freq=1000MHz
	18	20.8		dB	Freq=2000MHz
		19.2		dB	Freq=3000MHz
Gain Flatness		±1.1		dB	100MHz to 2000MHz
Noise Figure		3.8		dB	Freq=2000MHz
Input VSWR		1.7:1			In a 50Ω system, DC to 3000MHz
Output VSWR		1.7:1			In a 50Ω system, DC to 3000MHz
Output IP_3		+23		dBm	Freq=2000MHz±100kHz, P_{TONE}=-18dBm
Output P_{1dB}		+12.1		dBm	Freq=2000MHz
Reverse Isolation		23.2		dB	Freq=2000MHz
Thermal					I_{CC}=35mA, P_{DISS}=120mW
$Theta_{JC}$		199		°C/W	
Maximum junction temperature		109		°C	
Mean Time Between Failures		$2.0x10^4$		years	T_{AMB}=+85°C
Mean Time Between Failures		$1.4x10^7$		years	T_{AMB}=+25°C
Mean Time Between Failures		$5.3x10^{11}$		years	T_{AMB}=-40°C
Power Supply					With 22Ω bias resistor
Operating Voltage	3.0	3.5	4.0	V	At pin 3 with I_{CC}=35mA
Operating Current		35		mA	

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 75 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
4	GND	Same as pin 2.	

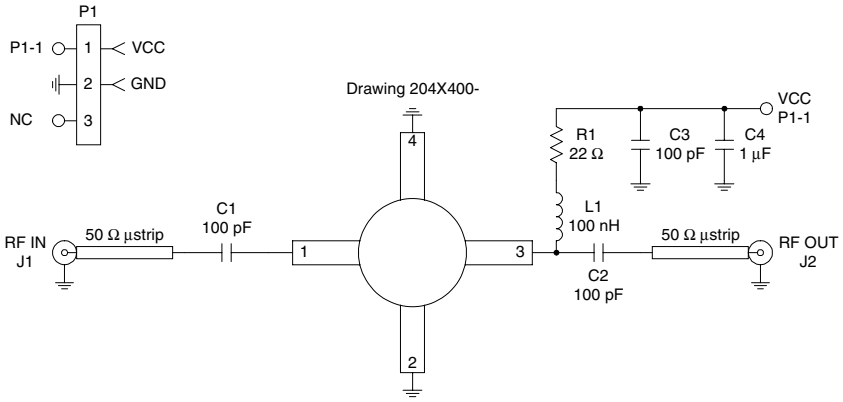
Application Schematic



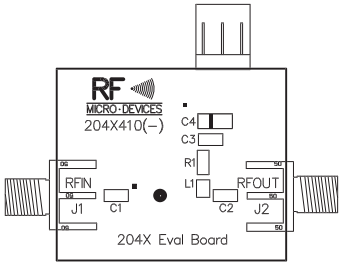
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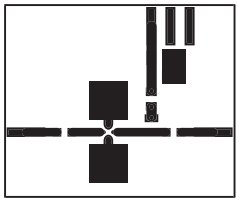
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



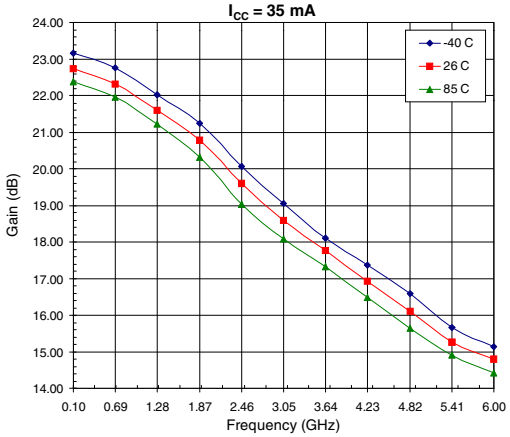
Evaluation Board Layout
Board Size 1.195" x 1.000"



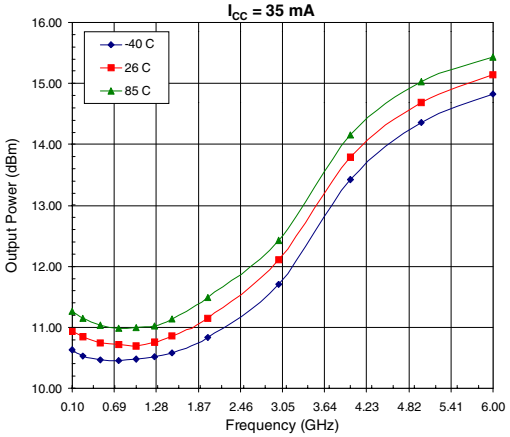


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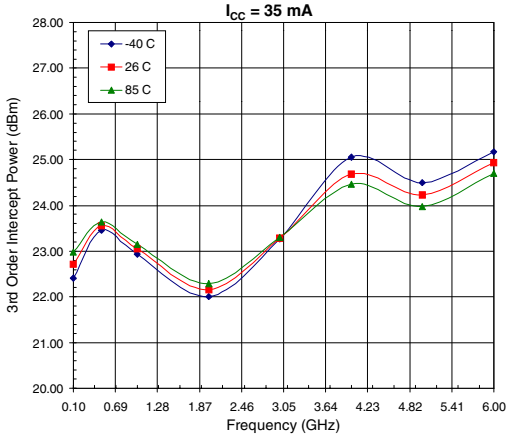
Gain versus Frequency Across Temperature
I_{CC} = 35 mA



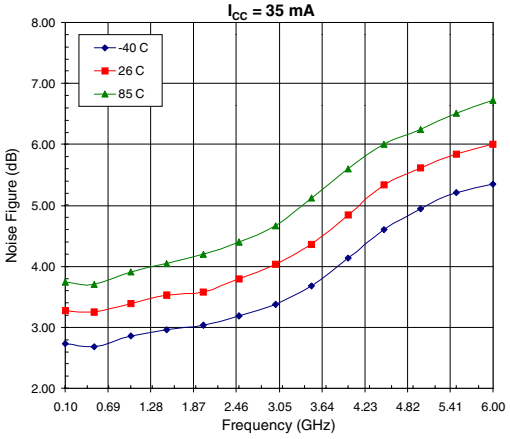
Output P1dB versus Frequency Across Temperature
I_{CC} = 35 mA



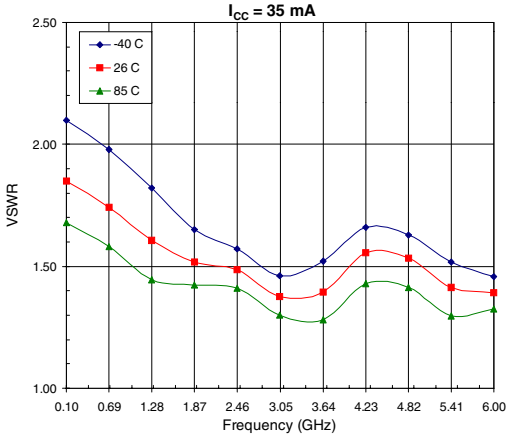
Output IP3 versus Frequency Across Temperature
I_{CC} = 35 mA



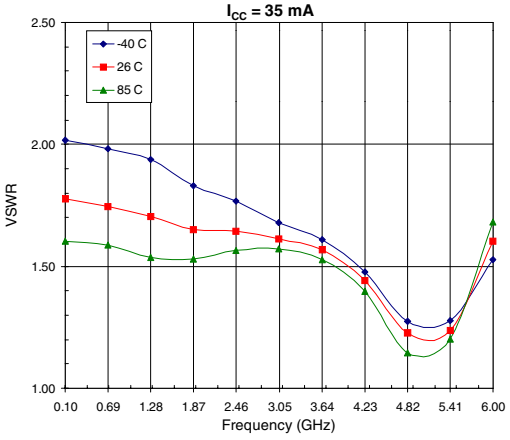
Noise Figure versus Frequency Across Temperature
I_{CC} = 35 mA



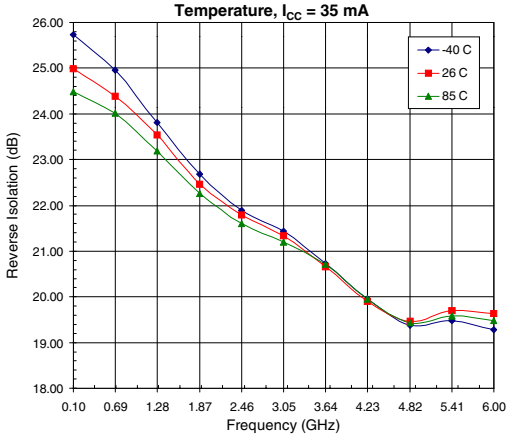
Input VSWR versus Frequency Across Temperature
I_{CC} = 35 mA



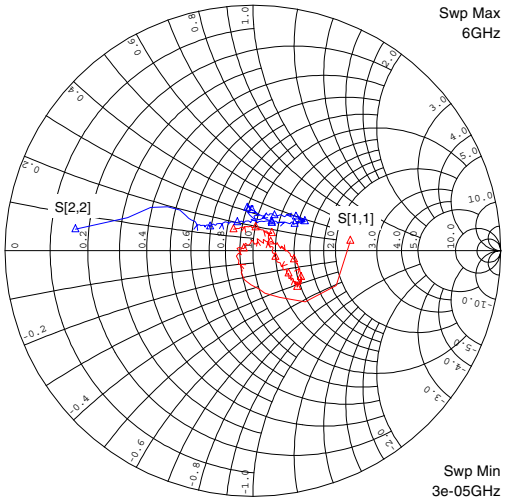
Output VSWR versus Frequency Across Temperature
I_{CC} = 35 mA



Reverse Isolation versus Frequency Across Temperature, I_{CC} = 35 mA



50 Ohm, 35 mA



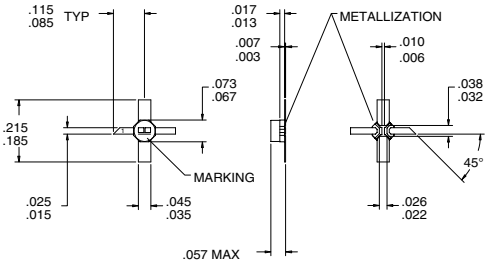
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Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- High Reliability Applications
- Broadband Test Equipment

Product Description

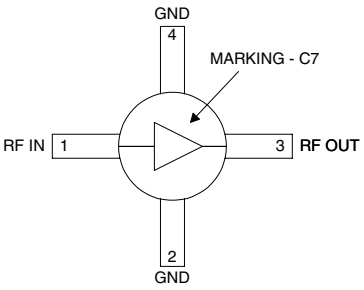
The RF2047 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. With a goal of enhanced reliability, the extremely small Micro-X-CF ceramic package offers significantly lower thermal resistance than similar size plastic packages.



Package Style: Micro-X-CF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to 6000MHz Operation
- Internally matched Input and Output
- 16dB Small Signal Gain
- +26dBm Output IP3
- +12dBm Output Power
- Excellent Gain Flatness

Ordering Information

RF2047	General Purpose Amplifier
RF2047 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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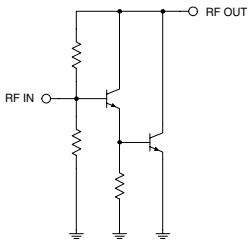
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	75	mA
Input RF Power	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

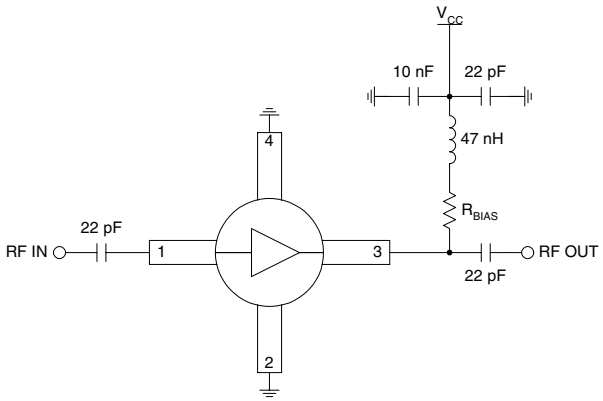
Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_D=3.6V, I_{CC}=40mA
Frequency Range		DC to 6000		MHz	
3dB Bandwidth		>6		GHz	
Gain		16.3		dB	Freq=100MHz
		16.0		dB	Freq=1000MHz
	14.0	15.3		dB	Freq=2000MHz
		15.0		dB	Freq=3000MHz
		14.8		dB	Freq=4000MHz
		14.0		dB	Freq=6000MHz
Gain Flatness		±0.5		dB	100MHz to 2000MHz
Noise Figure		4.2		dB	Freq=2000MHz
Input VSWR		1.8:1			In a 50Ω system, DC to 3000MHz
		1.6:1			In a 50Ω system, 3000MHz to 6000MHz
Output VSWR		1.7:1			In a 50Ω system, DC to 3000MHz
		2.2:1			In a 50Ω system, 3000MHz to 6000MHz
Output IP_3		+26		dBm	Freq=2000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+11.9		dBm	Freq=2000MHz
Reverse Isolation		19.4		dB	Freq=2000MHz
Thermal					I_{CC}=40mA, P_{DISS}=135mW
$Theta_{JC}$		196		°C/W	
Maximum junction temperature		112		°C	
Mean Time Between Failures		$1.5x10^4$		years	T_{AMB}=+85°C
Mean Time Between Failures		$9.3x10^6$		years	T_{AMB}=+25°C
Mean Time Between Failures		$2.9x10^{11}$		years	T_{AMB}=-40°C
Power Supply					With 22Ω bias resistor
Device Operating Voltage	3.0	3.6	4.0	V	At pin 3 with I_{CC}=40mA
Operating Current		40		mA	

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 75 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
4	GND	Same as pin 2.	

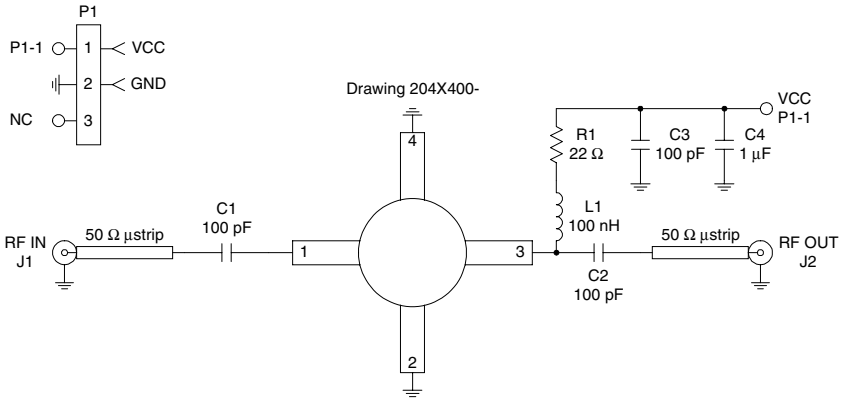
Application Schematic



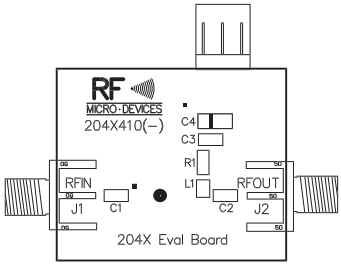
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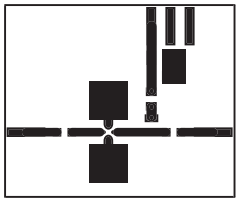
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

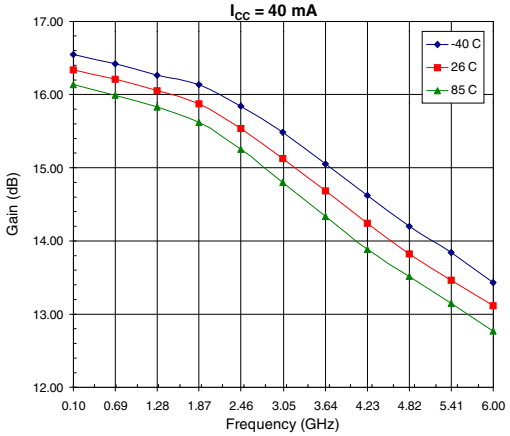


Evaluation Board Layout
Board Size 1.195" x 1.000"

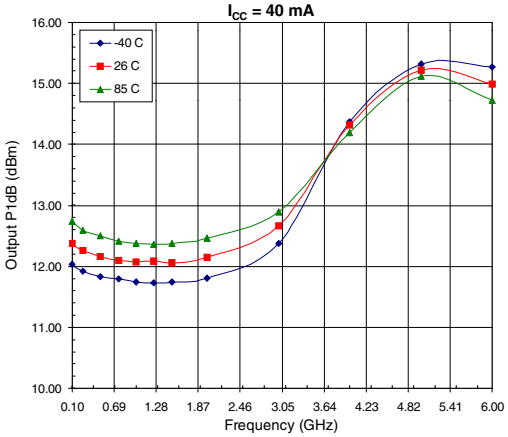




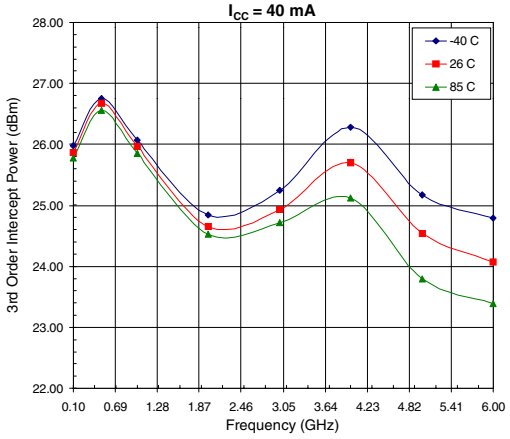
Gain versus Frequency Across Temperature
I_{CC} = 40 mA



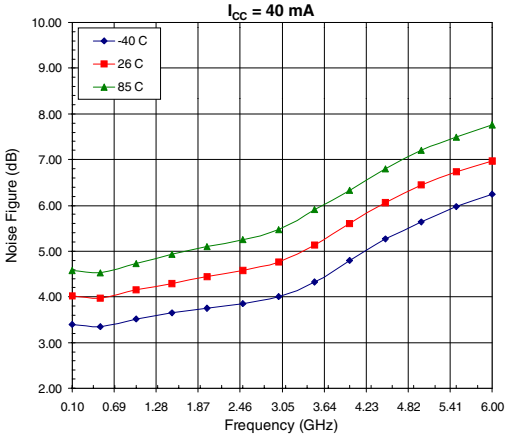
Output P1dB versus Frequency Across Temperature
I_{CC} = 40 mA



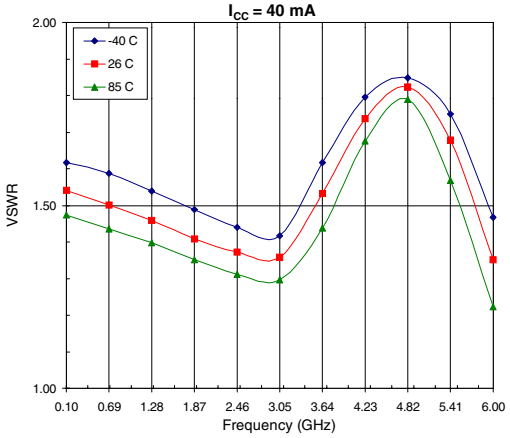
Output IP3 versus Frequency Across Temperature
I_{CC} = 40 mA



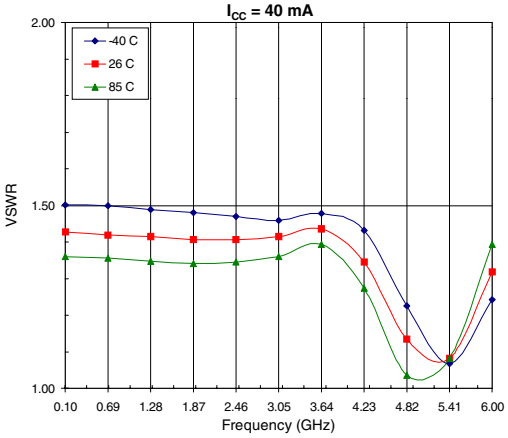
Noise Figure versus Frequency Across Temperature
I_{CC} = 40 mA

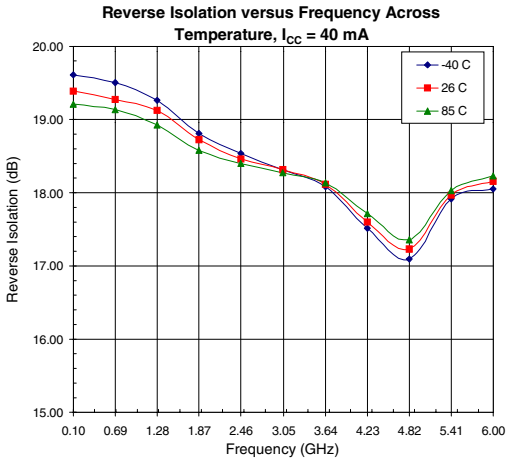


Input VSWR versus Frequency Across Temperature
I_{CC} = 40 mA



Output VSWR versus Frequency Across Temperature
I_{CC} = 40 mA




Reverse Isolation versus Frequency Across Temperature, I_{CC} = 40 mA
-40 C
26 C
85 C
Reverse Isolation (dB)
20.00
19.00
18.00
17.00
16.00
15.00
0.10
0.69
1.28
1.87
2.46
3.05
3.64
4.23
4.82
5.41
6.00
Frequency (GHz)

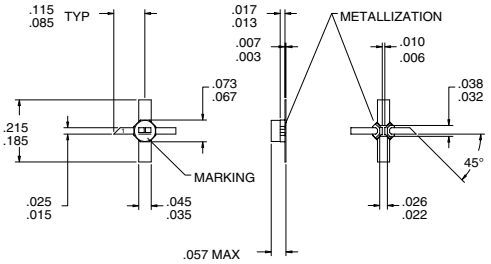
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Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- High Reliability Applications
- Broadband Test Equipment

Product Description

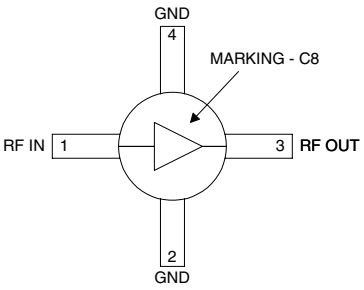
The RF2048 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 8000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. With a goal of enhanced reliability, the extremely small Micro-X-CF ceramic package offers significantly lower thermal resistance than similar size plastic packages.



Package Style: Micro-X-CF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- DC to 8000MHz Operation
- Internally matched Input and Output
- 12dB Small Signal Gain
- +26dBm Output IP3
- +12dBm Output Power
- Single Positive Power Supply

Ordering Information

RF2048	General Purpose Amplifier
RF2048 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

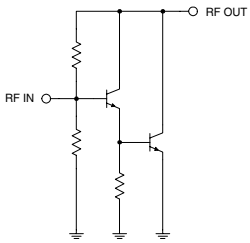
Parameter	Rating	Unit
Supply Current	75	mA
Input RF Power	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

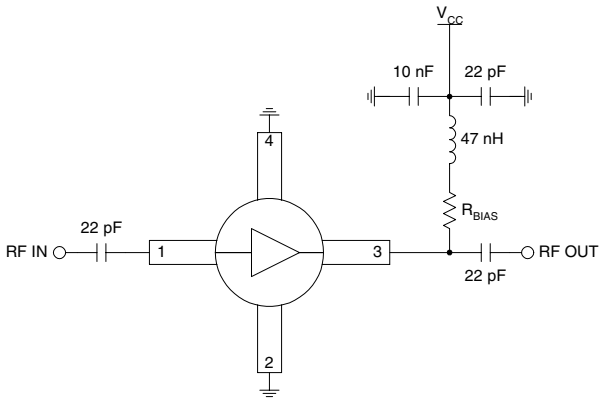
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_D=3.6V, I_{CC}=40mA
Frequency Range		DC to 8000		MHz	
Gain		12.2		dB	Freq=100MHz
		12.1		dB	Freq=1000MHz
	10	11.8		dB	Freq=2000MHz
		11.5		dB	Freq=3000MHz
		11.3			Freq=4000MHz
		11.0			Freq=6000MHz
		10.2			Freq=8000MHz
Gain Flatness		±0.2		dB	100MHz to 2000MHz
Noise Figure		5.3		dB	Freq=2000MHz
Input VSWR		1.6:1			In a 50Ω system, DC to 3000MHz
		1.8:1			In a 50Ω system, 3000MHz to 8000MHz
Output VSWR		1.5:1			In a 50Ω system, DC to 3000MHz
		1.9:1			In a 50Ω system, 3000MHz to 8000MHz
Output IP_3		+26		dBm	Freq=2000MHz±100kHz, P_{TONE}=-5dBm
Output P_{1dB}		+11.7		dBm	Freq=2000MHz
Reverse Isolation		16.6		dB	Freq=2000MHz
Thermal					I_{CC}=40mA, P_{DISS}=137mW
$Theta_{JC}$		213		°C/W	
Maximum junction temperature		115		°C	
Mean Time Between Failures		$1.2x10^4$		years	T_{AMB}=+85°C
Mean Time Between Failures		$6.6x10^6$		years	T_{AMB}=+25°C
Mean Time Between Failures		$1.7x10^{11}$		years	T_{AMB}=-40°C
Power Supply					With 22Ω bias resistor
Operating Device Voltage	3.0	3.6	4.0	V	At pin 3 with I_{CC}=40mA
Operating Current		40		mA	

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 75 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
4	GND	Same as pin 2.	

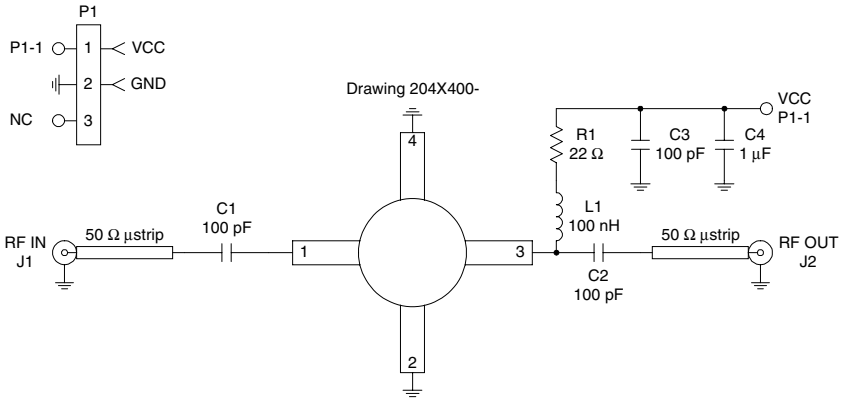
Application Schematic



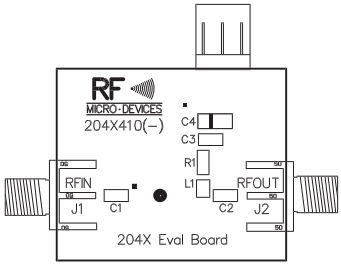
Db00.bk Page 34 Thursday, January 6, 2000 6:50 PM

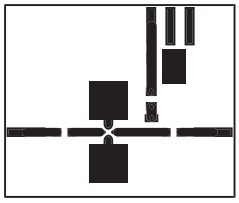
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



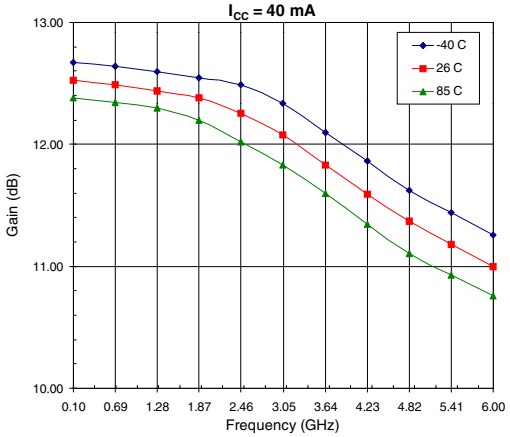
Evaluation Board Layout
Board Size 1.195" x 1.000"



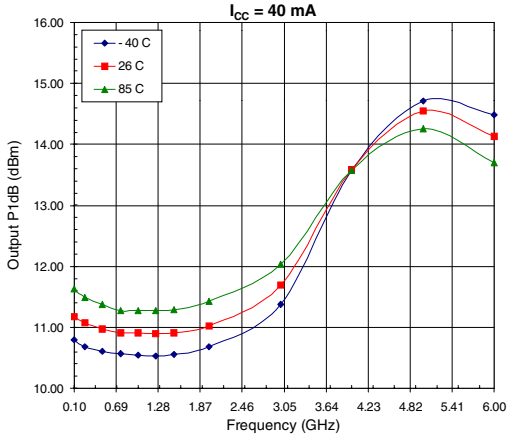


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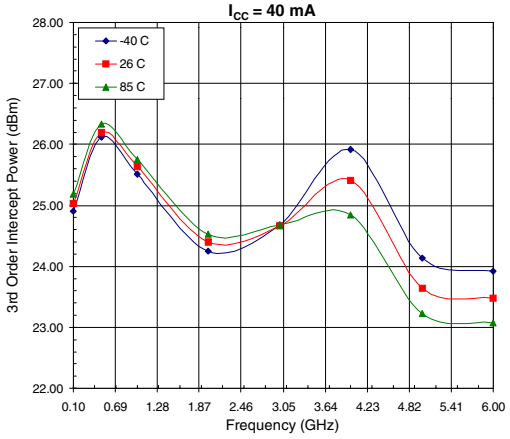
Gain versus Frequency Across Temperature
I_{CC} = 40 mA



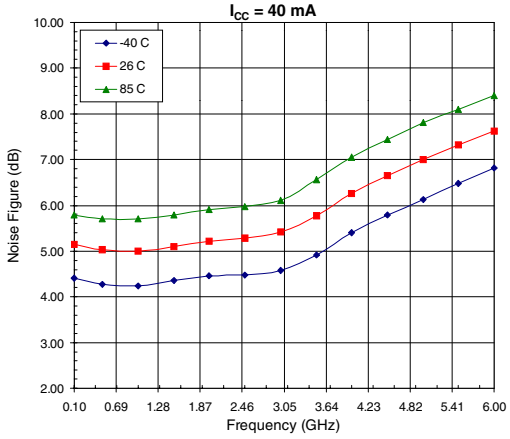
Output P1dB versus Frequency Across Temperature
I_{CC} = 40 mA



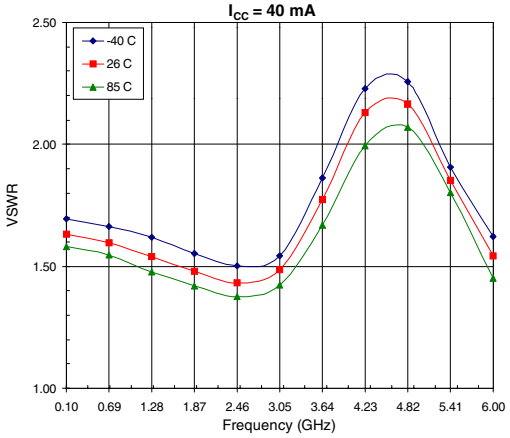
Output IP3 versus Frequency Across Temperature
I_{CC} = 40 mA



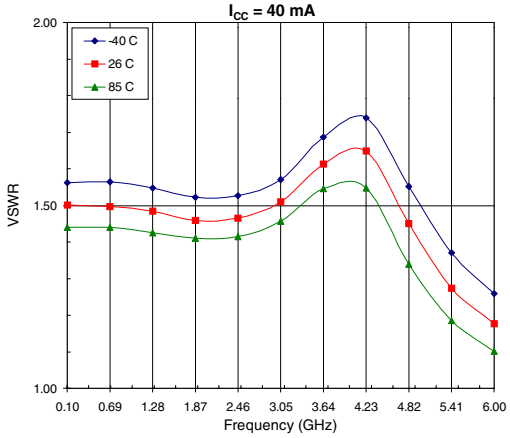
Noise Figure versus Frequency Across Temperature
I_{CC} = 40 mA

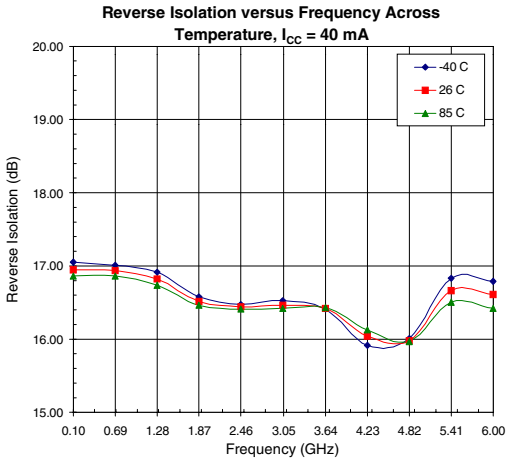


Input VSWR versus Frequency Across Temperature
I_{CC} = 40 mA



Output VSWR versus Frequency Across Temperature
I_{CC} = 40 mA




Reverse Isolation versus Frequency Across Temperature, I_{CC} = 40 mA
-40 C
26 C
85 C
Reverse Isolation (dB)
20.00
19.00
18.00
17.00
16.00
15.00
0.10
0.69
1.28
1.87
2.46
3.05
3.64
4.23
4.82
5.41
6.00
Frequency (GHz)

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RF2301

HIGH ISOLATION BUFFER AMPLIFIER

Typical Applications

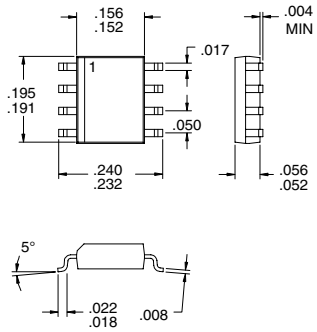
- Local Oscillator Buffer Amplifiers
- FDD and TDD Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- Wireless LAN
- ISM Band Applications

Product Description

The RF2301 is a high reverse isolation buffer amplifier. The device is manufactured on a low-cost Gallium Arsenide MESFET process, and has been designed for use as a general purpose buffer in high-end communication systems operating at frequencies from less than 300MHz to higher than 2500MHz. With +5dBm output power, it may also be used as a driver in transmitter applications. The device is packaged in an 8-lead plastic package. The product is self-contained, requiring just a resistor and blocking capacitors to operate. The output power, combined with 50dB reverse isolation at 900MHz allows excellent buffering of LO sources to impedance changes. The device can be used in 3V battery applications. The unit has a total gain of 17dB with only 14mA current from a 3V supply.

Optimum Technology Matching® Applied

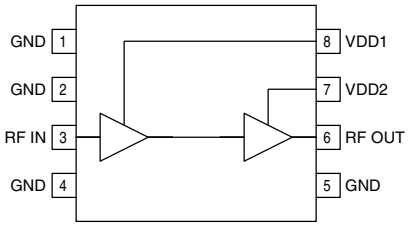
- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Package Style: SOP-8

Features

- Single 2.7V to 6.0V Supply
- +4dBm Output Power
- 21dB Small Signal Gain
- 50dB Reverse Isolation at 900MHz
- Low DC Current Consumption of 14mA
- 300MHz to 2500MHz Operation



Functional Block Diagram

Ordering Information

RF2301	High Isolation Buffer Amplifier
RF2301 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2301

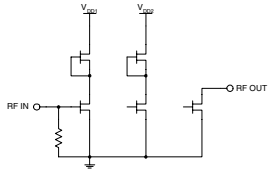
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +6.5	V_{DC}
DC Supply Current	60	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

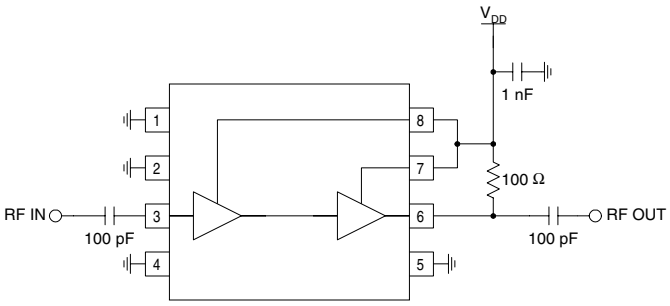
Caution! ESD sensitive device.

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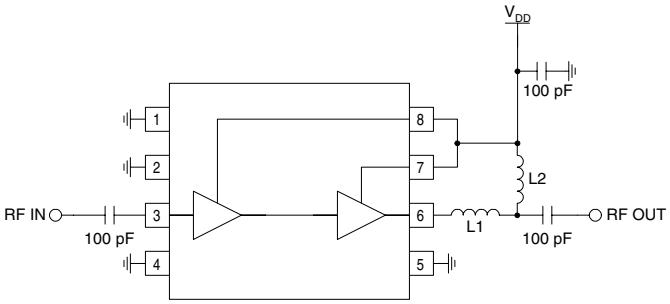
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=5V_{DC}
Nominal Frequency Range		300 to 2500		MHz	
Input IP_3		-8		dBm	
Noise Figure			8	dB	
Input VSWR		<2:1			In a 50Ω system
Output VSWR		<2:1			In a 50Ω system
Power Supply Voltage		2.7 to 6.0		V	
Nominal 5V Configuration					Using Broad Band Application Circuit, V_{DD}=5V_{DC}, Freq=2500MHZ, T=25°C
Gain	17	21	25	dB	
P_{1dB} Output Power		+4		dBm	
Supply Current	10	30	40	mA	
Reverse Isolation		50		dB	900MHz, without RF input
		50		dB	900MHz, with RF input, saturated
		40		dB	2500MHz, without RF input
		40		dB	2500MHz, with RF input, saturated
Nominal 3V Configuration					Using Broad Band Application Circuit, V_{DD}=3V_{DC}, Freq=2500MHZ, T=25°C
Gain	15	17		dB	
P_{1dB} Output Power		0		dBm	
Supply Current		14		mA	
Reverse Isolation		50		dB	900MHz, without RF input
		50		dB	900MHz, with RF input, saturated
		40		dB	2500MHz, without RF input
		40		dB	2500MHz, with RF input, saturated

Pin	Function	Description	Interface Schematic
1	GND	Low inductance ground connections. Use individual vias to backside ground plane, placed within 0.030" of pin landing for optimum performance.	
2	GND	Same as pin 1.	
3	RF IN	DC coupled RF input. A broadband impedance match is produced by internal shunt resistive feedback. The DC level is 0V. If a DC voltage is present from connected circuitry, an external DC blocking capacitor is required for the proper DC operating point.	
4	GND	Same as pin 1.	
5	GND	Same as pin 1.	
6	RF OUT	Open drain RF output. A broadband impedance match is produced by an external 100Ω resistor to power supply as shown in Application Schematic 1. Approximately 3dB improvement in gain and output power can be obtained over at least a 20% bandwidth by replacing the resistor to power supply with an external chip inductor network as shown in Application Schematic 2. An external DC blocking capacitor is required if the following circuitry is not DC blocked.	
7	VDD2	Power supply connections. Bypass with external chip capacitor and individual via to backside ground plane.	
8	VDD1	Power supply connections. Bypass with external chip capacitor and individual via to backside ground plane.	

Application Schematic 1
Broadband Match



Application Schematic 2
Optimum Match

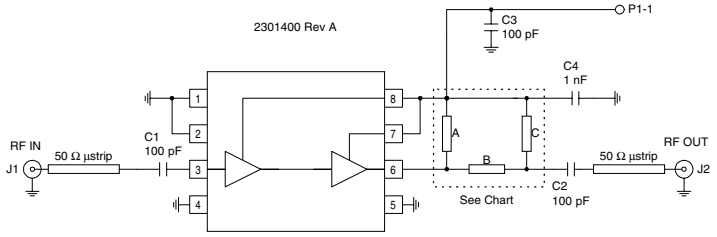


FREQUENCY	L1	L2
900 MHz	18 nH	22 nH
2500 MHz	—	2.7 nH

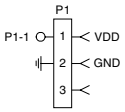
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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

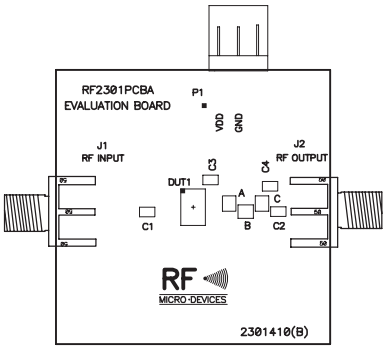


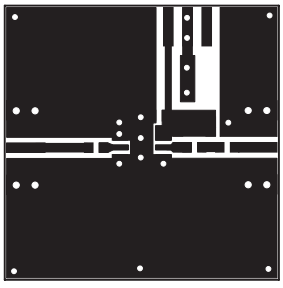
FREQUENCY BAND	COMPONENT		
	A	B	C
BROADBAND (default config.)	100 Ω	0 Ω	N/A
900 MHz	N/A	18 nH	22 nH
2450 MHz	2.7 nH	0 Ω	N/A



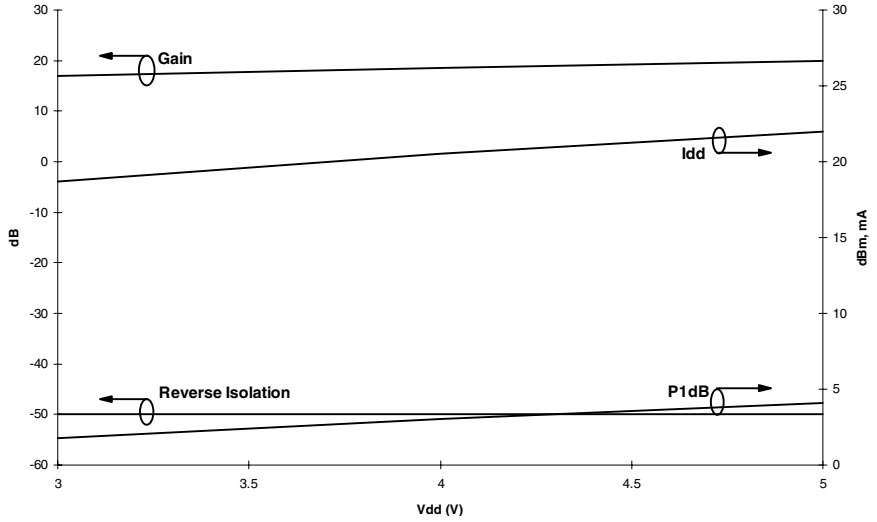
Evaluation Board Layout
1.43” x 1.43”

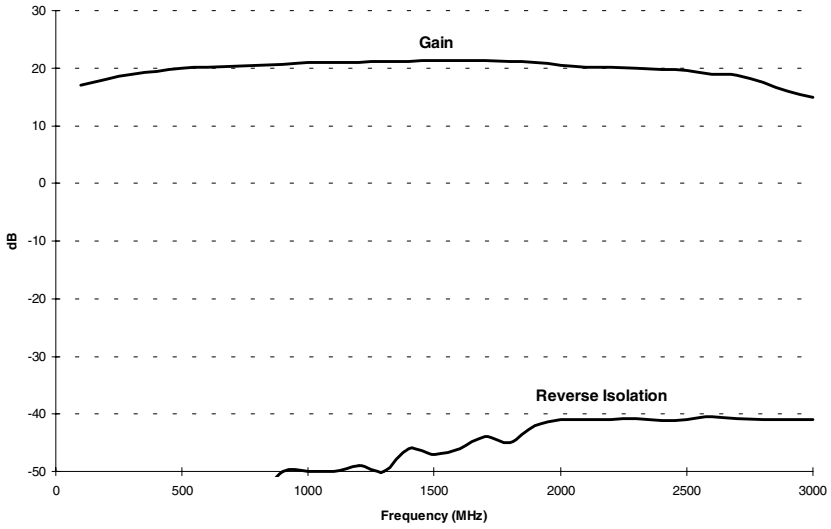
Board Thickness 0.031”; Board Material FR-4





Typical Characteristics
Broadband Application Circuit





RF2302

BROADBAND LINEAR VARIABLE GAIN AMPLIFIER

Typical Applications

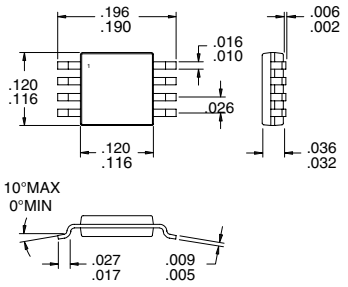
- CDMA Cellular/PCS and JCDMA Systems
- TDMA Cellular/PCS Systems
- GSM Systems
- Wireless Local Loop Systems
- Wideband CDMA Systems
- PDC Systems (950MHz and 1450MHz)

Product Description

The RF2302 is a broadband linear variable gain amplifier that was designed specifically for digital communications systems that require linear amplification over a wide gain control range. It is suitable for use in CDMA or TDMA systems in the cellular or PCS band, in DAMPS systems, and in PDC systems. Operating supply voltage ranges from 3V to 6V. The device operates over a large frequency band, from 100MHz to 2000MHz, and is tuned to a specific frequency band with an output bias feed inductor and blocking capacitor. Bias optimization may be achieved by adjusting the voltage to pin 8 (PD). The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process and is featured in a new standard miniature 8-lead plastic MSOP package.

Optimum Technology Matching® Applied

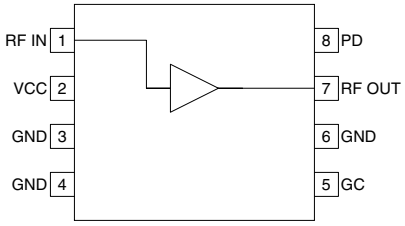
- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Package Style: MSOP-8

Features

- 25dB Linear Gain Control range
- +14dBm OP1dB at 3.5V (836MHz)
- Single 3V to 6V Supply
- 14dB Max Gain at 836MHz
- 10dB Max Gain at 1900MHz
- 4dB Noise Figure at 836MHz



Functional Block Diagram

Ordering Information

RF2302	Broadband Linear Variable Gain Amplifier
RF2302 PCBA-L	Fully Assembled Evaluation Board 836MHz
RF2302 PCBA-H	Fully Assembled Evaluation Board 1.88GHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2302

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Power Down Voltage	0 to +3.1	V_{DC}
Gain Control Voltage	0 to +3.1	V_{DC}
DC Current	100	mA
Output Load VSWR	12:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

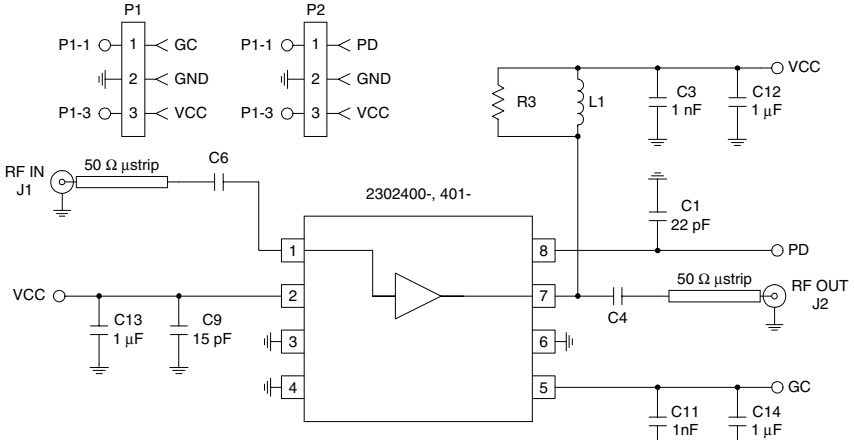
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=3.5V, V_{PD}=2.8V, V_{GC}=2.2V, T=25°C
RF Frequency Range	100		2000	MHz	
Small Signal Maximum Gain	12	14		dB	Freq=836MHz
	8	10		dB	Freq=1900MHz
Small Signal Minimum Gain		-11		dB	Freq=836MHz
		-15		dB	Freq=1900MHz
Noise Figure		4		dB	Freq=836MHz
		7		dB	Freq=1900MHz
Linear Gain Control Range	25			dB	V_{GC}=0.5V to 2.2V
Gain Control Slope	1		3	V/V	Slope=ΔOutput peak voltage/ΔV_{GC}
Output P_{1dB}		+14		dBm	Freq=836 MHz, V_{CC}=3.5V at max gain
		+13		dBm	Freq=836 MHz, V_{CC}=3.0V at max gain
		+10		dBm	Freq=1900 MHz, V_{CC}=3.0V at max gain
Input P_{1dB}		-5		dBm	Freq=836MHz; over entire V_{GC} range
		-3		dBm	Freq=1900MHz; over entire V_{GC} range
Input VSWR		1.8:1	3:1		In 50Ω system; over entire V_{GC} range
Output VSWR		2.5:1			In 50Ω system
Power Supply					T=25°C
Supply Voltage	3		6	V	
Power Down Voltage High	2.7		2.9	V	Specifications
Power Down Voltage Low			1.0		
DC Current Consumption		35		mA	V_{CC}=3.5V, V_{PD}=2.8V, V_{GC}=2.2V
V_{PD} Current		7		mA	V_{PD}=2.8V
V_{GC} Current		33	60	µA	V_{GC}=2.2V
Power Down Current			10	µA	V_{PD}<1V, V_{GC}<1V
Turn On/Off Time			100	nS	

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is DC coupled and requires a blocking capacitor.	
2	VCC	Power supply. This pin is connected to a battery or a regulated supply and requires a bypass capacitor as close to the pin as possible.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
5	GC	Analog gain control pin. This pin controls the gain of the IC. Minimum gain occurs at V_{GC}<1V and maximum gain is achieved with V_{GC}=2.2V. 25dB of linear gain control with no variation of input P_{1dB} is available, and additional attenuation is possible with V_{GC}<1V with input P_{1dB} variation. Bypass this pin near the device.	
6	GND	Same as pin 3.	
7	RF OUT	RF output pin. This pin is DC coupled and requires V_{CC} through a bias inductor sized accordingly to provide a high pass transformation with a series capacitor. This LC transformation sets the output load line for the amplifier. If this amplifier is driving a power amplifier or antenna, no additional matching is required. However, to improve the output match, a parallel resistor can be added across the inductor. For 836MHz applications use a 10nH bias inductor (optional resistor R3=100 ohms) and 2.7pF coupling capacitor. For 1900MHz applications use a 2.7nH bias inductor (optional resistor R3=150ohms) and 1.0pF coupling capacitor.	
8	PD	Power down pin. This pin provides bias for the amplifier. To turn the amplifier on, this pin should be at 2.8V. Reducing this voltage below 0.5V ensures that the amplifier will draw less than 10µA current from the supply. Additionally, bias current can be optimized for lower output power by adjusting this voltage over a 2.7V to 2.9V range from a regulated supply.	

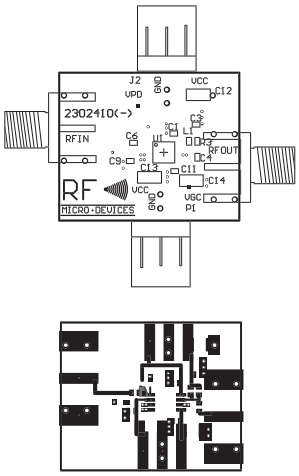
Evaluation Board Schematic
836 MHz or 1900 MHz

(Download Bill of Materials from www.rfmd.com.)

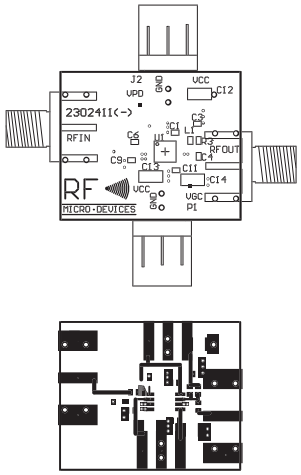


Board	C6 (pF)	R3 (Ω)	L1 (nH)	C4 (pF)
L (836 MHz)	12	100	10	2.7
H (1900 MHz)	3.3	150	2.7	1

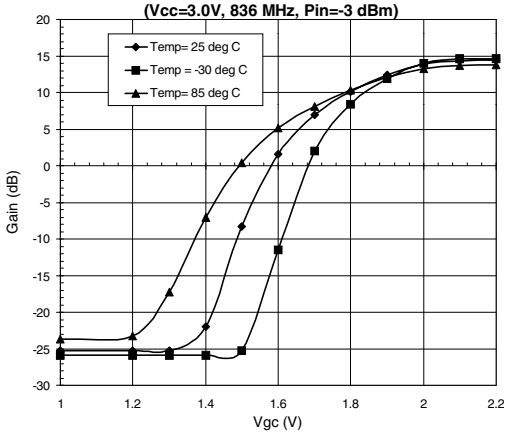
Evaluation Board Layout 836MHz
Board Size 2.0” x 2.0”



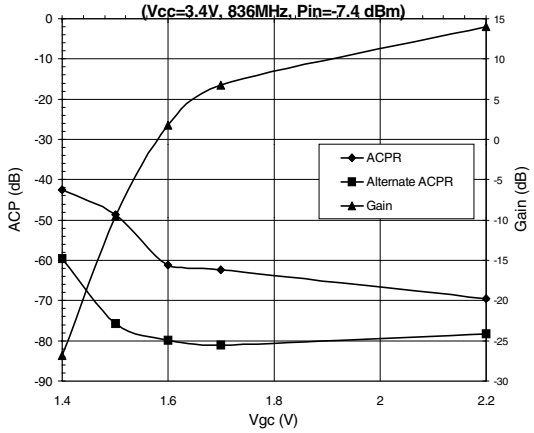
Evaluation Board Layout 1.88GHz
Board Size 2.0” x 2.0”



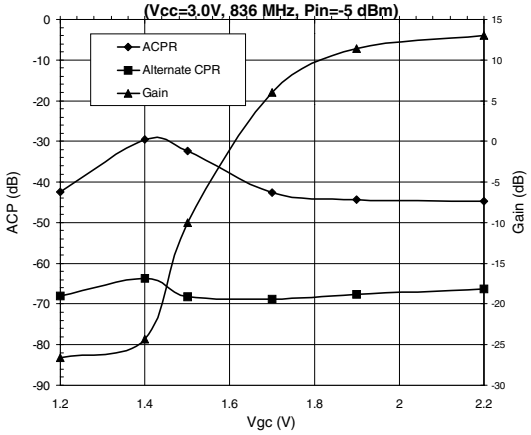
RF2302 Gain vs. Gain Control Voltage
(Vcc=3.0V, 836 MHz, Pin=-3 dBm)



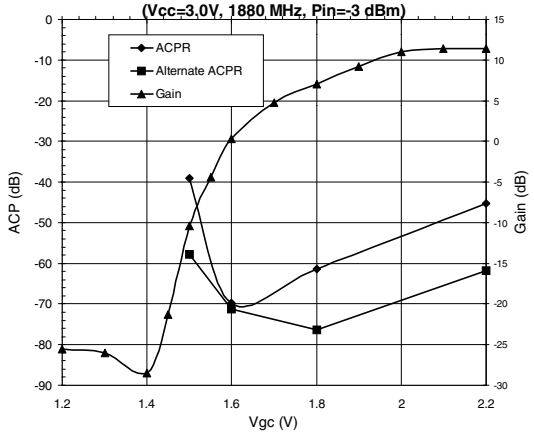
RF2302 IS95 Adj. Channel Power vs. Vgc
(Vcc=3.4V, 836MHz, Pin=-7.4 dBm)



RF2302 NADC Adj. Channel Power vs. Vgc
(Vcc=3.0V, 836 MHz, Pin=-5 dBm)

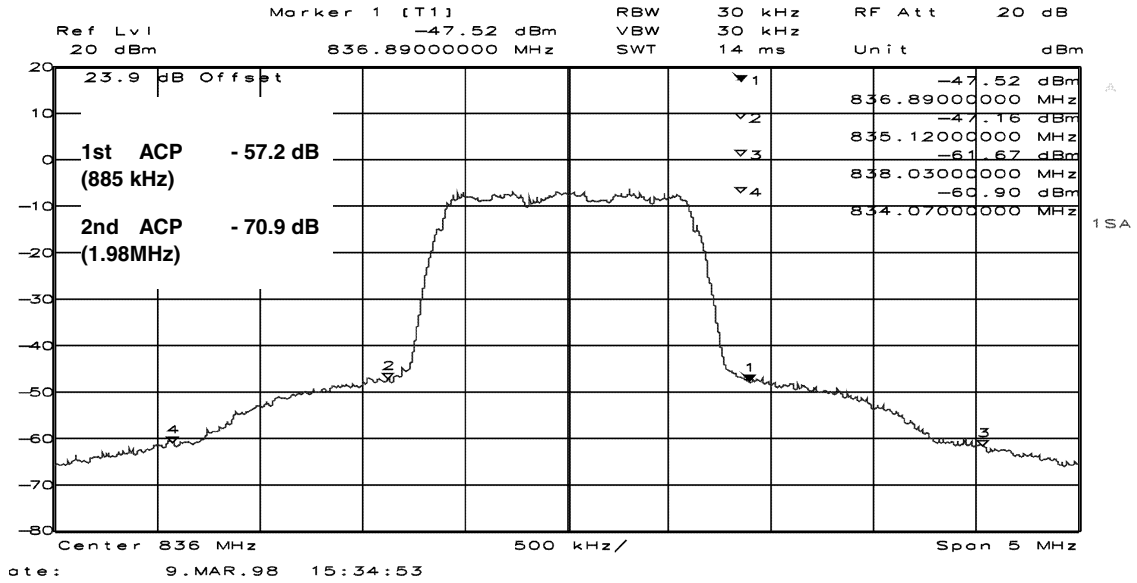


RF2302 PCS1800 CDMA Adj. Channel Power vs. Vgc
(Vcc=3.0V, 1880 MHz, Pin=-3 dBm)



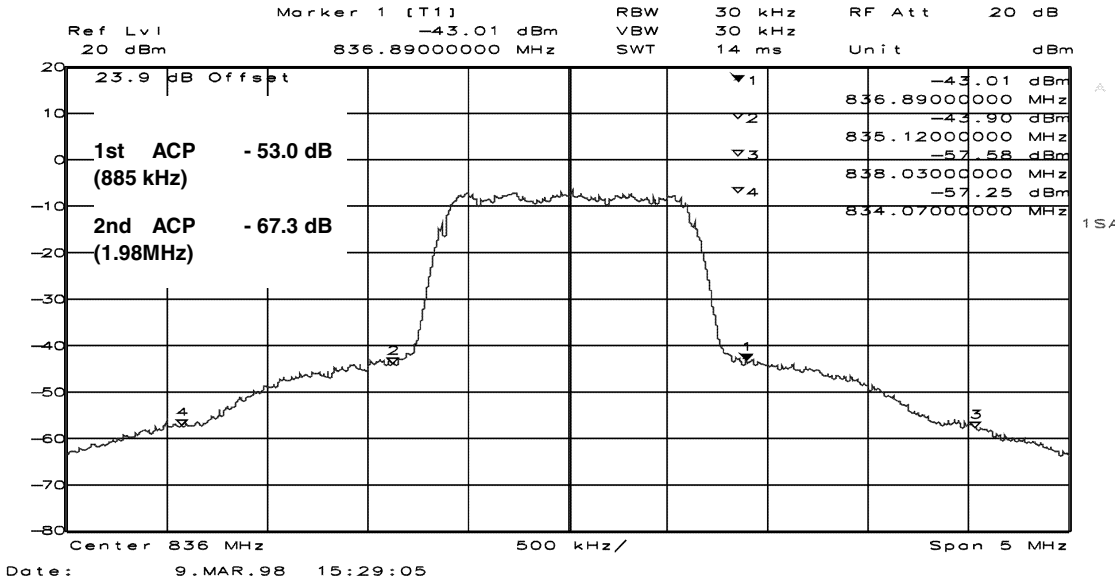
RF2302 IS95 Adjacent Channel Power (Pout= +10dBm)

(Frequency=836MHz, Vcc=3.5V, Vgc=2.2V, Pin=-2.5dBm)



RF2302 IS95 Adjacent Channel Power (Pout= +10dBm)

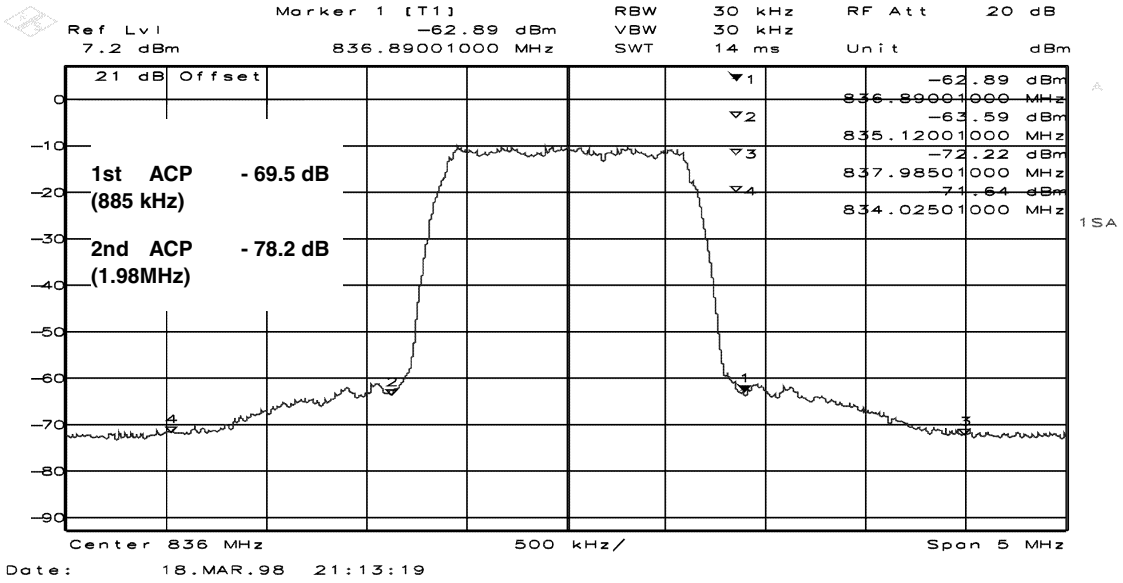
(Frequency=836MHz, Vcc=3.0V, Vgc=2.2V, Pin=-2.4dBm)



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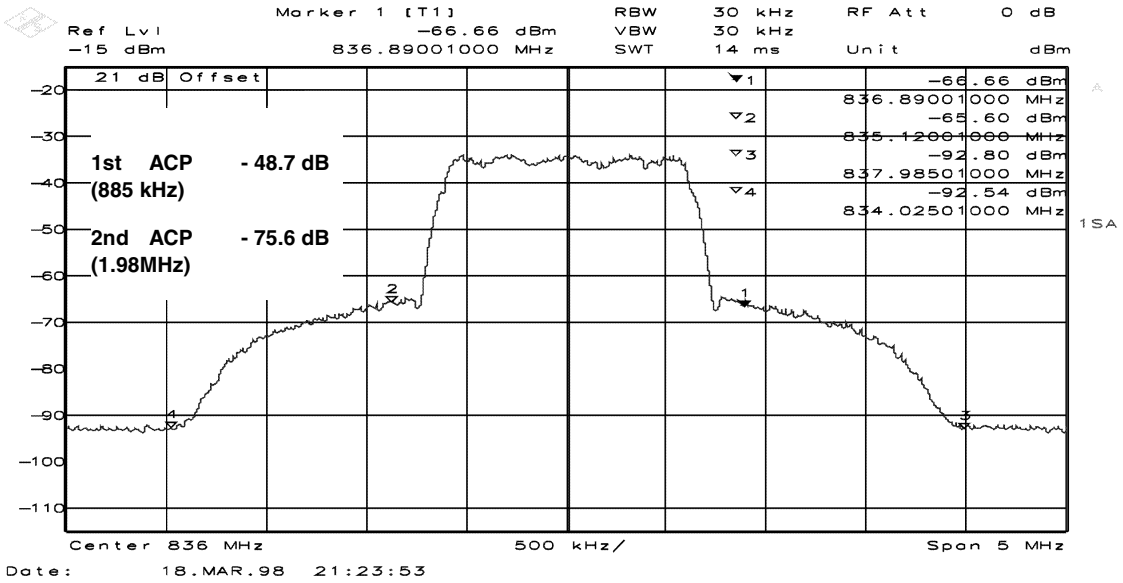
RF2302 IS95 Adjacent Channel Power (Pout= +6.63dBm)

(Frequency=836MHz, Vcc=3.4V, Vgc=2.2V, Pin=-7.4dBm)



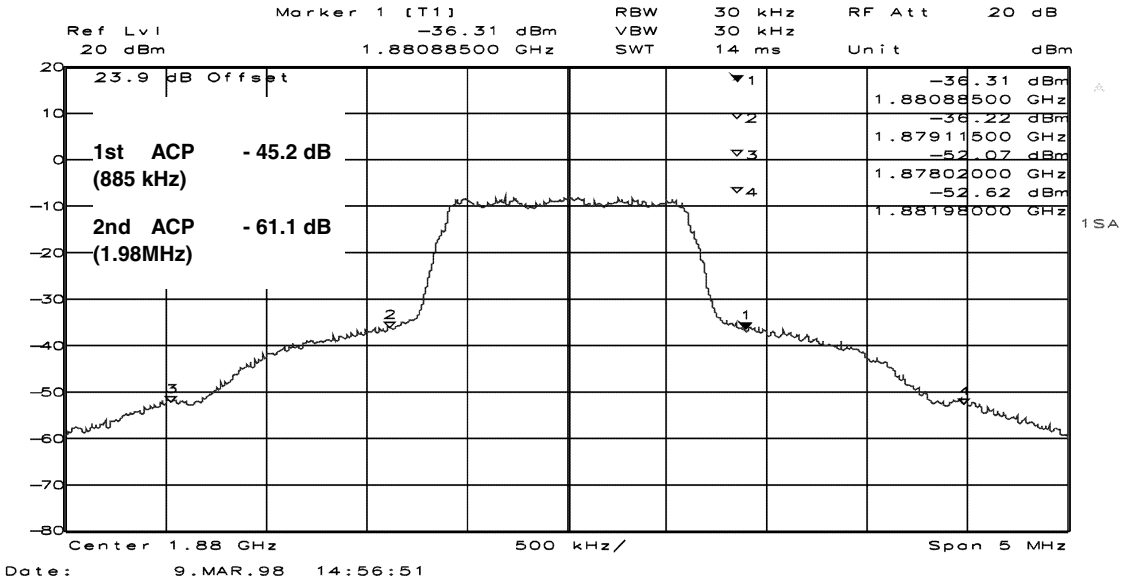
RF2302 IS95 Adjacent Channel Power (Pout= -16.9dBm)

(Frequency=836MHz, Vcc=3.4V, Vgc=1.5V, Pin=-7.4dBm)



RF2302 PCS1800 CDMA Adjacent Channel Power (Pout= 9.0dBm)

(Frequency=1880MHz, Vcc=3.5V, Vgc=2.2V, Pin=-2.3dBm)



RF MICRO·DEVICES

Preliminary

RF2303

BROADBAND LINEAR VARIABLE GAIN AMPLIFIER

Typical Applications

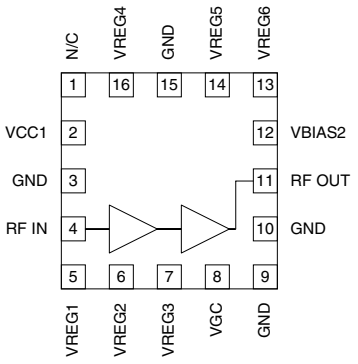
- CDMA Cellular/PCS and JCDMA Systems
- TDMA Cellular/PCS Systems
- Wideband CDMA Systems
- Wireless Local Loop Systems
- GSM Systems
- PDC Systems (950MHz and 1450MHz)

Product Description

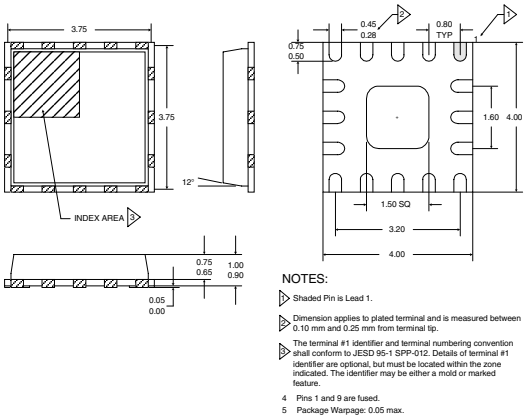
The RF2303 is a broadband linear variable gain amplifier that was designed specifically for digital communications systems that require linear amplification over a wide gain control range. It is suitable for use in WCDMA, as well as CDMA or TDMA systems in the cellular or PCS band, in DAMPS systems, and in PDC systems. Operating supply voltage ranges from 3V to 6V. The device operates over a large frequency band, from 100MHz to 2000MHz, and is tuned to a specific frequency band with an output bias feed inductor and blocking capacitor. Bias optimization may be achieved by adjusting the voltage to pin 5 (VREG). The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process and is featured in a 4mmx4mm leadless plastic MLF16 package.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: MLF16

Features

- 58dB Linear Gain Control range
- Single 3V to 6V Supply
- 25dB Max Gain at 1900MHz
- 4dB Min Noise Figure at 1900MHz

Ordering Information

RF2303	Broadband Linear Variable Gain Amplifier
RF2303 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Power Down Voltage	0 to +3.1	V_{DC}
Gain Control Voltage	0 to +3.1	V_{DC}
DC Current	100	mA
Output Load VSWR	12:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

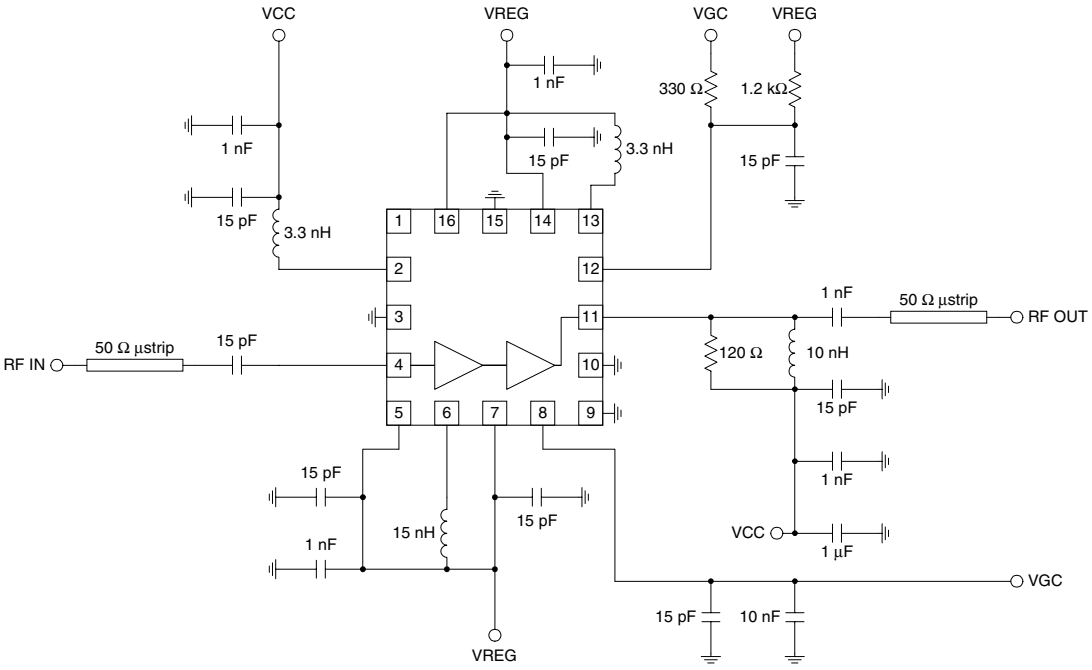
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=3.4V, V_{REG}=2.8V, V_{GC}=2.0V, T=25°C
RF Frequency Range	100		2000	MHz	
Small Signal Maximum Gain		23		dB	Freq=1900MHz
Small Signal Minimum Gain		-35		dB	Freq=1900MHz
Minimum Noise Figure		4			Freq=1900MHz
Linear Gain Control Range		50		dB	V_{GC}=0.5V to 2.0V
Gain Control Slope		TBD		V/V	Slope=ΔOutput peak voltage/ΔV_{GC}
Output P_{1dB}		16		dBm	Freq=1900 MHz, V_{CC}=3.4V at max gain
Input P_{1dB}		TBD		dBm	Freq=1900MHz; over entire V_{GC} range
Input VSWR		1.8:1	3:1		In 50Ω system; over entire V_{GC} range
Output VSWR		2.5:1			In 50Ω system
Power Supply					T=25°C
Supply Voltage	3		6	V	
Power Down Voltage High	2.7		2.9	V	Specifications
Power Down Voltage Low			1.0		
DC Current Consumption		25		mA	V_{CC}=3.4V, V_{REG}=2.8V, V_{GC}=2.0V
V_{REG} Current		TBD		µA	V_{REG}=2.8V
V_{GC} Current		15	60	µA	V_{GC}=2.0V
Power Down Current			10	µA	V_{REG}<1V, V_{GC}<1V
Turn On/Off Time			100	nS	

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Pin	Function	Description	Interface Schematic
1	N/C	Not connected.	
2	VCC1	Power supply. This pin is connected to a battery or regulated supply. A series inductor and bypass capacitor should be placed as close to the part as possible. See application schematic for recommended component values.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	RF IN	RF input pin. There is an internal blocking capacitor for this pin.	
5	VREG1	Power down pin. This pin provides bias for the amplifier. To turn the amplifier on, this pin should be at 2.8V. Reducing this voltage below 0.5V ensures that the amplifier will draw less than 10µA current from the supply. Additionally, bias current can be optimized for lower output power by adjusting this voltage over a 2.7V to 2.9V range from a regulated supply.	
6	VREG2	Power down/bias pin. An inductor should be placed in series with this pin. See application schematic for recommended inductor value.	
7	VREG3	Same as pin 5.	
8	VGC	Analog gain control pin. This pin controls the gain of the IC. Minimum gain occurs at V_{GC}<1V and maximum gain is achieved with V_{GC}=2.2V. Greater than 50dB of linear gain control with no variation of input P_{1dB} is available, and additional attenuation is possible with V_{GC}<1V with input P_{1dB} variation. Bypass this pin near the device.	
9	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
10	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
11	RF OUT	RF output and bias pin. This pin is DC coupled and requires VCC through a bias inductor sized accordingly to provide a high pass transformation with a series capacitor.	
12	VBIAS2	Bias pin. Refer to application schematic for recommended biasing scheme.	
13	VREG6	Power down/bias pin. An inductor should be placed in series with this pin. See application schematic for recommended inductor value.	
14	VREG5	Same as pin 5.	
15	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. Use a separate ground via for this pin.	
16	VREG4	Same as pin 5.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

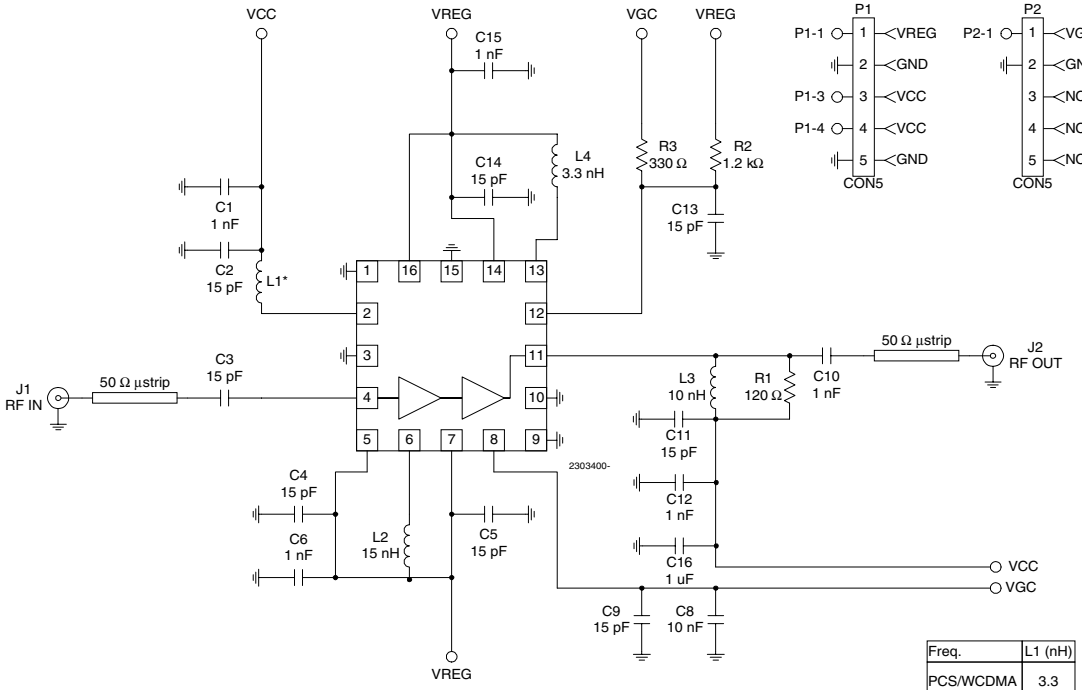
PCS Application Schematic



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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



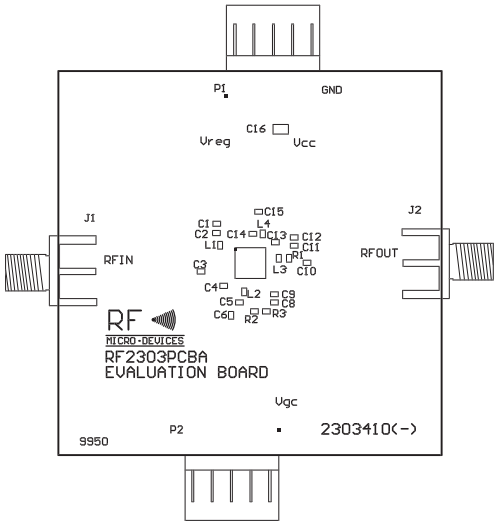
Freq.	L1 (nH)
PCS/WCDMA	3.3
Cellular	47

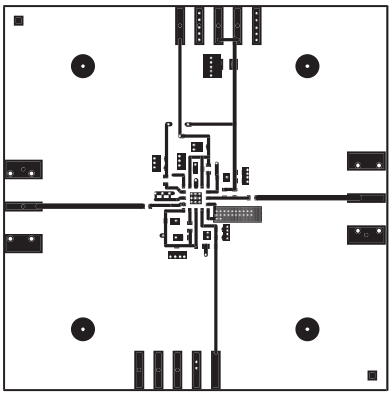
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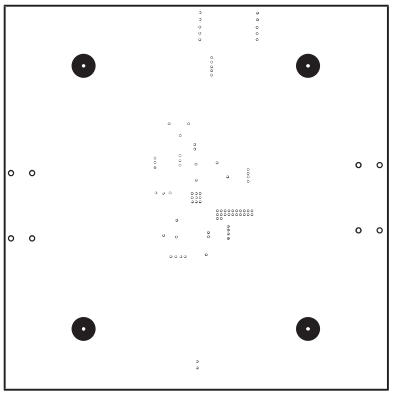
GENERAL PURPOSE AMPLIFIERS

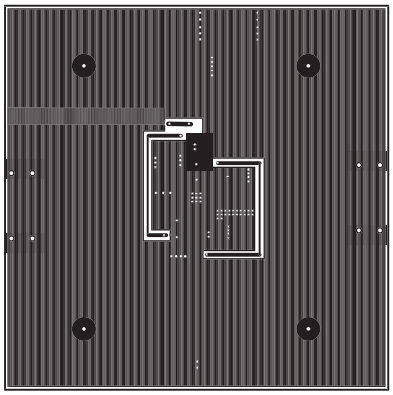
Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4









RF2304

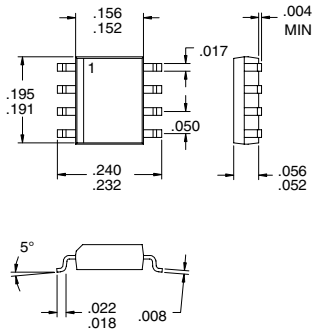
GENERAL PURPOSE LOW-NOISE AMPLIFIER

Typical Applications

- Receive or Transmit Low-Noise Amplifiers
- FDD and TDD Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- Wireless LAN
- ISM Band Applications

Product Description

The RF2304 is a low-noise small-signal amplifier. The device is manufactured on a low-cost Gallium Arsenide MESFET process, and has been designed for use as a gain block in high-end communication systems operating from less than 300MHz to above 2.5GHz. With +6dBm output power, it may also be used as a driver in transmitter applications, or in highly linear receivers. The device is packaged in an 8-lead plastic package and is self-contained, requiring just an inductor and blocking capacitors to operate. The +6dBm output power, combined with the 1.8dB noise figure at 900MHz allows excellent dynamic range for a variety of receive and transmit applications.



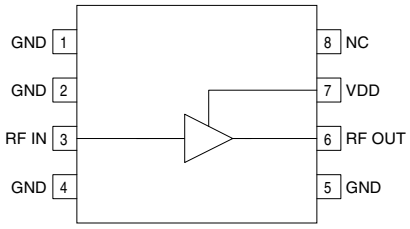
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS

Features

- Single 2.7V to 6.0V Supply
- 6dBm Output Power
- 8dB Small Signal Gain at 900MHz
- 1.8dB Noise Figure at 900MHz
- Low DC Current Consumption of 5mA
- 300MHz to 2500MHz Operation



Functional Block Diagram

Ordering Information

RF2304	General Purpose Low-Noise Amplifier
RF2304 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2304

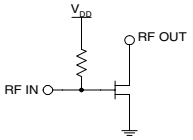
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +6.5	V_{DC}
DC Current	40	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

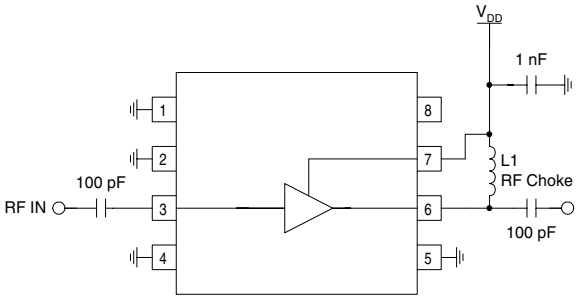
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=5V_{DC}
Nominal Frequency Range		300 to 2500		MHz	
Input IP_3		+8		dBm	
Reverse Isolation		18		dB	
Input VSWR		<2:1			In a 50Ω system
Output VSWR		<2:1			In a 50Ω system
Power Supply Voltage		2.7 to 6.0		V	
Nominal 5V Configuration					V_{DD}=5V_{DC}, Freq=2500MHz, T=25°C
Gain	6	8		dB	
P_{1dB} Output Power		+6		dBm	
Supply Current	7	11	26	mA	
Noise Figure		1.8		dB	900MHz
Noise Figure		2.3		dB	2500MHz
Nominal 3V Configuration					V_{DD}=3V_{DC}, Freq=2500MHz, T=25°C
Gain		7		dB	
P_{1dB} Output Power		+3		dBm	
Supply Current		5.5		mA	
Noise Figure		1.8		dB	900MHz
Noise Figure		2.3		dB	2500MHz

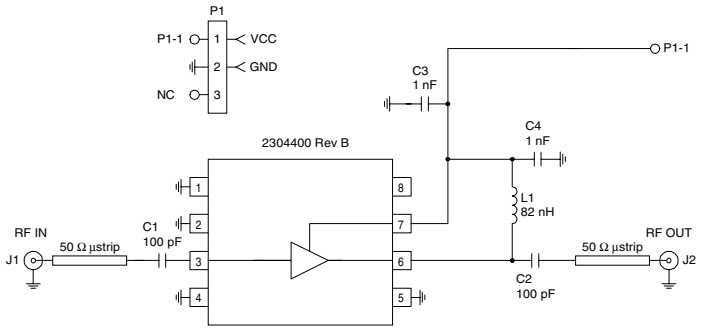
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	DC coupled RF input. A broadband impedance match is produced by internal shunt resistive feedback. The DC level is approximately 200mV. If a DC path exists in the connected circuitry, an external DC blocking capacitor is required to properly maintain the DC operating point.	
4	GND	Same as pin 1.	
5	GND	Same as pin 1.	
6	RF OUT	RF output. A broadband impedance match is produced by internal shunt resistive feedback. The DC connection to the power supply is provided through an external chip inductor having greater than 150Ω reactance at the operating frequency. An external DC blocking capacitor is required if the following circuitry is not DC blocked.	
7	VDD2	Bias control connection. This pin is normally connected to the power supply, but can be used to switch the amplifier on and off by switching between power supply voltage and ground. This pin sinks approximately 600µA when connected to V_{DD}, and sources less than 10µA when grounded.	
8	NC	No connection.	

Application Schematic

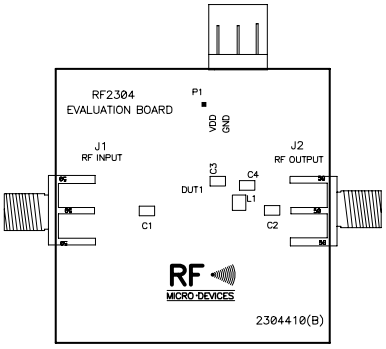


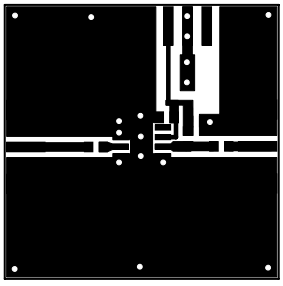
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

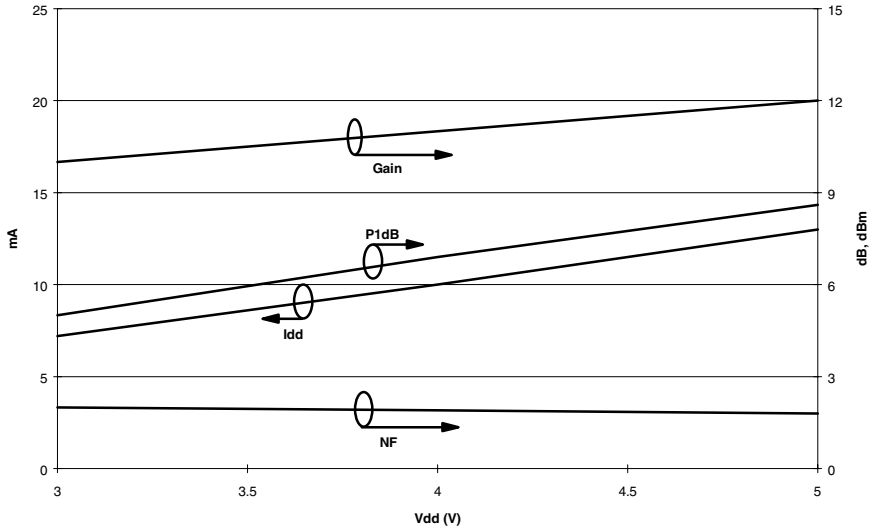


Evaluation Board Layout
1.43” x 1.43”

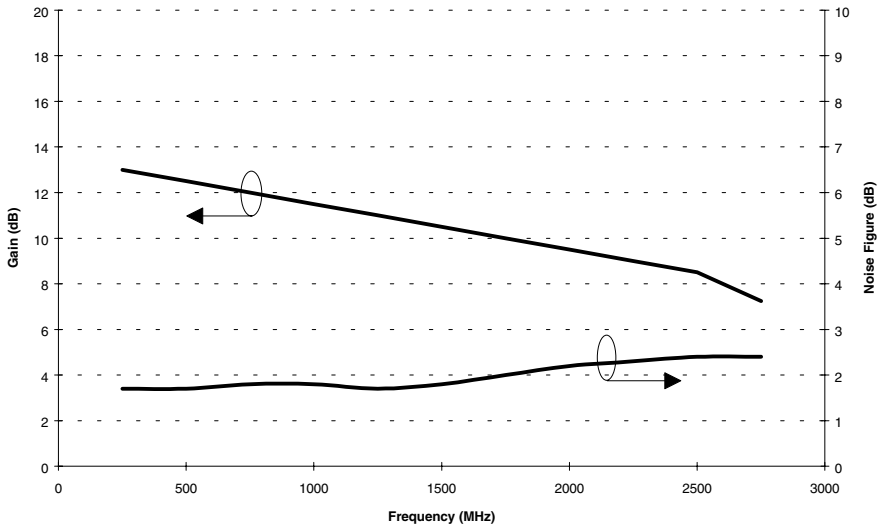




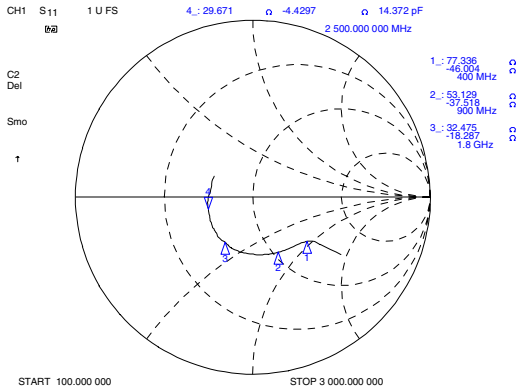
Typical Characteristics
f=900MHz

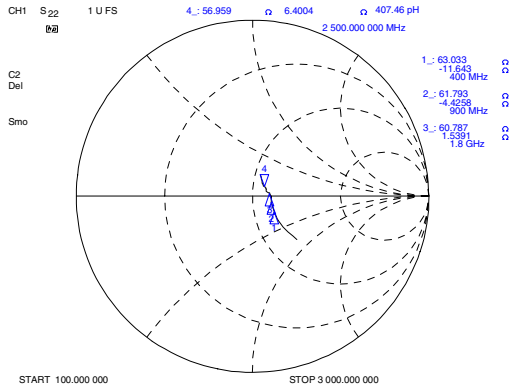


Typical Characteristics
V_{DD}=5.0V

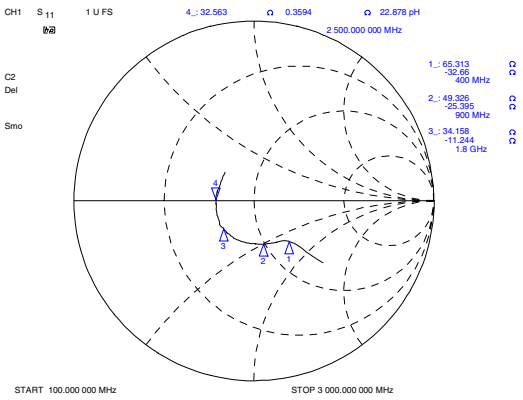


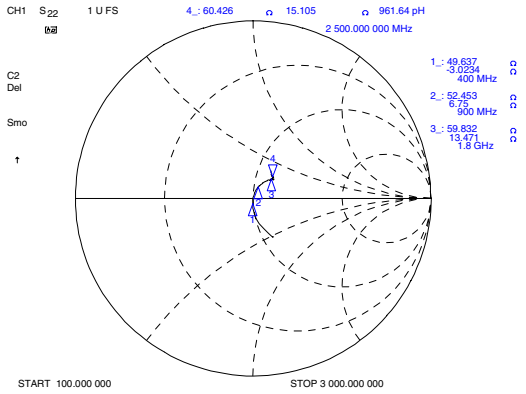
Typical Characteristics with V_{cc}=3.0V Typical Characteristics





Typical Characteristics with V_{cc}=5.0V





RF2306

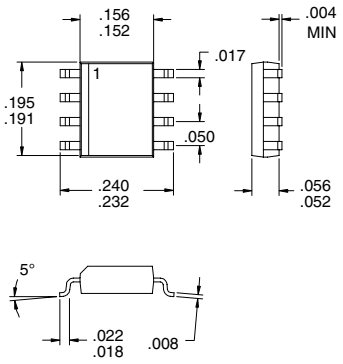
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Portable Battery Powered Equipment
- Broadband Test Equipment

Product Description

The RF2306 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 2000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified.



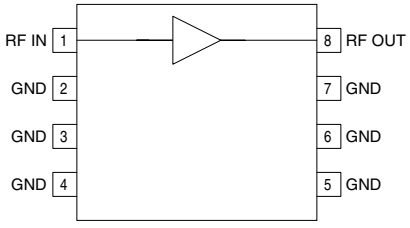
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 2000MHz Operation
- Internally matched Input and Output
- 20dB Small Signal Gain
- 3.5dB Noise Figure
- 10mW Linear Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2306	General Purpose Amplifier
RF2306 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2306

Absolute Maximum Ratings

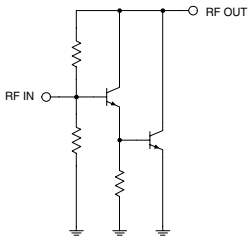
Parameter	Rating	Unit
Supply Current	65	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

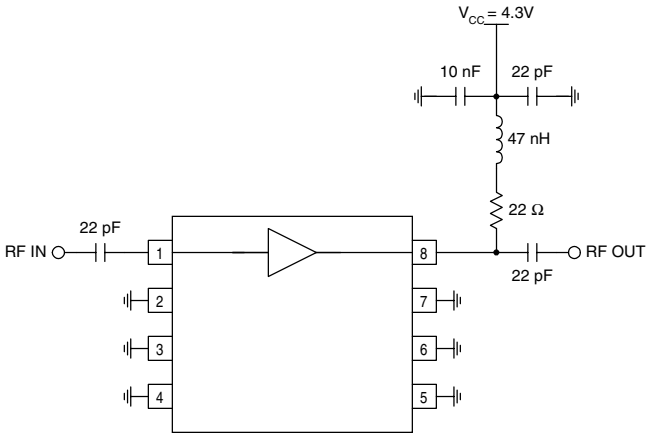
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=4.3V, R_C=22Ω, Freq=1000MHz
Frequency Range		DC to 2000		MHz	
Gain	18	19.5	22	dB	Freq=1000MHz
	19.5	21	23.5	dB	Freq=100MHz
Noise Figure		3.5		dB	
Input VSWR		<2:1			In a 50Ω system
Output VSWR		<2:1			In a 50Ω system
Output IP_3		+20		dBm	
Output P_{1dB}	+10	+12		dBm	
Saturated Output Power		+15		dBm	
Reverse Isolation		>20		dB	
Power Supply					
Operating Voltage		3.7		V	At pin 8
Operating Current	28	35	42	mA	V_{CC}=4.3V, R_C=22Ω
Operating Current Range		20 to 65		mA	

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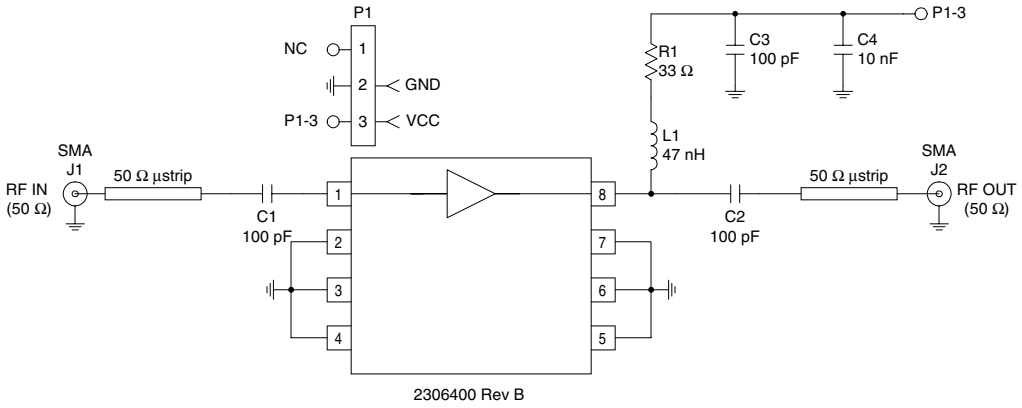
Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. At room temperature, this pin will bias itself to 3.7V as long as the current is held between 20mA and 65mA. Thus the resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - 3.7)}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 65 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.7V is available. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

Application Schematic



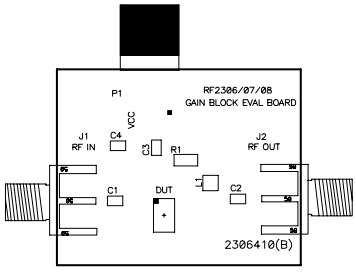
Evaluation Board Schematic

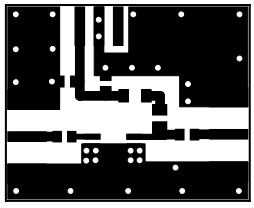
(Download Bill of Materials from www.rfmd.com.)



2306400 Rev B

Evaluation Board Layout
1.27” x 1.02”





RF MICRO·DEVICES

RF2307

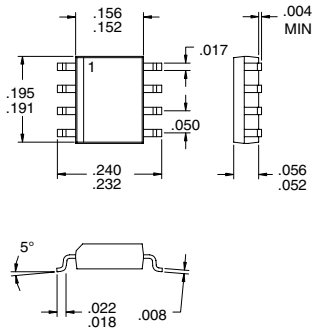
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Portable Battery Powered Equipment
- Broadband Test Equipment

Product Description

The RF2307 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 3000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified.



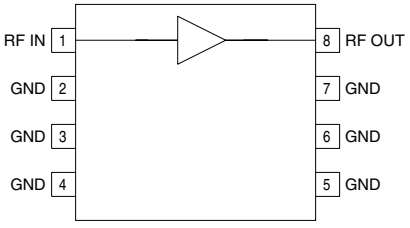
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 3000MHz Operation
- Internally matched Input and Output
- 15dB Small Signal Gain
- 4dB Noise Figure
- 25mW Linear Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2307	General Purpose Amplifier
RF2307 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2307

Absolute Maximum Ratings

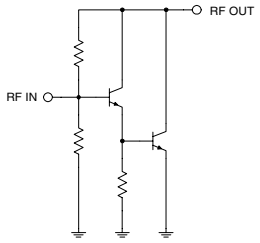
Parameter	Rating	Unit
Supply Current	65	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

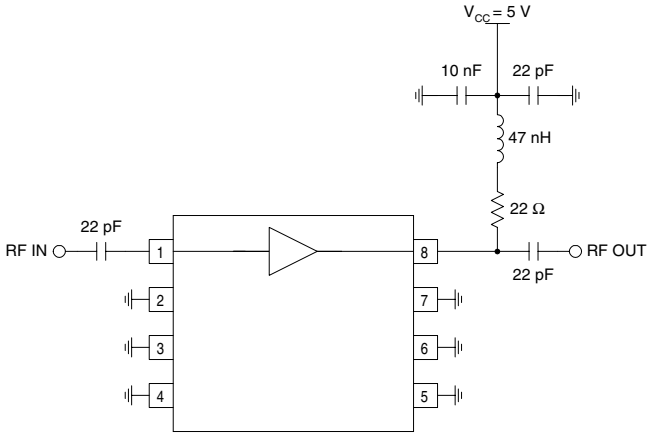
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=5.0 V, R_C=22Ω, Freq=1000 MHz
Frequency Range		DC to 3000		MHz	
Gain	14.2	15.2	16.2	dB	Freq=1000 MHz
	14.7	15.7	16.7	dB	Freq=100 MHz
Noise Figure		4		dB	
Input VSWR		<2:1			
Output VSWR		<2:1			
Output IP_3		+24		dBm	
Output P_{1dB}	+10	+14		dBm	
Saturated Output Power		+15		dBm	
Reverse Isolation		>18		dB	
Power Supply					
Operating Voltage		3.7		V	At pin 8
Operating Current	40	50	60	mA	V_{CC}=5.0 V, R_C=22Ω
Operating Current Range		20 to 65		mA	

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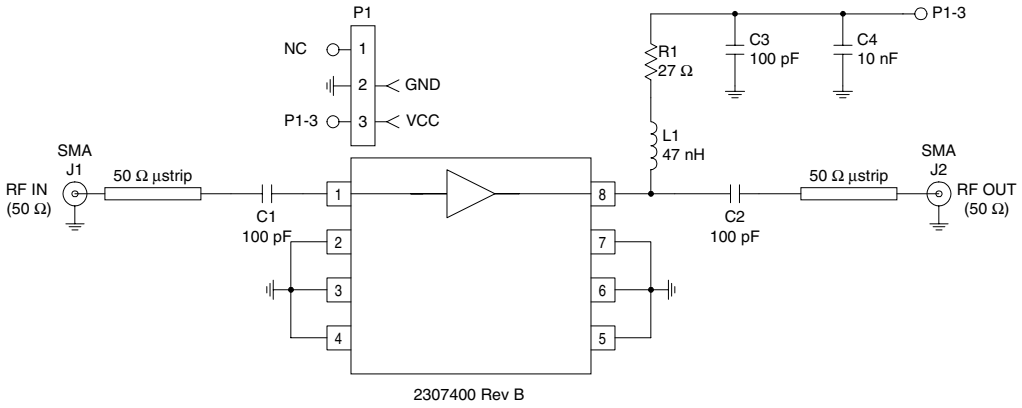
Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is chosen to set the DC current into this pin to a desired level. At room temperature, this pin will bias itself to 3.7V as long as the current is held between 20mA and 65mA. Thus the resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - 3.7)}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 65 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.7V is available. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

Application Schematic

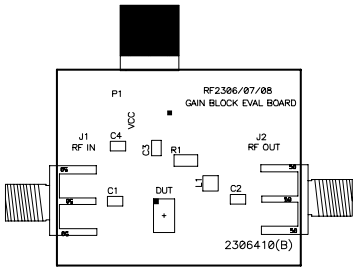


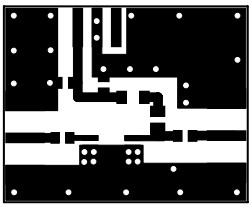
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Uses same board as RF2306
1.27” x 1.02”





RF2308

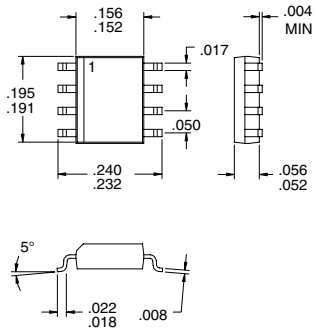
GENERAL PURPOSE AMPLIFIER

Typical Applications

- General Purpose Broadband Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Portable Battery Powered Equipment
- Broadband Test Equipment

Product Description

The RF2308 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 4000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified.



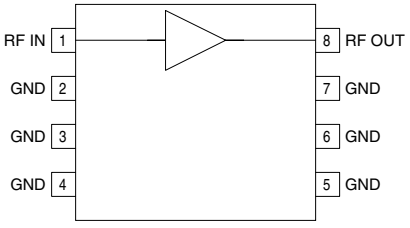
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 4000MHz Operation
- Internally matched Input and Output
- 12dB Small Signal Gain
- 5dB Noise Figure
- 20mW Linear Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2308	General Purpose Amplifier
RF2308 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2308

Absolute Maximum Ratings

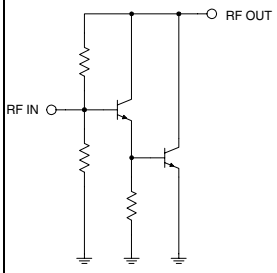
Parameter	Rating	Unit
Supply Current	65	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

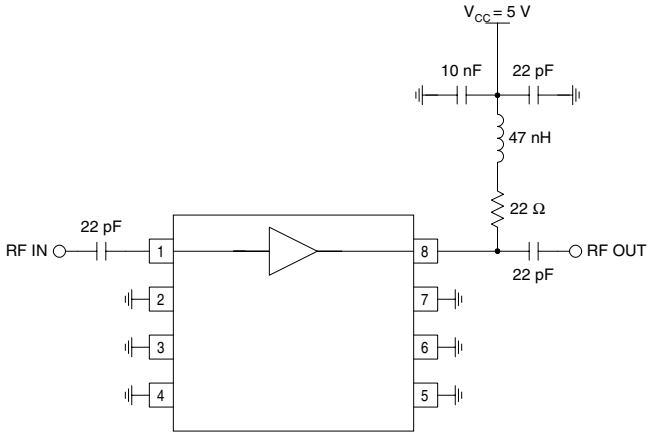
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=4.3V, R_C=22Ω, Freq=1000MHz
Frequency Range		DC to 4000		MHz	
Gain	10	11.7	12.5	dB	Freq=1000MHz
	10.2	11.9	12.7	dB	Freq=100MHz
Noise Figure		5		dB	
Input VSWR		<2:1			
Output VSWR		<2:1			
Output IP_3		+23		dBm	
Output P_{1dB}		+13		dBm	
Saturated Output Power		+15		dBm	
Reverse Isolation		>15		dB	
Power Supply					
Operating Voltage		3.7		V	At pin 8
Operating Current	28	35	42	mA	V_{CC}=4.3V, R_C=22Ω
Operating Current Range		20 to 65		mA	

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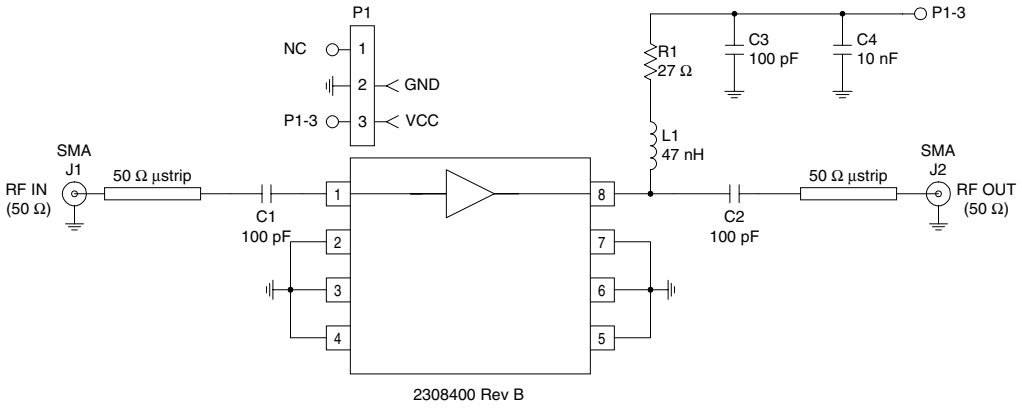
Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is chosen to set the DC current into this pin to a desired level. At room temperature, this pin will bias itself to 3.7V as long as the current is held between 20 and 65mA. Thus the resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - 3.7)}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 65 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.7V is available. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

Application Schematic



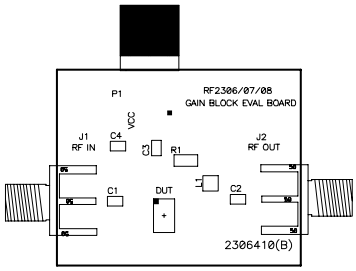
Evaluation Board Schematic

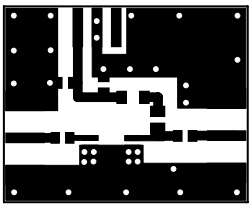
(Download Bill of Materials from www.rfmd.com.)



2308400 Rev B

Evaluation Board Layout
Uses same board as RF2306
1.27” x 1.02”





RF2310

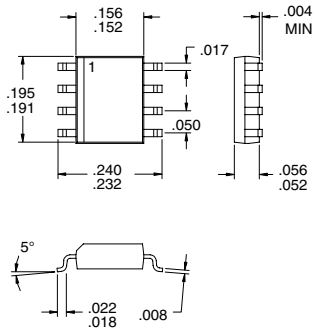
WIDEBAND GENERAL PURPOSE AMPLIFIER

Typical Applications

- General Purpose High Bandwidth Gain Blocks
- IF or RF Buffer Amplifiers
- Broadband Test Equipment
- Final PA for Medium Power Applications
- Driver Stage for Power Amplifiers

Product Description

The RF2310 is a general purpose, low-cost, high linearity RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 2500MHz. The gain flatness over a very wide bandwidth makes the device suitable for many applications. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified.



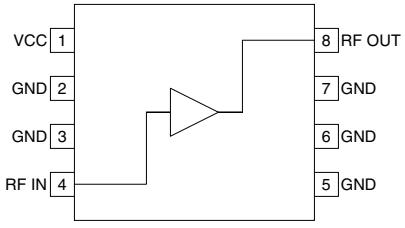
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to well over 2500MHz Operation
- Internally Matched Input and Output
- 15dB Small Signal Gain
- 5dB Noise Figure
- +19dBm Output Power
- Single 3.5V to 6V Positive Power Supply



Functional Block Diagram

Ordering Information

RF2310	Wideband General Purpose Amplifier
RF2310 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2310

Absolute Maximum Ratings

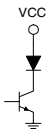
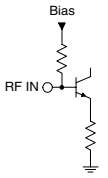
Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature	175	°C
Thermal Resistance, Junction to Case	179	°C/W
Notes; case reference: pins 5-7, conditions: no signal in and both RF ports terminated in 50Ω; average junction temperature measured at 85 °C ambient: 143 °C		

Caution! ESD sensitive device.

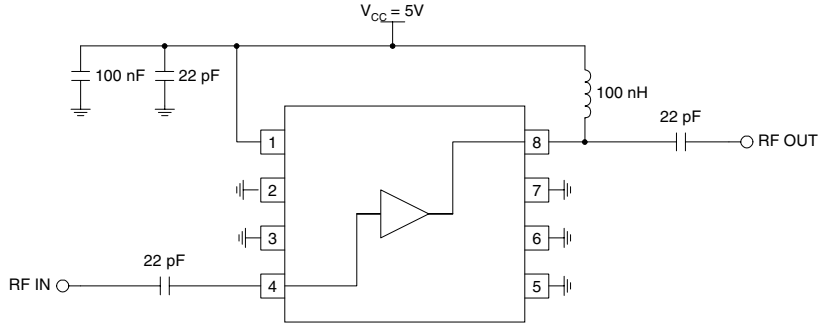
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=5V, Freq=900MHz
Frequency Range		DC to 2500		MHz	0.5dB Bandwidth
Gain	14.0	15.5		dB	
		14.5		dB	V_{CC}=3.6V
Noise Figure		6		dB	V_{CC}=5.0V
		5		dB	V_{CC}=3.6V
Input VSWR		<1.5:1			
Output VSWR		<1.5:1			300MHz to 1200MHz
		<2.5:1			1200MHz to 2500MHz
Output IP_3	+28	+31		dBm	900MHz, V_{CC}=5V
		+19		dBm	900MHz, V_{CC}=3.6V
Output IP_3		+26		dBm	2500MHz, V_{CC}=5V
		+16		dBm	2500MHz, V_{CC}=3.6V
Saturated Output Power	+18	+19		dBm	900MHz, V_{CC}=5V
		+12		dBm	900MHz, V_{CC}=3.6V
Saturated Output Power		+17		dBm	2500MHz, V_{CC}=5V
		+10		dBm	2500MHz, V_{CC}=3.6V
Reverse Isolation		20		dB	
Power Supply					
Operating Voltage		3.5 to 6		V	
Operating Current Range	40	50	65	mA	V_{CC}=5V
		20	25	mA	V_{CC}=3.6V

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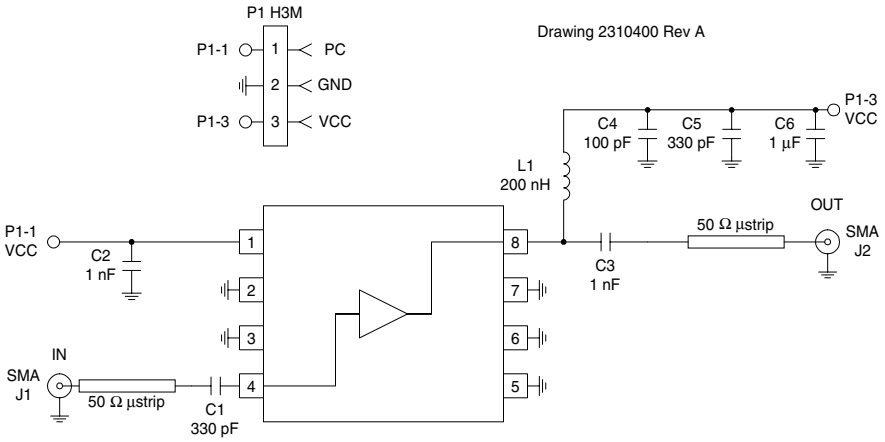
Pin	Function	Description	Interface Schematic
1	VCC	Power supply pin. An external bypass capacitor is recommended. The total supply current is shared between this pin and pin 8 (through the inductor).	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance. To achieve the performance as specified, and to minimize instability, it is recommended to have a local ground plane under the device, as shown in the evaluation board layout.	
3	GND	Same as pin 2.	
4	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output and bias pin. Biasing is accomplished with an external choke inductor to V_{CC} that provides high impedance at the operating frequency. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

Application Schematic



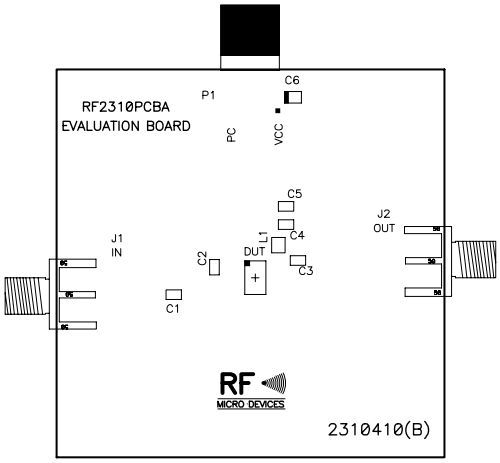
Evaluation Board Schematic

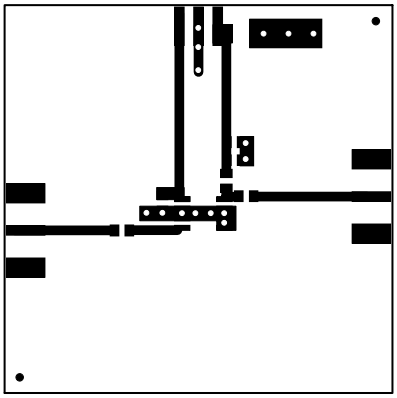
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
2” x 2”





RF2311

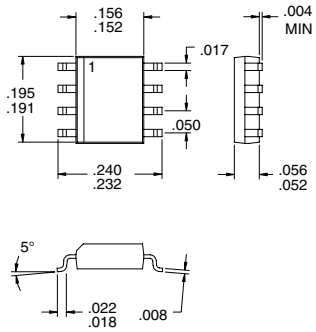
GENERAL PURPOSE AMPLIFIER

Typical Applications

- General Purpose High Bandwidth Gain Blocks
- IF or RF Buffer Amplifiers
- Broadband Test Equipment
- Final PA for Medium Power Applications
- Driver Stage for Power Amplifiers

Product Description

The RF2311 is a general purpose, low cost low power RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 1600MHz. The gain flatness and high bandwidth make the device suitable for many other applications as well. The device is self-contained with 50Ω input and output impedances, and no external DC biasing elements are required to operate as specified.



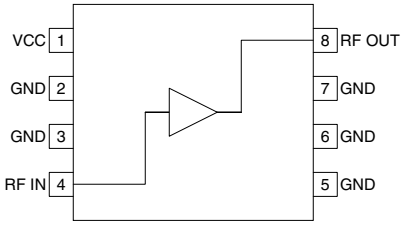
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to well over 1600MHz Operation
- Internally Matched Input and Output
- 14dB Small Signal Gain
- 4.2dB Noise Figure
- +9dBm Output Power
- Single 2.7V to 6V Positive Power Supply



Functional Block Diagram

Ordering Information

RF2311	General Purpose Amplifier
RF2311 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2311

Absolute Maximum Ratings

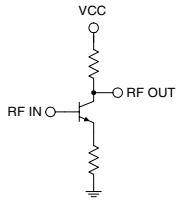
Parameter	Rating	Unit
Supply Voltage	-0.5 to +6	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

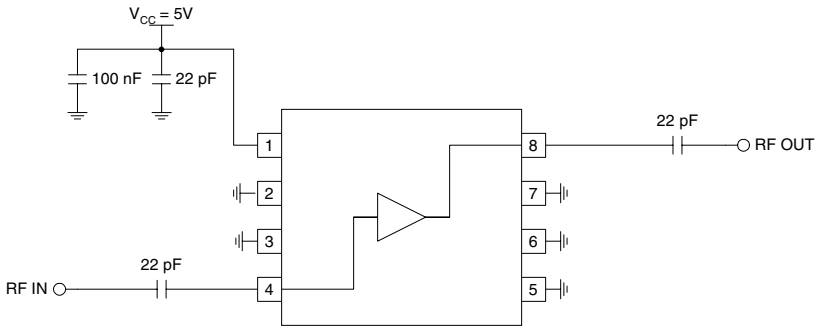
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=5V, Freq=900MHz
Frequency Range		DC to 1600		MHz	3dB Bandwidth
Gain	12	14	16	dB	V_{CC}=5V
		13		dB	V_{CC}=3.6V
Noise Figure		4.2		dB	V_{CC}=5V
		4.0		dB	V_{CC}=3.6V
Input VSWR		<1.5:1			
Output VSWR		<1.3:1			300MHz to 1200MHz
Output IP_3	+14	+16		dBm	900MHz, V_{CC}=5V
		+8		dBm	900MHz, V_{CC}=3.6V
Saturated Output Power	+8	+9		dBm	900MHz, V_{CC}=5V
		+1		dBm	900MHz, V_{CC}=3.6V
Reverse Isolation		20		dB	
Power Supply					
Operating Voltage		2.7 to 6		V	
Operating Current Range	12	17	21	mA	V_{CC}=5V
		8	11	mA	V_{CC}=3.6V

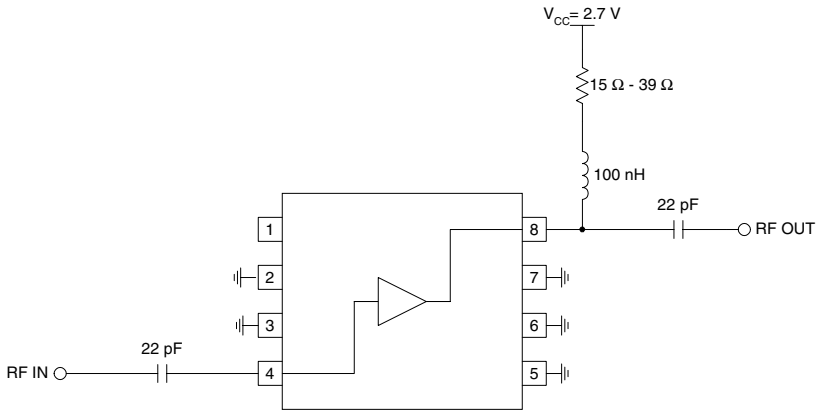
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Pin	Function	Description	Interface Schematic
1	VCC	Power supply pin. An external bypass capacitor is recommended. The total supply current is shared between this pin and pin 8 (through the inductor).	See pin 8.
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	See pin 8.
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	RF OUT	RF output pin. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The DC voltage on this pin is typically 2.4V. Alternatively, power supply may be connected to this pin. A series resistor and inductor should be used, in which case the L should be large enough to present a high impedance at the lowest operating frequency, and the R should be (V_{CC} - 2.4) / I, where I is the desired device current (between 8mA and 20mA).	

Application Schematic 5V Supply Voltage

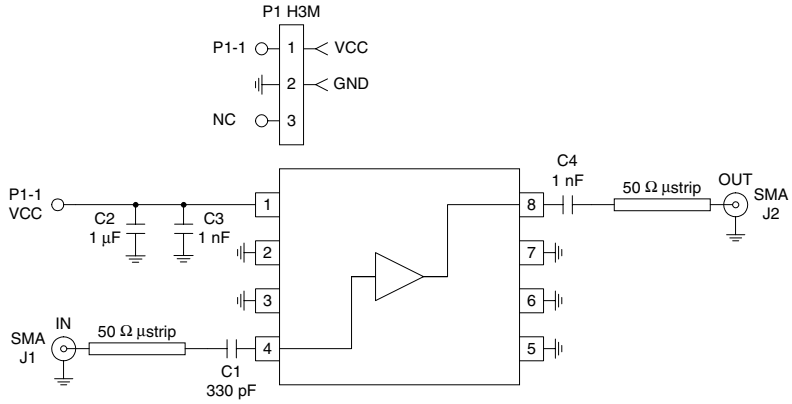


Application Schematic 2.7V Supply Voltage



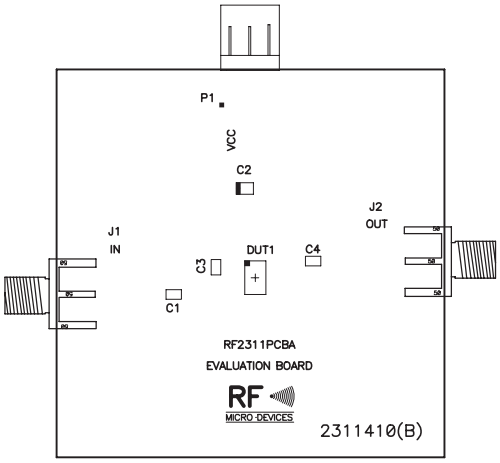
Evaluation Board Schematic

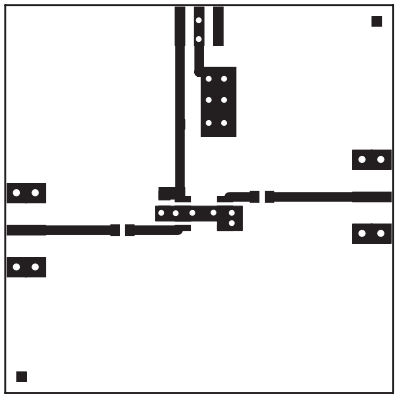
(Download Bill of Materials from www.rfmd.com.)



Drawing 2311400 Rev B

Evaluation Board Layout
2” x 2”





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RF2314

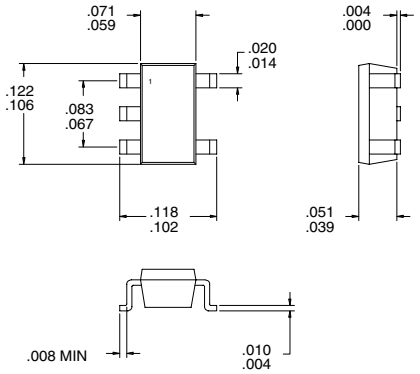
GENERAL PURPOSE LOW NOISE AMPLIFIER

Typical Applications

- Broadband Gain Blocks
- Final PA for Low-Power Applications
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

The RF2314 is a general purpose, low-cost, high performance amplifier designed for operation from a 2.7V to 6V supply with low current consumption. The circuit configuration with resistive feedback allows for broadband cascadable amplification. Feedback with capacitive compensation extends the bandwidth of the amplifier, and is designed for optimized noise figure. The device is unconditionally stable and internally matched to 50Ω. **No external components** are required. The RF2314 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



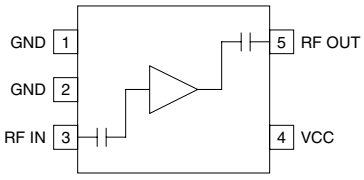
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- 150MHz to 2500MHz Operation
- 2.7V to 6.0V Single Supply
- +18dBm Output IP_3 at 5V
- 14dB Gain at 900MHz
- 8.6dB Gain at 1900MHz
- Low Current Consumption of 5mA at 3V



Functional Block Diagram

Ordering Information

RF2314	General Purpose Low Noise Amplifier
RF2314 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2314

Absolute Maximum Ratings

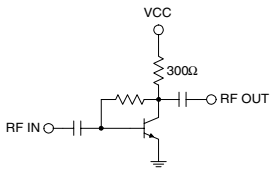
Parameter	Rating	Unit
Supply Voltage	8.0	V
Supply Current	32	mA
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

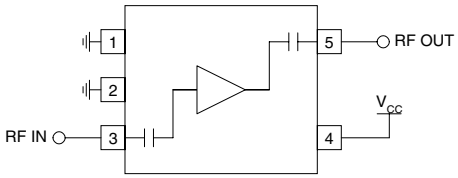
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=3.0V, Freq=900MHz
Frequency Range		150 to >2500		MHz	NOTE: Lower frequencies can be obtained with inductive coupling.
3.0V Performance					T=27°C, V_{CC}=3.0V, Freq=900MHz
Gain		12.9		dB	
		16.6		dB	Freq=150MHz
		7.9		dB	Freq=1900MHz
Noise Figure		1.4		dB	
Output IP3		+9.0		dBm	
Output P_{1dB}		-1.0		dBm	
Input Return Loss		10		dB	
Output Return Loss		17		dB	
Isolation		20		dB	
5.0V Performance					T=27°C, V_{CC}=5.0V, Freq=900MHz
Gain		14.2		dB	
		19.1		dB	Freq=150MHz
		8.6		dB	Freq=1900MHz
Noise Figure		1.5		dB	
Output IP3		+18.0		dBm	
Output P_{1dB}		+8.0		dBm	
Input Return Loss		13		dB	
Output Return Loss		28		dB	
Isolation		20		dB	
Power Supply					
Operating Voltage		2.7 to 6.0		V	
Operating Current		5.7		mA	V_{CC}=3.0V
		12.5		mA	V_{CC}=5.0V

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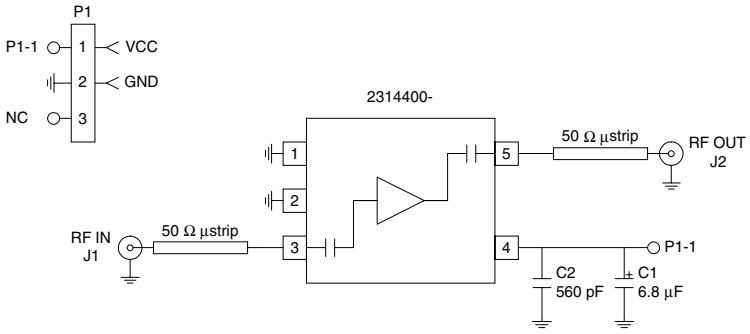
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is internally DC blocked and thus does not require an external blocking capacitor. The input impedance of this pin is internally matched to 50Ω using resistive feedback.	
4	VCC	Supply connection. Generally, there is no need for an external bypass capacitor.	See pin 3 schematic.
5	RF OUT	RF output pin. The output impedance of this pin is internally matched to 50Ω using resistive feedback.	See pin 3 schematic.

Application Schematic

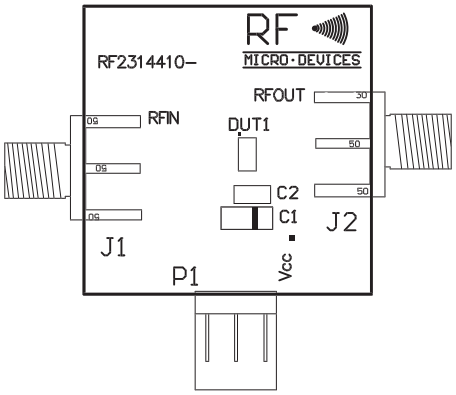


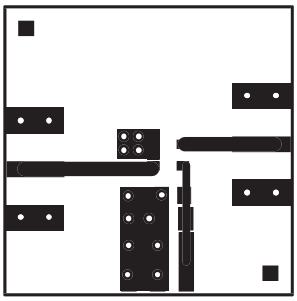
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.0” x 1.0”





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RF2321

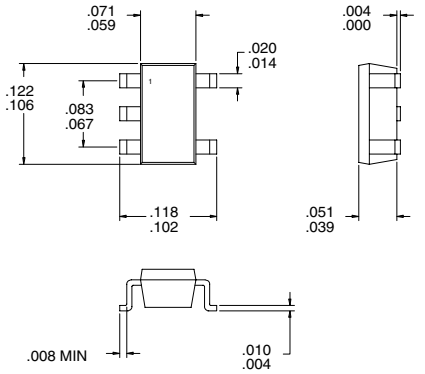
3V GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband Gain Blocks
- Final PA for Low-Power Applications
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

The RF2321 is a general purpose, low-cost silicon amplifier designed for operation from a 3V supply. The circuit configuration with resistive feedback allows for broadband cascadable amplification. Capacitive compensation extends the bandwidth of the amplifier and input stage design optimizes noise figure. The device is unconditionally stable and internally matched to 50Ω. The only external components required for specified performance are bypass and DC blocking capacitors (as shown in application schematic). The RF2321 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



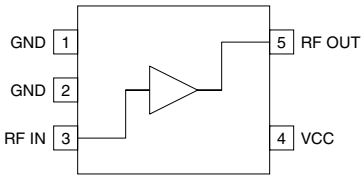
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to >2000MHz Operation
- 2.7V to 3.3V Single Supply
- +3dBm Output IP3
- 12dB Gain at 900MHz
- 12dB Gain at 1900MHz
- High Isolation (37dB at 900MHz)



Functional Block Diagram

Ordering Information

RF2321	3V General Purpose Amplifier
RF2321 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

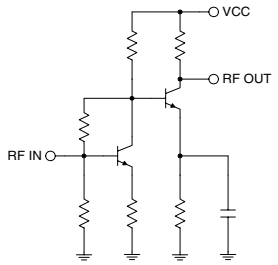
Parameter	Rating	Unit
Supply Voltage	4.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

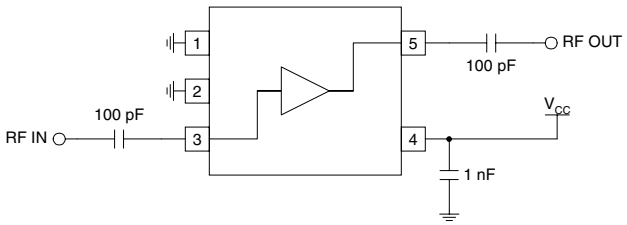
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=3.0V
Frequency Range		DC to >2000		MHz	
100MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		3.6		dB	
Output IP3		4		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		15		dB	
Output Return Loss		11		dB	
Isolation		52		dB	
500MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		3.8		dB	
Output IP3		4		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		15		dB	
Output Return Loss		11		dB	
Isolation		42		dB	
900MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		3.7		dB	
Output IP3		3		dBm	
Output P_{1dB}		-7		dBm	
Input Return Loss		13		dB	
Output Return Loss		9		dB	
Isolation		36		dB	
1000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		3.7		dB	
Output IP3		3		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		13		dB	
Output Return Loss		9		dB	
Isolation		35		dB	
2000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		4.5		dB	
Output IP3		2		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		8		dB	
Output Return Loss		9		dB	
Isolation		25		dB	
Power Supply					
Operating Voltage		3.0±10%		V	
Operating Current		7.7		mA	V_{CC}=3.0V

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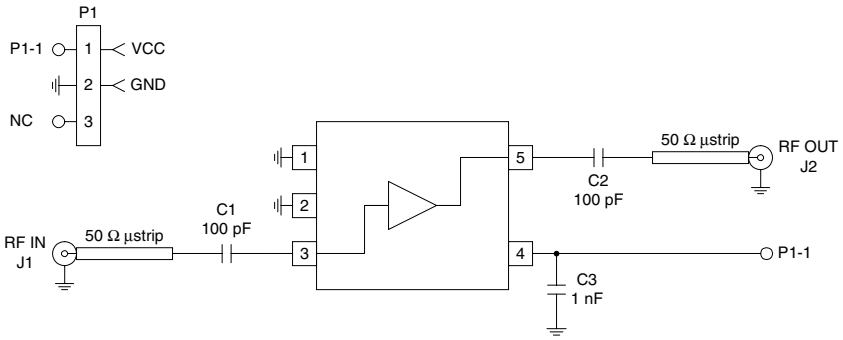
Pin	Function	Description	Interface Schematic
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4	VCC	Supply connection. This pin should be bypassed with a suitable capacitor(s).	
5	RF OUT	RF output and bias pin. The output impedance of this pin is internally matched to 50Ω using resistive feedback. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic).	See pin 3 schematic.

Application Schematic



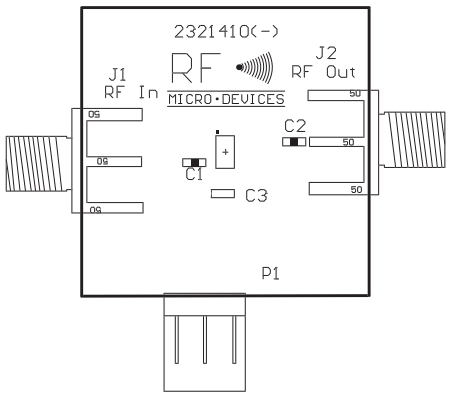
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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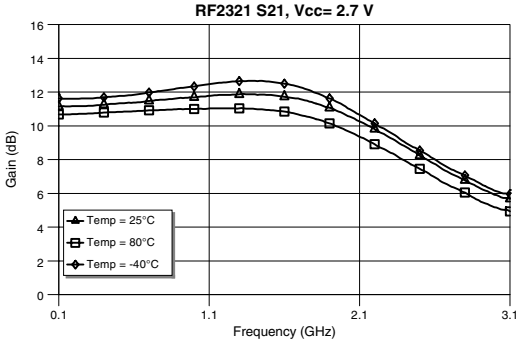
Evaluation Board Layout
1” x 1”



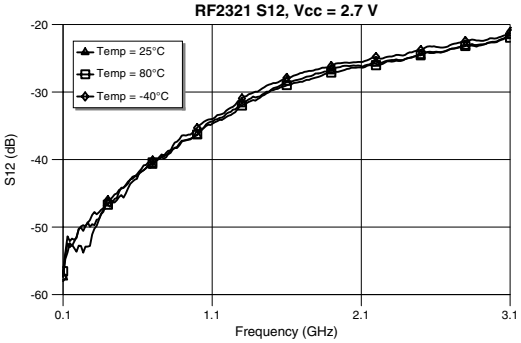


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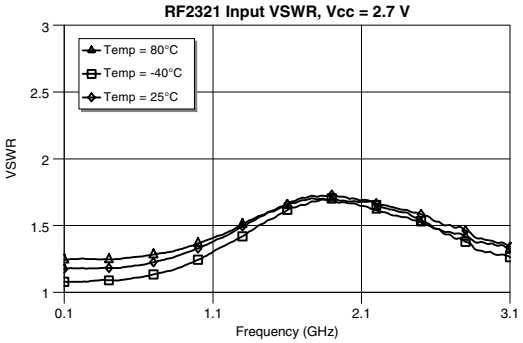
RF2321 S21, Vcc= 2.7 V



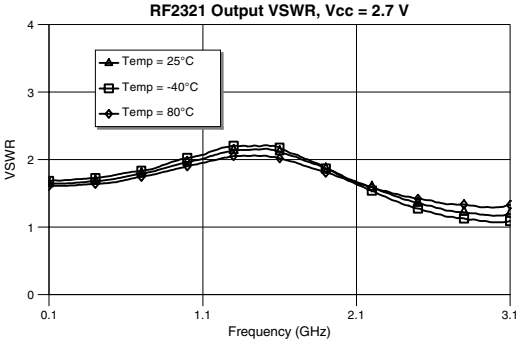
RF2321 S12, Vcc = 2.7 V



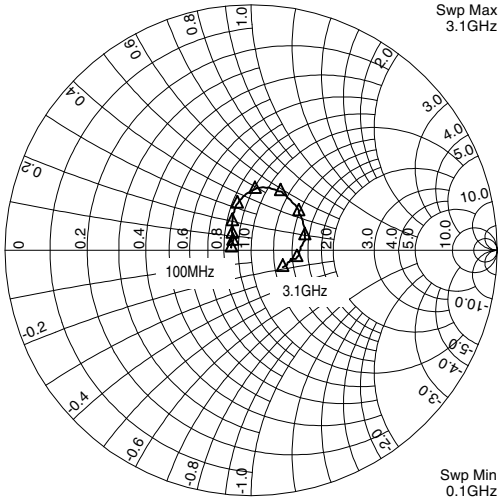
RF2321 Input VSWR, Vcc = 2.7 V



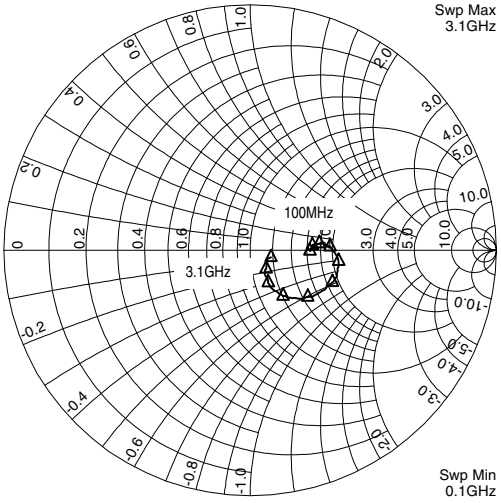
RF2321 Output VSWR, Vcc = 2.7 V



RF2321 S11, Vcc = 2.7 V, Temp = 25°C

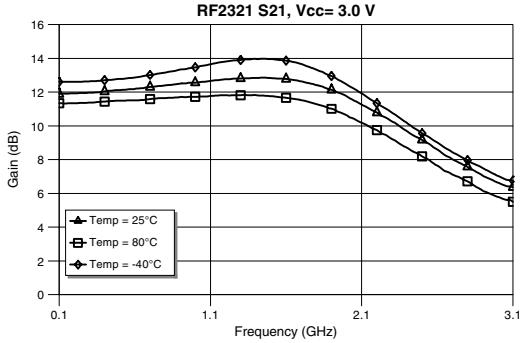


RF2321 S22, Vcc = 2.7 V, Temp= 25°C

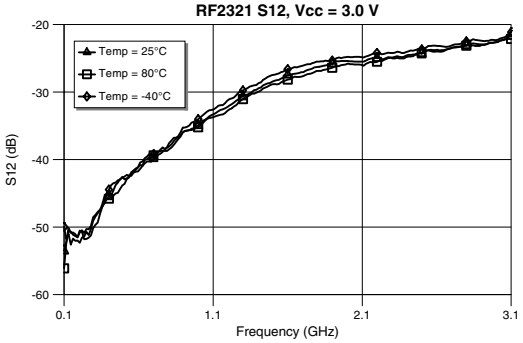


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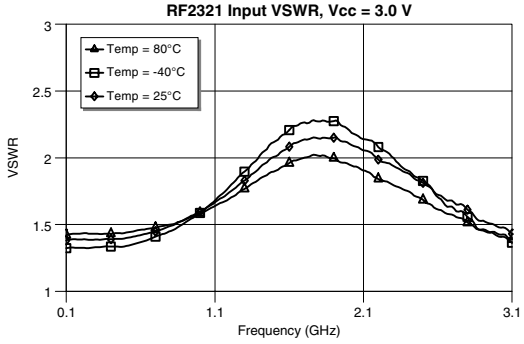
RF2321 S21, Vcc= 3.0 V



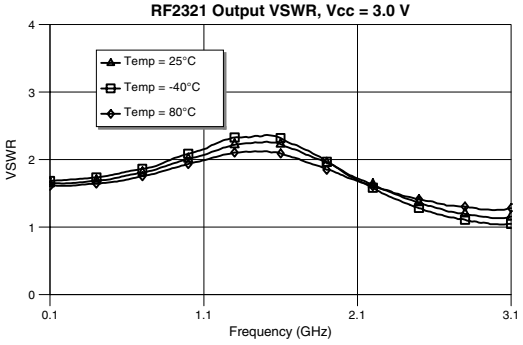
RF2321 S12, Vcc = 3.0 V



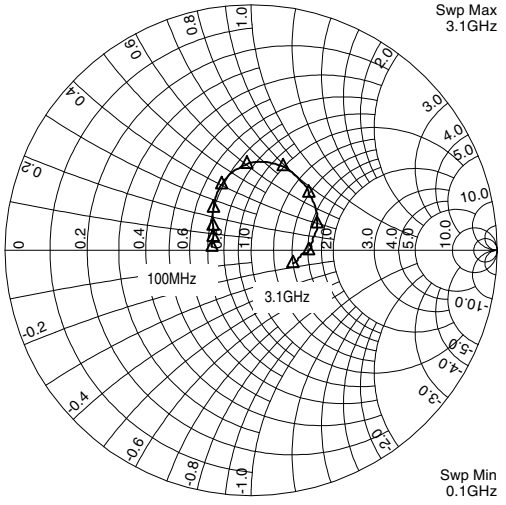
RF2321 Input VSWR, Vcc = 3.0 V



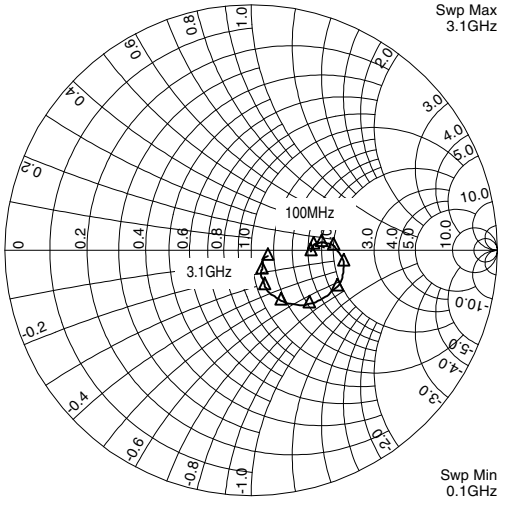
RF2321 Output VSWR, Vcc = 3.0 V



RF2321 S11, Vcc = 3.0 V, Temp = 25°C

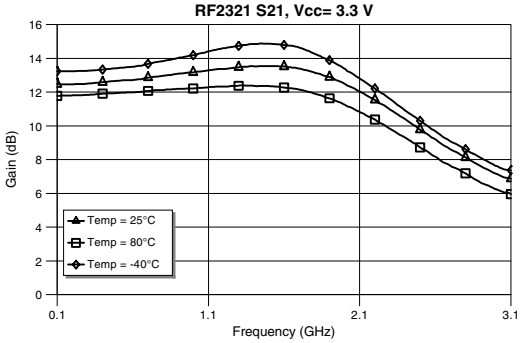


RF2321 S22, Vcc = 3.0 V, Temp= 25°C

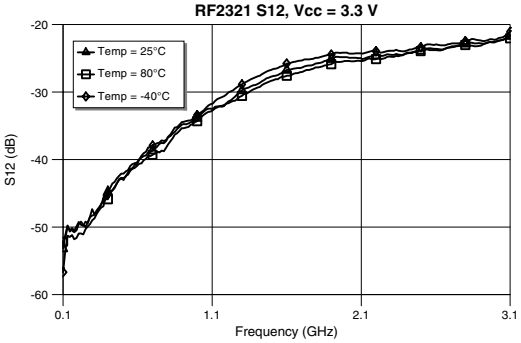


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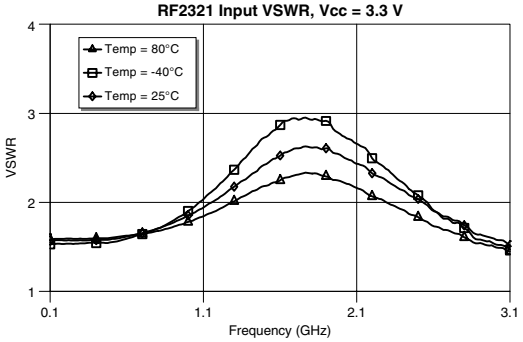
RF2321 S21, Vcc= 3.3 V



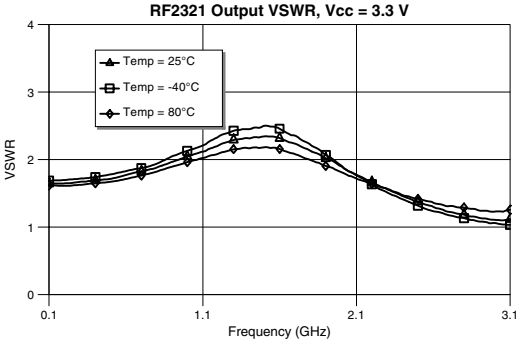
RF2321 S12, Vcc = 3.3 V



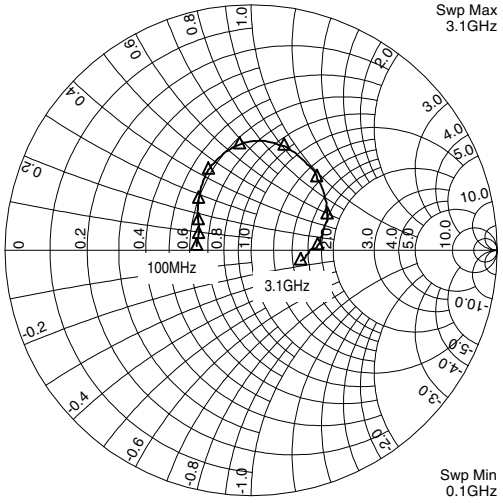
RF2321 Input VSWR, Vcc = 3.3 V



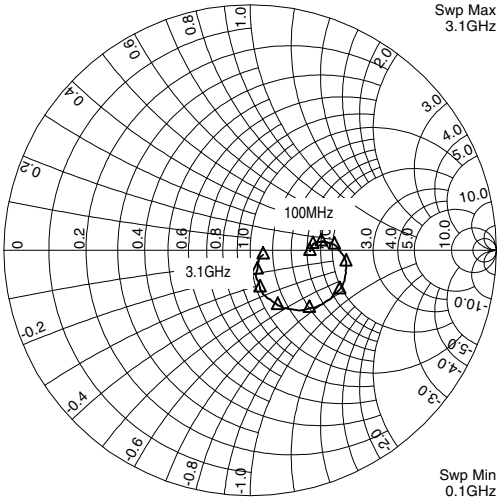
RF2321 Output VSWR, Vcc = 3.3 V



RF2321 S11, Vcc = 3.3 V, Temp = 25°C



RF2321 S22, Vcc = 3.3 V, Temp= 25°C



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RF MICRO·DEVICES

Preliminary

RF2322

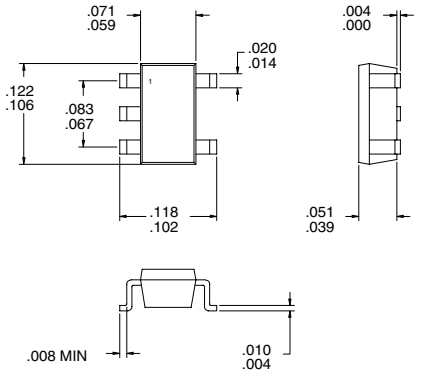
3V GENERAL PURPOSE AMPLIFIER

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- Final PA for Low-Power Applications
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

The RF2322 is a general purpose, low-cost silicon amplifier designed for operation from a 3V supply. The circuit configuration with resistive feedback allows for broadband cascadable amplification. Capacitive compensation extends the bandwidth of the amplifier and input stage design optimizes noise figure. The device is unconditionally stable and internally matched to 50Ω. The only external components required for specified performance are bypass and DC blocking capacitors (as shown in application schematic). The RF2322 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



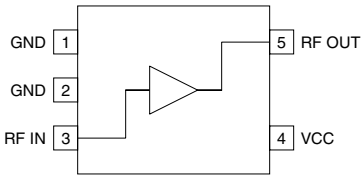
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to >2000MHz Operation
- 2.7V to 3.3V Single Supply
- +3dBm Output IP3
- 19dB Gain at 900MHz
- 12dB Gain at 1900MHz
- High Isolation (38dB at 900MHz)



Functional Block Diagram

Ordering Information

RF2322	3V General Purpose Amplifier
RF2322 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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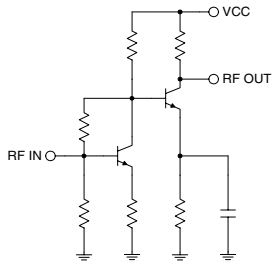
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

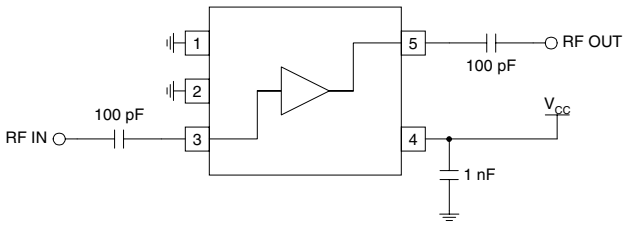
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=3.0V
Frequency Range		DC to >2000		MHz	
100MHz Performance					T=27°C, V_{CC}=3.0V
Gain		20		dB	
Noise Figure		3.2		dB	
Output IP3		4		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		19		dB	
Output Return Loss		11		dB	
Isolation		55		dB	
500MHz Performance					T=27°C, V_{CC}=3.0V
Gain		20		dB	
Noise Figure		3.4		dB	
Output IP3		4		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		18		dB	
Output Return Loss		9		dB	
Isolation		45		dB	
900MHz Performance					T=27°C, V_{CC}=3.0V
Gain		19		dB	
Noise Figure		3.3		dB	
Output IP3		3		dBm	
Output P_{1dB}		-7		dBm	
Input Return Loss		13		dB	
Output Return Loss		8		dB	
Isolation		38		dB	
1000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		19		dB	
Noise Figure		3.2		dB	
Output IP3		3		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		12		dB	
Output Return Loss		8		dB	
Isolation		35		dB	
2000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		4.0		dB	
Output IP3		2		dBm	
Output P_{1dB}		-8		dBm	
Input Return Loss		11		dB	
Output Return Loss		15		dB	
Isolation		26		dB	
Power Supply					
Operating Voltage		3.0±10%		V	
Operating Current		7.5		mA	V_{CC}=3.0V

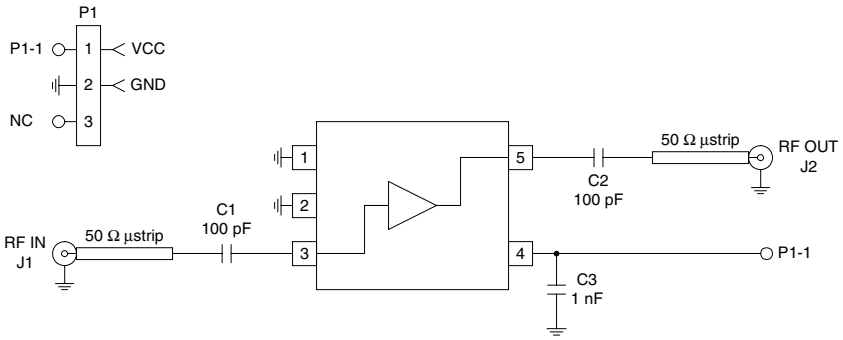
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4	VCC	Supply connection. This pin should be bypassed with a suitable capacitor(s).	
5	RF OUT	RF output and bias pin. The output impedance of this pin is internally matched to 50Ω using resistive feedback. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic).	See pin 3 schematic.

Application Schematic



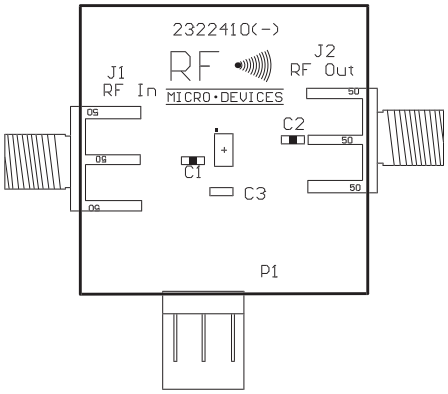
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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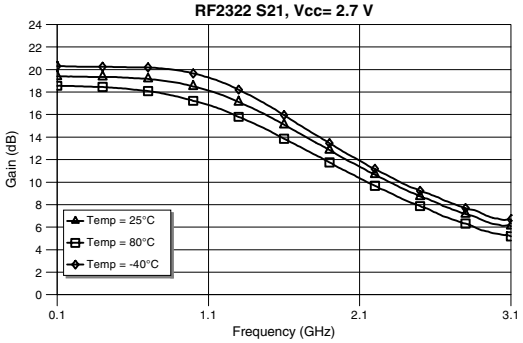
Evaluation Board Layout
1” x 1”



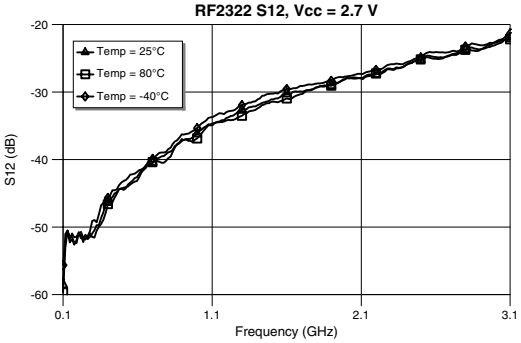


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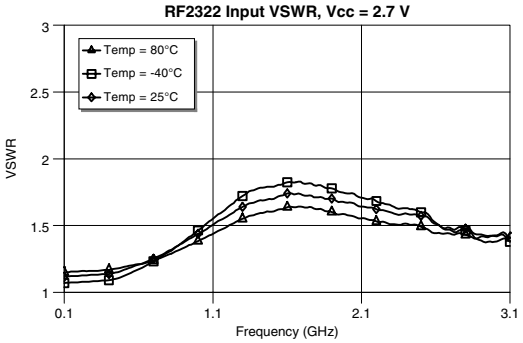
RF2322 S21, Vcc= 2.7 V



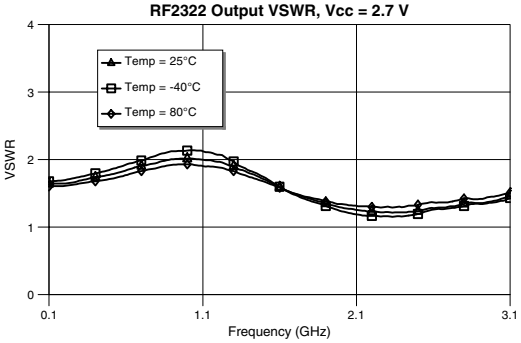
RF2322 S12, Vcc = 2.7 V



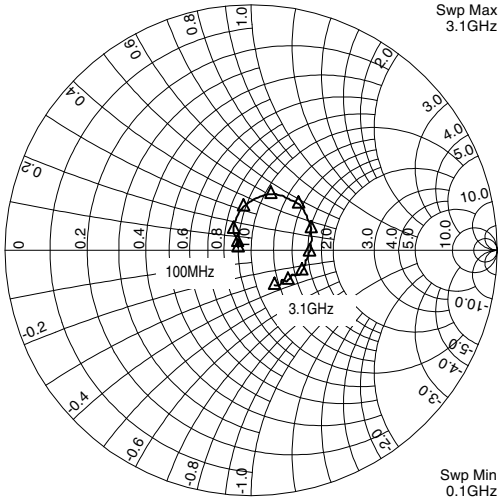
RF2322 Input VSWR, Vcc = 2.7 V



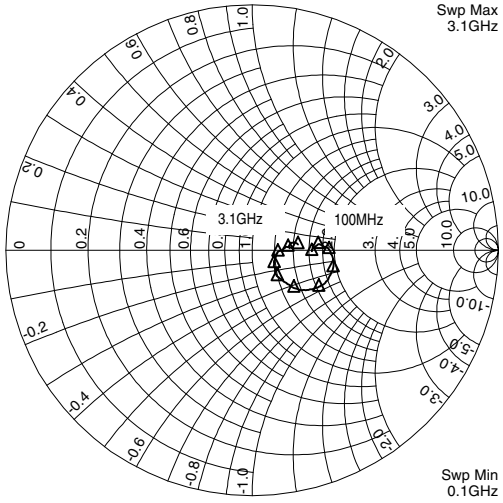
RF2322 Output VSWR, Vcc = 2.7 V



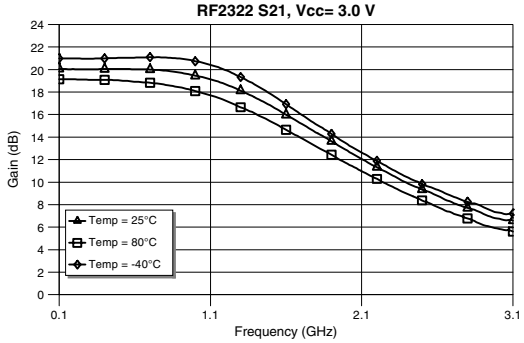
RF2322 S11, Vcc = 2.7 V, Temp = 25°C



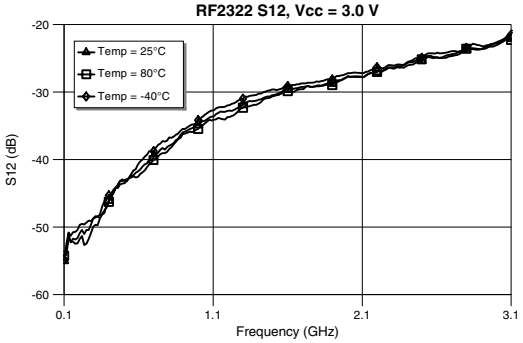
RF2322 S22, Vcc = 2.7 V, Temp= 25°C



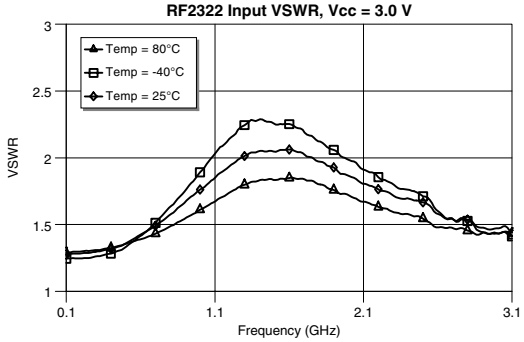
RF2322 S21, Vcc= 3.0 V



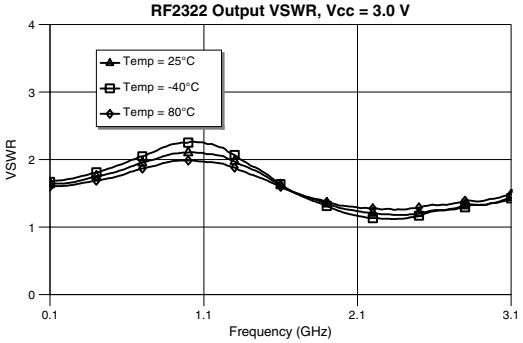
RF2322 S12, Vcc = 3.0 V



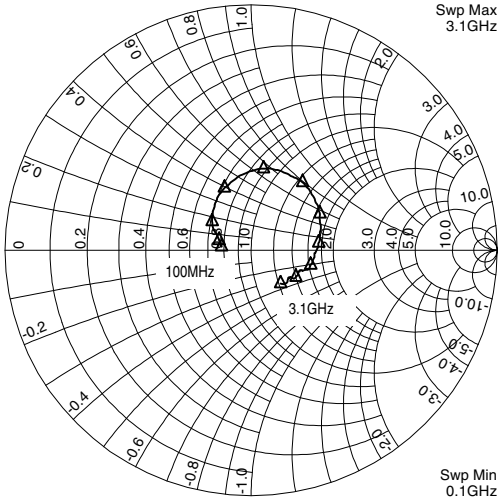
RF2322 Input VSWR, Vcc = 3.0 V



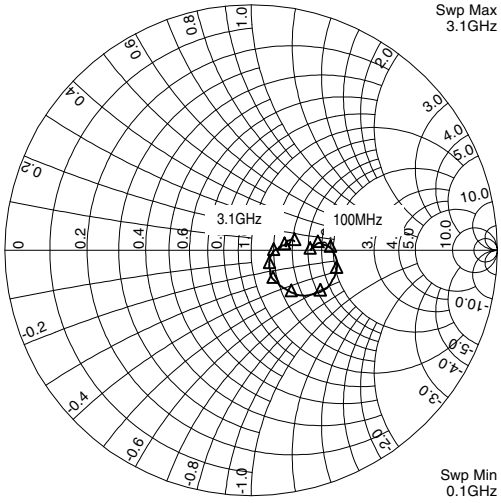
RF2322 Output VSWR, Vcc = 3.0 V



RF2322 S11, Vcc = 3.0 V, Temp = 25°C

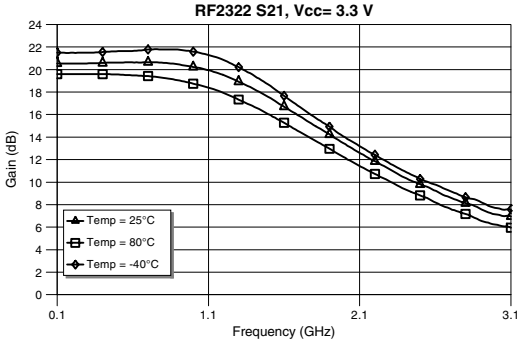


RF2322 S22, Vcc = 3.0 V, Temp= 25°C

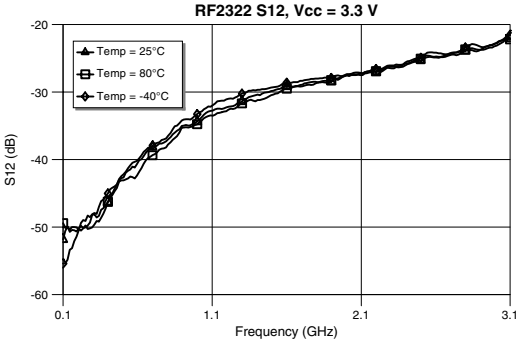


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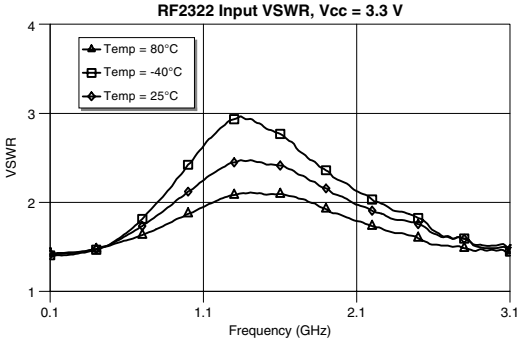
RF2322 S21, Vcc= 3.3 V



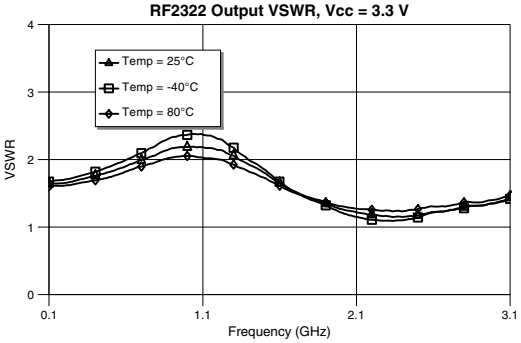
RF2322 S12, Vcc = 3.3 V



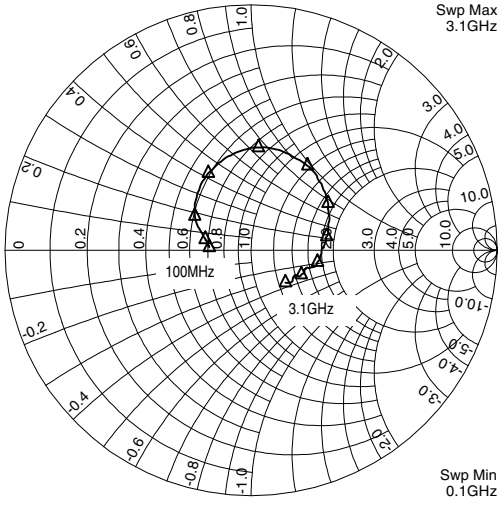
RF2322 Input VSWR, Vcc = 3.3 V



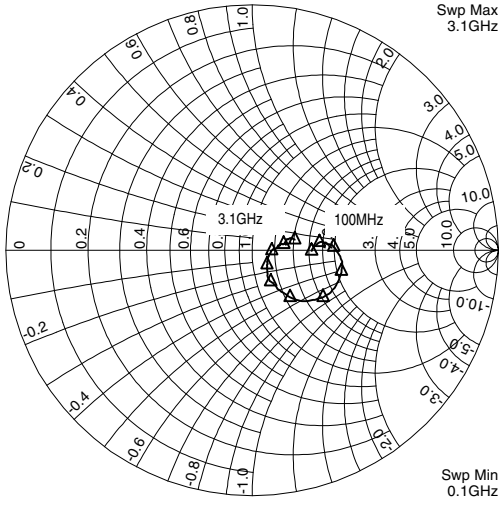
RF2322 Output VSWR, Vcc = 3.3 V



RF2322 S11, Vcc = 3.3 V, Temp = 25°C



RF2322 S22, Vcc = 3.3 V, Temp= 25°C



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RF MICRO·DEVICES

Preliminary

RF2323

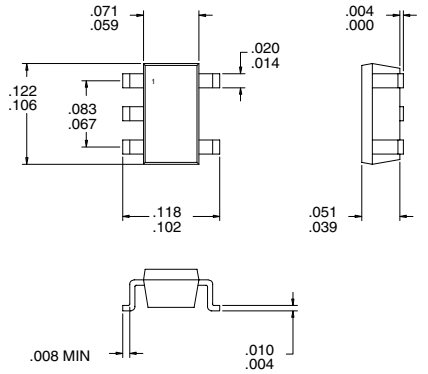
3V GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband Gain Blocks
- Low Noise Amplifiers
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers
- Receiver Front-Ends

Product Description

The RF2323 is a general purpose, low-cost silicon amplifier designed for operation from a 3V supply. The circuit configuration with resistive feedback allows for broadband cascadable amplification. Capacitive compensation extends the bandwidth of the amplifier and input stage design optimizes noise figure. The device is unconditionally stable and internally matched to 50Ω. The only external components required for specified performance are bypass and DC blocking capacitors (as shown in application schematic). The RF2323 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



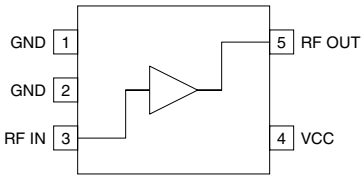
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to >2000MHz Operation
- 2.7V to 3.3V Single Supply
- 2.3dB Noise Figure
- 21dB Gain at 900MHz
- 12dB Gain at 1900MHz
- High Isolation (33dB at 900MHz)



Functional Block Diagram

Ordering Information

RF2323	3V General Purpose Amplifier
RF2323 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

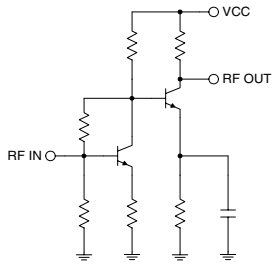
Parameter	Rating	Unit
Supply Voltage	4.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

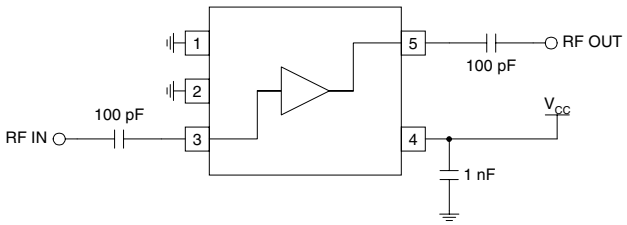
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=3.0V
Frequency Range		DC to >2000		MHz	
100MHz Performance					T=27°C, V_{CC}=3.0V
Gain		20		dB	
Noise Figure		2.0		dB	
Output IP3		5		dBm	
Output P_{1dB}		-6		dBm	
Input Return Loss		19		dB	
Output Return Loss		12		dB	
Isolation		50		dB	
500MHz Performance					T=27°C, V_{CC}=3.0V
Gain		19		dB	
Noise Figure		2.3		dB	
Output IP3		4		dBm	
Output P_{1dB}		-6		dBm	
Input Return Loss		9		dB	
Output Return Loss		11		dB	
Isolation		41		dB	
900MHz Performance					T=27°C, V_{CC}=3.0V
Gain	19.0	21	21.5	dB	
Noise Figure		2.3		dB	
Output IP3		2		dBm	
Output P_{1dB}		-7		dBm	
Input Return Loss		6		dB	
Output Return Loss		8		dB	
Isolation		33		dB	
1000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		20		dB	
Noise Figure		2.3		dB	
Output IP3		2		dBm	
Output P_{1dB}		-7		dBm	
Input Return Loss		6		dB	
Output Return Loss		8		dB	
Isolation		32		dB	
2000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		4.0		dB	
Output IP3		3		dBm	
Output P_{1dB}		-7		dBm	
Input Return Loss		14		dB	
Output Return Loss		20		dB	
Isolation		27		dB	
Power Supply					
Operating Voltage		3.0±10%		V	
Operating Current		6.8		mA	V_{CC}=3.0V

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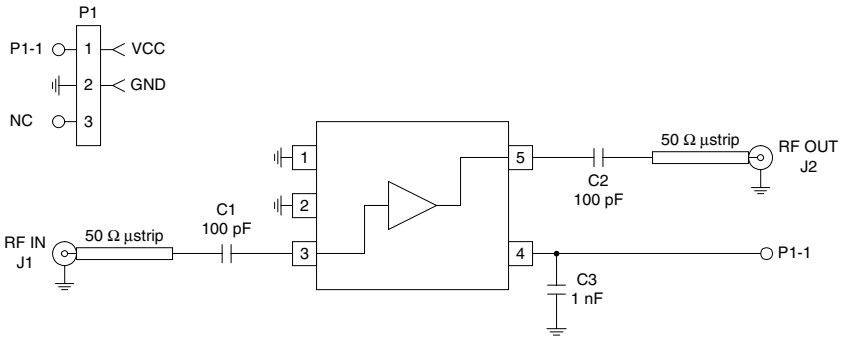
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is not internally DC blocked and thus requires an external blocking capacitor suitable for the frequency of operation. The input impedance of this pin is internally matched to 50Ω using resistive feedback.	
4	VCC	Supply connection. This pin should be bypassed with a suitable capacitor(s).	
5	RF OUT	RF output and bias pin. The output impedance of this pin is internally matched to 50Ω using resistive feedback. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic).	See pin 3 schematic.

Application Schematic



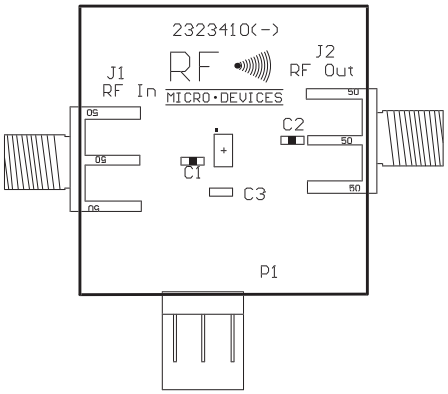
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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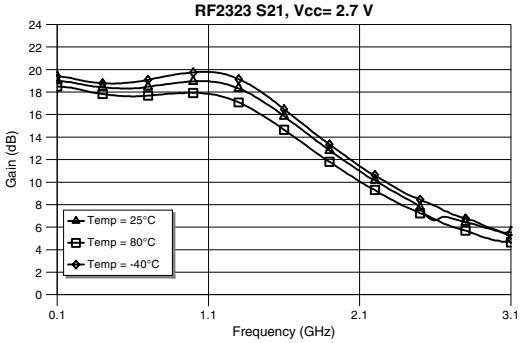
Evaluation Board Layout
1” x 1”



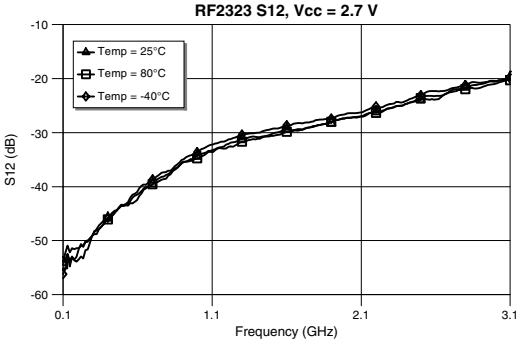


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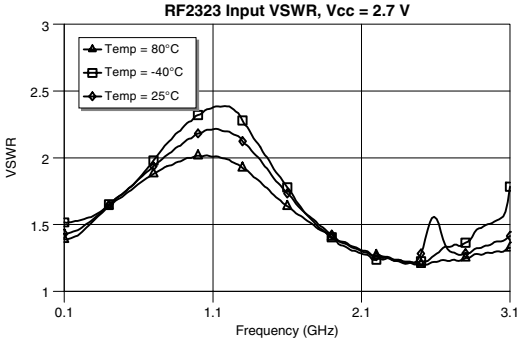
RF2323 S21, Vcc= 2.7 V



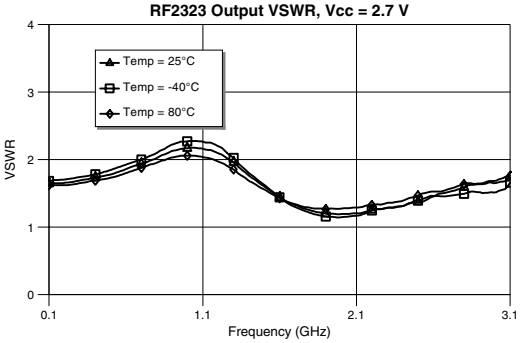
RF2323 S12, Vcc = 2.7 V



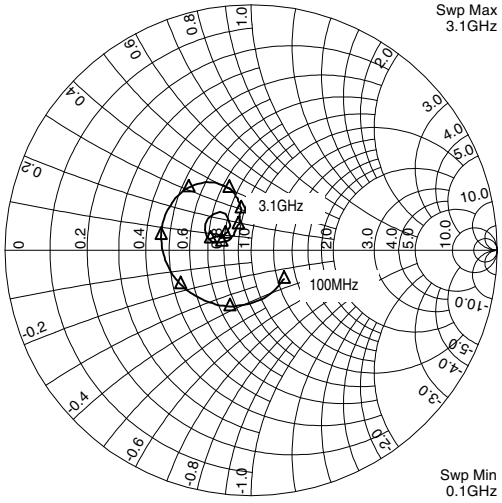
RF2323 Input VSWR, Vcc = 2.7 V



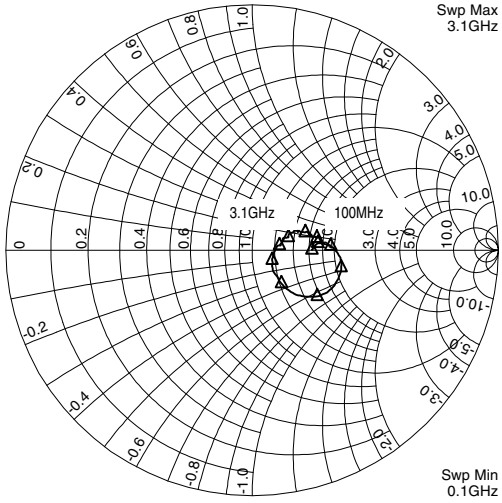
RF2323 Output VSWR, Vcc = 2.7 V



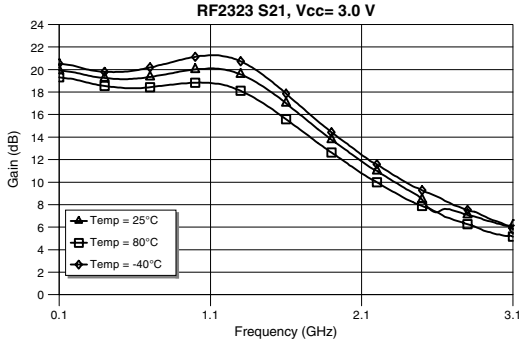
RF2323 S11, Vcc = 2.7 V, Temp = 25°C



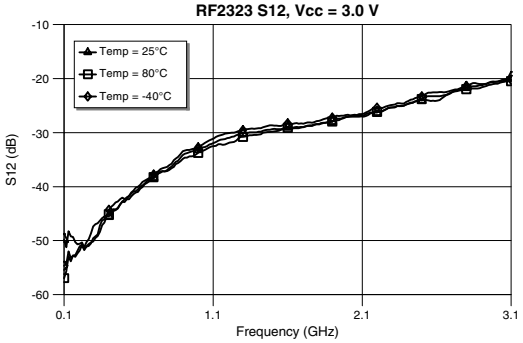
RF2323 S22, Vcc = 2.7 V, Temp= 25°C



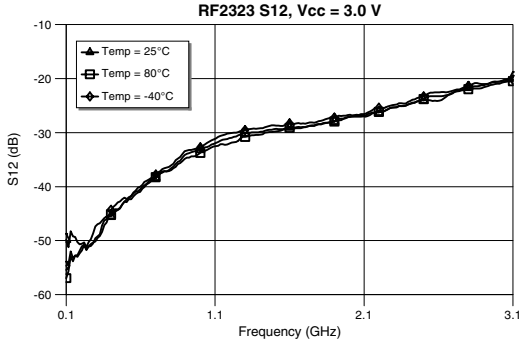
RF2323 S21, Vcc= 3.0 V



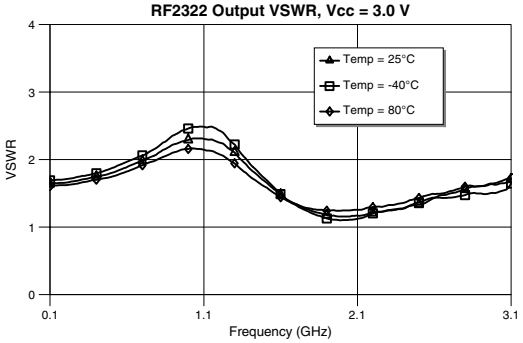
RF2323 S12, Vcc = 3.0 V



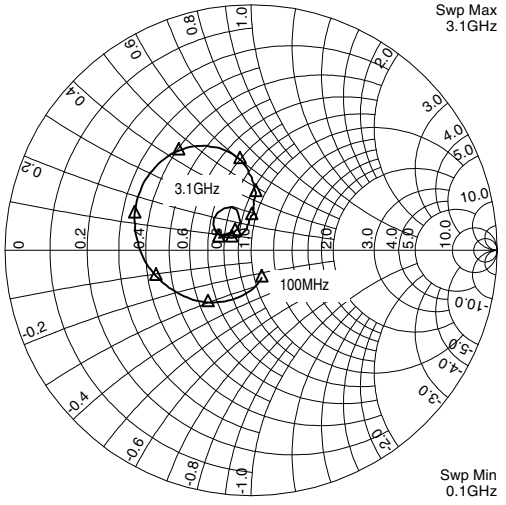
RF2323 S12, Vcc = 3.0 V



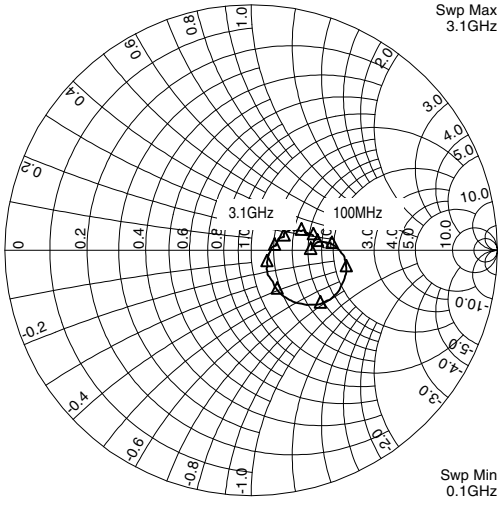
RF2322 Output VSWR, Vcc = 3.0 V



RF2323 S11, Vcc = 3.0 V, Temp = 25°C

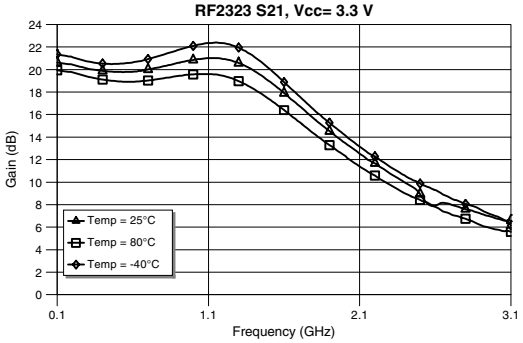


RF2323 S22, Vcc = 3.0 V, Temp= 25°C

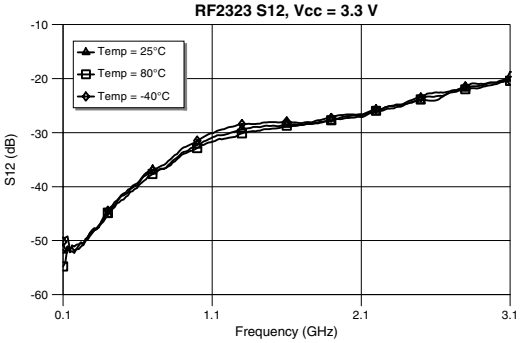


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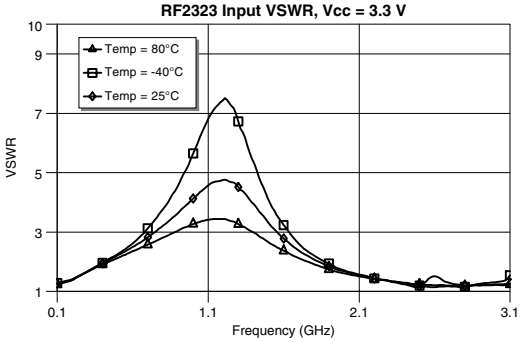
RF2323 S21, Vcc= 3.3 V



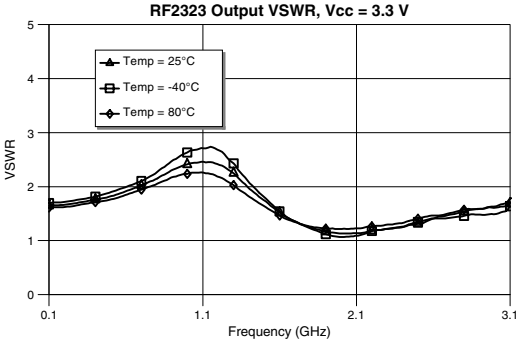
RF2323 S12, Vcc = 3.3 V



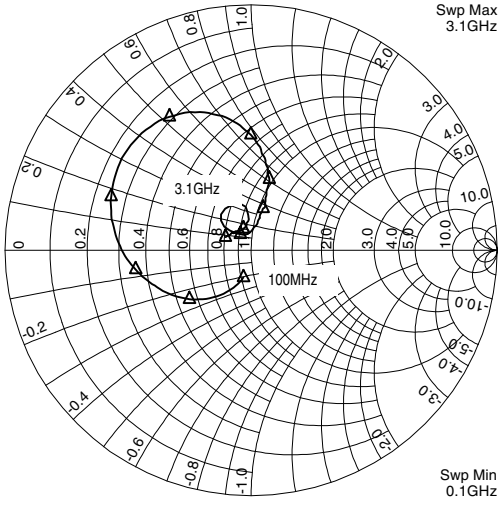
RF2323 Input VSWR, Vcc = 3.3 V



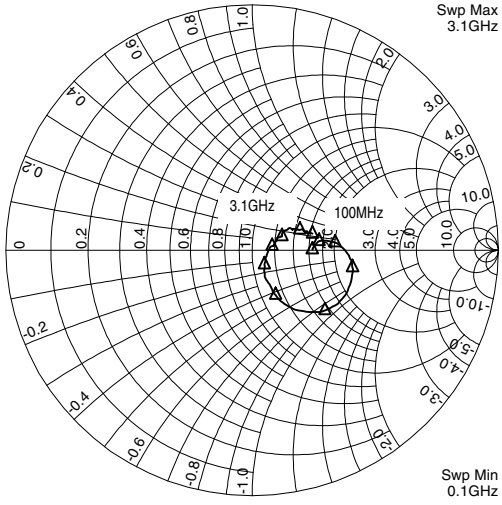
RF2323 Output VSWR, Vcc = 3.3 V



RF2323 S11, Vcc = 3.3 V, Temp = 25°C



RF2323 S22, Vcc = 3.3 V, Temp= 25°C



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RF2324

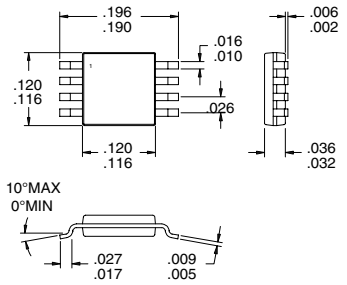
PCS CDMA/TDMA 3V PA DRIVER AMPLIFIER

Typical Applications

- TDMA/CDMA/FM PCS Tx Amplifier
- Low Noise Transmit Driver Amplifier
- 2.4GHz WLAN Systems
- ISM Band LNA/Driver
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

The RF2324 is a low noise CDMA/TDMA PA driver amplifier with a very high dynamic range designed for transmit digital PCS applications at 1880MHz. The device functions as an outstanding PA driver amplifier in the transmit chain of digital subscriber units where low transmit noise power is a concern. The IC includes a power down feature that can be used to completely turn off the device. The IC is featured in a standard miniature 8-lead plastic MSOP package.



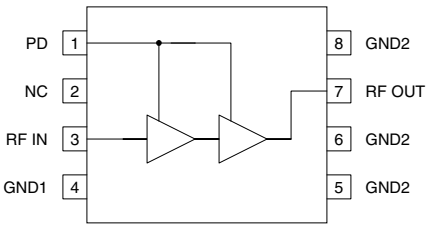
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8

Features

- Low Noise and High Intercept Point
- Power Down Control
- Single 2.5V to 6.0V Power Supply
- 150MHz to 2500MHz Operation
- Extremely Small MSOP-8 Package



Functional Block Diagram

Ordering Information

RF2324	PCS CDMA/TDMA 3V PA Driver Amplifier
RF2324 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

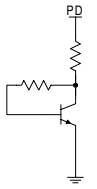
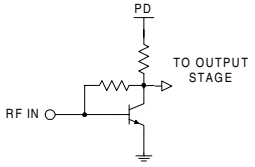
Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

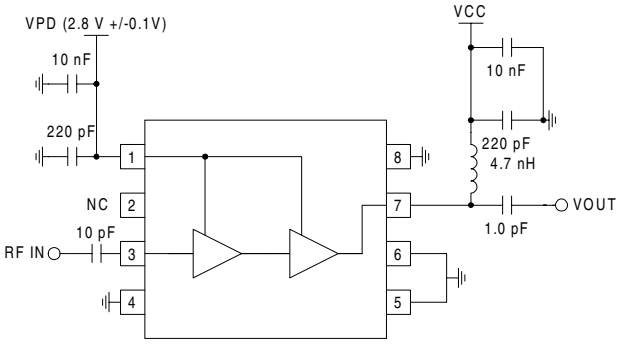
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		150 to 2500		MHz	
1880MHz Performance					Schematic per Evaluation Board, T=25°C, RF=1880MHz, V_{PD}=2.8V
Gain	21	22	23	dB	V_{CC}=3.5V
	21	22	23	dB	V_{CC}=3.0V
	21	22	23	dB	V_{CC}=2.5V
Output IP3	+26	+28	+35	dBm	V_{CC}=3.5V
		+26		dBm	V_{CC}=3.0V
		+25		dBm	V_{CC}=2.5V
Noise Figure		1.8	2.5	dB	V_{CC}=3.5V
		1.8	2.5	dB	V_{CC}=3.0V
		1.8	2.5	dB	V_{CC}=2.5V
Reverse Isolation		36		dB	V_{CC}=3.5V
		36		dB	V_{CC}=3.0V
		35		dB	V_{CC}=2.5V
Input VSWR		1.3:1	2.0:1		
Output VSWR		1.25:1	2.0:1		Using External LC network used on Evaluation Board
P_{1dB}	14	16		dBm	V_{CC}=3.5V
	12.5	14.5		dBm	V_{CC}=3.0V
	11	13		dBm	V_{CC}=2.5V
Power Supply					T=25°C
Voltage (V_{CC})		2.5 to 6.0		V	
Voltage (V_{PD})	2.7	2.8	2.9	V	
Current Consumption	24	33	43	mA	V_{CC}=3.5V; V_{PD}=2.8V; V_{PD}+ V_{CC} - Current Consumption from V_{PD} is 8.5 mA Typ. @ V_{PD} = 2.8V and 12 mA Max @ V_{PD} =2.9V
	24	31	38	mA	V_{CC}=3.0V; V_{PD}=2.7V; V_{PD}+ V_{CC}
	29	36	43	mA	V_{CC}=2.5V; V_{PD}=2.9V; V_{PD}+ V_{CC}
- Power Down			10	μA	V_{CC}=3.5V; V_{PD} ≤0.9V

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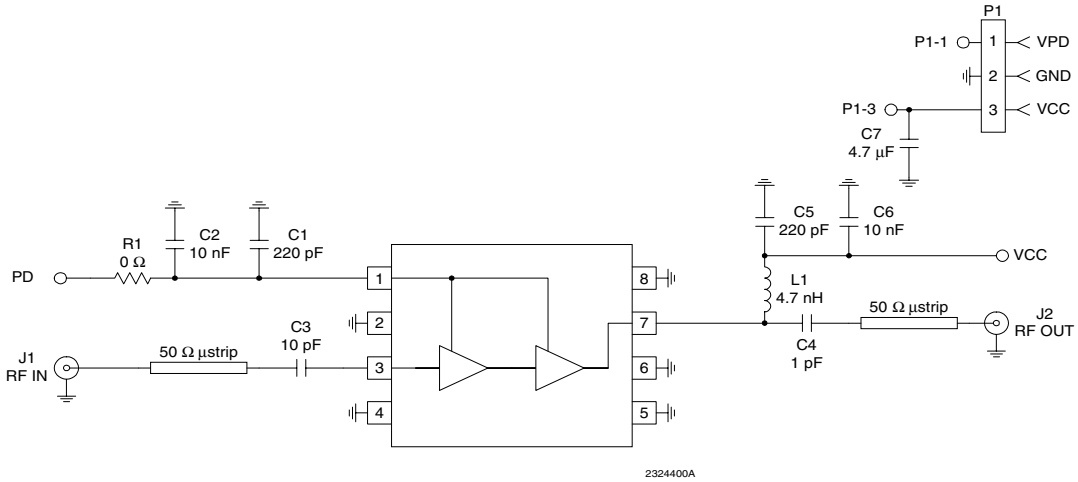
Pin	Function	Description	Interface Schematic
1	PD	Power Down for the IC. V_{PD} = 2.8V +/- 0.1V turns on the Part. V_{PD} < 0.9V turns off the Part. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Nominal current required for V_{PD} = 2.8V is 8.5 mA typical and 12 mA Max (@ V_{PD} = 2.9 V).	
2	NC	No connection. This pin is typically left unconnected or grounded.	
3	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 1880MHz.	
4	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	GND2	See pin 6.	
6	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 7 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
8	GND2	See pin 6.	

Application Schematic: ~1880 MHz Operation, Internal Collector Bias



Evaluation Board Schematic

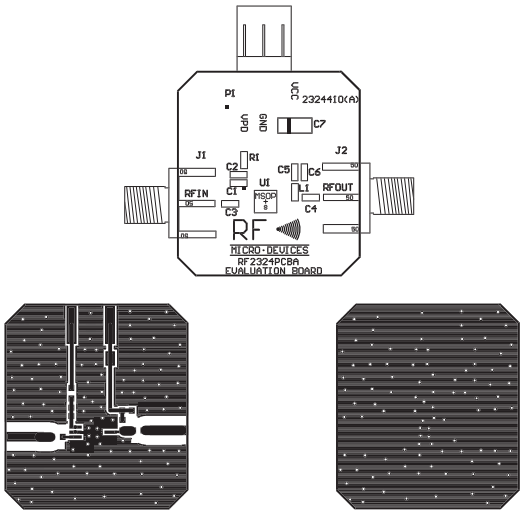
(Download Bill of Materials from www.rfmd.com.)



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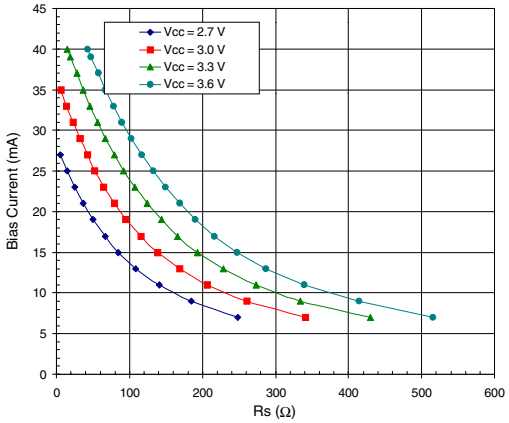
Evaluation Board Layout
Board Size 1” x 1”

Board Thickness 0.031”; Board Material FR-4; Multi-Layer

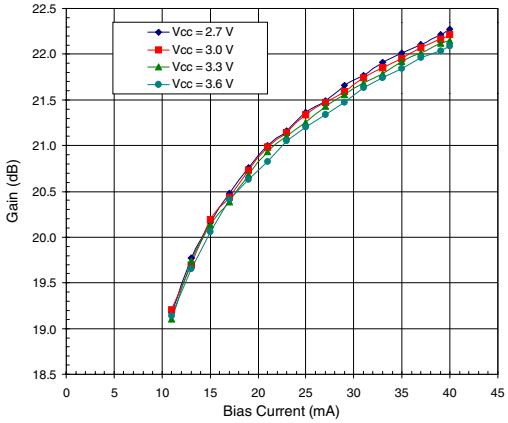


RF2324

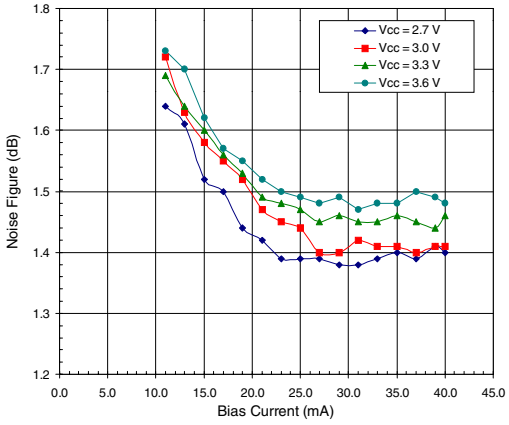
RF2324 Bias Current versus Rc



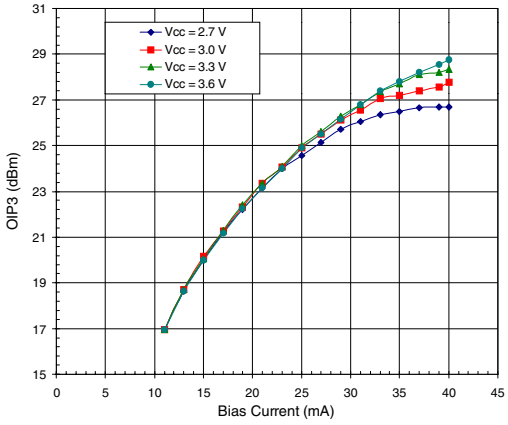
RF2324 Gain versus Bias Current



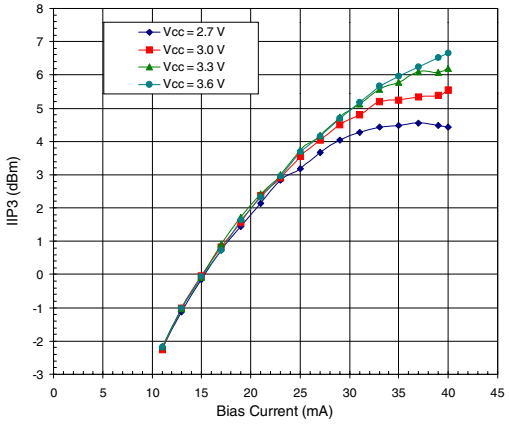
RF2324 Noise Figure versus Bias Current



RF2324 OIP3 versus Bias Current



RF2324 IIP3 versus Bias Current



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RF MICRO·DEVICES

Preliminary

RF2325

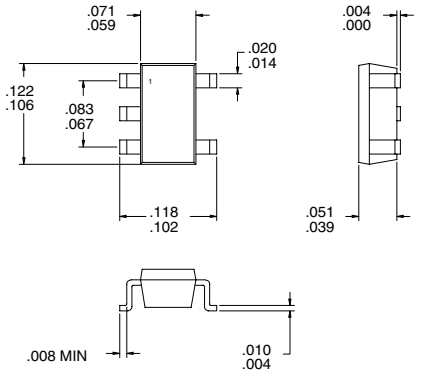
3V GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband Gain Blocks
- Final PA for Low-Power Applications
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

The RF2325 is a general purpose, low-cost silicon amplifier designed for operation from a 3V supply. The Darlington circuit configuration with resistive feedback allows for broadband cascadable amplification. The device is unconditionally stable and internally matched to 50Ω. The only external components required for specified performance are bypass and DC blocking capacitors and two bias elements (as shown in application schematic). The RF2325 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



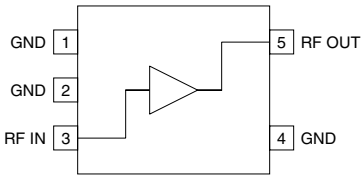
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to >2000MHz Operation
- 2.7V to 3.3V Single Supply
- +17dBm Output IP3
- 16dB Gain at 900MHz
- 12dB Gain at 1900MHz
- Internally 50Ω Matched Input and Output



Functional Block Diagram

Ordering Information

RF2325	3V General Purpose Amplifier
RF2325 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

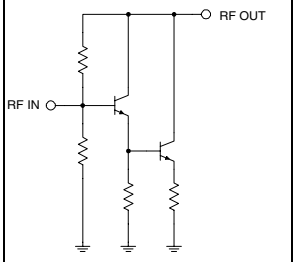
Parameter	Rating	Unit
Supply Voltage	4.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

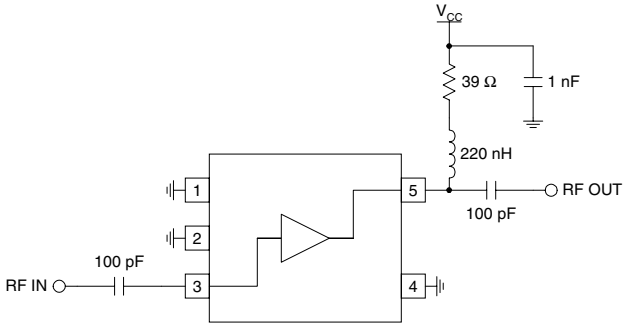
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=3.0V
Frequency Range		DC to >2000		MHz	
100MHz Performance					T=27°C, V_{CC}=3.0V
Gain		20		dB	
Noise Figure		5.0		dB	
Output IP3		18		dBm	
Output P_{1dB}		8		dBm	
Input Return Loss		15		dB	
Output Return Loss		18		dB	
Isolation		23		dB	
500MHz Performance					T=27°C, V_{CC}=3.0V
Gain		19		dB	
Noise Figure		5.0		dB	
Output IP3		18		dBm	
Output P_{1dB}		7		dBm	
Input Return Loss		12		dB	
Output Return Loss		23		dB	
Isolation		22		dB	
900MHz Performance					T=27°C, V_{CC}=3.0V
Gain	15.3	16	17.3	dB	
Noise Figure		5.0		dB	
Output IP3		17		dBm	
Output P_{1dB}		7		dBm	
Input Return Loss		10		dB	
Output Return Loss		20		dB	
Isolation		22		dB	
1000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		16		dB	
Noise Figure		5.0		dB	
Output IP3		17		dBm	
Output P_{1dB}		7		dBm	
Input Return Loss		10		dB	
Output Return Loss		19		dB	
Isolation		22		dB	
2000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		5.4		dB	
Output IP3		16		dBm	
Output P_{1dB}		6		dBm	
Input Return Loss		10		dB	
Output Return Loss		17		dB	
Isolation		19		dB	
Power Supply					
Operating Voltage		3.0±10%		V	
Operating Current	23.5	27	29.5	mA	V_{CC}=3.0V

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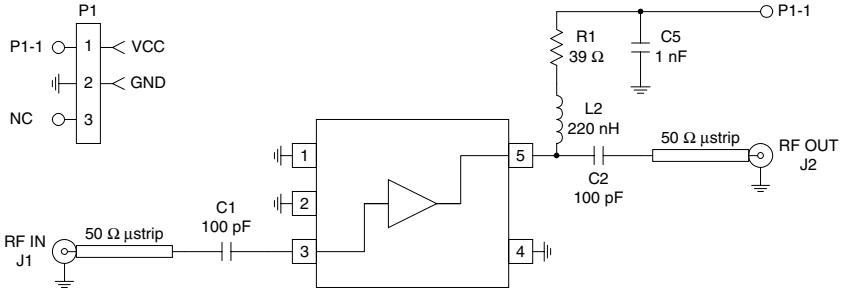
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is not externally DC blocked and thus requires an external blocking capacitor suitable for the frequency of operation. The input impedance of this pin is internally matched to 50Ω using resistive feedback.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. The input impedance of this pin is internally matched to 50Ω using resistive feedback. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well-bypassed.	See pin 3 schematic.

Application Schematic



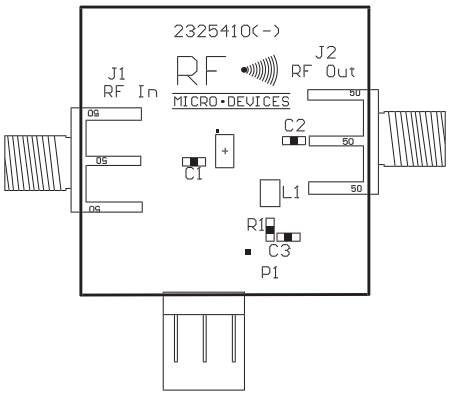
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



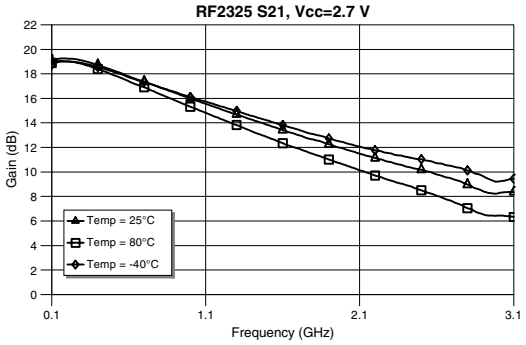
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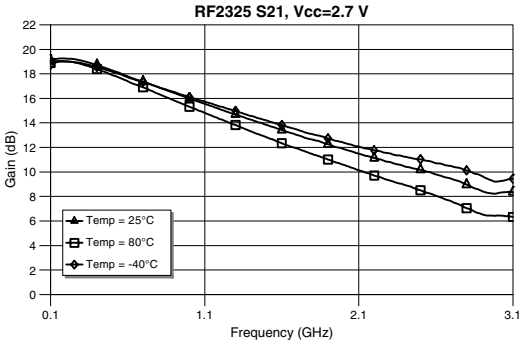
Evaluation Board Layout
1” x 1”

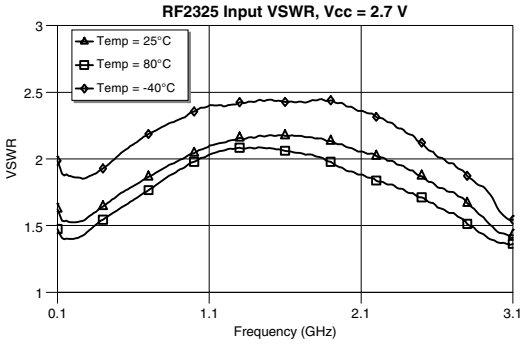


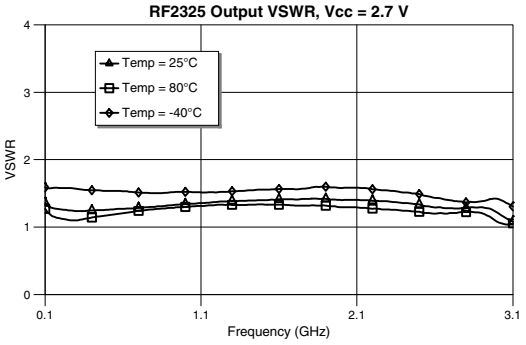


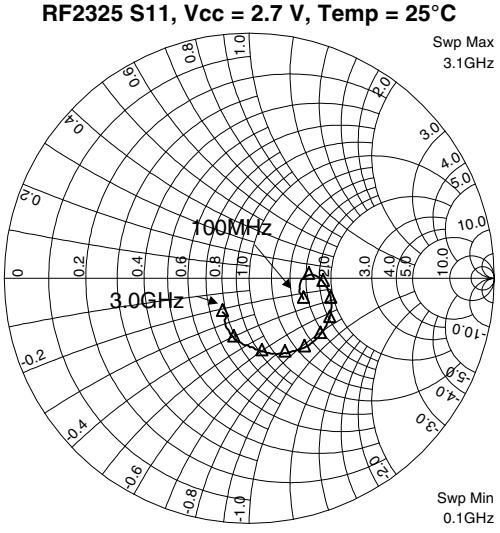
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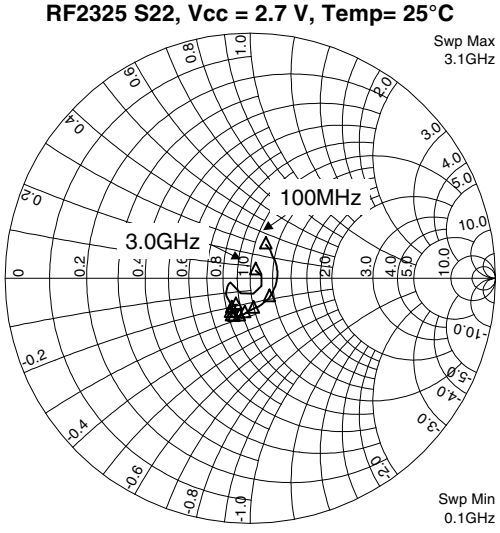










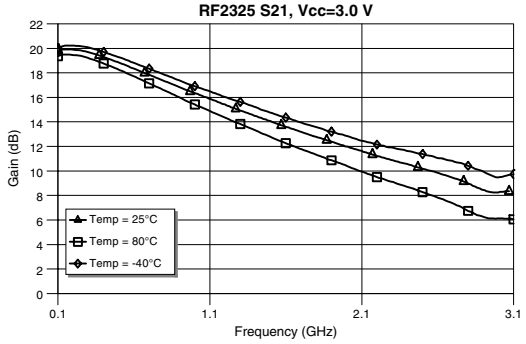


4

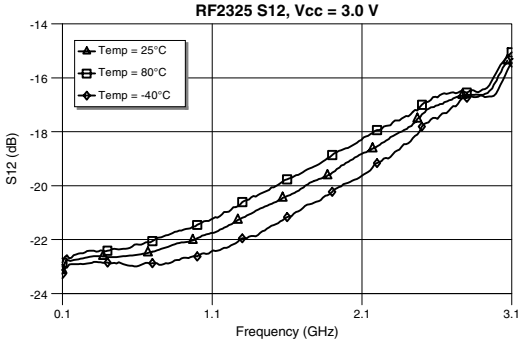
GENERAL PURPOSE AMPLIFIERS

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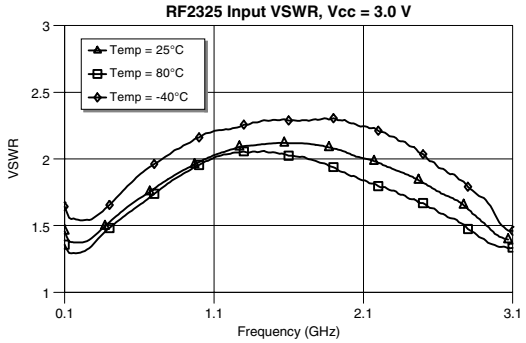
RF2325 S21, Vcc=3.0 V



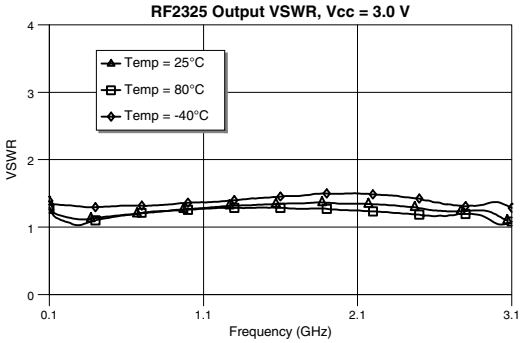
RF2325 S12, Vcc = 3.0 V



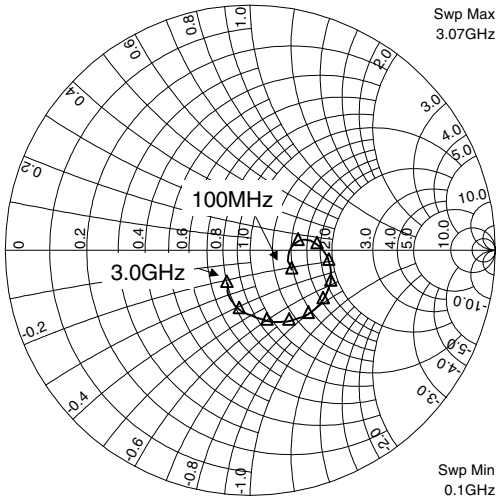
RF2325 Input VSWR, Vcc = 3.0 V



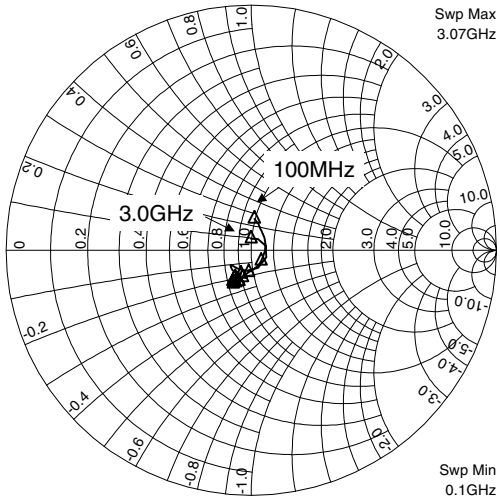
RF2325 Output VSWR, Vcc = 3.0 V



RF2325 S11, Vcc = 3.0 V, Temp = 25°C

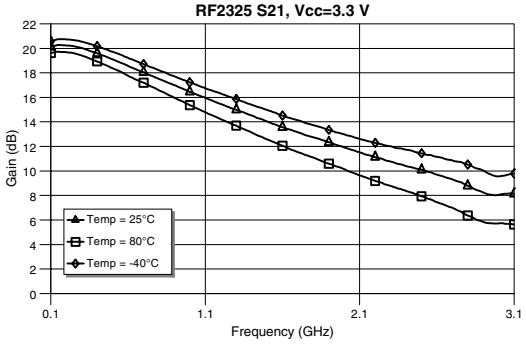


RF2325 S22, Vcc = 3.0 V, Temp= 25°C

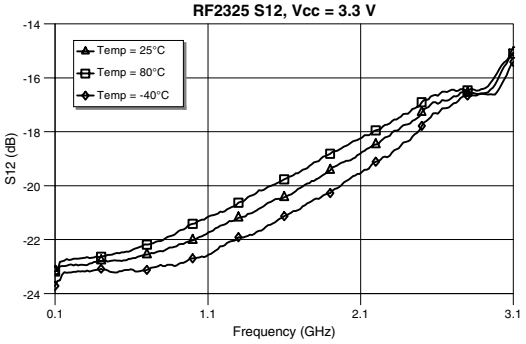


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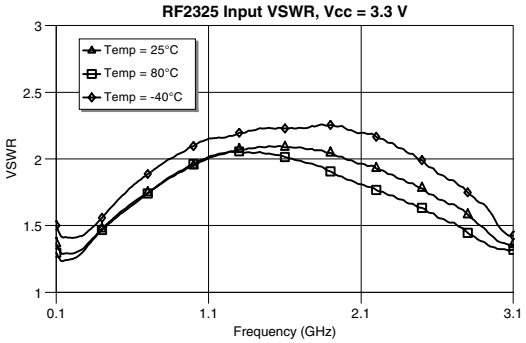
RF2325 S21, Vcc=3.3 V



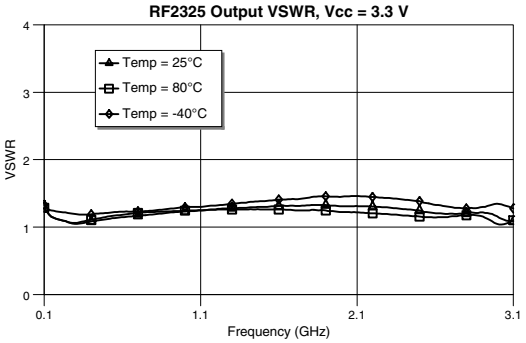
RF2325 S12, Vcc = 3.3 V



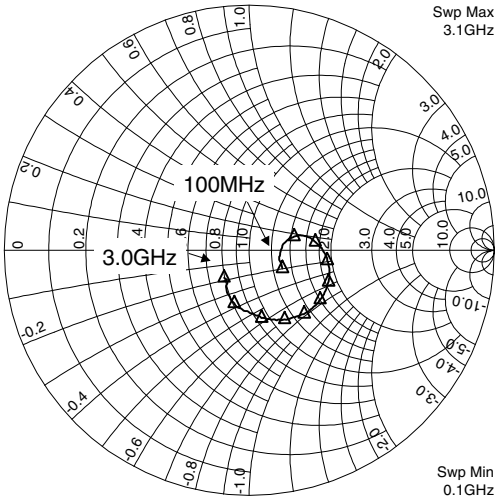
RF2325 Input VSWR, Vcc = 3.3 V



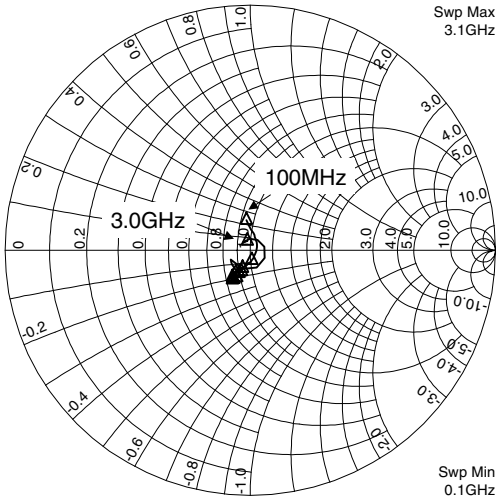
RF2325 Output VSWR, Vcc = 3.3 V



RF2325 S11, Vcc = 3.3 V, Temp = 25°C



RF2325 S22, Vcc = 3.3 V, Temp= 25°C



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MICRO·DEVICES

Preliminary

RF2326

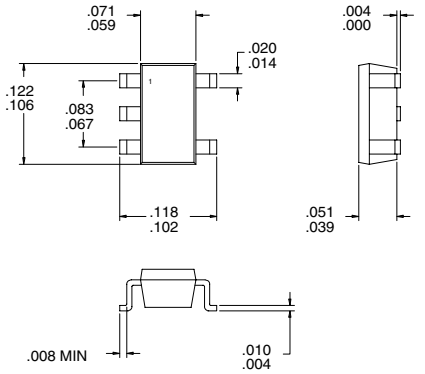
3V GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband Gain Blocks
- Final PA for Low-Power Applications
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

The RF2326 is a general purpose, low-cost silicon amplifier designed for operation from a 3V supply. The Darlington circuit configuration with resistive feedback allows for broadband cascadable amplification. The device is unconditionally stable and internally matched to 50Ω. The only external components required for specified performance are bypass and DC blocking capacitors and two bias elements (as shown in application schematic). The RF2326 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



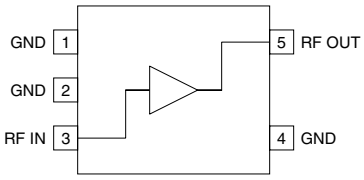
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to >2000MHz Operation
- 2.7V to 3.3V Single Supply
- +18dBm Output IP3
- 12dB Gain at 900MHz
- 10dB Gain at 1900MHz
- Internally 50Ω Matched Input and Output



Functional Block Diagram

Ordering Information

RF2326	3V General Purpose Amplifier
RF2326 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

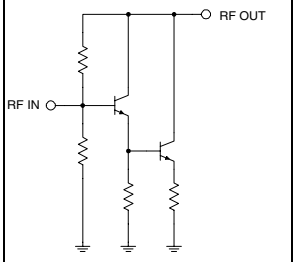
Parameter	Rating	Unit
Supply Voltage	4.0	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

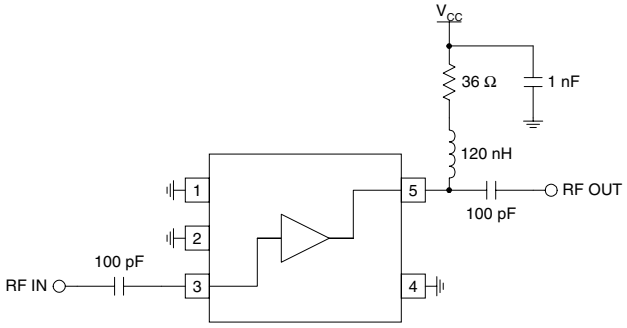
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=3.0V
Frequency Range		DC to >2000		MHz	
100MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		5.9		dB	
Output IP3		19		dBm	
Output P_{1dB}		7		dBm	
Input Return Loss		13		dB	
Output Return Loss		13		dB	
Isolation		18		dB	
500MHz Performance					T=27°C, V_{CC}=3.0V
Gain		13		dB	
Noise Figure		5.9		dB	
Output IP3		19		dBm	
Output P_{1dB}		8		dBm	
Input Return Loss		15		dB	
Output Return Loss		27		dB	
Isolation		17		dB	
900MHz Performance					T=27°C, V_{CC}=3.0V
Gain	10.6	12	13.5	dB	
Noise Figure		5.7		dB	
Output IP3		18		dBm	
Output P_{1dB}		7		dBm	
Input Return Loss		12		dB	
Output Return Loss		21		dB	
Isolation		18		dB	
1000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		12		dB	
Noise Figure		5.8		dB	
Output IP3		17		dBm	
Output P_{1dB}		6		dBm	
Input Return Loss		11		dB	
Output Return Loss		20		dB	
Isolation		18		dB	
2000MHz Performance					T=27°C, V_{CC}=3.0V
Gain		10		dB	
Noise Figure		5.8		dB	
Output IP3		13		dBm	
Output P_{1dB}		4		dBm	
Input Return Loss		9		dB	
Output Return Loss		16		dB	
Isolation		18		dB	
Power Supply					
Operating Voltage		3.0±10%		V	
Operating Current	24.6	25	28.7	mA	V_{CC}=3.0V

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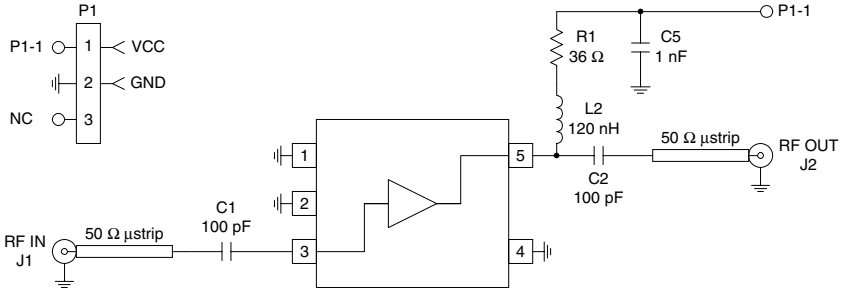
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is not externally DC blocked and thus requires an external blocking capacitor suitable for the frequency of operation. The input impedance of this pin is internally matched to 50Ω using resistive feedback.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. The input impedance of this pin is internally matched to 50Ω using resistive feedback. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well-bypassed.	See pin 3 schematic.

Application Schematic



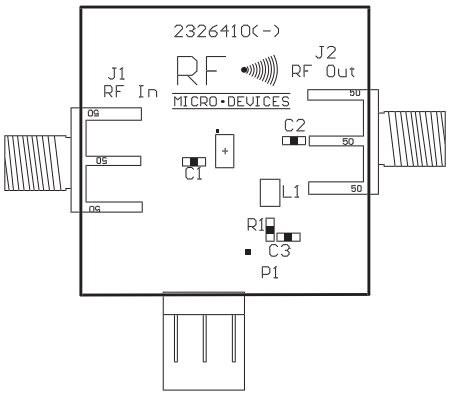
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



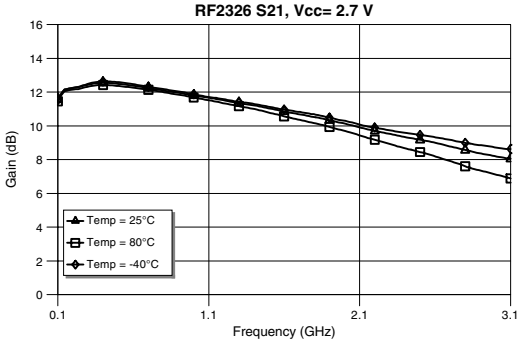
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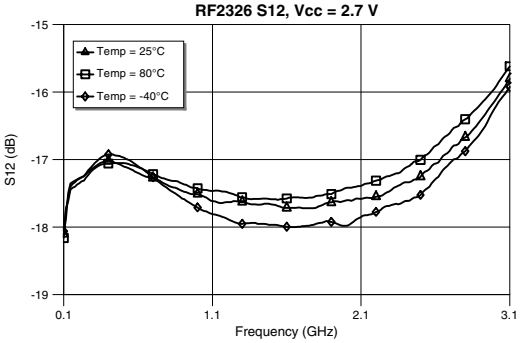
Evaluation Board Layout
1” x 1”

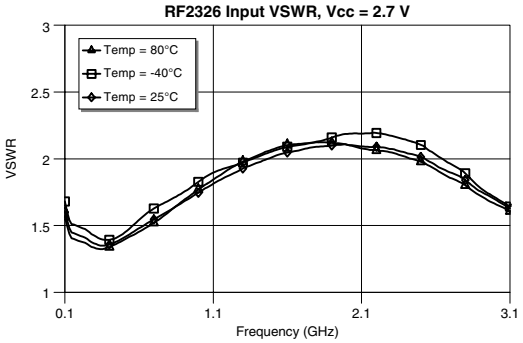


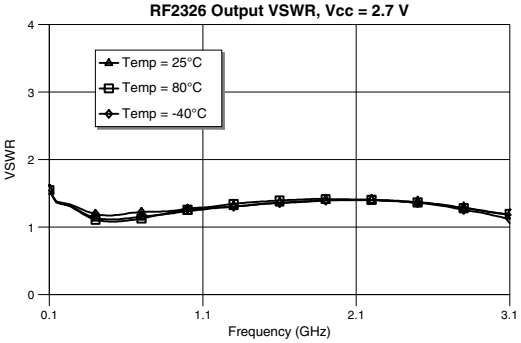


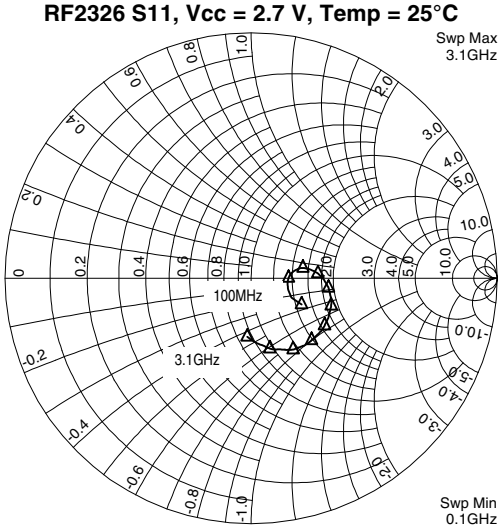
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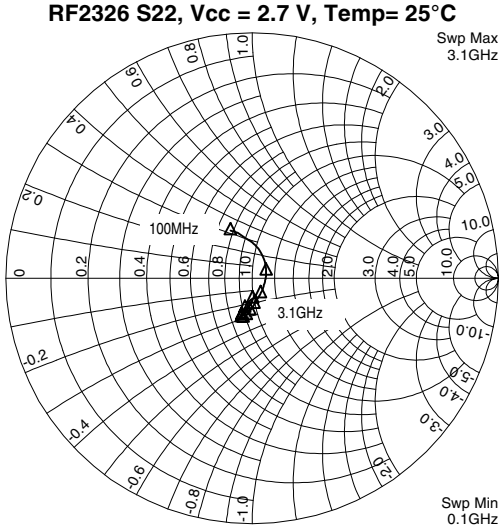








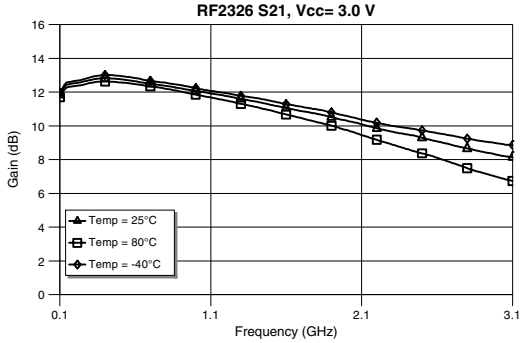




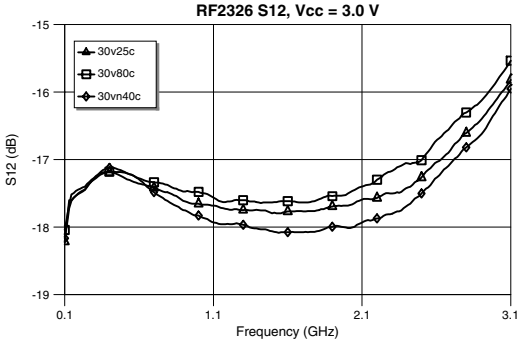
4

GENERAL PURPOSE AMPLIFIERS

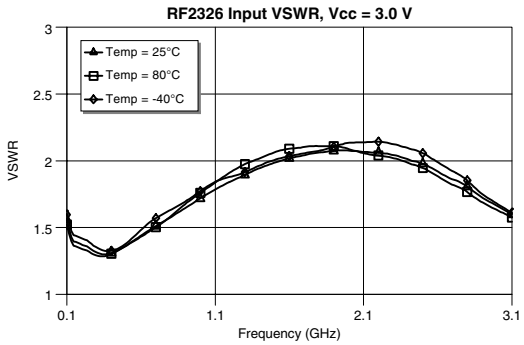
RF2326 S21, Vcc= 3.0 V



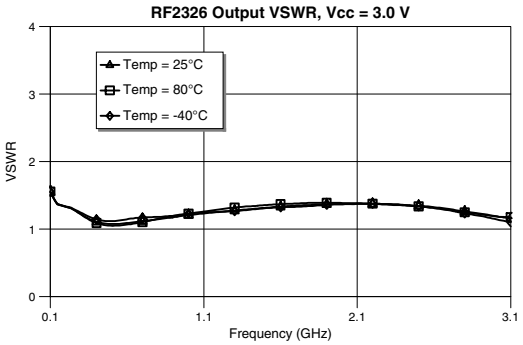
RF2326 S12, Vcc = 3.0 V



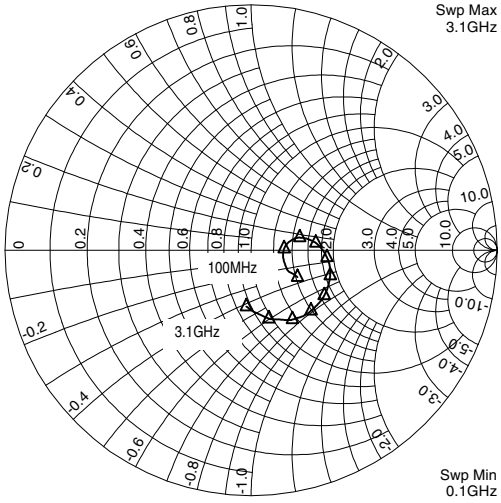
RF2326 Input VSWR, Vcc = 3.0 V



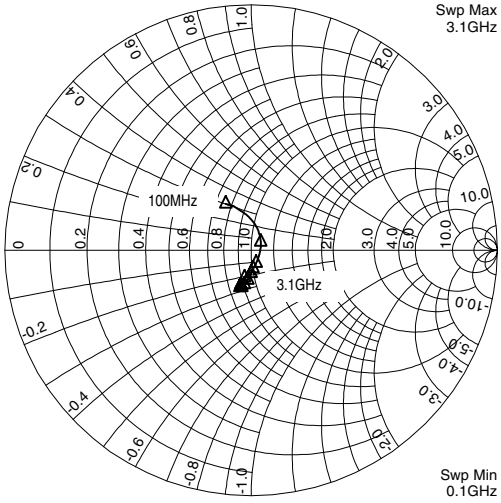
RF2326 Output VSWR, Vcc = 3.0 V



RF2326 S11, Vcc = 3.0 V, Temp = 25°C

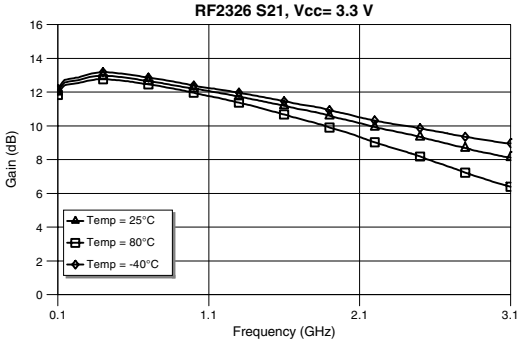


RF2326 S22, Vcc = 3.0 V, Temp= 25°C

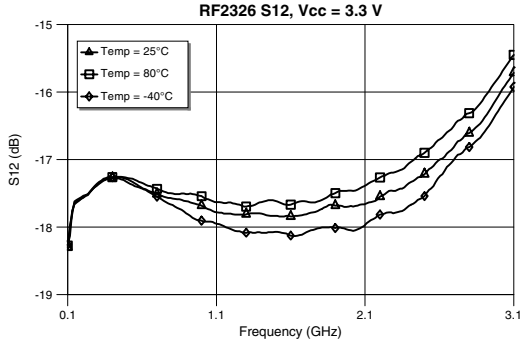


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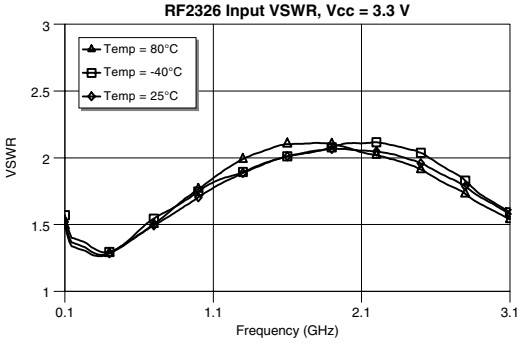
RF2326 S21, Vcc= 3.3 V



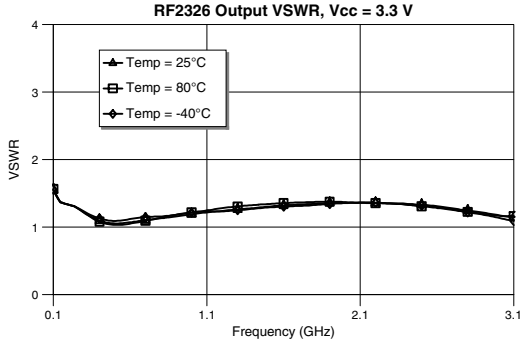
RF2326 S12, Vcc = 3.3 V



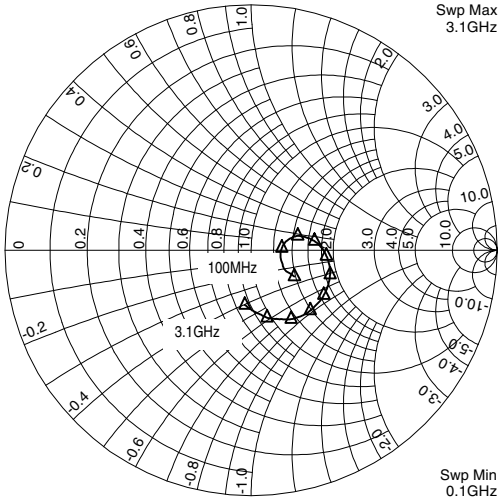
RF2326 Input VSWR, Vcc = 3.3 V



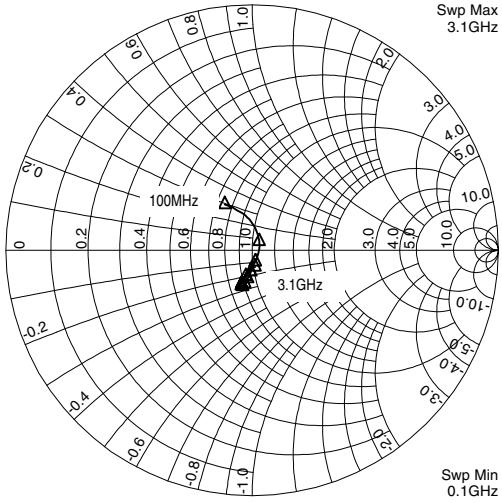
RF2326 Output VSWR, Vcc = 3.3 V



RF2326 S11, Vcc = 3.3 V, Temp = 25°C



RF2326 S22, Vcc = 3.3 V, Temp= 25°C



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RF2333

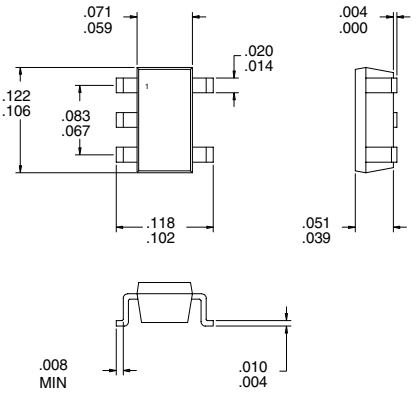
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Broadband Test Equipment

Product Description

The RF2333 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. The RF2333 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



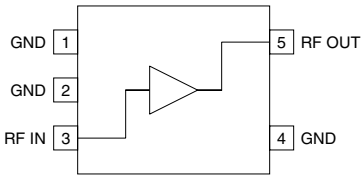
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 6000MHz Operation
- Internally matched Input and Output
- 10dB Small Signal Gain
- +34dBm Output IP3
- +18.5dBm Output Power
- Good Gain Flatness



Functional Block Diagram

Ordering Information

RF2333	General Purpose Amplifier
RF2333 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2333

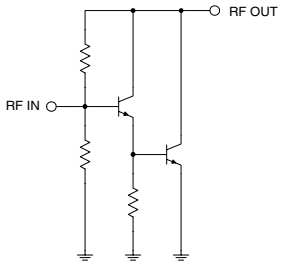
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	120	mA
Input RF Power	+20	dBm
Operating Ambient Temperature	-40 to +65	°C
Storage Temperature	-60 to +150	°C

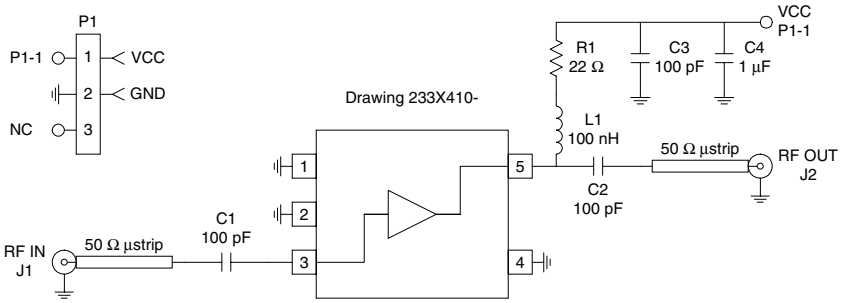
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

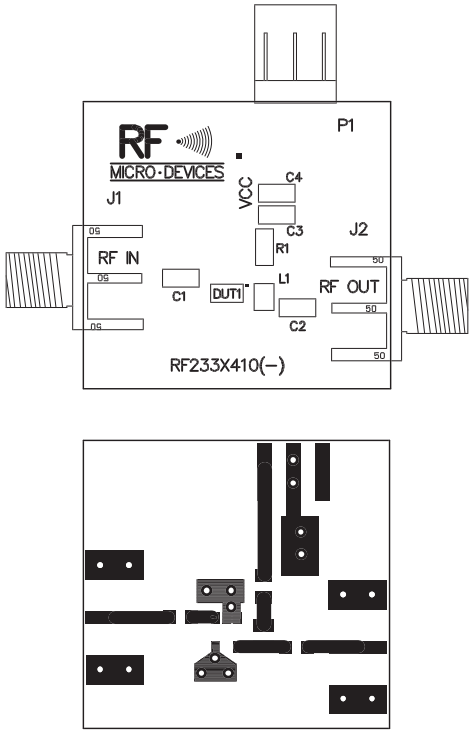
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_D=5.5V, I_{CC}=70mA
Frequency Range		DC to 6000		MHz	
3dB Bandwidth		6		GHz	
Gain		11.2		dB	Freq=100MHz
		11		dB	Freq=1000MHz
		10.4		dB	Freq=2000MHz
		10.2		dB	Freq=3000MHz
		10			Freq=4000MHz
		9.2			Freq=5000MHz
		8.3			Freq=6000MHz
Gain Flatness		±0.4		dB	100MHz to 2000MHz
Noise Figure		8.2		dB	Freq=2000MHz
Input VSWR		1.7:1			In a 50Ω system, DC to 4000MHz
Output VSWR		1.7:1			In a 50Ω system, DC to 4000MHz
Output IP_3		+34.5		dBm	Freq=1000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+18.5		dBm	Freq=1000MHz
Reverse Isolation		17		dB	Freq=2000MHz
Power Supply					With 22Ω bias resistor
Device Operating Voltage	5.0	5.5	6.0	V	At pin 3 with I_{CC}=70mA
Operating Current		70		mA	

Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 120 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 5.5V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

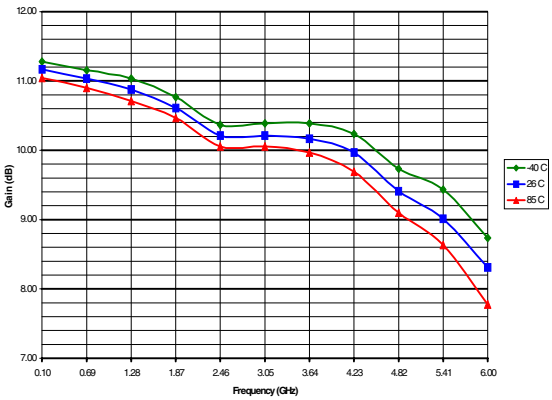
Evaluation Board Schematic



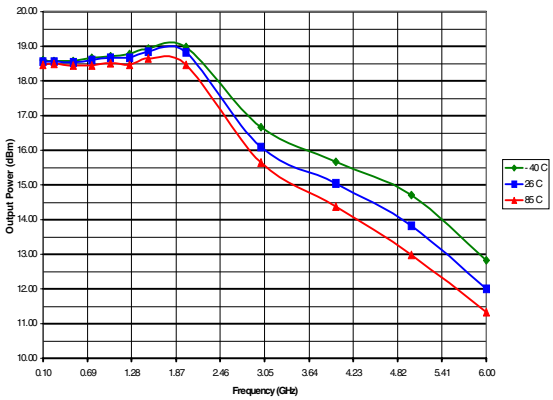
Evaluation Board Layout
Board Size 1” x 1”



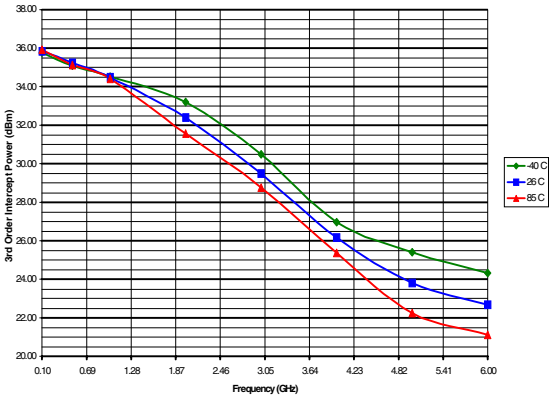
RF2333 Gain vs. Frequency across Temperature
Icc = 70 mA



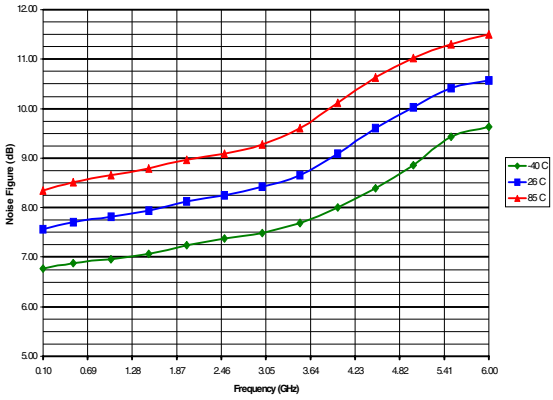
RF2333 Output P1dB vs. Frequency across Temperature
Icc = 70 mA



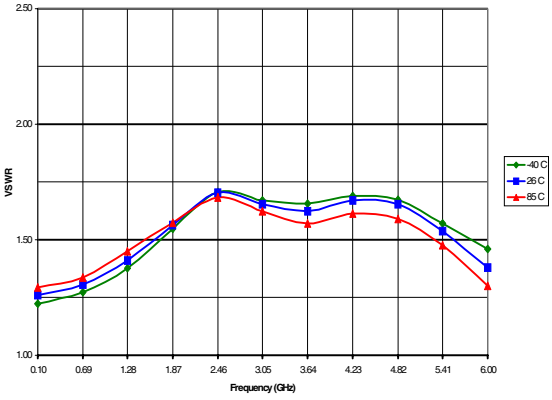
RF2333 Output IP3 vs. Frequency across Temperature
Icc = 70 mA



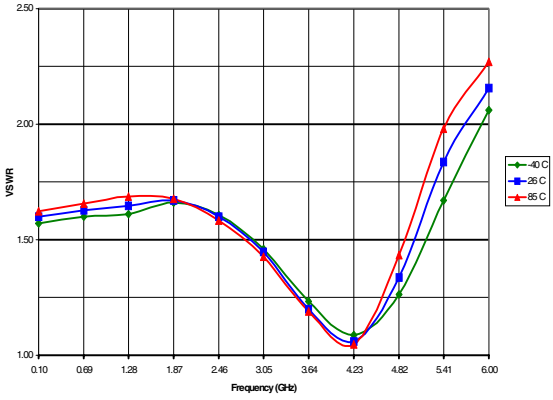
RF2333 Noise Figure vs. Frequency across Temperature
Icc = 70 mA

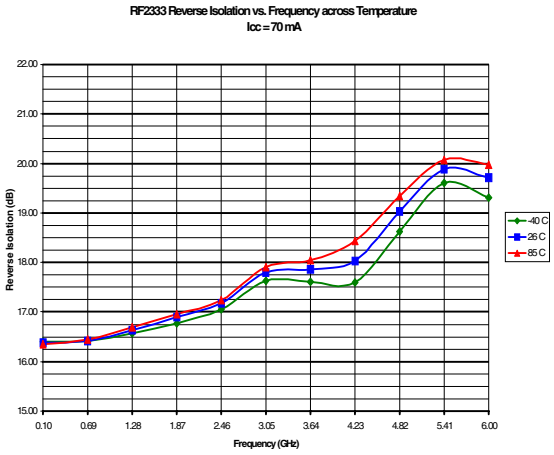


RF2333 Input VSWR vs. Frequency across Temperature
Icc = 70 mA



RF2333 Output VSWR vs. Frequency across Temperature
Icc = 70 mA




RF2333 Reverse Isolation vs. Frequency across Temperature
Icc = 70 mA
Reverse Isolation (dB)
22.00
21.00
20.00
19.00
18.00
17.00
16.00
15.00
0.10
0.69
1.28
1.87
2.46
3.05
3.64
4.23
4.82
5.41
6.00
Frequency (GHz)
-40 C
25 C
85 C

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RF2334

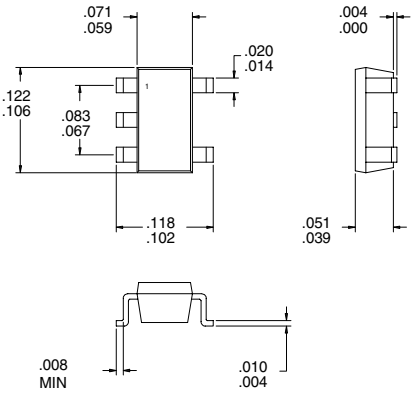
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Broadband Test Equipment

Product Description

The RF2334 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 4000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. The RF2334 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



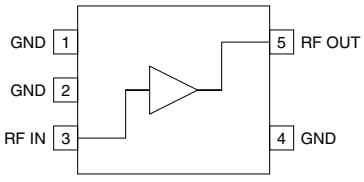
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 4000MHz Operation
- Internally matched Input and Output
- 16dB Small Signal Gain
- 5dB Noise Figure
- 50mW Linear Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2334	General Purpose Amplifier
RF2334 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2334

Absolute Maximum Ratings

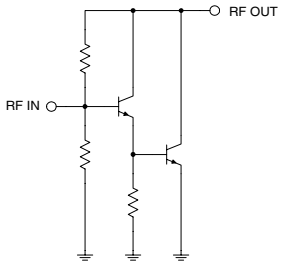
Parameter	Rating	Unit
Supply Current	120	mA
Input RF Power	+13	dBm
Operating Ambient Temperature	-40 to +75	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

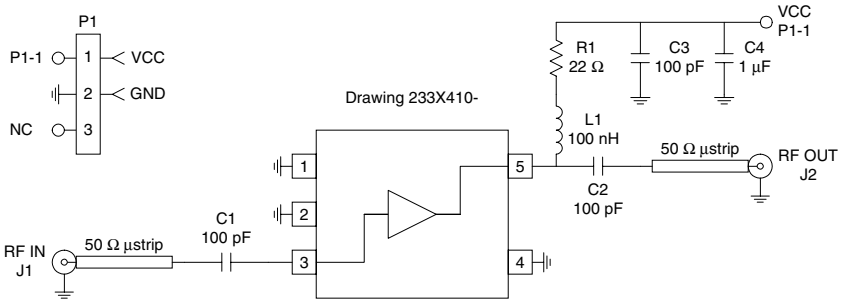
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=65mA
Frequency Range		DC to 4000		MHz	
3dB Bandwidth		2.5		GHz	
Gain		19.4		dB	Freq=100MHz
		18		dB	Freq=1000MHz
		16		dB	Freq=2000MHz
		14		dB	Freq=3000MHz
		13			Freq=4000MHz
Gain Flatness		±2		dB	100MHz to 2000MHz
Noise Figure		4.8		dB	Freq=2000MHz
Input VSWR		2.1:1			In a 50Ω system, DC to 4000MHz
Output VSWR		1.8:1			In a 50Ω system, DC to 4000MHz
Output IP_3		+33		dBm	Freq=1000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+18.5		dBm	Freq=1000MHz
Reverse Isolation		20.5		dB	Freq=2000MHz
Power Supply					With 22Ω bias resistor
Device Operating Voltage		4.8		V	At pin 3 with I_{CC}=65mA
Operating Current		65		mA	

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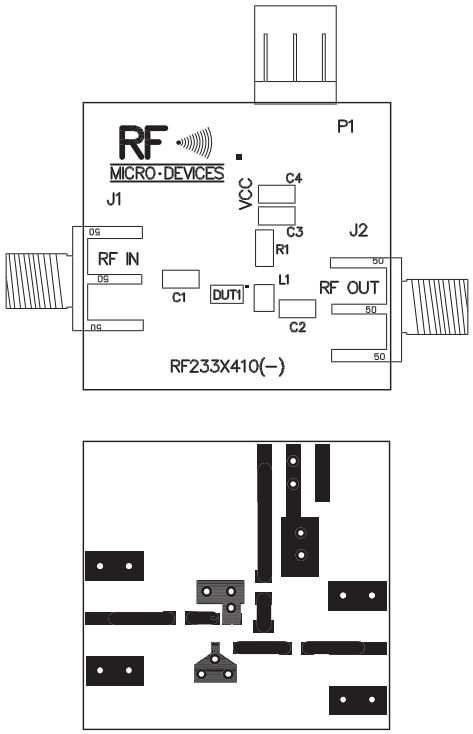
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 120 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 4.9V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1” x 1”



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RF2335

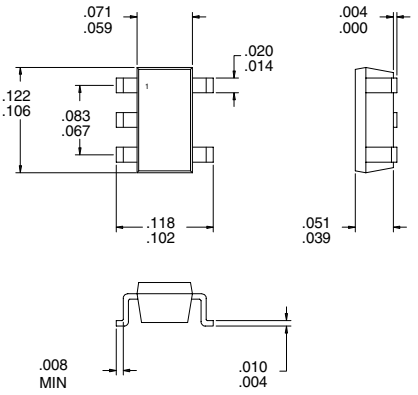
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Broadband Test Equipment

Product Description

The RF2335 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. The RF2335 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



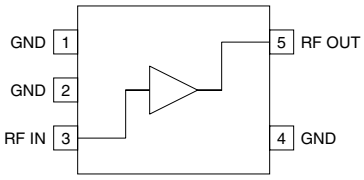
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 6000MHz Operation
- Internally matched Input and Output
- 12dB Small Signal Gain
- +33dBm Output IP3
- +17dBm Output Power
- Good Gain Flatness



Functional Block Diagram

Ordering Information

RF2335	General Purpose Amplifier
RF2335 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2335

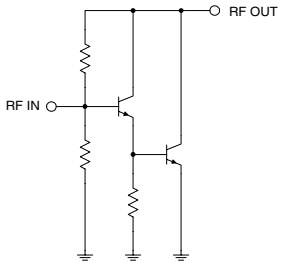
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	120	mA
Input RF Power	+20	dBm
Operating Ambient Temperature	-40 to +70	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

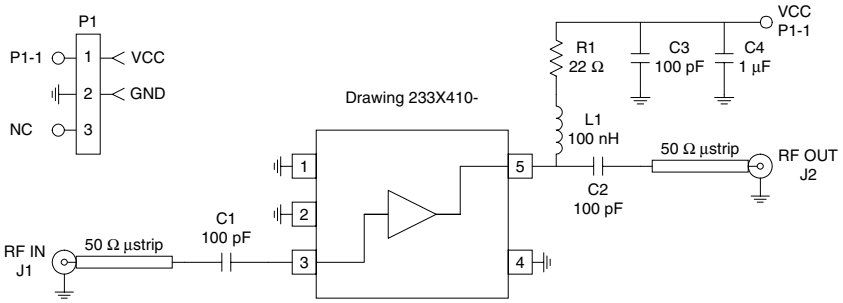
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=65mA
Frequency Range		DC to 6000		MHz	
3dB Bandwidth		3		GHz	
Gain		13.7		dB	Freq=100MHz
		13.1		dB	Freq=1000MHz
		12.4		dB	Freq=2000MHz
		11		dB	Freq=3000MHz
		10.6		dB	Freq=4000MHz
		10		dB	Freq=5000MHz
		9.8		dB	Freq=6000MHz
Gain Flatness		±1		dB	100MHz to 2000MHz
Noise Figure		5.6		dB	Freq=1000MHz
Input VSWR		1.8:1			In a 50Ω system, DC to 2000MHz
Output VSWR		1.7:1			In a 50Ω system, DC to 2000MHz
Output IP_3		+33		dBm	Freq=1000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+17.3		dBm	Freq=1000MHz
Reverse Isolation		17.2		dB	Freq=2000MHz
Power Supply					With 22Ω bias resistor
Device Operating Voltage		5.0		V	At pin 3 with I_{CC}=65mA
Operating Current		65		mA	

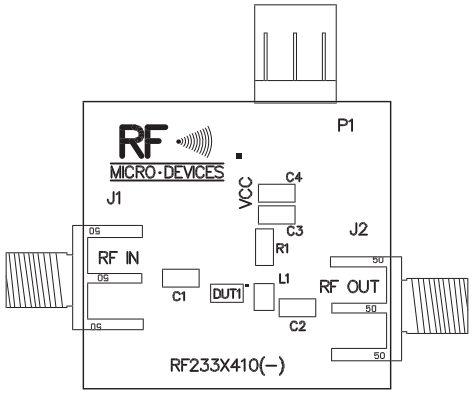
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 120 mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 5.0V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

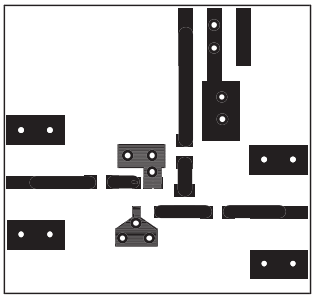
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1” x 1”





RF2336

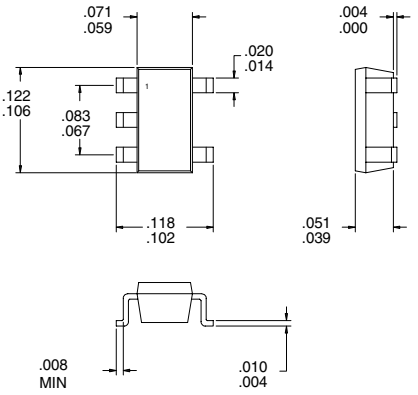
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Broadband Test Equipment

Product Description

The RF2336 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 3000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. The RF2336 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



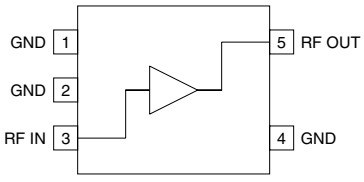
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 3000MHz Operation
- Internally matched Input and Output
- 20dB Small Signal Gain
- 3.8dB Noise Figure
- 10mW Linear Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2336	General Purpose Amplifier
RF2336 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2336

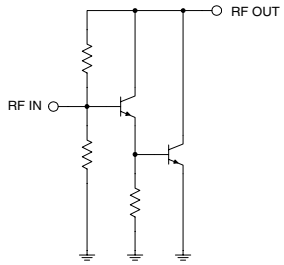
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	75	mA
Input RF Power	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

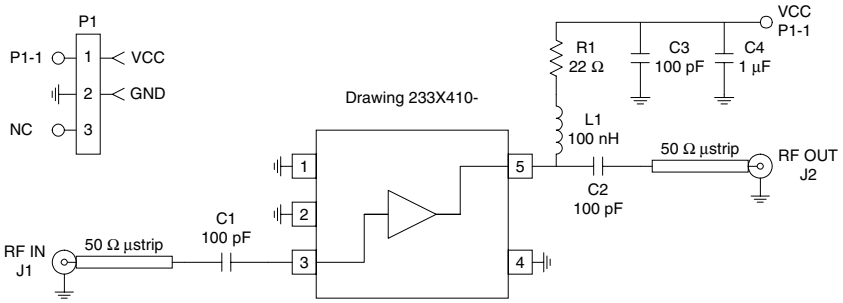
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=35mA
Frequency Range		DC to 3000		MHz	
Gain		22		dB	Freq=100MHz
		20.5		dB	Freq=1000MHz
		18		dB	Freq=2000MHz
		15.3		dB	Freq=3000MHz
Gain Flatness		±2		dB	100MHz to 2000MHz
Noise Figure		3.8		dB	Freq=2000MHz
Input VSWR		2.3:1			In a 50Ω system, DC to 3000MHz
Output VSWR		2.1:1			In a 50Ω system, DC to 3000MHz
Output IP_3		+22.5		dBm	Freq=2000MHz±50kHz, P_{TONE}=-18dBm
Output P_{1dB}		+11.2		dBm	Freq=2000MHz
Reverse Isolation		20.7		dB	Freq=2000MHz
Power Supply					With 22Ω bias resistor
Device Operating Voltage		3.5		V	At pin 3 with I_{CC}=35mA
Operating Current		35		mA	

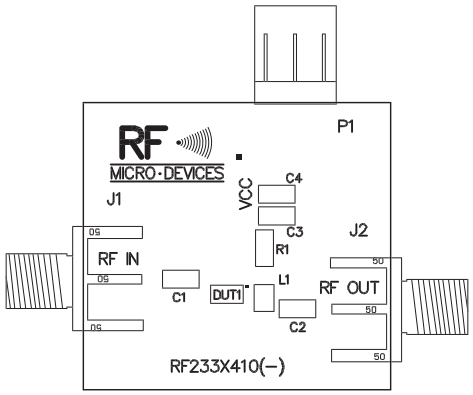
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 75mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

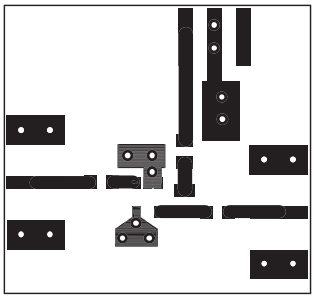
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1” x 1”





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RF2337

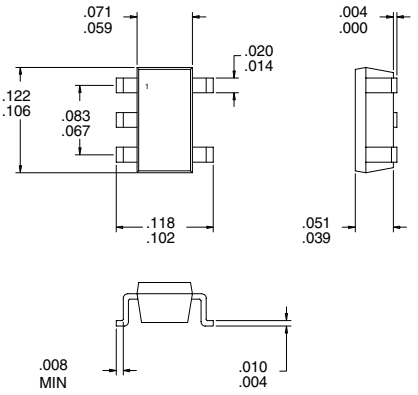
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Broadband Test Equipment

Product Description

The RF2337 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. The RF2337 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



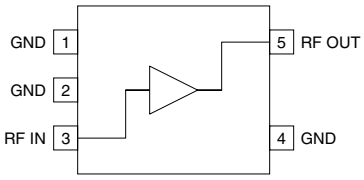
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 6000MHz Operation
- Internally matched Input and Output
- 15dB Small Signal Gain
- +25dBm Output IP3
- +12dBm Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2337	General Purpose Amplifier
RF2337 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2337

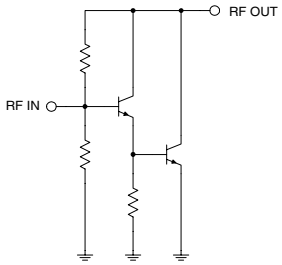
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	75	mA
Input RF Power	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

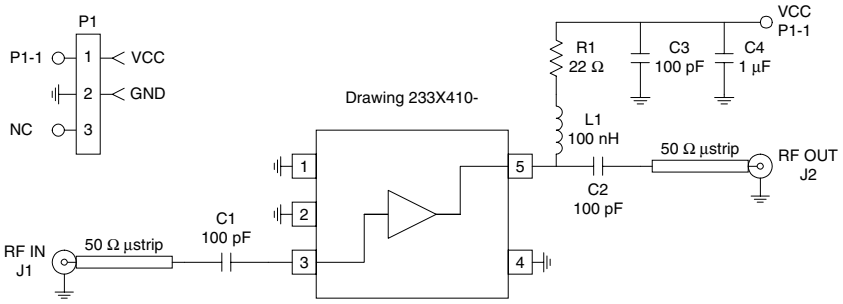
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=40mA
Frequency Range		DC to 6000		MHz	
3dB Bandwidth		2		GHz	
Gain		16		dB	Freq=100MHz
		15.4		dB	Freq=1000MHz
		14.4		dB	Freq=2000MHz
		12.5		dB	Freq=3000MHz
		11.5			Freq=4000MHz
		10.6			Freq=5000MHz
		10			Freq=6000MHz
Noise Figure		4.5		dB	Freq=2000MHz
Input VSWR		2.0:1			In a 50Ω system, DC to 3000MHz
Output VSWR		2.0:1			In a 50Ω system, DC to 3000MHz
Output IP_3		+25		dBm	Freq=1000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+11.8		dBm	Freq=2000MHz
Reverse Isolation		17.5		dB	Freq=2000MHz
Power Supply					With 22Ω bias resistor
Device Operating Voltage		3.6		V	At pin 3 with I_{CC}=40mA
Operating Current		40		mA	

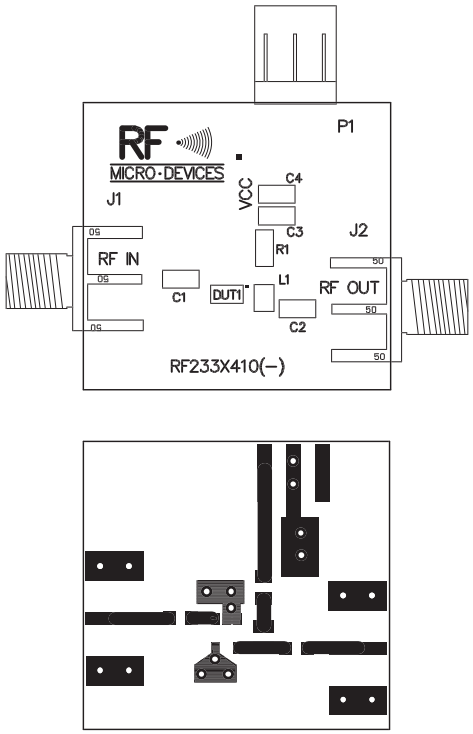
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 75mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1” x 1”



RF2338

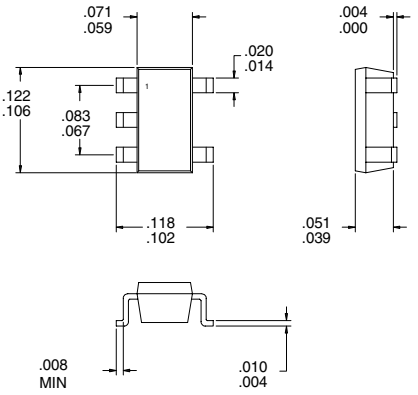
GENERAL PURPOSE AMPLIFIER

Typical Applications

- Broadband, Low Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low Power Applications
- Broadband Test Equipment

Product Description

The RF2338 is a general purpose, low cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC biasing elements to operate as specified. The RF2338 is available in a very small industry-standard SOT-23 5-lead surface mount package, enabling compact designs which conserve board space.



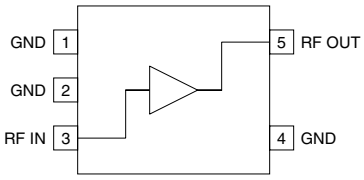
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- DC to 6000MHz Operation
- Internally matched Input and Output
- 12dB Small Signal Gain
- +24dBm Output IP3
- +11dBm Output Power
- Single Positive Power Supply



Functional Block Diagram

Ordering Information

RF2338	General Purpose Amplifier
RF2338 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2338

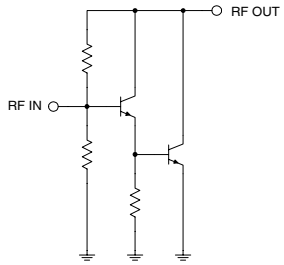
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current	75	mA
Input RF Power	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-60 to +150	°C

Caution! ESD sensitive device.

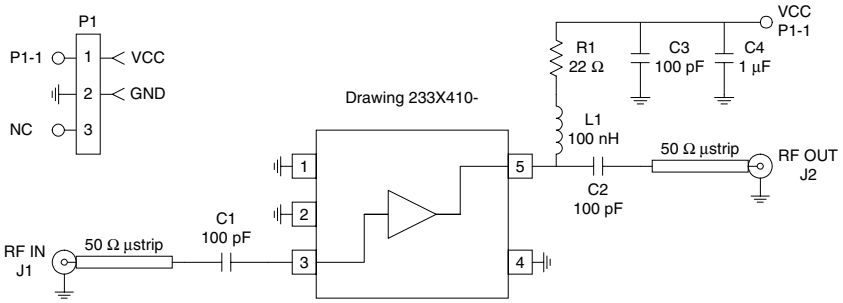
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, I_{CC}=40mA
Frequency Range		DC to 6000		MHz	
3dB Bandwidth		3.5		GHz	
Gain		12.1		dB	Freq=100MHz
		11.8		dB	Freq=1000MHz
		11.2		dB	Freq=2000MHz
		9.7		dB	Freq=3000MHz
		8.7		dB	Freq=4000MHz
		8		dB	Freq=5000MHz
		7.3		dB	Freq=6000MHz
Gain Flatness		±0.5		dB	100MHz to 2000MHz
Noise Figure				dB	Freq=2000MHz
Input VSWR		2.0:1			In a 50Ω system, DC to 3000MHz
Output VSWR		2.0:1			In a 50Ω system, DC to 3000MHz
Output IP_3		+24		dBm	Freq=2000MHz±50kHz, P_{TONE}=-10dBm
Output P_{1dB}		+10.5		dBm	Freq=2000MHz
Reverse Isolation		15.6		dB	Freq=2000MHz
Power Supply					With 22Ω bias resistor
Device Operating Voltage		3.6		V	At pin 3 with I_{CC}=40mA
Operating Current		40		mA	

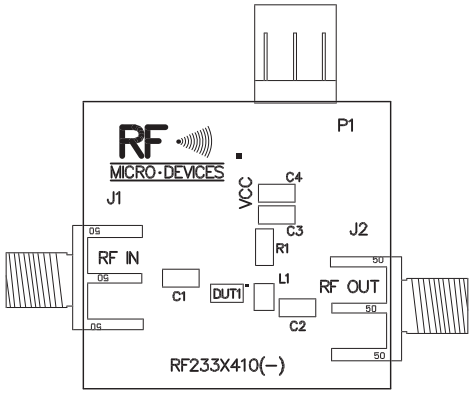
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	GND	Same as pin 1.	
3	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
4	GND	Same as pin 1.	
5	RF OUT	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$$ Care should also be taken in the resistor selection to **ensure that the current into the part never exceeds 75mA over the planned operating temperature**. This means that a resistor between the supply and this pin is always required, even if a supply near 3.6V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	

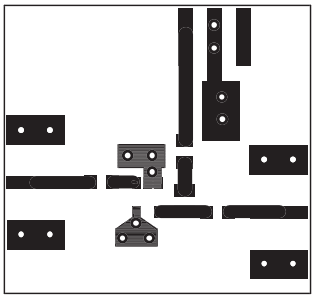
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1” x 1”





RF2347

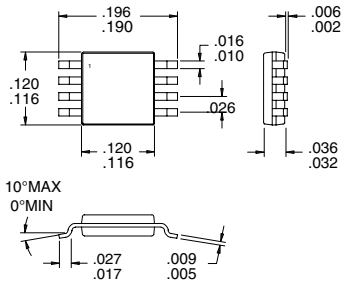
3V LOW NOISE AMPLIFIER/ 3V PA DRIVER AMPLIFIER

Typical Applications

- TDMA/CDMA/FM Cellular LNA
- Low Noise Transmit Driver Amplifier
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

The RF2347 is a low noise amplifier with a very high dynamic range designed for digital cellular applications at 900MHz. The device functions as an outstanding front end low noise amplifier or power amplifier driver amplifier in the transmit chain of digital subscriber units where low transmit noise power is a concern. When used as an LNA, the bias current can be set externally. When used as a PA driver, the IC can operate directly from a single cell Li-ion battery and includes a power down feature that can be used to completely turn off the device. The IC is featured in a standard miniature 8-lead plastic MSOP package.



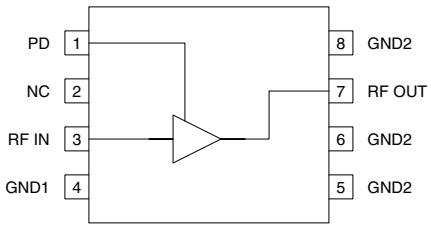
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8

Features

- Low Noise and High Intercept Point
- Power Down Control
- Single 2.5V to 6.0V Power Supply
- 150MHz to 2500MHz Operation
- Extremely Small MSOP-8 Package



Functional Block Diagram

Ordering Information

RF2347	3V Low Noise Amplifier/ 3V PA Driver Amplifier
RF2347 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2347

Absolute Maximum Ratings

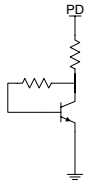
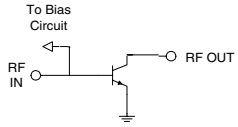
Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

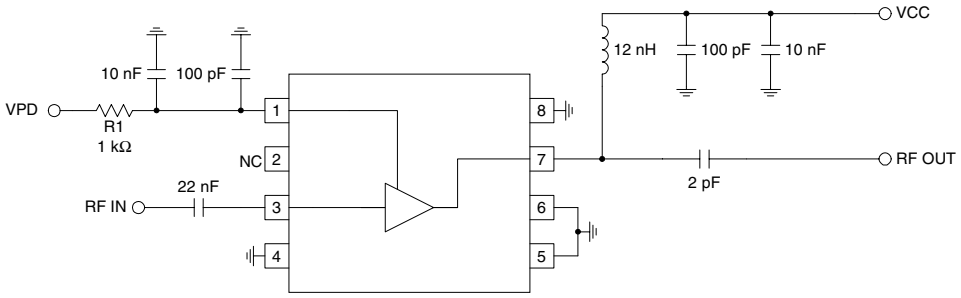
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		150 to 2500		MHz	
Low Noise Amplifier 880MHz Performance					Schematic per LNA Application; T = 25°C, RF = 880MHz
Gain	19.5	21.0		dB	V_{CC}=3.0V, I_{CC}=11mA
	19.5	21.0		dB	V_{CC}=2.7V, I_{CC}=11mA
Noise Figure		1.4	1.6	dB	V_{CC}=3.0V, I_{CC}=11mA
		1.4	1.6	dB	V_{CC}=2.7V, I_{CC}=11mA
Input IP3		+6.0		dBm	V_{CC}=3.0V, I_{CC}=11mA
		+5.0		dBm	V_{CC}=2.7V, I_{CC}=11mA
Max Input IP3		+7.5		dBm	V_{CC}=3.0V, I_{CC}=20mA
		+6.0		dBm	V_{CC}=2.7V, I_{CC}=20mA
Driver Amplifier 836MHz Performance					Schematic per Driver Amplifier Application T = 25°C, RF = 836MHz, V_{PD}=2.8V
Gain	19.5	20.5	21.5	dB	V_{CC}=3.5V
	19.5	20.5	21.5	dB	V_{CC}=3.0V
	19.5	20.5	21.5	dB	V_{CC}=2.5V
Output IP3	25	+28.5	35	dBm	V_{CC}=3.5V
		+28.5		dBm	V_{CC}=3.0V
		+27		dBm	V_{CC}=2.5V
Noise Figure		1.4	2.0	dB	V_{CC}=3.5V
		1.4	2.0	dB	V_{CC}=3.0V
		1.3	2.0	dB	V_{CC}=2.5V
Reverse Isolation		26		dB	V_{CC}=3.5V
		26		dB	V_{CC}=3.0V
		25		dB	V_{CC}=2.5V
Input VSWR		1.5:1	2.0:1		
Output VSWR		1.25:1	2.0:1		Using External LC network used on Evaluation Board
P_{1dB}	13	15.5		dBm	V_{CC}=3.5V
	12	14.5		dBm	V_{CC}=3.0V
	10.5	13		dBm	V_{CC}=2.5V
Power Supply					T = 25 °C
Voltage (V_{CC})		2.5 to 6.0		V	
Voltage (V_{PD})	2.7	2.8	2.9	V	
Current Consumption	12.5	22	26.5	mA	V_{CC}=3.5V; V_{PD}=2.8V; V_{PD}+ V_{CC} - Current Consumption from V_{PD} is 2.0 mA Typ. @ V_{PD} = 2.8V and 3.0 mA Max @ V_{PD} =2.9V
	18	20	22	mA	V_{CC}=3.5V; V_{PD}=2.7V; V_{PD}+ V_{CC}
	19	24	29	mA	V_{CC}=3.5V; V_{PD}=2.9V; V_{PD}+ V_{CC}
Power Down			10	μA	V_{CC}=3.5V; V_{PD} ≤ 0.9V

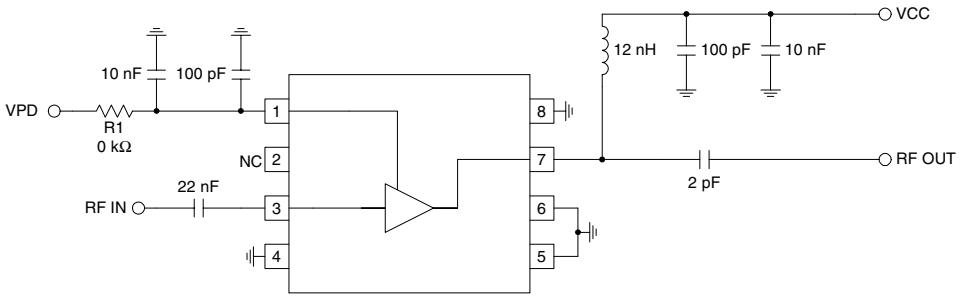
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Pin	Function	Description	Interface Schematic
1	PD	For low noise amplifier applications, this pin is used to control the bias current. See plots for bias current settings. For driver amplifier applications, this is the Power Down pin for the IC. V_{PD} =2.8V +/- 0.1V is required for proper operation. V_{PD}< 0.9V turns off the Part. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Nominal current required for V_{PD}=2.8V is 2.0mA typical and 3.0mA Max (@ V_{PD}=2.9V).	
2	NC	No connection. This pin is typically left unconnected or grounded.	
3	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 836MHz.	
4	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	NC	See pin 2. This pin is typically grounded.	
6	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 7 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
8	GND2	See pin 6.	

Application Schematic
Low Noise Amplifier ~880 MHz Operation



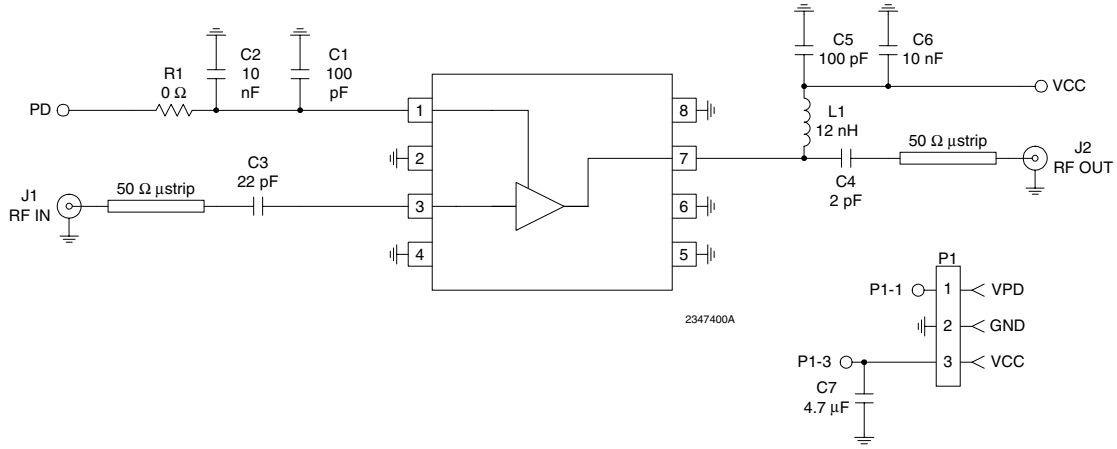
Application Schematic
Driver Amplifier ~836 MHz Operation



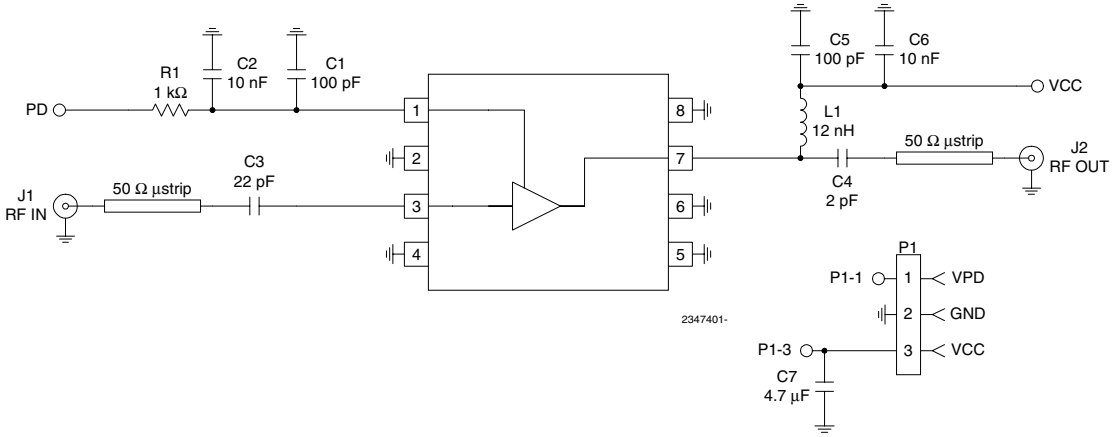
Db00.bk Page 167 Thursday, January 6, 2000 6:50 PM

Evaluation Board Schematic
Driver Amplifier Operation

(Download Bill of Materials from www.rfmd.com.)

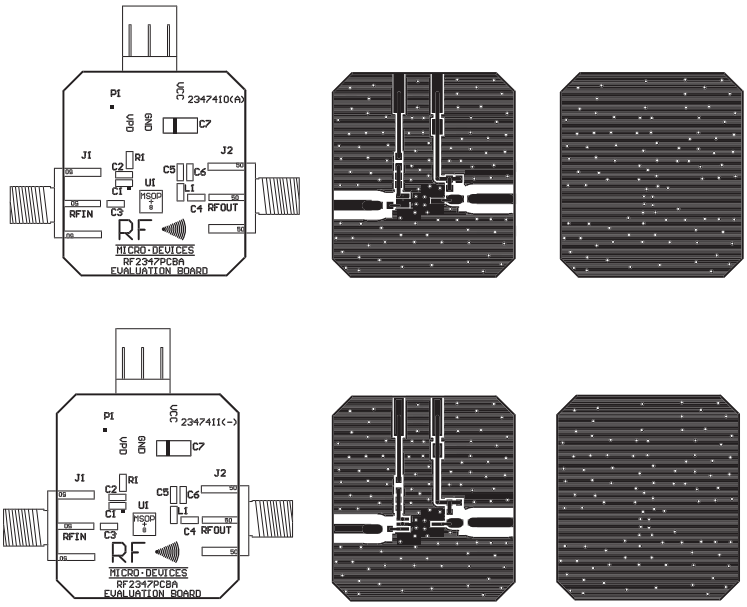


Evaluation Board Schematic
Low Noise Amplifier Operation

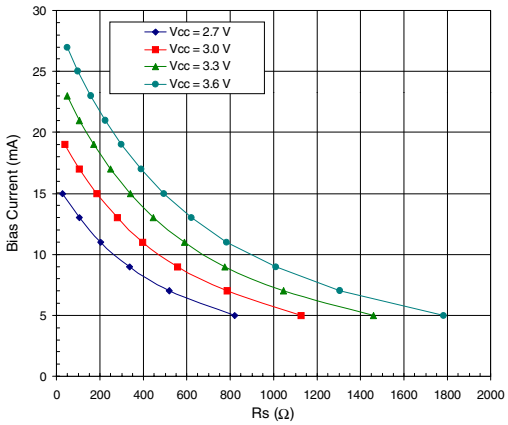


Evaluation Board Layout
Board Size 1.0" x 1.0"

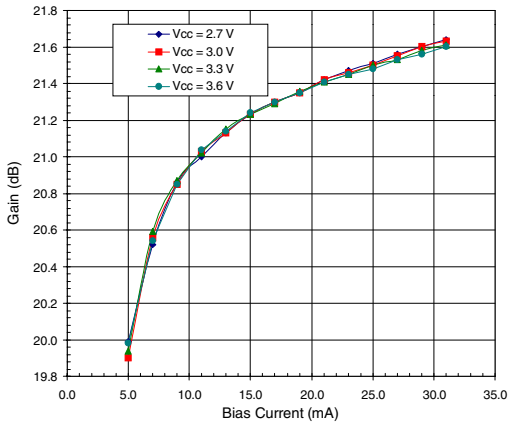
Board Thickness 0.031"; Board Material FR-4



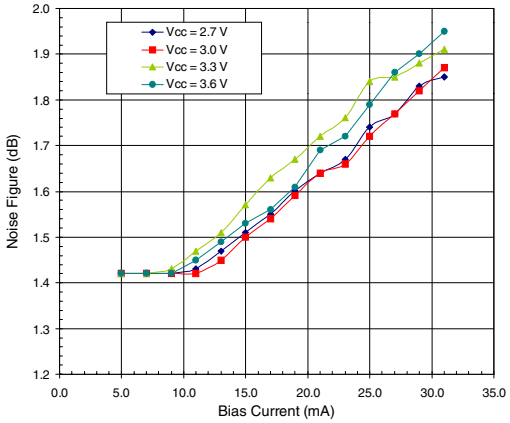
RF2347 Bias Current versus Rc



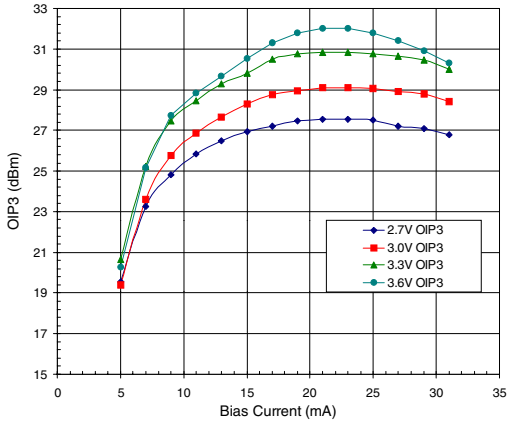
RF2347 Gain versus Bias Current



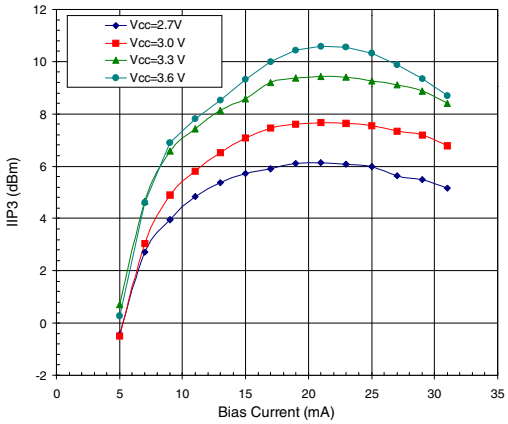
RF2347 Noise Figure versus Bias Current



RF2347 OIP3 versus Bias Current



RF2347 IIP3 versus Bias Current



4

GENERAL PURPOSE AMPLIFIERS

RF2347

RF MICRO·DEVICES

Preliminary

RF2351

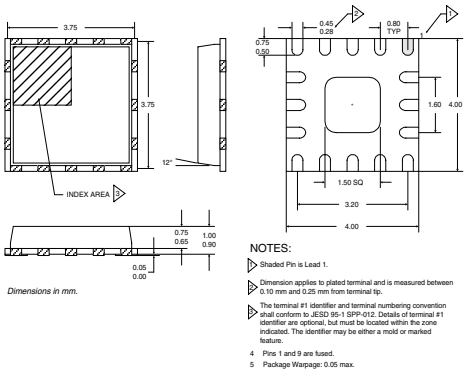
3V PCS CDMA SPLIT BAND PA DRIVER

Typical Applications

- CDMA PCS Systems
- TDMA PCS Systems
- GSM Systems
- Wireless Local Loop Systems
- Wideband CDMA Systems

Product Description

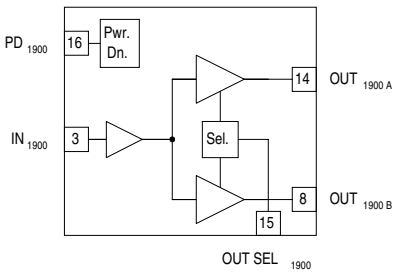
The RF2351 is a broadband linear gain amplifier that was designed specifically for digital communications systems. It is suitable for use in CDMA or TDMA systems in the PCS band. Operating supply voltage ranges from 3V to 6V. Bias optimization may be achieved by adjusting the power down voltage. The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process and is featured in an MLF16 package.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MLF16



Functional Block Diagram

Features

- +16dBm OP1dB at 3.5V
- Single 3V to 6V Supply
- 21dB Gain
- 2.5dB Noise Figure
- Band Selection

Ordering Information

RF2351	3V PCS CDMA Split Band PA Driver
RF2351 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

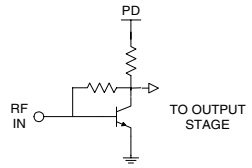
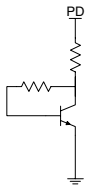
Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Power Down Voltage	0 to +3.1	V_{DC}
DC Current	100	mA
Output Load VSWR	12:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

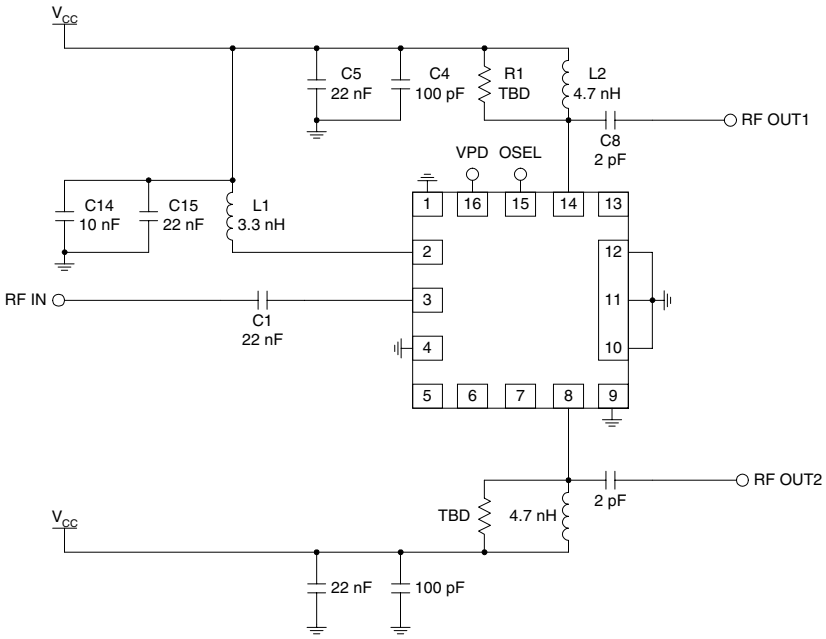
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=3.5, T=25°C
RF Frequency Range		1710 to 1910		MHz	
Small Signal Gain	18	21	24	dB	Freq=1880MHz, V_{CC} = 3.5V, V_{PD} = 2.8V
Noise Figure		2.5		dB	Freq=1880MHz
Output P_{1dB}	+16			dBm	Freq=1880 MHz, V_{CC}=3.5V
Isolation Between Outputs		30		dB	
Input VSWR		1.5:1			In 50Ω system
Output VSWR		1.5:1			In 50Ω system
Adjacent Channel Power Rejection @ 1.25 MHz	-56	-60		dBc	IS-95A CDMA, P_{OUT}=+10dBm
Power Supply					T=25°C
Supply Voltage	3	3.5	6	V	
Power Down Voltage High	2.7	2.8	2.9	V	
Power Down Voltage Low			1.0		
Output Select Voltage High		2	3.5		
Output Select Voltage Low		0	0.4		
DC Current Consumption	30	48	55	mA	V_{CC}=3.5V, V_{PD}=2.8V
V_{PD} Current		8		mA	V_{PD}=2.8V
Power Down Current			10	µA	V_{PD}<1V
Turn On/Off Time			100	nS	

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Pin	Function	Description	Interface Schematic
1	GND3	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	VCC1	Preamplifier output. This pin must be biased to V_{CC} through a matching inductor. Refer to application schematic.	
3	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 1880MHz.	
4	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	NC	No connection. This pin is typically left unconnected or grounded.	
6	NC	No connection. This pin is typically left unconnected or grounded.	
7	NC	No connection. This pin is typically left unconnected or grounded.	
8	RF OUT2	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 7 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
9	GND3	See pin 1.	
10	GND3	See pin 1.	
11	GND3	See pin 1.	
12	GND3	See pin 1.	
13	NC	No connection. This pin is typically left unconnected or grounded.	
14	RF OUT1	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 7 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
15	OSEL	2V to 3.5V range selects RF OUT2; 0V to 0.4V range selects RF OUT1.	
16	VPD	Power Down for the IC. $V_{PD} = 2.8V \pm 0.1V$ turns on the Part. $V_{PD} < 0.9V$ turns off the Part. External RF bypassing is required. Nominal current required for $V_{PD} = 2.8V$ is 8.5 mA typical.	
Pkg Base			

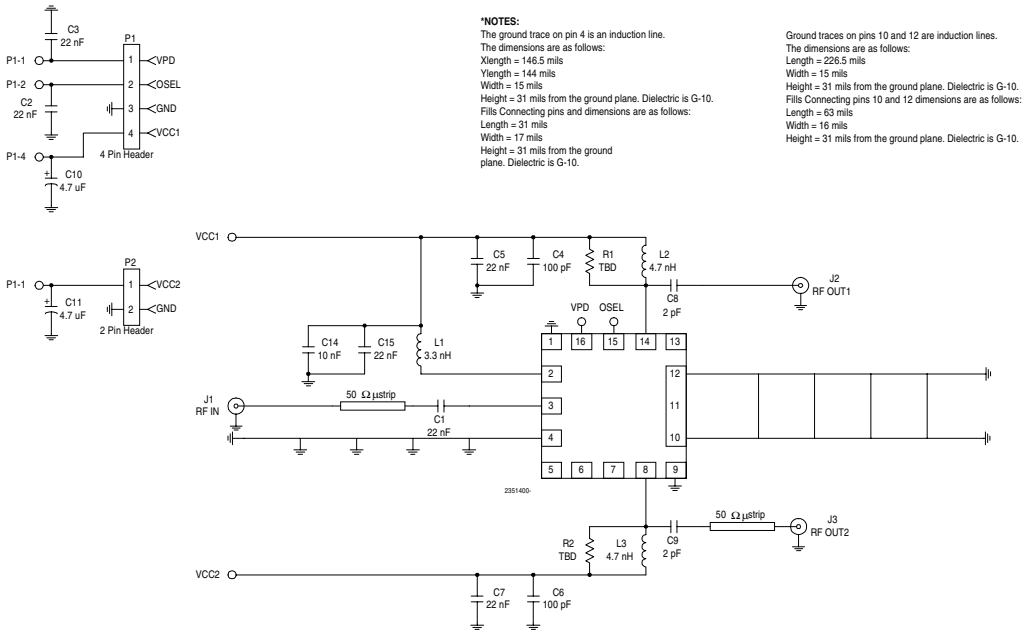
Application Schematic



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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



***NOTES:**

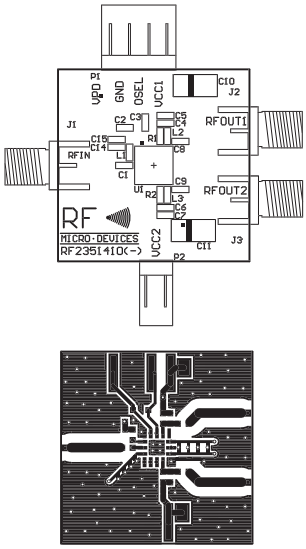
The ground trace on pin 4 is an induction line.
The dimensions are as follows:
Xlength = 146.5 mils
Ylength = 144 mils
Width = 15 mils
Height = 31 mils from the ground plane. Dielectric is G-10.
Fills Connecting pins and dimensions are as follows:
Length = 31 mils
Width = 17 mils
Height = 31 mils from the ground plane. Dielectric is G-10.

Ground traces on pins 10 and 12 are induction lines.
The dimensions are as follows:
Length = 226.5 mils
Width = 15 mils
Height = 31 mils from the ground plane. Dielectric is G-10.
Fills Connecting pins 10 and 12 dimensions are as follows:
Length = 63 mils
Width = 16 mils
Height = 31 mils from the ground plane. Dielectric is G-10.

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Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.031", Board Material FR-4



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RF2352

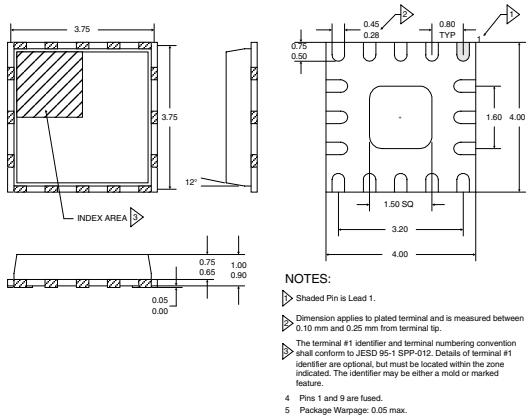
3V CDMA DRIVER AMPLIFIER

Typical Applications

- TDMA/CDMA/FM Driver Amplifier
- Low Noise Transmit Driver Amplifier
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

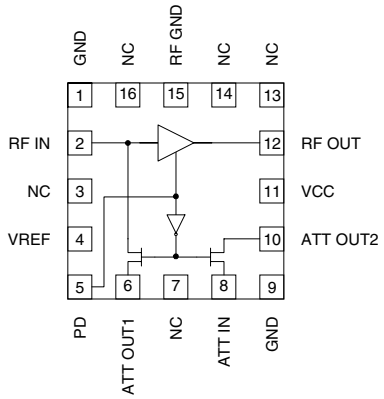
The RF2352 is a low noise driver amplifier for 900MHz CDMA/AMPS applications. The device is designed for operation from 2.7V to 3.6V, and features selectable high and low gain modes. In high gain mode, the device will provide about 19dB of gain, and the linearity and current drain are set with an external resistor, allowing the designer to select the optimum performance for a given application. In the low gain, or "bypass" mode, the gain is controlled by an external attenuator network, and the device draws essentially no current. The part is fabricated using a high performance silicon BiCMOS process, and is packaged in a 4mmx4mm leadless plastic package.



Package Style: MLF16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Low Noise and High Intercept Point
- Power Down Control
- Gain Control
- Single 2.7V to 3.6V Power Supply
- Extremely Small MLF16 Package

Ordering Information

RF2352	3V CDMA Driver Amplifier
RF2352 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

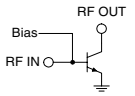
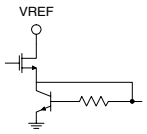
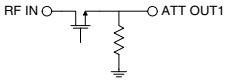
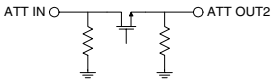
Parameter	Rating	Unit
Supply Voltage	-0.5 to +4.5	V_{DC}
Input RF Level	0	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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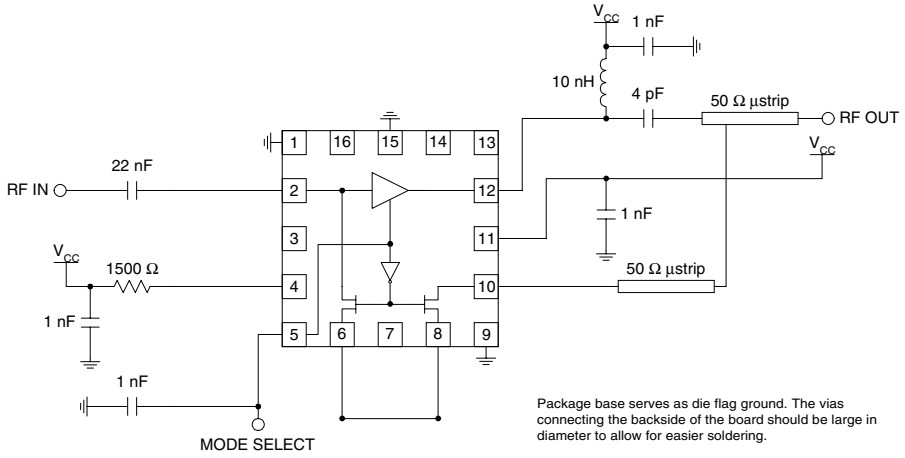
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=3.0V, T=25°C, External Matching Components Required.
High Gain Mode					V_{PD}=2.8V, P_{OUT}=+4dBm, I_{CC}=15mA
Gain	18	20	22	dB	At 824MHz
Noise Figure		1.9	2.9	dB	
Input VSWR		1.3	1.5		
Output VSWR		1.6	1.8		
Adjacent Channel Power Rejection (ACPR1)	57	60		dBc	900kHz offset
Alternate Channel Power Rejection (ACPR2)	78	80		dBc	1.98MHz offset
Gain	17	19	21	dB	At 874MHz
Noise Figure		2.0	3.0	dB	
Input VSWR		1.6	1.8		
Output VSWR		1.5	1.7		
Adjacent Channel Power Rejection (ACPR1)	58	60		dBc	900kHz offset
Alternate Channel Power Rejection (ACPR2)	76	77		dBc	1.98MHz offset
Gain	16.5	18.5	20.5	dB	At 925MHz
Noise Figure		2.2	3.2	dB	
Input VSWR		1.8	2.0		
Output VSWR		1.4	1.6		
Adjacent Channel Power Rejection (ACPR1)	57	60		dBc	900kHz offset
Alternate Channel Power Rejection (ACPR2)	76	77		dBc	1.98MHz offset
Bypass (Low Gain) Mode					V_{PD}=0V, Pins 6 and 8 shorted.
Gain		-4.2		dB	At 824MHz
Noise Figure		4.2		dB	
Input VSWR		1.2	1.4		
Output VSWR		1.4	1.6		
Gain		-3.7		dB	At 874MHz
Noise Figure		3.7		dB	
Input VSWR		1.4	1.6		
Output VSWR		1.3	1.5		
Gain		-4.7		dB	At 925MHz
Noise Figure		4.7		dB	
Input VSWR		1.5	1.7		
Output VSWR		1.4	1.6		
Power Supply					
Power Supply Range (V_{CC})	2.7	3.0	3.6	V	
Current Drain (I_{CC})		15.0		mA	V_{PD}=2.8V (High Gain Mode)
Current Drain (I_{CC})			10	µA	V_{PD}=0V (Bypass Mode)

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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	RF IN	RF input pin. It is DC coupled and looks like 50Ω from 824MHz to 925MHz.	
3	NC	Not connected.	
4	VREF	Provides the bias voltage for controlling the RF amplifier current drain. This pin is typically connected through a resistor to an external regulated power supply. It may be connected to the same power supply as the VCC pin. However, if more bias control is desired, it may be connected to a separate supply. With a series external resistor of 1500Ω and power supply of 3V applied, the amplifier current drain should be around 14mA. By increasing the resistor, the amplifier current drain may be dropped. Conversely, by decreasing the resistor, the amplifier current may be increased to a maximum of 30mA.	
5	PD	Power down function. When 0V to 0.5V is applied, the device is in Bypass Mode: the amplifier is shut off and the MOSFET switches are activated. There is no DC current dissipation in this state. When 1.5V to 3V is applied, the device is switched to High Gain Mode: the amplifier is activated and the MOSFET switches are opened. This is the normal operating mode.	
6	ATT OUT1	Output of the first MOSFET switch. DC coupled. When the PD pin is grounded (Bypass Mode), the MOSFET switches are shorted, sending any signals at the RF IN pin through the first MOSFET and off the chip. In cases where minimum RF attenuation is desired, this pin should be shorted with 50Ω microstrip to the ATT IN pin. This setup will yield approximately 4dB of insertion loss. If more attenuation is desired, a resistive pad between the ATT OUT1 and ATT IN pins can be added to the PC board.	
7	NC	Not connected.	
8	ATT IN	Input to the second MOSFET switch. DC coupled. When the PD pin is grounded (Bypass Mode), the MOSFET switches are shorted. See the ATT OUT1 pin description for setup options.	
9	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
10	ATT OUT2	Output of the second MOSFET switch. DC coupled. When the PD pin is grounded (Bypass Mode), the MOSFET switches are shorted. This pin should be shorted with 50Ω microstrip to the amplifier load.	
11	VCC	Provides the power supply to the logic circuitry on the IC.	
12	RF OUT	Amplifier output pin. An open collector output that needs VCC applied to it through an inductor. Typically, a shunt inductor, series capacitor matching network is used to provide a 50Ω output match.	
13	NC	Not connected.	
14	NC	Not connected.	
15	RF GND	Amplifier ground. Keep traces physically short and connect immediately to ground plane for best performance.	
16	NC	Not connected.	
Pkg Base	GND	Ground connection for die flag. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

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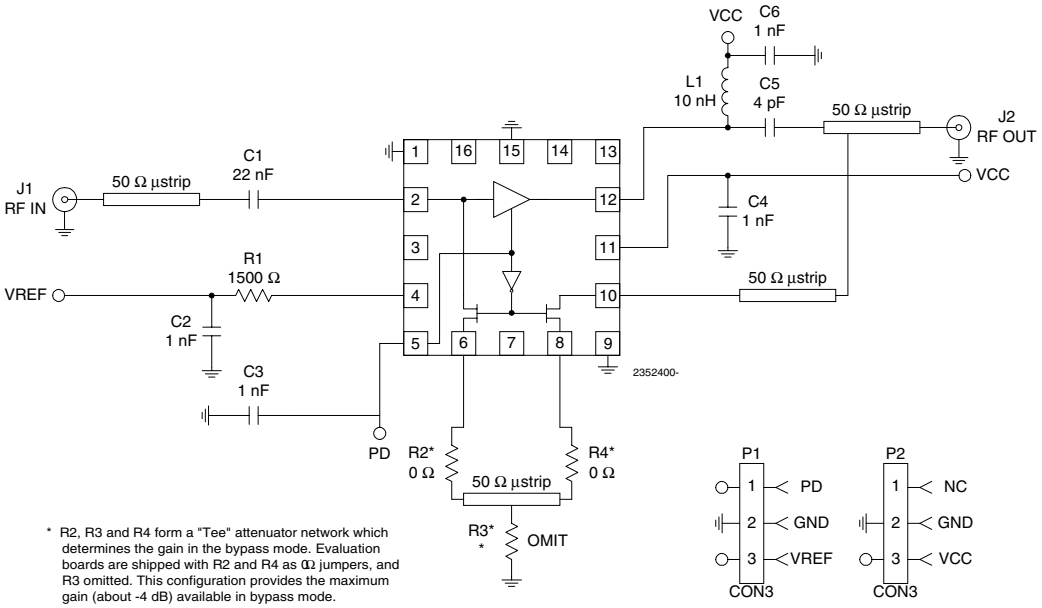
Application Schematic



Package base serves as die flag ground. The vias connecting the backside of the board should be large in diameter to allow for easier soldering.

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



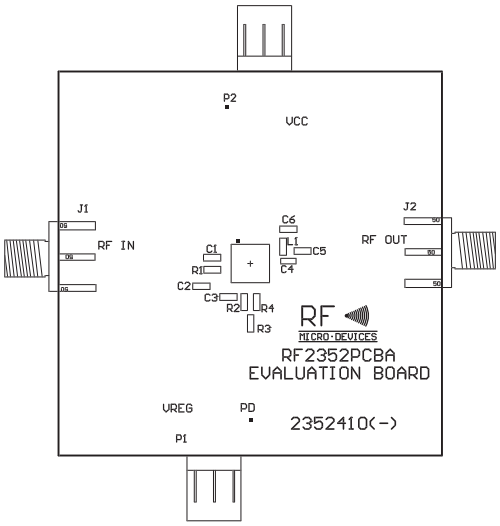
* R2, R3 and R4 form a "Tee" attenuator network which determines the gain in the bypass mode. Evaluation boards are shipped with R2 and R4 as 0Ω jumpers, and R3 omitted. This configuration provides the maximum gain (about -4 dB) available in bypass mode.

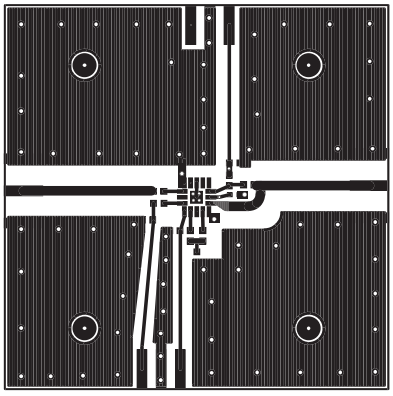
Package base serves as die flag ground. The vias connecting the backside of the board should be large in diameter to allow for easier soldering.

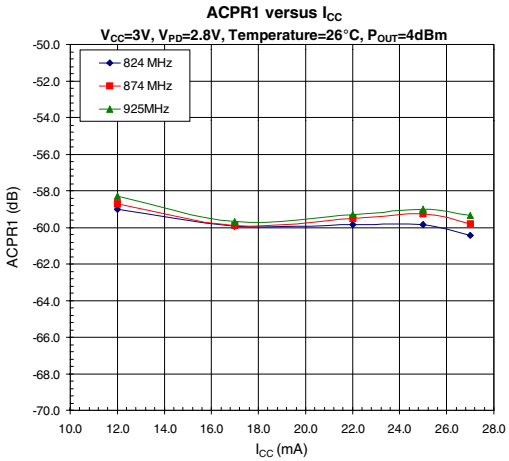
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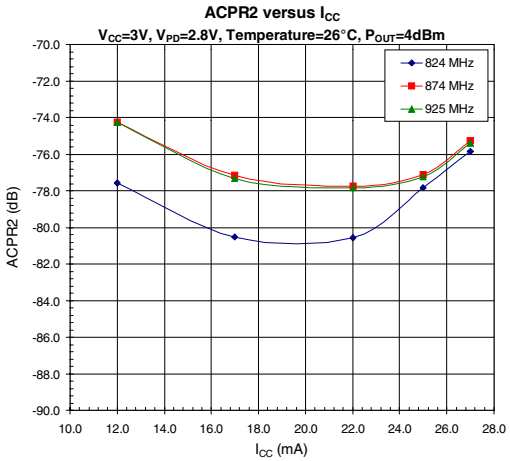
Evaluation Board Layout
Board Size 2.0" x 2.0"

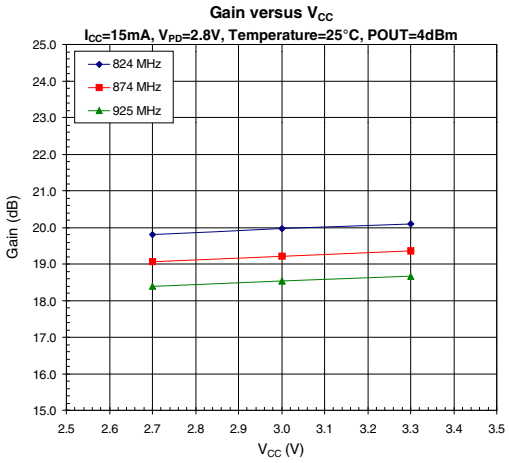
Board Thickness 0.031”; Board Material FR-4






ACPR1 versus I_{CC}
V_{CC}=3V, V_{PD}=2.8V, Temperature=26°C, P_{OUT}=4dBm
824 MHz
874 MHz
925MHz
ACPR1 (dB)
I_{CC} (mA)


ACPR2 versus I_{CC}
V_{CC}=3V, V_{PD}=2.8V, Temperature=26°C, P_{OUT}=4dBm
824 MHz
874 MHz
925 MHz
ACPR2 (dB)
I_{CC} (mA)


Gain versus V_{CC}
I_{CC}=15mA, V_{PD}=2.8V, Temperature=25°C, POUT=4dBm
824 MHz
874 MHz
925 MHz
Gain (dB)
V_{CC} (V)

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RF2361

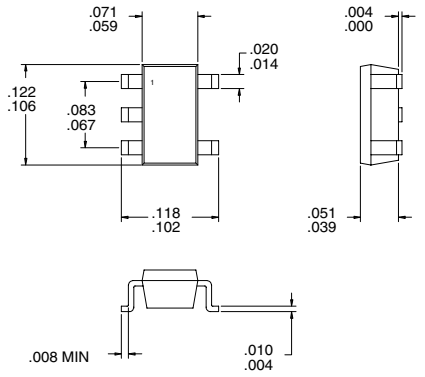
3V LOW NOISE AMPLIFIER/ 3V PA DRIVER AMPLIFIER

Typical Applications

- TDMA/CDMA/FM Cellular PCS LNA
- Low Noise Transmit Driver Amplifier
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

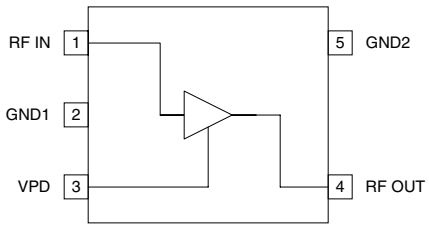
The RF2361 is a low noise amplifier with a very high dynamic range designed for digital cellular applications. The device functions as an outstanding front end low noise amplifier or power amplifier driver amplifier in the transmit chain of digital subscriber units where low transmit noise power is a concern. When used as an LNA, the bias current can be set externally. When used as a PA driver, the IC can operate directly from a single cell Li-ion battery and includes a power down feature that can be used to completely turn off the device. The IC is featured in a standard SOT23-5 plastic package.



Package Style: SOT23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Low Noise and High Intercept Point
- Adjustable Bias Current
- Power Down Control
- Single 2.5V to 6.0V Power Supply
- 150MHz to 2500MHz Operation
- Extremely Small SOT23-5 Package

Ordering Information

RF2361	3V Low Noise Amplifier/ 3V PA Driver Amplifier
RF2361 PCBA-D	Fully Assembled Evaluation Board (Driver)
RF2361 PCBA-L	Fully Assembled Evaluation Board (LNA)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2361

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

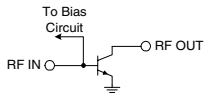
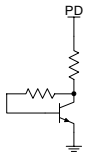
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		150 to 2500		MHz	
Low Noise Amplifier 881MHz Performance					Schematic per LNA Application; T=25°C, RF=881MHz, V_{PD}=2.8V, R1=1kΩ
Gain	19.5	20		dB	V_{CC}=3.0V, I_{CC}=7.6mA
	19.5	20		dB	V_{CC}=2.7V, I_{CC}=7.5mA
Noise Figure		1.4	1.6	dB	V_{CC}=3.0V, I_{CC}=7.6mA
		1.4	1.6	dB	V_{CC}=2.7V, I_{CC}=7.5mA
Input IP3		+6.0		dBm	V_{CC}=3.0V, I_{CC}=7.6mA
		+5.5		dBm	V_{CC}=2.7V, I_{CC}=7.5mA
Low Noise Amplifier 1950MHz Performance					Schematic per LNA Application; T=25°C, RF=1950MHz, V_{PD}=2.8V, R1=1kΩ
Gain	12.5	13		dB	V_{CC}=3.0V, I_{CC}=6.4mA
	12.5	13		dB	V_{CC}=2.7V, I_{CC}=6.3mA
Noise Figure		1.3	1.5	dB	V_{CC}=3.0V, I_{CC}=6.4mA
		1.3	1.5	dB	V_{CC}=2.7V, I_{CC}=6.3mA
Input IP3		+16.5		dBm	V_{CC}=3.0V, I_{CC}=6.4mA
		+16.0		dBm	V_{CC}=2.7V, I_{CC}=6.3mA
Driver Amplifier 836MHz Performance					Schematic per Driver Amplifier Application; T=25°C, RF=836MHz, V_{PD}=2.8V
Gain	19.5	20.5	21.5	dB	V_{CC}=3.5V
	19.5	20.5	21.5	dB	V_{CC}=3.0V
	19.5	20.5	21.5	dB	V_{CC}=2.7V
Output IP3	25	+32.0	35	dBm	V_{CC}=3.5V
		+29.0		dBm	V_{CC}=3.0V
		+27.8		dBm	V_{CC}=2.7V
Noise Figure		1.9	2.0	dB	V_{CC}=3.5V
		1.85	2.0	dB	V_{CC}=3.0V
		1.8	2.0	dB	V_{CC}=2.7V
Reverse Isolation		25		dB	V_{CC}=3.5V
		25		dB	V_{CC}=3.0V
		25		dB	V_{CC}=2.7V
Input VSWR		1.8:1	2.0:1		
Output VSWR		1.25:1	2.0:1		Using External LC network used on evaluation board.
P_{1dB}	13	14.4		dBm	V_{CC}=3.5V
	12	12.5		dBm	V_{CC}=3.0V
	10.5	11.5		dBm	V_{CC}=2.7V

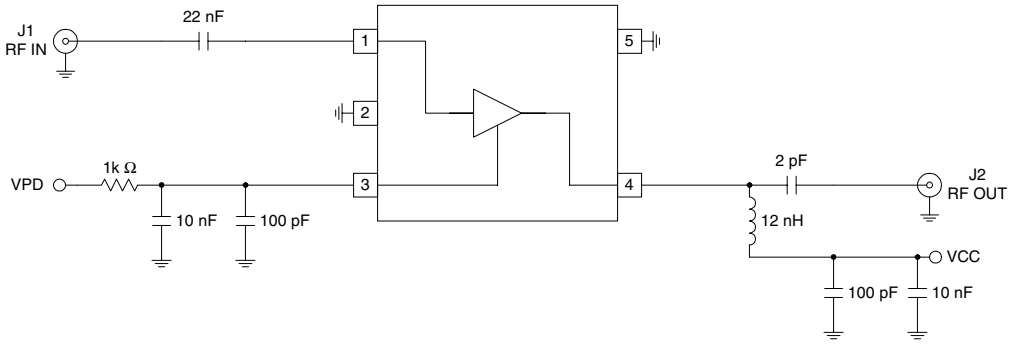
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Power Supply					T=25 °C
Voltage (V_{CC})		2.5 to 6.0		V	
Voltage (V_{PD})	2.7	2.8	2.9	V	
Current Consumption - Driver Amplifier	12.5	21.5	27	mA	V_{CC}=3.5V; V_{PD}=2.8V; V_{PD}+V_{CC} - Current Consumption from V_{PD} is 2.0mA Typ. @ V_{PD}=2.8V and 3.0mA Max @ V_{PD}=2.9V
	18	20	22	mA	V_{CC}=3.5V; V_{PD}=2.7V; V_{PD}+ V_{CC}
	19	23	29	mA	V_{CC}=3.5V; V_{PD}=2.9V; V_{PD}+ V_{CC}
Power Down			10	µA	V_{CC}=3.5V; $V_{PD} \leq$ 0.9V
Driver Amplifier 1880MHz Performance					Schematic per Driver Amplifier Application; T=25°C, RF=1880MHz, V_{PD}=2.8V
Gain	13.0	14.0	14.5	dB	V_{CC}=3.5V
	13.0	14.0	14.5	dB	V_{CC}=3.0V
	13.0	14.0	14.5	dB	V_{CC}=2.7V
Output IP3	27	+35.0	38	dBm	V_{CC}=3.5V
		+31.0		dBm	V_{CC}=3.0V
		+28.8		dBm	V_{CC}=2.7V
Noise Figure		1.85	2.0	dB	V_{CC}=3.5V
		1.8	2.0	dB	V_{CC}=3.0V
		1.75	2.0	dB	V_{CC}=2.7V
Reverse Isolation		19		dB	V_{CC}=3.5V
		19		dB	V_{CC}=3.0V
		19		dB	V_{CC}=2.7V
Input VSWR		1.6:1	2.0:1		
Output VSWR		1.6:1	2.0:1		Using External LC network used on evaluation board.
P_{1dB}	14	15.6		dBm	V_{CC}=3.5V
	13	14.1		dBm	V_{CC}=3.0V
	12	13.1		dBm	V_{CC}=2.7V
Power Supply					T=25 °C
Voltage (V_{CC})		2.5 to 6.0		V	
Voltage (V_{PD})	2.7	2.8	2.9	V	
Current Consumption - Driver Amplifier	11.5	19.5	25.5	mA	V_{CC}=3.5V; V_{PD}=2.8V; V_{PD}+V_{CC} - Current Consumption from V_{PD} is 2.0mA Typ.@ V_{PD}=2.8V and 3.0mA Max @ V_{PD}=2.9V
	16	18	20	mA	V_{CC}=3.5V; V_{PD}=2.7V; V_{PD}+ V_{CC}
	18	20.5	27	mA	V_{CC}=3.5V; V_{PD}=2.9V; V_{PD}+ V_{CC}
Power Down			10	µA	V_{CC}=3.5V; $V_{PD} \leq$ 0.9V

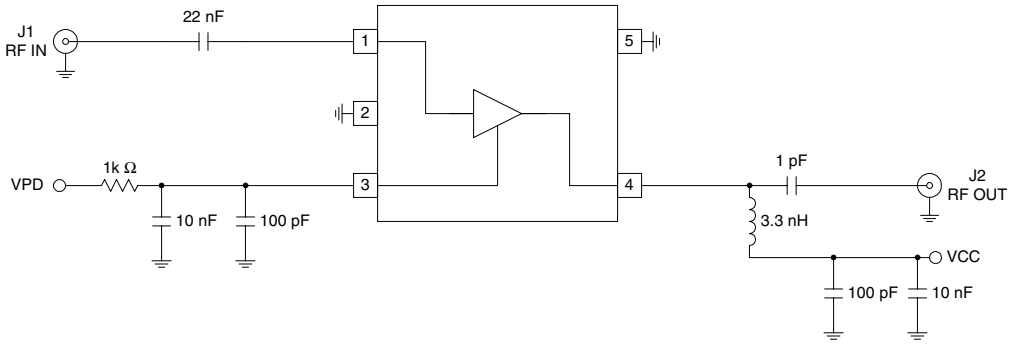
RF2361

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 836 MHz.	
2	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VPD	For low noise amplifier applications, this pin is used to control the bias current. See plots for bias current settings. An external resistor (R1) can be used to set the bias current for any V_{PD} voltage. For driver amplifier applications, this is the Power Down pin for the IC. V_{PD}=2.8V +/- 0.1V is required for proper operation. V_{PD}< 0.9V turns off the Part. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Nominal current required for V_{PD}=2.8V is 2.0mA typical and 3.0mA Max (@ V_{PD}=2.9V).	
4	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 4 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
5	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	

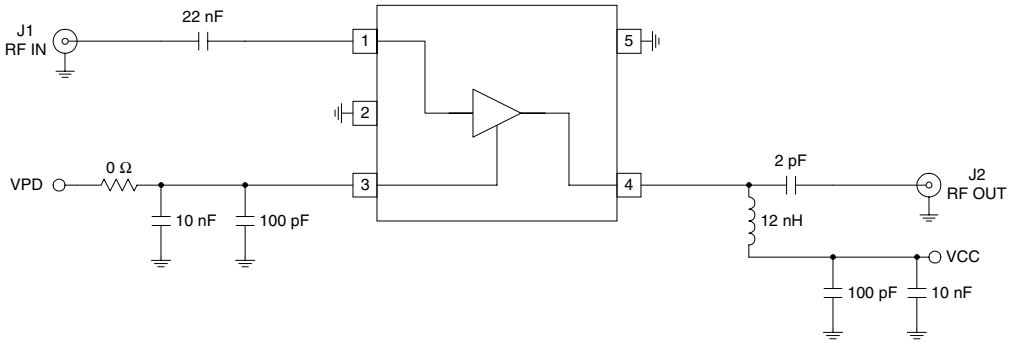
Application Schematic: Low Noise Amplifier ~881MHz Operation



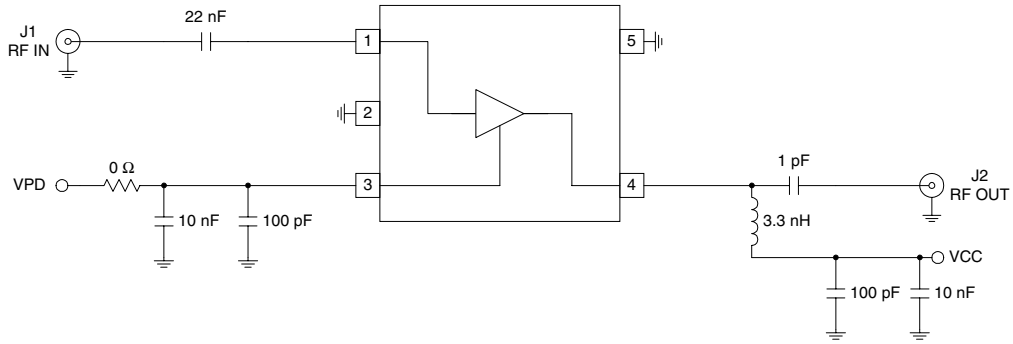
Application Schematic: Low Noise Amplifier ~1950MHz Operation



Application Schematic: Driver Amplifier ~836MHz Operation



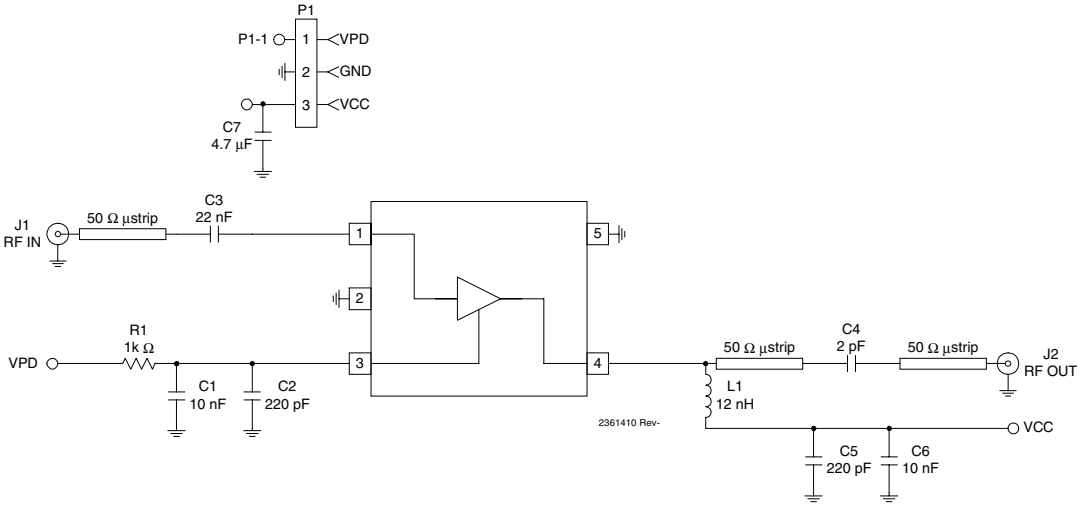
Application Schematic: Driver Amplifier ~1880MHz Operation



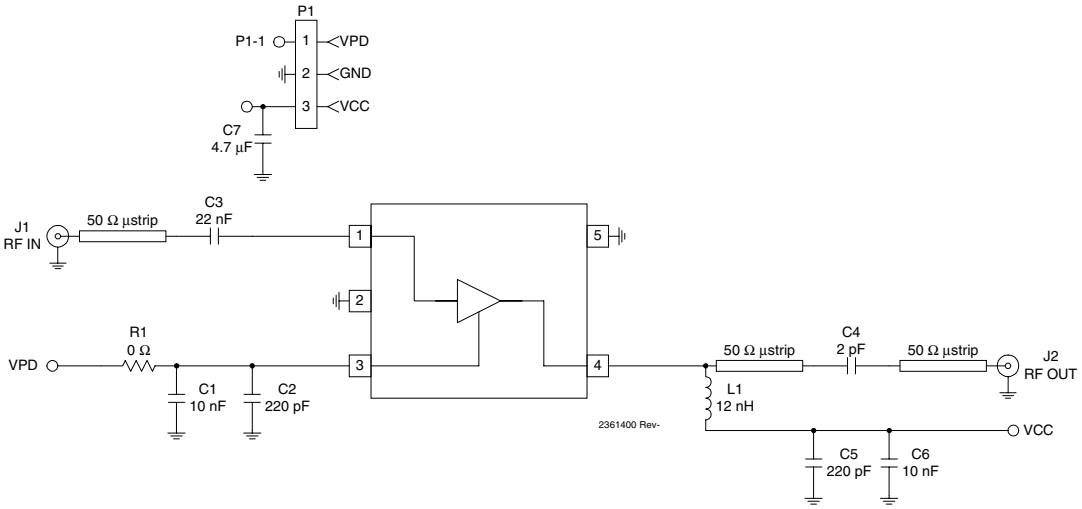
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Evaluation Board Schematic: Low Noise Amplifier ~881MHz Operation

(Download Bill of Materials from www.rfmd.com.)

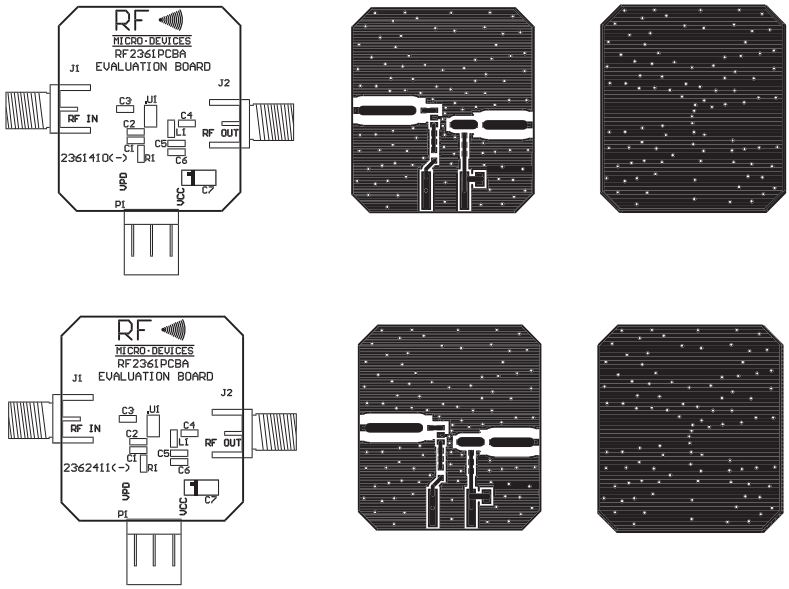


Evaluation Board Schematic: Driver Amplifier ~836MHz Operation

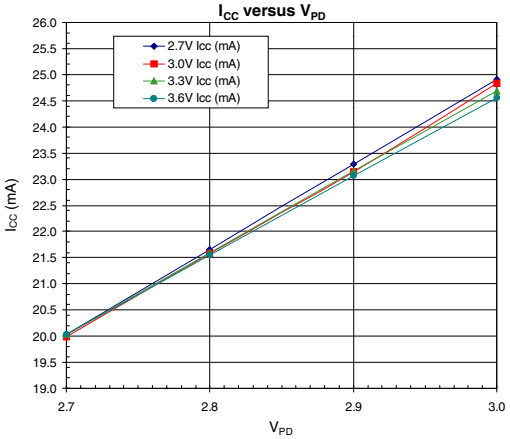


Evaluation Board Layout
Board Size 0.948” x 1.063”

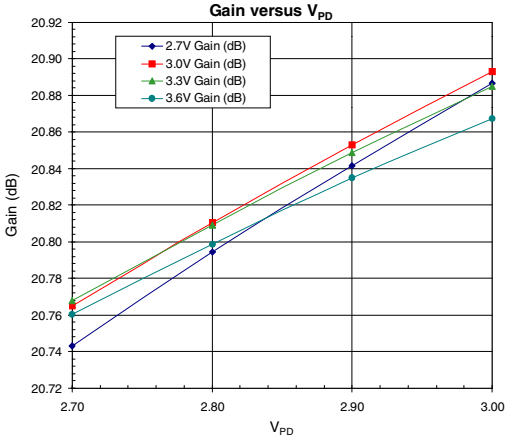
Board Thickness 0.031”; Board Material FR-4



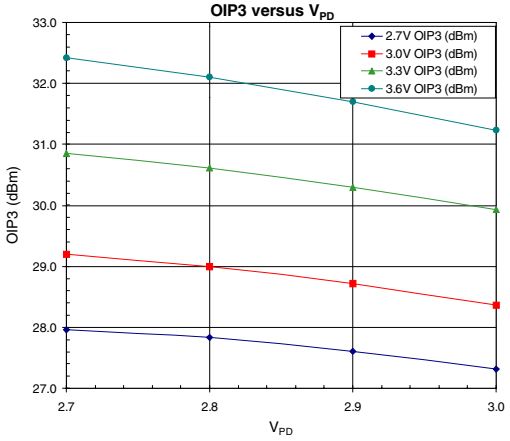
Driver Amp 836 MHz
I_{CC} versus V_{PD}



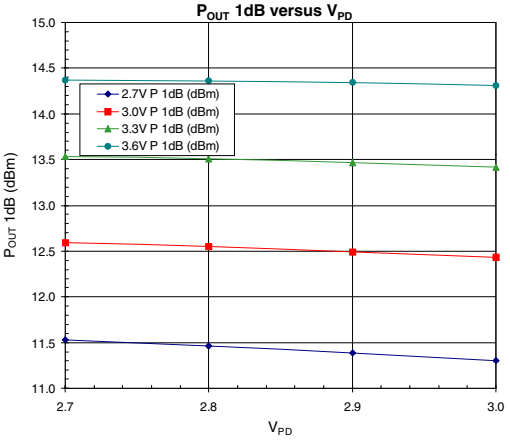
Driver Amp 836 MHz
Gain versus V_{PD}



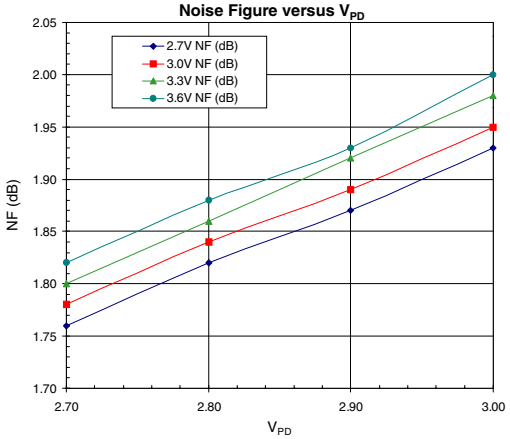
Driver Amp 836 MHz
OIP3 versus V_{PD}



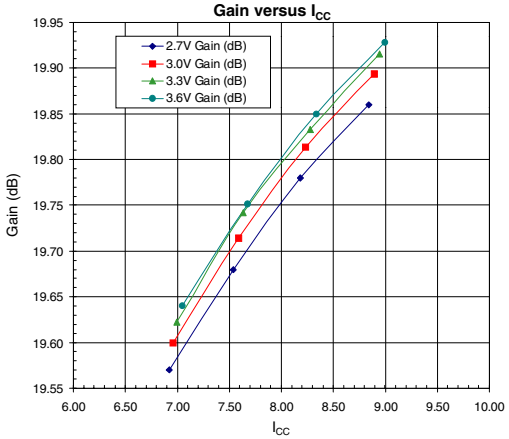
Driver Amp 836 MHz
P_{OUT} 1dB versus V_{PD}



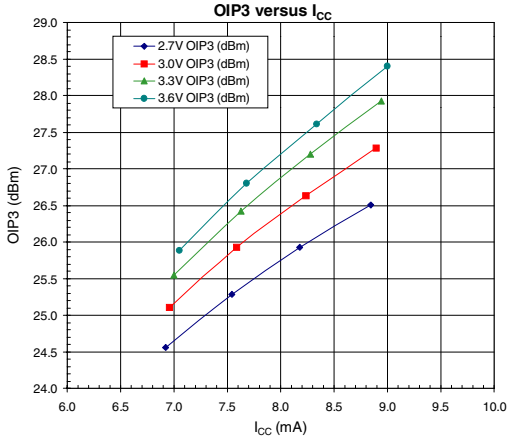
Driver Amp 836 MHz
Noise Figure versus V_{PD}



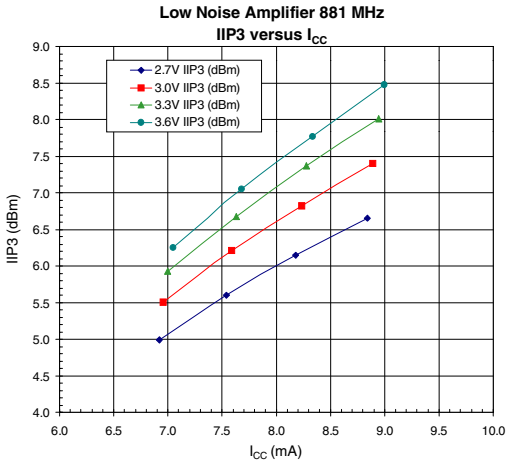
Low Noise Amplifier 881 MHz
Gain versus I_{CC}



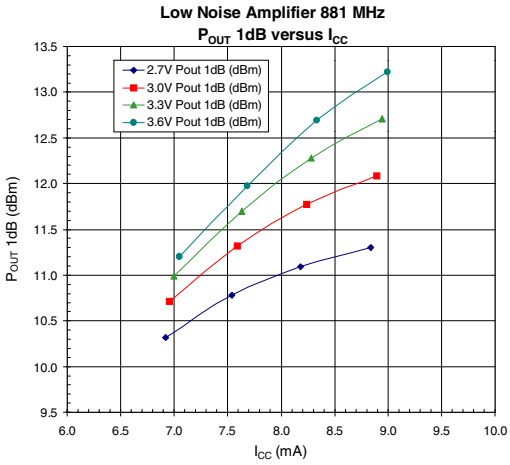
Low Noise Amplifier 881 MHz
OIP3 versus I_{CC}



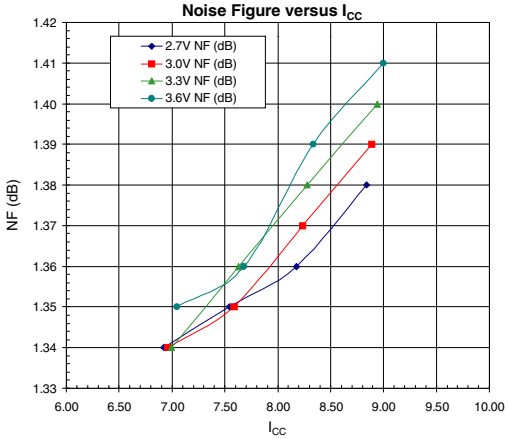
Low Noise Amplifier 881 MHz
IIP3 versus I_{CC}



Low Noise Amplifier 881 MHz
P_{OUT} 1dB versus I_{CC}



Low Noise Amplifier 881 MHz
Noise Figure versus I_{CC}



RF2362

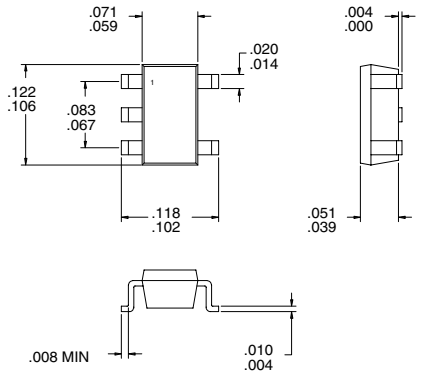
PCS CDMA/TDMA 3V PA DRIVER AMPLIFIER

Typical Applications

- TDMA/CDMA/FM PCS Tx Amplifier
- Low Noise Transmit Driver Amplifier
- 2.4 GHz WLAN Systems
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

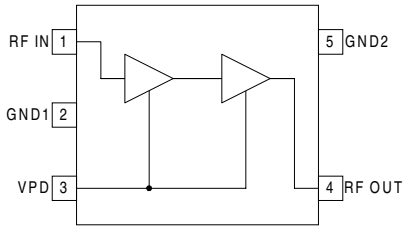
The RF2362 is a low noise CDMA/TDMA PA driver amplifier with a very high dynamic range designed for transmit digital PCS applications at 1880MHz. The device functions as an outstanding PA driver amplifier in the transmit chain of digital subscriber units where low transmit noise power is a concern. The IC includes a power down feature that can be used to completely turn off the device. The IC is featured in a standard SOT23-5 plastic package.



Package Style: SOT23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Low Noise and High Intercept Point
- Adjustable Bias Current
- Power Down Control
- Single 2.5V to 6.0V Power Supply
- 150MHz to 2500MHz Operation
- Extremely Small SOT23-5 Package

Ordering Information

RF2362	PCS CDMA/TDMA 3V PA Driver Amplifier
RF2362 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2362

Absolute Maximum Ratings

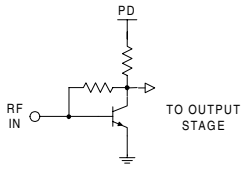
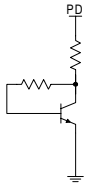
Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

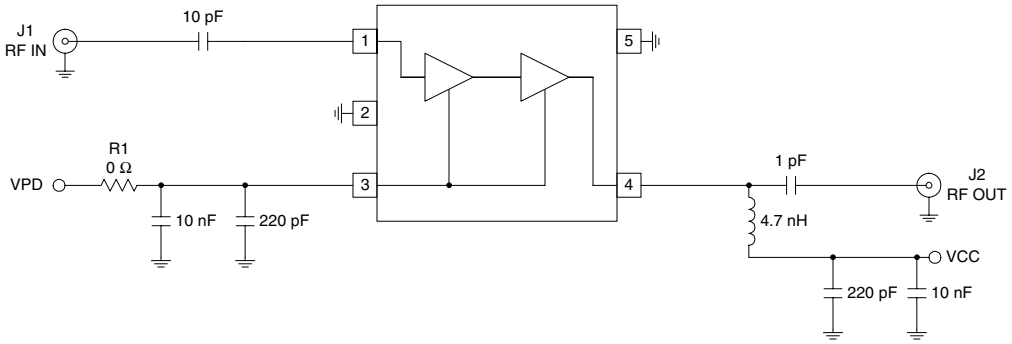
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		150 to 2500		MHz	
1880MHz Performance					Schematic per Evaluation Board, T=25°C, RF=1880MHz, V_{PD}=2.8V
Gain	19	20.1	21.5	dB	V_{CC}=3.5V
	19	20.1	21.5	dB	V_{CC}=3.0V
	19	20.1	21.5	dB	V_{CC}=2.7V
Output IP3	+24	+25.5	+35	dBm	V_{CC}=3.5V
		+25.0		dBm	V_{CC}=3.0V
		+24.5		dBm	V_{CC}=2.7V
Noise Figure		2.2	2.5	dB	V_{CC}=3.5V
		2.2	2.5	dB	V_{CC}=3.0V
		2.2	2.5	dB	V_{CC}=2.7V
Reverse Isolation		32		dB	V_{CC}=3.5V
		32		dB	V_{CC}=3.0V
		32		dB	V_{CC}=2.7V
Input VSWR		1.8:1	2.0:1		
Output VSWR		1.6:1	2.0:1		Using External LC network used on Evaluation Board
P_{1dB}	14	14.5		dBm	V_{CC}=3.5V
	12.5	14		dBm	V_{CC}=3.0V
	11	13.5		dBm	V_{CC}=2.7V
Power Supply					T=25°C
Voltage (V_{CC})		2.5 to 6.0		V	
Voltage (V_{PD})	2.7	2.8	2.9	V	
Current Consumption	24	35	43	mA	V_{CC}=3.5V; V_{PD}=2.8V; V_{PD}+ V_{CC} - Current Consumption from V_{PD} is 8.5 mA Typ. @ V_{PD} = 2.8V and 12 mA Max @ V_{PD} =2.9V
	24	32	38	mA	V_{CC}=3.0V; V_{PD}=2.7V; V_{PD}+ V_{CC}
	29	37	43	mA	V_{CC}=2.7V; V_{PD}=2.9V; V_{PD}+ V_{CC}
- Power Down			10	μA	V_{CC}=3.5V; V_{PD} ≤0.9V

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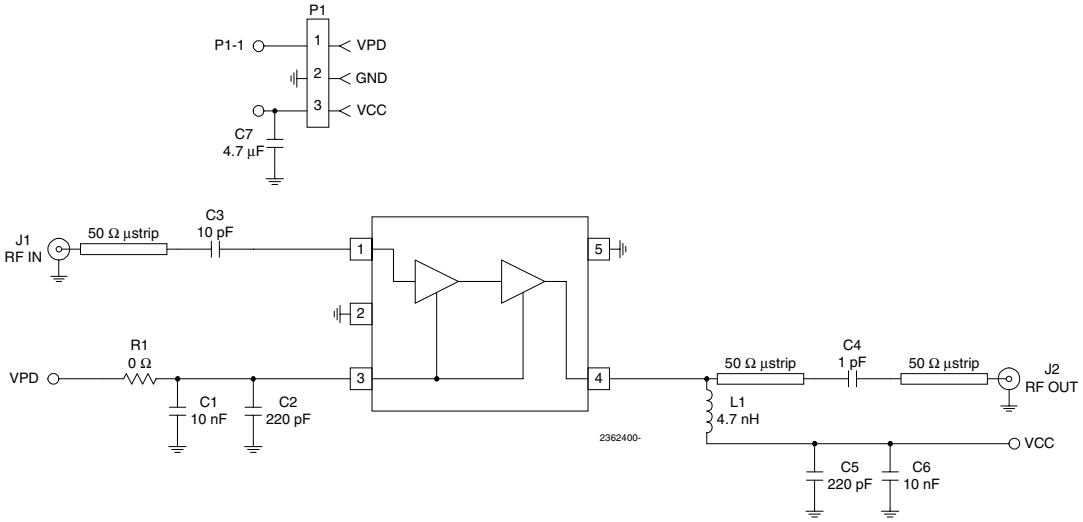
Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 1880MHz.	
2	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VPD	Power Down for the IC. V_{PD} = 2.8V +/- 0.1V turns on the Part. V_{PD} < 0.9V turns off the Part. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Nominal current required for V_{PD} = 2.8V is 8.5 mA typical and 12 mA Max (@ V_{PD} = 2.9 V).	
4	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 4 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
5	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	

Application Schematic: ~1880 MHz Operation, Internal Collector Bias



Evaluation Board Schematic

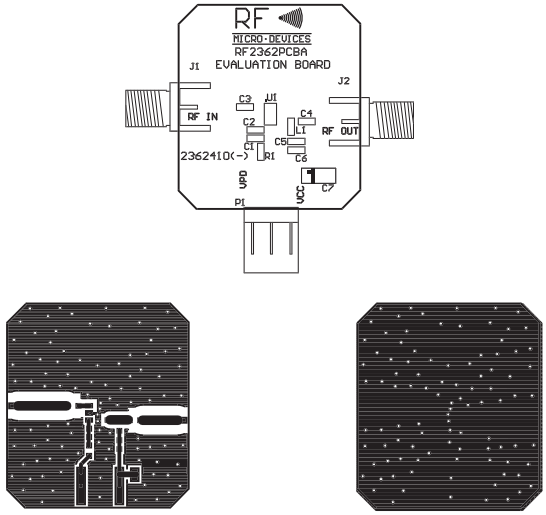
(Download Bill of Materials from www.rfmd.com.)



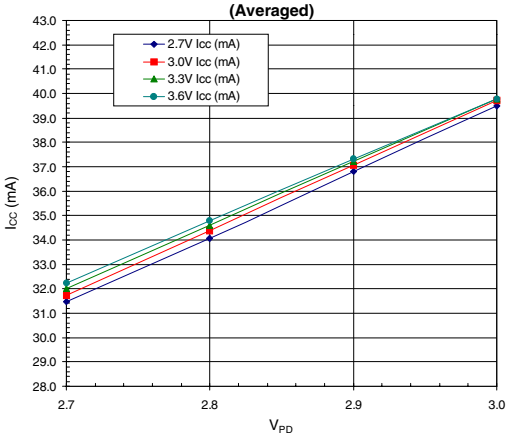
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Evaluation Board Layout
Board Size 1” x 1”

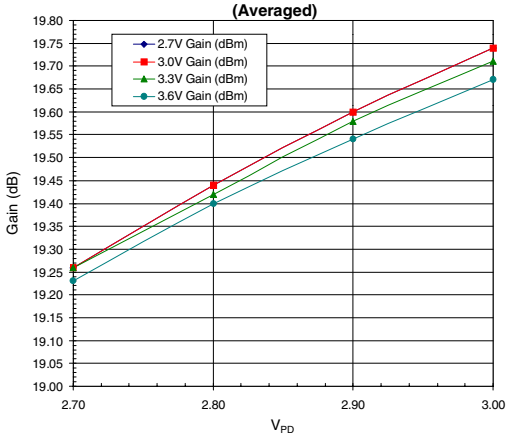
Board Thickness 0.014”; Board Material FR-4



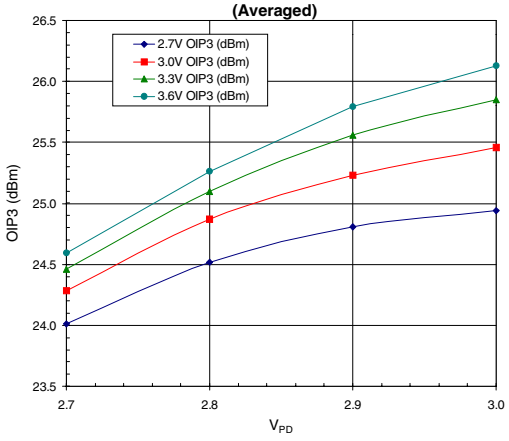
I_{CC} versus V_{PD} (Averaged)



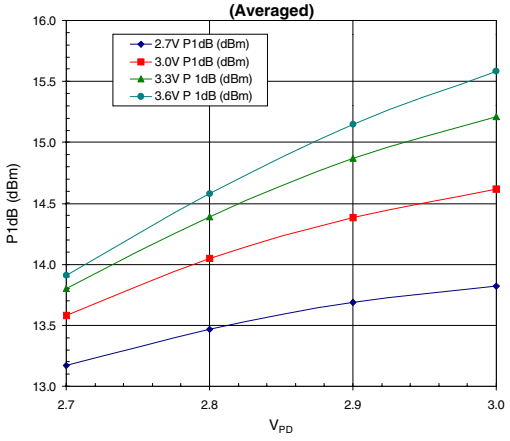
Gain versus V_{PD} (Averaged)



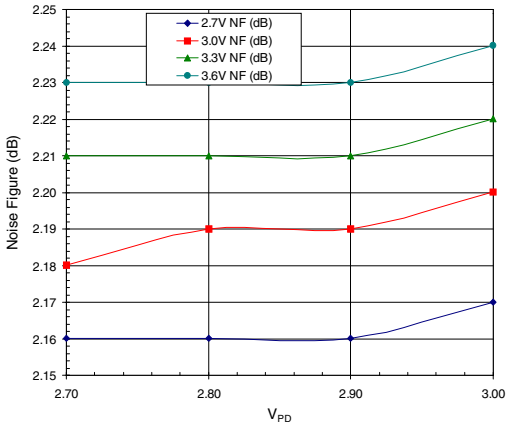
OIP3 versus V_{PD} (Averaged)



P1dB versus V_{PD} (Averaged)



Noise Figure versus V_{PD}



RF MICRO·DEVICES

Preliminary

RF2363

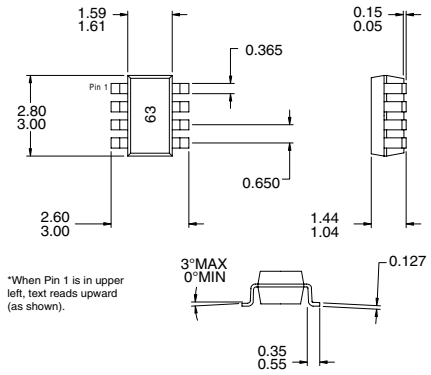
DUAL-BAND 3V LOW NOISE AMPLIFIER

Typical Applications

- GSM/DCS Dual-Band Handsets
- Cellular/PCS Dual-Band Handsets
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

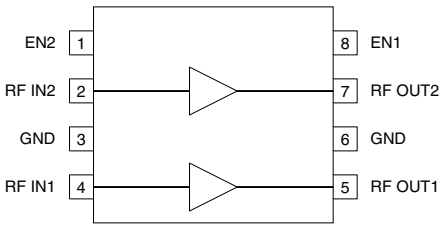
The RF2363 is a dual-band Low Noise Amplifier designed for use as a front-end for 950MHz GSM/1850MHz DCS applications and may be used for dual-band cellular/PCS applications. The 900MHz LNA is a single-stage amplifier; the 1900MHz LNA is a 2-stage amplifier. The part may also be tuned for applications in other frequency bands. The device has an excellent combination of low noise figure and high linearity at a very low supply current. It is packaged in a very small industry standard SOT23 8-lead plastic package.



Package Style: SOT23-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Low Noise and High Intercept Point
- 18dB Gain at 900MHz
- 21dB Gain at 1900MHz
- Low Supply Current
- Single 2.5V to 5.0V Power Supply
- Very Small SOT23-8 Plastic Package

Ordering Information

RF2363	Dual-Band 3V Low Noise Amplifier
RF2363 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

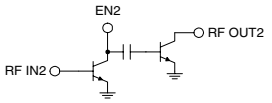
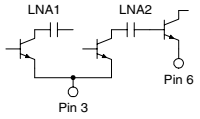
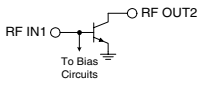
Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		800 to 1000 1800 to 2000		MHz MHz	
950MHz Performance					T=25°C, RF=950MHz, V_{CC}=2.8V, EN1=2.8V, EN2=0V
Gain	16	18	20	dB	
Isolation		16		dB	EN1=0V
Gain Step		34		dB	Gain - Isolation
Noise Figure		1.3		dB	
Output IP3	+18	+24		dBm	
Input P1dB		-10		dBm	
Reverse Isolation		20		dB	
Input VSWR		1.8:1	2:1		No external matching
Output VSWR		1.8:1	2:1		With external match as per GSM/DCS Application Schematic
1850MHz Performance					T=25°C, RF=1850MHz, V_{CC}=2.8V, EN2=2.8V, EN1=0V
Gain	20	21.5	24	dB	
Isolation		10		dB	EN2=0V
Gain Step		31.5		dB	Gain - Isolation
Noise Figure		1.4		dB	
Output IP3	+17	+22		dBm	
Input P1dB		-12		dBm	
Reverse Isolation		30		dB	
Input VSWR		1.7:1	2:1		No external matching
Output VSWR		1.7:1	2:1		With external match as per GSM/DCS Application Schematic
LNA Select					
"Enable" Voltage		V_{CC}		V	
"Disable" Voltage		0		V	
Power Supply					T=25°C
Voltage		2.8		V	Specifications
		2.5 to 5.0		V	Operating limits
Current Consumption		5		mA	900MHz LNA Enabled, 1900MHz LNA Disabled; total DC current
		7.5		mA	1900MHz LNA Enabled, 900MHz LNA Disabled; total DC current
			1	µA	EN1=EN2=0V

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Pin	Function	Description	Interface Schematic
1	EN2	Enable pin for ~1900MHz LNA. A voltage equal to the supply voltage LNA. This pin should be disabled (0V) when the ~900MHz LNA is in use. See package drawing for description of pin orientation.	
2	RF IN2	RF input pin for ~1900MHz. This pin is matched to approximately 50Ω at DCS/PCS frequencies. An external AC coupling capacitor is required at this pin.	
3	GND	Ground connection. NOTE: Ground traces on pins 3 and 6 are equivalent to a small amount of inductance (~0.75nH). The dimensions of these lines are as follows. Pin 3: L=56mils, W=15mils, H=30mils Pin 6: L=56mils, W=15mils, H=30mils Dielectric is FR-4.	
4	RF IN1	RF input pin for ~900MHz. This pin is matched to approximately 50Ω at GSM/Cellular frequencies. An external AC coupling capacitor is required at this pin.	
5	RF OUT1	RF output pin for ~900MHz LNA. This pin is an open-collector output. It must be biased to either V_{CC} or pin 8 through a choke or matching inductor. It is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 4.
6	GND	See pin 3.	See pin 3.
7	RF OUT2	RF output pin for ~1900MHz LNA. This pin is an open-collector output. It must be biased to either V_{CC} or pin 8 through a choke or matching inductor. It is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 2.
8	EN1	Enable pin for ~900MHz LNA. A voltage equal to the supply voltage LNA. This pin should be disabled (0V) when the ~1900MHz LNA is in use.	

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RF2363 Theory of Operation and Application Information

The RF2363 contains two independent low noise amplifiers which have been optimized for dual-band applications in the GSM (905MHz to 960MHz) and DCS (1805MHz to 1880MHz) frequency bands. Fabricated using heterojunction bipolar transistor (HBT) technology, the RF2363 delivers high linear gain at a very low noise figure and low power consumption. Internal temperature compensation keeps the gain tightly controlled over temperature extremes (typically less than 1dB of gain variation from -40°C to +85°C at 2.8V). A 50Ω input impedance allows the part to be connected to standard receiver front end filters without additional matching components.

MODE CONTROL

The RF2363 incorporates two enable pins (EN1 and EN2) for biasing the desired LNA according to the table below.

EN1	EN2	Mode
GND	GND	Power Down
GND	VCC	1900MHz LNA On
VCC	GND	900MHz LNA On

900MHz LNA

The 900MHz LNA is a single-stage, common emitter amplifier. Since the input pin contains a DC bias, an AC coupling capacitor is required at this pin. An external bias inductor from the output pin (RF OUT1) to VCC provides DC biasing for the amplifier transistor and assists in matching the output impedance to the next receiver stage. A capacitor having a good RF bypass characteristic at the frequency of operation should be placed as close as possible to the supply voltage side of the bias inductor; a low frequency bypass capacitor should also be included. The EN1 pin supplies VCC to the bias circuits of the LNA and should also be effectively bypassed with both low and high frequency capacitors.

1900MHz LNA

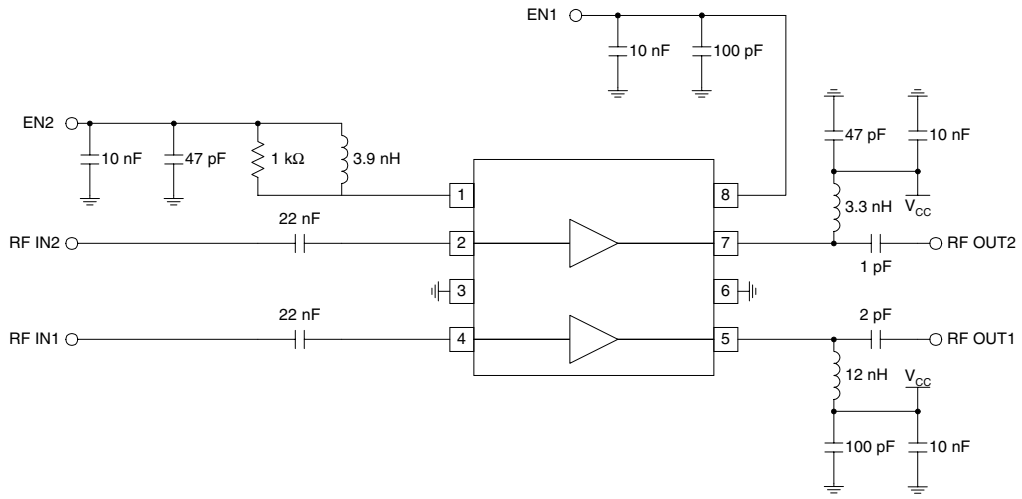
The 1900MHz LNA is implemented by two common emitter stages in cascade. The first stage is biased through an external inductor at the EN2 pin. This inductor also acts as an interstage match; a resistor in parallel with the inductor is recommended to 'de-Q' the inductor, thus providing a broader band interstage match. An external bias inductor from the output pin (RF OUT2) to VCC provides DC biasing for the second stage transistor and assists in matching the output impedance to the next receiver stage. Low and high frequency bypass capacitors should be used on the supply side of both the EN2 and RF OUT2 bias inductors. An AC coupling capacitor is required at the RF IN2 pin.

LAYOUT CONSIDERATIONS

To provide optimal balance of gain and linearity, a small amount of inductance is required in the ground traces of the PCB. The recommended inductance is between 0.5 and 1.0nH, with 0.75nH used on the Evaluation Board. Depending on the application, more gain with less linearity or more linearity with less gain may be desired. Appropriate adjustment of the ground inductance can accomplish these objectives. Minimizing the ground inductance will maximize the gain at the expense of linearity while increasing the ground inductance will increase the linearity at the expense of gain. It is important to remember that the Pin 3 ground inductance affects the performance of both LNAs, while the Pin 6 ground inductance affects only the 1900MHz LNA.

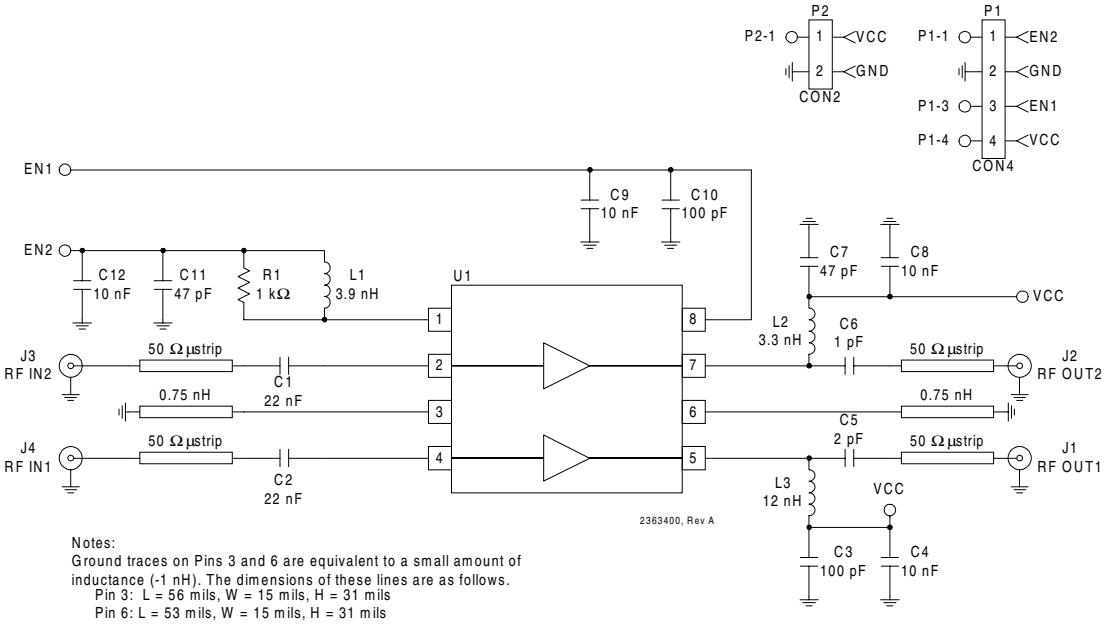
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Application Schematic (GSM/DCS)



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

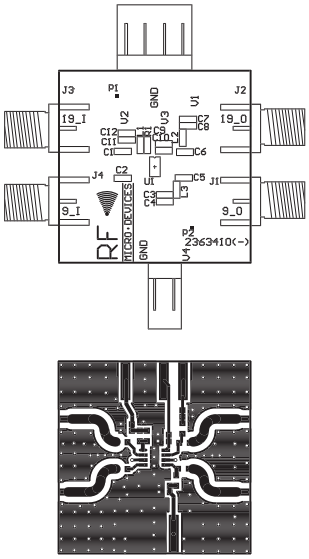


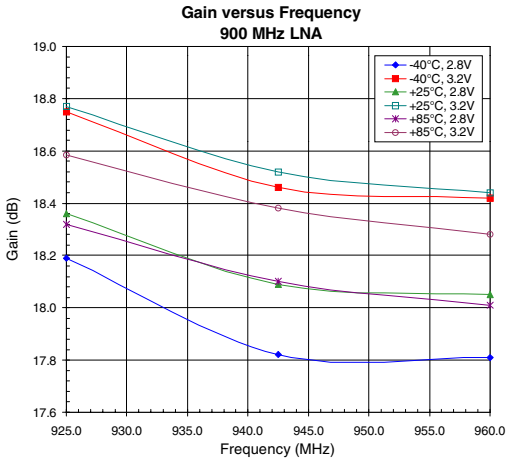
Notes:
Ground traces on Pins 3 and 6 are equivalent to a small amount of inductance (-1 nH). The dimensions of these lines are as follows.
Pin 3: L = 56 mils, W = 15 mils, H = 31 mils
Pin 6: L = 53 mils, W = 15 mils, H = 31 mils
Dielectric is FR-4

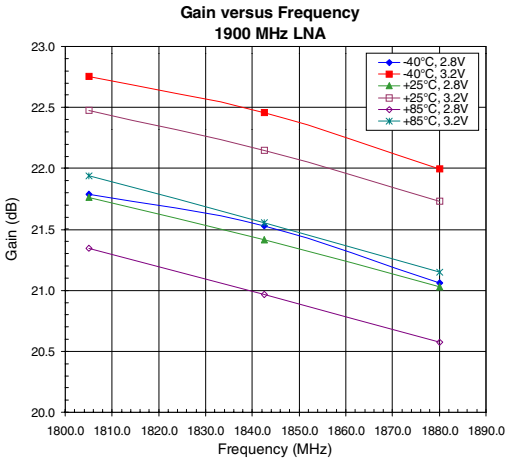
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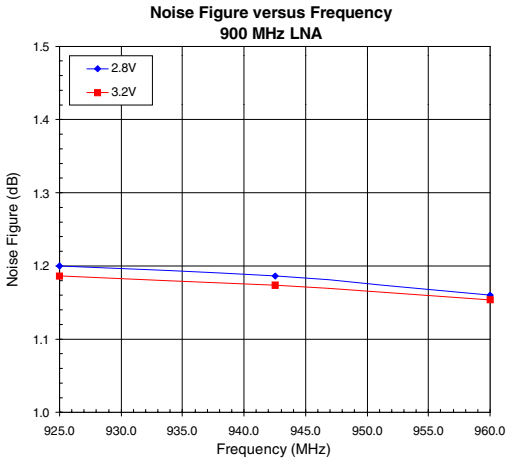
Evaluation Board Layout
Board Size 1.0" x 1.0"

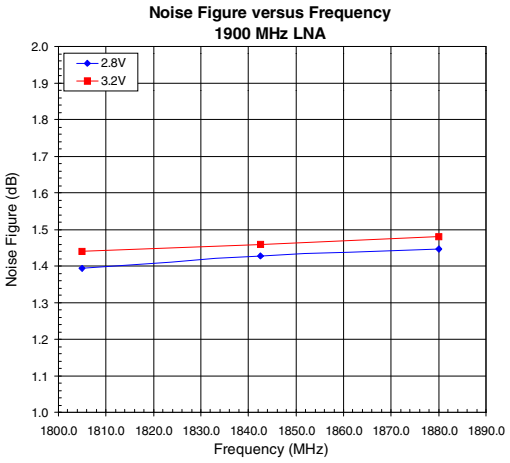
Board Thickness 0.031", Board Material FR-4

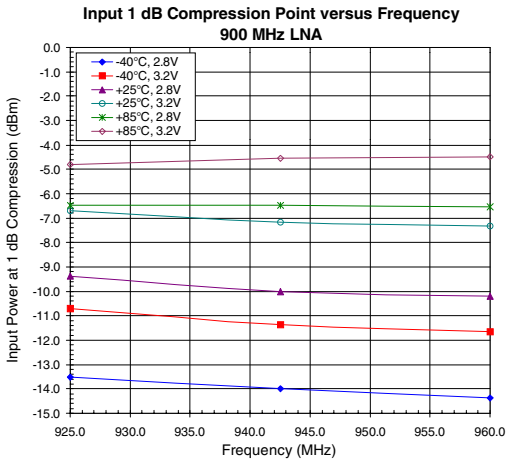


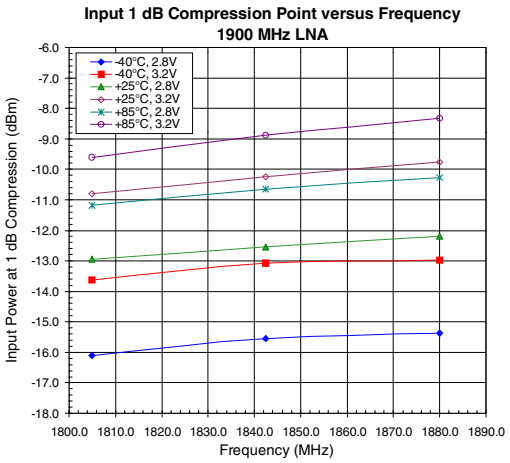

Gain versus Frequency
900 MHz LNA
-40°C, 2.8V
-40°C, 3.2V
+25°C, 2.8V
+25°C, 3.2V
+85°C, 2.8V
+85°C, 3.2V
Gain (dB)
Frequency (MHz)


Gain versus Frequency
1900 MHz LNA
-40°C, 2.8V
-40°C, 3.2V
+25°C, 2.8V
+25°C, 3.2V
+85°C, 2.8V
+85°C, 3.2V
Gain (dB)
Frequency (MHz)

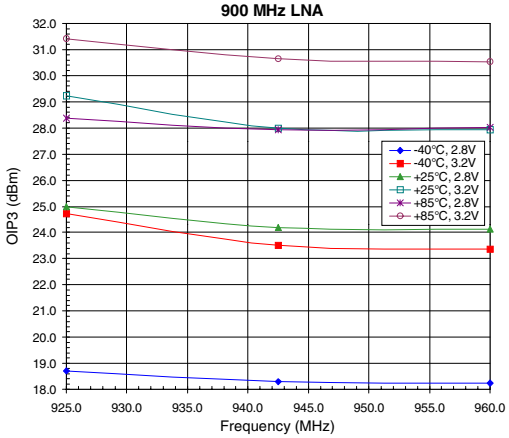

Noise Figure versus Frequency
900 MHz LNA
2.8V
3.2V
Noise Figure (dB)
Frequency (MHz)


Noise Figure versus Frequency
1900 MHz LNA
2.8V
3.2V
Noise Figure (dB)
Frequency (MHz)

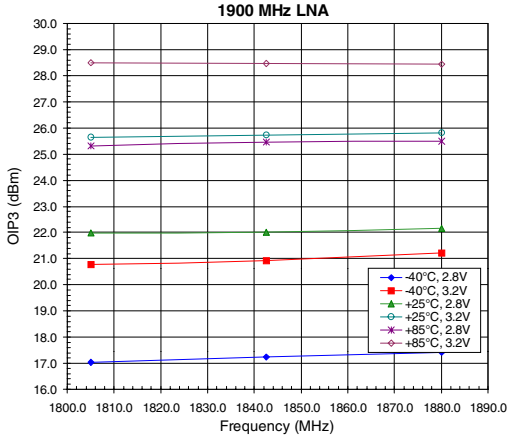

Input 1 dB Compression Point versus Frequency
900 MHz LNA
-40°C, 2.8V
-40°C, 3.2V
+25°C, 2.8V
+25°C, 3.2V
+85°C, 2.8V
+85°C, 3.2V
Input Power at 1 dB Compression (dBm)
Frequency (MHz)


Input 1 dB Compression Point versus Frequency
1900 MHz LNA
-40°C, 2.8V
-40°C, 3.2V
+25°C, 2.8V
+25°C, 3.2V
+85°C, 2.8V
+85°C, 3.2V
Input Power at 1 dB Compression (dBm)
Frequency (MHz)

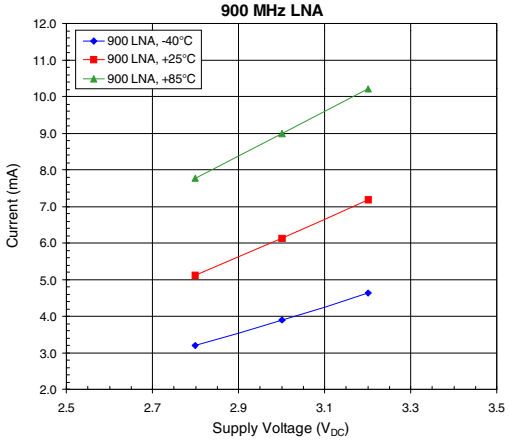
Output 3rd Order Intercept Point versus Frequency
900 MHz LNA



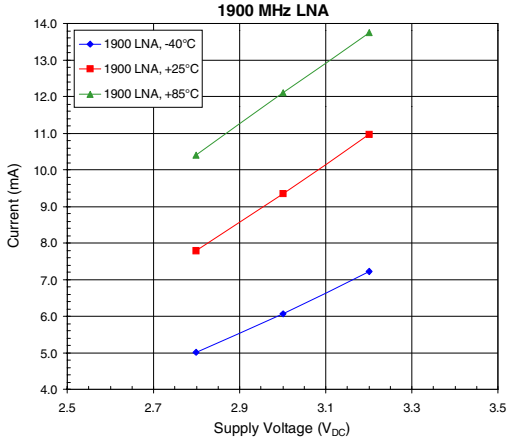
Output 3rd Order Intercept Point versus Frequency
1900 MHz LNA

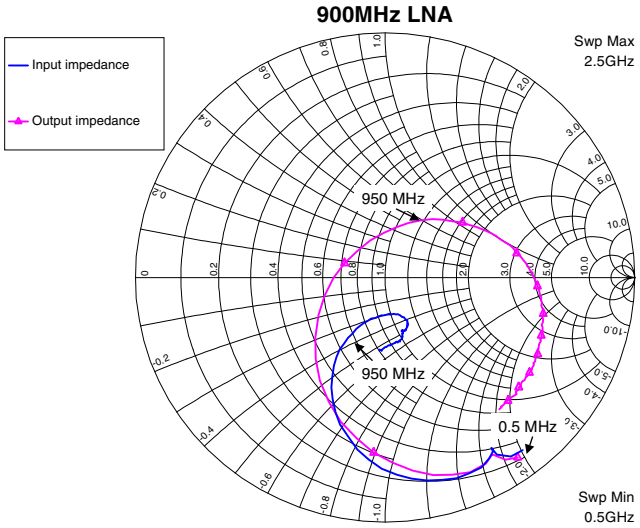


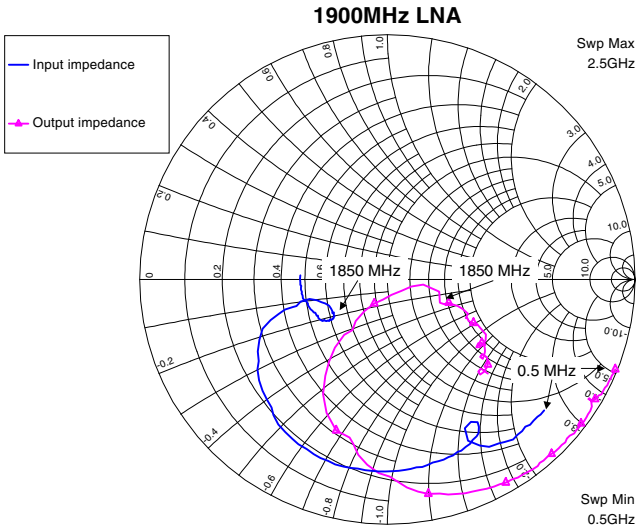
Current versus Supply Voltage
900 MHz LNA



Current versus Supply Voltage
1900 MHz LNA




900MHz LNA
Input impedance
Output impedance
Swp Max
2.5GHz
950 MHz
950 MHz
0.5 MHz
Swp Min
0.5GHz


1900MHz LNA
Input impedance
Output impedance
Swp Max
2.5GHz
1850 MHz
1850 MHz
0.5 MHz
Swp Min
0.5GHz

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Preliminary

RF2364

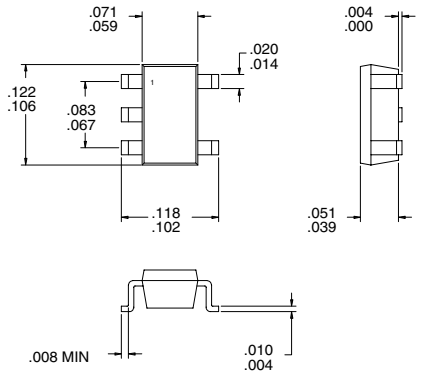
3V PCS LOW NOISE AMPLIFIER

Typical Applications

- CDMA PCS LNA
- TDMA PCS LNA
- WCDMA/CDMA2000 LNA
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

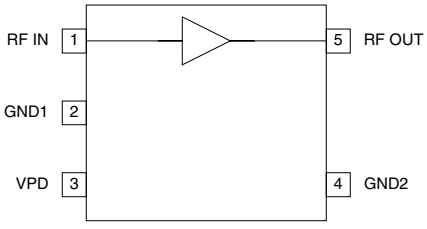
The RF2364 is a low noise amplifier with a high dynamic range designed for CDMA and TDMA PCS, as well as WCDMA/CDMA2000 applications. The device functions as an outstanding front end low noise amplifier and the bias current can be set externally. Includes a power down feature that can be used to completely turn-off the device. The IC is featured in a standard SOT23-5 plastic package.



Package Style: SOT23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Low Noise and High Intercept Point
- 19dB Gain
- Power Down Control
- Single 3.0V Power Supply
- PCS and WCDMA Band Operation
- Extremely Small SOT23-5 Package

Ordering Information

RF2364	3V PCS Low Noise Amplifier
RF2364 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

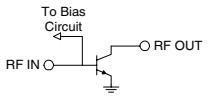
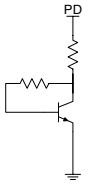
Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

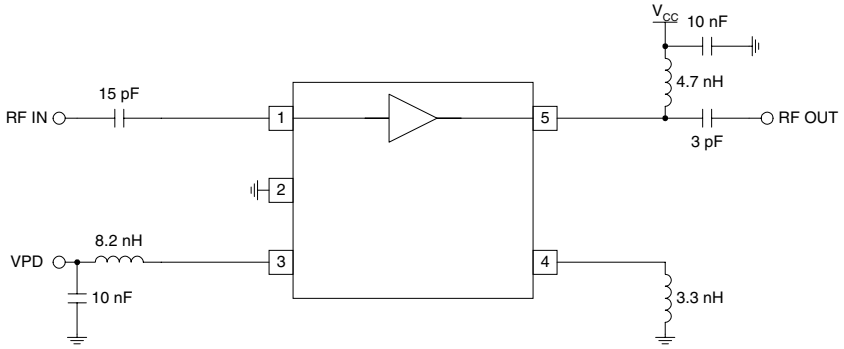
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range	1930		1990	MHz	
Low Noise Amplifier Performance					Schematic per LNA Application T=25°
Power Gain		19	21	dB	V_{CC}=3.0V, I_{CC}=17mA
Noise Figure		1.8		dB	
Input IP3		+5		dBm	V_{CC}=3.0V
Input VSWR			2:1		
Output VSWR			2:1		With external matching components.
Isolation		27		dB	At 1950MHz
Input P1dB		8.5		dBm	
Power Supply					T=25 °C
Voltage (V_{CC})	2.7	3.0	3.3	V	
Current Consumption		17.0	22.5	mA	V_{CC}=3.0V
Power Down			10	µA	V_{CC}=3.0V; $V_{PD} \leq 0.9$ V

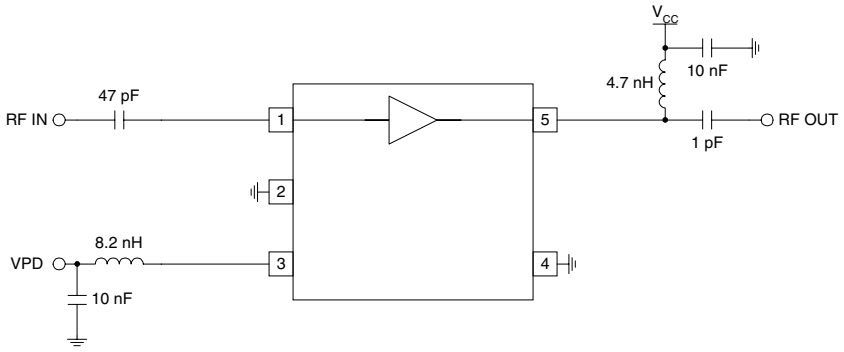
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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω.	
2	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VPD	For low noise amplifier applications, this pin is used to control the bias current. See plots for bias current settings. An external resistor (R1) can be used to set the bias current for any V_{PD} voltage. For driver amplifier applications, this is the Power Down pin for the IC. V_{PD}=2.8V +/- 0.1V is required for proper operation. V_{PD}< 0.9V turns off the Part. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Nominal current required for V_{PD}=2.8V is 2.0mA typical and 3.0mA Max (@ V_{PD}=2.9V).	
4	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 4 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	

Application Schematic PCS Band

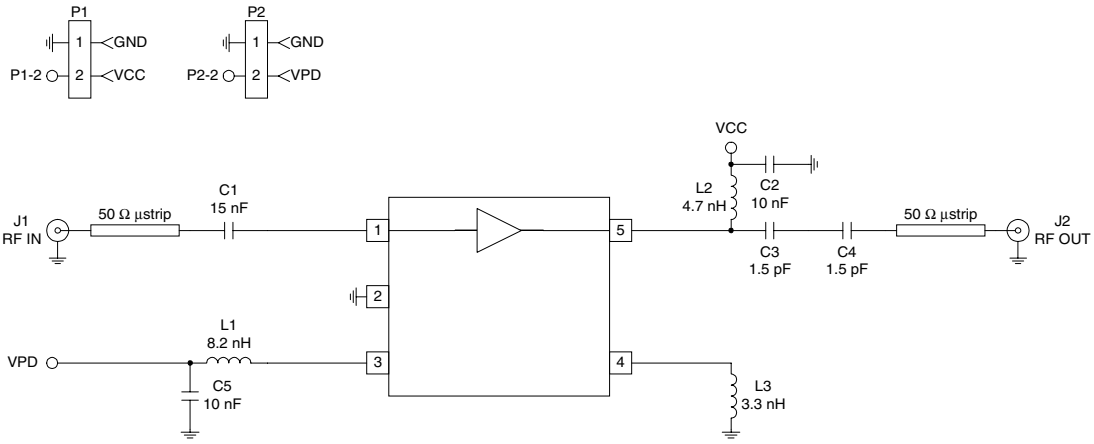


Application Schematic WCDMA Band



Evaluation Board Schematic

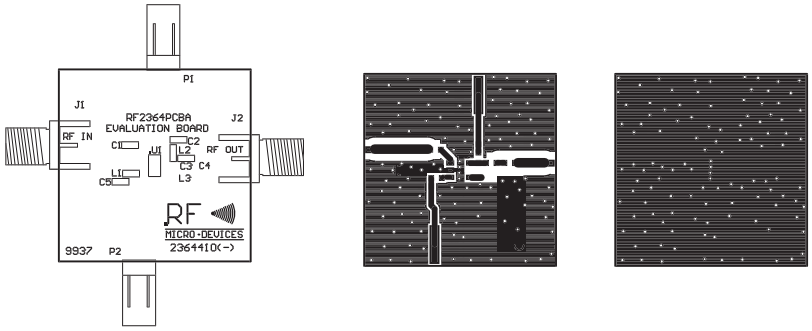
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
Board Size 1” x 1”

Board Thickness 0.031”; Board Material FR-4



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RF MICRO·DEVICES

Preliminary

RF2365

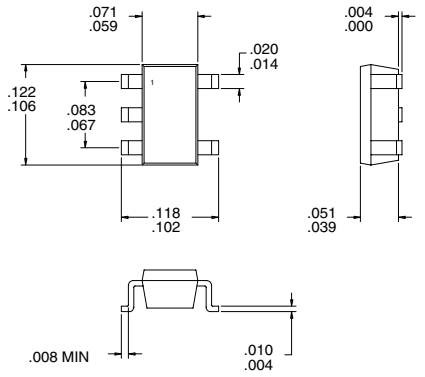
3V LOW NOISE AMPLIFIER

Typical Applications

- DCS GSM
- PCS CDMA
- PCS TDMA
- 2.4GHz Systems
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

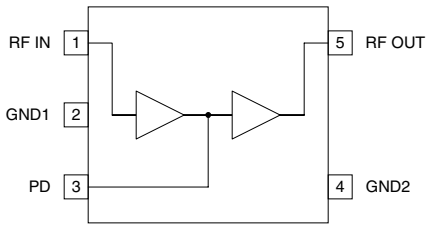
The RF2365 is a low noise amplifier with a high dynamic range designed for the receive front end of digital cellular applications at PCS/DCS frequencies. It is designed to amplify low level signals with minimum noise contribution while operating in the harsh, interference-rich environments of newly deployed digital subscriber units. The part provides excellent performance as a LNA for 2.4GHz radio applications. The IC is featured in a standard SOT23-5 plastic package.



Package Style: SOT23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 1.6dB Noise Figure @ 1850MHz
- 1.75dB Noise Figure @ 2450MHz
- 18.0dB Gain at PCS/DCS
- 15.5dB Gain at 2.45GHz
- External Bias Control
- Extremely Small SOT23-5 Package

Ordering Information

RF2365	3V Low Noise Amplifier
RF2365 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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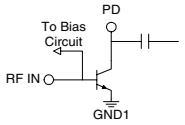
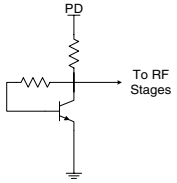
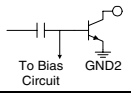
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

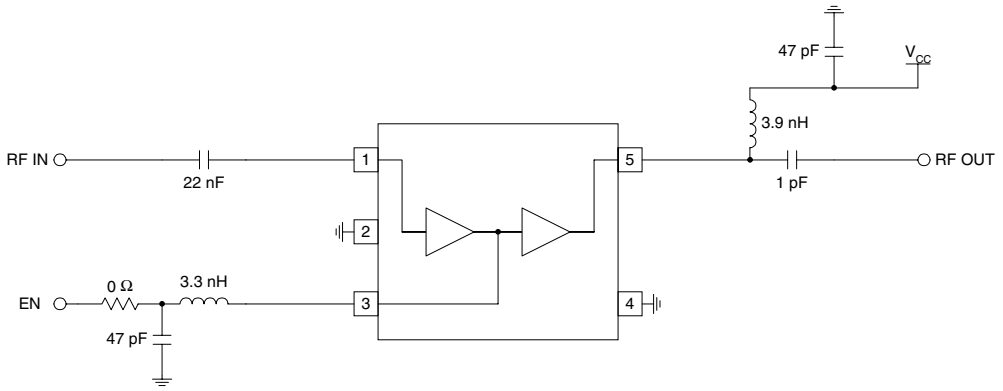
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range	1500		2500	MHz	
PCS Performance					Schematic per 1.9GHz LNA Application Schematic, V_{PD} = 3.0 V_{CC} = 3.0V, T=25°C
Gain		18		dB	V_{CC}=3.0V, I_{CC}=8.0mA
Noise Figure		1.6		dB	
Off Mode Gain		-15		dB	V_{CC}=3.0V, V_{PD}=0
$\|S_{12}\|$		25		dB	
Input IP3		-3.5		dBm	V_{CC}=3.0V, I_{CC}=5.0mA, R_1=150Ω (see application schematic)
		+2.0		dBm	V_{CC}=3.0V, I_{CC}=6.5mA, R_1=75Ω (see application schematic)
		+4.0		dBm	V_{CC}=3.0V, I_{CC}=8.0mA, R_1=0Ω (see application schematic)
Input VSWR		1.7			
Output VSWR		1.4			
2.4GHz Performance					Schematic per 2.4GHz LNA Application Schematic T=25°C
Gain		15.5		dB	V_{CC}=3.0V, I_{CC}=8.0mA
Noise Figure		1.75		dB	
Input IP3		+2.0		dBm	V_{CC}=3.0V, I_{CC}=8.0mA
Input VSWR		1.3			
Output VSWR		1.75			
Power Supply					T=25 °C
Voltage (V_{CC})		3.0		V	
Current Consumption		8.0		mA	V_{CC}=3.0V, IIP3=+4.0dBm
		6.5		mA	V_{CC}=3.0V, IIP3=+2.0dBm
		5.0		mA	V_{CC}=3.0V, IIP3=-3.5dBm
Into VPD Current		TBD		mA	
Power Down			10	µA	V_{CC}=3.5V; V_{PD}≤0.9V

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is DC coupled.	
2	GND1	Ground connection. See evaluation board schematic notes.	
3	PD	Power down pin. This pin serves as the interstage for the 2-stage LNA. An inductor is required to pull pin 3 to V_{CC} (see application schematic). If desired, this voltage can be lowered to trade off IP3 versus $I_{CC,TOTAL}$. (See table below.)	
4	GND2	Ground connection. See evaluation board schematic notes.	
5	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 4 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	

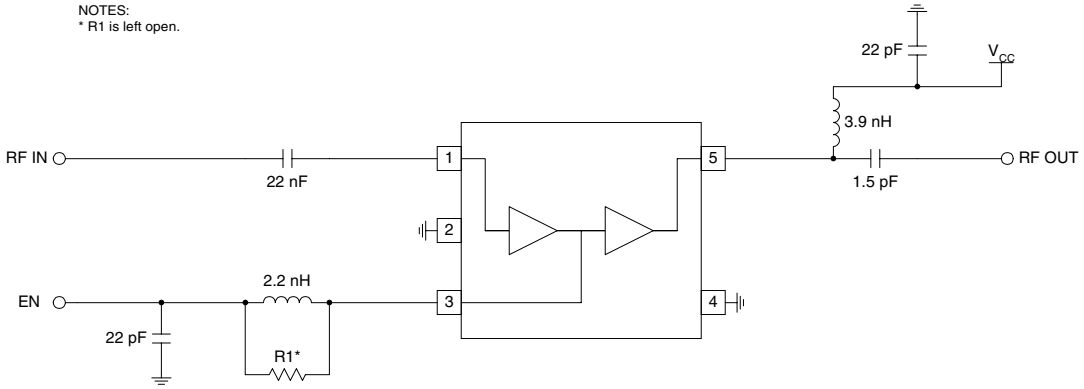
R1	IIP3	I_{CC}
0Ω	+4.0dBm	8.0mA
75Ω	+2.0dBm	6.5mA
150Ω	-3.5dBm	5.0mA

Application Schematic - 1.9GHz



Application Schematic - 2.4GHz

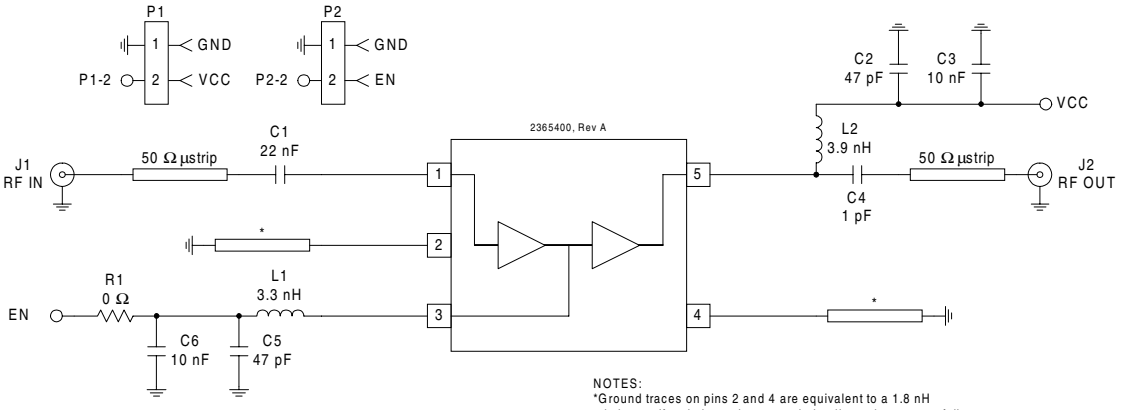
NOTES:
* R1 is left open.



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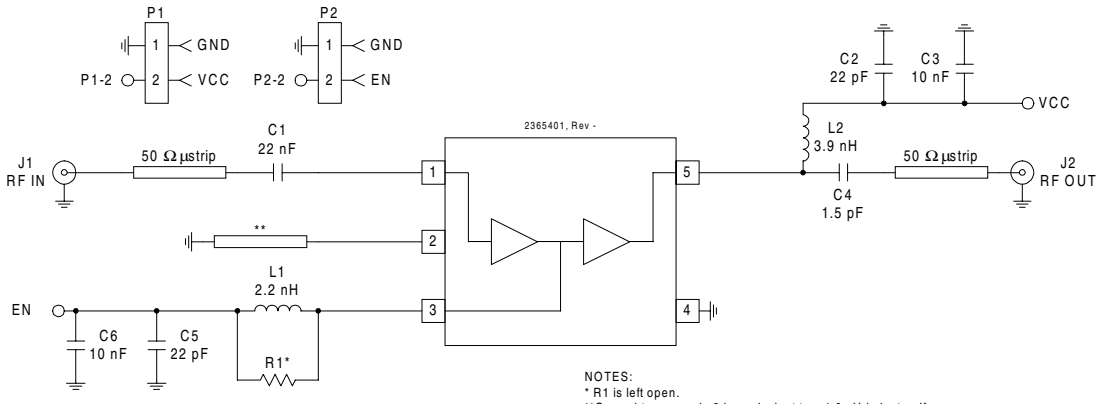
Evaluation Board Schematic - 1.9GHz

(Download Bill of Materials from www.rfmd.com.)



NOTES:
*Ground traces on pins 2 and 4 are equivalent to a 1.8 nH inductor. If an inductor is not used, the dimensions are as follows:
Length = 140 mils
Width = 20 mils
Height = 31 mils from the gound plane. Dielectric is FR-4.

Evaluation Board Schematic - 2.4GHz

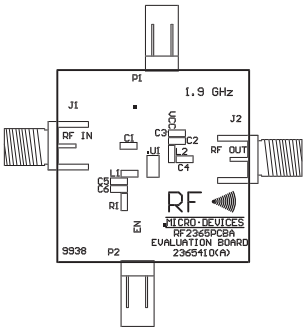


NOTES:
* R1 is left open.
**Ground trace on pin 2 is equivalent to a 1.0 nH inductor. If an inductor is not used, the dimensions are as follows:
Length = 85 mils
Width = 20 mils
Height = 31 mils from the gound plane. Dielectric is FR-4.

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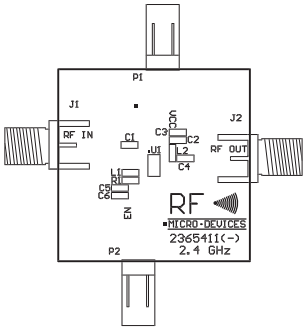
Evaluation Board Layout
Board Size 1” x 1”
1.9GHz

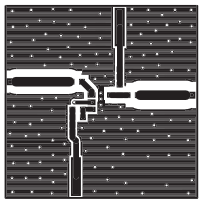
Board Thickness 0.031”; Board Material FR-4





2.4GHz





RF MICRO·DEVICES

Preliminary

RF2371

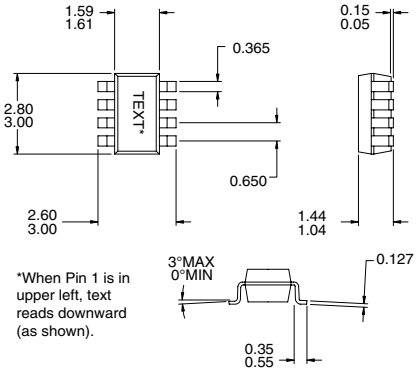
3V LOW NOISE AMPLIFIER

Typical Applications

- GSM Handsets
- CDMA Handsets
- TDMA Handsets
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

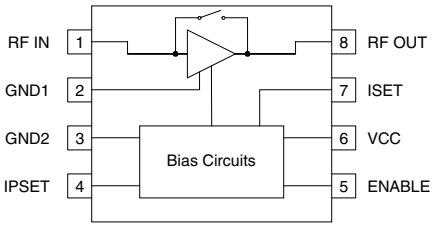
The RF2371 is a general purpose, low-cost, high performance low noise amplifier designed for operation from a 2.7V to 4V supply with low current consumption. The attenuation of the device is controlled when in power down mode, providing a known gain step. The RF2371 is available in a small industry-standard SOT23-8 surface mount package, enabling compact designs which conserve board space. The design features a highly accurate PTAT (Proportional To Absolute Temperature) biasing scheme using bandgap cells.



Package Style: SOT23-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 700MHz to 2000MHz Operation
- 2.7V to 3.6V Single Supply
- +5dBm Input IP_3 at 3.0mA
- 12dB Gain at 1950MHz
- 1.8dB Noise Figure at 1950MHz
- 17dB Gain Step

Ordering Information

RF2371	3V Low Noise Amplifier
RF2371 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4.0	V
Supply Current	20	mA
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

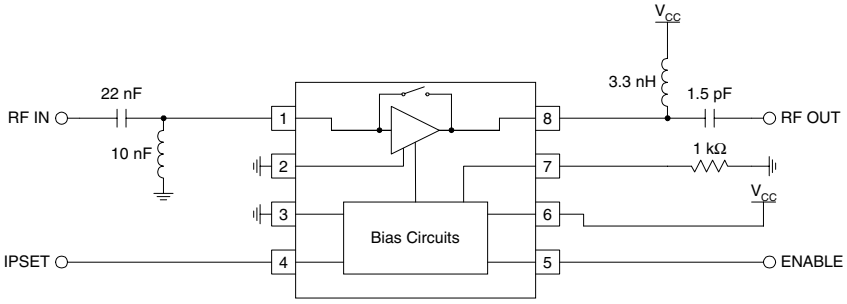
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=2.7V, $V_{ISELECT}$=0V, V_{ENABLE}=2.7V
Frequency Range		700 to 2000		MHz	
LNA Performance					Freq=1.95GHz
Gain	10.5	12.5		dB	
Noise Figure		1.6		dB	
Input IP3	+4.5	+8		dBm	At 2.9mA
Input VSWR		5:1		dB	(Noise match)
Output VSWR			1.5:1	dB	
Off Mode Gain		-5.0		dB	V_{ENABLE}=0V
Gain		17		dB	Freq=836MHz
Noise Figure		1.6		dB	
Input IP3		0		dBm	
Off Mode Gain		-8		dB	V_{ENABLE}=0V
Current Control					
Internal Current Setting “ON”		CMOS Low		V	Voltage on ISELECT
External Current Setting “ON”		CMOS High		V	Voltage on ISELECT
Current into ISELECT			1	µA	$V_{ISELECT}$=2.7V
Power Control					
Power “ON” Voltage		CMOS High		V	Voltage on ENABLE
Power “OFF” Voltage		CMOS Low		V	Voltage on ENABLE
Current into ENABLE			1	µA	V_{ENABLE}=2.7V
Power Supply					
Operating Voltage		2.7 to 3.6		V	
Operating Current		2.9	5	mA	V_{CC}=2.7V, Internal current setting
Leakage Current			1	µA	V_{ENABLE}=0V

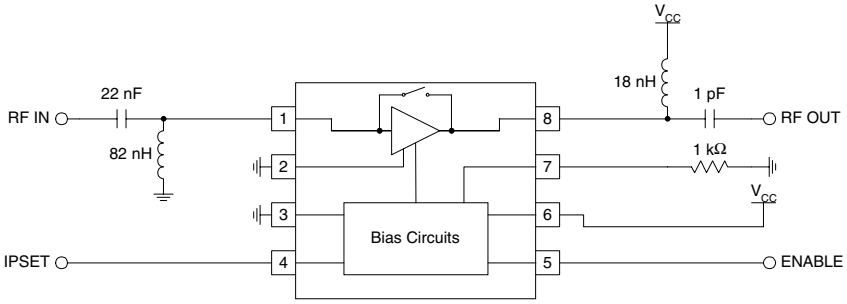
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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is not internally DC blocked and requires an external blocking capacitor.	
2	GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND2	Ground connection for the bias circuits.	
4	IPSET	This pin selects the internal current setting when CMOS level “low”, and the external current setting when this pin is CMOS level “high”. The current is set to 2.8mA using the internal current setting, and can be up to 20mA using the external current setting.	
5	ENABLE	Power down control. This is a CMOS input. When this pin is CMOS “high” the device is enabled. When the level is CMOS “low” the device is shut off and a controlled attenuator is turned on.	
6	VCC	Power supply for the bias circuits.	
7	ISET	This pin sets the current for the device. A resistor to ground of 1kΩ provides a current of 17.5mA. The condition for optimal IP3 is to use the internal current setting option and leave this pin open (no connect).	
8	RF OUT	RF output pin. Bias for the LNA is provided through this pin, hence it should be connected to VCC through an inductor.	

Application Schematic 1.95GHz



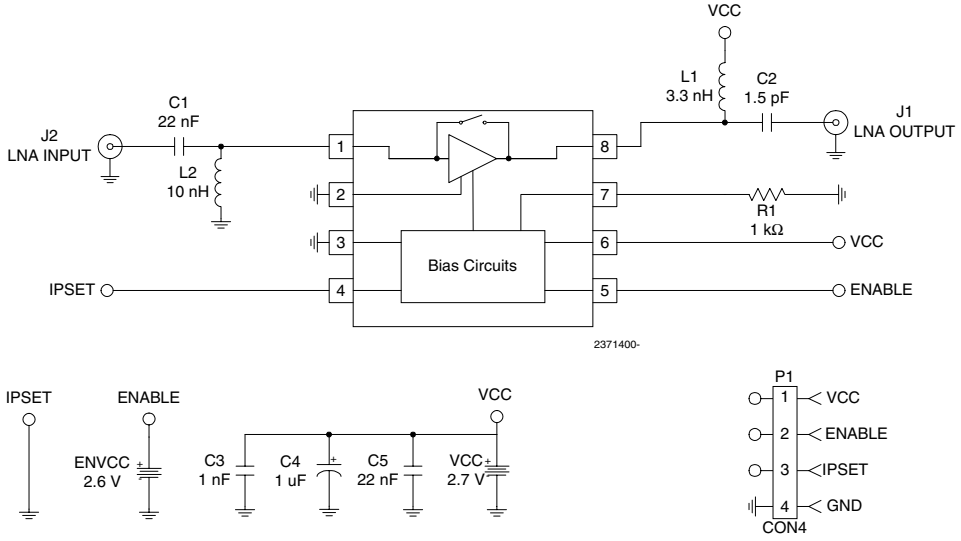
Application Schematic 836MHz



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Evaluation Board Schematic

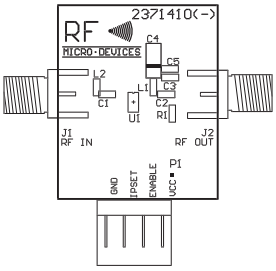
(Download Bill of Materials from www.rfmd.com.)

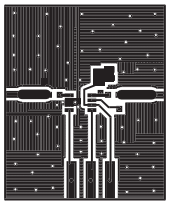


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Evaluation Board Layout
Board Size 0.833” x 1.009”

Board Thickness 0.031”, Board Material FR-4





RF MICRO·DEVICES

Preliminary

RF2375

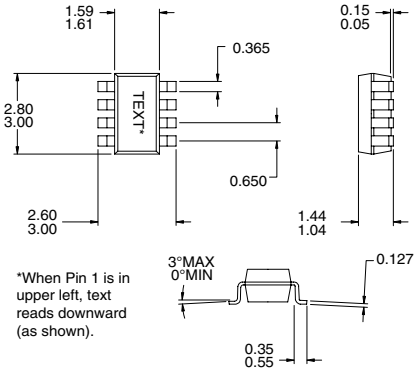
3V DCS LOW NOISE AMPLIFIER

Typical Applications

- LNA for DCS 1800/1900 Handsets
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

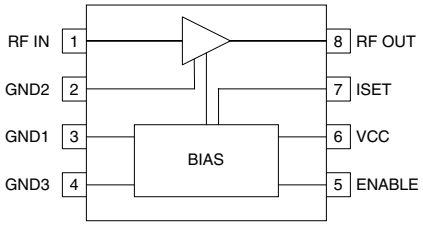
The RF2375 is a general purpose, low-cost, high performance, low noise amplifier designed for operation from a 2.7V to 4V supply with low current consumption. The attenuation of the device is controlled when in power down mode, providing a known gain step. The input IP_3 can be set with an external resistor to allow maximizing of the dynamic range of the receiver design. The RF2375 is available in a small industry-standard SOT-23-8 lead surface mount package, enabling compact designs which conserve board space. PTAT bias currents are used to bias the LNA.



Package Style: SOT-23-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- 700MHz to 2000MHz Operation
- 2.7V to 3.6V Single Supply
- -5dBm Input IP_3 at 5.3mA
- 18dB Gain at 1950MHz
- 2.5dB Noise Figure
- 25dB Gain Step

Ordering Information

RF2375	3V DCS Low Noise Amplifier
RF2375 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4.0	V
Supply Current	20	mA
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

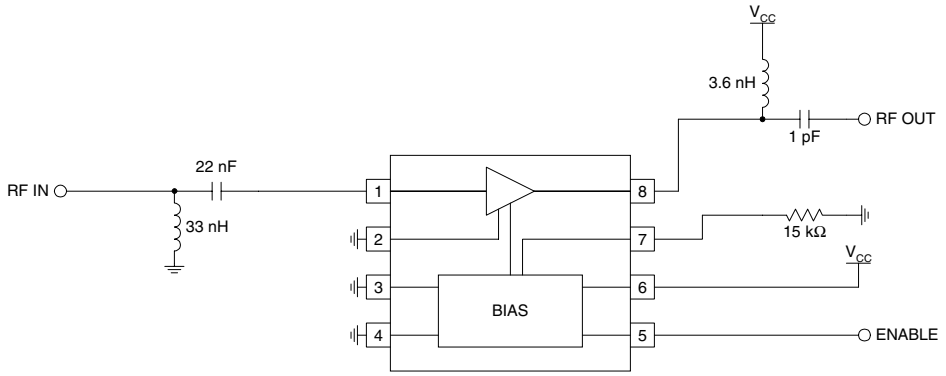
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=2.7V, Freq=1950MHz
Frequency Range		700 to 2000		MHz	
LNA Performance					
Gain	16	18		dB	
Noise Figure		2.5		dB	
Input IP3	-6	-5		dBm	At 5.3mA
Input VSWR		2:1		dB	
Output VSWR			1.5:1	dB	
Off Mode Gain		-7		dB	
Power Control					
Power “ON” Voltage		CMOS High		V	Voltage on ENABLE
Power “OFF” Voltage		CMOS Low		V	Voltage on ENABLE
Current into ENABLE			1	µA	V_{ENABLE}=2.7V
Power Supply					
Operating Voltage		2.7 to 3.6		V	
Operating Current		5.3	7	mA	V_{CC}=2.7V, R_{ISET}=15kΩ
Leakage Current			1	µA	V_{ENABLE}=0V

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is not internally DC blocked and requires an external blocking capacitor. The input impedance of this pin is internally matched to 50Ω using feedback.	
2	GND2	Ground connection for the bias circuits.	
3	GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND3	Same as pin 3.	
5	ENABLE	Power down control. This is a CMOS input. When this pin is CMOS "high" the device is enabled. When the level is CMOS "low" the device is shut off and a controlled attenuator is turned on.	
6	VCC	Power supply for the bias circuits.	
7	ISET	This pin sets the current for the device. A resistor to ground of 15kΩ provides a current of 5.3mA.	
8	RF OUT	RF output pin. The output impedance of this pin is internally matched to 50Ω using feedback. Bias for the LNA is provided through this pin, hence it should be connected to VCC through an inductor.	

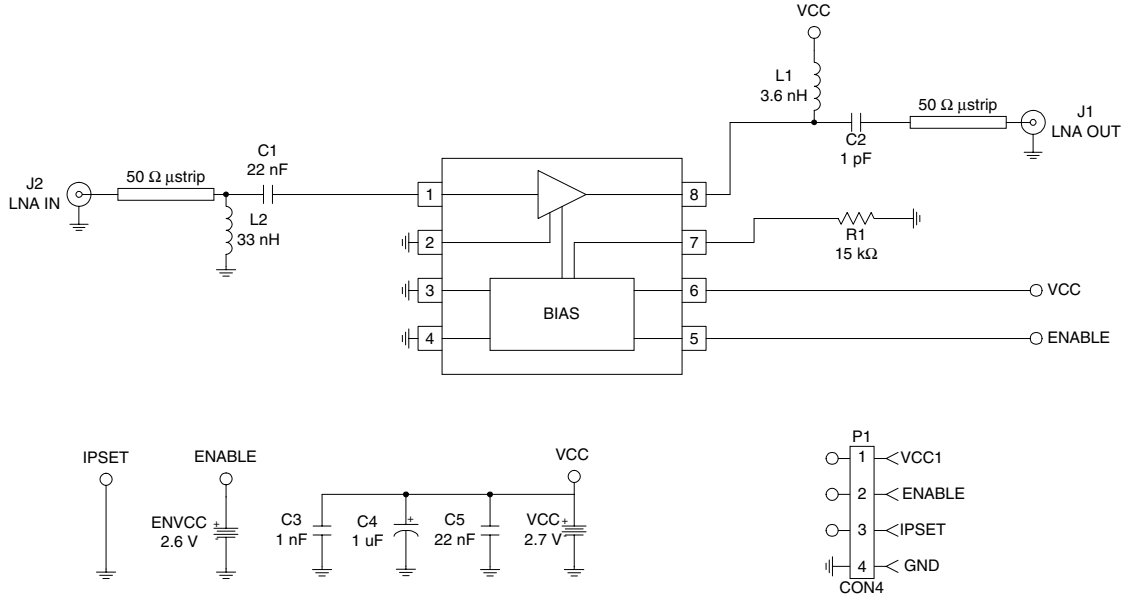
Application Schematic



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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



RF2442

HIGH-LINEARITY LOW NOISE AMPLIFIER

Typical Applications

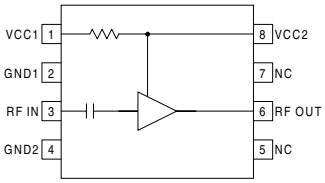
- TDMA/CDMA/FM Cellular Rx LNA
- TDMA/CDMA PCS Rx LNA
- Low Noise Transmit Driver Amplifier
- ISM Band LNA/Driver
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

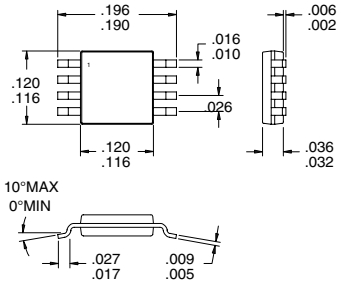
The RF2442 is a low noise amplifier with a very high dynamic range designed for the receive front end of digital cellular applications at 900MHz, 1900MHz, and 2400MHz. It is designed to amplify low level signals with minimum noise contribution while operating in the harsh, interference-rich environments of newly deployed digital subscriber units. The device also functions as an outstanding PA driver amplifier in the transmit chain of digital subscriber units where low transmit noise power is a concern. The device supports trade-offs between linearity and current drain. The designer has control of these trade-offs with the choice of an external bias resistor. The IC is featured in a standard miniature 8-lead plastic MSOP package.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: MSOP-8

Features

- Low Noise and High Intercept Point
- External Bias Control
- Single 2.5V to 5.0V Power Supply
- 500MHz to 2500MHz Operation
- Extremely Small MSOP-8 Package

Ordering Information

RF2442	High-Linearity Low Noise Amplifier
RF2442 PCBA-L	Fully Assembled Evaluation Board (~900MHz)
RF2442 PCBA-M	Fully Assembled Evaluation Board (~1900MHz)
RF2442 PCBA-H	Fully Assembled Evaluation Board (~2400MHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2442

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

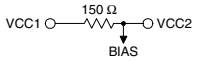
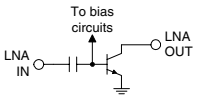
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		500 to 2500		MHz	Requires input tuning inductor below 1GHz
881MHz Performance					Schematic Evaluation Board L (R_C=0), T=25°C, RF=881MHz
Gain		20		dB	V_{CC}=3.6V
		19		dB	V_{CC}=3.0V
		18		dB	V_{CC}=2.5V
Output P1dB		+13		dBm	V_{CC}=3.6V
		+11		dBm	V_{CC}=3.0V
Output IP3		+27		dBm	V_{CC}=3.6V
		+22		dBm	V_{CC}=3.0V
		+16		dBm	V_{CC}=2.5V
Noise Figure		1.6		dB	V_{CC}=3.6V
		1.5		dB	V_{CC}=3.0V
		1.4		dB	V_{CC}=2.5V
Reverse Isolation		24		dB	V_{CC}=3.6V
		24		dB	V_{CC}=3.0V
		23		dB	V_{CC}=2.5V
1960MHz Performance					Schematic Evaluation Board M (R_C=0), T=25°C, RF=1960MHz
Gain		12		dB	V_{CC}=3.6V
		12		dB	V_{CC}=3.0V
		12		dB	V_{CC}=2.5V
Output P1dB		+16		dBm	V_{CC}=3.6V
		+13		dBm	V_{CC}=3.0V
Output IP3		+26		dBm	V_{CC}=3.6V
		+21		dBm	V_{CC}=3.0V
		+15		dBm	V_{CC}=2.5V
Noise Figure		1.6		dB	V_{CC}=3.6V
		1.5		dB	V_{CC}=3.0V
		1.4		dB	V_{CC}=2.5V
Reverse Isolation		20		dB	V_{CC}=3.6V
		19		dB	V_{CC}=3.0V
		19		dB	V_{CC}=2.5V

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
2400MHz Performance					Schematic Evaluation Board H (R_C=0), T=25°C, RF=2400MHz
Gain		9		dB	V_{CC}=3.6V
		9		dB	V_{CC}=3.0V
		8		dB	V_{CC}=2.5V
Output IP3		+26		dBm	V_{CC}=3.6V
		+21		dBm	V_{CC}=3.0V
		+15		dBm	V_{CC}=2.5V
Noise Figure		1.6		dB	V_{CC}=3.6V
		1.5		dB	V_{CC}=3.0V
		1.4		dB	V_{CC}=2.5V
Reverse Isolation		17		dB	V_{CC}=3.6V
		17		dB	V_{CC}=3.0V
		17		dB	V_{CC}=2.5V
Power Supply					T=25°C
Voltage		2.5 to 5.0		V	
Current Consumption		19		mA	V_{CC}=3.6V
		12		mA	V_{CC}=3.0V
		9		mA	V_{CC}=2.5V

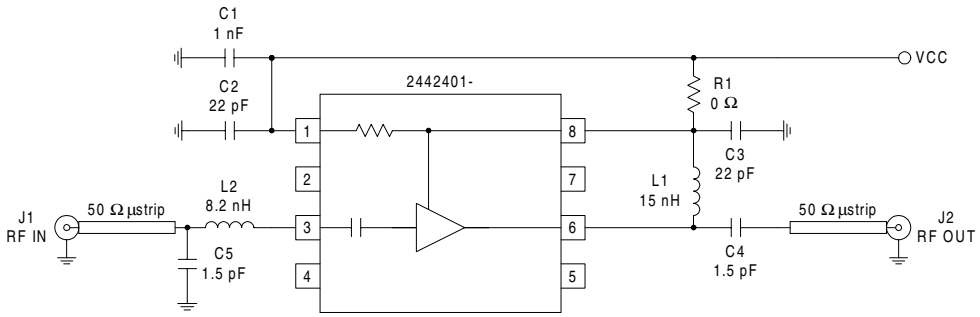
RF2442

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LNA. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. This pin connects to pin 8 through a 150Ω resistor. This allows for simple biasing of the collector at pin 6. Refer to Application Schematics 1 and 3.	
2	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	RF IN	RF input pin. This pin is internally DC blocked and matched to 50Ω for frequencies above 1 GHz. When using below 1 GHz, it is recommended that this pin be matched with series inductance to series-resonate out the internal blocking capacitor. Refer to Application Schematics 1 and 2.	
4	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	NC	No connection. This pin is typically left unconnected or grounded.	
6	RF OUT	LNA Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 8 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 3.
7	NC	No connection. This pin is typically left unconnected or grounded.	
8	VCC2	Optional power supply connection for biasing pin 6. This pin connects to pin 1 through a 150Ω resistor. This allows for simple biasing of the collector at pin 6. When used, this pin should be RF bypassed. Refer to Application Schematics 1 and 3.	See pin 1.

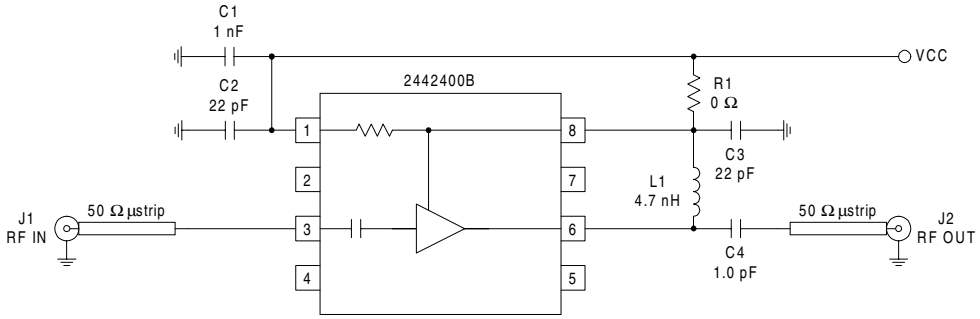
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Evaluation Board Schematic (L board) ~900 MHz

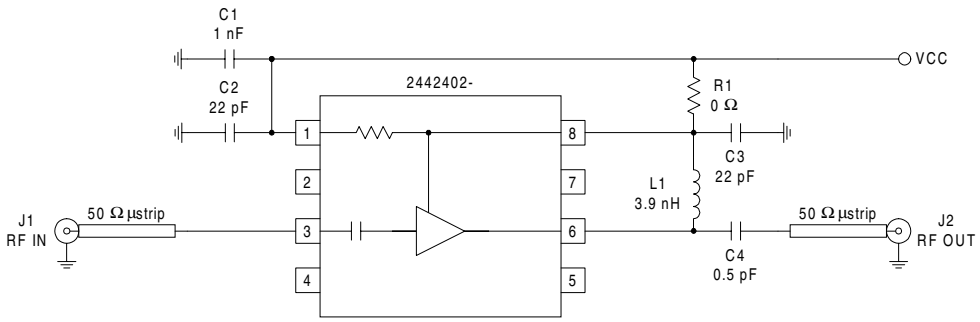
(Download Bill of Materials from www.rfmd.com.)



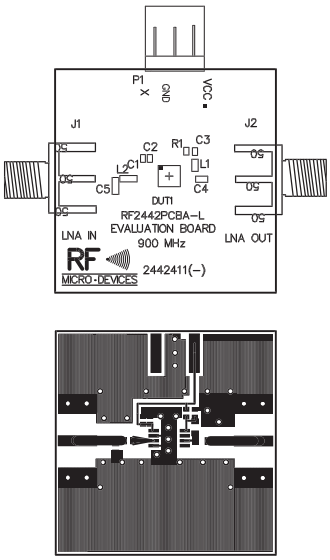
Evaluation Board Schematic (M board) ~1900 MHz



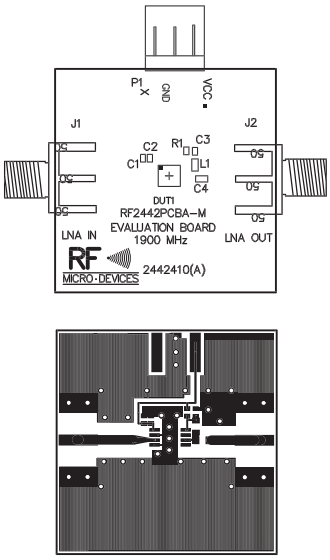
Evaluation Board Schematic (H board) ~2400 MHz



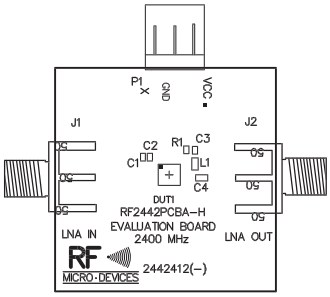
Evaluation Board Layout 900MHz
Board Size 1.150" x 1.165"

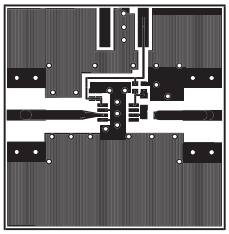


Evaluation Board Layout 1900MHz
Board Size 1.150" x 1.165"

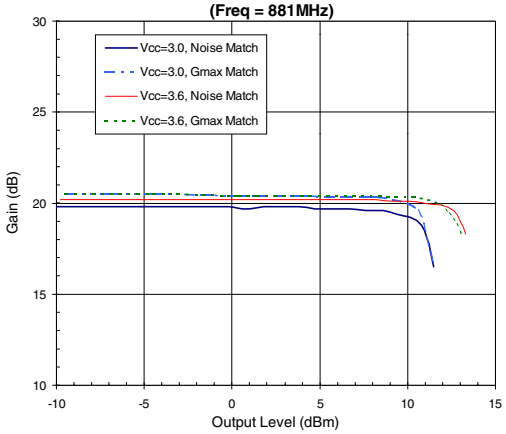


Evaluation Board Layout 2400MHz
Board Size 1.150" x 1.165"

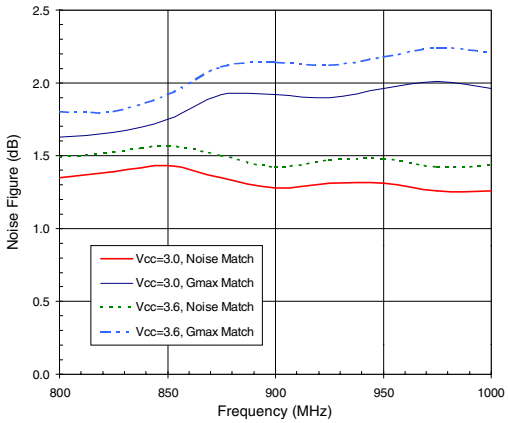




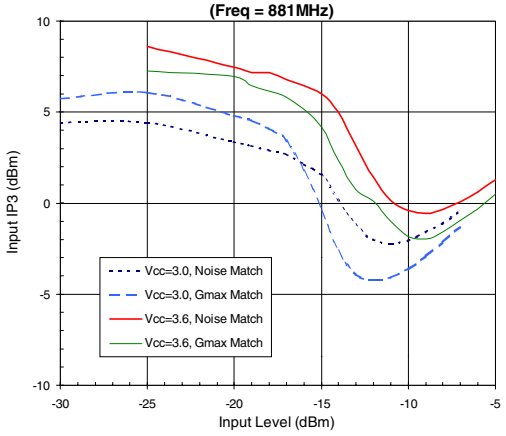
Gain vs. Output Level (Freq = 881MHz)



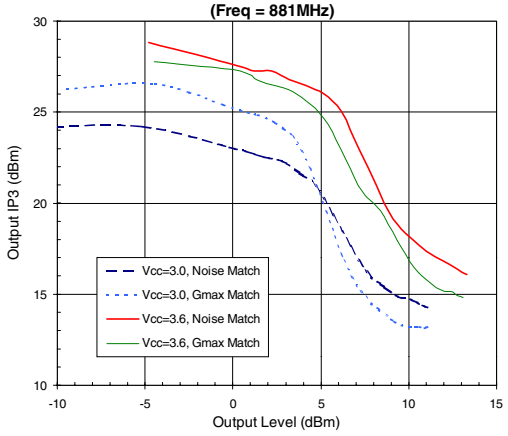
Noise Figure vs. Frequency



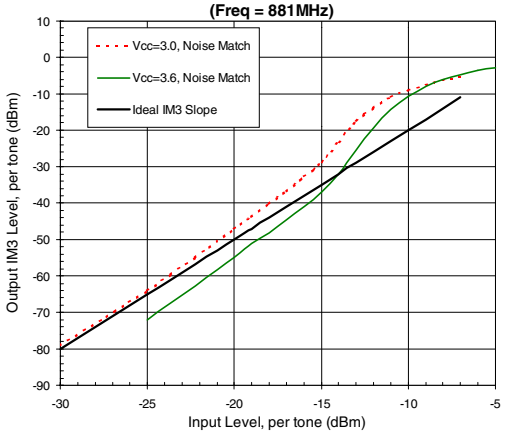
Input IP3 vs. Input Level (Freq = 881MHz)



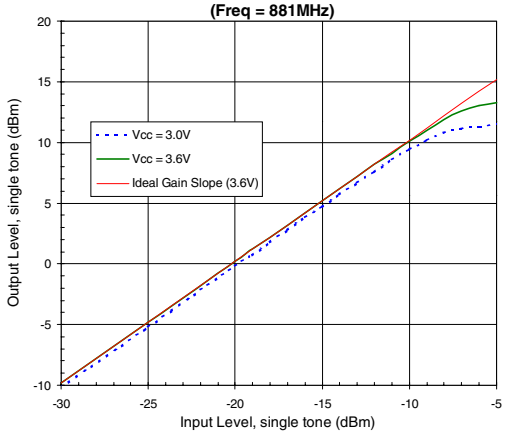
Output IP3 vs. Output Level (Freq = 881MHz)



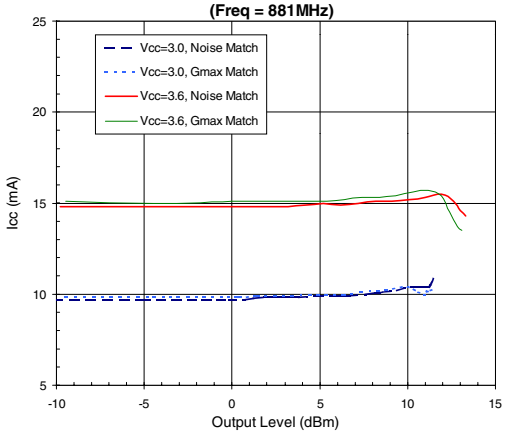
Output IM3 Level vs. Input Level (Freq = 881MHz)



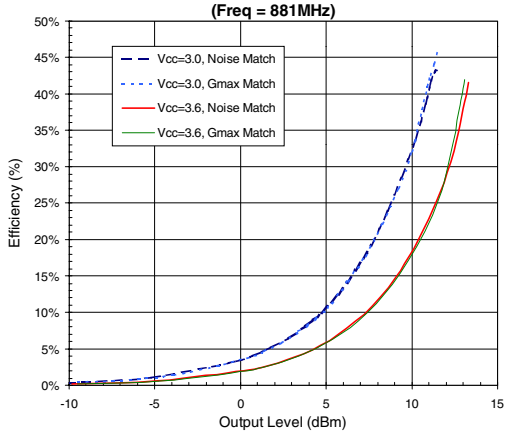
Power Out vs. Power In (Freq = 881MHz)



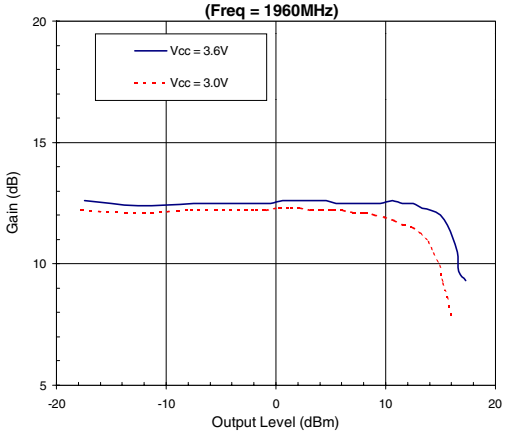
Icc vs. Output Level (Freq = 881MHz)



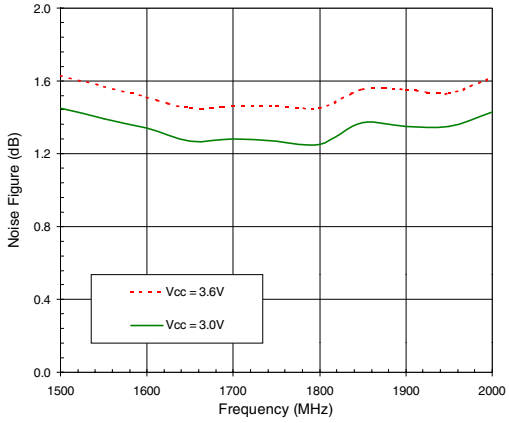
Efficiency vs. Output Level (Freq = 881MHz)



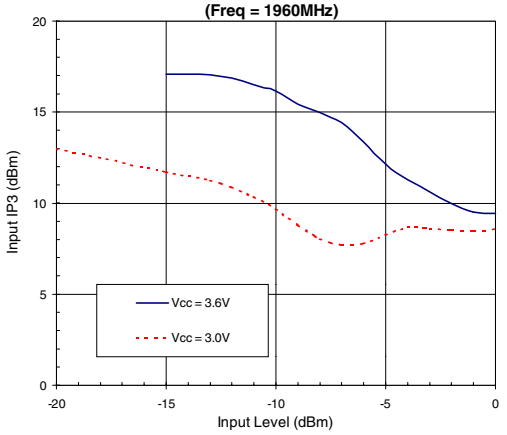
Gain vs. Output Level (Freq = 1960MHz)



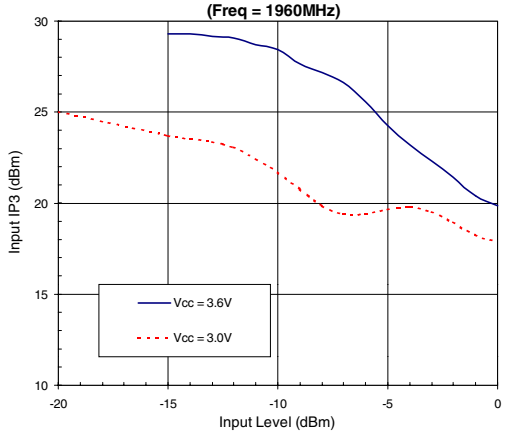
Noise Figure vs. Frequency



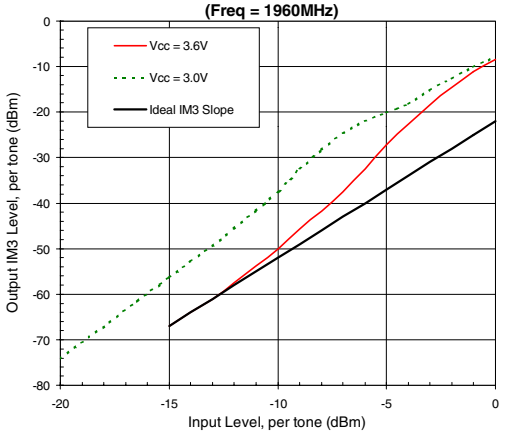
Input IP3 vs. Input Level (Freq = 1960MHz)



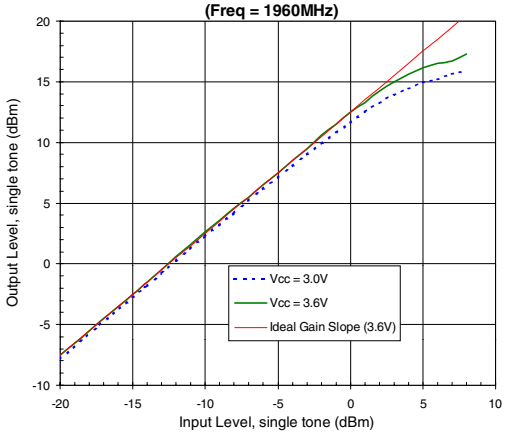
Output IP3 vs. Input Level (Freq = 1960MHz)



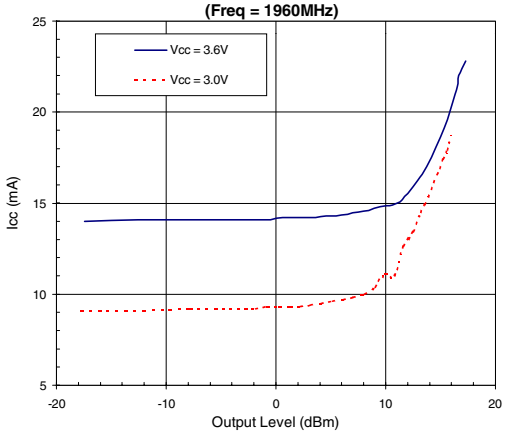
Output IM3 Level vs. Input Level (Freq = 1960MHz)



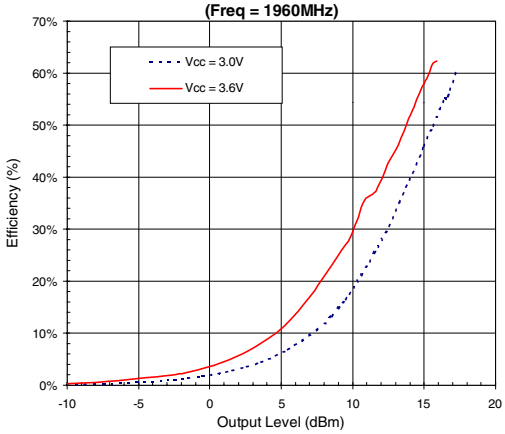
Power Out vs. Power In (Freq = 1960MHz)



Icc vs. Output Level (Freq = 1960MHz)



Efficiency vs. Output Level (Freq = 1960MHz)



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RF2445

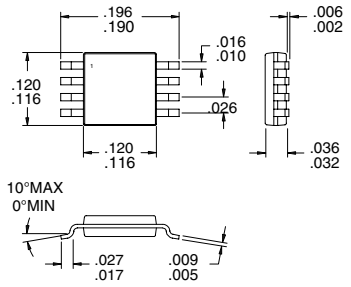
3V DCS LOW NOISE AMPLIFIER

Typical Applications

- LNA for DCS 1800/1900 Handsets
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

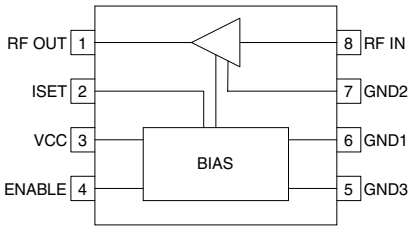
The RF2445 is a general purpose, low-cost, high-performance, low-noise amplifier designed for operation from a 2.7V to 3.6V supply with low current consumption. The device features a power-down mode with controlled attenuation, which can be used to save current while providing a controlled gain step. The device linearity (Input IP3) and current drain are set with an external resistor, allowing the designer to select the optimum performance for a given application. "Proportional to Absolute Temperature (PTAT)" biasing is used to provide consistent performance across a wide temperature range. The RF2445 is available in a small industry-standard MSOP-8 lead surface mount package, enabling compact designs which conserve board space.



Package Style: MSOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- 700MHz to 2000MHz Operation
- 2.7V to 3.6V Single Supply
- -5dBm Input IP_3 at 5.3mA
- 19dB Gain at 1950MHz
- 2.2dB Noise Figure
- 27dB Gain Step

Ordering Information

RF2445	3V DCS Low Noise Amplifier
RF2445 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2445

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4.0	V
Supply Current	20	mA
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

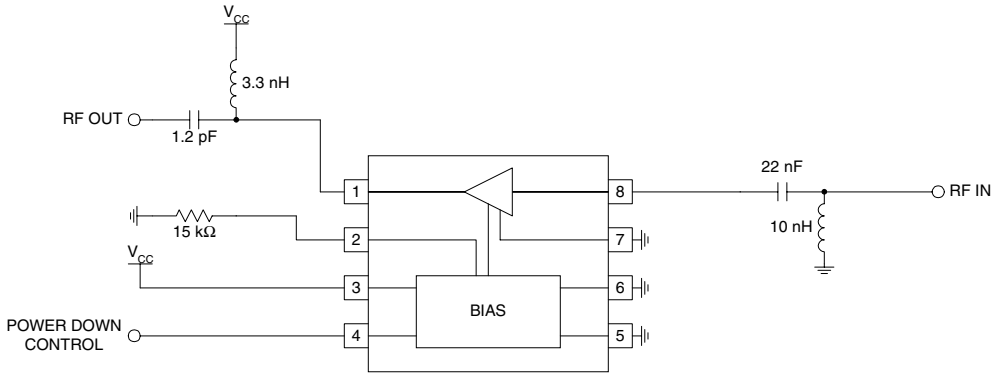
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=2.7V, T=27°C
Frequency Range		700 to 2000		MHz	
High Gain Mode					V_{ENABLE}=2.7V, R_{ISET}=15kΩ
Gain		20.5		dB	At 1700MHz
Noise Figure		1.8		dB	
Input IP3		-6.0		dBm	
Gain		18.5		dB	At 1880MHz
Noise Figure		2.2		dB	
Input IP3		-4.0		dBm	
Input VSWR		2:1			
Output VSWR		1.5:1			
Gain		18		dB	At 2000MHz
Noise Figure		2.5		dB	
Input IP3		-3.0		dBm	
Power-Down Mode					V_{ENABLE}=0V
Gain		-6.0		dB	At 1700MHz
Gain		-8.0		dB	At 1880MHz
Gain		-7.0		dB	At 2000MHz
Power Supply					
Power Supply Range (VCC)	2.7	3.0	3.6	V	
Current Drain (ICC)		5.3	7.0	mA	V_{ENABLE}=2.7V, R_{ISET}=15kΩ (High Gain Mode)
Current into ENABLE			1	µa	V_{ENABLE}=2.7V
Current Drain (ICC)			1	µa	V_{ENABLE}=0V (Power-Down Mode)

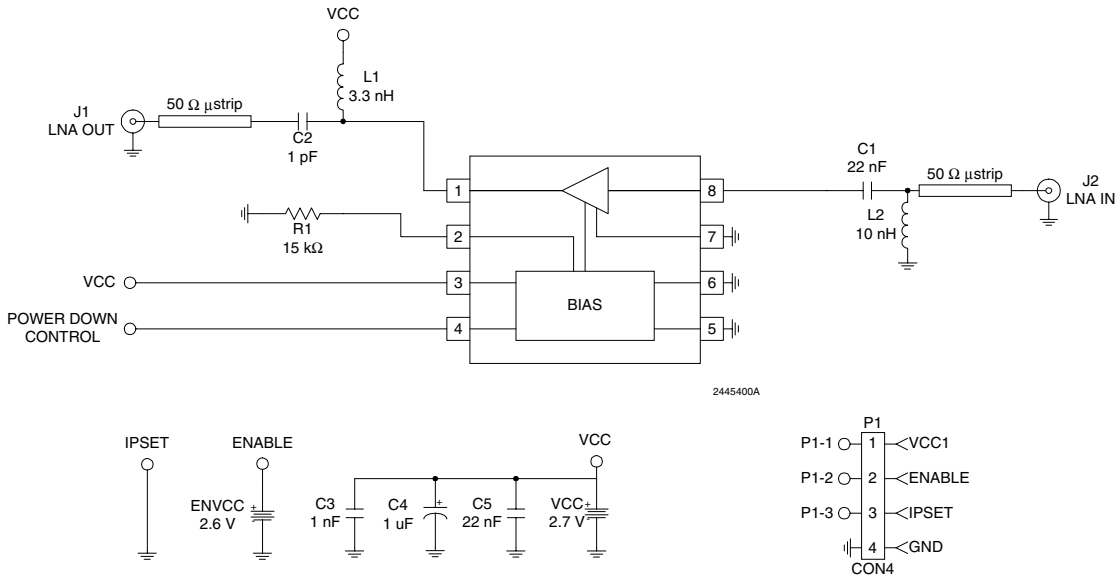
Pin	Function	Description	Interface Schematic
1	RF OUT	RF output pin. The output impedance of this pin is internally matched to 50Ω using feedback. Bias for the LNA is provided through this pin, hence it should be connected to VCC through an inductor.	
2	ISET	This pin sets the current for the device. A resistor to ground of 15kΩ provides a current of 5.3mA.	
3	VCC	Power supply for the bias circuits.	
4	POWER DOWN CONTROL	Power down control. This is a CMOS input. When this pin is CMOS "high" the device is enabled. When the level is CMOS "low" the device is shut off and a controlled attenuator is turned on.	
5	GND3	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
6	GND1	Same as pin 5.	
7	GND2	Ground connection for the bias circuits.	
8	RF IN	RF input pin. This pin is not internally DC blocked and requires an external blocking capacitor. The input impedance of this pin is internally matched to 50Ω using feedback.	

Application Schematic



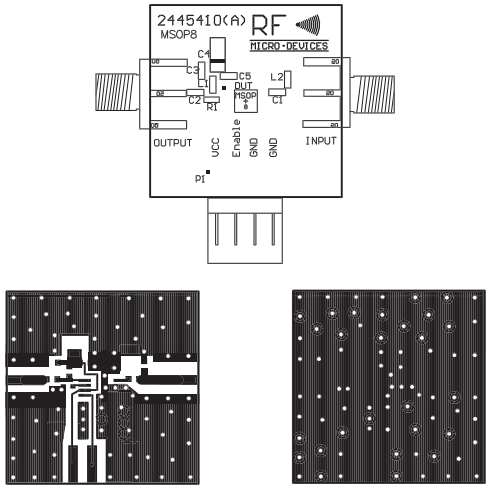
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.0" x 1.0"

Board Thickness 0.031”; Board Material FR-4



RF2445

RF2451

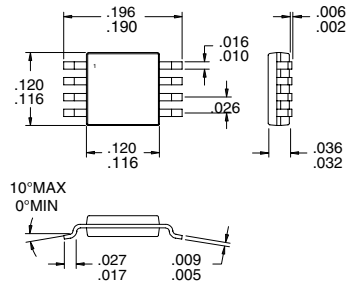
3V LOW NOISE AMPLIFIER

Typical Applications

- GSM Handsets
- CDMA Handsets
- TDMA Handsets
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Oscillator Loop Amplifiers

Product Description

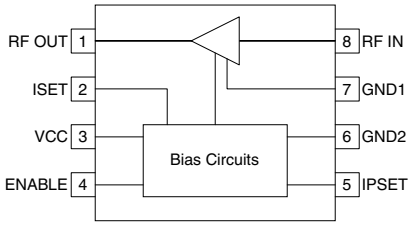
The RF2451 is a general purpose, low-cost, high performance low noise amplifier designed for operation from a 2.7V to 4V supply with low current consumption. The attenuation of the device is controlled when in power down mode, providing a known gain step. The RF2451 is available in a small industry-standard MSOP-8 surface mount package, enabling compact designs which conserve board space. The design features accurate PTAT (Proportional To Absolute Temperature) biasing scheme using band gap cells.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8



Functional Block Diagram

Features

- 700MHz to 2000MHz Operation
- 2.7V to 3.6V Single Supply
- +5dBm Input IP_3 at 3.0mA
- 12dB Gain at 1950MHz
- 1.8dB Noise Figure at 1950MHz
- 17dB Gain Step

Ordering Information

RF2451	3V Low Noise Amplifier
RF2451 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2451

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4.0	V
Supply Current	20	mA
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

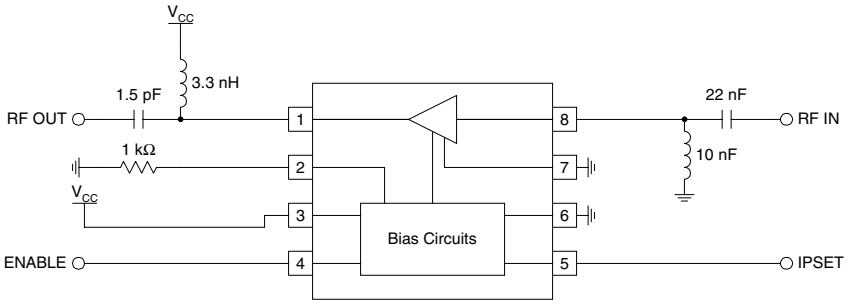
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=27°C, V_{CC}=2.7V, $V_{ISELECT}$=0V, V_{ENABLE}=2.7V
Frequency Range		700 to 2000		MHz	
LNA Performance					Freq=1.95GHz
Gain	10.5	12.5		dB	
Noise Figure		1.6		dB	
Input IP3	+4.5	+8		dBm	At 2.9mA
Input VSWR		5:1		dB	(Noise match)
Output VSWR			1.5:1	dB	
Off Mode Gain		-5.0		dB	V_{ENABLE}=0V
Gain		17		dB	Freq=836MHz
Noise Figure		1.6		dB	
Input IP3		0		dBm	
Off Mode Gain		-8		dB	V_{ENABLE}=0V
Current Control					
Internal current setting “ON”		CMOS Low		V	Voltage on ISELECT
External current setting “ON”		CMOS High		V	Voltage on ISELECT
Current into ISELECT			1	µA	$V_{ISELECT}$=2.7V
Power Control					
Power “ON” Voltage		CMOS High		V	Voltage on ENABLE
Power “OFF” Voltage		CMOS Low		V	Voltage on ENABLE
Current into ENABLE			1	µA	V_{ENABLE}=2.7V
Power Supply					
Operating Voltage		2.7 to 3.6		V	
Operating Current		2.9	5	mA	V_{CC}=2.7V, Internal current setting
Leakage Current			1	µA	V_{ENABLE}=0V

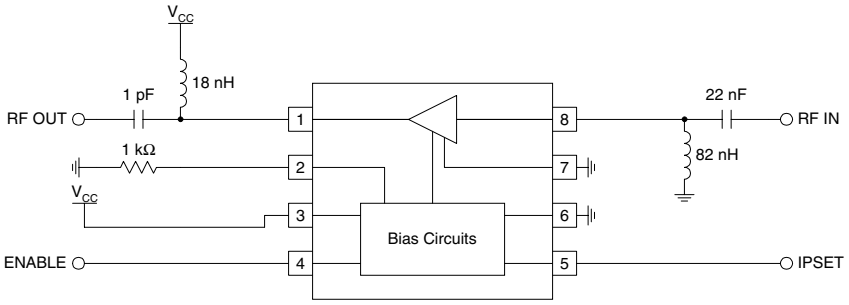
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Pin	Function	Description	Interface Schematic
1	RF OUT	RF output pin. Bias for the LNA is provided through this pin, hence it should be connected to VCC through an inductor.	
2	ISET	This pin sets the current for the device. A resistor to ground of 1kΩ provides a current of 17.5mA. The condition for optimal IP3 is to use the internal current setting option and leave this pin open (no connect).	
3	VCC	Power supply for the bias circuits.	
4	ENABLE	Power down control. This is a CMOS input. When this pin is CMOS “high” the device is enabled. When the level is CMOS “low” the device is shut off and a controlled attenuator is turned on.	
5	IPSET	This pin selects the internal current setting when CMOS level “low”, and the external current setting when this pin is CMOS level “high”. The current is set to 2.8mA using the internal current setting, and can be up to 20mA using the external current setting.	
6	GND2	Ground connection for the bias circuits.	
7	GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
8	RF IN	RF input pin. This pin is not internally DC blocked and requires an external blocking capacitor.	

Application Schematic 1.95GHz

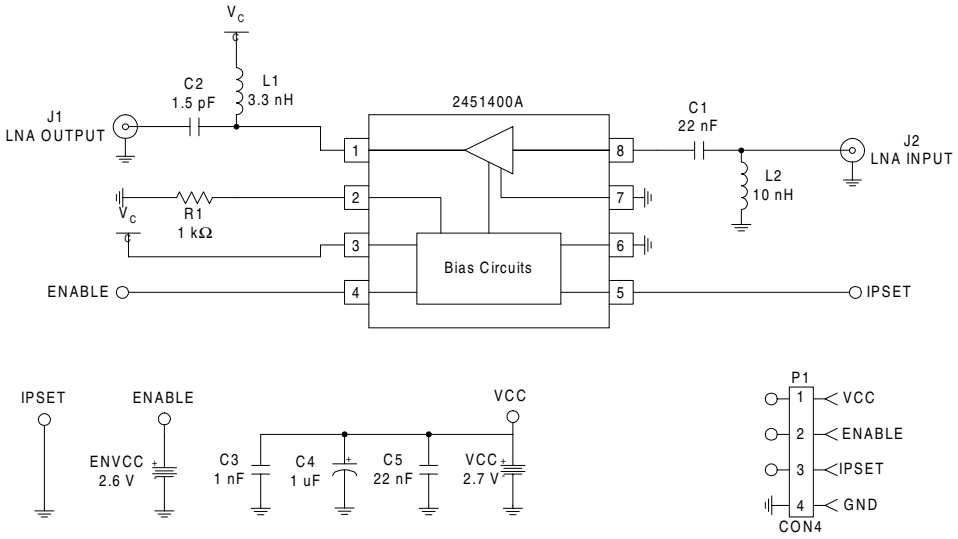


Application Schematic 836MHz



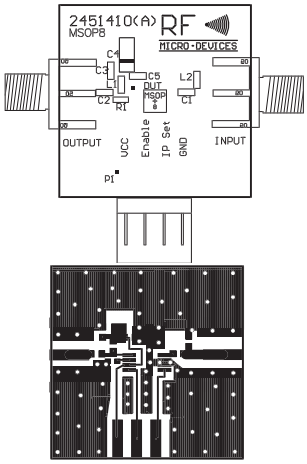
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1” x 1”

Board Thickness 0.031”, Board Material FR-4



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5 Modulators And Upconverters

Part	Description	Frequency (MHz)	Vcc (Volts)	Conversion Method	Icc (mA)	Gain Control (dB)	Mod BW (MHz)	Package	Page
RF2402	UHF Quadrature Modulator	600 to 1000	3 to 5.5	Direct	28	n/a	100	SOP-14	5-1
RF2412	Broadband Dual-Conversion Quadrature Modulator	100 to 1000	3 to 6.5	Dual	31	n/a	50	SOP-20	5-7
RF2413	Gain Controlled Dual-Conversion Quadrature Modulator	200 to 1000	3 to 6.5	Dual	35	60	25	SOP-20	5-19
RF2422	2.5GHz Direct Quadrature Modulator	800 to 2500	4.5 to 6.0	Direct	45	n/a	250	SOP-16	5-29
RF2423	100mW Spread-Spectrum Transmitter IC	800 to 1000	4.5 to 6.0	Direct	110	25	100	SOP-16	5-35
RF2424	UHF Quadrature Modulator	700 to 1000	2.7 to 5.5	Direct	45	n/a	TBD	SOP-16	5-43
RF2454	VHF Quadrature Modulator	200 to 600	3 to 5.5	Direct	28	n/a	100	SOP-14	5-49
RF2464	VHF Quadrature Modulator	200 to 600	4.5 to 5.5	Direct	28	n/a	100	SOP-14	5-55
RF2658	Transmit Modulator, IF AGC, and Upconverter	900 to 1000	2.7 to 3.3	Dual	43 to 63	88	50	SSOP-28	5-61
RF2668	CDMA/FM Transmit Modulator, IF AGC, and Upconverter with Integrated PLL	700 to 2000	2.7 to 3.3	Dual	40 to 69	95	20	LQFP-48	5-71
RF2713	Quadrature Modulator/Demodulator	0.1 to 250	2.7 to 6	Direct	10	n/a	50	SOP-14	5-83
RF2909	3V 915MHz Spread-Spectrum Transmitter IC	100 to 1100	2.7 to 5.0	Direct	30 to 175	20	10	SSOP-24	11-103
RF9958	CDMA/FM Transmit Modulator, IF AGC, and Upconverter	900 to 1000	2.7 to 3.3	Dual	43 to 63	88	50	SSOP-28	5-93

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RF MICRO·DEVICES

RF2402

UHF QUADRATURE MODULATOR

Typical Applications

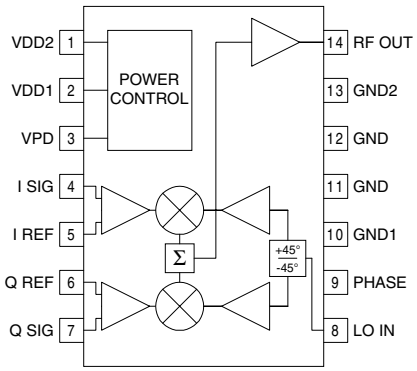
- Digital and Spread Spectrum Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- GSM and D-AMPS Cellular Systems
- AM, SSB, DSB Modulation
- Image-Reject Upconverters

Product Description

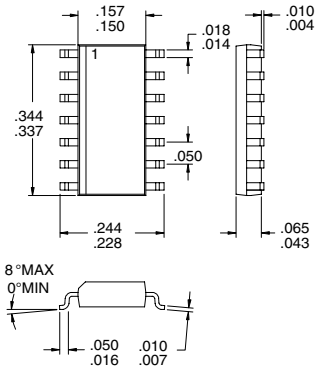
The RF2402 is a monolithic integrated universal modulation system capable of generating modulated AM, PM, or compound carriers in the UHF frequency range. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining amplifier, and an output RF amplifier which will drive a 50Ω load. Component matching, which can only be accomplished with monolithic construction, is used to full advantage to obtain excellent amplitude balance and high phase accuracy. The unit features low power consumption, single power supply operation, and adjustment free operation with no external parts required to operate the part as specified.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

5 MODULATORS AND UPCONVERTERS

Features

- Single 3V to 5V Power Supply
- Low Power and Small Size
- CMOS Compatible Power Down Control
- Excellent Amplitude and Phase Balance
- Low Broadband Noise Floor
- 600MHz to 1000MHz Operation

Ordering Information

RF2402	UHF Quadrature Modulator
RF2402 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2402

Absolute Maximum Ratings

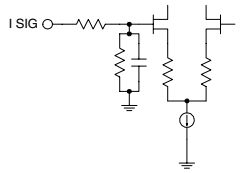
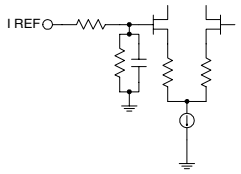
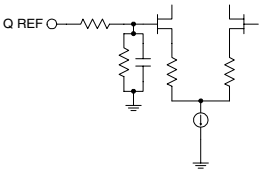
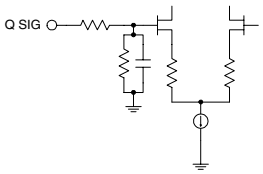
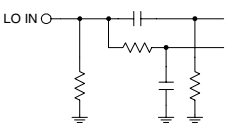
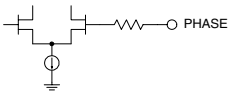
Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +7.5	V_{DC}
Power Down Voltage	-0.5 to V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

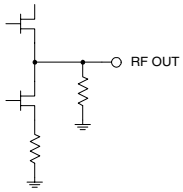
Caution! ESD sensitive device.

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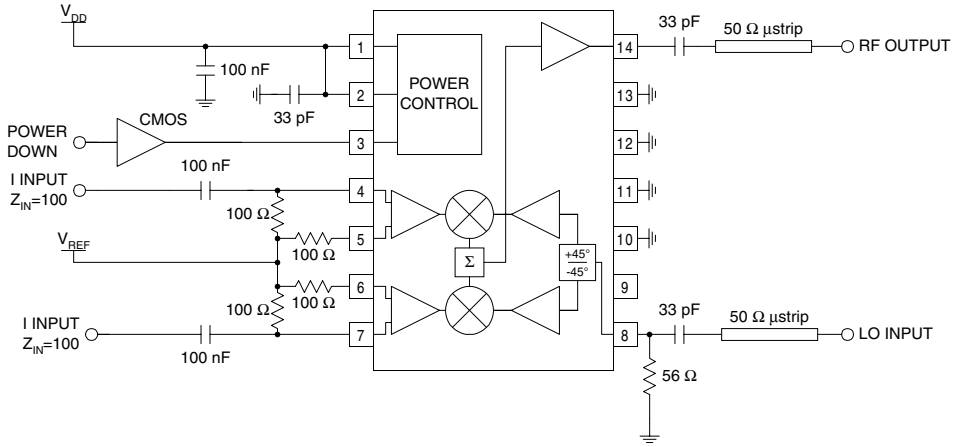
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input					T=25°C, V_{CC}=5V_{DC}, I&Q inputs=2V_{PP}
Frequency Range		600 to 1000		MHz	
Power Level		-3 to +6		dBm	
Input VSWR		1.2:1			With external 50Ω termination.
Input Impedance		200-j200		Ω	At 900MHz, without external 50Ω termination.
Modulation Input					
Frequency Range		DC to 100		MHz	
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Modulation (I&Q)		V_{REF}±2		V	I & Q signals for 0dBm output power.
Maximum Modulation (I&Q)		V_{REF}±2.5		V	In-phase and quadrature signals.
Input Resistance		3000		Ω	
DC Offset		50	150	mV	I_{SIG}-I_{REF} and Q_{SIG}-Q_{REF} for DC balance
Amplitude Error (I/Q)		0.2		dB	
Quadrature Phase Error		±3		°	From 800MHz to 1000MHz.
RF Output					V_{DD}=5V, LO Power=0dBm, LO Freq=900MHz, SSB
Output Power		0		dBm	
Output Impedance		50		Ω	
Output VSWR		1.5:1			
Broadband Noise Floor		-155		dBm/Hz	
Sideband Suppression		25		dB	
Carrier Suppression		40		dB	Modulation DC offset externally adjusted for optimum suppression. Suppression is typically better than 25dB without adjustment.
Power Down					
Turn On/Off Time			<100	ns	
PD Input Resistance		>1		MΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage
Power Down "OFF"		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 5.5		V	Operating Limits
Current		28	39	mA	Operating
		0.5	2	mA	Power Down

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Pin	Function	Description	
1	VDD2	Power supply for the RF Output amplifier. An external RF bypass capacitor is needed. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the capacitor should connect immediately to the ground plane.	
2	VDD1	Power supply for all other circuits. An external RF bypass capacitor is needed.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when +5V all circuits are operating. This is a high impedance input, internally connected to the gates of a few FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. In order to maximize output power this pin should be as close to +5V as possible during normal operation.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, it will typically be better than 25dB.	
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, it will typically be better than 25dB. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, Q SIG and Q REF also need to be swapped to maintain correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V.	
8	LO IN	The input of the phase shifting network. This high impedance input can be matched with an external 56Ω termination resistor. This pin is internally connected to ground through a 4kΩ resistor. Putting a DC voltage on this pin is not recommended. However, connecting this pin to ground, e.g. through a shunt inductor, is allowed.	
9	PHASE	This pin adjusts the phase of the I/Q signals. However, the control is very sensitive and hard to control. Control voltage change for a few degrees adjustment is in the order of 10mV. Device to device and temperature variation are not characterized. Therefore it is not recommended to use this pin; leave it not connected. Do NOT connect it to ground. For compensating large errors in the I/Q signals supplied to the device or in control loops, this pin may prove useful.	

10	**GND1**	Ground connection of the LO phase shift network. This pin should be connected directly to the ground plane.	
11	**GND**	Ground connection for other circuits. Keep traces short and connect to ground plane immediately.	
12	**GND**	Same as pin 11.	
13	**GND2**	Ground connection for the RF output stage. A good ground connection is especially important at this pin to avoid interference with other circuits.	
14	**RF OUT**	50Ω output. This pin carries a DC voltage, and an external blocking capacitor is recommended.	

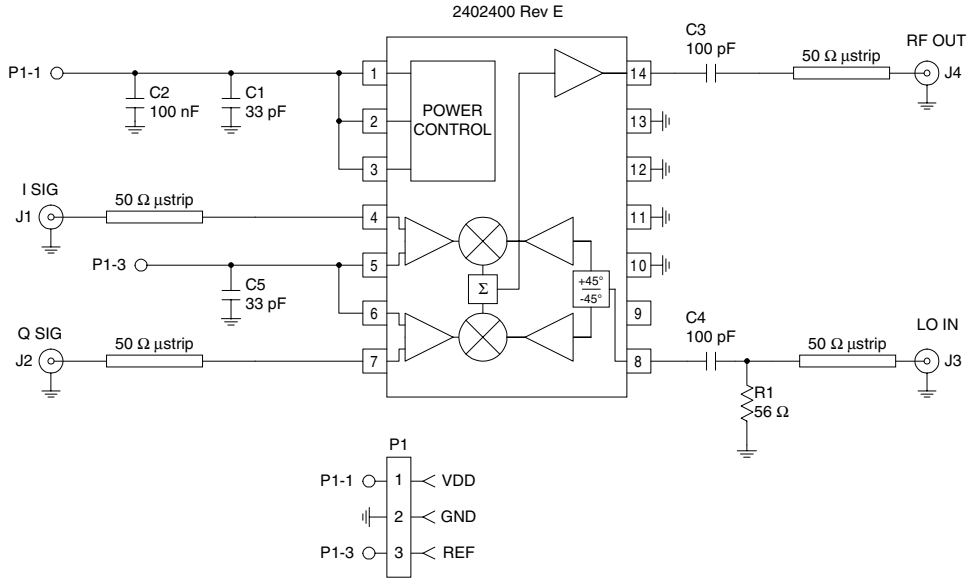
Application Schematic



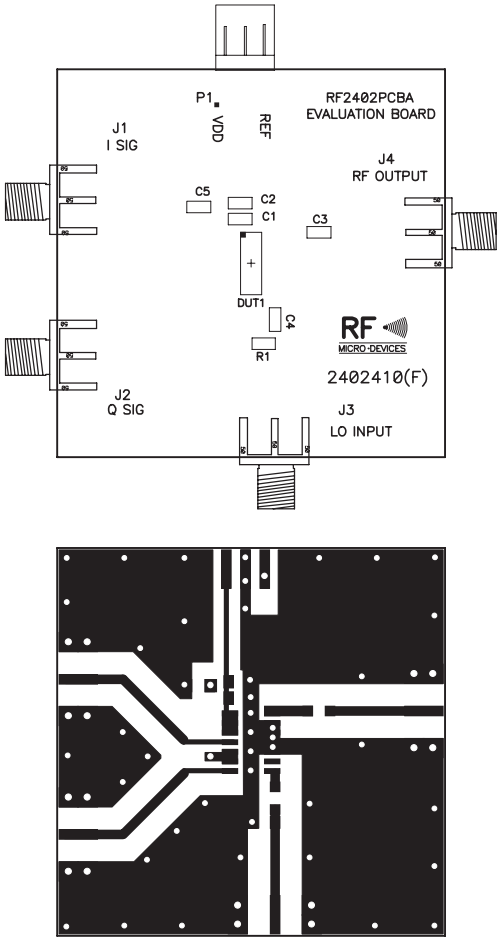
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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2.020" x 2.020"



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RF MICRO·DEVICES

RF2412

BROADBAND DUAL-CONVERSION QUADRATURE MODULATOR

Typical Applications

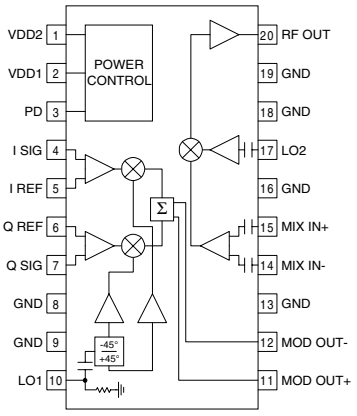
- Digital and Spread Spectrum Systems
- Analog Communication Systems
- UHF Digital and Analog Transmitters
- GMSK, QPSK, DQPSK, QAM
- Portable Battery Powered Equipment
- Commercial and Consumer Systems

Product Description

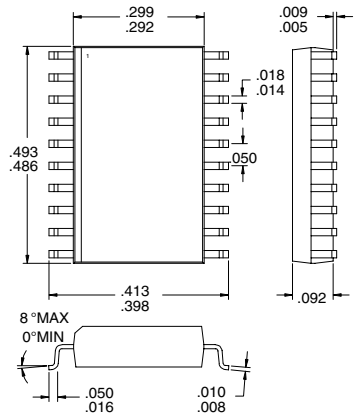
The RF2412 is a monolithic integrated transmitter universal modulation IC capable of generating modulated AM, PM, or compound carriers in the VHF/UHF frequency range. The modulation is performed at VHF, then the resulting spectrum is upconverted to a frequency range between 100MHz to 1000MHz. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a LO 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining differential amplifier, a second upconvert balanced mixer, and an output RF amplifier which will drive a 50Ω load. Since the modulation is performed at a low frequency, excellent amplitude balance and phase accuracy are obtained.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-20

Features

- Single 3V to 6V Power Supply
- Digitally-Controlled Power Down Mode
- Dual Conversion
- DC to 50MHz Modulation Frequency
- 50MHz to 150MHz IF Frequency
- 100MHz to 1000MHz RF Frequency

Ordering Information

RF2412	Broadband Dual-Conversion Quadrature Modulator
RF2412 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2412

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.5	V_{DC}
PD Voltage	V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

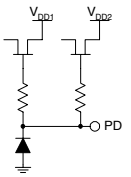
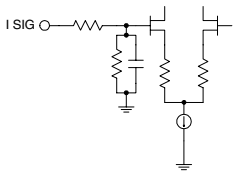
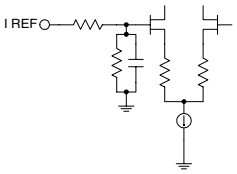
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

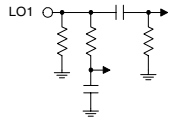
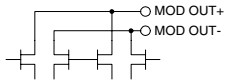
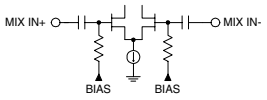
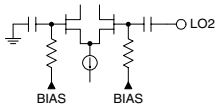
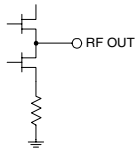
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Modulation Signals (I&Q)					T=25°C, V_{DD}=5V, V_{REF}=2.5V, BB=100kHz, LO1=70MHz, LO2=700MHz, V_{MOD}=3.0V_{PP}, SSB, unless indicated otherwise.
Frequency Range		DC to 50		MHz	
Signal Level		2.2		V_{PP}	For 1dB compression
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Input Impedance to GND		3		kΩ	
Amplitude Balance		0.1		dB	
Quadrature Phase Error		1		°	
First LO Input					
Frequency Range		50 to 150		MHz	For 30dB sideband suppression
		30 to 225		MHz	For 20dB sideband suppression
Power Level		-5 to +6		dBm	
Input Impedance		750-j400		Ω	Without external 50Ω termination
Second LO Input					
Frequency Range		100 to 1000		MHz	
Power Level		-5 to +6		dBm	
Input Impedance		600-j700		Ω	Without external 50Ω termination
RF Output					
Output Power					V_{DD}=5V, LO1,2 level=0dBm, SSB
		+4		dBm	Freq=200MHz to 500MHz
		0		dBm	Freq=500MHz to 800MHz
		-4		dBm	Freq=800MHz to 1000MHz
Output Power					V_{DD}=6V, LO1,2 power=0dBm, SSB
		+6		dBm	Freq=200MHz to 500MHz
		+3		dBm	Freq=500MHz to 800MHz
		-1		dBm	Freq=800MHz to 1000MHz
Nominal Output Impedance		50		Ω	
Output VSWR		1.5:1			Freq<600MHz
		3:1			600MHz<Freq<1000MHz
Output Broadband Noise Power		-155		dBm/Hz	
Spurious					Single sideband modulation
Sideband Suppression		35		dBc	
Carrier Suppression		25		dBc	Unadjusted. Modulation DC offset may be externally adjusted for maximum suppression. See Pin Descriptions.
First LO Harmonics		-20		dBc	Odd unfiltered IF
		-30		dBc	Even unfiltered IF
Power Supply					
Voltage		3 to 6.5		V	Operating limits
Current Consumption		31	35	mA	V_{CC}=5.0V

Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down “ON”		V_{CC}		V	Threshold voltage
Power Down “OFF”		0		V	Threshold voltage

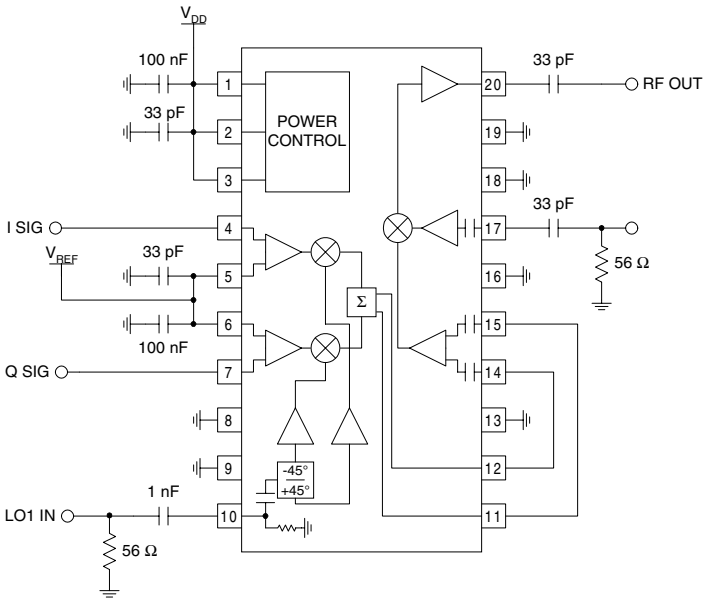
RF2412

Pin	Function	Description	Interface Schematic
1	VDD2	Supply Voltage for the RF Output Stage only. A 33pF external bypass capacitor is required, and an optional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Though the part is designed to run from a 5V supply, it will also work at 4V. Gain and available output power will be reduced by 5dB to 10dB. Pins 1 and 2 may share a common bypass capacitor.	
2	VDD1	Supply Voltage for all circuits but the RF Output Stage. The same comments as for VDD2 apply to this pin. Pins 1 and 2 may share a common bypass capacitor.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when connected to V_{DD}, all circuits are operational. This is a high impedance input, internally connected to the parallel gates of two switching FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. Turn-on voltage of some parts of the circuit may be as low as 0.1V. In order to maximize output power, the voltage on this pin should be as close to V_{DD} as possible during normal operation. A 33pF capacitor is recommended for bypassing. If this pin is not used for power down control, it may be tied to pins 1 and 2, and all three pins may share one 33pF capacitor, provided that the associated trace lengths are minimized.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. A DC reference of approximately $V_{DD}/2$ must be supplied to this pin. The input impedance of this pin is about 3kΩ. The SIG and REF inputs are inputs of a differential amplifier. Therefore, the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF pins also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven differentially to increase conversion gain.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ± 0.15V (relative to the I SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3kΩ.	
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3 kΩ.	Same as pin 5.
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. A DC reference of approximately $V_{DD}/2$ must be supplied to this pin. The input impedance of this pin is about 3 kΩ. Therefore, the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven differentially to increase conversion gain.	Same as pin 4.
8	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
9	GND	Same as pin 8.	

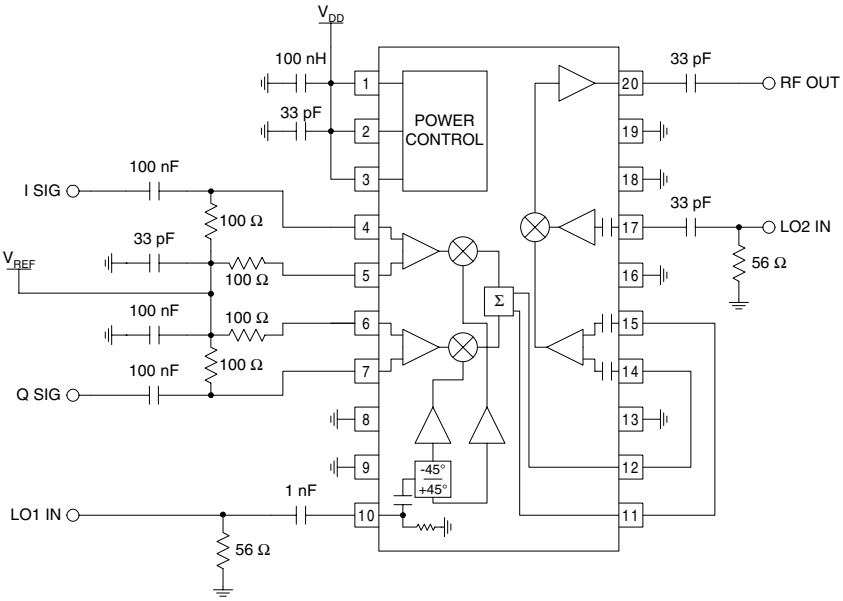
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10	**LO1**	High impedance modulator LO input. If approximately 0dBm of LO power is available, a shunt 56Ω resistor may be used for matching. If the available LO power is approximately -6dBm, then a reactive match may be required. There is an internal blocking capacitor between this pin and the LO circuitry, but not between the pin and an internal resistor to ground (see the functional block diagram). An external blocking capacitor should be provided if the pin is connected to a device with DC present. A DC path to ground (an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 1nF is recommended.	
11	**MOD OUT+**	Balanced IF output port. If no filtering is required this pin can be connected directly to the MIX IN+ pin. This pin is NOT DC blocked and carries DC. A blocking capacitor of 1nF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
12	**MOD OUT-**	Same as pin 11, except complementary output.	See pin 11.
13	**GND**	Same as pin 8.	
14	**MIX IN-**	High impedance balanced input to the IF stage. This pin has an internal DC blocking capacitor. If no IF filter is needed this pin may be connected directly to MOD OUT-. If an IF filter is used, an external shunt resistor to ground may be needed to provide correct matching for the filter.	
15	**MIX IN+**	Same as pin 14, except complementary input.	See pin 14.
16	**GND**	Same as pin 8.	
17	**LO2**	Mixer LO Input port. A shunt 56Ω resistor can be used for matching. This pin has internal DC blocking,	
18	**GND**	Same as pin 8.	
19	**GND**	Same as pin 8.	
20	**RF OUT**	50Ω output. This pin is not internally DC blocked, and an external blocking capacitor of 33pF is required.	

Application Schematic
915 MHz Operation, DC Coupled I and Q Inputs



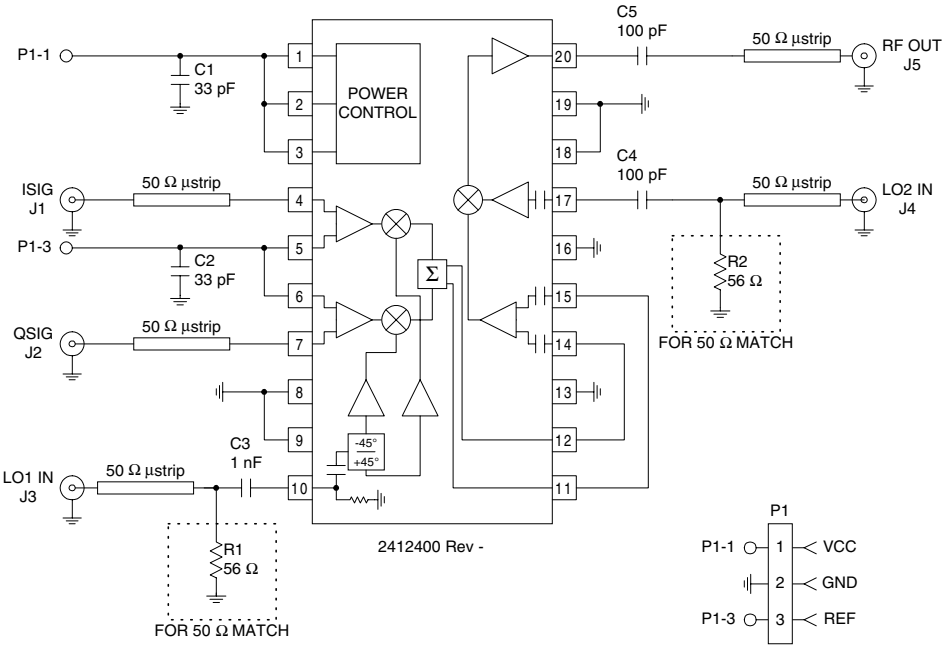
Application Schematic
915 MHz Operation, AC Coupled I and Q Inputs



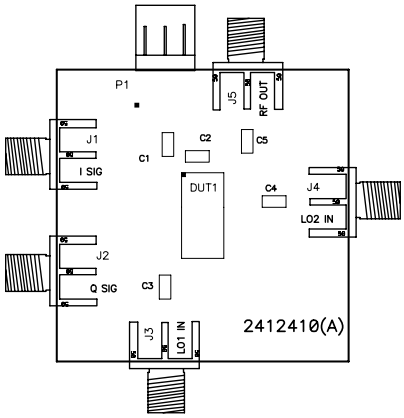
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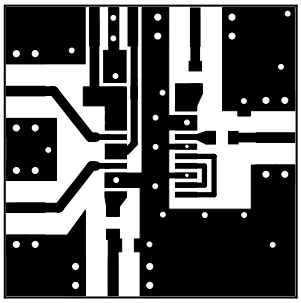
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

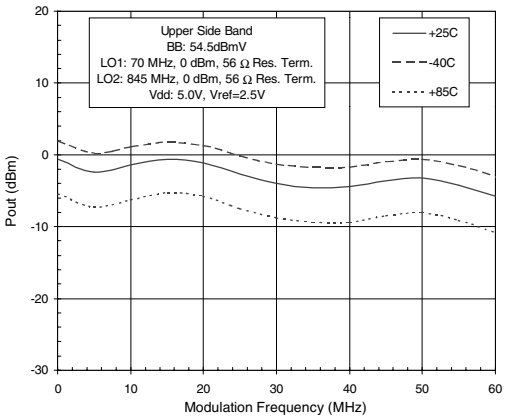


Evaluation Board Layout
1.52” x 1.52”

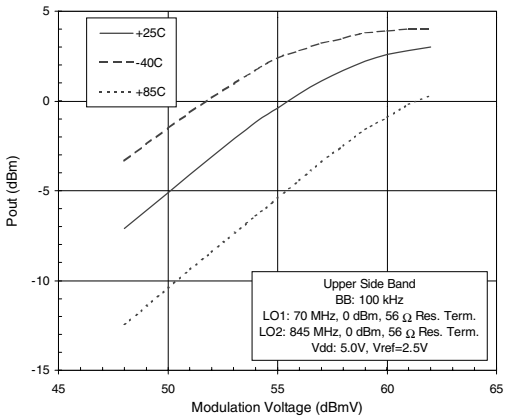




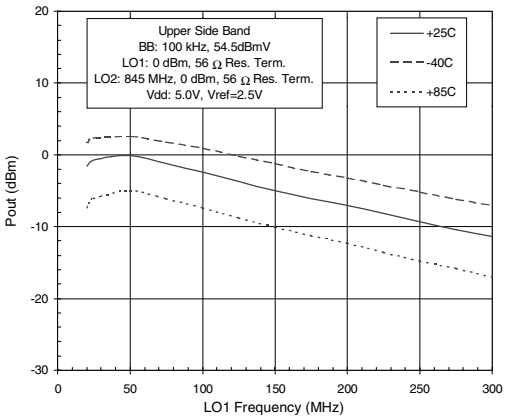
Pout vs. Baseband Modulation Frequency



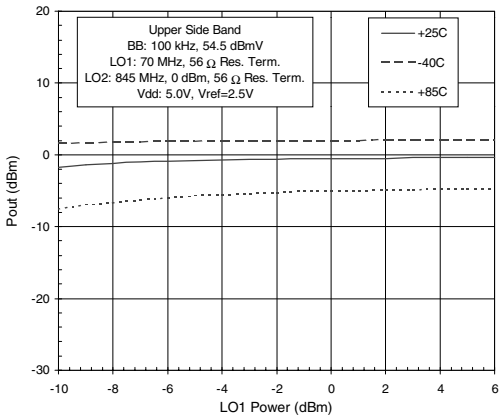
Pout vs. Baseband Modulation Voltage



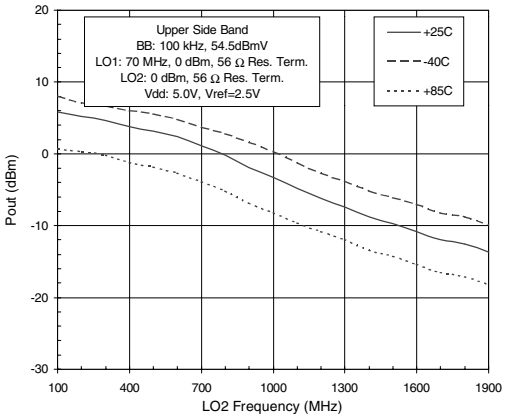
Pout vs. LO1 Frequency



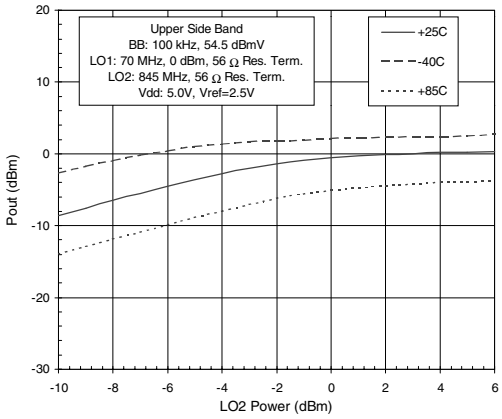
Pout vs. LO1 Power



Pout vs. LO2 Frequency



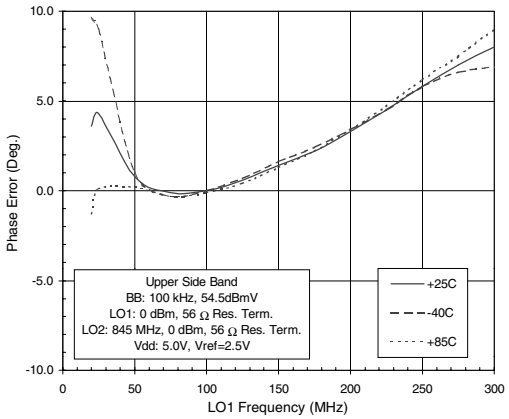
Pout vs. LO2 Power



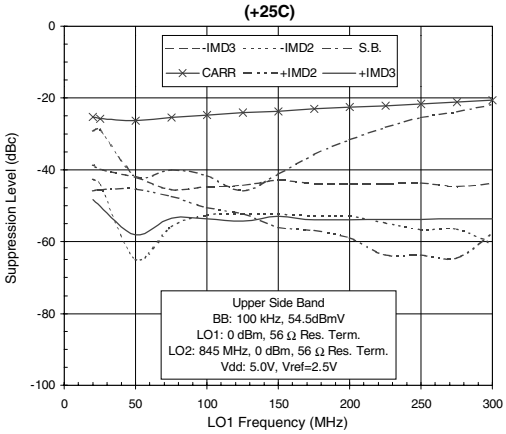
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MODULATORS AND UPCONVERTERS

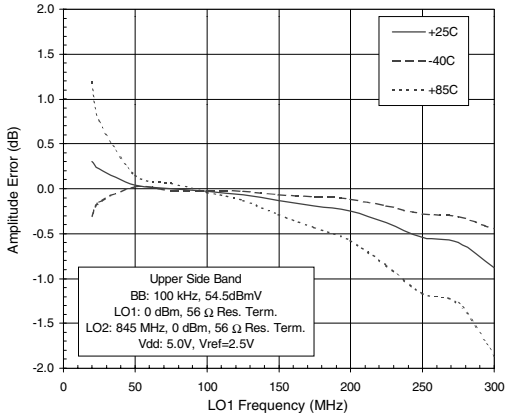
Phase Error vs. LO1 Frequency



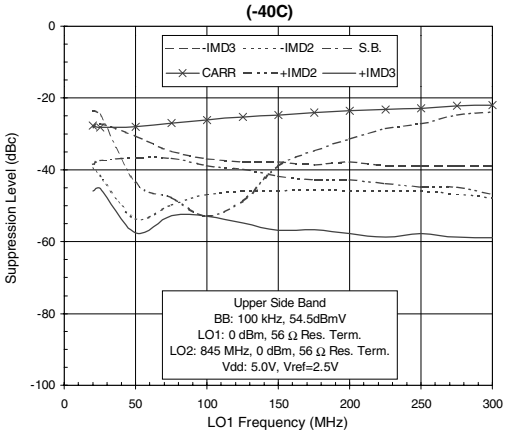
Suppression Levels vs. LO1 Frequency (+25C)



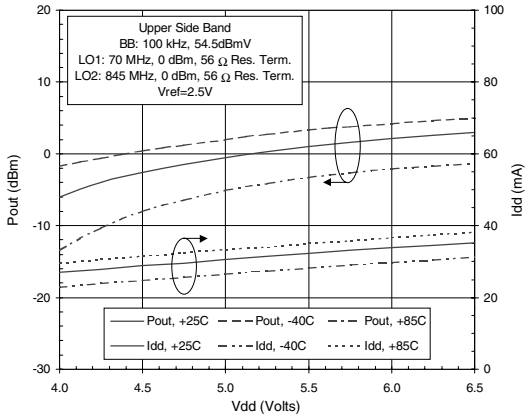
Amplitude Error vs. LO1 Frequency



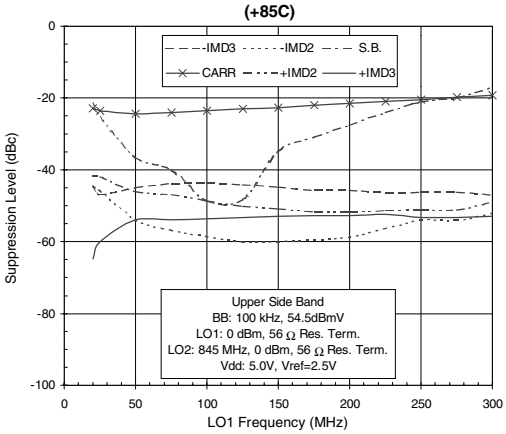
Suppression Levels vs. LO1 Frequency (-40C)



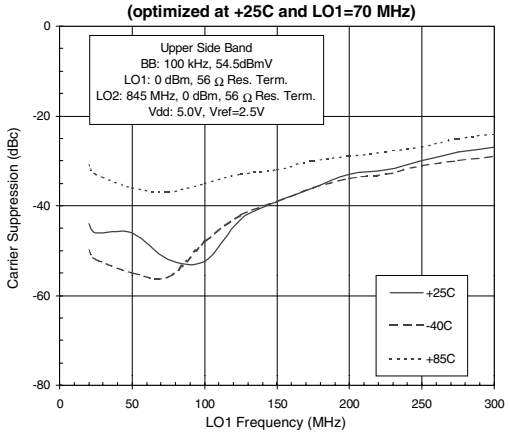
Pout and Idd vs. Vdd



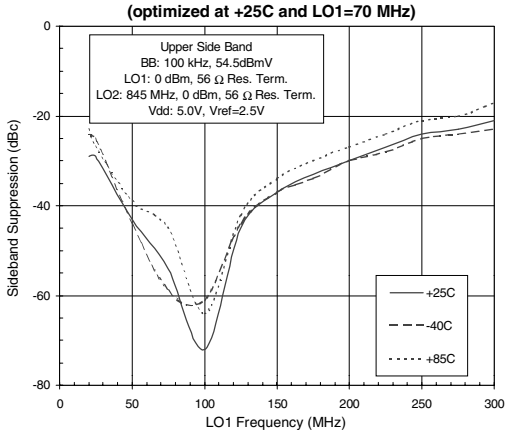
Suppression Levels vs. LO1 Frequency (+85C)



Optimized Carrier Suppression vs. LO1 Frequency (optimized at +25C and LO1=70 MHz)



Optimized Sideband Suppression vs. LO1 Frequency (optimized at +25C and LO1=70 MHz)



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RF2413

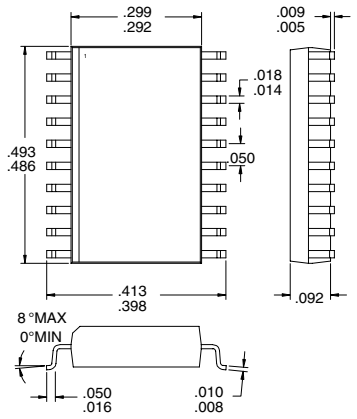
GAIN CONTROLLED DUAL-CONVERSION QUADRATURE MODULATOR

Typical Applications

- Digital and Spread Spectrum Systems
- Analog Communication Systems
- GSM Systems
- CDMA Systems
- General Purpose Frequency Conversion
- Portable Battery Powered Equipment

Product Description

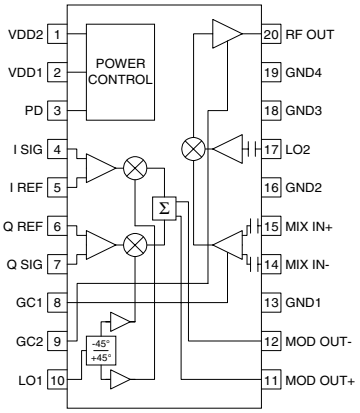
The RF2413 is a monolithic integrated transmitter universal modulation IC capable of generating modulated AM, PM, or compound carriers in the VHF/UHF frequency range. The modulation is performed at VHF, then the resulting spectrum is upconverted to a frequency range between 100MHz and 1000MHz. Up to 60dB of power control is possible through the use of two gain control pins. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining, gain-controlled differential amplifier, a second balanced mixer, and an output gain-controlled RF amplifier which will drive a 50Ω load.



Package Style: SOP-20

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V to 6.5V Power Supply
- Low Broadband Noise Floor
- Excellent Amplitude & Phase Balance
- Digitally Controlled Power Down
- 30MHz to 100MHz IF Frequency
- 200MHz to 1000MHz RF Frequency

Ordering Information

RF2413	Gain Controlled Dual-Conversion Quadrature Modulator
RF2413 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2413

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
I and Q Modulation Levels	V_{DD}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

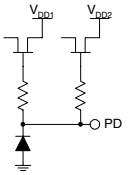
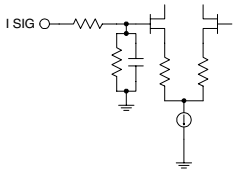
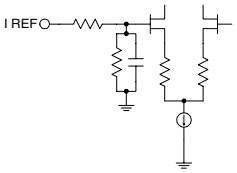
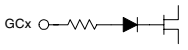
Caution! ESD sensitive device.

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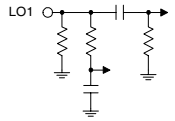
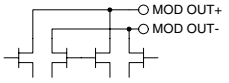
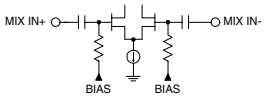
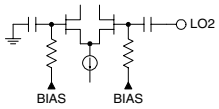
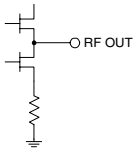
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Modulation Signals (I&Q)					T=25°C, V_{DD}=5V, V_{REF}=2.5V, BB=100kHz, LO1=70MHz, LO2=700MHz, V_{MOD}=3.0V_{PP}, SSB, unless indicated otherwise.
Frequency Range		DC to 25		MHz	
Signal Level		3.0		V_{PP}	For 1dB compression
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Input Impedance		3		kΩ	
Amplitude Balance		0.1		dB	
Quadrature Phase Error		1		°	
First LO Input					
Frequency Range		30 to 200		MHz	For 30dB sideband suppression
		30 to 250		MHz	For 20dB sideband suppression
Power Level		-5 to +6		dBm	
Input Impedance		750-j500		Ω	At 100MHz, without external 50Ω termination
IF Inputs & Outputs (MOD OUT & MIX IN)					
Output Impedance		290-j160		Ω	At 100MHz
		170-j180		Ω	At 200MHz
Input Impedance		6000-j2500		Ω	At 100MHz
		5200-j2800		Ω	At 200MHz
Second LO Input					
Frequency Range		100 to 1000		MHz	
Power Level		0 to +6		dBm	
Input Impedance		2000-j3000		Ω	At 300MHz, without external 50Ω termination
		600-j1400		Ω	At 1000MHz, without external 50Ω termination
RF Output					
Output Power					V_{DD}=6V, LO1,2 power=0dBm, SSB
		+6		dBm	Freq=200MHz to 500MHz
	-2	+2	+5	dBm	Freq=500MHz to 800MHz
		-1		dBm	Freq=800MHz to 1000MHz
Total Gain Control Range		75		dB	Gain 1 and Gain 2
Gain Control Voltage for minimum gain		1.5		V	
Gain Control Voltage for maximum gain		5.0		V	
Nominal Output Impedance		50		Ω	
Output VSWR		1.5:1			Freq<600MHz
		3:1			600MHz<Freq<1000MHz
Output Broadband Noise Power		-155		dBm/Hz	

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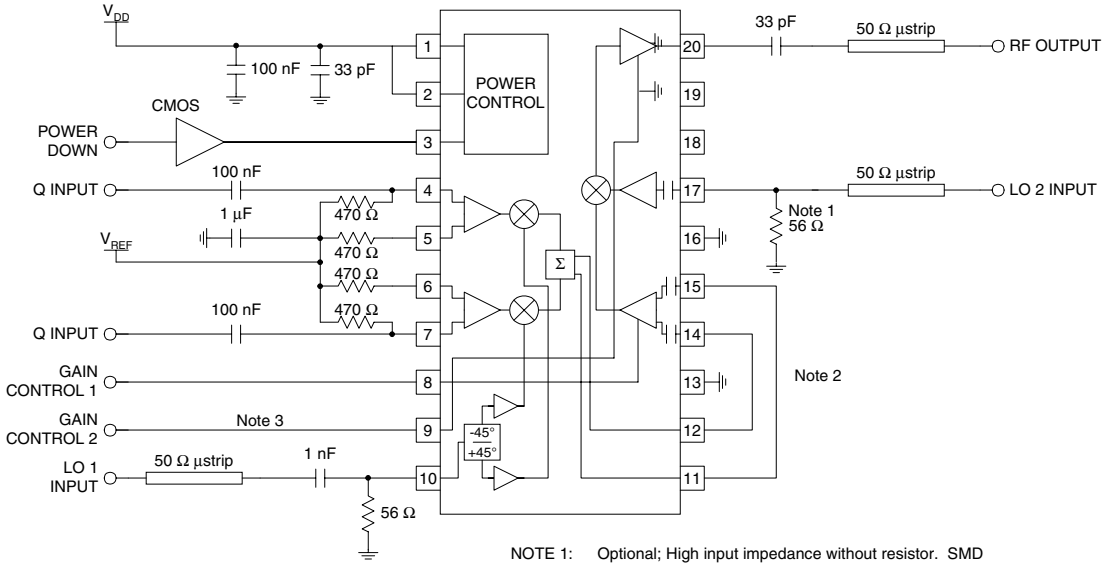
Spurious					Single sideband modulation
Sideband Suppression	30	35		dBc	Unadjusted.
Carrier Suppression	20	25		dBc	Unadjusted. Modulation DC offset may be externally adjusted for maximum suppression. Suppression is then typically 40dBc.
First LO Harmonics		20		dBc	Odd unfiltered IF
		30		dBc	Even unfiltered IF
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down “ON”		V_{CC}		V	Threshold voltage
Power Down “OFF”		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 6.5		V	Operating limits
Current Consumption		35	50	mA	

Pin	Function	Description	Interface Schematic
1	VDD2	Supply Voltage for the RF Output Stage only. A 33pF external bypass capacitor is required and an optional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Though the part is designed to run from a 5V supply, it will work at 3V. Gain and available output power will be reduced by 5 to 10dB. This also means that the part is sensitive to unintended power supply variation. Power supply voltage should be kept constant, or another way of maintaining constant output power is required.	
2	VDD1	Supply Voltage for all circuits except the RF Output Stage. The same comments as for VDD2 apply to this pin.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when this pin is VDD all circuits are operating. This is a high impedance input, internally connected to the gates of a few FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. Turn-on voltage of some parts of the circuit may be as low as 0.1V. In order to maximize output power this pin should be as close to VDD as possible during normal operation.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be VDD2/2. Input impedance of this pin is about 3kΩ.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning it will typically be better than 25dB. Input impedance of this pin is about 3kΩ.	
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3 kΩ.	Same as pin 5.
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be VDD2/2. Input impedance of this pin is about 3kΩ.	Same as pin 4.
8	GC1	Gain control of the IF input amplifier. This pin, when used as the only gain control, will give a 30dB control range. When used together with GC2, a 60dB range is available. When this pin is at 1.8V or lower, the gain is set to the minimum; when this pin is at 3.8V or above, the gain is set to the maximum; see the plot below for typical characteristics. If fixed maximum output level is required, it is recommended to connect this pin to VDD. There are no provisions in the chip for limiting the bandwidth of the gain control, so very fast response times are available. If a slower response is desired, an external capacitor can be added.	
9	GC2	Gain control for the RF output amplifier. This pin has the same control characteristics as GC1.	Same as pin 8.

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10	**LO1**	High impedance modulator LO input. A shunt 56Ω resistor can be used for matching. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 1nF is recommended.	
11	**MOD OUT+**	Balanced IF output port. If no filtering is required this pin can be connected directly to the MIX IN+ pin. This pin is NOT DC blocked and carries DC. A blocking capacitor of 1nF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
12	**MOD OUT-**	Same as pin 11, except complementary output.	See pin 11.
13	**GND1**	Ground connection for all baseband circuits, modulator and the IF buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
14	**MIX IN-**	High impedance balanced input to the gain controlled IF stage. This pin has an internal DC blocking capacitor. If no IF filter is needed, this pin may be connected directly to MOD OUT-. If an IF filter is used, an external shunt resistor to ground may be needed to provide correct matching for the filter.	
15	**MIX IN+**	Same as pin 14, except complementary input.	See pin 14.
16	**GND2**	Ground connection for the limiting LO2 buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
17	**LO2**	Mixer LO Input port. A shunt 56Ω resistor can be used for matching. This pin has internal DC blocking,	
18	**GND3**	Ground connection for the IF mixer and the RF gain control stage. Keep traces physically short and connect immediately to ground plane for best performance.	
19	**GND4**	Ground connection for the RF output stage. Keep traces physically short and connect immediately to ground plane for best performance.	
20	**RF OUT**	50Ω output. This pin is not internally DC blocked, and an external blocking capacitor of 100pF is required.	

Application Schematic



NOTE 1: Optional; High input impedance without resistor. SMD resistor mounted adjacent to package pin, grounded through via to the ground plane.

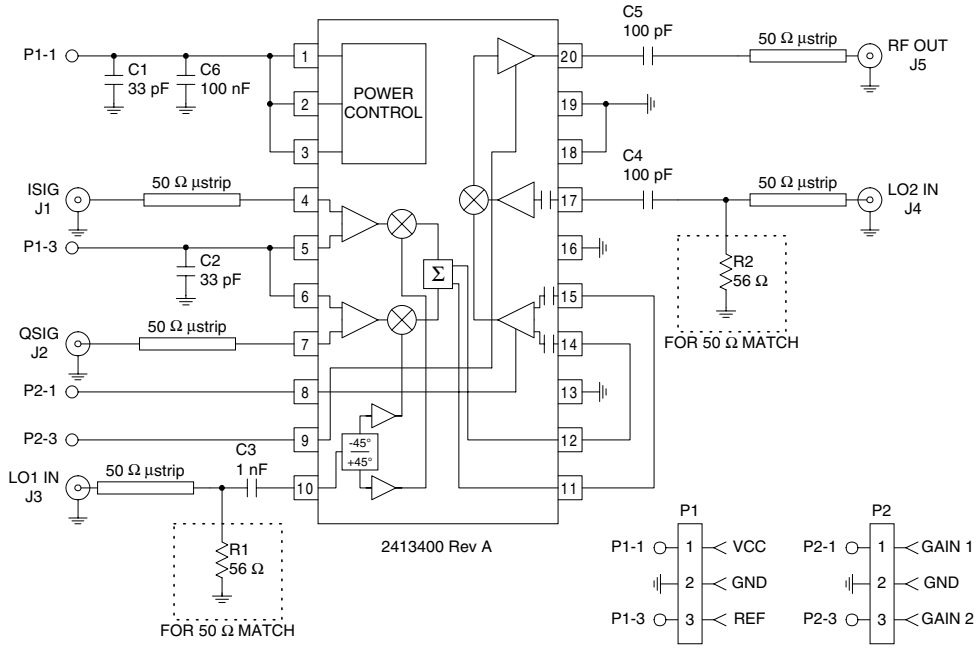
NOTE 2: If no IF filter is needed, tie pins 11, 12, 14, and 15 as shown. Otherwise insert the filter and the matching network.

NOTE 3: Gain control pins (8 and 9) may be tied together directly.

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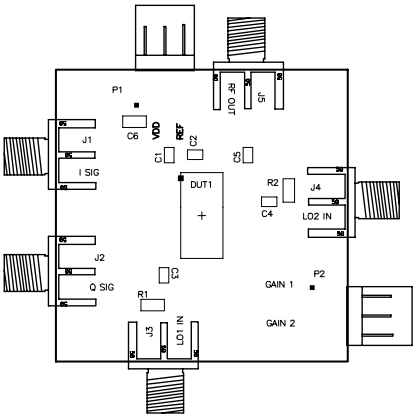
Evaluation Board Schematic

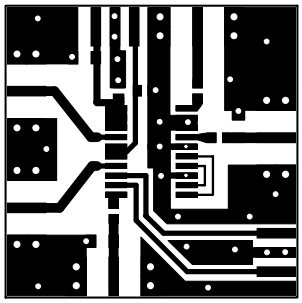
(Download Bill of Materials from www.rfmd.com.)



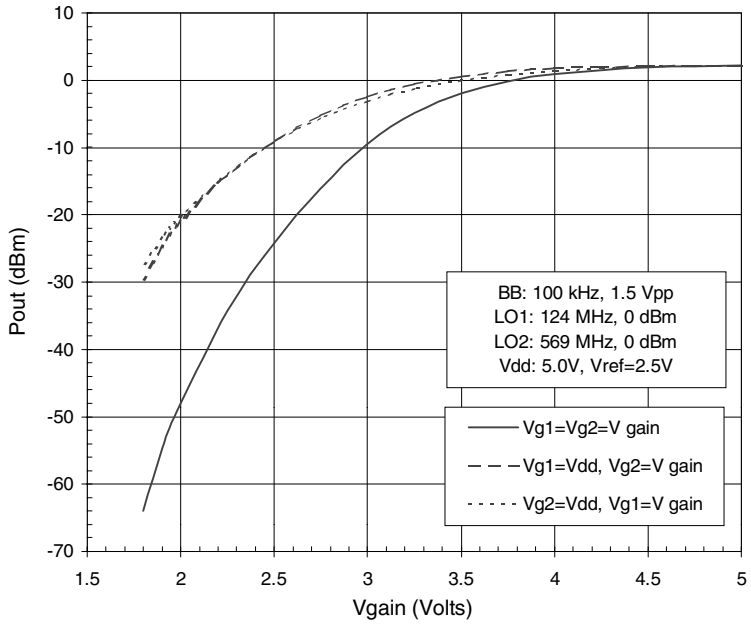
Evaluation Board Layout
1.52” x 1.52”

Board Size 0.039”; Board Material FR-4; Multi-Layer





Pout vs. Gain Control Voltages



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RF2422

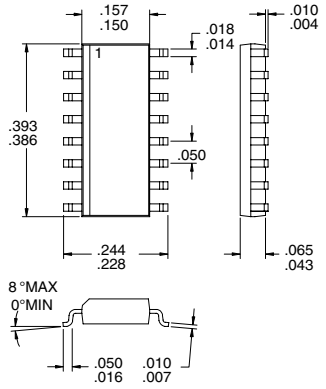
2.5GHZ DIRECT QUADRATURE MODULATOR

Typical Applications

- Digital Communications Systems
- Spread Spectrum Communication Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- GSM, DCS 1800, JDC, D-AMPS Systems
- Commercial and Consumer Systems

Product Description

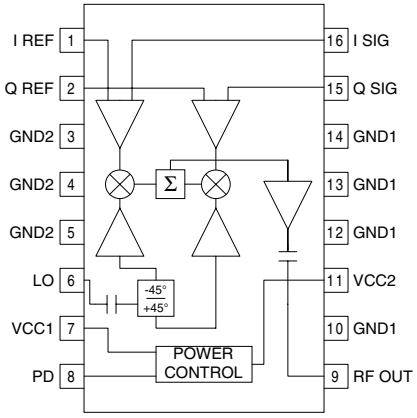
The RF2422 is a monolithic integrated quadrature modulator IC capable of universal direct modulation for high-frequency AM, PM, or compound carriers. This low-cost IC implements differential amplifiers for the modulation inputs, 90° carrier phase shift network, carrier limiting amplifiers, two matched double-balanced mixers, summing amplifier, and an output RF amplifier which will drive 50Ω from 800MHz to 2500MHz. Component matching, which can only be accomplished with monolithic construction, is used to full advantage to obtain excellent amplitude balance and phase accuracy.



Package Style: SOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 5V Power Supply
- Integrated RF Quadrature Network
- No Tuning Required
- Low LO Input Level
- Digitally Controlled Power Down Mode
- 800MHz to 2500MHz Operation

Ordering Information

RF2422	2.5GHz Direct Quadrature Modulator
RF2422 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2422

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

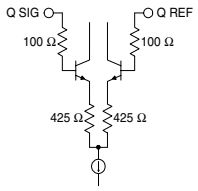
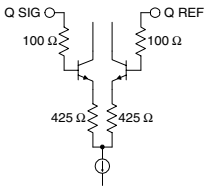
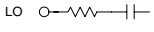
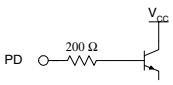
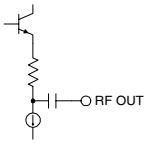
Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input					T=25°C, V_{CC}=5V
Frequency Range		800 to 2500		MHz	
Power Level		-6 to +6		dBm	
Input VSWR		5:1			At 900MHz
		1.8:1			At 1800MHz
		1.2:1			At 2500MHz
Modulation Input					
Frequency Range		DC to 250		MHz	
Reference Voltage (V_{REF})		3.0		V	
Maximum Modulation (I&Q)			V_{REF}±1.0	V	
Gain Asymmetry		0.2		dB	
Quadrature Phase Error		3		°	
Input Resistance		30		kΩ	
Input Bias Current			40	µA	
RF Output					LO=2GHz and -5dBm, I&Q=2.0V_{PP}, SSB
Output Power	-3		+3	dBm	
Output Impedance		50		Ω	
Output VSWR		3.5:1			At 900MHz
		1.3:1			At 2000MHz
		1.15:1			At 2500MHz
Harmonic Output	-30	-35		dBc	
Broadband Noise Floor		-135		dBm/Hz	
Sideband Suppression	25	35		dB	
Carrier Suppression	30	35		dB	
IM_3 Suppression	30	35		dB	Intermodulation of the carrier and the desired RF signal
	25	30		dB	Intermodulation of baseband signals
Broadband Noise Floor					At 20MHz offset, V_{CC}=5V. Tied to V_{REF}: ISIG, QSIG, IREF, and QREF.
		-145		dBm/Hz	At 850MHz
		-152		dBm/Hz	At 1900MHz
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Control “ON”			2.8	V	Threshold voltage
Power Control “OFF”	1.0	1.2		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		4.5 to 6.0		V	Operating Limits
Current		45	50	mA	Operating
			25	µA	Power Down

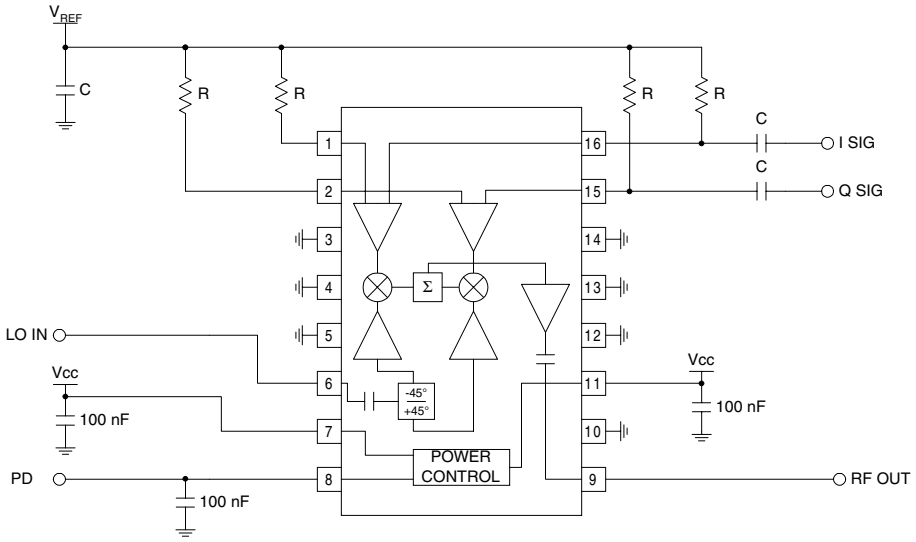
5 MODULATORS AND UPCONVERTERS

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Pin	Function	Description	Interface Schematic
1	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. A voltage of 3.0V is recommended. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	
2	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. A voltage of 3.0V is recommended.	
3	GND2	Ground connection of the LO phase shift network. This pin should be connected directly to the ground plane.	
4	GND2	Same as pin 3.	
5	GND2	Same as pin 3.	
6	LO	The input of the phase shifting network. This pin has an internal DC blocking capacitor. At frequencies higher than 2GHz this port is well-matched to 50Ω. This port is voltage driven so matching at lower frequencies is not required.	
7	VCC1	Power supply for all circuits except the RF output stage. An external capacitor is needed if no other low frequency bypass capacitor is nearby.	
8	PD	Power Down control. When this pin is "low", all circuits are shut off. A "low" is typically 1.2V or less at room temperature.When this pin is "high" (V_{CC}), all circuits are operating normally. If PD is below V_{CC}, output power and performance will be degraded. Operating in this region is not recommended, although it might be useful in some applications where power control is required.	
9	RF OUT	This is the 50Ω RF Output. This pin has an internal DC blocking capacitor. At frequencies higher than 2GHz this port is well-matched. Typical impedances at lower frequencies are: 24-j30 Ω @ 1GHz, 27-j10 Ω @ 1.4GHz, 31-j3 Ω @ 1.8GHz. At those frequencies, external matching may be needed to optimize output power.	
10	GND3	Ground connection for the RF output stage. This pin should be connected directly to the ground plane.	
11	VCC2	Power supply for the RF Output amplifier. An external capacitor is needed if no other low frequency bypass capacitor is near by.	
12	GND1	Ground connection for the LO and baseband amplifiers, and for the mixers. This pin should be connected directly to the ground plane.	
13	GND1	Same as pin 12.	
14	GND1	Same as pin 12.	
15	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 2V. The recommended DC level for this pin is 3.0V. The peak minimum voltage on this pin (V_{REF} - peak modulation amplitude) should never drop below 2.0V. The peak maximum voltage on this pin (V_{REF} + peak modulation amplitude) should never exceed 4.0V.	See pin 2.

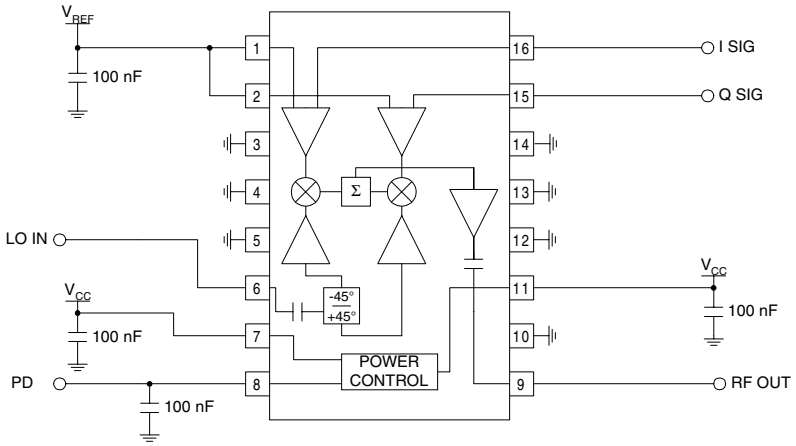
Pin	Function	Description	Interface Schematic
16	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 2V. The recommended DC level for this pin is 3.0V. The peak minimum voltage on this pin (V_{REF} - peak modulation amplitude) should never drop below 2.0V. The peak maximum voltage on this pin (V_{REF} + peak modulation amplitude) should never exceed 4.0V.	See pin 1.

Application Schematic
AC Coupled



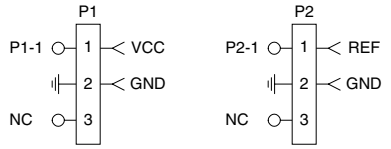
NOTE: The values of R and C depend on the minimum baseband frequency. I.e., the cutoff frequency of this high pass filter should be lower than the lowest frequency component in the I/Q spectrum.

Application Schematic
DC Coupled

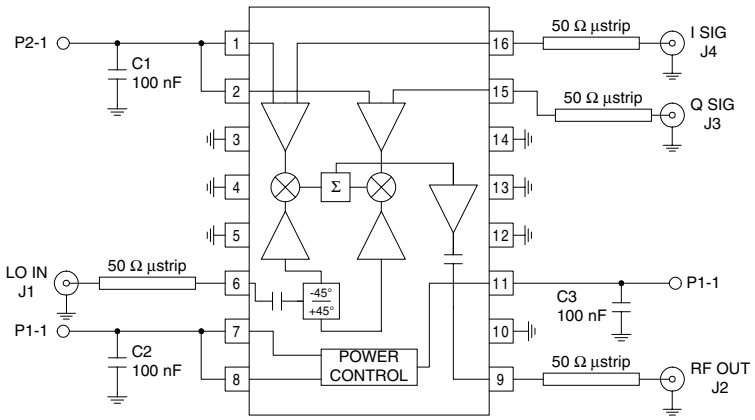


Evaluation Board Schematic
1.5” x 1.5”

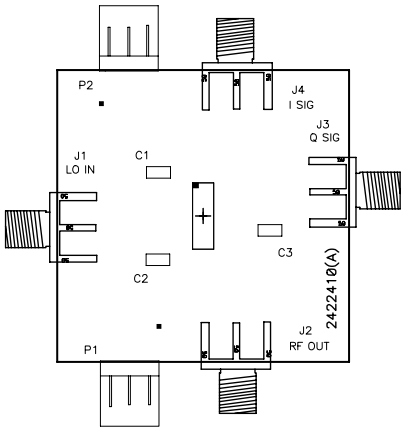
(Download Bill of Materials from www.rfmd.com.)

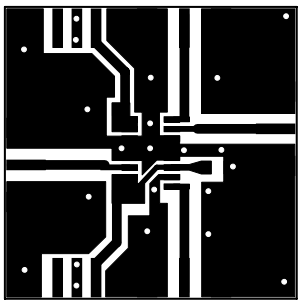


2422400 Rev A



Evaluation Board Layout





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RF2423

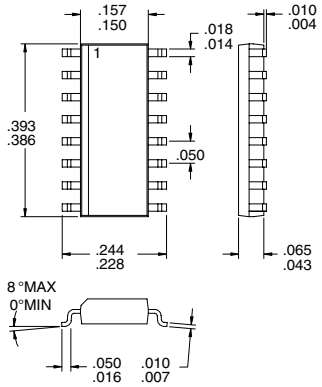
100mW SPREAD-SPECTRUM TRANSMITTER IC

Typical Applications

- Digital and Analog Communication Systems • GMSK, QPSK, DQPSK, QAM Modulation
- Spread Spectrum Communication Systems • AM, SSB, DSB Modulation
- Portable Battery Powered Equipment

Product Description

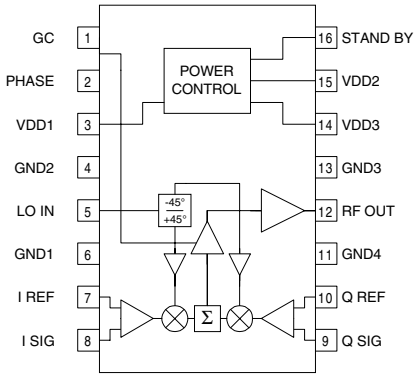
The RF2423 is a monolithic integrated transmitter IC capable of universal direct modulation for UHF AM, PM, or compound carriers. The transmitter may be used stand-alone for applications requiring not more than 100mW output power, or may be used to drive a final power amplifier. The maximum output level is 100mW, and is adjustable over a 25dB range by a single positive voltage. This low-cost IC implements differential amplifiers for the modulation inputs, 90 degree carrier phase shift network, carrier limiting amplifiers, two matched doubly-balanced mixers, variable gain summing amplifier for level control, and 100mW linear (class AB) output amplifier.



Package Style: SOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 5V Power Supply
- 100mW Output Power Into 50Ω
- 25dB Gain Control Range
- Excellent Phase & Amplitude Balance
- Digitally Controlled Stand-By Mode
- 800MHz to 1000MHz Operation

Ordering Information

RF2423	100mW Spread-Spectrum Transmitter IC
RF2423 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2423

Absolute Maximum Ratings

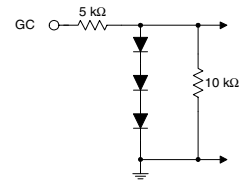
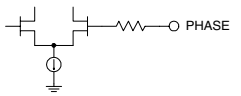
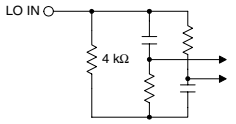
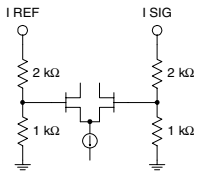
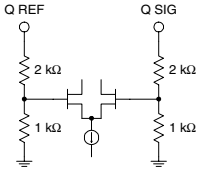
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Down Voltage (V_{PD})	V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

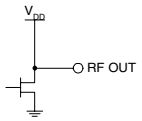
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input (LO IN)					T=25°C, V_{DD}=5.3V, V_{GC}=5.3V
Frequency Range		800 to 1000		MHz	
Power Level		0 to +6		dBm	
Input Impedance		55-j120		Ω	915MHz
Modulation Input					
Frequency Range		DC to 100		MHz	
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Modulation for 100mW Output Power (I & Q)		V_{REF}±2		V	
Maximum Modulation (I & Q)		V_{REF}±2.5		V	
Quadrature Phase Error		±3		°	
Input Impedance		3000		Ω	
DC Offset (I & Q)		40	200	mV	
RF Output					V_{DD}=5.3V, VGC=5.3V, LO power=0dBm, LO frequency=915MHz, SSB, I/Q=2.0V_P sine wave, V_{REF}=3V
Output Power	+22	+22		dBm	
	-15	-10	+5	dBm	V_{GAIN}=0V
Output Impedance		50		Ω	
Output VSWR		2:1			
Second Harmonic Output		-45		dBc	
Other Harmonics Output		<-20		dBc	
Sideband Suppression	25	35		dB	
Carrier Suppression	22	30		dB	Modulation DC offset can be externally adjusted for optimum suppression. Carrier suppression is then typically better than 40dB.
Output Level Control					
Control Range		25		dB	
Control Voltage		1 to 4		V	
Control Input Current		<1.5		mA	
Standby Mode					
Turn On/Off Time		<100		ns	
STANDBY Input Impedance		>50		kΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage; Part is turned "ON"
Power Down "OFF"		0		V	Threshold voltage; Part is turned "OFF"
Power Supply					
Voltage		5		V	Specifications
		4.5 to 6.0		V	Operating limits
Current	60	110	170	mA	Total, 100mW output power
		50		mA	Total, minimum output power
		2	20	mA	Standby mode

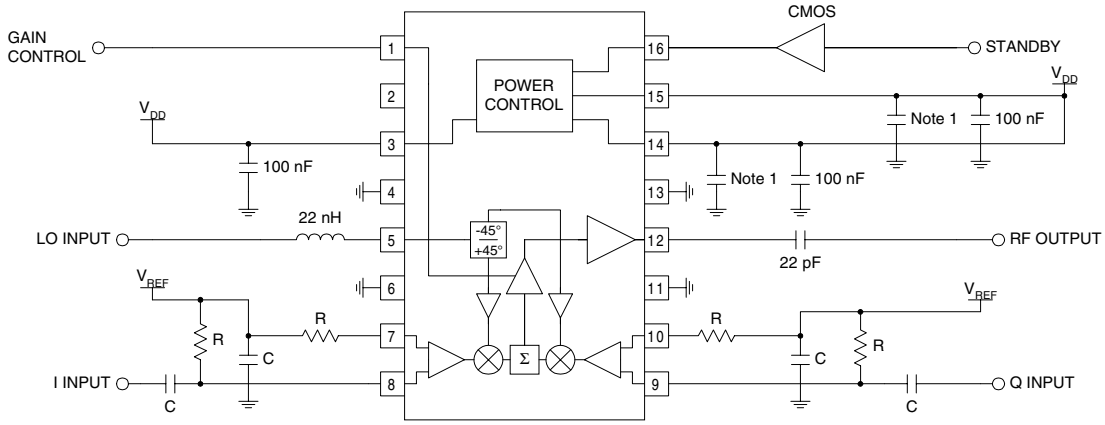
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Pin	Function	Description	Interface Schematic
1	GC	Gain control of the RF amplifier. This pin can be used to control the output power over a 25dB range. Output power is the lowest when the control voltage is 1V or lower, and the highest when set to 4V or higher. When a fixed maximum output level is needed, it is recommended to connect this pin to VDD.	
2	PHASE	This pin adjusts the phase of the I/Q signals. However, the control is very sensitive and hard to control. Control voltage change for a few degrees adjustment is in the order of 10mV. Device to device and temperature variation are not characterized. Therefore it is not recommended to use this pin; leave it not connected. Do NOT connect it to ground. For compensating large errors in the I/Q signals supplied to the device or in control loops, this pin may prove useful.	
3	VDD1	Power supply to all circuits except the RF output stages. It is recommended to put some RF decoupling on this pin, though it is not critical. An optional 0.1µF capacitor is required if no other low frequency bypass capacitor is nearby.	
4	GND2	Ground connection for the gain controlled RF amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LO IN	Modulator LO input. A series 22nH inductor can be used for matching. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 33pF is recommended.	
6	GND1	Ground connection for the baseband, LO and mixer circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
7	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, it will typically be better than 25dB. Input impedance of this pin is about 3kΩ.	
8	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be VDD2/2. Input impedance of this pin is about 3kΩ.	
9	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be VDD2/2. Input impedance of this pin is about 3kΩ.	
10	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning it will typically be better than 25dB. Input impedance of this pin is about 3kΩ.	

11	GND4	Ground connection for the RF driver and output stage. Keep traces physically short and connect immediately to ground plane for best performance. Having a good ground connection on this pin is extremely important due to the high RF levels in the circuits connected to this pin.	
12	RF OUT	50Ω RF output. This pin is not internally DC blocked and an external blocking capacitor of 22pF is needed.	
13	GND3	Ground connection for the RF driver and output stage. Keep traces physically short and connect immediately to ground plane for best performance. Having a good ground connection on this pin is extremely important due to the high RF levels in the circuits connected to this pin.	
14	VDD3	Power supply for the RF output stage. A 33pF external bypass capacitor is required and an optional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Having good bypassing on this pin is especially important because of the high levels of RF signal on the circuits connected to this pin.	
15	VDD2	Power supply for the RF driver stage. A 33pF external bypass capacitor is required and an optional 0.1µF will be required if no other low frequency bypass capacitors are near by. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Having good bypassing on this pin is especially important because of the high levels of RF signal on the circuits connected to this pin.	
16	STANDBY	Standby mode control. When this pin is 0V all circuits are turned off, and when this pin is VDD all circuits are operating. This is a high impedance input, internally connected to the gate of a few transistors. To minimize current consumption in power down mode, this pin should be as close to 0 V as possible, or even a little negative. Turn-on voltage of some parts of the circuit may be as low as 0.0 V. In order to maximize output power this pin should be as close to VDD as possible during normal operation.	

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Application Schematic

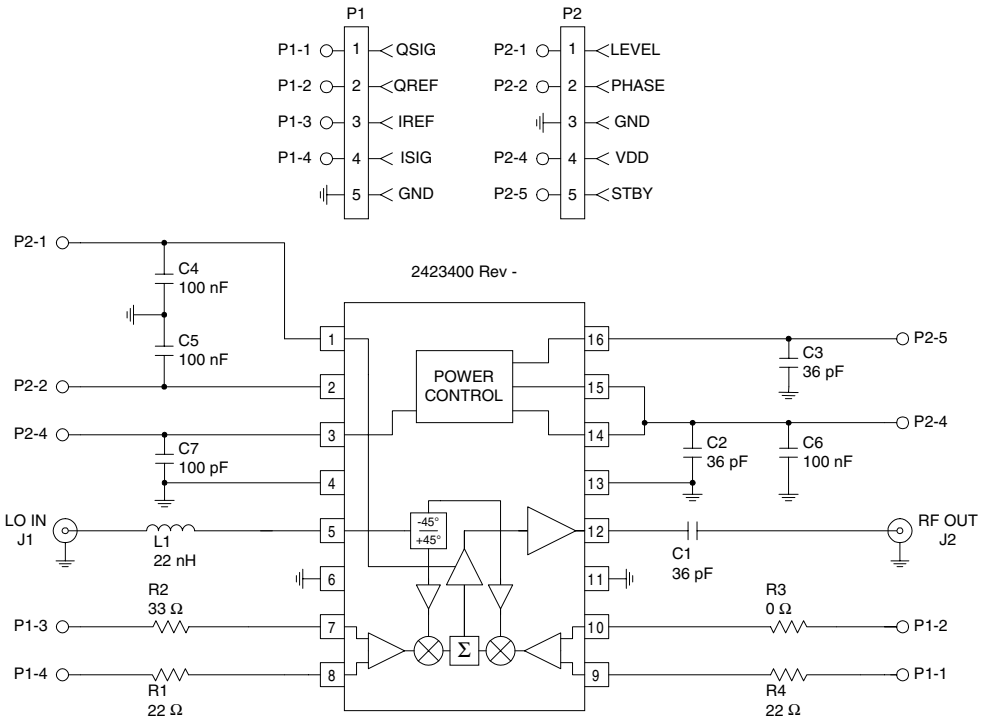


NOTE 1: 33 pF SMD capacitor mounted as close to the package pin as possible, grounded through via to the ground plane with minimum inductance.

NOTE 2: The values of R and C depend on the lowest frequency of the baseband signal.

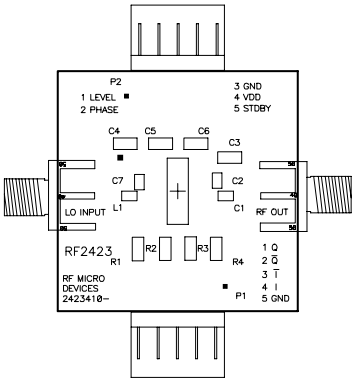
Evaluation Board Schematic

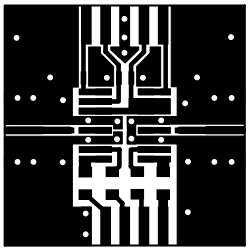
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
1.25” x 1.25”

Board Thickness 0.031”; Board Material FR-4





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RF2424

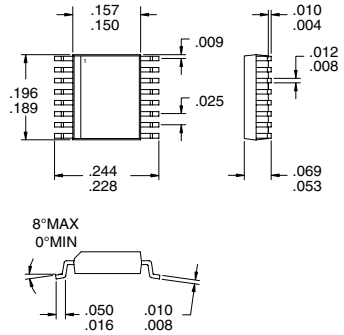
UHF QUADRATURE MODULATOR

Typical Applications

- Digital Communications Systems
- Spread Spectrum Communication Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- GSM and D-AMPS Systems
- AM, SSB, DSB Modulation
- Image-Reject Upconverters

Product Description

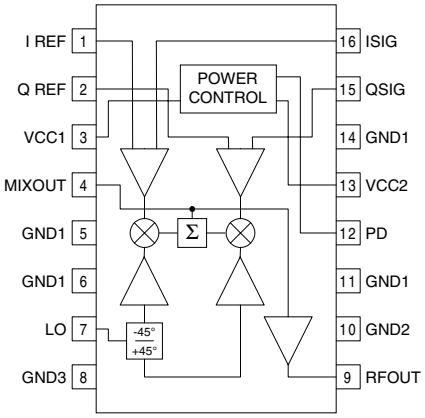
The RF2424 is a monolithic integrated quadrature modulator IC capable of universal direct modulation for high-frequency AM, PM, or compound carriers. Maximum output power is +7.5dBm, which is achieved with low input I and Q signal levels. This low-cost IC implements differential amplifiers for the modulation inputs, 90° carrier phase shift network, carrier limiting amplifiers, two matched double-balanced mixers, summing amplifier, and an output RF amplifier which will drive 50Ω from 700MHz to 1000MHz.



Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: SSOP-16



Functional Block Diagram

Features

- Single 2.7V to 5.5V Power Supply
- +7.5dBm Output Power
- No Tuning Required
- Low LO Input Level
- Digitally Controlled Power Down Mode
- 700MHz to 1000MHz Operation

Ordering Information

RF2424	UHF Quadrature Modulator
RF2424 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

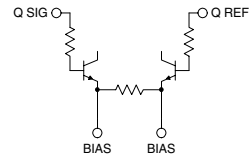
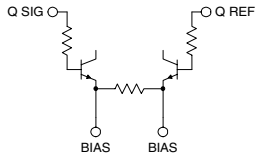
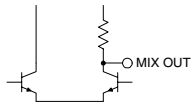
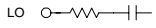
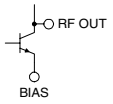
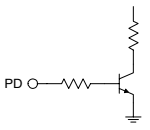
Parameter	Rating	Unit
Supply Voltage	TBD	V_{DC}
Input LO and RF Levels	TBD	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input					T=25 °C, V_{CC}=3V
Frequency Range		700 to 1000		MHz	
Power Level		-6 to +6		dBm	
Input impedance		43 + j1.8		Ω	At 900MHz
Modulation Input					
Frequency Range		DC to TBD		MHz	
Reference Voltage (V_{REF})		1.6		V	
Maximum Modulation (I&Q)		V_{REF} ± 0.3		V	
Gain Asymmetry		0.2		dB	
Quadrature Phase Error		1		°	
Input DC Resistance		40		kΩ	
Input Bias Current		40		µA	
RF Output					V_{CC}=3V, LO power=-3dBm, LO freq=900MHz, I/Q drive level=0.2V_P, SSB
Output Power		+7.5		dBm	
Output Impedance		50		Ω	
Broadband Noise Floor		-140		dBm/Hz	
Sideband Suppression	25	35		dB	
Carrier Suppression	25	30		dB	
IM_3 Suppression	25	30		dB	DSB output (+9dBm total power)
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>10		kΩ	
Power Down "ON"		V_{CC}		V	
Power Down "OFF"	1.0	1.2		V	
Power Supply					
Voltage		2.7 to 5.5		V	
Current		45		mA	V_{CC}=3V
		53		mA	V_{CC}=5V
			10	µA	

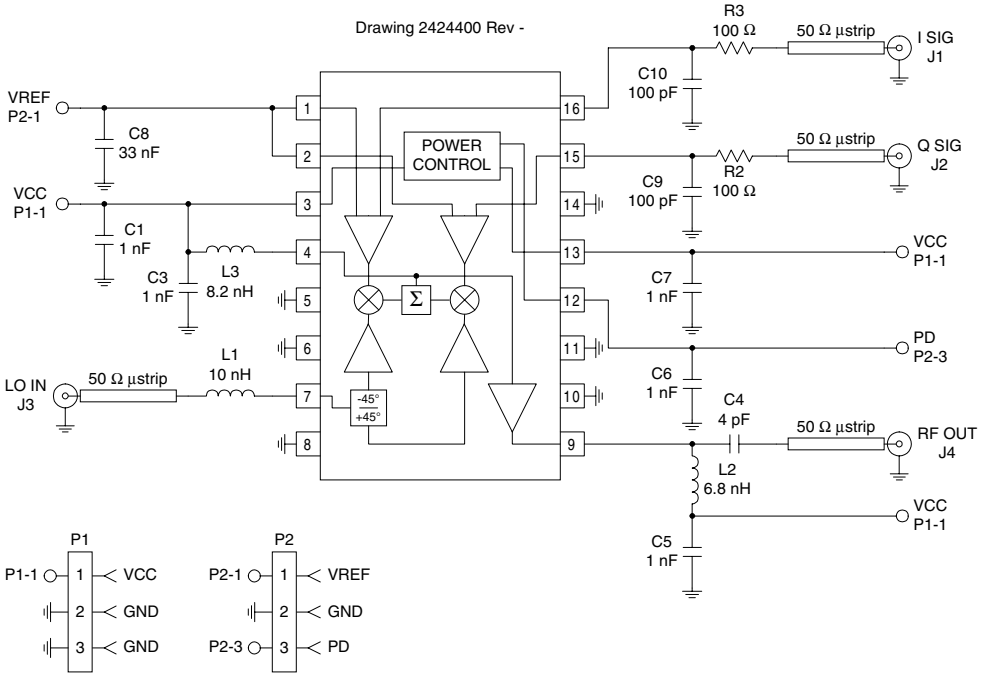
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Pin	Function	Description	Interface Schematic
1	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. A voltage of 1.6V is recommended. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. If single ended operation is desired then the input is applied to I SIG, pin 16. In that case, I REF and Q REF are tied together and AC coupled to ground. To obtain a carrier suppression of better than 40dB, I REF may be tuned ±20mV relative to the I SIG. Without tuning, it will typically be better than 25dB.	
2	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. A voltage of 1.6V is recommended. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the Q SIG and Q REF pins, the I SIG and I REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. If single ended operation is desired then the input is applied to Q SIG, pin 15. In that case, Q REF and Q REF are tied together and AC coupled to ground. To obtain a carrier suppression of better than 40dB, Q REF may be tuned ±20mV relative to the Q SIG. Without tuning, it will typically be better than 25dB.	
3	VCC1	Power supply for the I mixer, Q mixer and the RF Output amplifier.	
4	MIX OUT	MIXOUT: Combined output of the I mixer and Q mixer. By changing the inductor value, maximum RF output is tuned to different frequency. If the inductor value is changed, the RF output match needs to be adjusted for 50Ω output impedance.	
5	GND1	Ground connection for the LO and baseband amplifiers and mixers.	
6	GND1	Same as pin 5.	
7	LO IN	The input of the phase shifting network.	
8	GND3	Ground connection for the LO phase shift network.	
9	RF OUT	RF Output. An external LC matching network is needed for a 50Ω match.	
10	GND2	Ground connection for the RF output stage.	
11	GND1	Same as pin 5.	
12	PD	Power Down control. When this pin is “low”, all circuits are shut off.	
13	VCC2	Power supply for all circuits except mixers and output amplifier.	
14	GND1	Same as pin 5.	
15	Q SIG	Baseband input to the Q mixer. Maximum output power is obtained when the input signal has a peak to peak amplitude of 400mV. The DC level for this pin is 1.6V, same as QREF.	See pin 2.
16	I SIG	Baseband input to the Q mixer. Maximum output power is obtained when the input signal has a peak to peak amplitude of 400mV. The DC level for this pin is 1.6V, same as QREF.	See pin 1.

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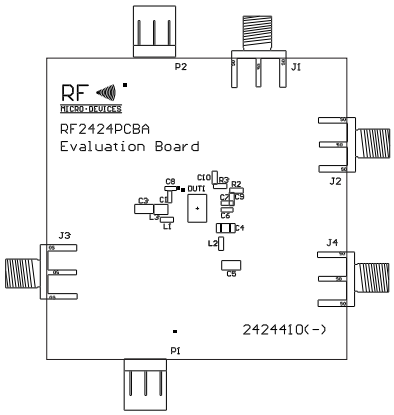
Evaluation Board Schematic

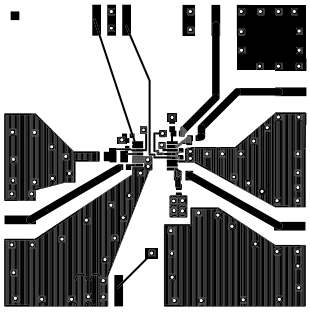
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Evaluation Board Layout
2” x 2”





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RF2454

VHF QUADRATURE MODULATOR

Typical Applications

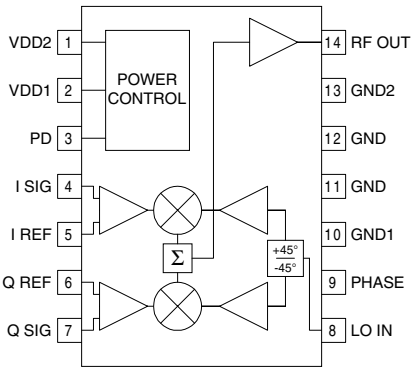
- Digital and Spread Spectrum Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- Private Mobile Radio Systems
- AM, SSB, DSB Modulation
- Image-Reject Upconverters

Product Description

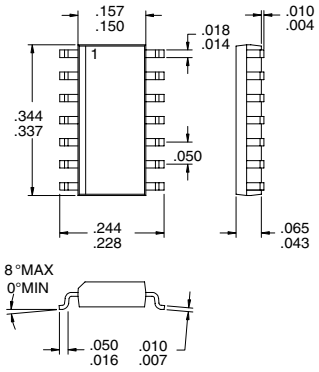
The RF2454 is a monolithic integrated universal modulation system capable of generating modulated AM, PM, or compound carriers in the VHF and UHF frequency range. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining amplifier, and an output RF amplifier which will drive a 50Ω load. Component matching, which can only be accomplished with monolithic construction, is used to full advantage to obtain excellent amplitude balance and high phase accuracy. The unit features low power consumption, single power supply operation and adjustment free operation with no external parts required to operate the part as specified.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Single 3V to 5V Power Supply
- Low Power and Small Size
- CMOS Compatible Power Down Control
- Excellent Amplitude and Phase Balance
- Low Broadband Noise Floor
- 200MHz to 600MHz Operation

Ordering Information

RF2454	VHF Quadrature Modulator
RF2454 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

5 MODULATORS AND UPCONVERTERS

RF2454

Absolute Maximum Ratings

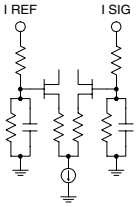
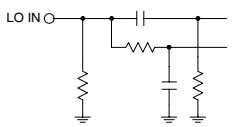
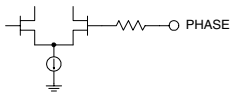
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Down Voltage	-0.5 to V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

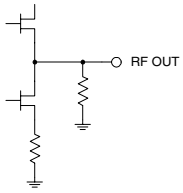
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LO Input					T=25°C, V_{DD}=5V_{DC}, I&Q inputs=2V_{PP}
Frequency Range		200 to 600		MHz	
Power Level		-3 to +6		dBm	
Input VSWR		1.2:1			With external 50Ω termination; see application schematic, note A.
Input Impedance		86-j242		Ω	At 200MHz, without external 50Ω termination.
		63-j139			At 400MHz, without external 50Ω termination.
		50-j106			At 600MHz, without external 50Ω termination.
Modulation Input					
Frequency Range		DC to 100		MHz	
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Modulation (I&Q)		V_{REF}±0.7		V	I & Q signals for 0dBm output power.
Modulation (I&Q)		V_{REF}±1.5		V	I & Q signals for +5dBm output power.
Maximum Modulation (I&Q)		V_{REF}±2.5		V	In-phase and quadrature signals.
Input Resistance		3000		Ω	
DC Offset		50	150	mV	I_{SIG}-I_{REF} and Q_{SIG}-Q_{REF}; to achieve maximum carrier suppression.
Amplitude Error (I/Q)		0.2		dB	
Quadrature Phase Error		±1	±3	°	From 350MHz to 450MHz.
RF Output					V_{DD}=5V, LO Power=0dBm, LO Freq=400MHz, SSB, I&Q input=0.7V_{PP}
Output Power	-1	+1	+3	dBm	
Output Impedance		50			
Output VSWR		1.5:1			
Broadband Noise Floor		-140		dBm/Hz	
Sideband Suppression		25	>40	dB	
Carrier Suppression	18	25	>40	dB	Modulation DC offset can be externally adjusted for optimum suppression. Suppression is typically better than 25dB without adjustment.
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>1		MΩ	
Power "ON"		V_{CC}		V	Threshold voltage
Power "OFF"		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 5.5		V	Operating Limits
Current		28	39	mA	Operating
		0.5	2	mA	Power Down

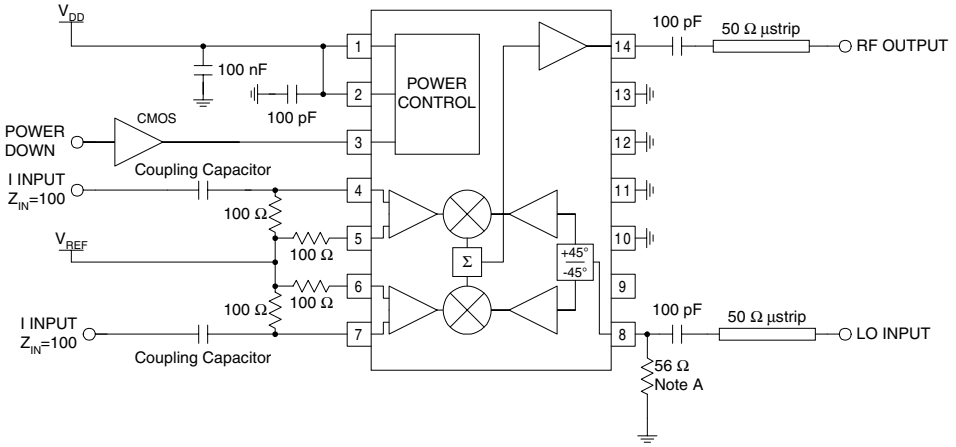
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Pin	Function	Description	Interface Schematic
1	VDD2	Power supply for the RF Output amplifier. An external RF bypass capacitor is needed. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the capacitor should connect immediately to the ground plane.	
2	VDD1	Power supply for all other circuits. An external RF bypass capacitor is needed.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when +5V all circuits are operating. This is a high impedance input, internally connected to the gates of a few FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. In order to maximize output power this pin should be as close to +5V as possible during normal operation.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, it will typically be better than 25dB.	See pin 4.
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, it will typically be better than 25dB. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, Q SIG and Q REF also need to be swapped to maintain correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	Same as pin 5.
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V.	Same as pin 4.
8	LO IN	The input of the phase shifting network. This high impedance input can be matched with an external 56Ω termination resistor. This pin is internally connected to ground through a 4kΩ resistor. Putting a DC voltage on this pin is not recommended. However, connecting this pin to ground, e.g., through a shunt inductor, is allowed.	
9	PHASE	This pin allows to adjust the phase of the I/Q signals. However, the control is very sensitive and hard to control. Control voltage change for a few degrees adjustment is in the order of 10mV. Device to device and temperature variation are not characterized. Therefor it is not recommended to use this pin and leave it not connected. Do NOT connect to ground.For compensating large errors in the I/Q signals supplied to the device or in control loops this pin may prove useful.	
10	GND1	Ground connection of the LO phase shift network. This pin should be connected directly to the ground plane.	
11	GND	Ground connection for other circuits. Keep traces short and connect to ground plane immediately.	
12	GND	Same as pin 11.	
13	GND2	Ground connection for the RF output stage. A good ground connection is especially important at this pin to avoid interference with other circuits.	

RF2454

Pin	Function	Description	Interface Schematic
14	RF OUT	50Ω output. This pin carries a DC voltage and an external blocking capacitor is recommended.	

Application Schematic

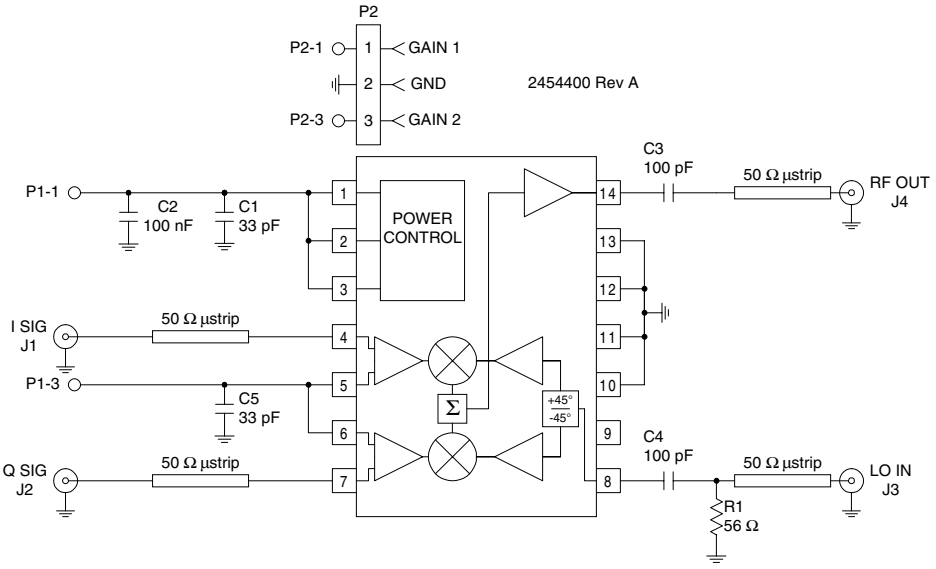


NOTE A: Optional; input impedance is about 63-j139Ω at 400 MHz without resistor. SMD resistor mounted adjacent to package pin, grounded through a via to the ground plane.

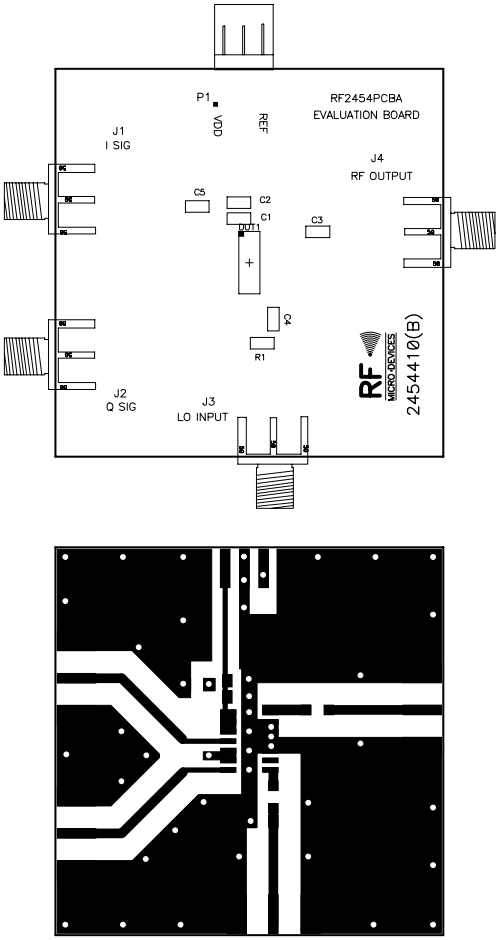
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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 2”



RF2464

VHF QUADRATURE MODULATOR

Typical Applications

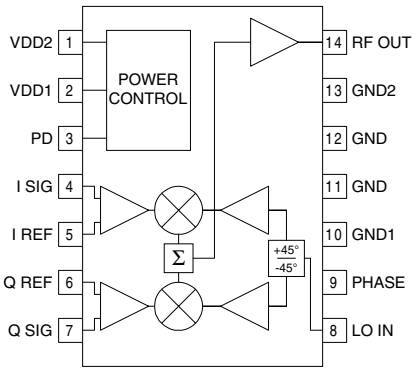
- Digital and Spread Spectrum Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- Private Mobile Radio and TETRA systems
- AM, SSB, DSB Modulation
- Image-Reject Upconverters

Product Description

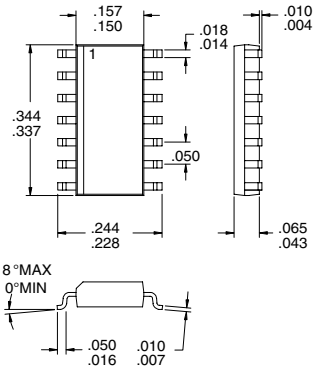
The RF2464 is a monolithic integrated universal modulation system capable of generating modulated AM, PM, or compound carriers in the VHF and UHF frequency range. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining amplifier, and an output RF amplifier which will drive a 50Ω load. Component matching, which can only be accomplished with monolithic construction, is used to full advantage to obtain excellent amplitude balance and high phase accuracy. The unit features low power consumption, single power supply operation and adjustment free operation with no external parts required to operate the part as specified.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Single 3V to 5V Power Supply
- Low Power and Small Size
- CMOS Compatible Power Down Control
- Excellent Amplitude and Phase Balance
- Low Broadband Noise Floor
- 200MHz to 600MHz Operation

Ordering Information

RF2464	VHF Quadrature Modulator
RF2464 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

5 MODULATORS AND UPCONVERTERS

RF2464

Absolute Maximum Ratings

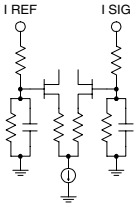
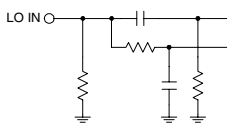
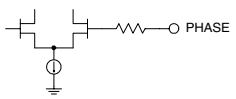
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Down Voltage	-0.5 to V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

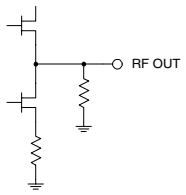
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LO Input					T=25°C, V_{DD}=5V_{DC}, I&Q inputs=2V_{PP}
Frequency Range		200 to 600		MHz	
Power Level		-3 to +6		dBm	
Input VSWR		1.2:1			With external 50Ω termination; see application schematic, note A.
Input Impedance		94-j264		Ω	At 200MHz, without external 50Ω termination.
		79-j158			At 400MHz, without external 50Ω termination.
		67-j117			At 600MHz, without external 50Ω termination.
Modulation Input					
Frequency Range		DC to 100		MHz	
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Modulation (I&Q)		V_{REF}±0.7		V	I & Q signals for 0dBm output power.
Modulation (I&Q)		V_{REF}±1.5		V	I & Q signals for +5dBm output power.
Maximum Modulation (I&Q)		V_{REF}±2.5		V	In-phase and quadrature signals.
Input Resistance		3000		Ω	
DC Offset		50	150	mV	I_{SIG}-I_{REF} and Q_{SIG}-Q_{REF}; to achieve maximum carrier suppression.
Amplitude Error (I/Q)		0.2		dB	
Quadrature Phase Error		±1	±3	°	From 350MHz to 450MHz.
RF Output					V_{DD}=5V, LO Power=0dBm, LO Freq=400MHz, SSB, I&Q input=0.7V_P
Output Power	-1	+1	+3	dBm	
Output Impedance		50			
Output VSWR		1.5:1			
Broadband Noise Floor		-150		dBm/Hz	
Sideband Suppression		25	>40	dB	
Carrier Suppression	18	25	>40	dB	Modulation DC offset can be externally adjusted for optimum suppression. Suppression is typically better than 25dB without adjustment.
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>1		MΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage
Power Down "OFF"		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 5.5		V	Operating Limits
Current		28	39	mA	Operating
		0.5	2	mA	Power Down

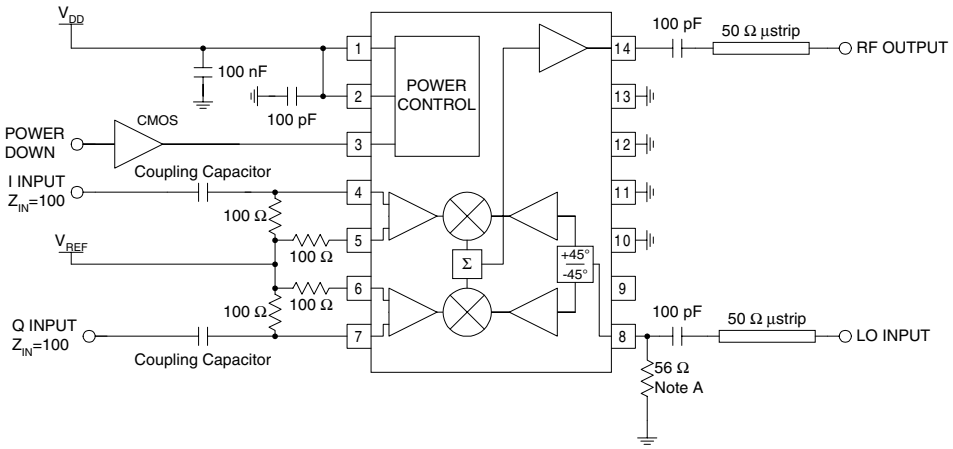
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Pin	Function	Description	Interface Schematic
1	VDD2	Power supply for the RF Output amplifier. An external RF bypass capacitor is needed. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the capacitor should connect immediately to the ground plane.	
2	VDD1	Power supply for all other circuits. An external RF bypass capacitor is needed.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when +5V all circuits are operating. This is a high impedance input, internally connected to the gates of a few FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. In order to maximize output power this pin should be as close to +5V as possible during normal operation.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, it will typically be better than 25dB.	See pin 4.
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, it will typically be better than 25dB. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, Q SIG and Q REF also need to be swapped to maintain correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	Same as pin 3.
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V.	Same as pin 4.
8	LO IN	The input of the phase shifting network. This high impedance input can be matched with an external 56Ω termination resistor. This pin is internally connected to ground through a 4kΩ resistor. Putting a DC voltage on this pin is not recommended. However, connecting this pin to ground, e.g., through a shunt inductor, is allowed.	
9	PHASE	This pin allows to adjust the phase of the I/Q signals. However, the control is very sensitive and hard to control. Control voltage change for a few degrees adjustment is in the order of 10mV. Device to device and temperature variation are not characterized. Therefore it is not recommended to use this pin; leave it not connected. Do NOT connect to ground.For compensating large errors in the I/Q signals supplied to the device or in control loops this pin may prove useful.	
10	GND1	Ground connection of the LO phase shift network. This pin should be connected directly to the ground plane.	
11	GND	Ground connection for other circuits. Keep traces short and connect to ground plane immediately.	
12	GND	Same as pin 11.	
13	GND2	Ground connection for the RF output stage. A good ground connection is especially important at this pin to avoid interference with other circuits.	

RF2464

Pin	Function	Description	Interface Schematic
14	RF OUT	50Ω output. This pin carries a DC voltage, and an external blocking capacitor is recommended.	

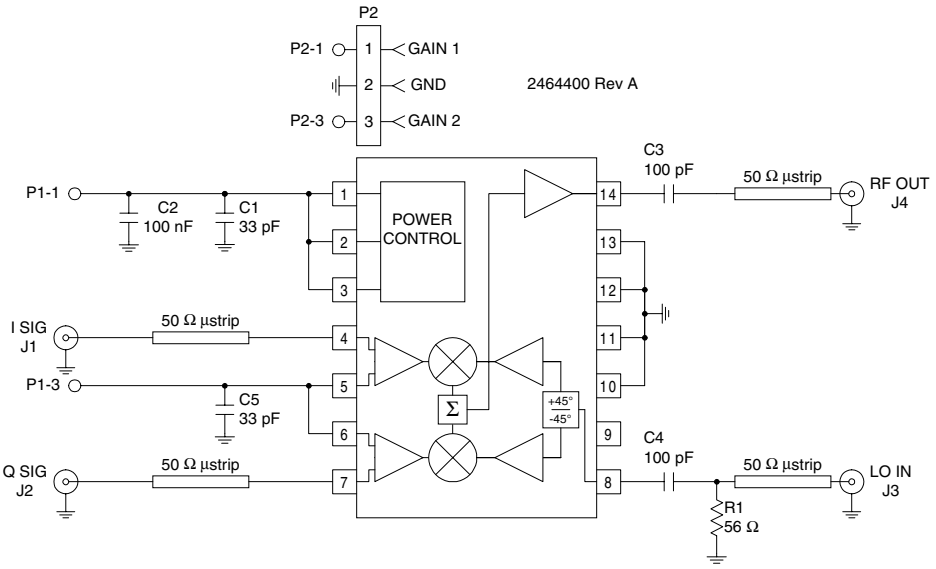
Application Schematic



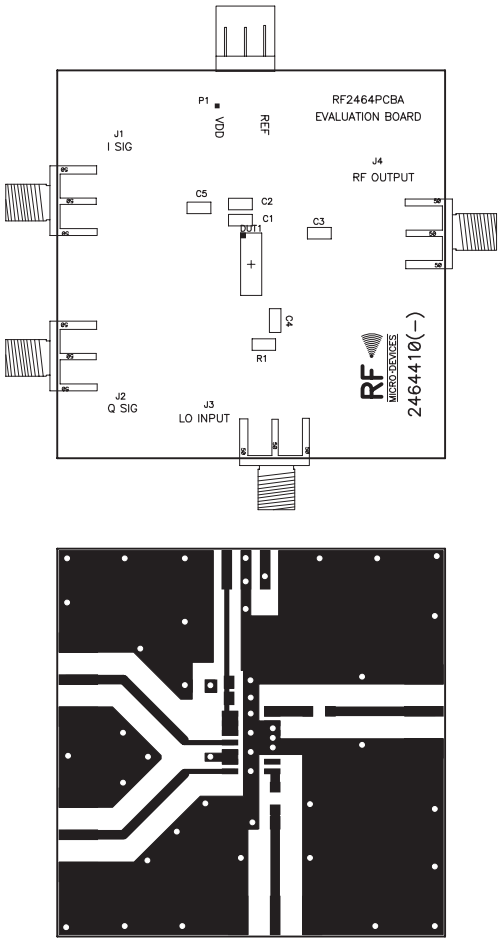
NOTE A: Optional; input impedance is about 79-J158 Ω at 400 MHz without resistor. SMD resistor mounted adjacent to package pin, grounded through a via to the ground plane.

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 2”



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RF2658

TRANSMIT MODULATOR, IF AGC, AND UPCONVERTER

Typical Applications

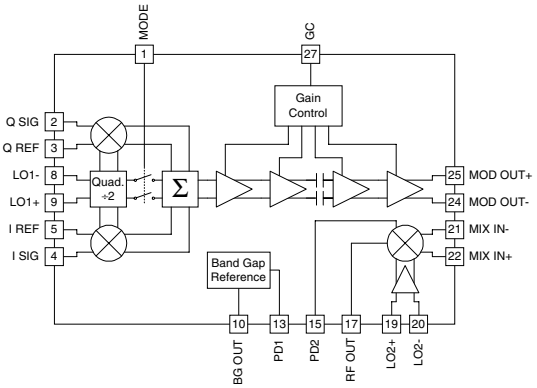
- CDMA/FM Cellular Systems
- CDMA PCS Systems
- GSM/DCS Systems
- TDMA Systems
- Spread Spectrum Cordless Phones
- Wireless Local Loop Systems

Product Description

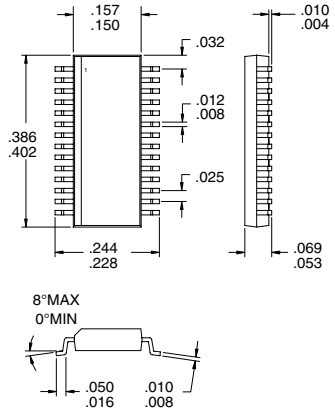
The RF2658 is an integrated complete Quadrature Modulator, IF AGC amplifier, and Upconverter developed for the transmit section of dual-mode CDMA/FM cellular and PCS applications and for GSM/DCS and TDMA systems. It is designed to modulate baseband I and Q signals, amplify the resulting IF signals while providing 95dB of gain control range, and perform the final upconversion to UHF. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 Interim Standard for CDMA cellular communications. This circuit is part of RFMD's line of complete solutions for digital radio applications. The IC is manufactured on an advanced 15GHz F_T Silicon Bipolar process, and is supplied in a 28-lead plastic SSOP package.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-28

Features

- Similar to RF9958 with increased IF range
- Supports Dual Mode Operation
- Digitally Controlled Power Down Modes
- 2.7V to 3.3V Operation
- Double-Balanced UHF Upconvert Mixer
- IF AGC Amp with 95 dB Gain Control

Ordering Information

RF2658	Transmit Modulator, IF AGC, and Upconverter
RF2658 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

5 MODULATORS AND UPCONVERTERS

RF2658

Absolute Maximum Ratings

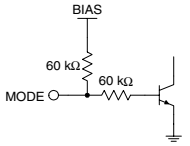
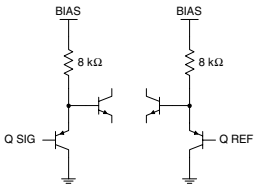
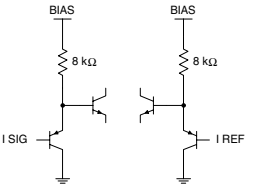
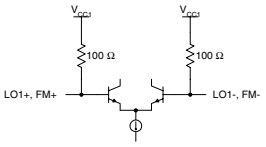
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V
I and Q Levels, per pin	1	V_{PP}
LO1 Level, balanced	+3	dBm
LO2 Level, balanced	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

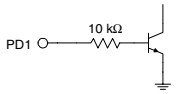
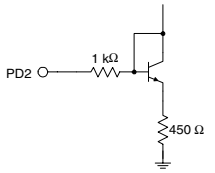
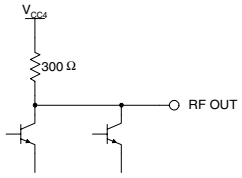
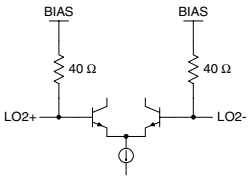
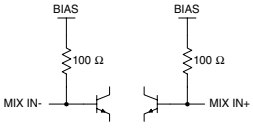
Caution! ESD sensitive device.

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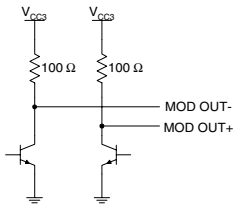
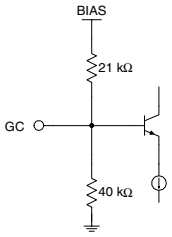
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q Modulator & AGC					T=25 °C, V_{CC}=3.0V, Z_{LOAD}=50Ω, LO1 =-8dBm @ 260 MHz, LO2=-3dBm @ 960MHz, I SIG=Q SIG=300mV$_{PP}$, RF Output externally matched
I/Q Input Frequency Range		0 to 20		MHz	Balanced
I/Q Input Impedance	50	80	110	kΩ	Balanced
I/Q Input Reference Level		0.6		V_{DC}	Per Pin
LO1/FM Frequency Range		240 to 600		MHz	
LO1/FM Input Level	-15	-8	-5	dBm	
LO1/FM Input Impedance	170	200	230	Ω	Balanced
Sideband Suppression	35	40		dBc	I/Q Amplitude adjusted to within ±20mV
		30		dBc	Unadjusted
Carrier Suppression	40	50		dBc	I/Q DC Offset adjusted to within ±20mV
		30		dBc	Unadjusted
Max Output, FM Mode	+2.5	+4		dBm	V_{GC}=2.5 V_{DC}
Max Output, CDMA Mode	-3	0		dBm	V_{GC}=2.5 V_{DC}
Min Output, CDMA Mode		-95	-89	dBm	V_{GC}=0.5 V_{DC}
Adjacent Channel Power Rejection @ 885kHz		-55		dBc	IS-95A CDMA Modulation P_{OUT}=-5dBm
Adjacent Channel Power Rejection @ 1.98MHz		-67		dBc	IS-95A CDMA Modulation P_{OUT}=-5dBm
Output Noise Power		-116	-111	dBm/Hz	P_{OUT}=-3 dBm
Output Noise Power		-164	-159	dBm/Hz	P_{OUT} < -70 dBm
Output Power Accuracy	-3		+3	dB	T=-20 to +85 °C, Ref=25 °C
Output Impedance	170	200	230	Ω	Balanced
UHF Upconverter					Output externally matched
Conversion Gain	-1	0.5		dB	
Noise Figure (SSB)		15		dB	
Output IP3		+14		dBm	
IF Input Impedance	170	200	230	Ω	Balanced
IF Input Frequency Range		120 to 180		MHz	
LO2 Input Impedance		50		Ω	Single Ended
LO2 Input Level	-6	-3	0	dBm	
LO2 Input Frequency Range		700 to 1100		MHz	
RF to LO2 Isolation		20		dB	
Power Supply					
Supply Voltage	2.7	3.0	3.3		
Current Consumption		43		mA	Modulator and AGC only, CDMA Mode
Current Consumption		20		mA	Mixer Only
Power Down Current			20	μA	
V_{PD} HIGH Voltage	V_{CC}-0.7				
V_{PD} LOW Voltage			0.5		

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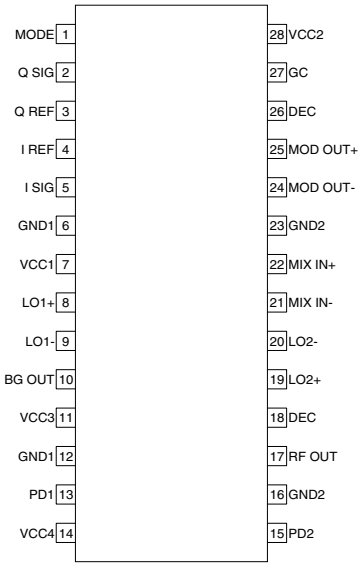
Pin	Function	Description	Interface Schematic
1	MODE	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" ($\geq V_{CC}$-0.7V_{DC}) selects CDMA mode. A logic "low" ($\geq$0.5V_{DC}) selects FM mode. In FM mode, this switch enables the FM amplifier and turns off the I&Q modulator. The impedance on this pin is 30kΩ.	
2	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum.	
3	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the Q SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum.	See pin 2.
4	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the I SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum.	See pin 5.
5	I SIG	Baseband input to the I mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum.	
6	GND1	Ground connection for all baseband circuits including bandgap, AGC, flip-flop, modulator and FM amp. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC1	Supply voltage for the LO1 flip-flop and limiting amp only. This supply is isolated to minimize the carrier leakage. A 1nF external bypass capacitor is required, and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. The part is designed to work from 2.7V to 3.3V supply.	
8	LO1+, FM+	One half of the balanced modulator LO1 input. The other half of the input, LO1-, is AC grounded for single-ended input applications. The frequency on these pins is divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 100Ω (balanced is 200Ω). This pin is NOT internally DC blocked. An external blocking capacitor (1nF recommended) must be provided if the pin is connected to a device with DC present. When FM mode is selected, the output of the flip-flop divider circuit is switched to the AGC amplifier inputs and the modulator mixers are not used. Note that the frequency deviation input here will be reduced by a factor of two, due to the frequency divider operation.	
9	LO1-, FM-	One half of the balanced modulator LO1 input. In single-ended applications (100Ω input impedance), this pin is AC grounded with a 1nF capacitor.	See pin 8.
10	BG OUT	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 1nF external bypass capacitor is required.	

Pin	Function	Description	Interface Schematic
11	VCC3	Supply voltage for the AGC and the Bandgap circuitry. A 1nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. The part is designed to work from 2.7V to 3.3V supply.	
12	GND1	Same as pin 6.	
13	PD1	Power down control for overall circuit. When logic "high" ($\geq V_{CC}$-0.7V), all circuits are operating; when logic "low" (<0.5V), all circuits are turned off. The input impedance of this pin is >10kΩ.	
14	VCC4	Supply for the mixer stage only. The supply for the mixer is separated to maximize IF to RF isolations and reduce the carrier leakage. A 100pF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are near by. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. The part is designed to work from 2.7V to 3.3V supply.	
15	PD2	Power down control for mixer only. When connected to pin 10 (BG OUT) the mixer circuits are operating; when connected to ground (≤0.5V), the mixer is turned off but all other circuits are operating.	
16	GND2	Ground connection for the mixer stage. Keep traces physically short and connect immediately to ground plane for best performance.	
17	RF OUT	RF output pin. An external shunt inductor to V_{CC} plus a series blocking/matching capacitor are required for 50Ω output.	
18	DEC	Current mirror decoupling pin. A 1000pF external capacitor is required to bypass this pin. The ground side of the bypass capacitors should connect immediately to ground plane.	
19	LO2+	One half of the balanced mixer LO2 input. In single-ended applications, the other half of the input, LO2- is AC grounded. This is a 50Ω impedance port. This pin is NOT internally DC blocked. An external blocking capacitor (100pF recommended) must be provided if the pin is connected to a device with DC present.	
20	LO2-	One half of the balance mixer LO2 input. In single ended applications, this pin is AC grounded with a 100pF capacitor.	See pin 19.
21	MIX IN-	One half of the 200Ω balanced impedance input to the mixer stage. This pin is NOT internally DC blocked. An external blocking capacitor (2200pF recommended) must be provided if the pin is connected to a device with DC present. If no IF filter is needed, this pin may be connected to MOD OUT+ through a DC blocking capacitor. An appropriate matching network may be needed if an IF filter is used.	
22	MIX IN+	Same as pin 21, except complementary input.	See pin 21.

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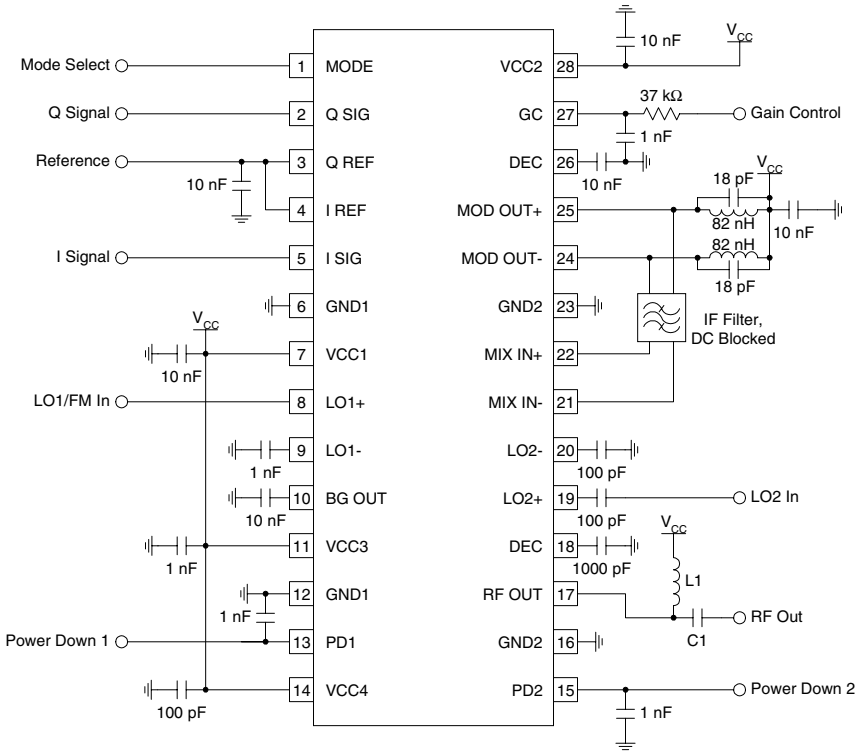
Pin	Function	Description	Interface Schematic
23	GND2	Same as pin 16.	
24	MOD OUT-	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. If no filtering is required, this pin can be connected to the MIX IN- pin through a DC blocking capacitor. This pin requires an inductor to V_{CC} to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
25	MOD OUT+	Same as pin 24, except complementary output.	See pin 24.
26	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
27	GC	Analog gain control for AGC amplifiers. Valid control voltage ranges are from 0.5V_{DC} to 2.5V_{DC}. The gain range for the AGC is 88dB. These voltages are valid ONLY for a 37kΩ source impedance.	
28	VCC2	Supply for the modulator stage only. A 10nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. The part is designed to work from 2.7V to 3.3V supply.	

RF2658 Pin-Out



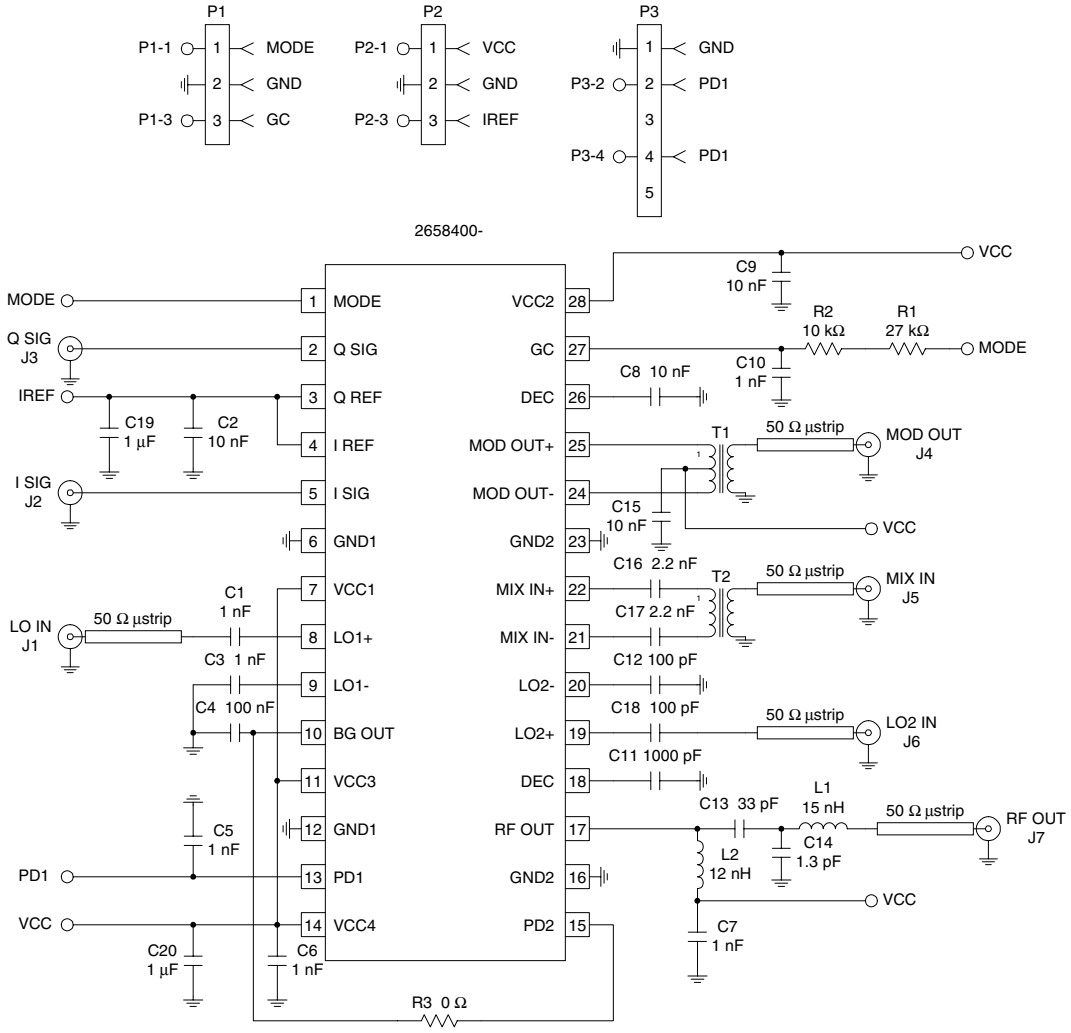
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Application Schematic

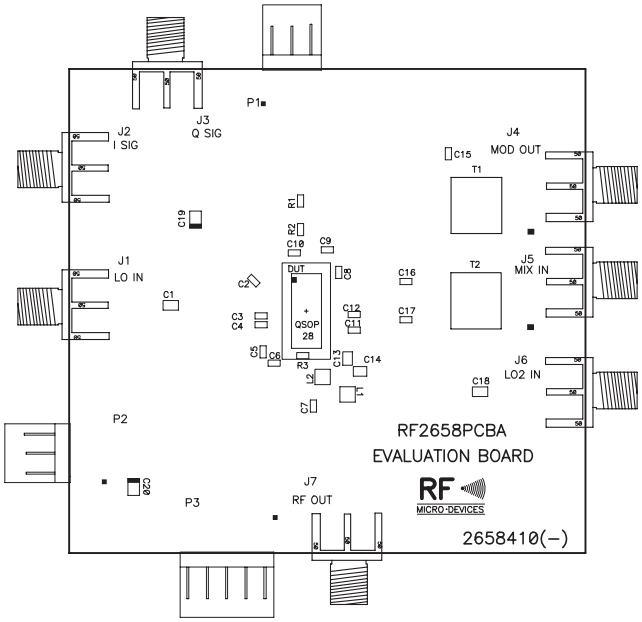


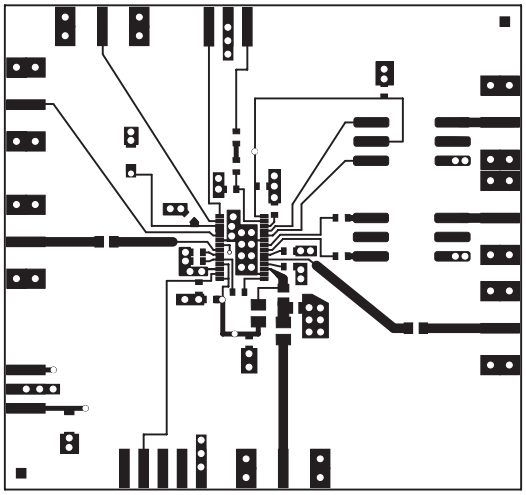
Evaluation Board Schematic

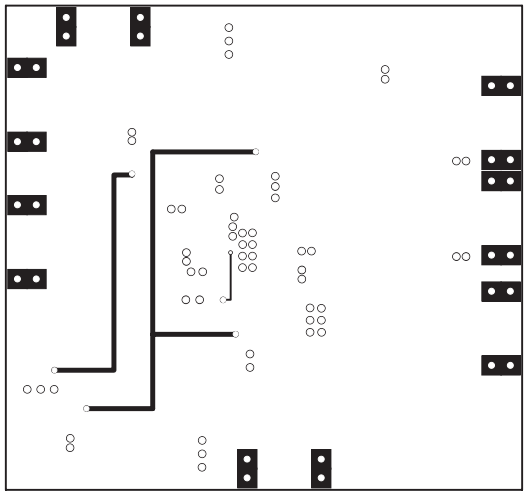
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.689" x 2.521"







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Preliminary

RF2668

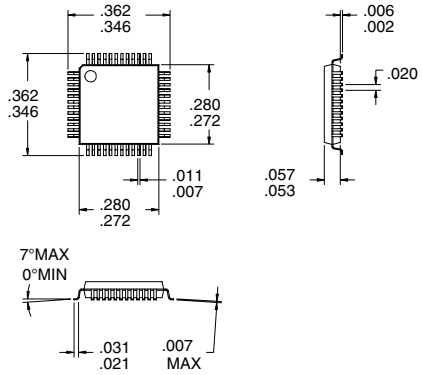
CDMA/FM TRANSMIT MODULATOR, IF AGC, AND UPCONVERTER WITH INTEGRATED PLL

Typical Applications

- CDMA/FM Cellular Systems
- CDMA PCS Systems
- W- CDMA Systems
- Wireless Local Loop Systems
- Spread Spectrum Cordless Phones
- High Speed Data Modems

Product Description

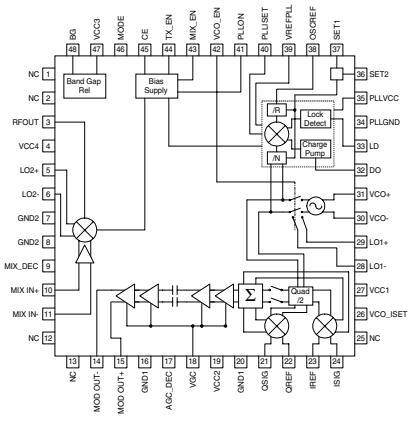
The RF2668 is an integrated complete Quadrature Modulator, IF AGC amplifier, Upconverter, and PLL, designed for the transmit section of dual-mode CDMA/FM cellular and PCS applications. It is designed to modulate baseband I and Q signals, amplify the resulting IF signals while providing 95dB of gain control range, and perform the final upconversion to UHF. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 Interim Standard for CDMA cellular communications. This circuit is designed as part of RFMD's newest CDMA Chip Set, which also includes the RF2667 CDMA/FM Receive IF AGC and Demodulator. The IC is manufactured on an advanced 18GHz F_T Silicon Bipolar process, and is supplied in a 48-lead plastic LQFP package.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation
- Digitally Controlled Power Down Modes
- 2.7V to 3.3V Operation
- Digital First LO Quadrature Divider
- Double-Balanced UHF Upconvert Mixer
- IF AGC Amp with 95dB Gain Control

Ordering Information

RF2668	CDMA/FM Transmit Modulator, IF AGC, and Upconverter with Integrated PLL
RF2668 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V
I and Q Levels, per pin	1	V_{PP}
LO1 Level, balanced	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

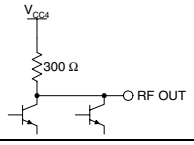
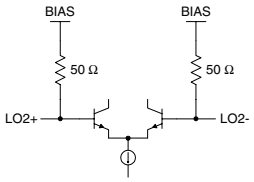
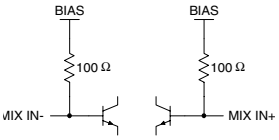
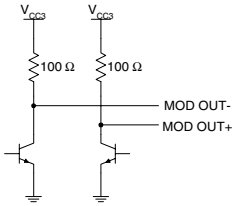
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q Modulator & AGC					T=25°C, V_{CC}=3.0V, Z_{LOAD}=200Ω, LO1=-10dBm @ 260MHz, IF=130MHz, I SIG=Q SIG=300mV_{PP}, RF Output externally matched
I/Q Input Frequency Range		0 to 20		MHz	Balanced
I/Q Input Impedance		80		kΩ	Balanced
I/Q Input Reference Level		1.3		V_{DC}	Per Pin
LO1/FM Frequency Range	0		800	MHz	
LO1/FM Input Level	-15	-10	-5	dBm	
LO1/FM Input Impedance		200		Ω	Balanced
Sideband Suppression	35	40		dBc	I/Q Amplitude adjusted to within ±20mV
		27		dBc	Unadjusted
Carrier Suppression	40	50		dBc	I/Q DC Offset adjusted to within ±20mV
		30		dBc	Unadjusted
Max Output, FM Mode	+2.5	+5		dBm	V_{GC}=2.4V_{DC}, T=-20°C to +85°C
Max Output, CDMA Mode	-3	0		dBm	V_{GC}=2.4V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
	-2	0		dBm	ISIG=QSIQ=300mVpp @ 100kHz
Min Output, CDMA Mode		-95	-89	dBm	V_{GC}=0.3V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
Output Power Accuracy	-3		+3	dB	T=-20 to +85°C, Ref=25°C
	-2		+2	dB	1.4V≤GC≤2.5
Adjacent Channel Power Rejection @ 885kHz		-60		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Adjacent Channel Power Rejection @ 1.98MHz		-69		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Output Noise Power		-117	-111	dBm/Hz	P_{OUT} = -1dBm, T=-20°C to +85°C
Output Impedance		200		Ω	Balanced
Current Consumption		40		mA	

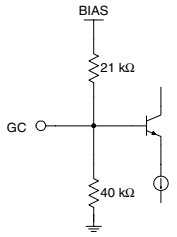
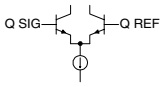
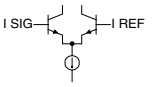
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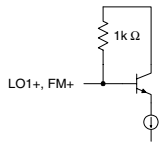
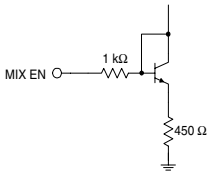
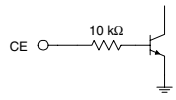
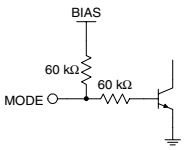
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
UHF Upconverter					Output externally matched
General					
IF Input Impedance		200		Ω	Balanced
IF Input Frequency Range	0		400	MHz	
LO2 Input Impedance		50		Ω	Single Ended
LO2 Input Level	-6	-3	0	dBm	
LO2 Input Frequency Range			2.5	GHz	
RF to LO2 Isolation		30		dB	
LO Input VSWR		<2:1			50Ω
Current Consumption		24		mA	
Cellular					
Conversion Gain	-1.5	-0.5		dB	RF_{OUT}=830MHz
Noise Figure (SSB)		15		dB	RF_{OUT}=830MHz
Output IP3		+13		dBm	P_{IN}=-15dBm per tone, 200kHz tone separation, RF_{OUT}=830MHz, LO2=960MHz@-3dBm
RF Output VSWR		<2:1			RF_{OUT} = 830MHz
PCS					
Conversion Gain		-1.5		dB	RF_{OUT}=1950MHz
Noise Figure		TBD			
Output IP3		10			P_{IN}=15dBm per tone, 200kHz tone separation, RF_{OUT}=1950MHz, LO2=1570MHz@-3dBm
RF Output VSWR		<2:1			RF_{OUT}=1950MHz. See note on eval board schematic.
VCO					PLL locked with Loop BW=5kHz, Tank Values: 39nH and SMV1234 varactor.
Phase Noise @ 100kHz		-110		dBc/Hz	
Current Consumption		1		mA	
PLL					
Charge Pump Current			100	μA	
TCXO Input Level		0.8		V_{PP}	
PLL Lock Time		4/Loop		BW	S
Current Consumption		4		mA	
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		69		mA	
Power Down Current		<10		μA	
VPD HIGH Voltage	V_{CC}-0.3			V	
VPD LOW Voltage			0.3	V	
PLL Settings					
Application	**Japan**	**Japan**	**US/Korea**		
LO Frequency, MHz	333.7	333.7	260.76		IF Frequency=LO Frequency/2
Crystal, MHz	19.2	19.8	19.68		
Reference Divider	192	198	252		
Phase Detector Frequency, kHz	100	100	78.09524		
Prescaler	32/33	32/33	32/33		
Swallow Counter (A)	9	9	11		
Fixed Divider (N)	104	104	104		
Net N in VCO Path	3337	3337	3339		
SEL1	VCC	GND	GND		
SEL2	GND	VCC	GND		

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Pin	Function	Description	Interface Schematic
1	NC	Not connected.	
2	NC	Not connected.	
3	RF OUT	RF output pin. An external shunt inductor to V_{CC} plus a series blocking/ matching capacitor are required for 50Ω output.	
4	VCC4	Supply for the mixer stage only. The supply for the mixer is separated to maximize IF to RF isolations and reduce the carrier leakage. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	LO2+	One half of the balanced mixer LO2 input. In single-ended applications, the other half of the input, LO2- is AC grounded. This is a 50Ω impedance port. This pin is NOT internally DC blocked. An external blocking capacitor (100pF recommended) must be provided if the pin is connected to a device with DC present.	
6	LO2-	One half of the balance mixer LO2 input. In single ended applications, this pin is AC grounded with a 100pF capacitor.	See pin 19.
7	GND2	Ground connection for the mixer stage. Keep traces physically short and connect immediately to ground plane for best performance.	
8	GND2	Same as pin 16.	
9	MIX_DEC	Current Mirror decoupling pin. A 1000pF external capacitor is required to bypass this pin. The ground side of the bypass capacitors should connect immediately to ground plane.	
10	MIX IN+	Same as pin 11, except complementary input.	See pin 11.
11	MIX IN-	One half of the 200Ω balanced impedance input to the mixer stage. This pin is NOT internally DC blocked. An external blocking capacitor (1000pF recommended) must be provided if the pin is connected to a device with DC present. If no IF filter is needed this pin may be connected to MOD OUT+ through a DC blocking capacitor. An appropriate matching network may be needed if an IF filter is used.	
12	NC	Not connected.	
13	NC	Not connected.	
14	MOD OUT-	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. If no filtering is required, this pin can be connected to the MIX IN- pin through a DC blocking capacitor. This pin requires an inductor to V_{CC} to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
15	MOD OUT+	Same as pin 14, except complementary output.	See pin 14.
16	GND1	Ground connection for all baseband circuits including bandgap, AGC, flip-flop, modulator and FM amp. Keep traces physically short and connect immediately to ground plane for best performance.	

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Pin	Function	Description	Interface Schematic
17	AGC_DEC	AGC decoupling pin. An external bypass capacitor of 1nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
18	VGC	Analog gain control for AGC amplifiers. Valid control voltage ranges are from $0.3V_{DC}$ to $2.4V_{DC}$. The gain range for the AGC is 95dB. These voltages are valid ONLY for a 39kΩ source impedance. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
19	VCC2	Supply for the modulator stage only. A 10nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
20	GND1	Same as pin 16.	
21	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The DC level of 1.3V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
22	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the Q SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 2.
23	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the I SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 5.
24	I SIG	Baseband input to the I mixer. This pin is DC coupled. The DC level of 1.3V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
25	NC	Not connected.	
26	VCO_ISET	An external resistor of 47kΩ is used to set the VCO current for minimum phase noise.	
27	VCC1	Supply Voltage for the LO1 flip-flop and limiting amp only. This supply is isolated to minimize the carrier leakage. A 1nF external bypass capacitor is required, and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
28	LO1-	External LO input to modulator. Controlled by VCO_EN signal. Logic low is internal VCO, while logic high is external VCO.	See pin 8.

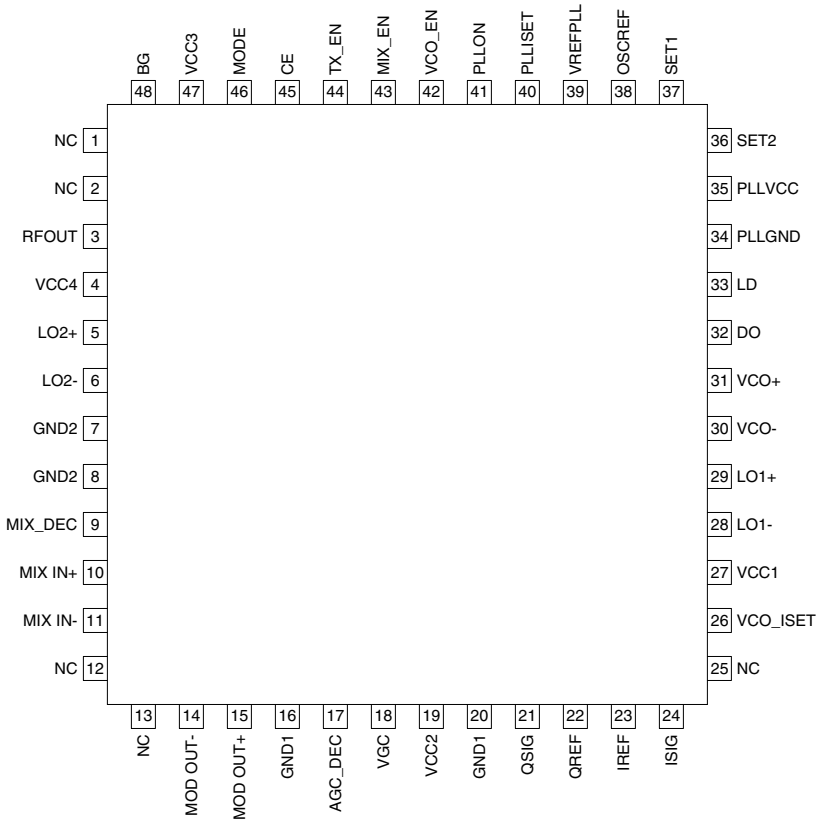
Pin	Function	Description	Interface Schematic
29	LO1+	External LO input to modulator. Controlled by VCO_EN signal. Logic low is internal VCO, while logic high is external VCO.	
30	VCO-	See VCO+ description.	
31	VCO+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 30 although a small imbalance can be used to tune in the proper frequency range.	
32	DO	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
33	LD	Lock detector output for synthesizer. Requires external transistor to provide hysteresis and inversion of signal. See Application circuit.	
34	PLLGND	Ground for synthesizer. Keep traces physically short and connect immediately to ground plane for best performance.	
35	PLLVCC	Supply for the PLLVCC only. A 10nF external bypass capacitor is required and an additional 0.1μF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
36	SET2	PLL Setting (Divider) pin. See the PLL settings table.	
37	SET1	See SET2.	
38	OSCREF	TCXO reference input for synthesizer.	
39	VREFPLL	Bypass pin for the synthesizer reference voltage.	
40	PLLISET	Current setting pin for synthesizer charge pump. For normal operation, a 390Ω resistor to ground should be used to set the current.	
41	PLLON	Synthesizer Enable pin.	See pin 45.
42	VCO_EN	VCO Enable pin. Switches between internal and external VCO.	See pin 45.
43	MIX_EN	Power down control for mixer only. When connected to logic “high” ($>V_{CC}$-0.3) the mixer circuits are operating; when connected to ground (≤0.3V), the mixer is turned off but all other circuits are operating. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
44	TX_EN	Shuts down the entire TX path. VCO is still active when TX disabled. Logic high (>VCC -0.3) for TX Enable.	
45	CE	Power down control for overall circuit. When logic “high” ($\geq V_{CC}$-0.3V), all circuits are operating; when logic “low” (≤0.3V), all circuits are turned off. The input impedance of this pin is >10kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
46	MODE	Selects between CDMA and FM mode. This is a digitally controlled input. A logic “high” ($\geq V_{CC}$-0.3V_{DC}) selects CDMA mode. A logic “low” (<0.3V_{DC}) selects FM mode. In FM mode, this switch enables the FM amplifier and turns off the I&Q modulator. The impedance on this pin is 30kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	

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Pin	Function	Description	Interface Schematic
47	VCC3	Supply voltage for the AGC and the Bandgap circuitry. A 1nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
48	BG OUT	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 1nF external bypass capacitor is required.	

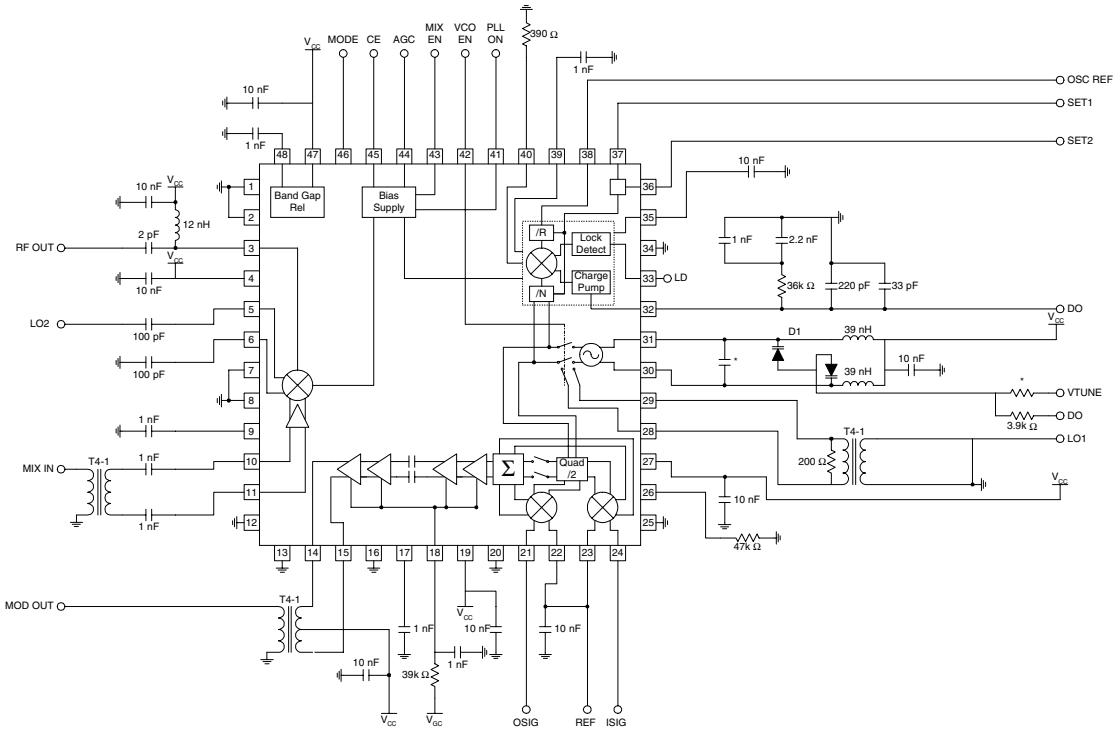
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RF2668 Pin-Out



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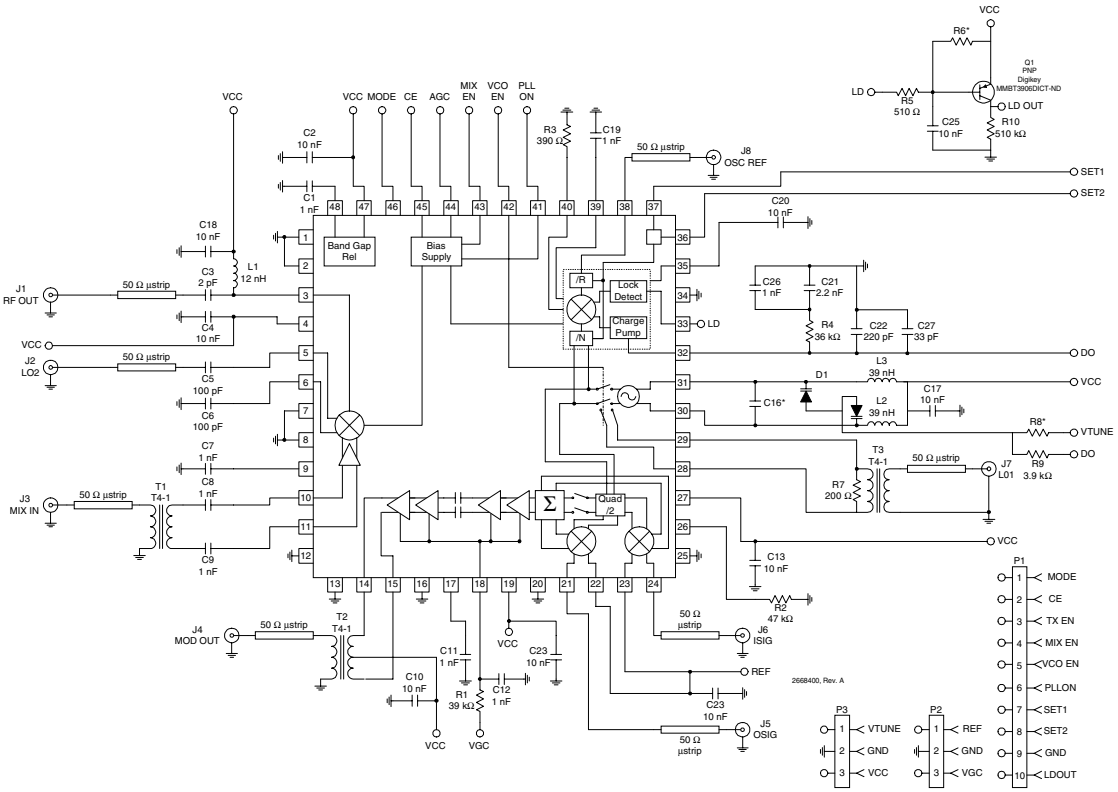
Application Schematic



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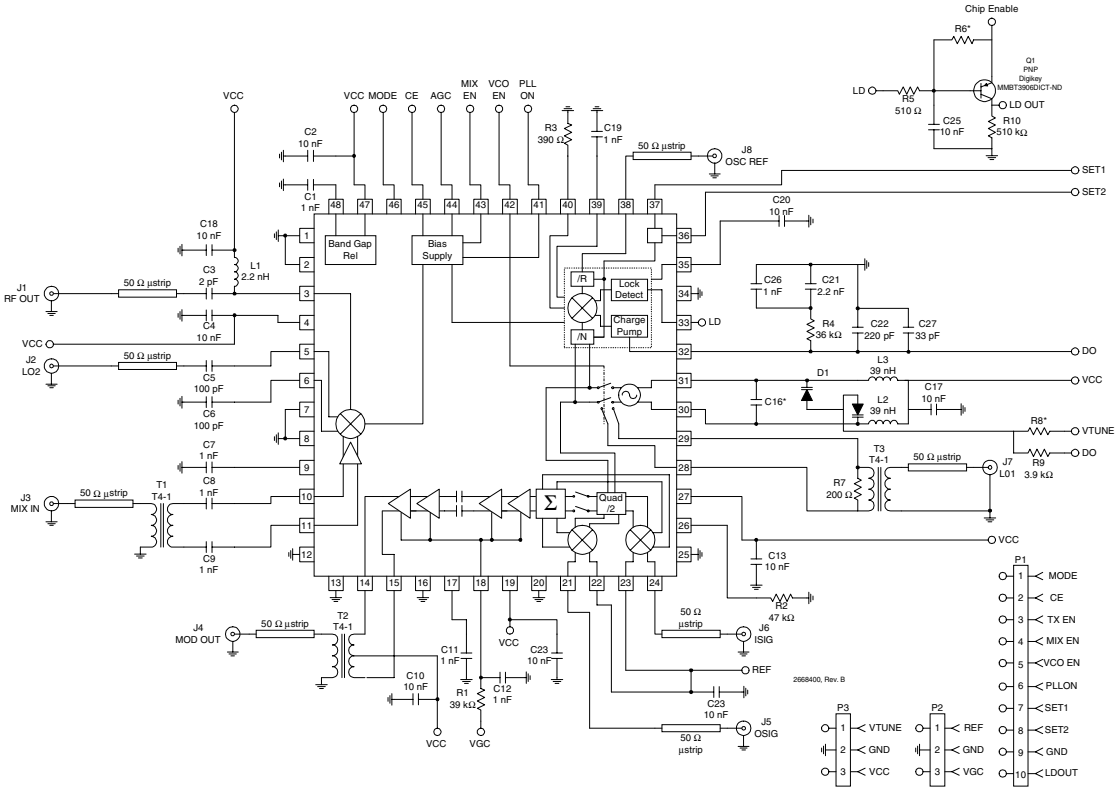
Evaluation Board Schematic
RF_{OUT}=830MHz

(Download Bill of Materials from www.rfmd.com.)



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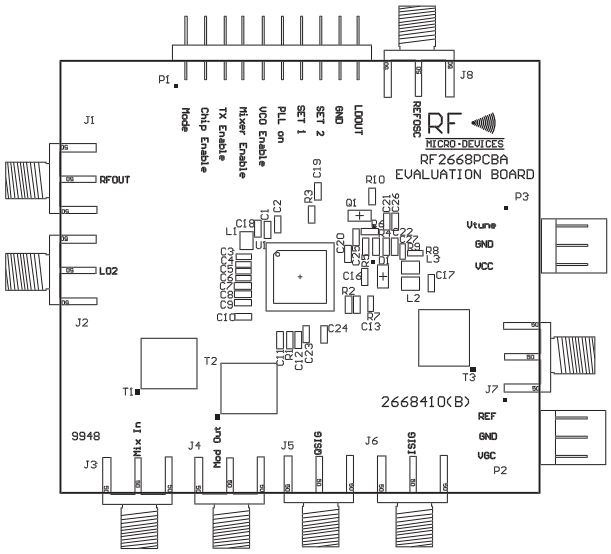
Evaluation Board Schematic
RF_{OUT}=1950MHz

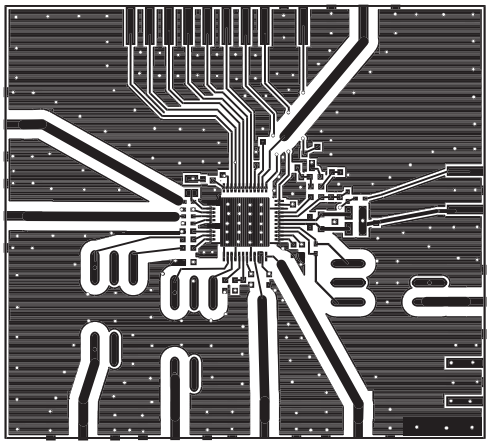


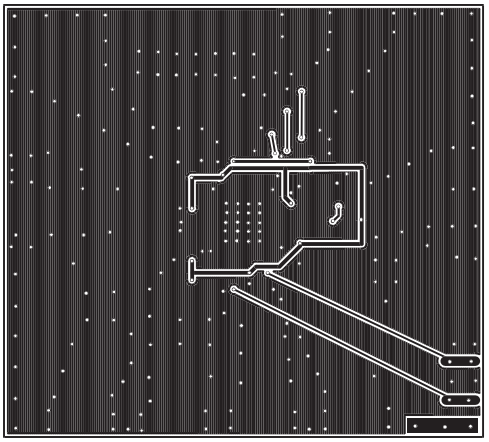
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Evaluation Board Layout
2.5" X 2.2"

Board Thickness 0.031”, Board Material FR-4







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Preliminary

RF2713

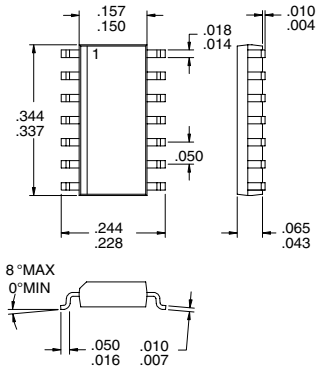
QUADRATURE MODULATOR/DEMODULATOR

Typical Applications

- Digital and Analog Receivers and Transmitters
- High Data Rate Digital Communications
- Spread Spectrum Communication Systems
- Interactive Cable Systems
- Portable Battery Powered Equipment

Product Description

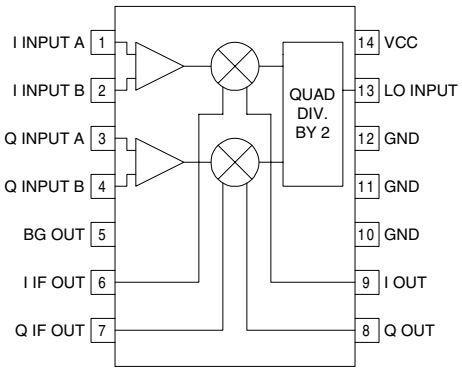
The RF2713 is a monolithic integrated quadrature modulator/demodulator. The demodulator is used to recover the I and Q baseband signals from the amplified and filtered IF. Likewise, the inputs and outputs can be reconfigured to modulate I/Q signals onto an RF carrier. The RF2703 is intended for IF systems where the IF frequency ranges from 100kHz to 250MHz, and the LO frequency is two times the IF. The IC contains all of the required components to implement the modulation/demodulation function and contains a digital divider type 90° phase shifter, two double balanced mixers, and baseband amplifiers designed to interface with Analog to Digital Converters. The unit operates from a single 3V to 6V power supply.



Package Style: SOP-14

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 3V to 6V Operation
- Modulation or Demodulation
- IF From 100kHz to 250MHz
- Baseband From DC to 50MHz
- Digital LO Quadrature Divider
- Low Power and Small Size

Ordering Information

RF2713	Quadrature Modulator/Demodulator
RF2713 PCBA-D	Fully Assembled Evaluation Board (Demodulator)
RF2713 PCBA-M	Fully Assembled Evaluation Board (Modulator)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
IF Input Level	500	mV_{PP}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

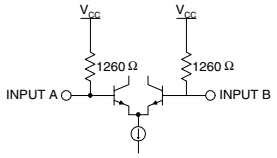
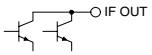
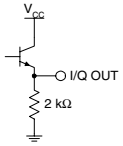
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, IF=100MHz, LO=200MHz, F_{MOD}=500kHz
IF Frequency Range		0.1 to 250		MHz	For IF frequencies below ~2.5MHz, the LO should be a square wave. IF frequencies lower than 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.
Baseband Frequency Range		DC to 50		MHz	
Input Impedance		1200 ‖ 1pF		Ω	Each input, single-ended
LO					
Frequency					Twice (2x) the IF frequency. For IF frequencies below ~2.5MHz, the LO should be a square wave. IF frequencies lower than 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.
Level		0.06 to 1		V_{PP}	
Input Impedance		500 ‖ 1pF		Ω	
Demodulator Configuration					IF_{IN}=28mV_{PP}, LO=200mV_{PP}, Z_{LOAD}=10kΩ
Output Impedance		50 ‖ 1pF		Ω	Each output, I_{OUT} and Q_{OUT}
Maximum Output		1.4		V_{PP}	Saturated
Voltage Gain		20		dB	V_{CC}=3.0V
	22.5	24	25.1	dB	V_{CC}=5.0V
Noise Figure		24		dB	Single Sideband, IF Input of device reactively matched
		35		dB	Single Sideband, 50Ω shunt resistor at IF Input
Input Third Order Intercept Point (IIP_3)		-22		dBm	V_{CC}=3.0V, IF Input of device reactively matched
		-11		dBm	V_{CC}=3.0V, 50Ω shunt resistor at IF Input
		-19			V_{CC}=5.0V, IF Input of device reactively matched
		-8		dBm	V_{CC}=5.0V, 50Ω shunt resistor at IF Input
		-28		dBm	V_{CC}=5.0V, IF Input of device reactively matched, Z_{LOAD}=50Ω
I/Q Amplitude Balance		0.1	0.5	dB	
Quadrature Phase Error		<±1		°	
DC Output		800		mV	V_{CC}=3.0V, I_{OUT} and Q_{OUT} to GND
	2.0	2.4	2.8	V	V_{CC}=5.0V, I_{OUT} and Q_{OUT} to GND
DC Offset		<10	60	mV	I_{OUT} to Q_{OUT}

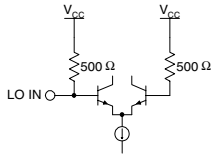
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Modulator Configuration					IF_{IN}=28mV_{PP}, LO=200mV_{PP}, Z_{LOAD}=1200Ω
Maximum Output		200		mV_{PP}	Saturated
Input Voltage		90		mV_{PP}	Single Sideband, 1dB Gain Compression.
Voltage Gain		6		dB	Single Sideband
I/Q Amplitude Balance		0.1		dB	
Quadrature Phase Error		<±1		°	
Carrier Suppression		25		dBc	Unadjusted. Carrier Suppression may be optimized further by adjusting the DC offset level between the A and B inputs.
Sideband Suppression		30		dBc	
Power Supply					
Voltage		2.7 to 6		V	Operating limits
Current		8		mA	V_{CC}=3.0V
	8	10	12	mA	V_{CC}=5.0V

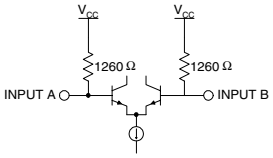
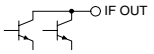
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Pin	Function	Description (Demodulator Configuration)	Interface Schematic
1	I INPUT A	When the RF2703 is configured as a Quadrature Demodulator, both mixers are driven by the IF. Whether driving the mixers single-endedly (as shown in the application schematic) or differentially, the A Inputs (pins 1 and 3) should be connected to each other. Likewise, both B Inputs (pins 2 and 4) should be connected to each other. This ensures that the IF will reach each mixer with the same amplitude and phase, yielding the best I and Q output amplitude and quadrature balance. Note that connecting the inputs in parallel changes the input impedance (see the Gilbert Cell mixer equivalent circuit). The single-ended input impedance (as shown in the application circuit) becomes 630Ω, but in the balanced configuration, the input impedance would remain 1260Ω. The mixers are Gilbert Cell designs with balanced inputs. The equivalent schematic for one of the mixers is shown on the following page. The input impedance of each pin is determined by the 1260Ω resistor to V_{CC} in parallel with a transistor base. Note from the schematic that all four input pins have an internally set DC bias. For this reason, all four inputs (pins 1 through 4) should be DC blocked. The capacitance values of the blocking capacitors is determined by the IF frequency. When driving single-endedly, both the series (pins 1 and 3) and shunt (pins 2 and 4) blocking capacitors should be low impedances, relative to the 630Ω input impedance.	
2	I INPUT B	Same as pin 1, except complementary input.	See pin 1.
3	Q INPUT A	Same as pin 1, except Q Buffer Amplifier.	See pin 1.
4	Q INPUT B	Same as pin 3, except complementary input.	See pin 1.
5	BG OUT	Band Gap voltage reference output. This voltage output is held constant over variations in supply voltage and operating temperature and may be used as a reference for other external circuitry. This pin should not be loaded such that the sourced current exceeds 1mA. This pin should be bypassed with a large (0.1μF) capacitor.	
6	I IF OUT	This pin is not used in the Demodulator Configuration, but must be connected to V_{CC} in order to properly bias the I mixer.	
7	Q IF OUT	Same as pin 6, except Q mixer.	Same as pin 6.
8	Q OUT	Q Mixer's Baseband Output. This pin is NOT internally DC blocked and has DC present due to internal biasing. This is an emitter-follower type output with an internal 2kΩ pull-down resistor. Even though the AC output impedance is ~50Ω, this pin is intended to drive only high impedance loads such as an opamp or an ADC. The output transistor is NOT biased such that it can drive a large signal into a 50Ω load. DC coupling of this output is permitted provided that the DC impedance to ground, which appears in parallel with the internal pull-down resistor, is significantly greater than 2kΩ.	
9	I OUT	Same as pin 8, except Q Mixer's Baseband Output.	Same as pin 8.
10	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
11	GND	Same as pin 10.	
12	GND	Same as pin 10.	

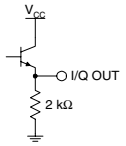
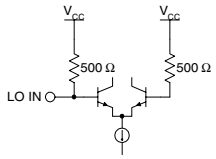
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Pin	Function	Description (Demodulator Configuration)	Interface Schematic
13	LO INPUT	High impedance, single-ended modulator LO input. The LO applied to this pin is frequency divided by a factor of 2 and becomes the "Carrier". For direct demodulation, the Carrier is equal in frequency to the center of the input IF spectrum (except in the case of SSB/SC). The input impedance is determined by an internal 500Ω bias resistor to V_{CC}. An external blocking capacitor should be provided if the pin is connected to a device with DC present. Matching the input impedance is typically achieved by adding a 51Ω resistor to ground on the source side of the AC coupling capacitor. For the LO input, maximum power transfer is not critical. The internal LO switching circuits are controlled by the voltage, not power, into the part. In cases where the LO source does not have enough available voltage, a reactive match (voltage transformer) can be used. The LO circuitry consists of a limiting amplifier followed by a digital divider. The limiting amp ensures that the flip-flop type divider is driven with a square wave over a wide range of input levels. Because the flip-flop uses the rising and falling edges of the limiter output, the quadrature accuracy of the Carrier supplied to the mixers is directly related to the duty cycle, or equivalently to the even harmonic content, of the input LO signal. In particular, care should be taken to ensure that the 2xLO level input to this pin is at least 20dB below the LO level. Otherwise, the LO input is not sensitive to the type of input wave form, except for IF frequencies below ~2.5MHz, in which case the LO input should be a square wave, in order to ensure proper triggering of the flip-flops. IF frequencies below 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.	
14	VCC	Voltage supply for the entire device. This pin should be well bypassed at all frequencies (IF, LO, Carrier, Baseband) that are present in the part.	

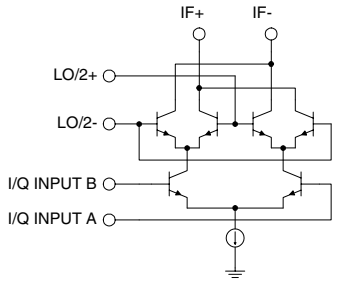
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Pin	Function	Description (Modulator Configuration)	Interface Schematic
1	I INPUT A	When the RF2703 is configured as a Quadrature Modulator, each mixer is driven by an independent baseband modulation channel (I and Q). The mixers can be driven single-endedly (as shown in the modulator application circuit) or differentially. When driving single-endedly, the B Inputs (pins 2 and 4) should be connected to each other. This ensures that the baseband signals will reach each mixer with the same DC reference, yielding the best carrier suppression. Note that the input impedance changes according to the drive mode (see the mixer equivalent circuit on the previous page). The single-ended input impedance (as shown in the modulator application circuit) is 1200Ω for each of the two inputs. In the balanced configuration, the input impedance would be 2400Ω for each of the two inputs. The mixers are Gilbert Cell designs with balanced inputs. The equivalent schematic for one of the mixers is shown on the previous page. The input impedance of each pin is determined by the 1200Ω resistor to V_{CC} in parallel with a transistor base. Note from the schematic that all four input pins have an internally set DC bias. For this reason, all four inputs (pins 1 through 4) should be DC blocked. The capacitance values of the blocking capacitors is determined by the baseband frequency. When driving single-endedly, both the series (pins 1 and 3) and shunt (pins 2 and 4) blocking capacitors should be low impedances, relative to the input impedance. DC bias voltages may be supplied to the inputs pins, if required, in order to increase the amount of carrier suppression. For example, the DC levels on the reference inputs (pins 2 and 4) may be offset from each other by adding different resistor values to ground. These resistors should be larger than 2kΩ. Note from the mixer schematic that all four input pins have an internally set DC bias. If DC bias is to be supplied, the allowable ranges are limited. For 5V applications, the DC reference on both I pins or both Q pins must not go below 2.7V_{DC}, and in no case should the DC voltage on any of the four pins go below 2.0V_{DC} or above 5.5V_{DC}. IF a DC reference is to be supplied, the source must also be capable of sinking current. If optimizing carrier suppression further is not a concern, it is recommended that all four inputs (pins 1 through 4) be DC blocked.	
2	I INPUT B	Same as pin 1, except complementary input.	See pin 1.
3	Q INPUT A	Same as pin 1, except Q Buffer Amplifier.	See pin 1.
4	Q INPUT B	Same as pin 3, except complementary input.	See pin 1.
5	BG OUT	Band Gap voltage reference output. This voltage output is held constant over variations in supply voltage and operating temperature and may be used as a reference for other external circuitry. This pin should not be loaded such that the sourced current exceeds 1mA. This pin should be bypassed with a large (0.1μF) capacitor.	
6	I IF OUT	Connecting pins 6 and 7 to each other accomplishes the summing function of the upconverted I and Q channels. In addition, because these outputs are open collector type, they must be connected to V_{CC} in order to properly bias the Gilbert Cell mixers. Maximum gain and output power occur when the load on these two pins is ~1200Ω. In most applications the impedance of the next stage will be lower and a reactive impedance transforming match should be used if maximum gain and output level are of concern. Biasing, DC blocking, and impedance transformation can simultaneously be achieved with the shunt-L / series-C topology shown in the Application Circuit. The inductance and capacitance values are chosen to achieve a specific impedance transforming ratio at a specific IF frequency. For applications where the gain is not as critical, a 1200Ω resistor may be added in parallel with a choke inductor in place of the matching inductor. If neither gain nor output level is critical, the inductor may be replaced with a resistor that sets the desired source impedance to drive the next stage. If the next stage is an "open" at DC, the blocking capacitor may be eliminated.	

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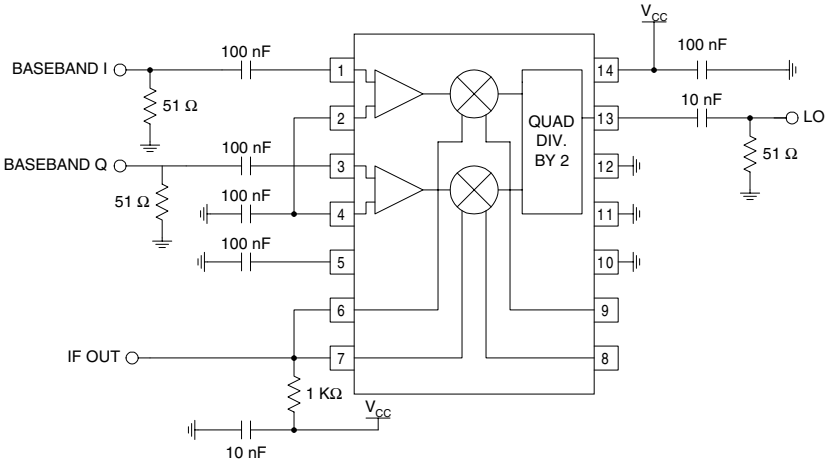
Pin	Function	Description (Demodulator Configuration)	Interface Schematic
7	Q IF OUT	Same as pin 6, except complementary input.	Same as pin 6.
8	Q OUT	Pins 8 and 9 are not used in a normal quadrature modulator application, and are left unconnected. Note, however, that the outputs of each of these pins are independent upconverted I and Q channels. These signals may be useful in other applications where independent IF channels are needed. Also note that these outputs are optimized as baseband outputs for the demodulator configuration. As a result, the gain rolls-off quickly with increasing frequency. This gain roll-off will limit the usefulness of these pins as independent I and Q upconverters. If these outputs are to be used, please refer to the Demodulator pin descriptions regarding load impedances.	
9	I OUT	Same as pin 8, except Q Mixer's Output.	Same as pin 8.
10	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
11	GND	Same as pin 10.	
12	GND	Same as pin 10.	
13	LO INPUT	High impedance, single-ended modulator LO input. The LO applied to this pin is frequency divided by a factor of 2 and becomes the "Carrier". For modulation, the Carrier is the center of the modulated output spectrum (except in the case of SSB/SC). The input impedance is determined by an internal 500Ω bias resistor to V_{CC}. An external blocking capacitor should be provided if the pin is connected to a device with DC present. Matching the input impedance is typically achieved by adding a 51Ω resistor to ground on the source side of the AC coupling capacitor. For the LO input, maximum power transfer is not critical. The internal LO switching circuits are controlled by the voltage, not power, into the part. In cases where the LO source does not have enough available voltage, a reactive match (voltage transformer) can be used. The LO circuitry consists of a limiting amplifier followed by a digital divider. The limiting amp ensures that the flip-flop type divider is driven with a square wave over a wide range of input levels. Because the flip-flop uses the rising and falling edges of the limiter output, the quadrature accuracy of the Carrier supplied to the mixers is directly related to the duty cycle, or equivalently to the even harmonic content, of the input LO signal. In particular, care should be taken to ensure that the 2xLO level input to this pin is at least 20dB below the LO level. Otherwise, the LO input is not sensitive to the type of input wave form, except for IF frequencies below ~2.5MHz, in which case the LO input should be a square wave, in order to ensure proper triggering of the flip-flops. IF frequencies below 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.	
14	VCC	Voltage supply for the entire device. This pin should be well bypassed at all frequencies (IF, LO, Carrier, Baseband) that are present in the part.	

Gilbert Cell Mixer Equivalent Circuit

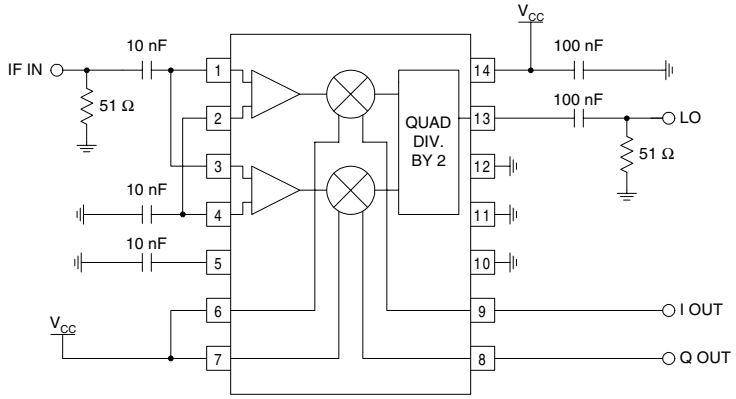


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Application Schematic
Modulator Configuration



Application Schematic
Demodulator Configuration



5
MODULATORS AND UPCONVERTERS

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RF9958

CDMA/FM TRANSMIT MODULATOR, IF AGC, AND UPCONVERTER

Typical Applications

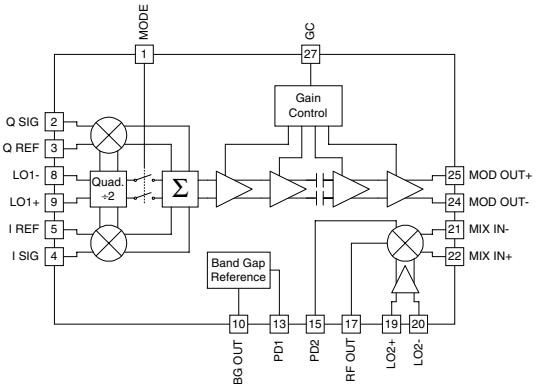
- CDMA/FM Cellular Systems
- CDMA PCS Systems
- Wireless Local Loop Systems
- Spread Spectrum Cordless Phones
- High Speed Data Modems
- General Purpose Digital Transmitters

Product Description

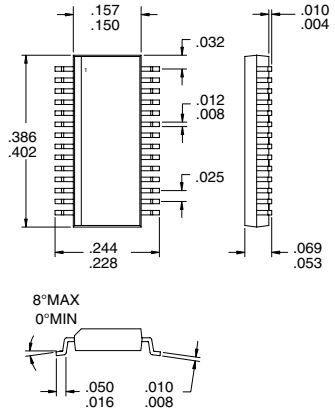
The RF9958 is an integrated complete Quadrature Modulator, IF AGC amplifier, and Upconverter designed for the transmit section of dual-mode CDMA/FM cellular and PCS applications. It is designed to modulate baseband I and Q signals, amplify the resulting IF signals while providing 95dB of gain control range, and perform the final upconversion to UHF. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 Interim Standard for CDMA cellular communications. This circuit is designed as part of RFMD's newest CDMA Chip Set, which also includes the RF9957 CDMA/FM Receive IF AGC and Demodulator. The IC is manufactured on an advanced 15GHz F_T Silicon Bipolar process, and is supplied in a 28-lead plastic SSOP package.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-28

Features

- Supports Dual Mode Operation
- Digitally Controlled Power Down Modes
- 2.7V to 3.3V Operation
- Digital First LO Quadrature Divider
- Double-Balanced UHF Upconvert Mixer
- IF AGC Amp with 95 dB Gain Control

Ordering Information

RF9958	CDMA/FM Transmit Modulator, IF AGC, and Upconverter
RF9958 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

5 MODULATORS AND UPCONVERTERS

RF9958

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC} + 0.7	V
I and Q Levels, per pin	1	V_{PP}
LO1 Level, balanced	+3	dBm
LO2 Level, balanced	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

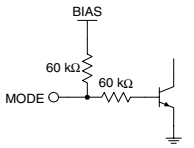
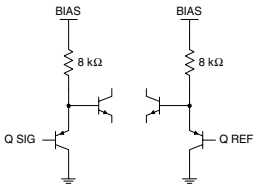
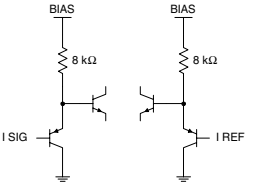
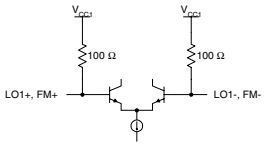
Caution! ESD sensitive device.

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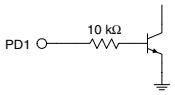
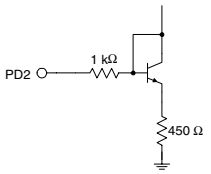
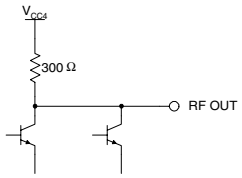
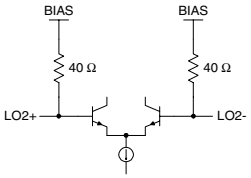
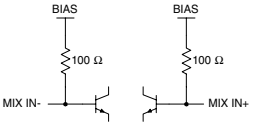
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q Modulator & AGC					T=25 °C, V_{CC}=3.0V, Z_{LOAD}=50Ω, LO1 = -8dBm @ 260 MHz, LO2 = -3dBm @ 960MHz, I SIG = Q SIG = 300mV$_{PP}$, RF Output externally matched
I/Q Input Frequency Range		0 to 20		MHz	Balanced
I/Q Input Impedance	50	80	110	kΩ	Balanced
I/Q Input Reference Level		0.6		V_{DC}	Per Pin
LO1/FM Frequency Range		240 to 360		MHz	
LO1/FM Input Level	-15	-8	-5	dBm	
LO1/FM Input Impedance	170	200	230	Ω	Balanced
Sideband Suppression	35	40		dBc	I/Q Amplitude adjusted to within ±20mV
		30		dBc	Unadjusted
Carrier Suppression	40	50		dBc	I/Q DC Offset adjusted to within ±20mV
		30		dBc	Unadjusted
Max Output, FM Mode	+2.5	+4		dBm	V_{GC}=2.5 V_{DC}, T=-20°C to +85°C
Max Output, CDMA Mode	-3	0		dBm	V_{GC}=2.5 V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
	-2	0		dBm	ISIG=QSIQ=300mVpp @ 100kHz
Min Output, CDMA Mode		-95	-89	dBm	V_{GC}=0.5 V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
Output Power Accuracy	-3		+3	dB	T=-20 to +85 °C, Ref=25 °C
	-2		+2	dB	1.4V≤GC≤2.5
Adjacent Channel Power Rejection @ 885kHz		-55		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Adjacent Channel Power Rejection @ 1.98MHz		-67		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Output Noise Power		-116	-111	dBm/Hz	P_{OUT} = -3 dBm, T=-20°C to +85°C
		-137	-132	dBm/Hz	P_{OUT} = -23 dBm, T=-20°C to +85°C
		-164	-159	dBm/Hz	P_{OUT} < -70 dBm, T=-20°C to +85°C
Output Impedance	170	200	230	Ω	Balanced
Power Dissipation			150	mW	T=-20°C to +85°C
UHF Upconverter					Output externally matched
Conversion Gain	-1	0.5		dB	
Noise Figure (SSB)		15		dB	
Output IP3		+14		dBm	
IF Input Impedance	170	200	230	Ω	Balanced
IF Input Frequency Range		120 to 180		MHz	
LO2 Input Impedance		50		Ω	Single Ended
LO2 Input Level	-6	-3	0	dBm	
LO2 Input Frequency Range		700 to 1100		MHz	
RF to LO2 Isolation		20		dB	

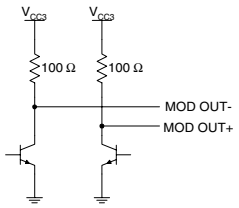
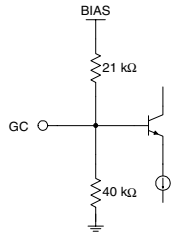
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		43		mA	Modulator and AGC only, CDMA Mode
Current Consumption		20		mA	Mixer Only
Power Down Current			20	µA	
VPD HIGH Voltage	V_{CC}-0.7			V	
VPD LOW Voltage			0.5	V	

RF9958

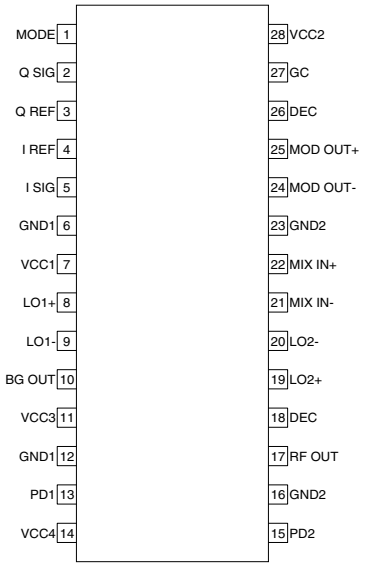
Pin	Function	Description	Interface Schematic
1	MODE	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" ($\geq V_{CC}$-0.7V_{DC}) selects CDMA mode. A logic "low" (<0.5V_{DC}) selects FM mode. In FM mode, this switch enables the FM amplifier and turns off the I&Q modulator. The impedance on this pin is 30kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
2	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
3	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the Q SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 2.
4	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the I SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 5.
5	I SIG	Baseband input to the I mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
6	GND1	Ground connection for all baseband circuits including bandgap, AGC, flip-flop, modulator and FM amp. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC1	Supply Voltage for the LO1 flip-flop and limiting amp only. This supply is isolated to minimize the carrier leakage. A 1nF external bypass capacitor is required, and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	LO1+, FM+	One half of the balanced modulator LO1 input. The other half of the input, LO1-, is AC grounded for single-ended input applications. The frequency on these pins is divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 100Ω (balanced is 200Ω). This pin is NOT internally DC blocked. An external blocking capacitor (1nF recommended) must be provided if the pin is connected to a device with DC present. When FM mode is selected, the output of the flip-flop divider circuit is switched to the AGC amplifier inputs and the modulator mixers are not used. Note that the frequency deviation input here will be reduced by a factor of two, due to the frequency divider operation.	
9	LO1-, FM-	One half of the balanced modulator LO1 input. In single-ended applications (100Ω input impedance), this pin is AC grounded with a 1nF capacitor.	See pin 8.

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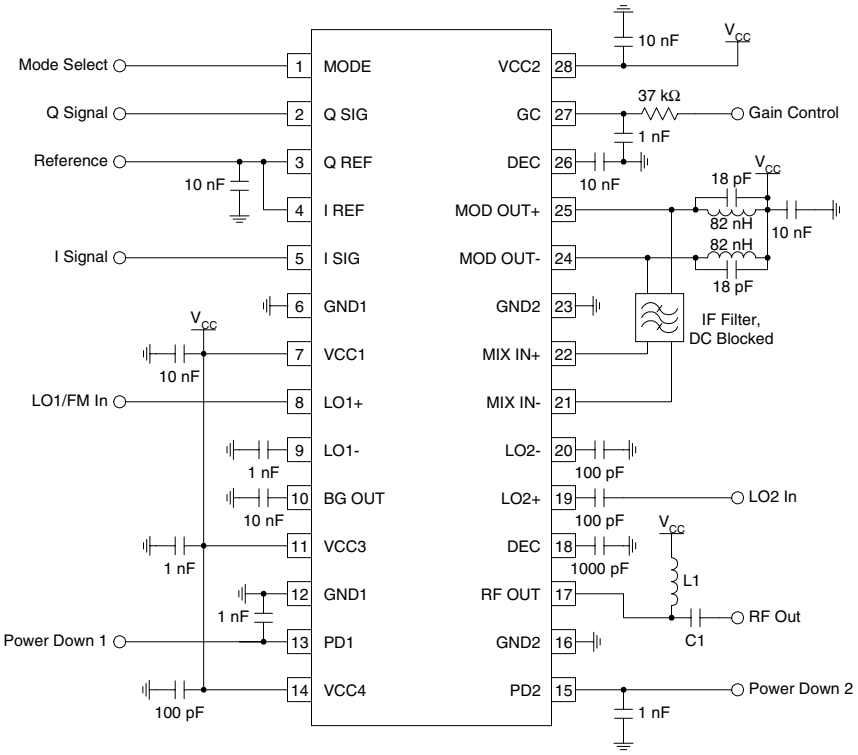
10	**BG OUT**	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 1nF external bypass capacitor is required.	
11	**VCC3**	Supply voltage for the AGC and the Bandgap circuitry. A 1nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
12	**GND1**	Same as pin 6.	
13	**PD1**	Power down control for overall circuit. When logic "high" ($\geq V_{CC}$-0.7V), all circuits are operating; when logic "low" (≤0.5V), all circuits are turned off. The input impedance of this pin is >10kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
14	**VCC4**	Supply for the mixer stage only. The supply for the mixer is separated to maximize IF to RF isolations and reduce the carrier leakage. A 100pF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
15	**PD2**	Power down control for mixer only. When connected to pin 10 (BG OUT) the mixer circuits are operating; when connected to ground (≤0.5V), the mixer is turned off but all other circuits are operating. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
16	**GND2**	Ground connection for the mixer stage. Keep traces physically short and connect immediately to ground plane for best performance.	
17	**RF OUT**	RF output pin. An external shunt inductor to V_{CC} plus a series blocking/ matching capacitor are required for 50Ω output.	
18	**DEC**	Current Mirror decoupling pin. A 1000pF external capacitor is required to bypass this pin. The ground side of the bypass capacitors should connect immediately to ground plane.	
19	**LO2+**	One half of the balanced mixer LO2 input. In single-ended applications, the other half of the input, LO2- is AC grounded. This is a 50Ω impedance port. This pin is NOT internally DC blocked. An external blocking capacitor (100pF recommended) must be provided if the pin is connected to a device with DC present.	
20	**LO2-**	One half of the balance mixer LO2 input. In single ended applications, this pin is AC grounded with a 100pF capacitor.	See pin 19.
21	**MIX IN-**	One half of the 200Ω balanced impedance input to the mixer stage. This pin is NOT internally DC blocked. An external blocking capacitor (2200pF recommended) must be provided if the pin is connected to a device with DC present. If no IF filter is needed this pin may be connected to MOD OUT+ through a DC blocking capacitor. An appropriate matching network may be needed if an IF filter is used.	
22	**MIX IN+**	Same as pin 21, except complementary input.	See pin 21.

23	**GND2**	Same as pin 16.	
24	**MOD OUT-**	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. If no filtering is required, this pin can be connected to the MIX IN- pin through a DC blocking capacitor. This pin requires an inductor to V_{CC} to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
25	**MOD OUT+**	Same as pin 24, except complementary output.	See pin 24.
26	**DEC**	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
27	**GC**	Analog gain control for AGC amplifiers. Valid control voltage ranges are from $0.5V_{DC}$ to $2.5V_{DC}$. The gain range for the AGC is 88dB. These voltages are valid ONLY for a 37kΩ source impedance. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
28	**VCC2**	Supply for the modulator stage only. A 10nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

RF9958 Pin-Out



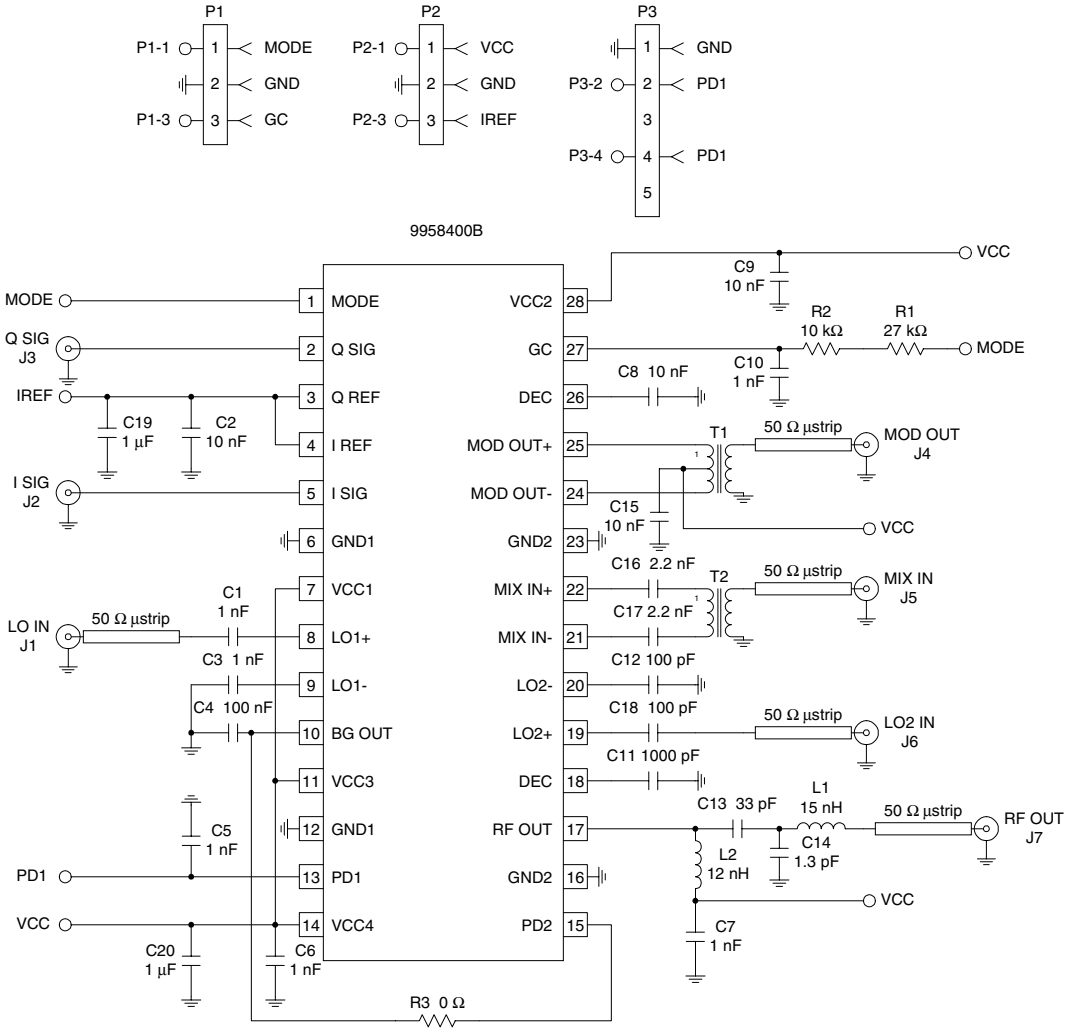
Application Schematic



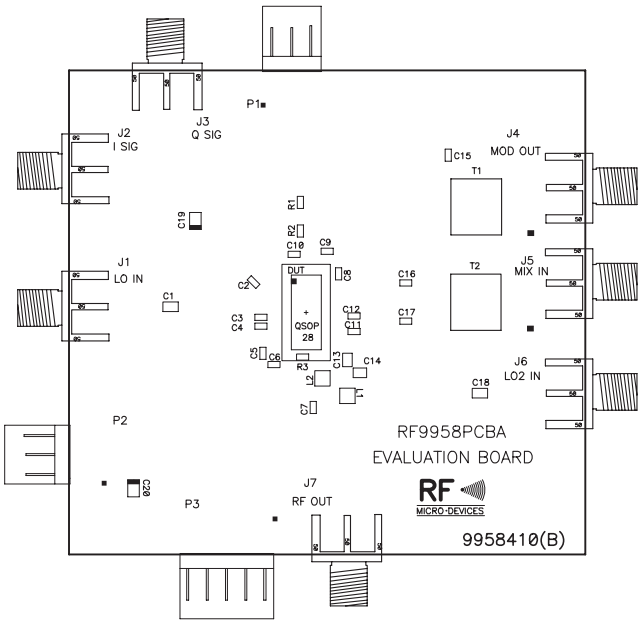
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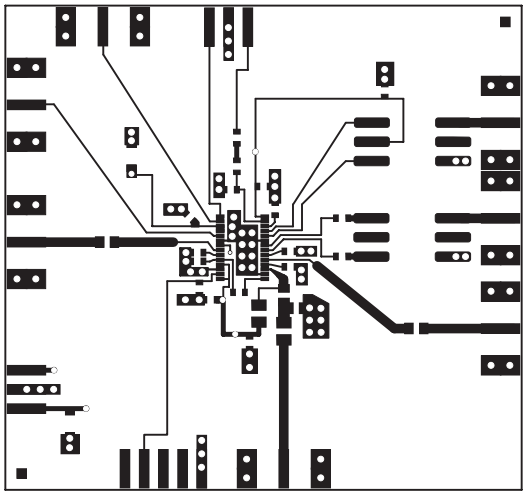
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

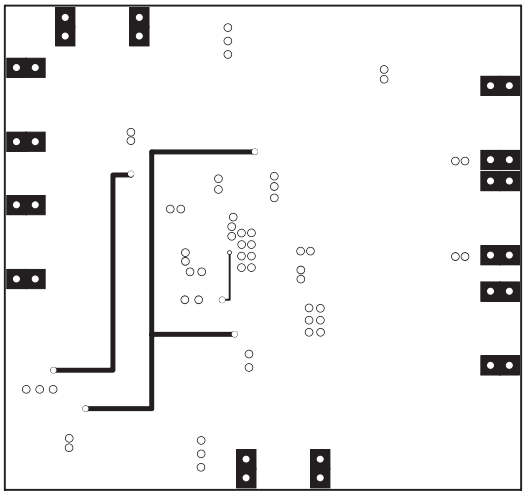


Evaluation Board Layout
2.689" X 2.521"

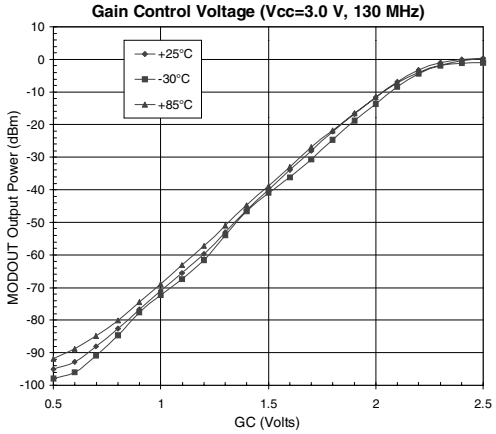




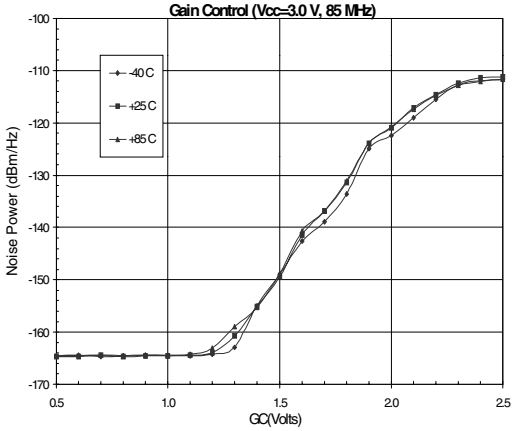
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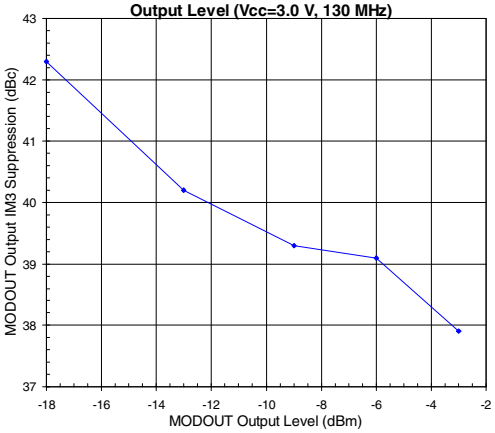
RF9958 MODOUT Output Power vs. Gain Control Voltage (Vcc=3.0 V, 130 MHz)



RF9958 MODOUT Noise Power vs. Gain Control (Vcc=3.0 V, 85 MHz)



RF9958 MODOUT IM3 Suppression vs. Output Level (Vcc=3.0 V, 130 MHz)



6 Mixers

Part	Description	Frequency (MHz)	IF (MHz)	Vcc (Volts)	Icc (mA)	Package	Page
RF2456	CDMA/FM Downconverter	500 to 1100	250	2.7 to 4.0	18	SSOP-16	6-1
RF2466	3V CDMA/FM Mixer	500 to 1100	0.1 to 250	2.7 to 4.0	18	MLF16	6-7
RF2608	CDMA/FM Upconverter/BPSK Modulator	500 to 1500	200	2.7 to 5.0	22	SOP-8	6-15
RF2628	CDMA/FM Upconverter/BPSK Modulator	500 to 1500	200	2.7 to 5.0	22	MSOP-8	6-19
RF2638	CDMA Upconverter/BPSK Modulator	500 to 2500	300	2.7 to 3.3	25	MSOP-8	6-25
RF2639	Upconverter/BPSK Modulator	500 to 2500	300	2.7 to 3.3	7	MSOP-8	6-31
RF2640	3V 900MHz Upconverter/ Driver Amplifier	824 to 849	180	2.7 to 3.3	45	MSOP-10	6-37
RF2641	CDMA Upconverter/BPSK Modulator	500 to 2500	DC to 300	2.7 to 3.3	13	MSOP-8	6-41
RF2642	3V 900MHz Upconverter/ Driver Amplifier with Bypass Mode	824 to 849	130	2.7 to 3.3	15	MLF16	6-49
RF9908	CDMA/FM Upconverter/BPSK Modulator	500 to 1500	200	3.6	18	SOP-8	6-57
RF9938	PCS Upconverter/BPSK Modulator	1200 to 2500	200	3.6	27	SOP-8	6-61

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RF2456

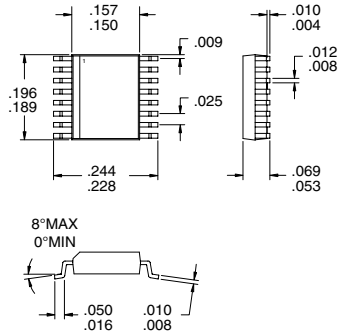
CDMA/FM DOWNCONVERTER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

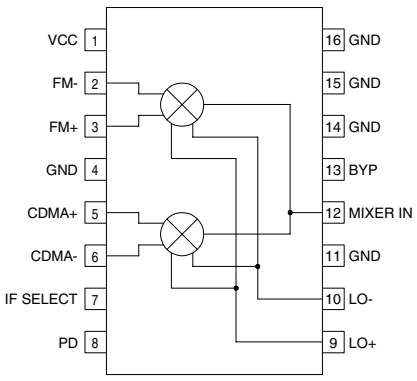
The RF2456 is a receiver dual downconverter designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to down-convert RF signals while providing 13dB gain in CDMA mode, and 7dB gain in FM mode. It also features digital control of IF output selection and power down mode. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-16.



Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: SSOP-16



Functional Block Diagram

Features

- Dual Mode CDMA/AMPS
- Dual Mode JCDMA/TACS
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation
- Power Down Mode

Ordering Information

RF2456	CDMA/FM Downconverter
RF2456 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2456

Absolute Maximum Ratings

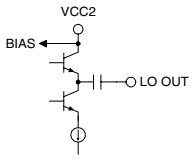
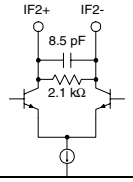
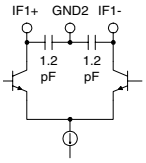
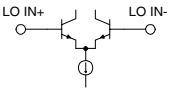
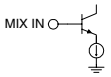
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

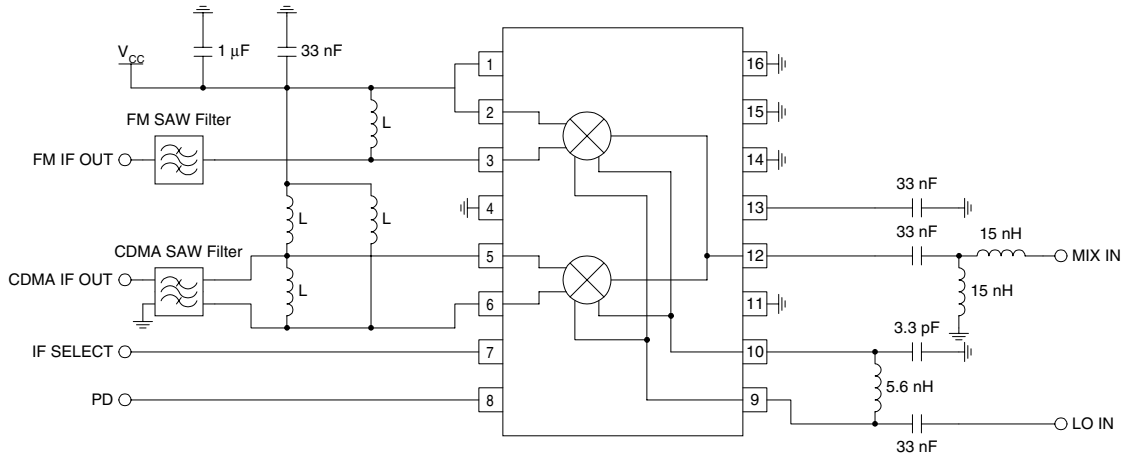
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=881MHz, LO=966MHz @ 0dBm, IF1= CDMA, IF2=FM
RF Frequency Range		200 to 1000		MHz	
LO Frequency Range		500 to 1100		MHz	
IF Frequency Range		0.1 to 250		MHz	
Conversion Gain	12.5	13		dB	IF1, 1kΩ balanced load.
	6	7		dB	IF2, 870Ω load.
Noise Figure		12		dB	IF1 single sideband.
		13		dB	IF2 single sideband
Input VSWR		<1.5:1			IF1 with external matching
		<2:1			IF2 with external matching
Input IP3		+3.5		dBm	IF1
		+10		dBm	IF2
Input P1dB		-7		dBm	IF1
		-4		dBm	IF2
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
LO Input					
LO Input Range	-10	-3	0	dBm	
LO IN to RF Input Rejection		20		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			IF1 with external matching network
		2.5			IF2 with external matching network
Power Supply					
Voltage	2.7	3.0	4.0	V	
Current Consumption		20	18	mA	IF1 selected
		15	16	mA	IF2 selected

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Pin	Function	Description	Interface Schematic
1	VCC	Supply Voltage for the mixers, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
2	IF2-	Same as pin 3, except complimentary output. For typical single ended operation, this pin is connected directly to V_{CC}.	See pin 3.
3	IF2+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85MHz. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
4	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
5	IF 1+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
6	IF 1-	Same as pin 5, except complementary output.	See pin 5.
7	IF SELECT	Control line for IF out select. A logic “low” enables the FM output. A logic “high” enables the CDMA output. The threshold voltage is 1.6V, and the pin draws less than 50µA when selected.	
8	PD	Power down pin. A logic “low” turns the part off. A logic “high” (>1.6V) turns the part on. In addition, pin 7 (IF SELECT) should also be taken low during power down.	
9	LO IN+	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 10 is bypassed to ground.	
10	LO IN-	Same as pin 9 except complementary input.	See pin 9.
11	GND	Ground connection for the mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
12	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
13	BYP	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
14	GND	Same as pin 4.	
15	GND	Same as pin 4.	
16	GND	Same as pin 4.	

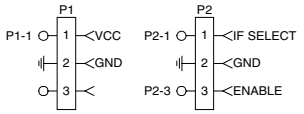
Application Schematic

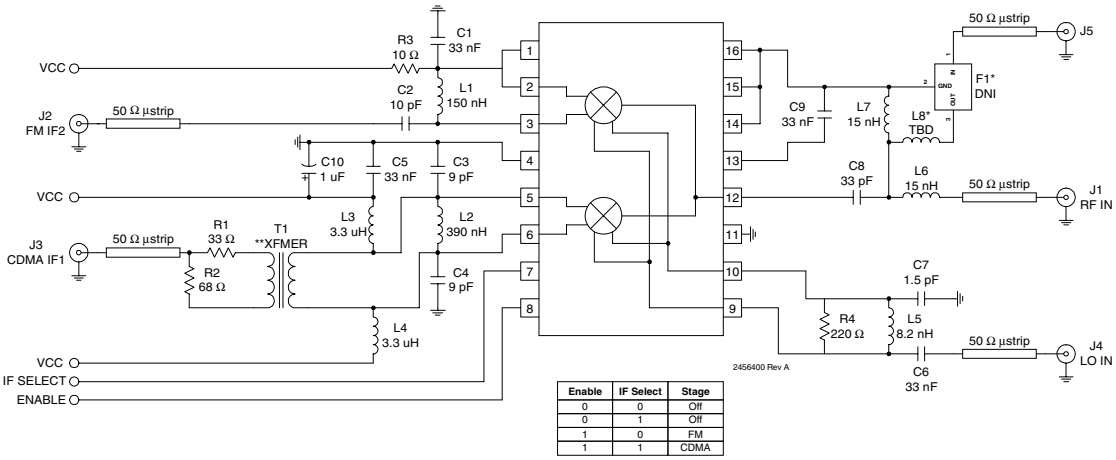


Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

NOTE:
**Core: Fair-Rite Balun #2865002402
L12: 3 turns #30 AWG (Green)
L34: 12 turns #32 AWG (Red)
One turn = One pass through BOTH holes winding starts and finishes on same end of core.
L12 and L34 exit opposite ends of core.



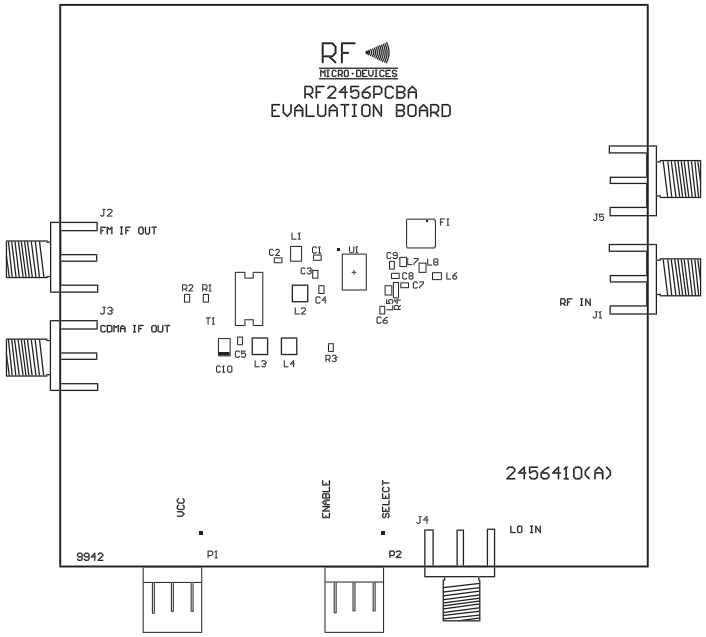


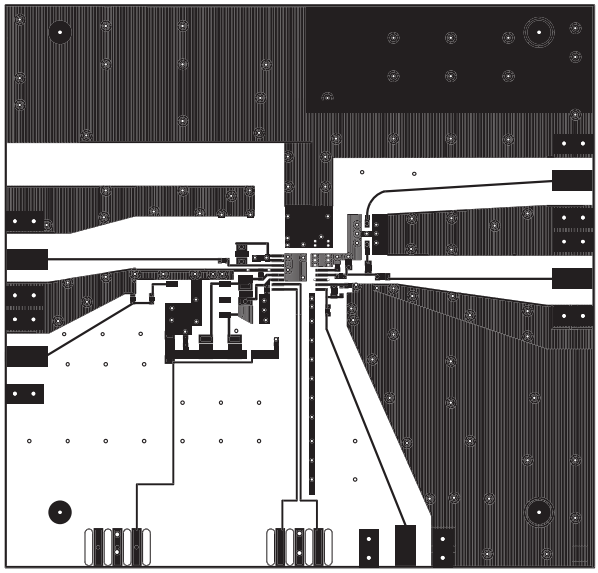
Enable	IF Select	Stage
0	0	Off
0	1	Off
1	0	FM
1	1	CDMA

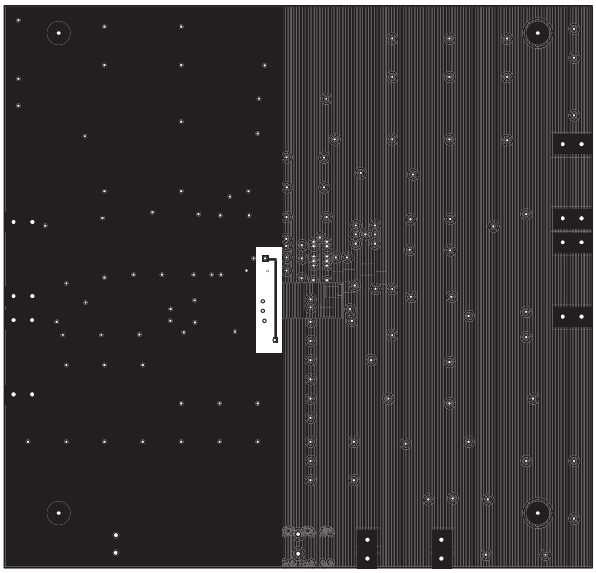
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Evaluation Board Layout
Board Size 3.070" X 2.928"

Board Thickness 0.056”, Board Material FR-4







RF MICRO·DEVICES

RF2466

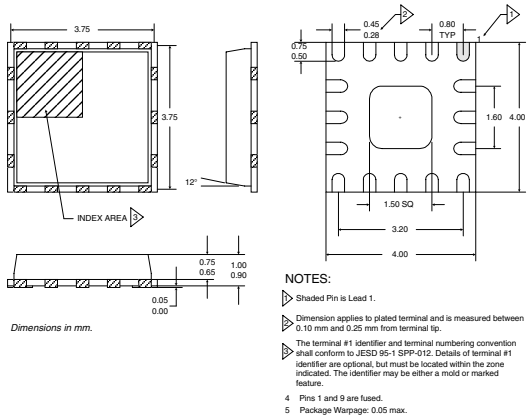
3V CDMA/FM MIXER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

The RF2466 is a receiver dual downconverter designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to down-convert RF signals while providing 14dB gain in CDMA mode and 7dB gain in FM mode. Also, it features IF output selection and power down mode. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process.



Dimensions in mm.

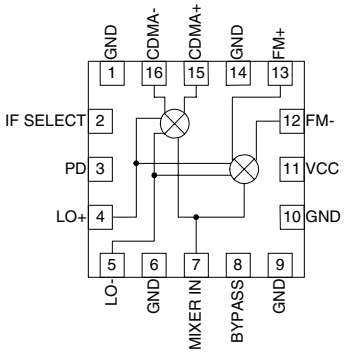
NOTES:

1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MLF16



Functional Block Diagram

Features

- Dual Mode CDMA/AMPS
- Dual Mode JCDMA/TACS
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation
- Power Down Mode

Ordering Information

RF2466	3V CDMA/FM Mixer
RF2466 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2466

Absolute Maximum Ratings

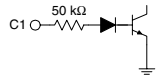
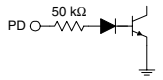
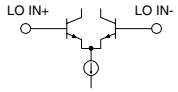
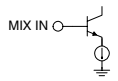
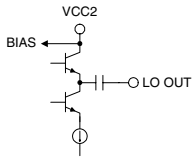
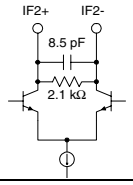
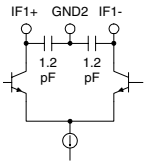
Parameter	Rating	Unit
Supply Voltage		V_{DC}
Input LO and RF Levels		dBm
Operating Ambient Temperature		°C
Storage Temperature		°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=881MHz, LO=966MHz @ 0dBm, IF1= CDMA, IF2=FM
RF Frequency Range		200 to 1000		MHz	
LO Frequency Range		500 to 1100		MHz	
IF Frequency Range		0.1 to 250		MHz	
Conversion Gain	12.5	14		dB	IF1, 1kΩ balanced load.
	6	7		dB	IF2, 870Ω load.
Noise Figure		9		dB	IF1 single sideband.
		10.5		dB	IF2 single sideband
Input VSWR		<1.5:1			IF1 with external matching
		<2:1			IF2 with external matching
Input IP3	+3	+7		dBm	IF1
	+3	+7		dBm	IF2
Input P1dB		-7		dBm	IF1
		-4		dBm	IF2
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
LO Input					
LO Input Range	-10	-3	0	dBm	
LO IN to RF Input Rejection		20		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			IF1 with external matching network
		2.5			IF2 with external matching network
Power Supply					
Voltage	2.7	3.0	4.0	V	
Current Consumption		16	18	mA	IF1 selected
		12	14	mA	IF2 selected

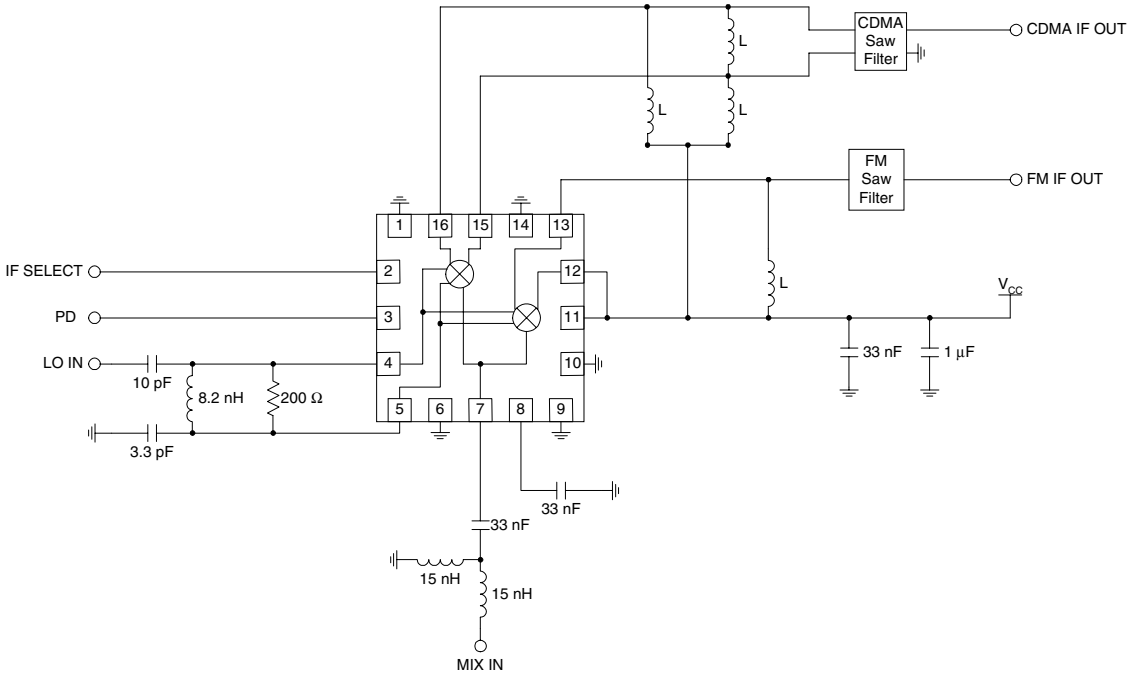
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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	IF SELECT	Control line for IF out select. A logic "low" enables the FM output. A logic "high" enables the CDMA output. The threshold voltage is 1.6V, and the pin draws less than 50µA when selected.	
3	PD	Power down pin. A logic "low" (<1.6V) turns the part off. A logic "high" (>1.6V) turns the part on. In addition, pin 2 (IF SELECT) should also be taken low during power down.	
4	LO+	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 5 is bypassed to ground.	
5	LO-	Same as pin 4 except complementary input.	See pin 4.
6	GND	Ground connection for the mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
7	MIXER IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
8	BYPASS	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
9	GND	Same as pin 1.	
10	GND	Same as pin 1.	
11	VCC	Supply Voltage for the mixers, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
12	FM-	Same as pin 13, except complimentary output. For typical single ended operation, this pin is connected directly to V_{CC}.	See pin 13.
13	FM+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85MHz. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
14	GND	Same as pin 1.	
15	CDMA+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
16	CDMA-	Same as pin 15, except complementary output.	See pin 15.

RF2466

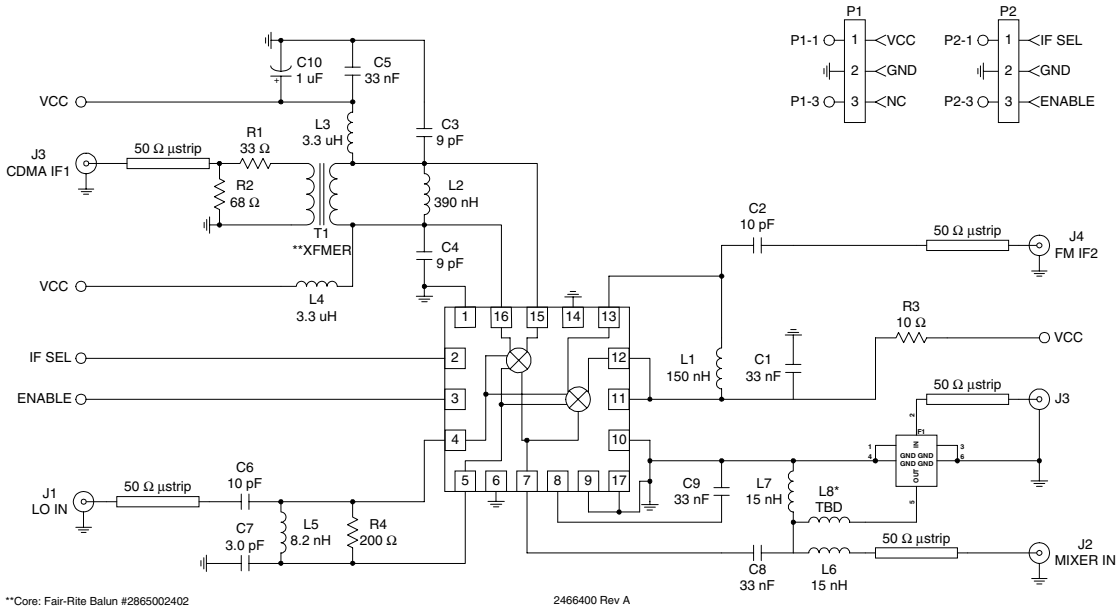
Pin	Function	Description	Interface Schematic
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



2466400 Rev A

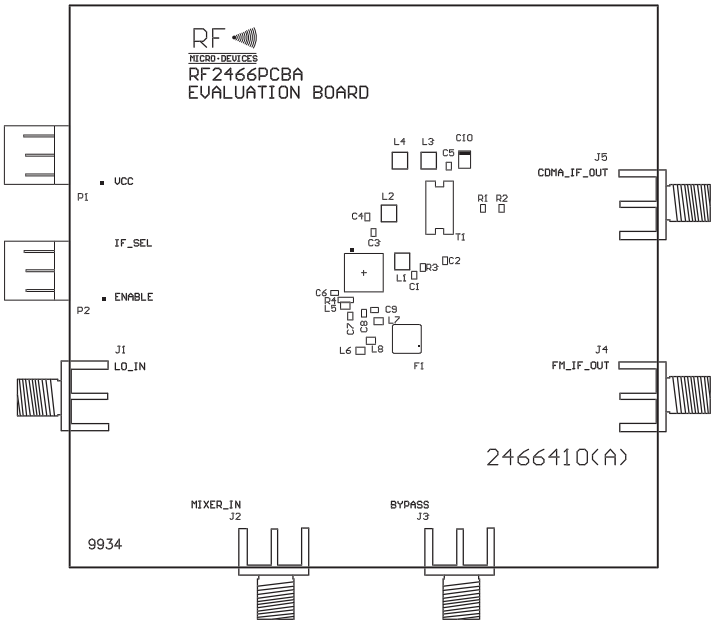
**Core: Fair-Rite Balun #2865002402
L12: 3 turns #30 AWG (Green)
L34: 12 turns #32 AWG (Red)
One turn = one pass through BOTH holes.
Winding starts and finishes on same end of core.
L12 and L34 exit opposite ends of core.
F1: filter

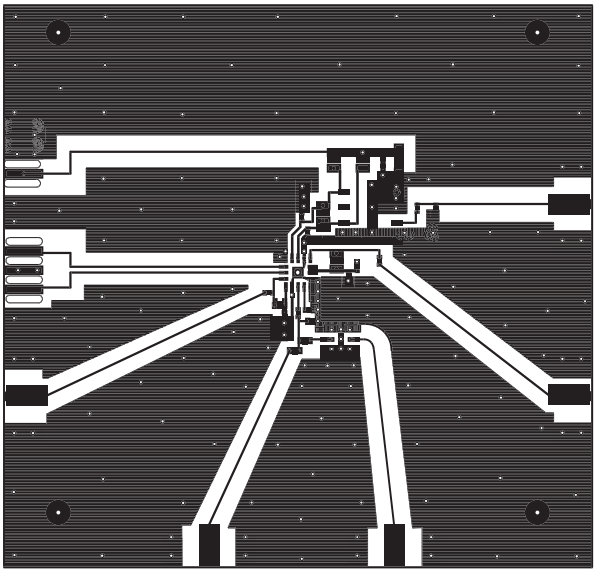
Enable	IF Select	Stage
0	0	Off
0	1	Off
1	0	FM
1	1	CDMA

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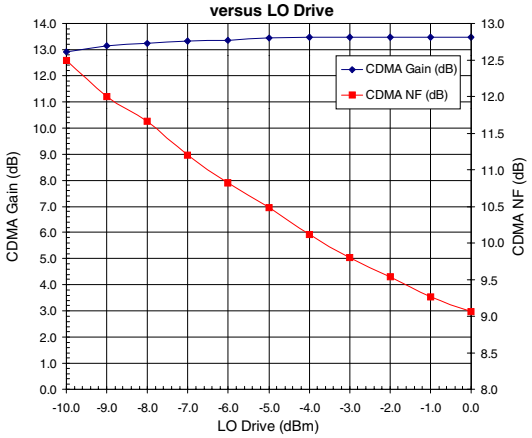
Evaluation Board Layout
Board Size 3.070" x 2.928"

Board Thickness 0.056", Board Material FR-4, Multi-Layer

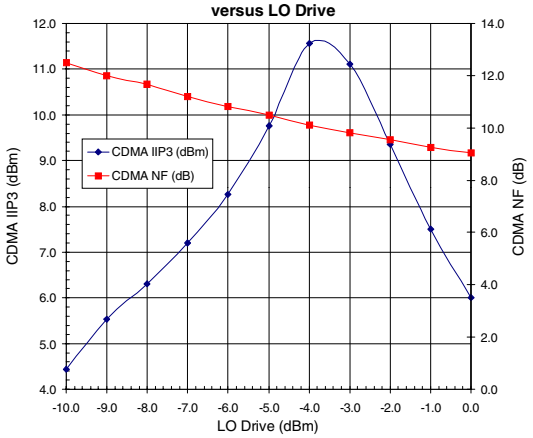




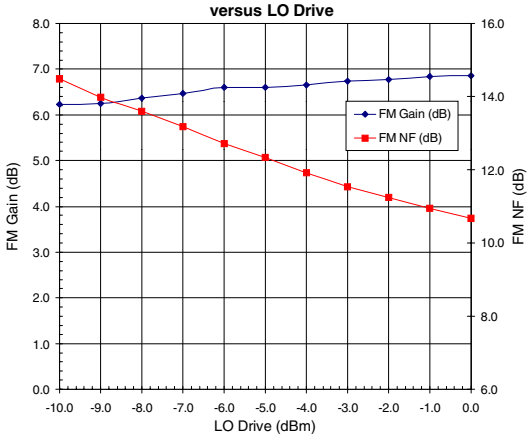
CDMA Gain and Noise Figure versus LO Drive



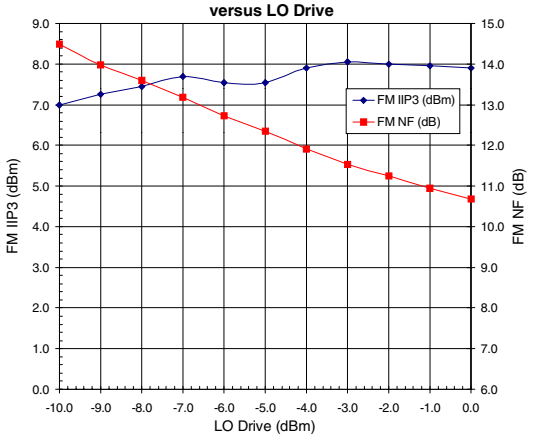
CDMA IIP3 and Noise Figure versus LO Drive



FM Gain and Noise Figure versus LO Drive



FM IIP3 and Noise Figure versus LO Drive



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RF2608

CDMA/FM UPCONVERTER/BPSK MODULATOR

Typical Applications

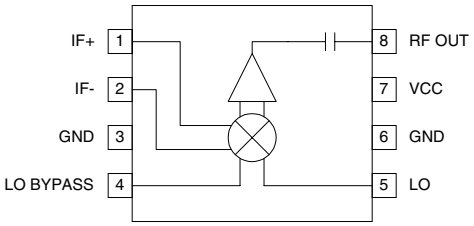
- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- Commercial and Consumer Systems
- Battery Operated Systems

Product Description

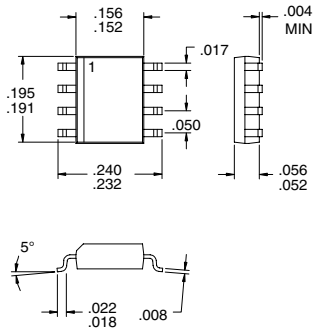
The RF2608 is a complete upconverter designed for CDMA/FM cellular applications. The IC contains a double-balanced mixer stage and an output buffer amplifier stage. This device may also be used to directly BPSK modulate a carrier. The mixer is a Gilbert cell with emitter degeneration resistors to provide high IP_3. The output stage is a class-B, push-pull configuration to reduce the overall current and still provide a good 50Ω output match. The unit operates at a supply voltage of 2.7V to 5.0V and does not require any external matching components other than coupling capacitors. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-8

Features

- Supports Dual Mode Operation
- +7dBm Output Intercept Point
- Single 2.7V to 5.0V Power Supply
- Internally Matched Inputs and Outputs
- Buffered Output
- Double-Balanced Mixer

Ordering Information

RF2608	CDMA/FM Upconverter/BPSK Modulator
RF2608 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2608

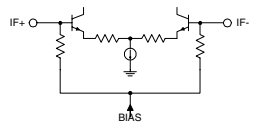
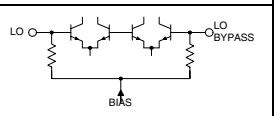
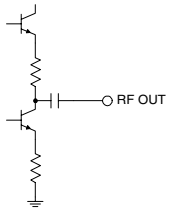
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

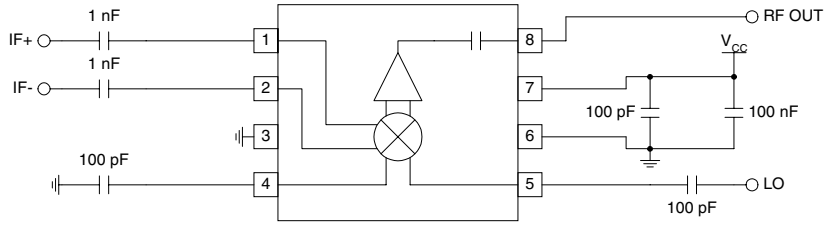
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=840MHz, LO=970MHz @ -2 dBm, IF=130MHz @ -12 dBm
RF Output Frequency Range	500	824 to 849	1500	MHz	
Conversion Gain	-1.3	+0.5	+1.6	dB	
Noise Figure		15	18	dB	
Output IP3	+5	+7		dBm	
Output VSWR		1.6:1	2.0:1		50Ω
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency	DC	130	200	MHz	
Differential Input Impedance	215	265	315	Ω	
IF to RF Output Isolation	21	23		dB	IF=130MHz
IF to LO Isolation	40	50		dB	
LO Input					
LO Frequency Range	300	954 to 979		MHz	
LO Level		-3 to +3		dBm	
LO to RF Output Leakage		-28	-25	dBm	
LO Input VSWR		<1.1:1	2.0:1		50Ω
Power Supply					
Voltage		2.7 to 5.0		V	
Current Consumption	16	22	28	mA	V_{CC}=3.6V

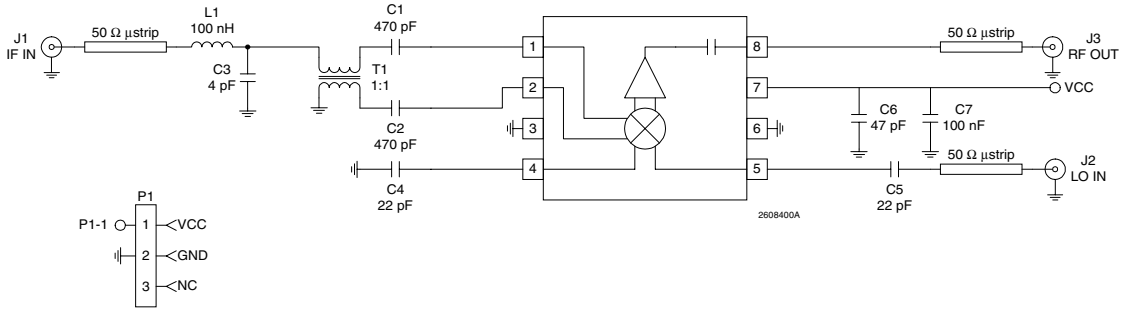
Pin	Function	Description	Interface Schematic
1	IF+	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 265Ω. The IF input should be used differentially when the part is used as a BPSK modulator.	
2	IF-	Same as pin 1, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LO BYPASS	Bypass connection for the LO. A capacitor of 100pF to ground should be connected to this pin	
5	LO	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced, as well single-ended, input impedance is 50Ω.	See pin 4.
6	GND	Same as pin 3.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin. This pin is internally DC blocked. The output impedance is 50Ω.	

Application Schematic



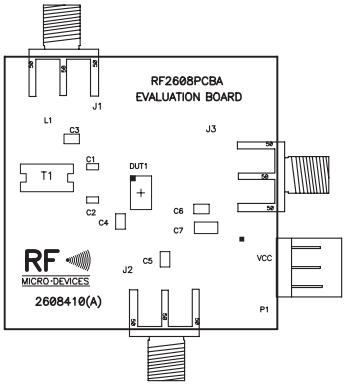
Evaluation Board Schematic

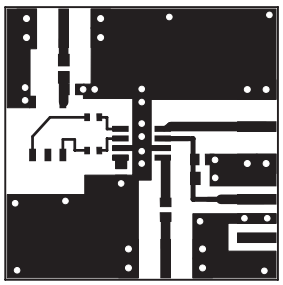
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.420" x 1.420"

Board Thickness 0.031", Board Material FR-4





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RF2628

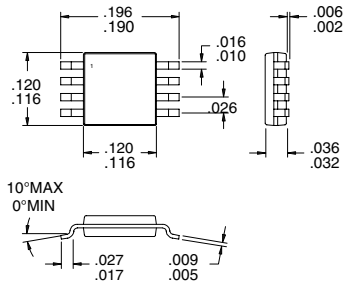
CDMA/FM UPCONVERTER/BPSK MODULATOR

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- Commercial and Consumer Systems
- Battery Operated Systems

Product Description

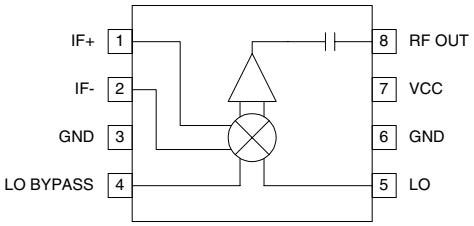
The RF2628 is a complete upconverter designed for CDMA/FM cellular applications. The IC contains a double-balanced mixer stage and an output buffer amplifier stage. This device may also be used to directly BPSK modulate a carrier. The mixer is a Gilbert cell with emitter degeneration resistors to provide high IP_3. The output stage is a class-B, push-pull configuration to reduce the overall current and still provide a good 50Ω output match. The unit operates at a supply voltage of 2.7V to 5.0V and does not require any external matching components other than coupling capacitors. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.



Package Style: MSOP-8

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation
- +9dBm Output Intercept Point
- Single 2.7V to 5.0V Power Supply
- Internally Matched Inputs and Outputs
- Buffered Output
- Double-Balanced Mixer

Ordering Information

RF2628	CDMA/FM Upconverter/BPSK Modulator
RF2628 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2628

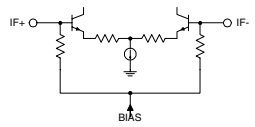
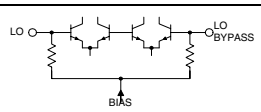
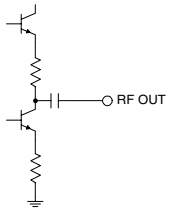
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 5.5	V_{DC}
Input RF Power	+20	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

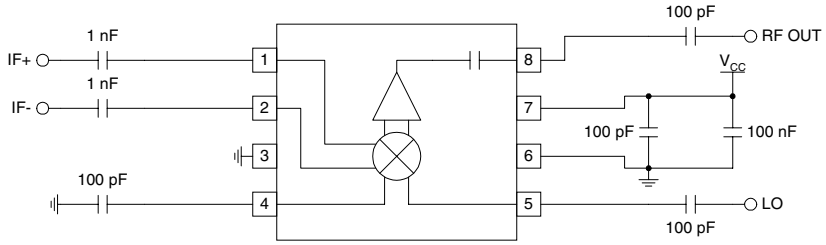
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=840MHz, LO=970MHz @ -2 dBm, IF=130MHz @ -15 dBm
RF Output Frequency Range	500	824 to 849	1500	MHz	
Conversion Gain	-2	0	+1	dB	
Noise Figure		15.5	18	dB	
Output IP3	+5	+9		dBm	
Output VSWR		1.6:1	1.8:1		50Ω
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency	DC	130	500	MHz	
Differential Input Impedance	215	265	315	Ω	
IF to RF Output Isolation	21	23		dB	IF=130MHz
IF to LO Isolation	40	45		dB	
LO Input					
LO Frequency Range	300	954 to 979	1700	MHz	
LO Level		-3 to +3		dBm	
LO to RF Output Leakage	-25	-28		dBm	
LO Input VSWR		1.1:1	1.5:1		50Ω
Power Supply					
Voltage		2.7 to 5.0		V	
Current Consumption		21	24	mA	V_{CC}=3.0V

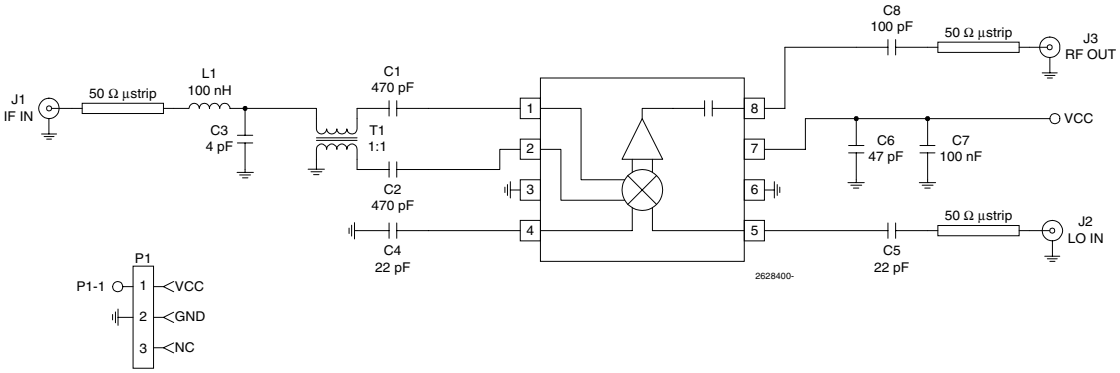
Pin	Function	Description	Interface Schematic
1	IF+	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 265Ω. The IF input should be used differentially when the part is used as a BPSK modulator.	
2	IF-	Same as pin 1, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LO BYPASS	Bypass connection for the LO. A capacitor of 100pF to ground should be connected to this pin	
5	LO	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced, as well single-ended, input impedance is 50Ω.	See pin 4.
6	GND	Same as pin 3.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin. This pin is internally DC blocked. The output impedance is 50Ω.	

Application Schematic



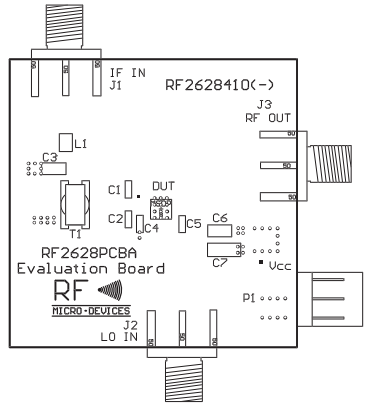
Evaluation Board Schematic

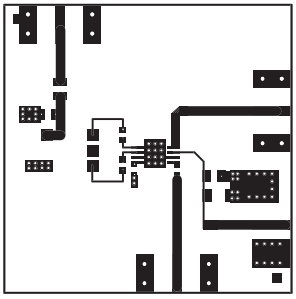
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.500" x 1.500"

Board Thickness 0.031”, Board Material FR-4





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RF2638

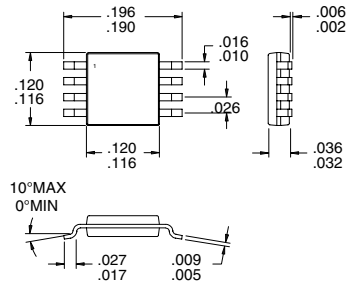
CDMA UPCONVERTER/BPSK MODULATOR

Typical Applications

- PCS/Cellular CDMA Systems
- PHS 1500/ WLAN 2400 Systems
- General Purpose Upconverter
- BPSK Modulation
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

The RF2638 is a complete upconverter designed for cellular and PCS applications. This device may also be used to directly BPSK modulate a carrier. The unit operates at 3.0V and is designed as part of the RFMD PCS/Cellular CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.



6

MIXERS

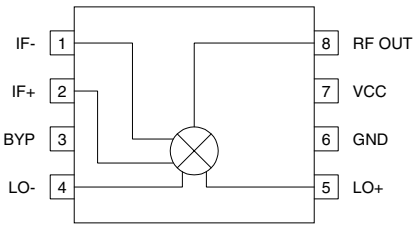
Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8

Features

- Supports Dual Mode Operation
- +13dBm Output IP3 (830MHz)
- Single 3.0V Power Supply
- Miniature 8 Pin Package
- Double-Balanced Mixer



Functional Block Diagram

Ordering Information

RF2638	CDMA Upconverter/BPSK Modulator
RF2638 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2638

Absolute Maximum Ratings

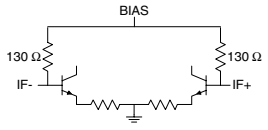
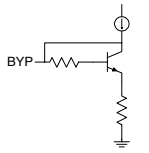
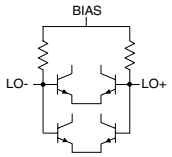
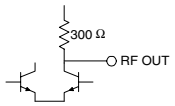
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

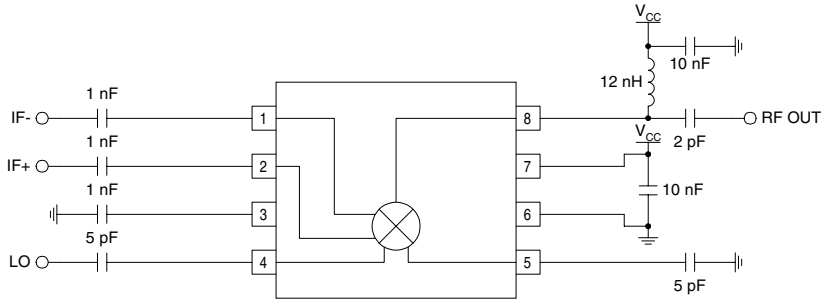
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, LO=1960MHz@-3dBm
RF Output Frequency Range		500 to 2500		MHz	
Conversion Gain		0		dB	RF out=830MHz
	-3.5	-1.5		dB	RF out=1830MHz
Noise Figure		14		dB	RF out=830MHz
		14		dB	RF out=1830MHz
Output IP3		+13		dBm	P_{IN}=-13dBm per Tone, RF out=830MHz
	+7	+11		dBm	P_{IN}=-13dBm per Tone, RF out=1830MHz
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency		DC to 300		MHz	
Differential Input Impedance	220	260	300	Ω	
IF to RF Output Isolation		30		dB	
IF to LO Isolation		30		dB	
LO Input					
LO Frequency Range		300 to 2700		MHz	
LO Level		-6 to 0		dBm	
LO to RF Output Leakage	-18	-25		dBm	
RF to LO Isolation		30		dB	
LO Input VSWR		2:1			50Ω
Power Supply					
Voltage	2.7	3.0	3.3	V	
Current Consumption		25		mA	

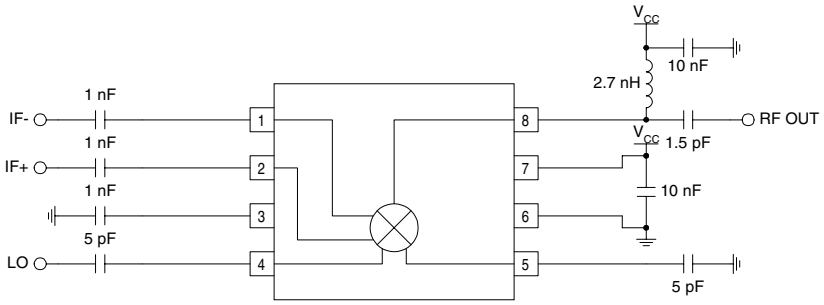
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Pin	Function	Description	Interface Schematic
1	IF-	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 260Ω.	
2	IF+	Same as pin 1, except complementary input.	See Pin 1.
3	BYP	Bypass pin for internal bias circuitry. Bypass with a 1nF capacitor.	
4	LO-	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 50Ω.	
5	LO+	Same as pin 4, except complementary input.	See Pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin.	

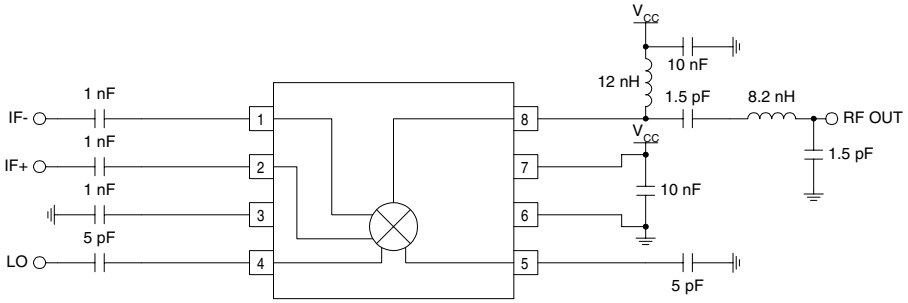
830MHz Application Schematic



1830MHz Application Schematic

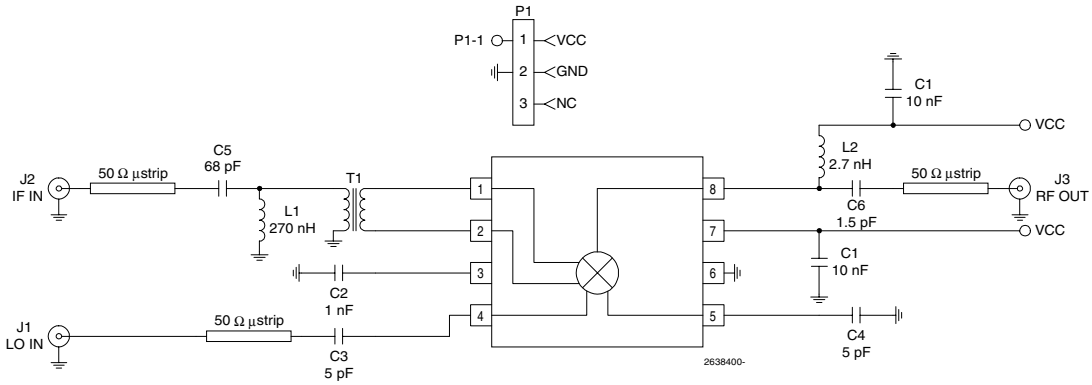


Dual-Band (830MHz to 1830MHz) Application Schematic



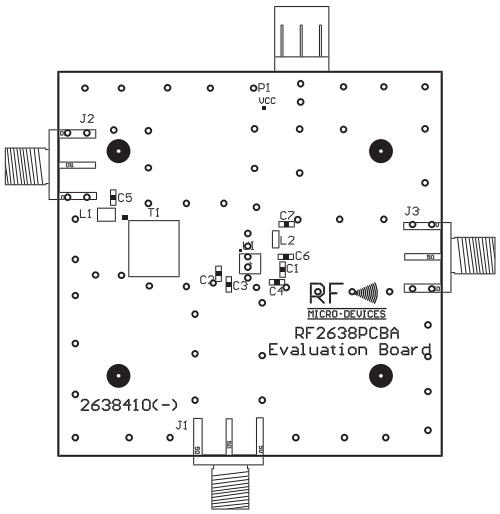
Evaluation Board Schematic

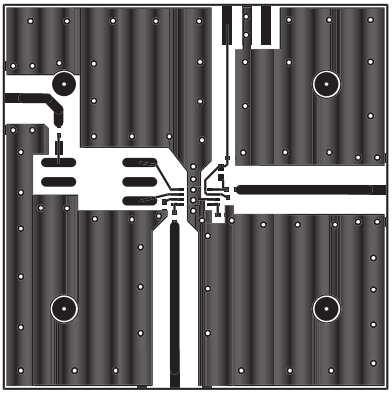
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4





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RF2639

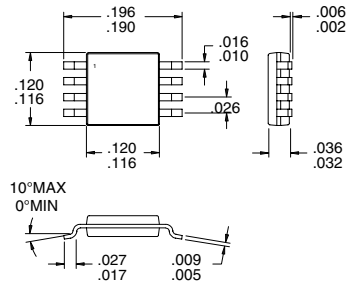
UPCONVERTER/BPSK MODULATOR

Typical Applications

- PCS/Cellular Systems
- PHS 1500/ WLAN 2400 Systems
- General Purpose Upconverter
- BPSK Modulation
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

The RF2639 is a complete upconverter designed for cellular and PCS applications. This device may also be used to directly BPSK modulate a carrier. The unit operates at 3.0V and is designed as part of the RFMD PCS/Cellular CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.



6

MIXERS

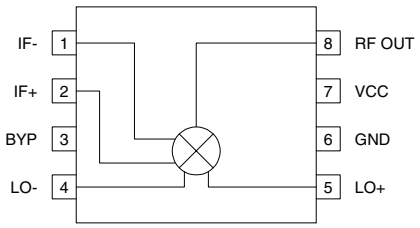
Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8

Features

- Supports Dual Mode Operation
- +2dBm Output Intercept Point
- Single 3.0V Power Supply
- Miniature 8 Pin Package
- Double-Balanced Mixer



Functional Block Diagram

Ordering Information

RF2639	Upconverter/BPSK Modulator
RF2639 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2639

Absolute Maximum Ratings

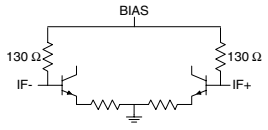
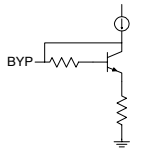
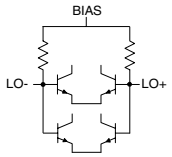
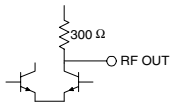
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

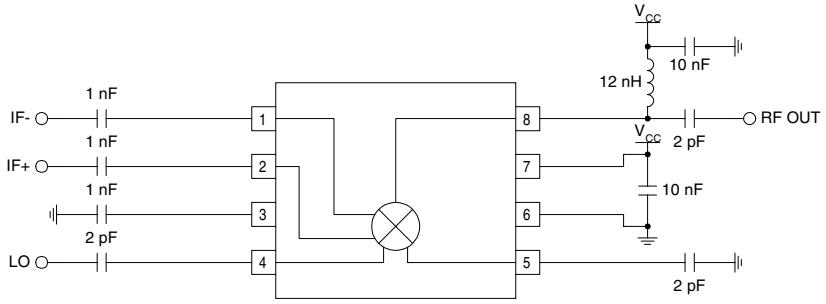
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V
RF Output Frequency Range		500 to 2500		MHz	
Conversion Gain		-1.0		dB	RF out=830MHz
		-3.0		dB	RF out=1830MHz
Noise Figure		11		dB	RF out=830MHz
		11		dB	RF out=1830MHz
Output IP3		+1		dBm	P_{IN}=-23dBm per Tone, RF out=830MHz
		-1		dBm	P_{IN}=-23dBm per Tone, RF out=1830MHz
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency		DC to 300		MHz	
Differential Input Impedance		260		Ω	
IF to RF Output Isolation		30		dB	
IF to LO Isolation		30		dB	
LO Input					
LO Frequency Range		300 to 2700		MHz	
LO Level		-6 to 0		dBm	
LO to RF Output Leakage		-20		dBm	
RF to LO Isolation		30		dB	
LO Input VSWR		2:1			50Ω
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		7		mA	

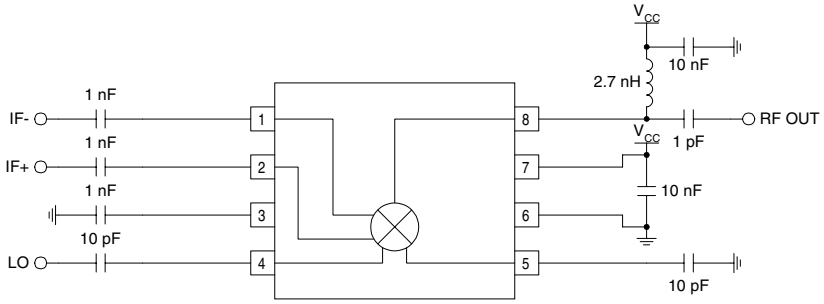
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Pin	Function	Description	Interface Schematic
1	IF-	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 260Ω.	
2	IF+	Same as pin 1, except complementary input.	See Pin 1.
3	BYP	Bypass pin for internal bias circuitry. Bypass with a 1nF capacitor.	
4	LO-	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground.	
5	LO+	Same as pin 4, except complementary input.	See Pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin.	

836 MHz Application Schematic

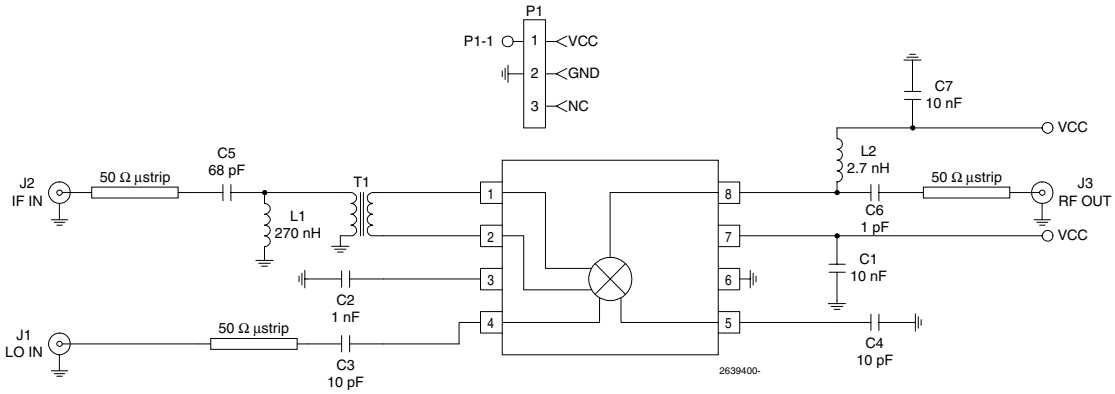


1830 MHz Application Schematic



Evaluation Board Schematic

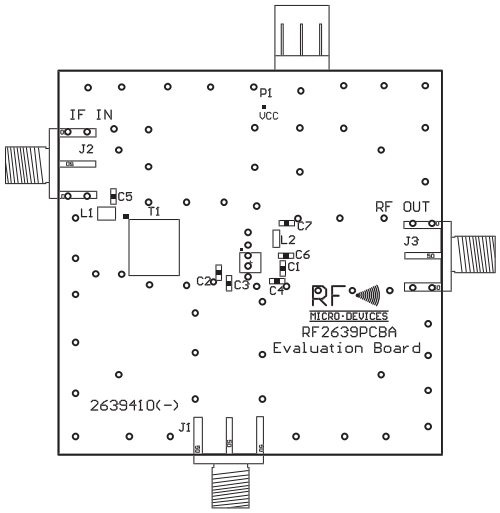
(Download Bill of Materials from www.rfmd.com.)

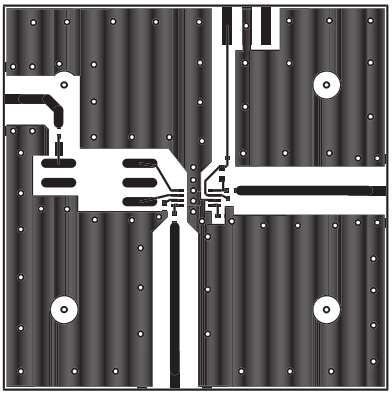


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Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4





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Preliminary

RF2640

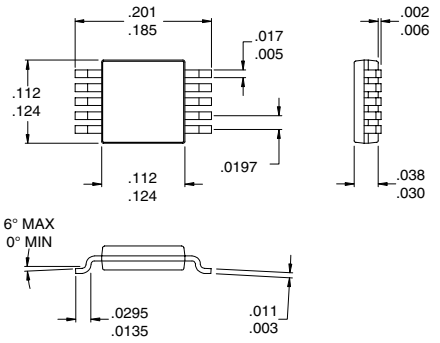
3V 900MHZ UPCONVERTER/ DRIVER AMPLIFIER

Typical Applications

- TDMA/AMPS Cellular Systems
- CDMA/AMPS Cellular Systems
- Portable Battery Powered Equipment

Product Description

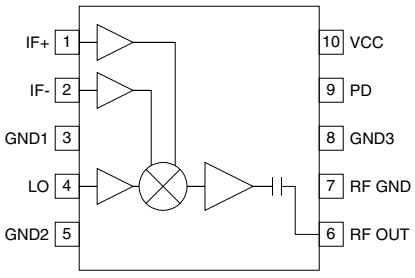
The RF2640 is a complete upconverter and power amplifier driver designed for TDMA and CDMA applications. The device features balanced IF inputs, single-ended LO input and RF output for ease of interface. Packaged in an industry standard MSOP-10 package, the device provides a low-cost solution while easing board space limitations.



Package Style: MSOP-10

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single Supply 3.0V Operation
- +8.5dBm Output P1dB
- +19dBm Output IP3
- Power Down Control
- 23dB Conversion Gain

Ordering Information

RF2640	3V 900MHz Upconverter/ Driver Amplifier
RF2640 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

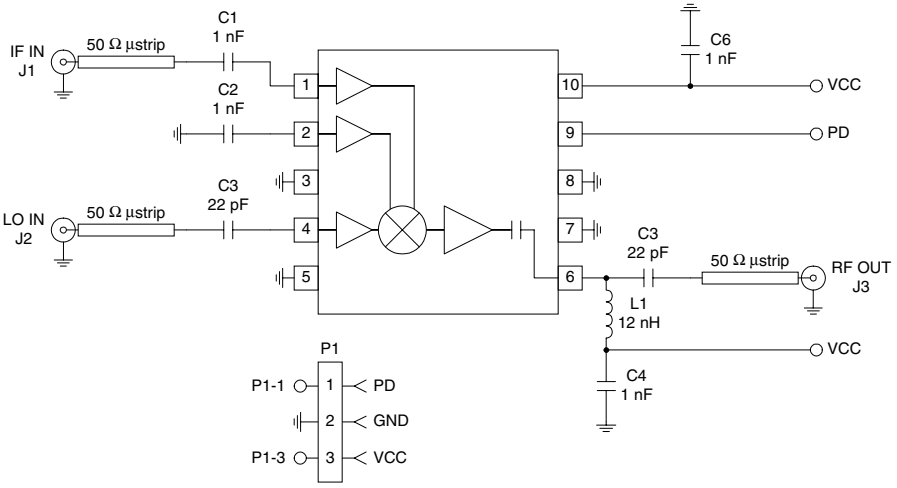
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.7V, RF Out=836MHz, LO=1016MHz @ -8dBm, IF=180MHz @ -30dBm
RF Output Frequency Range		824 to 849		MHz	
Conversion Gain	22	23.5	26	dB	
Noise Figure		12		dB	Single Sideband
Output P1dB		+8.5		dBm	
Output IP3	+17	+18.5		dBm	
Output VSWR		1.25:1			50Ω
IF Input					
IF Frequency		180		MHz	
IF Input Level	-60		-15	dBm	
Single-Ended Input Impedance		70		Ω	
IF to RF Isolation		45		dB	
LO Input					
LO Frequency Range		1004 to 1029		MHz	
LO Level	-10	-8	-6	dBm	
LO to RF Output Leakage			-18	dBm	IF Input<-24dBm
LO Input VSWR		1.25:1			50Ω
Power Supply					
Voltage	2.7		3.3	V	
Current Consumption		45	65	mA	Device is active (ON); V_{PD}=1.8V
			10	µA	Device is inactive (OFF); V_{PD}=0.6V
Power Down Voltage	0.0		0.6	V	Device is inactive (OFF); V_{PD}=0.6V
	1.2		1.8	V	Device is active (ON); V_{PD}=1.8V
Power Down Current			0.1	mA	Device is active (ON); V_{PD}=1.8V

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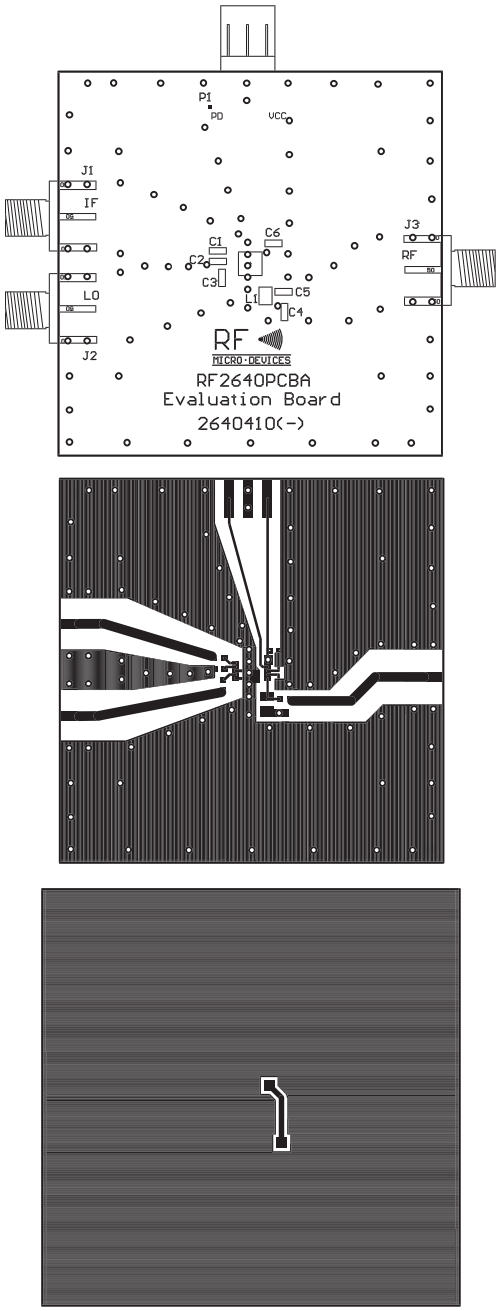
Pin	Function	Description	Interface Schematic
1	IF+	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The single-ended input impedance is 50Ω.	
2	IF-	Same as pin 1, except complementary input.	
3	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LO+	Single-ended LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. The single-ended input impedance is 50Ω.	
5	GND2	Same as pin 3, except complementary input.	
6	RF OUT	RF Output Pin. This pin is internally DC blocked. The output impedance is 50Ω.	
7	RF GND	This pin requires a small inductance to ground to optimize the gain and third order intercept point. See Evaluation Board Layout. The trace length on the board is approximately 65 mils.	
8	GND3	Same as pin 7.	
9	PD	Power Down Control. When logic “high” (between 1.2V and 1.8V) the device is active and all circuits are operating. When logic “low” (between 0.0V and 0.6V) the device is inactive and all circuits are turned off.	
10	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.0” x 2.0”



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RF2641

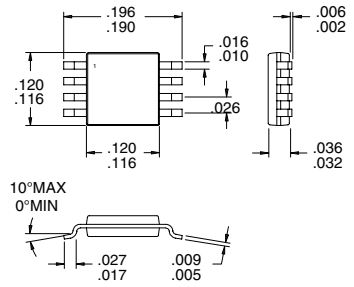
CDMA UPCONVERTER/BPSK MODULATOR

Typical Applications

- PCS/Cellular CDMA Systems
- PHS 1500/ WLAN 2400 Systems
- General Purpose Upconverter
- BPSK Modulation
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

The RF2641 is a complete upconverter designed for cellular and PCS applications. This device may also be used to directly BPSK modulate a carrier. The unit operates at 3.0V and is designed as part of the RFMD PCS/Cellular CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.



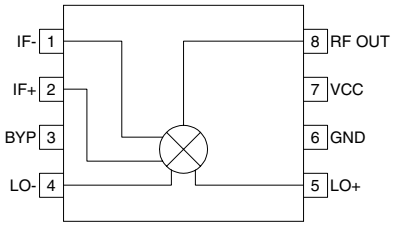
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8

Features

- Supports Dual Mode Operation
- +5.5dBm Output Intercept Point
- 7dB Conversion Gain (836MHz)
- Single 3.0V Power Supply
- Miniature 8 Pin Package
- Double-Balanced Mixer



Functional Block Diagram

Ordering Information

RF2641	CDMA Upconverter/BPSK Modulator
RF2641 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2641

Absolute Maximum Ratings

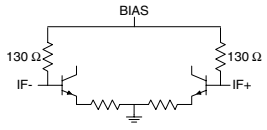
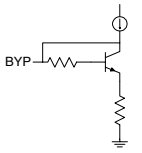
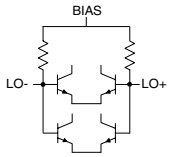
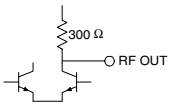
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

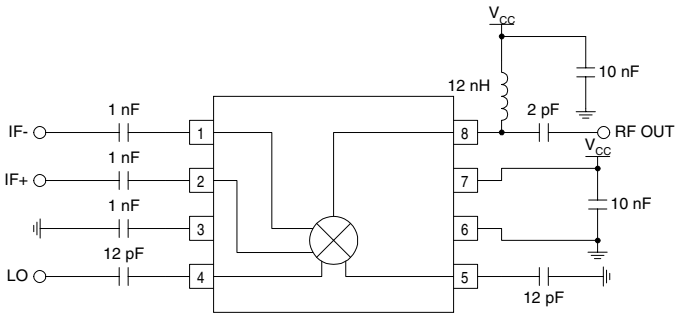
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, IF=130MHz
RF Output Frequency Range		500 to 2500		MHz	
Conversion Gain	5	7		dB	RF out=836MHz, LO=-3dBm@960MHz
		4		dB	RF out=1830MHz, LO=-3dBm@2010MHz
Noise Figure		10		dB	RF out=836MHz
		13		dB	RF out=1830MHz
Output IP3	+4	+5.5		dBm	P_{IN}=-18dBm per Tone, RF out=836MHz
		+4			P_{IN}=-18dBm per Tone, RF out=1830MHz
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency		DC to 300		MHz	
Differential Input Impedance		260		Ω	
IF to RF Output Isolation		30		dB	
IF to LO Isolation		30		dB	
LO Input					
LO Frequency Range		300 to 2700		MHz	
LO Level		-6 to 0		dBm	
LO to RF Output Leakage	-15	-20		dBm	
RF to LO Isolation		30		dB	
LO Input VSWR		2:1			50Ω
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		13	16	mA	

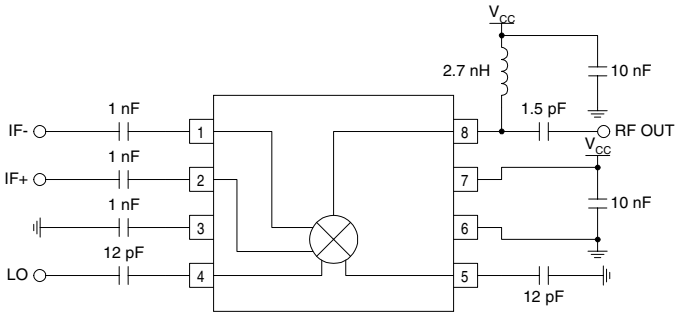
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Pin	Function	Description	Interface Schematic
1	IF-	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 260Ω.	
2	IF+	Same as pin 1, except complementary input.	See Pin 1.
3	BYP	Bypass pin for internal bias circuitry. Bypass with a 1nF capacitor.	
4	LO-	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 50Ω.	
5	LO+	Same as pin 4, except complementary input.	See Pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin.	

Application Schematic 836MHz



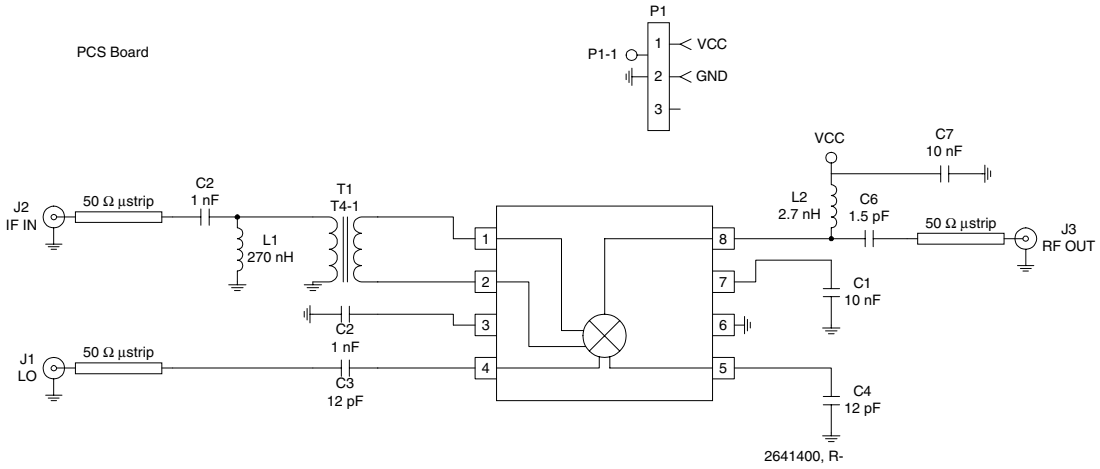
Application Schematic 1880MHz



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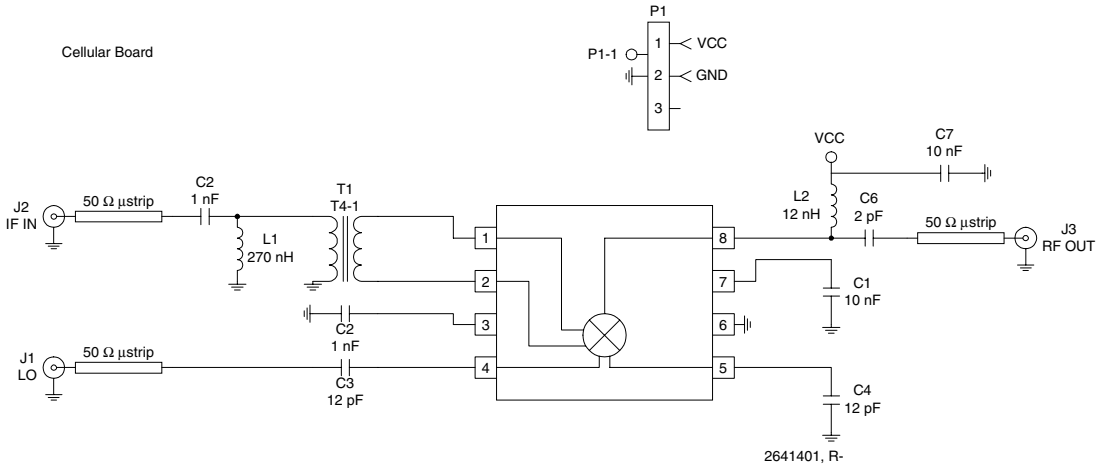
Evaluation Board Schematic
PCS Board

(Download Bill of Materials from www.rfmd.com.)



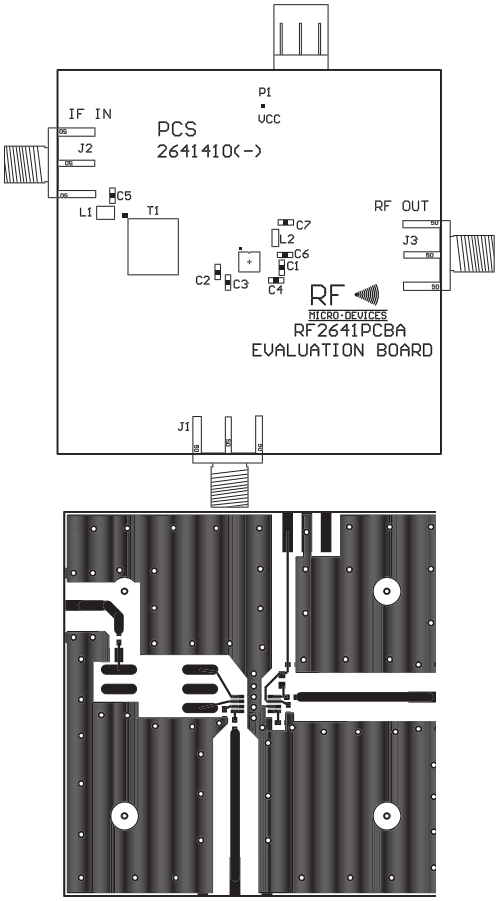
Evaluation Board Schematic
Cellular Board

(Download Bill of Materials from www.rfmd.com.)

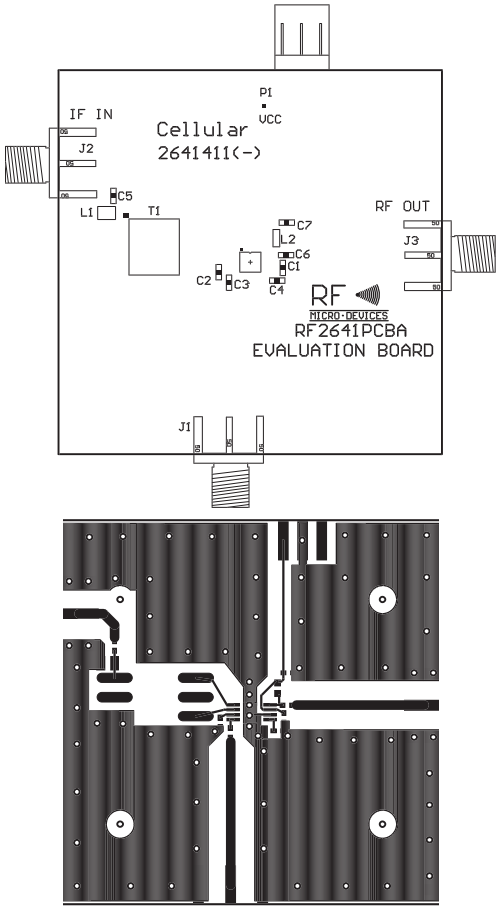


Evaluation Board Layout

Board Thickness 0.014”; Board Material FR-4



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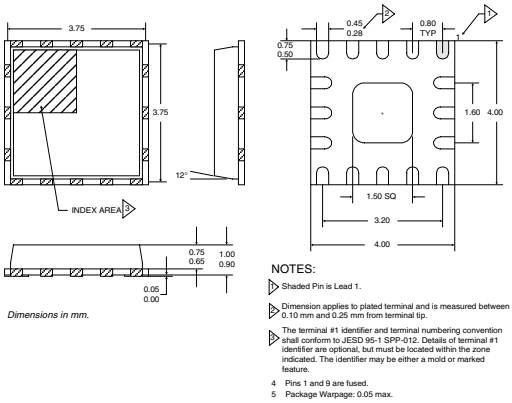
3V 900MHZ UPCONVERTER/ DRIVER AMPLIFIER WITH BYPASS MODE

Typical Applications

- CDMA/AMPS Cellular Systems
- TDMA/AMPS Cellular Systems
- General Purpose Upconverter/Driver
- Portable Battery Powered Equipment

Product Description

The RF2642 is a complete upconverter and power amplifier driver designed for CDMA applications. The design features driver amplifier high and low gain states. In the low gain state, the gain is adjustable and the device draws less current. The upconverter is always on. The power down mode turns off the driver amplifier. The device features balanced IF inputs, single-ended LO input and RF output for ease of interface. Packaged in an industry standard MLF16 package, the device provides a low-cost solution while easing board space limitations.



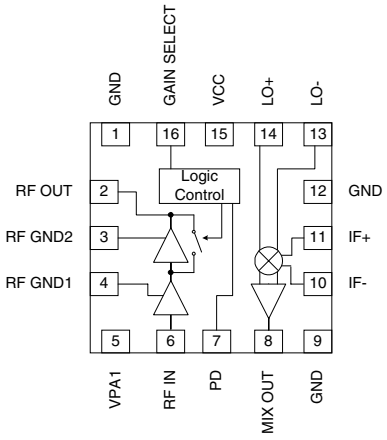
Dimensions in mm.

NOTES:
1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MLF16



Functional Block Diagram

Features

- Single Supply 3.0V Operation
- Step Gain Control
- Power Down Control
- ACPR1=61dBc @ 885kHz with P_{OUT}=+5dBm
- Small Leadless MLF16 Package

Ordering Information

RF2642	3V 900MHz Upconverter/ Driver Amplifier with Bypass Mode
RF2642 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +4.5	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-30 to +150	°C

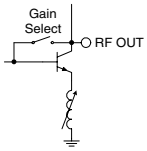
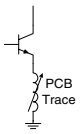
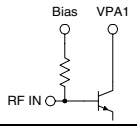
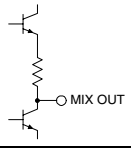
Caution! ESD sensitive device.

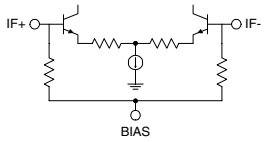
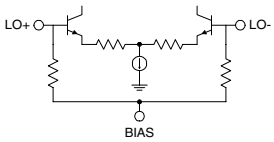
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF_{OUT}=830MHz, LO=960MHz @ -3dBm, IF=130MHz
RF Output Frequency Range		824 to 849		MHz	
IF Frequency Range		130		MHz	
Output Power	+5			dBm	CW
High Gain Mode					GAIN SELECT=2.7V, V_{PD}=2.7V
Gain	33	34.5	36	dB	
Noise Figure		12	14	dB	
IF Input Impedance		250		Ω	Differential @ 130MHz
RF Output VSWR		1.5	2:1		824MHz to 849MHz, external components required
Current Consumption		52		mA	
Adjacent Channel Power Rejection (ACPR1)	55	61		dBc	P_{OUT}=+5dBm, 885kHz offset
Alternate Channel Power Rejection (ACPR2)	65	78	80	dBc	P_{OUT}=+5dBm, 1.98MHz offset
Bypass Mode					GAIN SELECT=0V, V_{PD}=2.7V
Gain		11.9		dB	
Noise Figure		11.9	14	dB	
IF Input Impedance		250		Ω	Differential @ 130MHz
RF Output VSWR		1.5	2:1		824MHz to 849MHz, external components required
Output IP3	-4	+5.4		dBm	
Current Consumption		26		mA	
LO Input					954MHz to 979MHz
LO Frequency Range		954 to 979		MHz	
LO Level	-6	-3	0	dBm	
LO Input Impedance		50		Ω	
LO to Mixer RF Output Leakage	-20	-33		dBm	
LO Input VSWR		1.4	2:1		GAIN SELECT=0V
		1.7	2:1		GAIN SELECT=2.7V
Power Supply					
Voltage	2.7	3.0	3.3	V	
Current Consumption			15	mA	V_{PD}=0V

NOTE: The measured results do not include the losses from the IF balun and SAW filter. On the evaluation board, those losses are as follows: IF Balun=1dB, SAW Filter=2.5dB to 3.5dB.

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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane. This pin is internally connected to the die flag.	
2	RF OUT	Output match of the second stage of the power amplifier driver. This amplifier output pin is open collector. It is matched to 50Ω externally using a simple LC match. Refer to the application schematic.	
3	RF GND2	The ground connection for the second stage of the power amplifier driver. The inductance between this pin and the ground plane determines the gain of the second stage. Increased inductance results in reduced gain. On the evaluation board, the emitter ground inductance is set by the length of the PCB trace connected between this pin and the ground. By sliding a 0Ω ground jumper along this line, the inductance, and hence the gain, may be varied. The evaluation board is shipped with the 0Ω jumper very close to the part, resulting in minimum inductance, and therefore maximum second stage gain. This translates to higher output IP3 and maximum ACPR1. This setting results in performance 6dB better than the ACPR1 minimum specification of 50dBc in the CDMA IS-95 specification for a P_{OUT}=+5dBm.	
4	RF GND1	The ground connection for the first stage of the power amplifier driver. The inductance between this pin and the ground plane determines the gain of the first stage. Increased inductance results in reduced gain. On the evaluation board, the emitter ground inductance is set by the length of the PCB trace connected between this pin and the ground. By sliding a 0Ω ground jumper along this line, the inductance, and hence the gain, may be varied. The evaluation board is shipped with the 0Ω jumper far away from the part, resulting in maximum inductance, and therefore minimum first stage gain. More gain may be obtained by shifting the 0Ω jumper toward the part. A maximum total gain of 40dB may be achieved if the first stage is set to minimum emitter inductor trace length.	See pin 3.
5	VPA1	Power supply pin for the first stage power amplifier. External components provide tuning for the interstage match.	
6	RF IN	RF input to the power amplifier. This input is DC coupled, so an external blocking capacitor is needed if the pin is connected to a DC path.	
7	PD	Power Down control When this pin is low, the amplifier section of the IC is shut off. When this pin is high, the amplifier section of the IC is turned on. The upconverter portion of the IC remains on regardless of the state of PD.	
8	MIX OUT	Output for the upconverting mixer. This input is DC coupled, so an external blocking capacitor is needed if the pin is connected to a DC path. The output impedance is 50Ω.	
9	GND	Same as pin 1.	

Pin	Function	Description	Interface Schematic
10	IF-	Balanced IF Input Pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The input impedance is 250Ω in both the balanced and single-ended modes.	
11	IF+	Same as pin 10, except complementary input.	
12	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
13	LO-	Balanced LO Input Pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The input impedance is 50Ω in both the balanced and single-ended modes.	
14	LO+	Same as pin 13, except complementary input.	
15	VCC	Supply voltage for all bias circuits and logic circuits.	
16	GAIN SELECT	When GAIN SELECT is high: the driver amplifier is switched to high gain mode; both amplifier stages are active; the gain is maximized; and, the entire device draws approximately 51mA. When GAIN SELECT is low, the second stage of the PA driver is turned off and bypassed. This results in a device current of 26mA, which is approximately a 50% current reduction. The upconverting mixer remains on in both the high and low gain modes to prevent VCO pulling.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

PD	Gain Select	Mixer	Amplifier First Stage	Amplifier Second Stage	Gain (dB)*
0	0	ON	OFF	OFF	
0	1	ON	OFF	OFF	
1	0	ON	ACTIVE	BYPASSED	11.9
1	1	ON	ACTIVE	ACTIVE	34.5

*See parameter specifications for conditions.

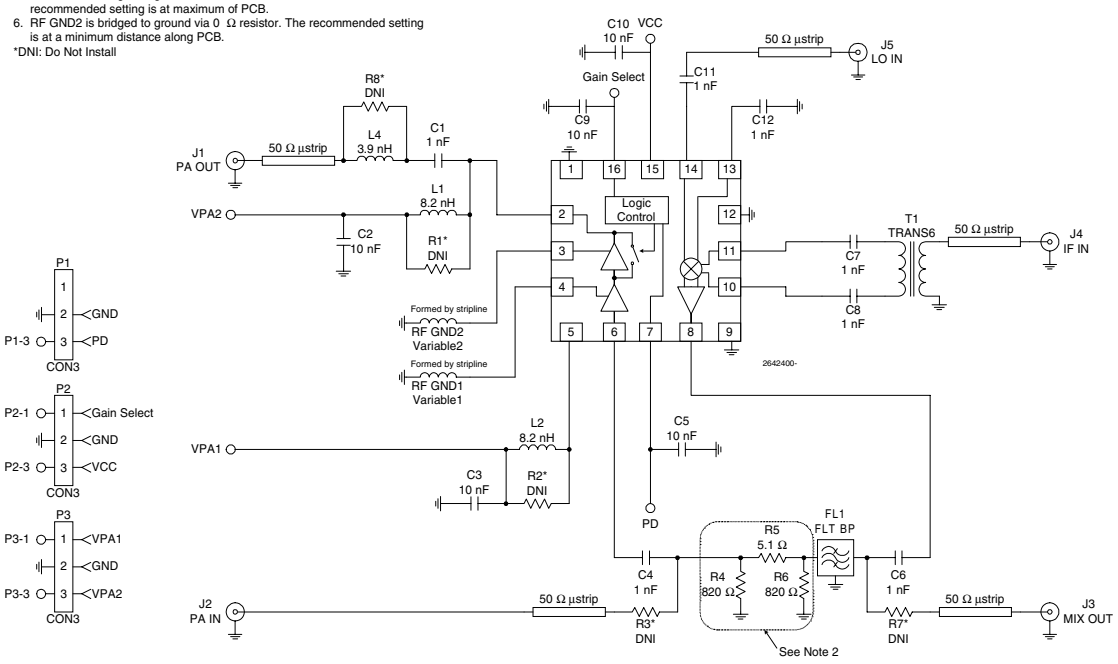
Db00.bk Page 53 Thursday, January 6, 2000 6:50 PM

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

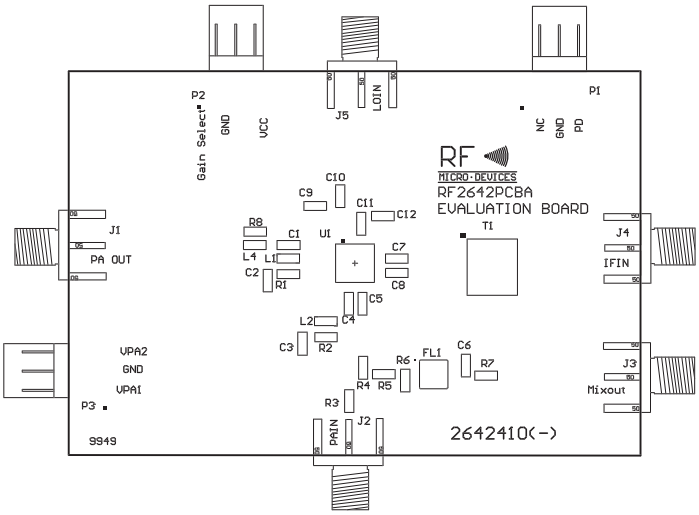
NOTE:
1. R1, R2 and R8 are optional.
2. R4, R5 and R6 form T-attenuator with a loss of 1 dB. For 0 dB loss, R4 and R6 are removed, and R5 is a 0 Ω short.
3. R3 and R7 are normally open.
4. FLT BP recommended is a Murata filter: SAFC836.5MC90T-TC12.
5. RF GND1 is bridged to ground via 0 Ω 0402 size resistor. The recommended setting is at maximum of PCB.
6. RF GND2 is bridged to ground via 0 Ω resistor. The recommended setting is at a minimum distance along PCB.

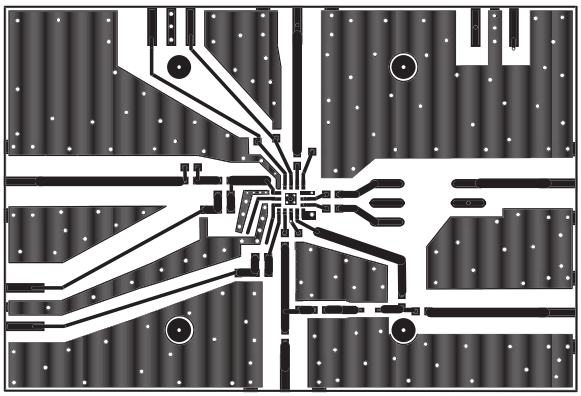
*DNI: Do Not Install

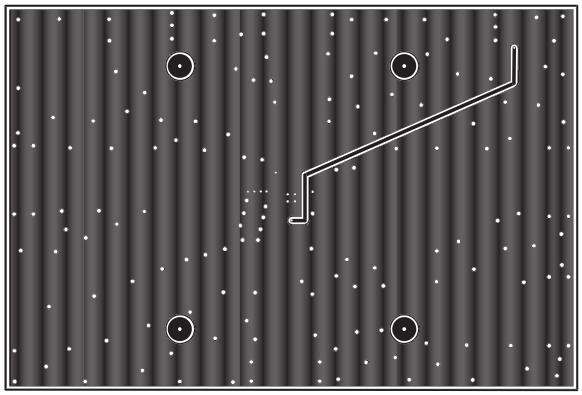


Evaluation Board Layout
Board Size 2.981" x 2.981"

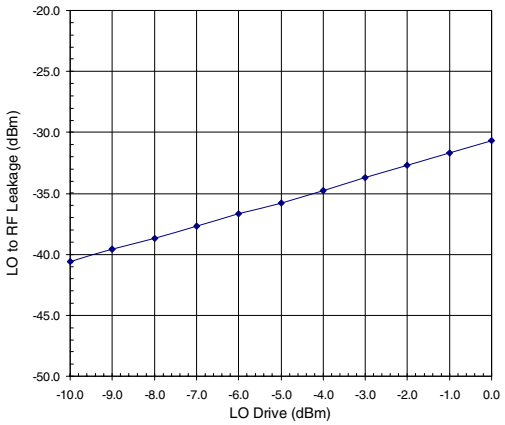
Board Thickness 0.031", Board Material FR-4



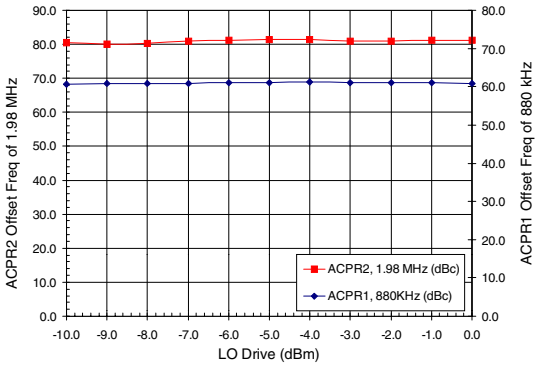




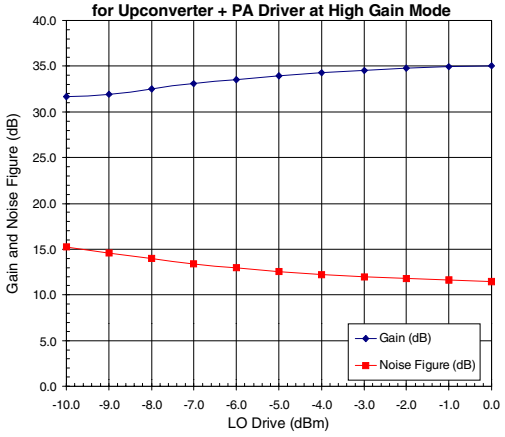
LO to RF Leakage for Upconverter Mixer Alone



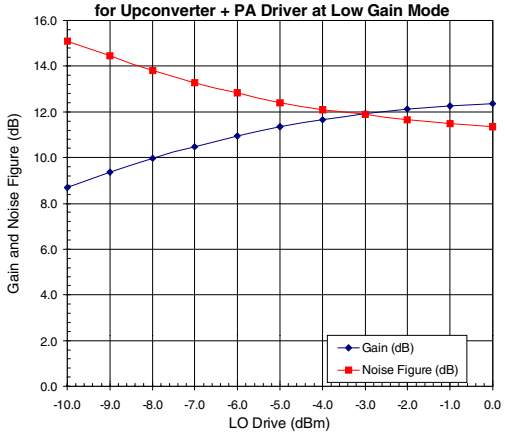
ACPR1 and ACPR2 versus LO Drive at V_{CC}=3.0V for Upconverter + PA Driver at High Gain Mode



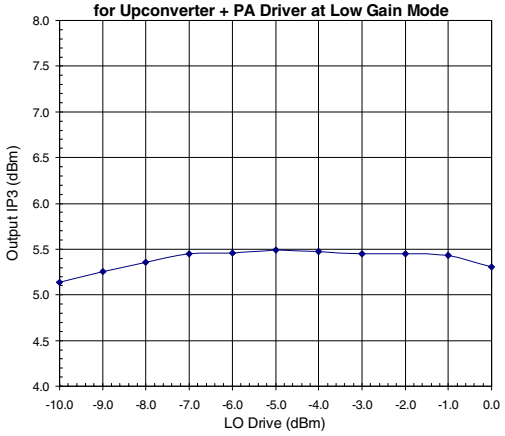
Gain and Noise Figure versus LO Drive at V_{CC}=3.0V for Upconverter + PA Driver at High Gain Mode



Gain and Noise Figure versus LO Drive at V_{CC}=3.0V for Upconverter + PA Driver at Low Gain Mode



Output IP3 versus Drive Level at V_{CC}=3.0V for Upconverter + PA Driver at Low Gain Mode



6 MIXERS

RF9908

CDMA/FM UPCONVERTER/BPSK MODULATOR

Typical Applications

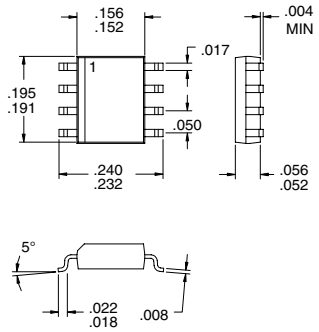
- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- Commercial and Consumer Systems
- 3-Cell Battery Operated Systems

Product Description

The RF9908 is a complete upconverter designed for CDMA/FM cellular applications. The IC contains a double-balanced mixer stage and an output buffer amplifier stage. This device may also be used to directly BPSK modulate a carrier. The mixer is a Gilbert cell with emitter degeneration resistors to provide high IP_3. The output stage is a class-B, push-pull configuration to reduce the overall current and still provide a good 50Ω output match. The unit operates at 3.6V and does not require any external matching components other than coupling capacitors. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.

Optimum Technology Matching® Applied

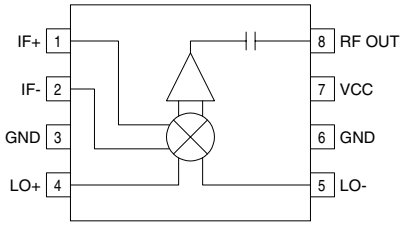
- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Package Style: SOP-8

Features

- Supports Dual Mode Operation
- +8dBm Input/Output Intercept Point
- Single 3.6V Power Supply
- Internally Matched Inputs and Outputs
- Buffered Output
- Double-Balanced Mixer



Functional Block Diagram

Ordering Information

RF9908	CDMA/FM Upconverter/BPSK Modulator
RF9908 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF9908

Absolute Maximum Ratings

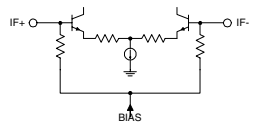
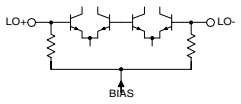
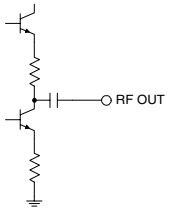
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input RF Power	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

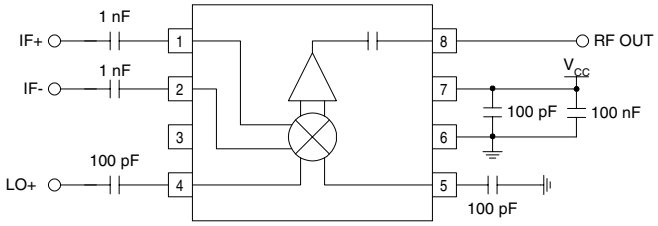
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=840MHz, LO=970MHz, IF=130MHz
RF Output Frequency Range		500 to 1500		MHz	
Conversion Gain		0		dB	Over temperature and frequency
Noise Figure		14		dB	
Output IP3		+8		dBm	
Output ACP		-54		dB	Referenced to a 1.23MHz in-band power. (±885kHz offset)
Output ALT		-75		dB	Referenced to a 1.23MHz in-band power. (±1.98MHz offset)
Output VSWR		1.5:1			50Ω
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency		DC to 200		MHz	
Differential Input Impedance		265		Ω	
IF to RF Output Isolation		30		dB	
IF to LO Isolation		30		dB	
LO Input					
LO Frequency Range		300 to 1700		MHz	
LO Level		-6 to 0		dBm	
LO to RF Output Leakage		-30	-20	dBm	
RF to LO Isolation		30		dB	
LO Input VSWR		2:1			50Ω
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		18		mA	

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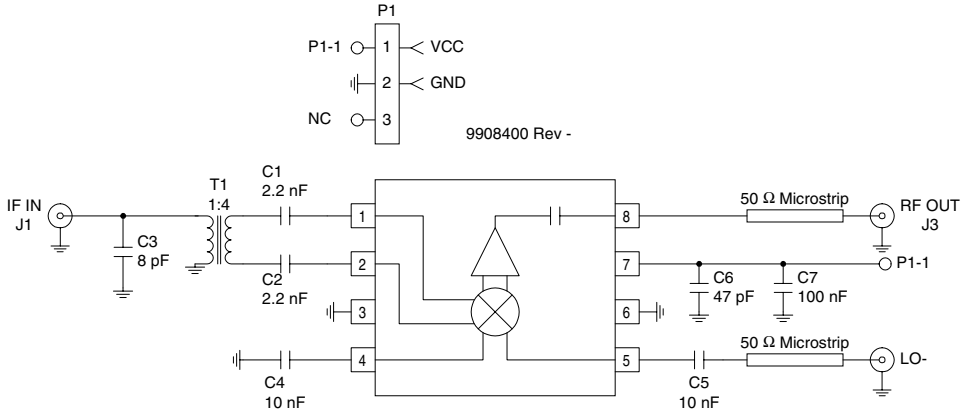
Pin	Function	Description	Interface Schematic
1	IF+	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 265Ω.	
2	IF-	Same as pin 1, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LO+	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced, as well single-ended, input impedance is 50Ω.	
5	LO-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Same as pin 3.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin. This pin is internally DC blocked. The output impedance is 50Ω.	

Application Schematic



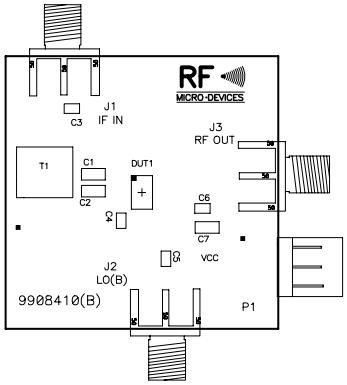
Evaluation Board Schematic

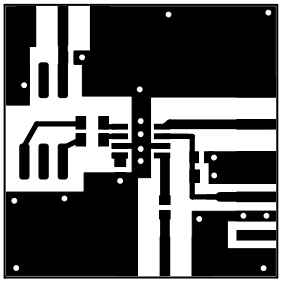
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.4” x 1.4”

Board Thickness 0.031”, Board Material FR-4





RF9938

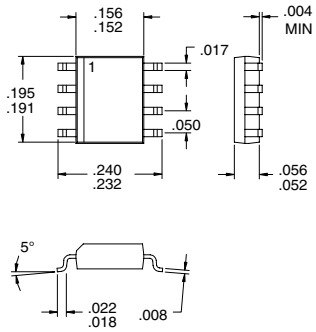
PCS UPCONVERTER/BPSK MODULATOR

Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/ WLAN 2400 Systems
- General Purpose Upconverter
- BPSK Modulation
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

The RF9938 is a complete upconverter designed for PCS applications. The IC contains a double-balanced mixer stage and an output buffer amplifier stage. This device may also be used to directly BPSK modulate a carrier. The mixer is a Gilbert cell with emitter degeneration resistors to provide high IP_3. The output stage is a class-B, push-pull configuration to reduce the overall current and still provide a good 50Ω output match. The unit operates at 3.6V and is designed as part of the RFMD PCS CDMA Chip Set, consisting of a Transmit IF AGC Amp, this Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp.



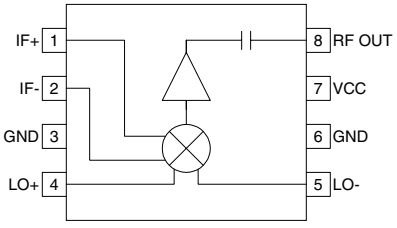
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- Supports Dual Mode Operation
- +8dBm Output Intercept Point
- Single 3.6V Power Supply
- Internally Matched Inputs and Outputs
- Buffered Output
- Double-Balanced Mixer



Functional Block Diagram

Ordering Information

RF9938	PCS Upconverter/BPSK Modulator
RF9938 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF9938

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Input RF Power	+6	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

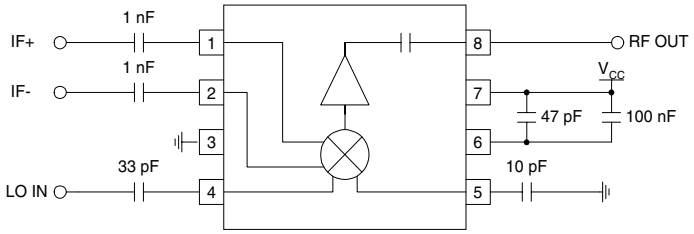
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF out=1880MHz, LO=1750MHz @ -3dBm, IF=130MHz @ -10dBm in
RF Output Frequency Range		1200 to 2500		MHz	
Conversion Gain	-3.8	-2.8	-1.0	dB	
Noise Figure		14		dB	
Output IP3	+5	+8		dBm	P_{IN}=-13dBm per Tone
Output ACP		-64		dB	Referenced to a 1.23MHz in-band power. At ±1.25MHz Offset (CDMA P_{IN}=-10dBm)
Output VSWR		1.5:1			50Ω
Spurious Product Rejection		30		dBc	Referenced to RF output
IF Input					
IF Frequency		DC to 200		MHz	
Differential Input Impedance		265		Ω	
IF to RF Output Isolation		30		dB	
IF to LO Isolation		30		dB	
LO Input					
LO Frequency Range		1000 to 2700		MHz	
LO Level		-6 to 0		dBm	
LO to RF Output Leakage		-30	-20	dBm	
RF to LO Isolation		30		dB	
LO Input VSWR		2:1			50Ω
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		27	33	mA	

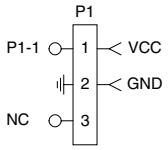
Pin	Function	Description	Interface Schematic
1	IF+	Balanced IF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 265Ω.	
2	IF-	Same as pin 1, except complementary input.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LO+	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced, as well as single-ended, input impedance is 50Ω.	
5	LO-	Same as pin 4, except complementary input.	
6	GND	Same as pin 3.	
7	VCC	Supply Voltage pin. External bypassing is required. External RF, LO, and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	RF OUT	RF Output Pin. This pin is internally DC blocked. The output impedance is 50Ω.	

Application Schematic

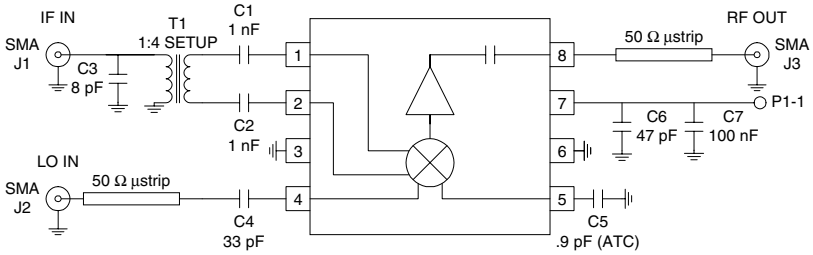


Evaluation Board Schematic

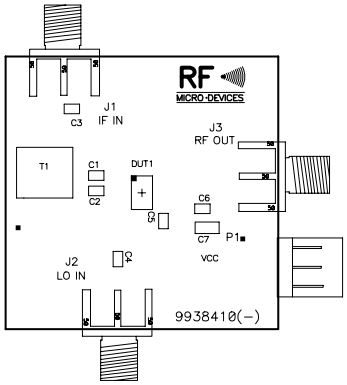
(Download Bill of Materials from www.rfmd.com.)

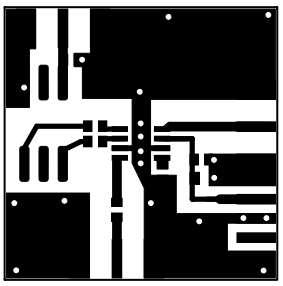


Drawing 9938400 Rev -



Evaluation Board Layout
1.4” x 1.4”





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7 Quadrature Demodulators

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	LO Freq	Amp Phase Bal	Demod Gain (dB)	Package	Page
RF2667	Receive AGC and Demodulator	50 to 300	2.7 to 3.3	20	2xIF	0.1dB, ±1°	-55 to +50	SSOP-24	7-1
RF2711	Quadrature Demodulator	0.1 to 250	4.5 to 5.5	4.5	2xIF	0.1dB, ±1°	14	SOP-14	7-11
RF2713	Quadrature Modulator/Demodulator	0.1 to 250	2.7 to 6	8	2xIF	0.1dB, ±1°	20	SOP-14	7-17
RF9957	CDMA/FM Receive AGC and Demodulator	50 to 250	2.7 to 3.3	14	2xIF	0.1dB, ±1°	-55 to +50	SSOP-24	7-27

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RF2667

RECEIVE AGC AND DEMODULATOR

Typical Applications

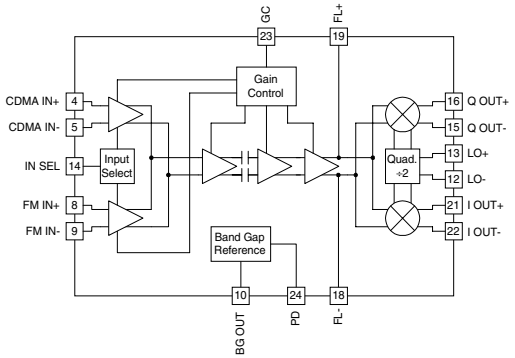
- CDMA/FM Cellular Systems
- CDMA PCS Systems
- GSM/DCS Systems
- TDMA Systems
- Spread Spectrum Cordless Phones
- Wireless Local Loop Systems

Product Description

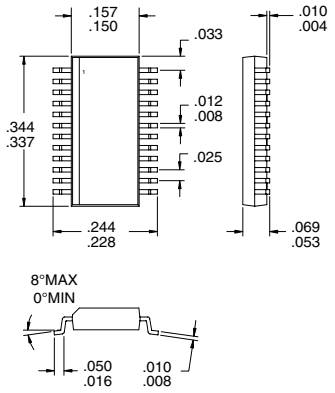
The RF2667 is an integrated complete IF AGC amplifier and Quadrature Demodulator developed for the receive section of dual-mode CDMA/FM cellular and PCS applications and for GSM/DCS and TDMA systems. It is designed to amplify received IF signals, while providing 100dB of gain control range, and demodulate to baseband I and Q signals. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98, and J-STD-018 Interim Standard for CDMA cellular communications. This circuit is part of the RFMD's line of complete solutions for digital radio applications. The IC is manufactured on an advanced 15GHz F_T Silicon Bipolar process, and is packaged in a standard miniature 24-lead plastic SSOP package.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-24

Features

- Similar to RF9957 with increased IF freq. range and higher I/Q output voltage
- Supports Dual Mode Operation
- Digitally Controlled Power Down Mode
- 2.7V to 3.3V Operation
- IF AGC Amp with 100dB Gain Control

Ordering Information

RF2667	Receive AGC and Demodulator
RF2667 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

7 QUADRATURE DEMODULATORS

RF2667

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V_{DC}
Input RF Power	+3	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

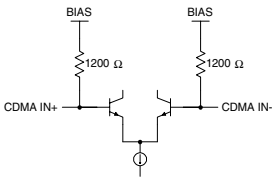
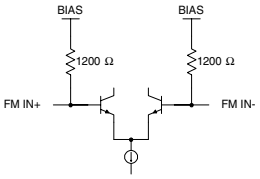
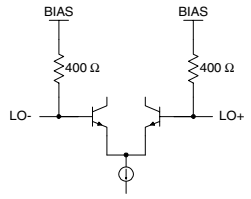
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

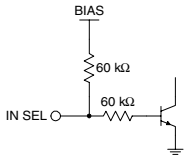
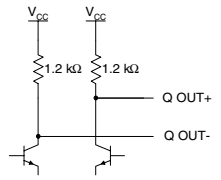
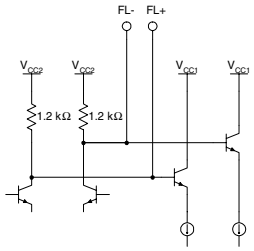
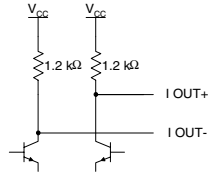
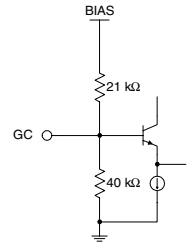
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (Cascaded)					T=25°C, V_{CC}=3.0V, Z_{LOAD}=5kΩ, LO=170MHz @400mV_{PP} IF Freq=85MHz, Z_S=500Ω (CDMA), Z_S=850Ω (FM)
Maximum Gain	+45	+50		dB	V_{GC}=2.5V, FM or CDMA Input, Balanced
Minimum Gain		-55	-50	dB	V_{GC}=0.5V, FM or CDMA Input, Balanced
Gain Variation	-3		+3	dB	T=-20°C to +85°C, Ref = 25°C
Input IP3	-54	-50		dBm	V_{GC}=2.5V, Maximum Gain
	-7	-4		dBm	V_{GC}=0.5V, Minimum Gain
	-39	-36		dBm	Gain = 35 dB, P_{IN}=-61dBm
Noise Figure		5	8	dB	V_{GC}=2.5V, Maximum Gain
		70	77	dB	V_{GC}=0.5V, Minimum Gain
IF Input Frequency Range	50	70 to 230	300	MHz	
IF Input Impedance	2040	2400	2760	Ω	FM or CDMA, Balanced
	1020	1200	1380	Ω	FM or CDMA, Single-ended
I/Q Frequency Range	0		50	MHz	
I/Q Amplitude Balance		0.1	0.5	dB	
I/Q Phase Balance		1	5	deg	
Max I/Q Output Voltage	2.0	2.4		V_{PP}	Balanced, maximum output level
I/Q Output Impedance	1020	1200	1380	Ω	Single-ended
	2040	2400	2760	Ω	Balanced
I/Q DC Output		2.0		V_{DC}	Common Mode
I/Q DC Offset		20		mV_{DC}	I OUT+ to I OUT-; Q OUT+ to Q REF-
LO Input Frequency Range	100	140 to 460	600	MHz	
LO Input Level	60	400	600	mV_{PP}	Balanced
LO Input Impedance	680	800	920	Ω	Balanced
	340	400	460	Ω	Single Ended
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		20	23	mA	CDMA Mode
		20	23	mA	FM Mode
Power Down Current			20	µA	
V_{PD} HIGH Voltage	V_{CC}-0.7			V	
V_{PD} LOW Voltage			0.5	V	

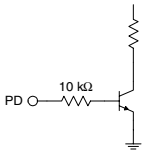
7 QUADRATURE DEMODULATORS

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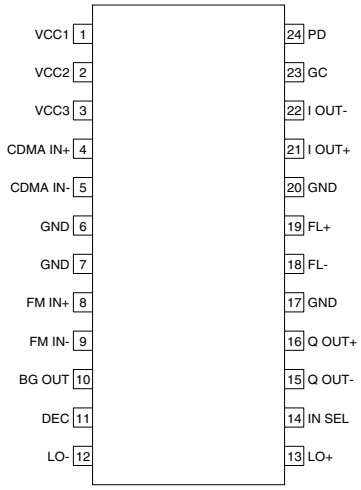
Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LO flip-flop divider and limiting amp. This pin may be connected in parallel with pins 2 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
2	VCC2	Supply voltage for the bandgap, gain control bias circuitry, and AGC stages 2, 3, and 4. This pin may be connected in parallel with pins 1 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
3	VCC3	Supply voltage for the FM and CDMA AGC input stages. This pin may be connected in parallel with pins 1 and 2. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
4	CDMA IN+	CDMA Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
5	CDMA IN-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	GND	Same as pin 6.	
8	FM IN+	FM Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other FM input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
9	FM IN-	Same as pin 8, except complementary input.	See pin 8.
10	BG OUT	Bandgap Voltage Reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
12	LO-	LO Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The frequency of the signal applied to these pins is internally divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 400Ω (balanced is 800Ω). The LO input may be driven single-ended but balanced provides optimum gain and phase balance.	
13	LO+	Same as pin 12, except complementary input.	See pin 12.

RF2667

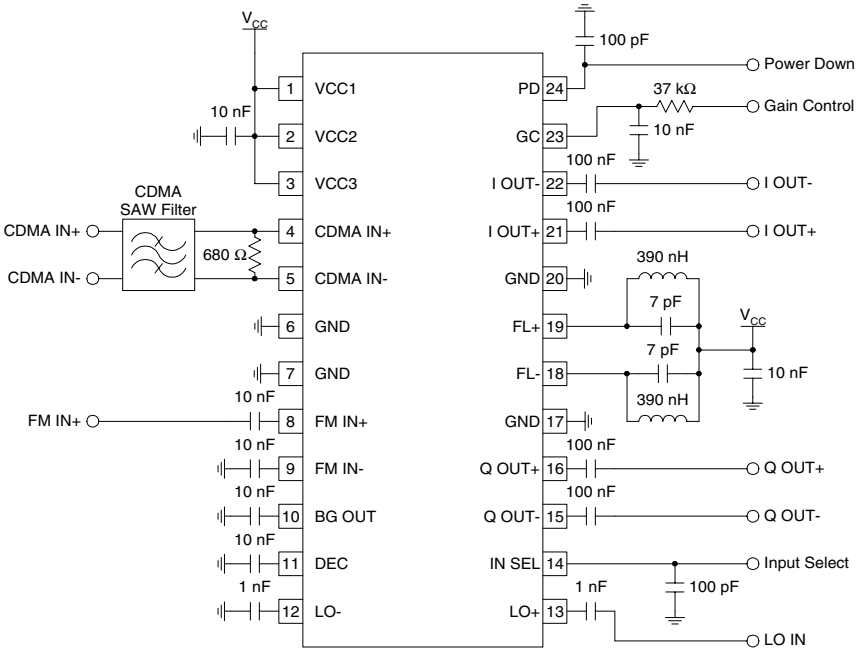
Pin	Function	Description	Interface Schematic
14	IN SEL	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" (≥VCC-0.7V_{DC}) selects CDMA mode. A logic "low" (<0.5V_{DC}) selects FM mode. The impedance on this pin is 30kΩ.	
15	Q OUT-	Balanced Baseband Output of Q Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in both CDMA and FM modes. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5kΩ. The balanced load should be 5kΩ. The single-ended output impedance is 1.2kΩ, while the balanced output impedance is 2.4kΩ.	
16	Q OUT+	Same as pin 15, except complementary output.	See pin 15.
17	GND	Same as pin 6.	
18	FL-	Balanced AGC Output/Demod Input. This balanced node is pinned out to allow shunt filtering of the AGC output signal as it enters the demodulator. The basic configuration of the filter should consist of a shunt inductor and shunt capacitor, both connected to the power supply, as the internal circuitry requires this power supply connection through the inductor to operate.	
19	FL+	Same as pin 18, except complementary.	See pin 18.
20	GND	Same as pin 6.	
21	I OUT+	Balanced Baseband Output of I Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in both CDMA and FM modes. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5kΩ. The balanced load should be 5kΩ. The single-ended output impedance is 1.2kΩ, while the balanced output impedance is 2.4kΩ.	
22	I OUT-	Same as pin 21, except complementary output.	See pin 22.
23	GC	Analog Gain Control for AGC Amplifiers. The valid control range is from 0.5 to 2.5V_{DC}. These voltages are valid for ONLY a 37kΩ source impedance. The gain range for the AGC is 95dB.	

Pin	Function	Description	Interface Schematic
24	PD	Power Down Control. When logic "high" ($\geq V_{CC}$-0.3V), all circuits are operating; when logic "low" ($\leq$0.5V), all circuits are turned off. The input impedance of this pin is 10kΩ.	

RF2667 Pin-Out



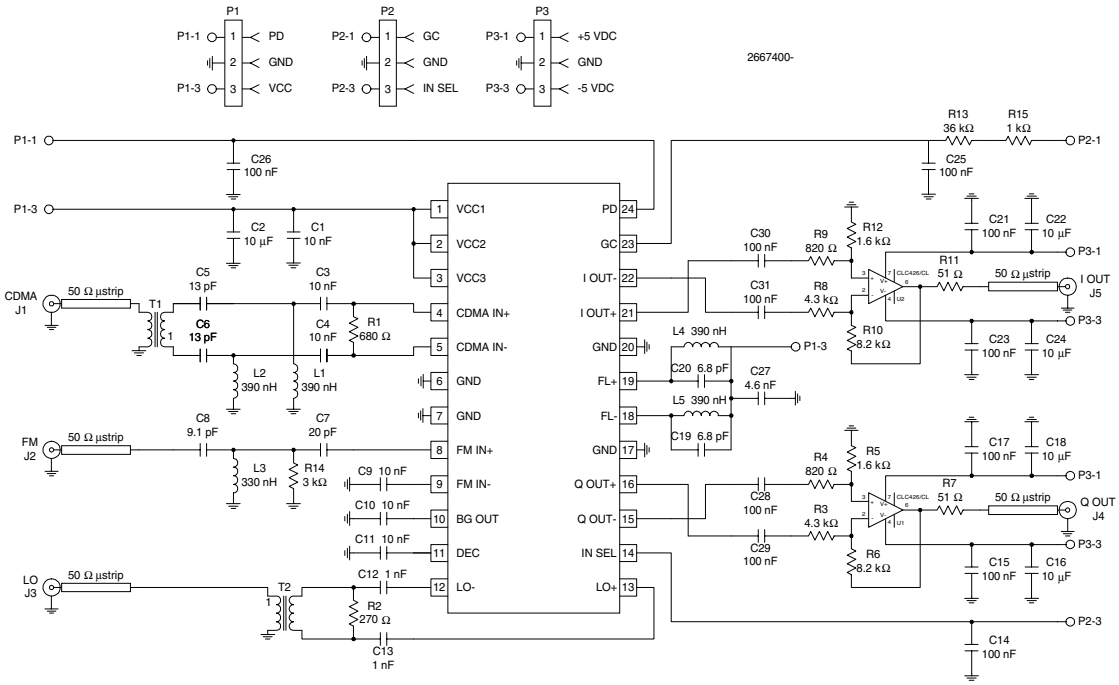
Application Schematic



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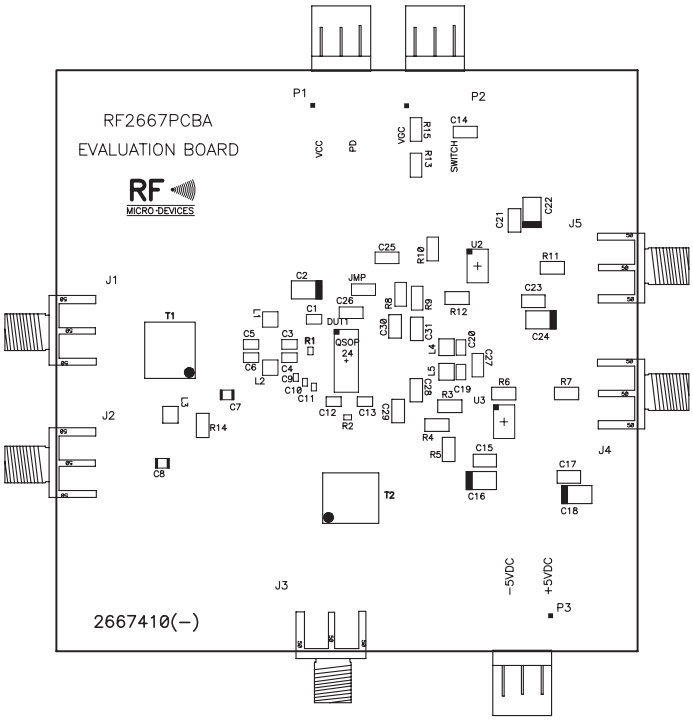
Evaluation Board Schematic
85MHz IF

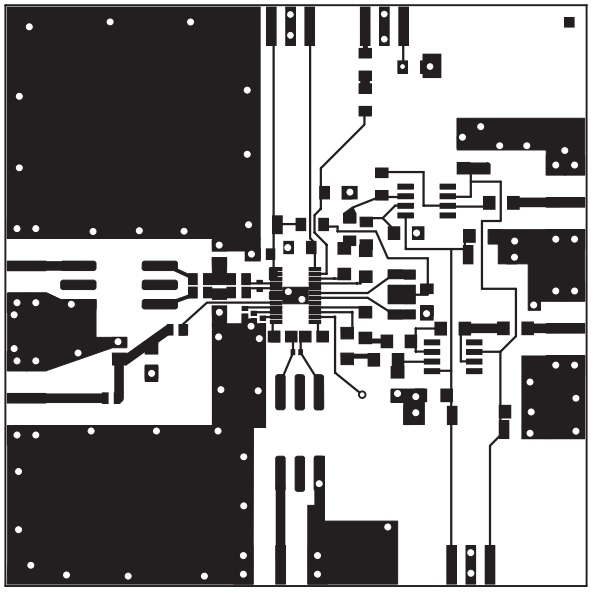
(Download Bill of Materials from www.rfmd.com.)



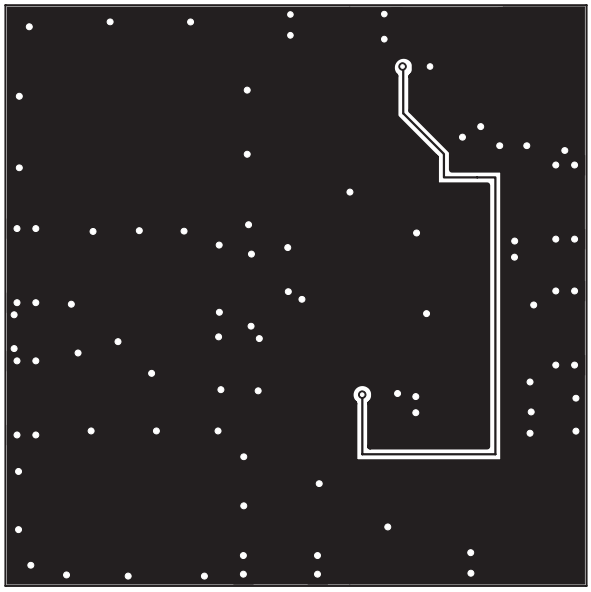
Evaluation Board Layout
3.025” x 3.025”

(Assembly, Top layer, Bottom layer)

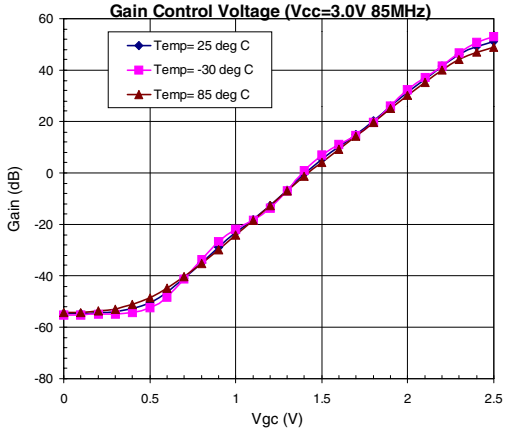




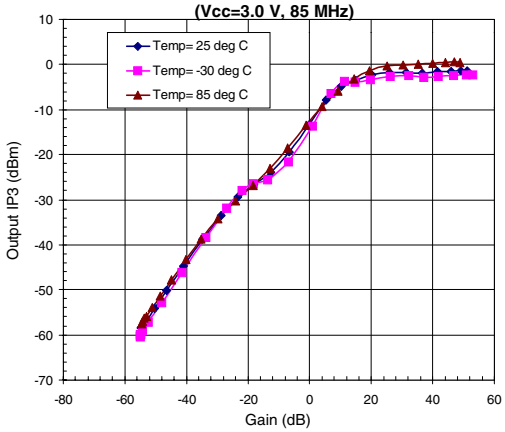
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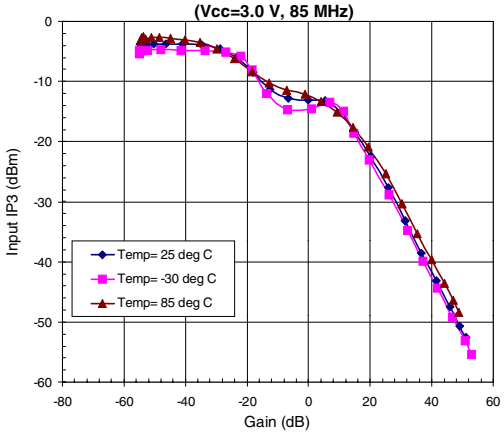
RF2667 CDMA Cascade Conversion Gain vs. Gain Control Voltage (Vcc=3.0V 85MHz)



RF2667 CDMA OIP3 vs. Gain (Vcc=3.0 V, 85 MHz)



RF2667 CDMA IIP3 vs. Gain (Vcc=3.0 V, 85 MHz)



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RF2711

QUADRATURE DEMODULATOR

Typical Applications

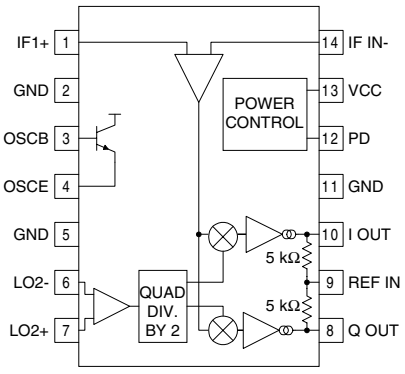
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

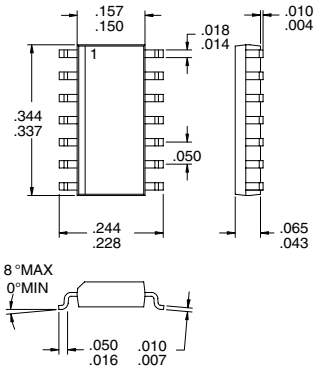
The RF2711 is a monolithic integrated quadrature demodulator intended for use in digital mobile radio receivers. In this application it is used to recover the In-phase and Quadrature baseband signals from the amplified and filtered IF. The RF2711 is intended for IF systems where the IF frequency ranges from 100kHz to 250MHz, and the LO frequency is two times the IF. The IC contains all of the required components to implement the demodulation function of the receiver and contains a digital divider type 90° phase shifter, two double balanced mixers, and baseband amplifiers designed to interface with Analog to Digital Converters. The output DC offset may be slaved to the reference of the ADCs to maintain DC accuracy.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- 5V Power Supply
- On-Chip Active Device for Oscillator
- ADC Compatible Outputs
- Low LO Power Requirement
- Digitally Controlled Power Down Mode
- 100kHz to 250MHz IF Operation

Ordering Information

RF2711	Quadrature Demodulator
RF2711 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

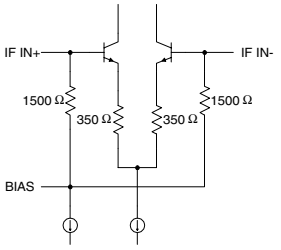
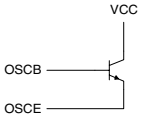
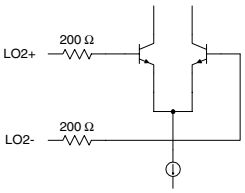
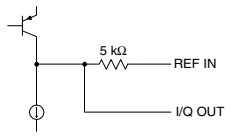
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V_{DC}
IF Input Level	2.0	V_{PP}
LO Input Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

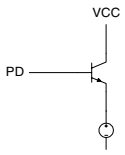
Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5.0V
IF Frequency Range		0.1 to 250		MHz	
Baseband Frequency Range		DC to >10		MHz	Load Impedance > 5kΩ, C_{SHUNT} < 1pF
Baseband Frequency Range		DC to 1		MHz	Load Impedance > 5kΩ, C_{SHUNT} < 10pF
Input Impedance		1000-j1300		Ω	At 50MHz, each input
Output Impedance		5000		Ω	
Maximum Output		>1.25		V_{PP}	With 250mV input
Gain	13	14		dB	Small-signal, 100mV input
I/Q Amplitude Balance		0.1	0.5	dB	
I/Q Phase Accuracy		±1	±5	°	
Reference Voltage		1.5 to 3.5		V	The reference voltage input should provide a low impedance at the I/Q frequency. The voltage sets the DC level seen on the I and Q ports.
DC Offset		3	20	mV	I to Q
DC Offset		3	20	mV	I or Q to REF IN
LO					
Oscillator					Use provided transistor or external LO
Frequency					Twice (2x) the IF frequency
Level		0.1-1		V_{PP}	
Input Impedance		400-j1200		Ω	At 100MHz
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down "ON"		2.5	3.0	V	Threshold voltage; Part is "ON"
Power Down "OFF"	0.5	0.8		V	Threshold voltage; Part is "OFF"
Power Supply					
Voltage		5		V	Specifications
		4.5 to 5.5		V	Operating limits
Current		4.5	7.2	mA	Operating
		300	500	µA	Power Down

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Pin	Function	Description	Interface Schematic
1	IF IN+	Balanced IF input. An input level of 400mV$_{PP}$ gives full output swing; a level of maximum 250mV$_{PP}$ is recommended for linear operation. This pin has no internal DC block, and an external capacitor of 100nF is needed if connected to a DC path.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	OSCB	Base of the LO transistor. This pin is not connected to anything else. This transistor can be used for an oscillator. The collector of the transistor is connected to V_{CC}.	
4	OSCE	Emitter of the LO transistor. This pin is not connected to anything else. Maximum collector current of this device is 1mA, f_T=4.5GHz, h_{fe}=100	See pin 3.
5	GND	Same as pin 2.	
6	LO2-	Balanced input for the doubled LO. An internal divide-by-2 network generates the actual LO for the mixers. The divided signal is not accessible. When the LO is driven single ended this pin should be connected to a 100nF capacitor to ground. This pin has an internal pull-up resistor to V_{CC} and an external DC blocking capacitor of 100nF is recommended.	
7	LO2+	Balanced input for the doubled LO. The input frequency should be twice (2x) the IF frequency. An internal divide-by-2 network generates the actual LO for the mixers. This pin has an internal pull-up resistor to V_{CC}, and an external DC blocking capacitor of 100nF is recommended. LO frequencies below 100kHz are acceptable, providing that the LO signal is square wave. Above 100kHz a sine wave signal is acceptable. The quadrature accuracy of the LO/2 frequency into the mixers is affected by the duty cycle of the LO input signal. Square wave signals with other than 50% duty cycle will degrade the quadrature accuracy of the LO signal, thereby adversely affecting the I and Q quadrature accuracy. Since the LO input is AC coupled, asymmetric sine waves and sine waves clipped on either the top or bottom half will not have 50% duty cycles relative to the internal DC reference point. For this reason, distorted LO sine wave signals will degrade performance in a fashion similar to non-50% duty cycle square waves. A sine wave input with even harmonics less than -15dBc is recommended. The internal limiting buffer amplifier ensures the amplitude stability of the demodulator.	See pin 6.
8	Q OUT	Demodulated baseband Q output. The reference DC level of this pin is set by the voltage of pin 9 (REF IN), which is connected to this pin through a 5kΩ resistor to the collectors of this push-pull output. This results in an output impedance of 5kΩ if the REF IN pin is connected to a low impedance source. The capacitance of the load determines the maximum baseband frequency. A very low capacitive load may stretch the 3dB bandwidth over 10MHz. Another way to increase bandwidth is by connecting a shunt resistor. This will trade-off gain for bandwidth.	
9	REF IN	Reference voltage input for the baseband outputs. This pin can be connected to the reference voltage source of the Analog to Digital Converter. It is connected to the I and Q outputs through 5kΩ resistors. This pin should have an external decoupling capacitor large enough to decouple the lowest baseband frequency.	See pin 8.

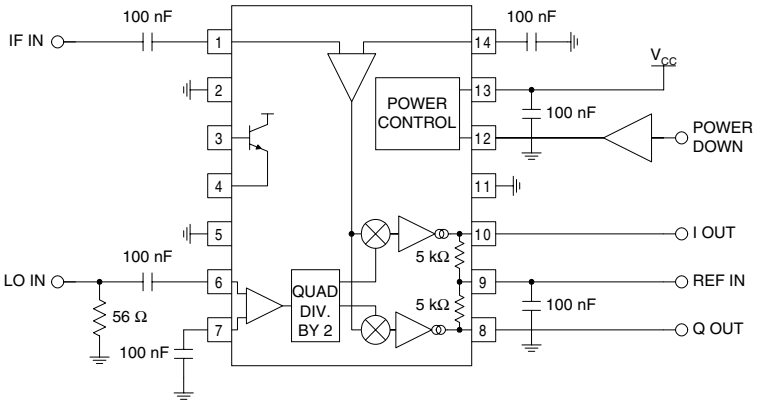
Pin	Function	Description	Interface Schematic
10	I OUT	Demodulated baseband I output. The reference DC level of this pin is set by the voltage of pin 9 (REF IN), which is connected to this pin through a 5kΩ resistor to the collectors of this push-pull output. This results in an output impedance of 5kΩ if the REF IN pin is connected to a low impedance source. The capacitance of the load determines the maximum baseband frequency. A very low capacitive load may stretch the 3dB bandwidth over 10MHz. Another way to increase bandwidth is by connecting a shunt resistor. This will trade gain for bandwidth.	See pin 8.
11	GND	Same as pin 2.	
12	PD	Power Down control. When this pin is "low", all circuits are shut off. A "low" is typically 0.8V or less at room temperature. When this pin is "high", all circuits are operating normally.	
13	VCC	Power supply pin. An external 100nF bypass capacitor is recommended if no other bypass capacitor is nearby.	
14	IF IN-	Balanced IF input. An input level of 400mV$_{PP}$ gives full output swing; a level of maximum 250mV$_{PP}$ is recommended for linear operation. This pin has no internal DC block and an external capacitor of 100nF is needed if connected to a DC path. If the IF is driven by a single-ended source, connect this pin to an 100nF capacitor to ground.	See pin 1.

Spice model for oscillator transistor:

.MODEL RFM2 npn (BF=115.5 VAF=40 IS=.00722F RE=12.1 RC=77.20 RB=1082.6 RBM=295.0 BR=0.6593 CJE=36.7F TF=24.485p CJC=38.75F CJS=161.1F)

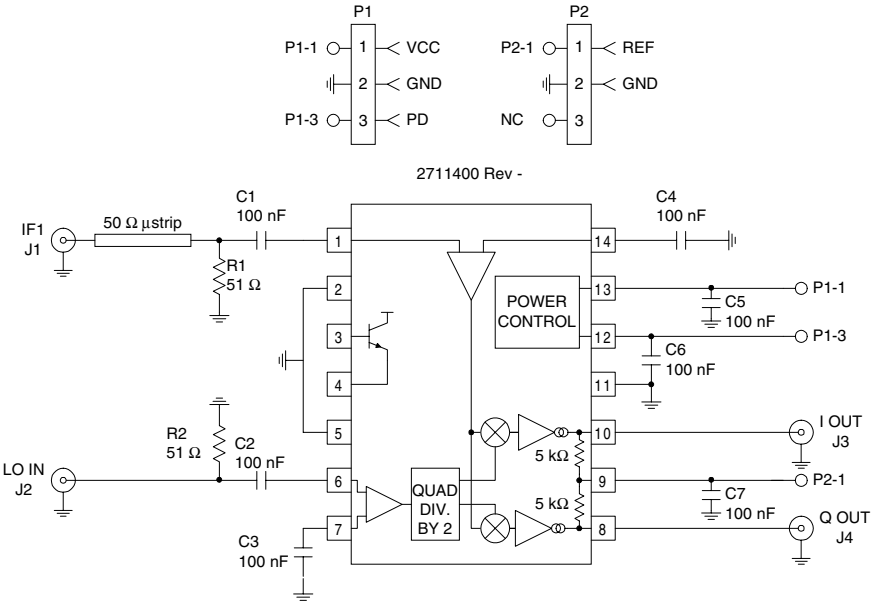
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Application Schematic



Evaluation Board Schematic

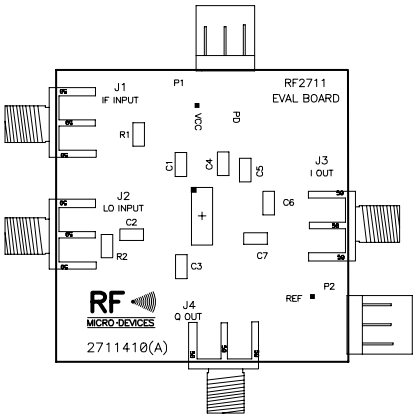
(Download Bill of Materials from www.rfmd.com.)

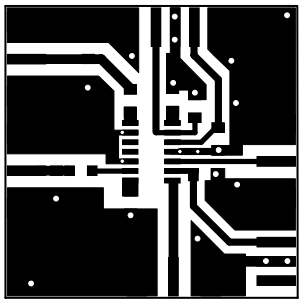


7

QUADRATURE DEMODULATORS

Evaluation Board Layout
1.5” x 1.5”





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Typical Applications

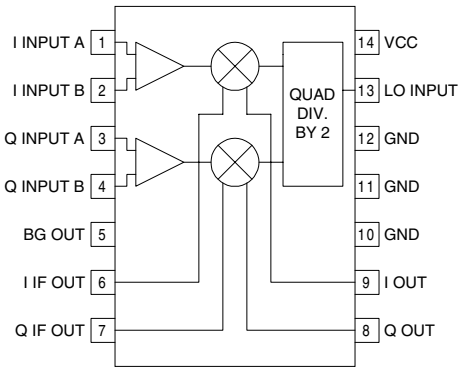
- Digital and Analog Receivers and Transmitters
- High Data Rate Digital Communications
- Spread Spectrum Communication Systems
- Interactive Cable Systems
- Portable Battery Powered Equipment

Product Description

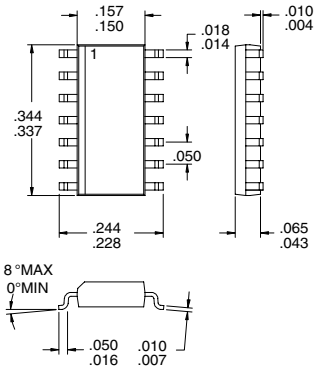
The RF2713 is a monolithic integrated quadrature modulator/demodulator. The demodulator is used to recover the I and Q baseband signals from the amplified and filtered IF. Likewise, the inputs and outputs can be reconfigured to modulate I/Q signals onto an RF carrier. The RF2703 is intended for IF systems where the IF frequency ranges from 100kHz to 250MHz, and the LO frequency is two times the IF. The IC contains all of the required components to implement the modulation/demodulation function and contains a digital divider type 90° phase shifter, two double balanced mixers, and baseband amplifiers designed to interface with Analog to Digital Converters. The unit operates from a single 3V to 6V power supply.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- 3V to 6V Operation
- Modulation or Demodulation
- IF From 100kHz to 250MHz
- Baseband From DC to 50MHz
- Digital LO Quadrature Divider
- Low Power and Small Size

Ordering Information

RF2713	Quadrature Modulator/Demodulator
RF2713 PCBA-D	Fully Assembled Evaluation Board (Demodulator)
RF2713 PCBA-M	Fully Assembled Evaluation Board (Modulator)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
IF Input Level	500	mV_{PP}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

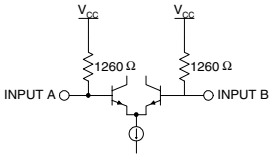
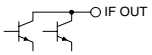
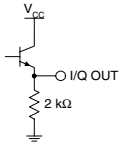
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, IF=100MHz, LO=200MHz, F_{MOD}=500kHz
IF Frequency Range		0.1 to 250		MHz	For IF frequencies below ~2.5MHz, the LO should be a square wave. IF frequencies lower than 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.
Baseband Frequency Range		DC to 50		MHz	
Input Impedance		1200 ‖ 1pF		Ω	Each input, single-ended
LO					
Frequency					Twice (2x) the IF frequency. For IF frequencies below ~2.5MHz, the LO should be a square wave. IF frequencies lower than 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.
Level		0.06 to 1		V_{PP}	
Input Impedance		500 ‖ 1pF		Ω	
Demodulator Configuration					IF_{IN}=28mV_{PP}, LO=200mV_{PP}, Z_{LOAD}=10kΩ
Output Impedance		50 ‖ 1pF		Ω	Each output, I_{OUT} and Q_{OUT}
Maximum Output		1.4		V_{PP}	Saturated
Voltage Gain		20		dB	V_{CC}=3.0V
	22.5	24	25.1	dB	V_{CC}=5.0V
Noise Figure		24		dB	Single Sideband, IF Input of device reactively matched
		35		dB	Single Sideband, 50Ω shunt resistor at IF Input
Input Third Order Intercept Point (IIP_3)		-22		dBm	V_{CC}=3.0V, IF Input of device reactively matched
		-11		dBm	V_{CC}=3.0V, 50Ω shunt resistor at IF Input
		-19			V_{CC}=5.0V, IF Input of device reactively matched
		-8		dBm	V_{CC}=5.0V, 50Ω shunt resistor at IF Input
		-28		dBm	V_{CC}=5.0V, IF Input of device reactively matched, Z_{LOAD}=50Ω
I/Q Amplitude Balance		0.1	0.5	dB	
Quadrature Phase Error		<±1		°	
DC Output		800		mV	V_{CC}=3.0V, I_{OUT} and Q_{OUT} to GND
	2.0	2.4	2.8	V	V_{CC}=5.0V, I_{OUT} and Q_{OUT} to GND
DC Offset		<10	60	mV	I_{OUT} to Q_{OUT}

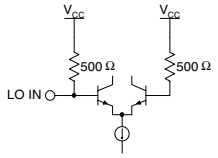
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Modulator Configuration					IF_{IN}=28mV_{PP}, LO=200mV_{PP}, Z_{LOAD}=1200Ω
Maximum Output		200		mV_{PP}	Saturated
Input Voltage		90		mV_{PP}	Single Sideband, 1dB Gain Compression.
Voltage Gain		6		dB	Single Sideband
I/Q Amplitude Balance		0.1		dB	
Quadrature Phase Error		<±1		°	
Carrier Suppression		25		dBc	Unadjusted. Carrier Suppression may be optimized further by adjusting the DC offset level between the A and B inputs.
Sideband Suppression		30		dBc	
Power Supply					
Voltage		2.7 to 6		V	Operating limits
Current		8		mA	V_{CC}=3.0V
	8	10	12	mA	V_{CC}=5.0V

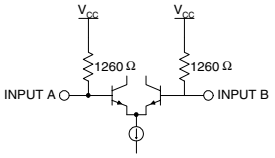
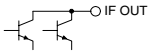
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Pin	Function	Description (Demodulator Configuration)	Interface Schematic
1	I INPUT A	When the RF2703 is configured as a Quadrature Demodulator, both mixers are driven by the IF. Whether driving the mixers single-endedly (as shown in the application schematic) or differentially, the A Inputs (pins 1 and 3) should be connected to each other. Likewise, both B Inputs (pins 2 and 4) should be connected to each other. This ensures that the IF will reach each mixer with the same amplitude and phase, yielding the best I and Q output amplitude and quadrature balance. Note that connecting the inputs in parallel changes the input impedance (see the Gilbert Cell mixer equivalent circuit). The single-ended input impedance (as shown in the application circuit) becomes 630Ω, but in the balanced configuration, the input impedance would remain 1260Ω. The mixers are Gilbert Cell designs with balanced inputs. The equivalent schematic for one of the mixers is shown on the following page. The input impedance of each pin is determined by the 1260Ω resistor to V_{CC} in parallel with a transistor base. Note from the schematic that all four input pins have an internally set DC bias. For this reason, all four inputs (pins 1 through 4) should be DC blocked. The capacitance values of the blocking capacitors is determined by the IF frequency. When driving single-endedly, both the series (pins 1 and 3) and shunt (pins 2 and 4) blocking capacitors should be low impedances, relative to the 630Ω input impedance.	
2	I INPUT B	Same as pin 1, except complementary input.	See pin 1.
3	Q INPUT A	Same as pin 1, except Q Buffer Amplifier.	See pin 1.
4	Q INPUT B	Same as pin 3, except complementary input.	See pin 1.
5	BG OUT	Band Gap voltage reference output. This voltage output is held constant over variations in supply voltage and operating temperature and may be used as a reference for other external circuitry. This pin should not be loaded such that the sourced current exceeds 1mA. This pin should be bypassed with a large (0.1μF) capacitor.	
6	I IF OUT	This pin is not used in the Demodulator Configuration, but must be connected to V_{CC} in order to properly bias the I mixer.	
7	Q IF OUT	Same as pin 6, except Q mixer.	Same as pin 6.
8	Q OUT	Q Mixer's Baseband Output. This pin is NOT internally DC blocked and has DC present due to internal biasing. This is an emitter-follower type output with an internal 2kΩ pull-down resistor. Even though the AC output impedance is ~50Ω, this pin is intended to drive only high impedance loads such as an opamp or an ADC. The output transistor is NOT biased such that it can drive a large signal into a 50Ω load. DC coupling of this output is permitted provided that the DC impedance to ground, which appears in parallel with the internal pull-down resistor, is significantly greater than 2kΩ.	
9	I OUT	Same as pin 8, except Q Mixer's Baseband Output.	Same as pin 8.
10	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
11	GND	Same as pin 10.	
12	GND	Same as pin 10.	

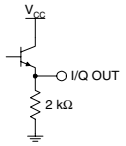
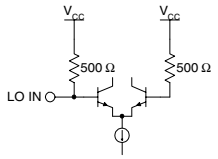
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Pin	Function	Description (Demodulator Configuration)	Interface Schematic
13	LO INPUT	High impedance, single-ended modulator LO input. The LO applied to this pin is frequency divided by a factor of 2 and becomes the "Carrier". For direct demodulation, the Carrier is equal in frequency to the center of the input IF spectrum (except in the case of SSB/SC). The input impedance is determined by an internal 500Ω bias resistor to V_{CC}. An external blocking capacitor should be provided if the pin is connected to a device with DC present. Matching the input impedance is typically achieved by adding a 51Ω resistor to ground on the source side of the AC coupling capacitor. For the LO input, maximum power transfer is not critical. The internal LO switching circuits are controlled by the voltage, not power, into the part. In cases where the LO source does not have enough available voltage, a reactive match (voltage transformer) can be used. The LO circuitry consists of a limiting amplifier followed by a digital divider. The limiting amp ensures that the flip-flop type divider is driven with a square wave over a wide range of input levels. Because the flip-flop uses the rising and falling edges of the limiter output, the quadrature accuracy of the Carrier supplied to the mixers is directly related to the duty cycle, or equivalently to the even harmonic content, of the input LO signal. In particular, care should be taken to ensure that the 2xLO level input to this pin is at least 20dB below the LO level. Otherwise, the LO input is not sensitive to the type of input wave form, except for IF frequencies below ~2.5MHz, in which case the LO input should be a square wave, in order to ensure proper triggering of the flip-flops. IF frequencies below 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.	
14	VCC	Voltage supply for the entire device. This pin should be well bypassed at all frequencies (IF, LO, Carrier, Baseband) that are present in the part.	

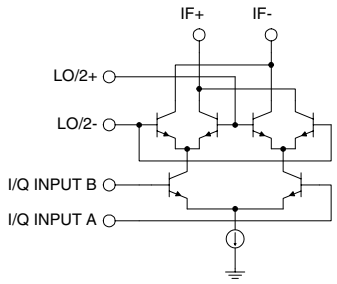
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Pin	Function	Description (Modulator Configuration)	Interface Schematic
1	I INPUT A	When the RF2703 is configured as a Quadrature Modulator, each mixer is driven by an independent baseband modulation channel (I and Q). The mixers can be driven single-endedly (as shown in the modulator application circuit) or differentially. When driving single-endedly, the B Inputs (pins 2 and 4) should be connected to each other. This ensures that the baseband signals will reach each mixer with the same DC reference, yielding the best carrier suppression. Note that the input impedance changes according to the drive mode (see the mixer equivalent circuit on the previous page). The single-ended input impedance (as shown in the modulator application circuit) is 1200Ω for each of the two inputs. In the balanced configuration, the input impedance would be 2400Ω for each of the two inputs. The mixers are Gilbert Cell designs with balanced inputs. The equivalent schematic for one of the mixers is shown on the previous page. The input impedance of each pin is determined by the 1200Ω resistor to V_{CC} in parallel with a transistor base. Note from the schematic that all four input pins have an internally set DC bias. For this reason, all four inputs (pins 1 through 4) should be DC blocked. The capacitance values of the blocking capacitors is determined by the baseband frequency. When driving single-endedly, both the series (pins 1 and 3) and shunt (pins 2 and 4) blocking capacitors should be low impedances, relative to the input impedance. DC bias voltages may be supplied to the inputs pins, if required, in order to increase the amount of carrier suppression. For example, the DC levels on the reference inputs (pins 2 and 4) may be offset from each other by adding different resistor values to ground. These resistors should be larger than 2kΩ. Note from the mixer schematic that all four input pins have an internally set DC bias. If DC bias is to be supplied, the allowable ranges are limited. For 5V applications, the DC reference on both I pins or both Q pins must not go below 2.7V_{DC}, and in no case should the DC voltage on any of the four pins go below 2.0V_{DC} or above 5.5V_{DC}. IF a DC reference is to be supplied, the source must also be capable of sinking current. If optimizing carrier suppression further is not a concern, it is recommended that all four inputs (pins 1 through 4) be DC blocked.	
2	I INPUT B	Same as pin 1, except complementary input.	See pin 1.
3	Q INPUT A	Same as pin 1, except Q Buffer Amplifier.	See pin 1.
4	Q INPUT B	Same as pin 3, except complementary input.	See pin 1.
5	BG OUT	Band Gap voltage reference output. This voltage output is held constant over variations in supply voltage and operating temperature and may be used as a reference for other external circuitry. This pin should not be loaded such that the sourced current exceeds 1mA. This pin should be bypassed with a large (0.1μF) capacitor.	
6	I IF OUT	Connecting pins 6 and 7 to each other accomplishes the summing function of the upconverted I and Q channels. In addition, because these outputs are open collector type, they must be connected to V_{CC} in order to properly bias the Gilbert Cell mixers. Maximum gain and output power occur when the load on these two pins is ~1200Ω. In most applications the impedance of the next stage will be lower and a reactive impedance transforming match should be used if maximum gain and output level are of concern. Biasing, DC blocking, and impedance transformation can simultaneously be achieved with the shunt-L / series-C topology shown in the Application Circuit. The inductance and capacitance values are chosen to achieve a specific impedance transforming ratio at a specific IF frequency. For applications where the gain is not as critical, a 1200Ω resistor may be added in parallel with a choke inductor in place of the matching inductor. If neither gain nor output level is critical, the inductor may be replaced with a resistor that sets the desired source impedance to drive the next stage. If the next stage is an "open" at DC, the blocking capacitor may be eliminated.	

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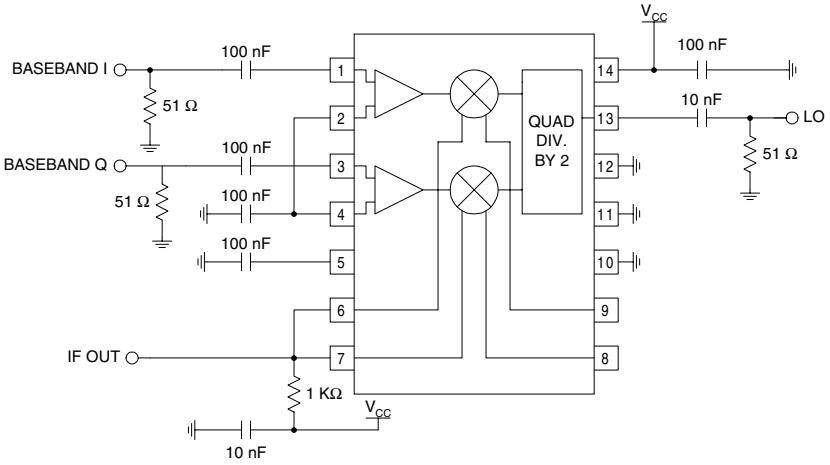
Pin	Function	Description	Interface Schematic
7	Q IF OUT	Same as pin 6, except complementary input.	Same as pin 6.
8	Q OUT	Pins 8 and 9 are not used in a normal quadrature modulator application, and are left unconnected. Note, however, that the outputs of each of these pins are independent upconverted I and Q channels. These signals may be useful in other applications where independent IF channels are needed. Also note that these outputs are optimized as baseband outputs for the demodulator configuration. As a result, the gain rolls-off quickly with increasing frequency. This gain roll-off will limit the usefulness of these pins as independent I and Q upconverters. If these outputs are to be used, please refer to the Demodulator pin descriptions regarding load impedances.	
9	I OUT	Same as pin 8, except Q Mixer's Output.	Same as pin 8.
10	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
11	GND	Same as pin 10.	
12	GND	Same as pin 10.	
13	LO INPUT	High impedance, single-ended modulator LO input. The LO applied to this pin is frequency divided by a factor of 2 and becomes the "Carrier". For modulation, the Carrier is the center of the modulated output spectrum (except in the case of SSB/SC). The input impedance is determined by an internal 500Ω bias resistor to V_{CC}. An external blocking capacitor should be provided if the pin is connected to a device with DC present. Matching the input impedance is typically achieved by adding a 51Ω resistor to ground on the source side of the AC coupling capacitor. For the LO input, maximum power transfer is not critical. The internal LO switching circuits are controlled by the voltage, not power, into the part. In cases where the LO source does not have enough available voltage, a reactive match (voltage transformer) can be used. The LO circuitry consists of a limiting amplifier followed by a digital divider. The limiting amp ensures that the flip-flop type divider is driven with a square wave over a wide range of input levels. Because the flip-flop uses the rising and falling edges of the limiter output, the quadrature accuracy of the Carrier supplied to the mixers is directly related to the duty cycle, or equivalently to the even harmonic content, of the input LO signal. In particular, care should be taken to ensure that the 2xLO level input to this pin is at least 20dB below the LO level. Otherwise, the LO input is not sensitive to the type of input wave form, except for IF frequencies below ~2.5MHz, in which case the LO input should be a square wave, in order to ensure proper triggering of the flip-flops. IF frequencies below 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.	
14	VCC	Voltage supply for the entire device. This pin should be well bypassed at all frequencies (IF, LO, Carrier, Baseband) that are present in the part.	

Gilbert Cell Mixer Equivalent Circuit

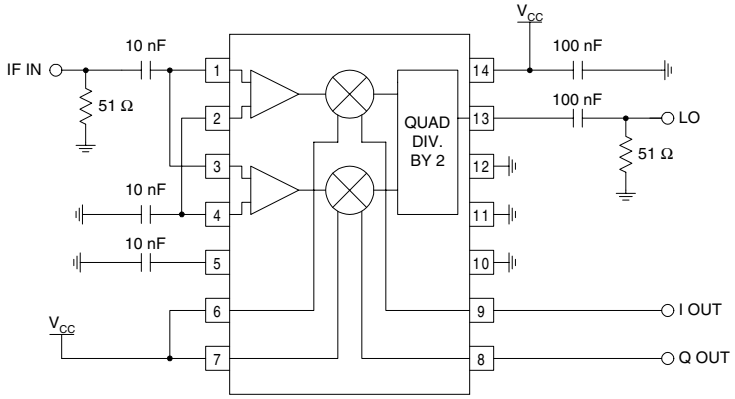


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Application Schematic
Modulator Configuration



Application Schematic
Demodulator Configuration



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RF9957

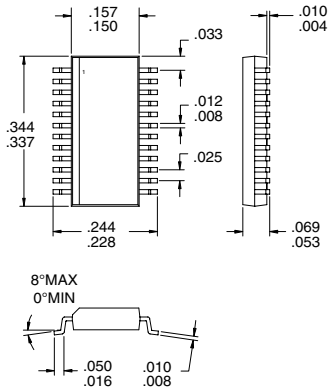
CDMA/FM RECEIVE AGC AND DEMODULATOR

Typical Applications

- CDMA/FM Cellular Systems
- CDMA PCS Systems
- Wireless Local Loop Systems
- Spread Spectrum Cordless Phones
- High Speed Data Modems
- General Purpose Digital Receivers

Product Description

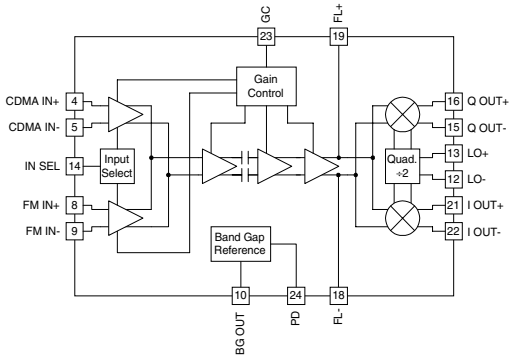
The RF9957 is an integrated complete IF AGC amplifier and Quadrature Demodulator designed for the receive section of dual-mode CDMA/FM cellular and PCS applications. It is designed to amplify received IF signals, while providing 100dB of gain control range, and demodulate to baseband I and Q signals. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 and J-STD-018 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced 15GHz F_T Silicon Bipolar process, and is packaged in a standard miniature 24-lead plastic SSOP package.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation (CDMA and FM)
- Digitally Controlled Power Down Mode
- 2.7V to 3.3V Operation
- Quadrature LO Divider
- IF AGC Amp with 100dB Gain Control

Ordering Information

RF9957	CDMA/FM Receive AGC and Demodulator
RF9957 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

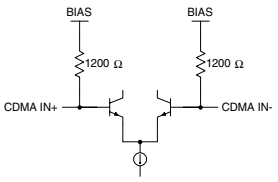
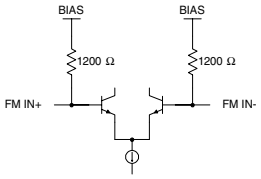
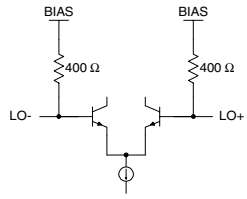
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V_{DC}
Input RF Power	+3	dBm
Ambient Operating Temperature	-40 to +85	℃
Storage Temperature	-40 to +150	℃

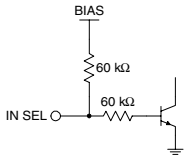
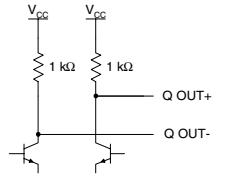
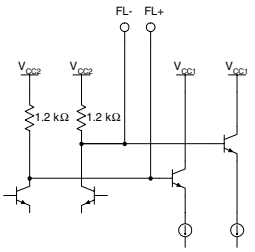
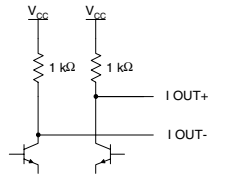
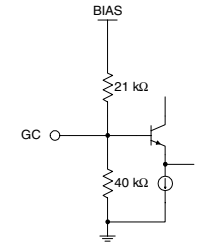
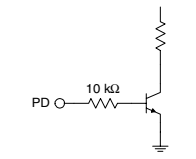
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

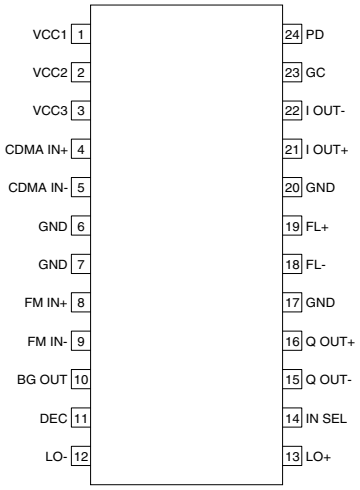
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (Cascaded)					T=25℃, V_{CC}=3.0V, Z_{LOAD}=5kΩ, LO=170MHz @400mV_{PP} IF Freq=85MHz, Z_S=500Ω (CDMA), Z_S=850Ω (FM)
Maximum Gain	+45	+50		dB	V_{GC}=2.5V, FM or CDMA Input, Balanced
Minimum Gain		-55	-50	dB	V_{GC}=0.5V, FM or CDMA Input, Balanced
Gain Variation vs. V_{CC} and T	-3		+3	dB	V_{CC}=2.7V to 3.3V and T=-30℃ to +85℃
Input IP3		-50		dBm	V_{GC}=2.5V, Maximum Gain
	-39	-36		dBm	Gain = 35 dB, P_{IN}=-61dBm
		-4		dBm	V_{GC}=0.5V, Minimum Gain
Noise Figure		5		dB	V_{GC}=2.5V, Maximum Gain
		70		dB	V_{GC}=0.5V, Minimum Gain
IF Input Frequency Range		50 to 250		MHz	
IF Input Impedance	2040	2400	2760	Ω	FM or CDMA, Balanced
	1020	1200	1380	Ω	FM or CDMA, Single Ended
I/Q Frequency Range		0 to 50		MHz	
I/Q Amplitude Balance		0.1	0.5	dB	
I/Q Phase Balance		1	5	deg	
Max I/Q Output Voltage	500			mV_{PP}	Balanced, maximum output level
I/Q DC Output		2.0		V_{DC}	Common Mode
I/Q DC Offset		5	20	mV_{DC}	I OUT+ to I OUT-; Q OUT+ to Q REF-
LO Input Frequency Range		100 to 500		MHz	
LO Input Level		60 to 600		mV_{PP}	Balanced
LO Input Impedance	680	800	920	Ω	Balanced
	340	400	460	Ω	Single Ended
Power Supply					
Supply Voltage	2.7	3.0	3.3	V_{DC}	
Current Consumption		14.5	18	mA	CDMA Mode
		12.5	16	mA	FM Mode
			10	µA	Sleep Mode (PD≤0.5V)

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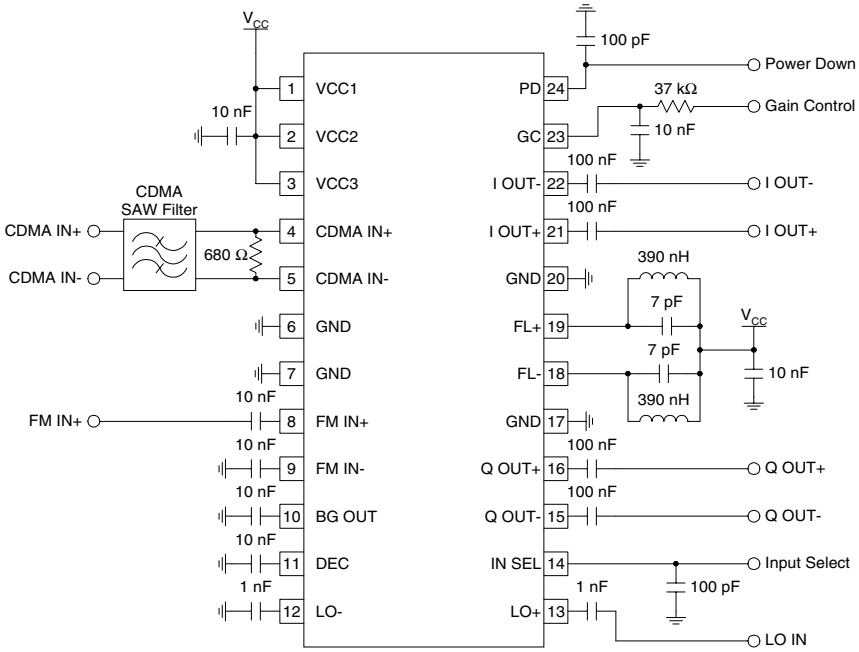
Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LO flip-flop divider and limiting amp. This pin may be connected in parallel with pins 2 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
2	VCC2	Supply voltage for the bandgap, gain control bias circuitry, and AGC stages 2, 3, and 4. This pin may be connected in parallel with pins 1 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
3	VCC3	Supply voltage for the FM and CDMA AGC input stages. This pin may be connected in parallel with pins 1 and 2. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
4	CDMA IN+	CDMA Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
5	CDMA IN-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	GND	Same as pin 6.	
8	FM IN+	FM Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other FM input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
9	FM IN-	Same as pin 8, except complementary input.	See pin 8.
10	BG OUT	Bandgap Voltage Reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
12	LO-	LO Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The frequency of the signal applied to these pins is internally divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 400Ω (balanced is 800Ω). The LO input may be driven single-ended but balanced provides optimum gain and phase balance.	
13	LO+	Same as pin 12, except complementary input.	See pin 12.

14	**IN SEL**	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" (≥VCC-0.7V_{DC}) selects CDMA mode. A logic "low" (<0.5V_{DC}) selects FM mode. In FM mode, ONLY the I mixer is active. There is no Q output in FM mode. The impedance on this pin is 30kΩ.	
15	**Q OUT-**	Balanced Baseband Output of Q Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in CDMA mode, but is NOT active in FM mode. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5kΩ. The balanced load should be 5kΩ. The single-ended output impedance is 1kΩ, while the balanced output impedance is 2kΩ.	
16	**Q OUT+**	Same as pin 15, except complementary output.	See pin 15.
17	**GND**	Same as pin 6.	
18	**FL-**	Balanced AGC Output/Demod Input. This balanced node is pinned out to allow shunt filtering of the AGC output signal as it enters the demodulator. The basic configuration of the filter should consist of a shunt inductor and shunt capacitor, both connected to the power supply, as the internal circuitry requires this power supply connection through the inductor to operate.	
19	**FL+**	Same as pin 18, except complementary.	See pin 18.
20	**GND**	Same as pin 6.	
21	**I OUT+**	Balanced Baseband Output of I Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in both CDMA and FM modes. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5kΩ. The balanced load should be 5kΩ. The single-ended output impedance is 1kΩ, while the balanced output impedance is 2kΩ.	
22	**I OUT-**	Same as pin 21, except complementary output.	See pin 22.
23	**GC**	Analog Gain Control for AGC Amplifiers. The valid control range is from 0.5 to 2.5V_{DC}. These voltages are valid for ONLY a 37kΩ source impedance. The gain range for the AGC is 95dB.	
24	**PD**	Power Down Control. When logic "high" (≥V_{CC}-0.3V), all circuits are operating; when logic "low" (≤0.5V), all circuits are turned off. The input impedance of this pin is 10kΩ.	

RF9957 Pin-Out



Application Schematic



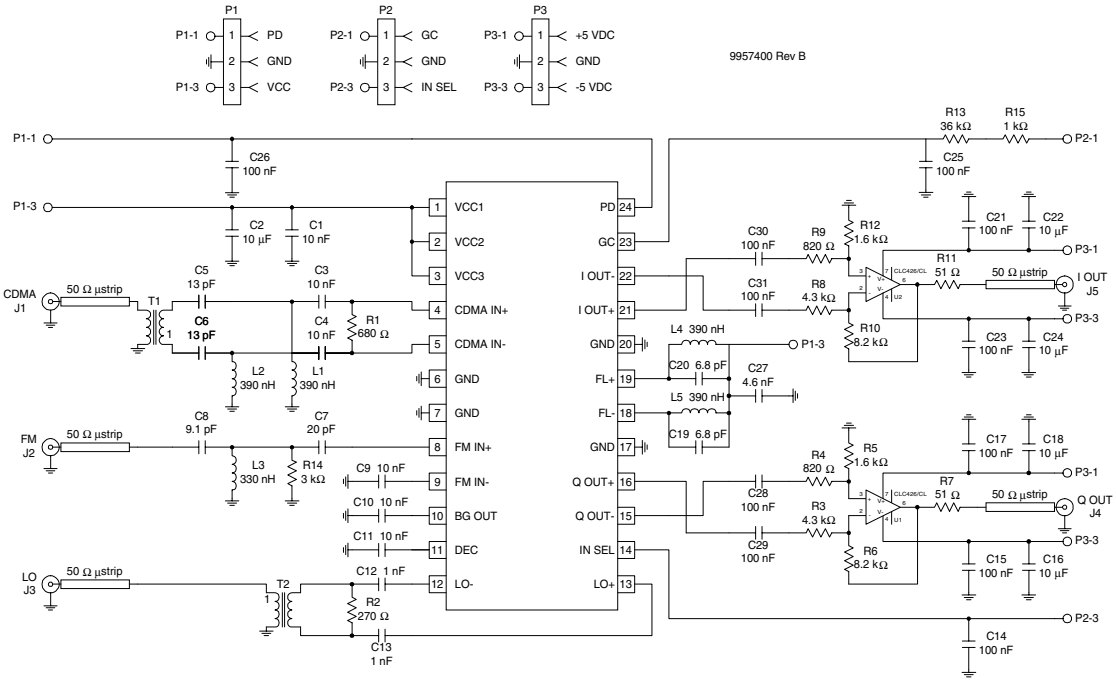
7

QUADRATURE DEMODULATORS

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Evaluation Board Schematic

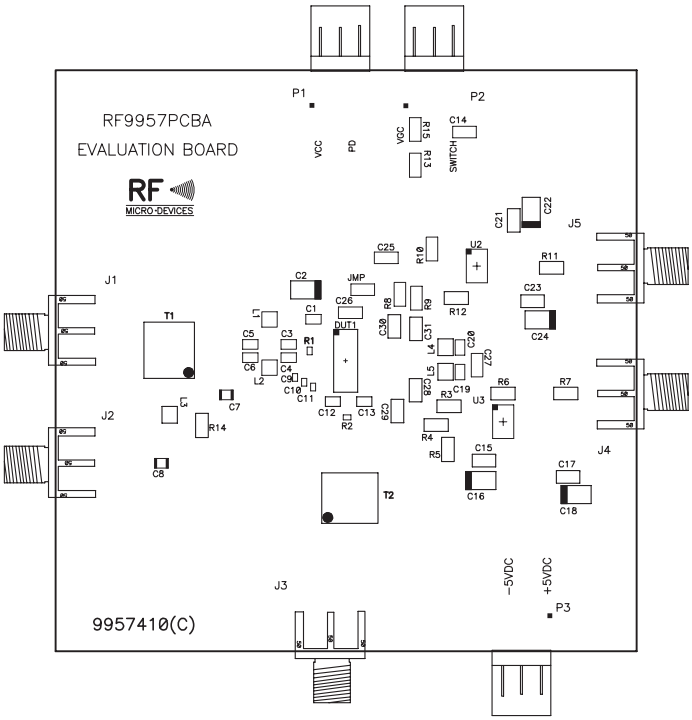
(Download Bill of Materials from www.rfmd.com.)

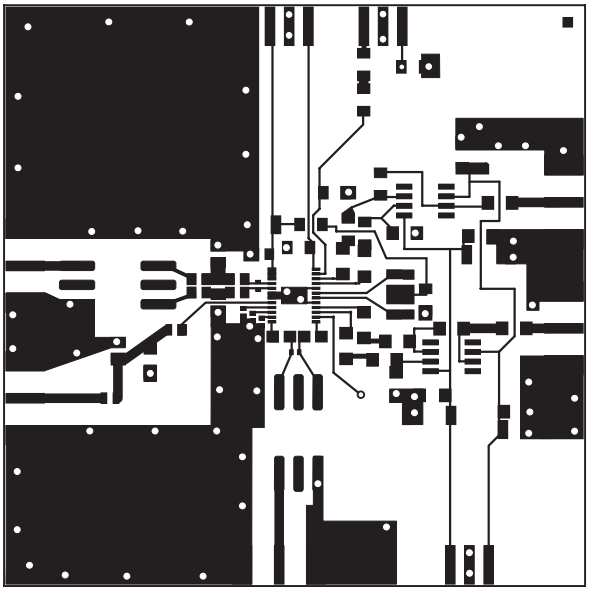


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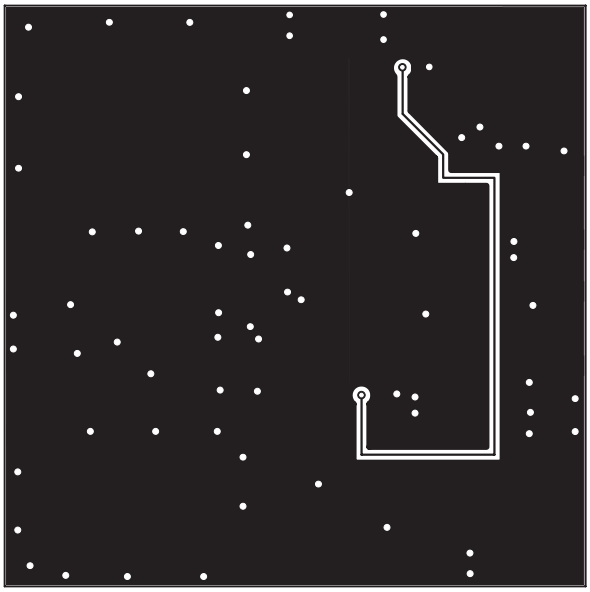
Evaluation Board Layout
3.025” x 3.025”

(Assembly, Top layer, Bottom layer)

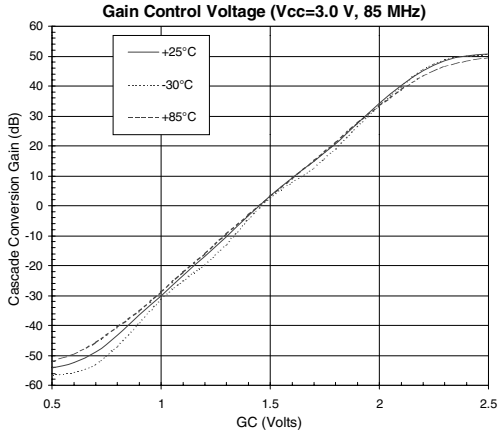




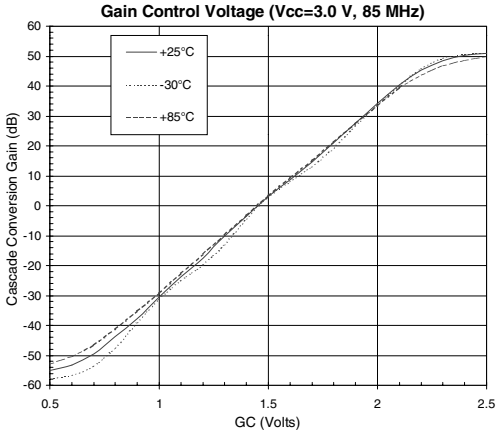
Evaluation Board Layout cont'd



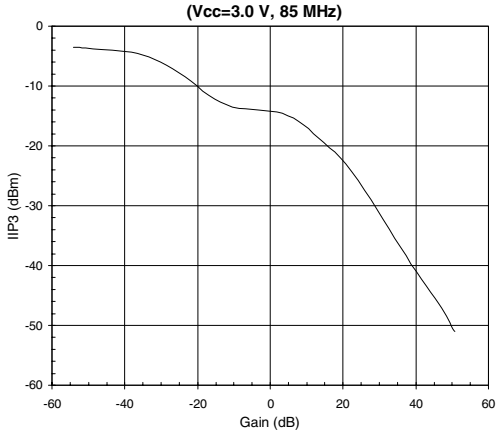
RF9957 CDMA Cascade Conversion Gain vs. Gain Control Voltage (Vcc=3.0 V, 85 MHz)



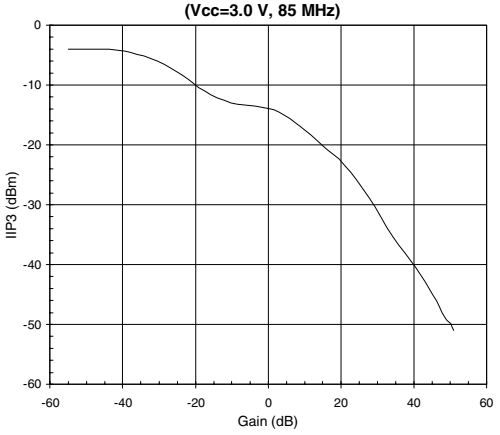
RF9957 FM Cascade Conversion Gain vs. Gain Control Voltage (Vcc=3.0 V, 85 MHz)



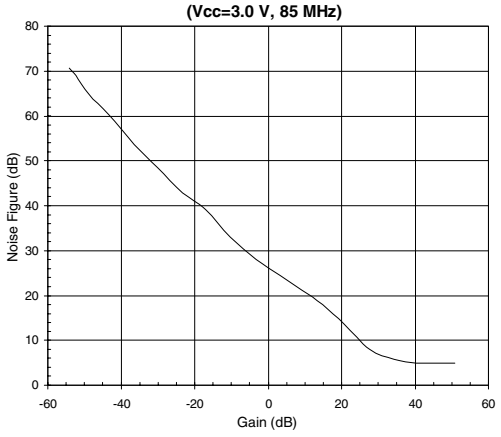
RF9957 CDMA IIP3 vs. Gain (Vcc=3.0 V, 85 MHz)



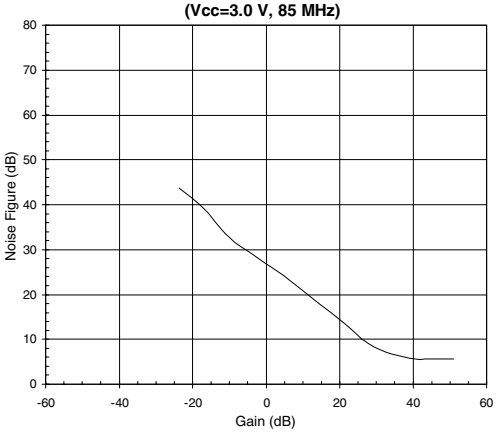
RF9957 FM IIP3 vs. Gain (Vcc=3.0 V, 85 MHz)



RF9957 CDMA Noise Figure vs. Gain (Vcc=3.0 V, 85 MHz)



RF9957 FM Noise Figure vs. Gain (Vcc=3.0 V, 85 MHz)



8 Front-Ends

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Casc. Gain (dB)	Gain Control (dB)	Casc. IIP_3 (dBm)	Casc. NF (dB)	Package	Page
RF2401	Low Noise Amplifier/Mixer	300 to 1100	5	20	24	21	-17	4.3	SOP-14	8-1
RF2406	CDMA/FM Low Noise Amplifier/Mixer	500 to 1100	2.7 to 4	23	27	19.5	-4	4.3	SSOP-28	8-13
RF2411	Low Noise Amplifier/Mixer	500 to 1900	3 to 6.5	20	27	n/a	-8	2.4	SOP-14	8-23
RF2418	Low Current LNA/Mixer	400 to 1100	3 to 6.5	4.5	19	n/a	-13	3.9	SOP-14	8-35
RF2431	High Frequency LNA/Mixer	1500 to 2500	3 to 6.5	13	23	n/a	-14	3.5	SOP-16	8-43
RF2442	High-Linearity Low Noise Amplifier	500 to 2500	3	12	19	n/a	+3	1.8	MSOP-8	4-231
RF2444	High Frequency LNA/Mixer	2400 to 2500	2.7 to 3.6	20	28	16	-23 to -8	4.5 to 18	SSOP-16 EPP	8-53
RF2448	PCS CDMA Low Noise Amplifier/Mixer 1500MHz to 2200MHZ Downconverter	1500 to 2200	2.65 to 3.9	8	-4 to +25	29	-11 to +17.5	3 to 23	SSOP-16 EDF	8-69
RF2449	CDMA/FM Low Noise Amplifier/Mixer 900MHz Downconverter	869 to 894	2.75	20	28	21			SSOP-24	8-75
RF2457	900MHz 3V Low Current LNA/Mixer	902 to 928	2.7 to 3.3	5	8.5	13	-3	2.5	MSOP-10	8-85
RF2458	3V PCS Downconverter	1500 to 2500	2.7 to 3.6	38	14	n/a	+3	10	MSOP-10	8-91
RF2459	3V PCS Downconverter	1500 to 2500	2.7 to 3.6	20	10	n/a	+7	14	MSOP-8	8-97
RF2486	PCS Low Noise Amplifier/Mixer	1500 to 2500	2.7 to 5.0	52	26	n/a	-15	4.0	SSOP-24	8-105
RF9906	CDMA/FM Low Noise Amplifier/Mixer	500 to 1500	3.6	30	30	9	-13	2.6	SSOP-24	8-113
RF9936	PCS Low Noise Amplifier/Mixer	1500 to 2500	3.6	5 to 46	28	10	-9 to -14	2.5 to 5.1	SSOP-24	8-121
RF9986	PCS Low Noise Amplifier/Mixer	1500 to 2500	3.6	5 to 48	26	n/a	-11	2.5	SSOP-24	8-131

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RF MICRO·DEVICES

RF2401

LOW NOISE AMPLIFIER/MIXER

Typical Applications

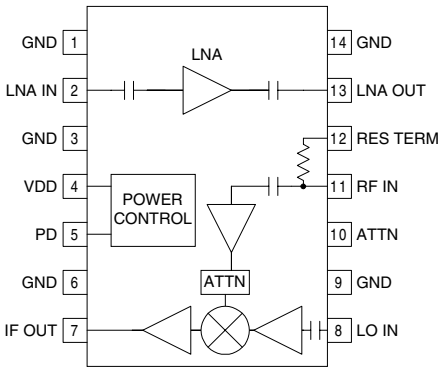
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

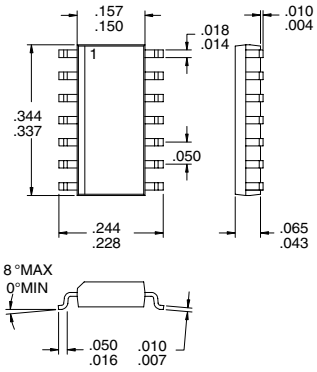
The RF2401 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the front-end functions of the receiver except for the passive filtering and LO generation. It contains a high dynamic range LNA (low-noise amplifier), an attenuator to reduce signal level in the presence of large received signals, a second RF amplifier, a double balanced mixer, an LO buffer amplifier, and an IF output amplifier which will drive a 50Ω load. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the attenuator. The mixer input is buffered to provide high isolation from the LO to the input port. Blocking capacitors are contained on the chip (except for the IF Output).

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Power Down Capability
- High Dynamic Range
- Low Current Drain
- High LO Isolation
- RF Attenuator for Large Signals
- 300MHz to 1100MHz Operation

Ordering Information

RF2401	Low Noise Amplifier/Mixer
RF2401 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

RF2401

Absolute Maximum Ratings

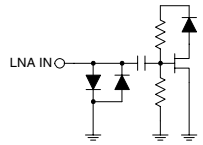
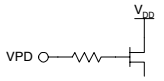
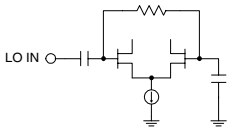
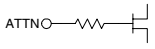
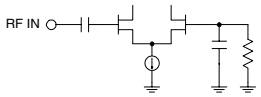
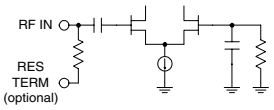
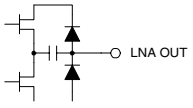
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

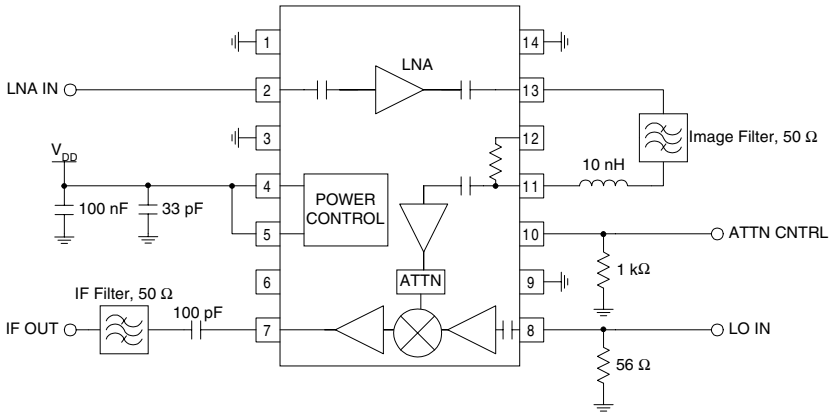
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=5V, RF=915MHz, LO=986MHz
Frequency Range		300 to 1100		MHz	
Cascade Gain	22	24		dB	RF=850MHz
Cascade IP3		-17		dBm	Referenced to input
Cascade Noise Figure		4.3		dB	Single sideband
LO to LNA Input Rejection		65		dB	
First Section (LNA)					
Noise Figure		2.9		dB	
Input VSWR		1.5:1			
Input IP3		-10		dBm	
Gain		11		dB	
Reverse Isolation		30		dB	
Output VSWR		1.3:1			
Second Section (RF Amp, Mixer, IF)					
Noise Figure		10		dB	Single sideband
Input VSWR		1.5:1			In order to achieve a low VSWR match at this input, a 10nH chip inductor is placed in series with this port. If direct coupling is used (no noise image filter between LNA OUT and RF IN ports), no inductor is necessary.
Input IP3		-7		dBm	
Conversion Gain		12		dB	ATTN=GND
Conversion Gain Change	-25	-21	-17	dB	ATTN=V_{DD}, RF=850MHz
Output Impedance		50		Ω	
LO Input					
LO Frequency		250 to 1150		MHz	
LO Level		-6 to +3		dBm	
LO to RF Rejection		25		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.3:1			With external 75Ω termination
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage; Part is "ON"
Power Down "OFF"		0		V	Threshold voltage; Part is "OFF"
Power Supply					
Voltage		4.5 to 6.5		V	
Current Consumption		20	30	mA	On
Current Consumption		0.2	0.5	mA	Power Down

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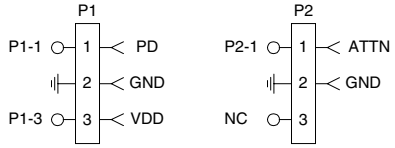
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	LNA IN	This pin has input protection diodes to protect the LNA from ESD and high RF levels. Because the diodes are present, an external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin.	
3	GND	Same as pin 1.	
4	VDD	Supply Voltage for the LNA, Mixer, and all three buffer amplifiers. An external RF bypass capacitor is required and an optional 0.01µF bypass capacitor will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	PD	Power Down control pin. With 0V connected to this pin, the part draws minimum current (<0.5mA). When connected to V_{DD}, the part is fully operational. For applications where VPD is not controlled, this pin is simply connected to V_{DD}.	
6	GND	Same as pin 1.	
7	IF OUT	50Ω buffered IF output port. This pin is NOT DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present, or a device that presents a finite DC impedance.	
8	LO IN	Mixer LO input. If approximately 0dBm of LO power is available, a shunt 56Ω resistor can be used for matching. If the available LO power is near -6dBm, then a reactive match may be required. A high pass matching network, such as a single shunt inductor is the recommended topology because it also rejects IF noise at the mixer input. This pin is internally DC blocked.	
9	GND	Same as pin 1.	
10	ATTN	Attenuation control for mixer RF input. When tied to V_{DD}, the mixer's conversion gain is reduced by approximately 20dB at 915MHz. When tied to ground, the mixer's conversion gain is at maximum (approximately 12dB at 915MHz).	
11	RF IN	Mixer RF Input port. For a 50Ω match at 900MHz use a 10nH series inductor. The mixer inputs are internally DC blocked. When pin 12 is tied to ground, an internal matching resistor is connected in parallel at the expense of increasing the mixer's noise figure and reducing its gain. There is an internal blocking capacitor between this pin and the mixer's input, but not between the pin and the internal matching resistor (see the functional block diagram).	
12	RES TERM	Connecting this pin to ground causes an internal matching resistor to be connected in parallel with the mixer's input. This eliminates the need for a matching inductor and matches the mixer input over a broad band, but the mixer's noise figure and gain will be degraded. When matching pin 11 with an inductor, pin 12 should be left unconnected.	
13	LNA OUT	This pin has protection diodes to protect the LNA from ESD and high RF levels. Because the diodes are present, an external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If pin 13 is connected directly to pin 11, then no blocking capacitor is required.	
14	GND	Same as pin 1.	

Application Schematic

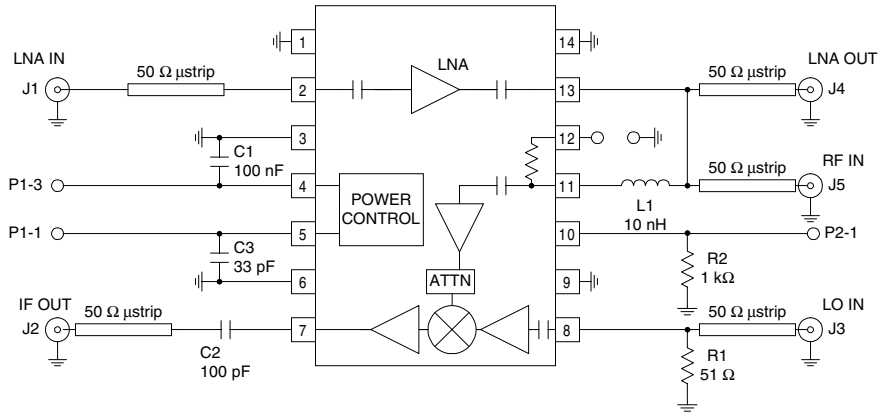


Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

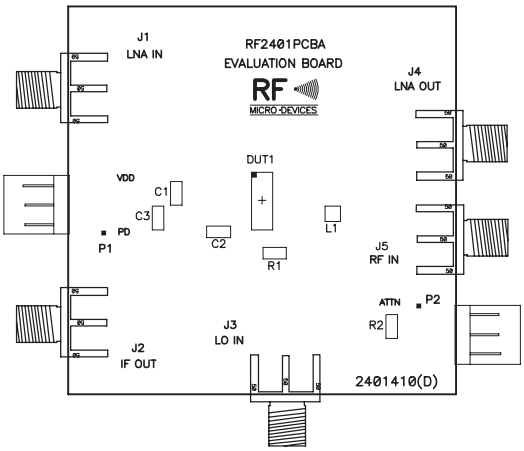


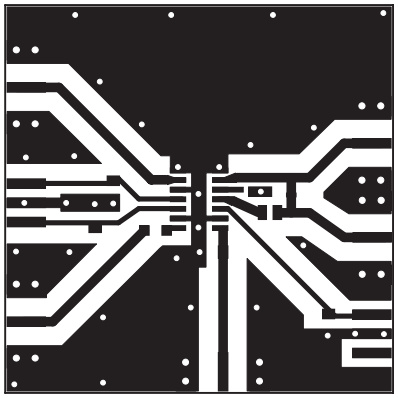
2401400 Rev E



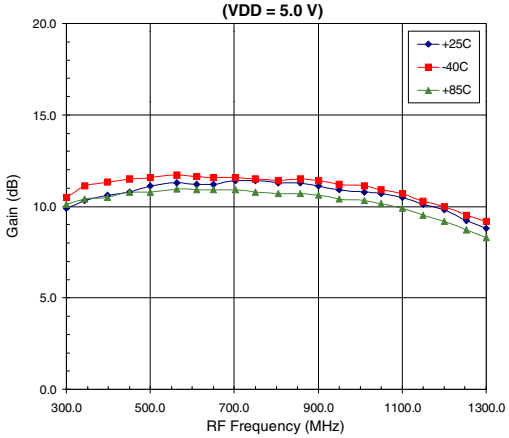
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Evaluation Board Layout
Board Size 2.020” x 2.020”

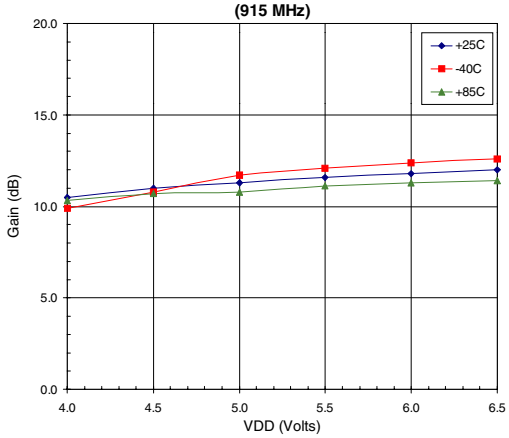




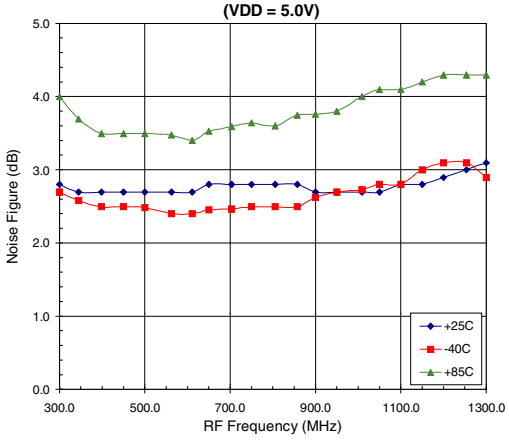
LNA Gain
(VDD = 5.0 V)



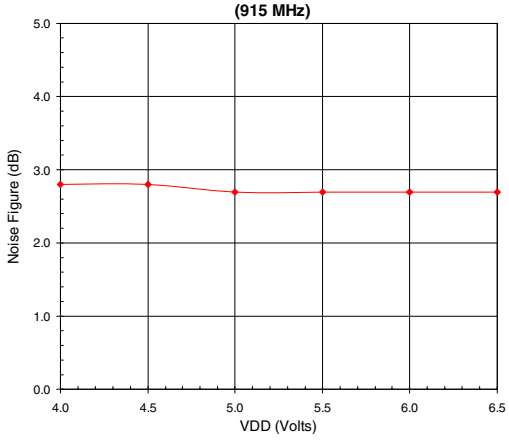
LNA Gain
(915 MHz)



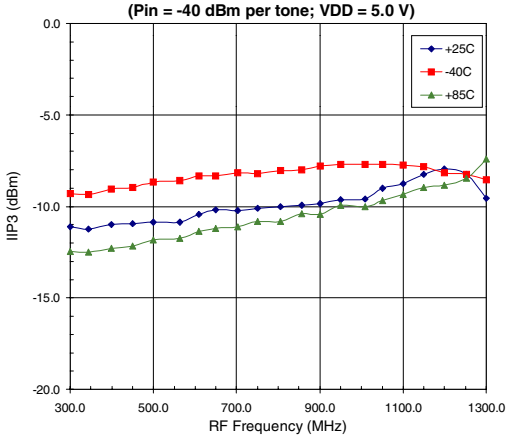
LNA Noise Figure
(VDD = 5.0V)



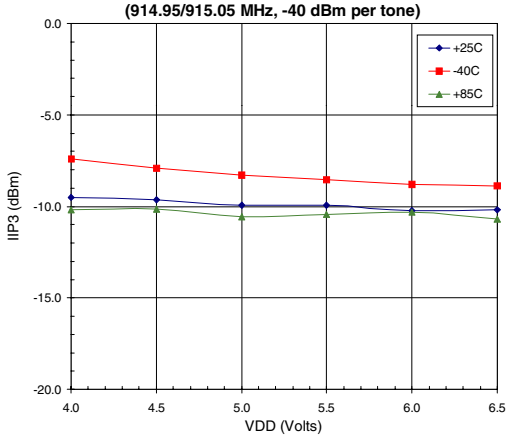
LNA Noise Figure
(915 MHz)



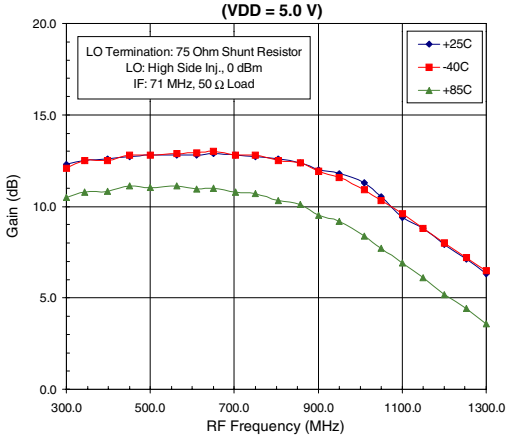
LNA Input IP3
(Pin = -40 dBm per tone; VDD = 5.0 V)



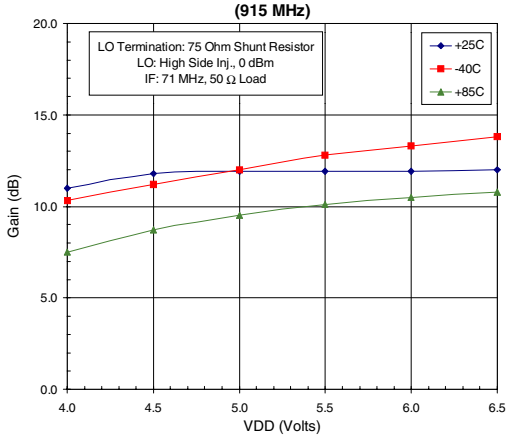
LNA Input IP3
(914.95/915.05 MHz, -40 dBm per tone)



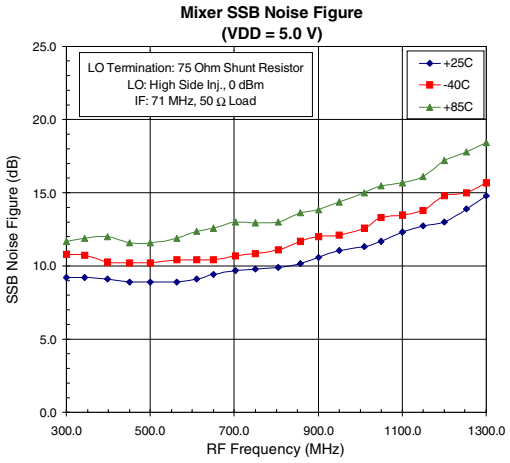
Mixer Power Gain
(VDD = 5.0 V)



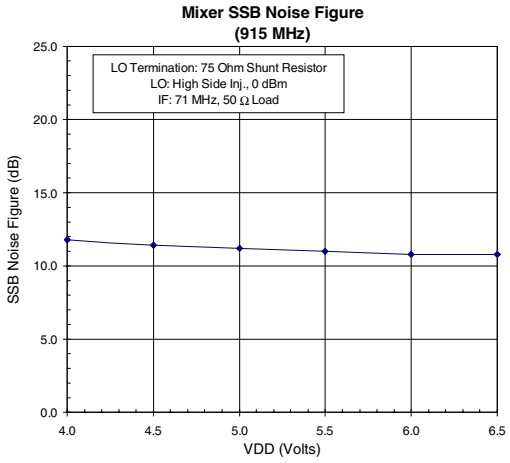
Mixer Power Gain
(915 MHz)



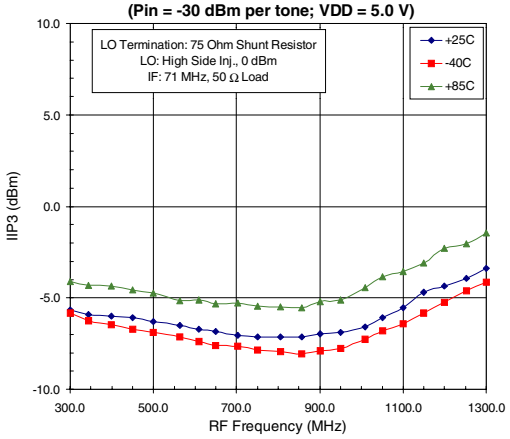
Mixer SSB Noise Figure
(VDD = 5.0 V)



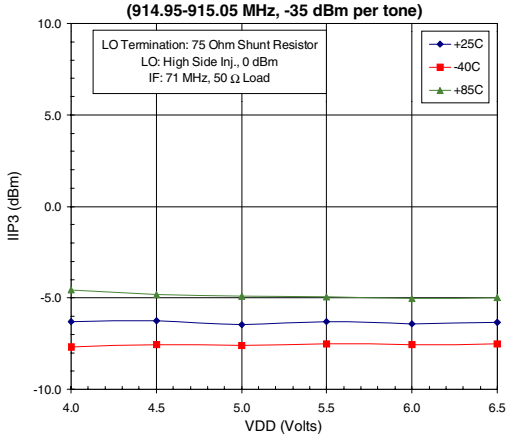
Mixer SSB Noise Figure
(915 MHz)



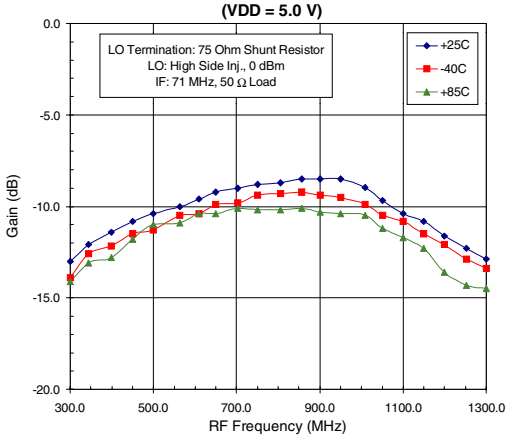
Mixer Input IP3
(Pin = -30 dBm per tone; VDD = 5.0 V)



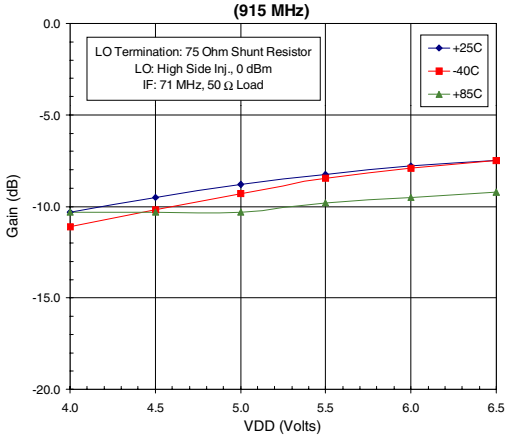
Mixer Input IP3
(914.95-915.05 MHz, -35 dBm per tone)



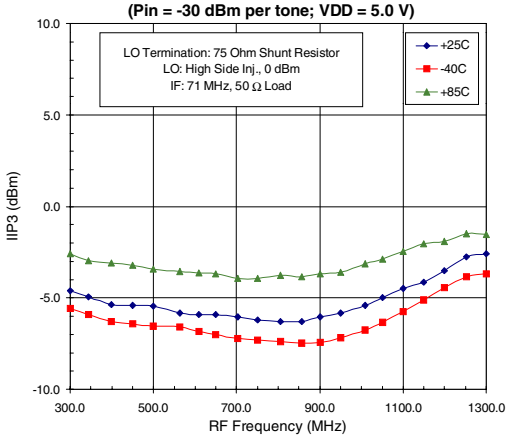
Mixer Power Gain, Attenuator On
(VDD = 5.0 V)



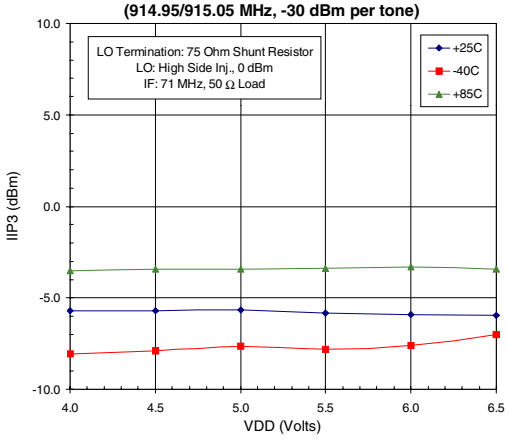
Mixer Power Gain, Attenuator On
(915 MHz)



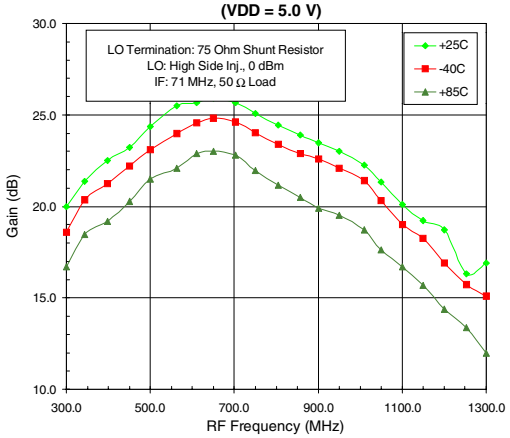
Mixer Input IP3, Attenuator On
(Pin = -30 dBm per tone; VDD = 5.0 V)



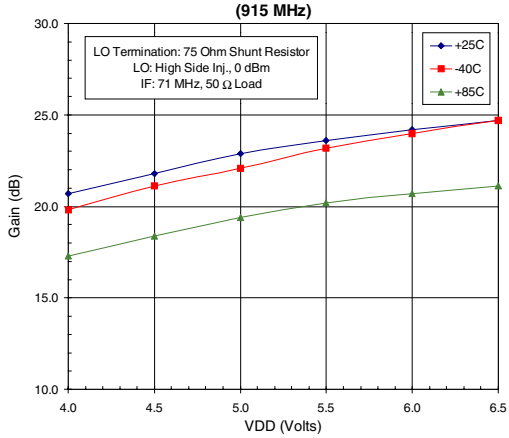
Mixer Input IP3, Attenuator On
(914.95/915.05 MHz, -30 dBm per tone)



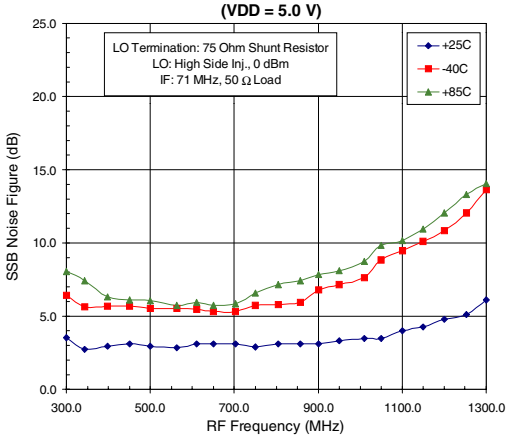
LNA + Mixer Power Gain (VDD = 5.0 V)



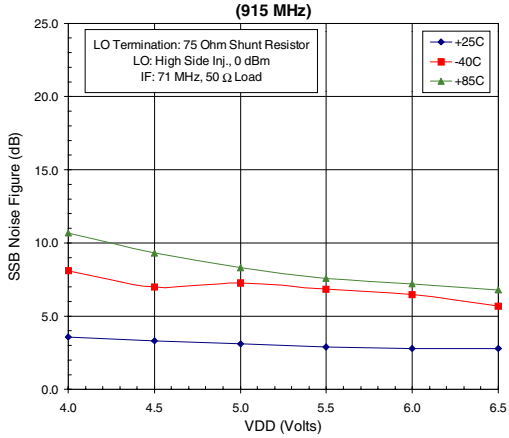
LNA + Mixer Power Gain (915 MHz)



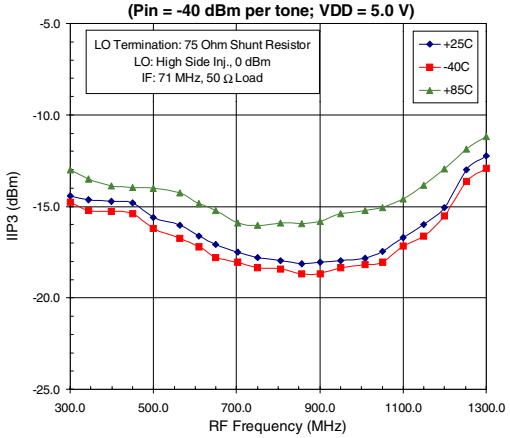
LNA + Mixer SSB Noise Figure (VDD = 5.0 V)



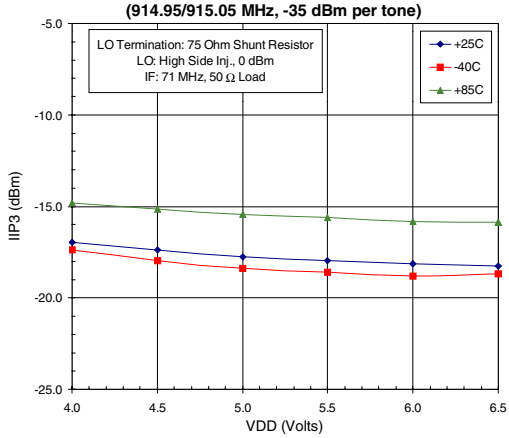
LNA + Mixer SSB Noise Figure (915 MHz)



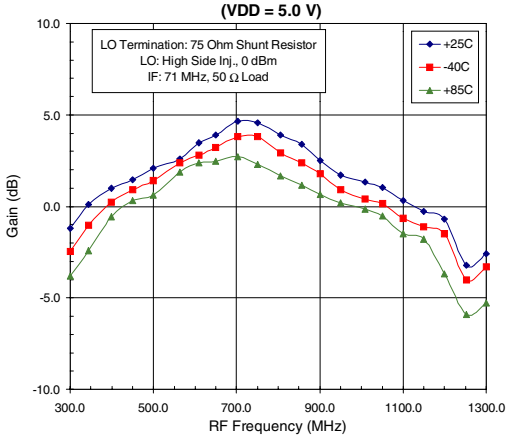
LNA + Mixer Input IP3 (Pin = -40 dBm per tone; VDD = 5.0 V)



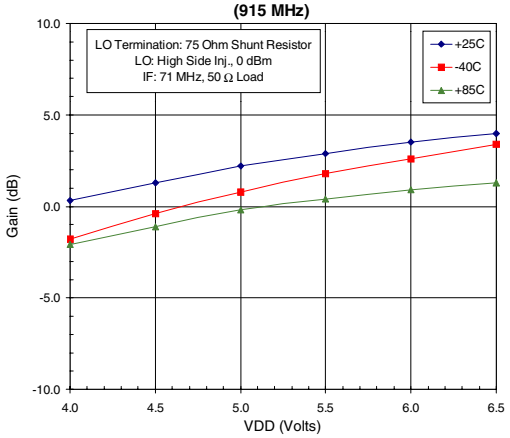
LNA + Mixer Input IP3 (914.95/915.05 MHz, -35 dBm per tone)



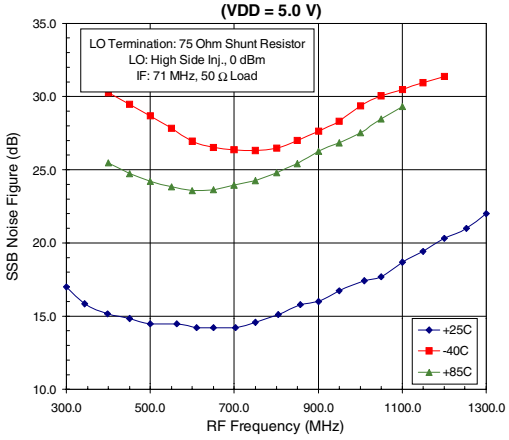
LNA + Mixer Power Gain, Attenuator On (VDD = 5.0 V)



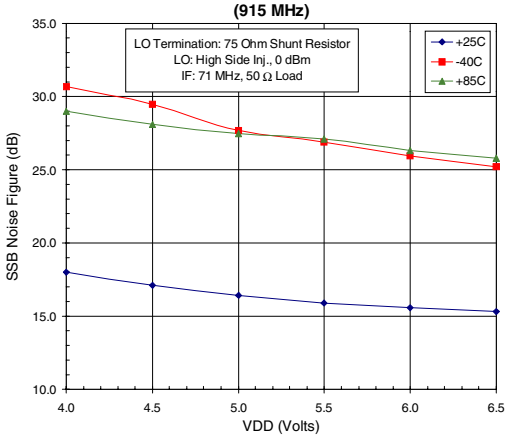
LNA + Mixer Power Gain, Attenuator On (915 MHz)



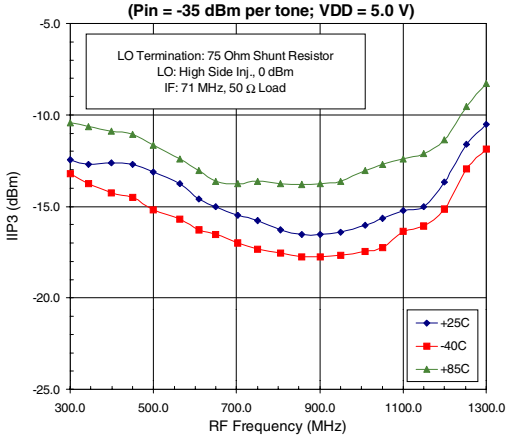
LNA + Mixer SSB Noise Figure, Attenuator On (VDD = 5.0 V)



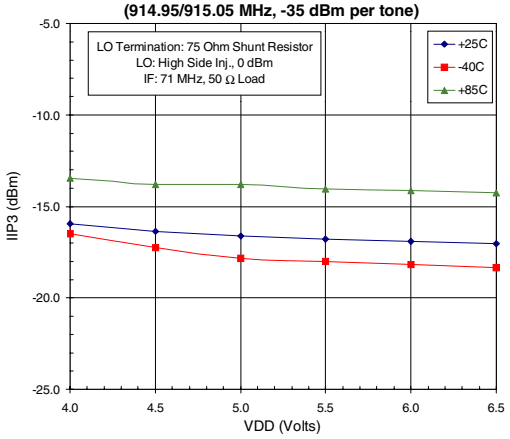
LNA + Mixer SSB Noise Figure, Attenuator On (915 MHz)



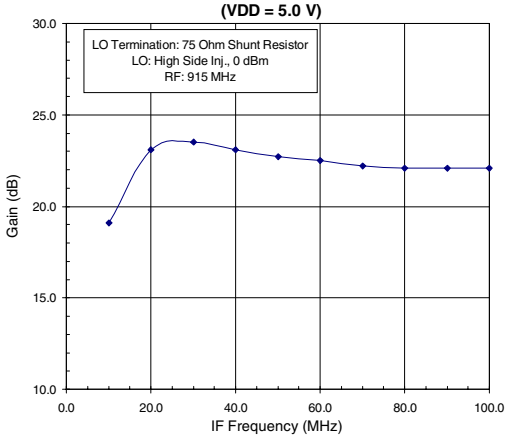
LNA + Mixer Input IP3, Attenuator On (Pin = -35 dBm per tone; VDD = 5.0 V)



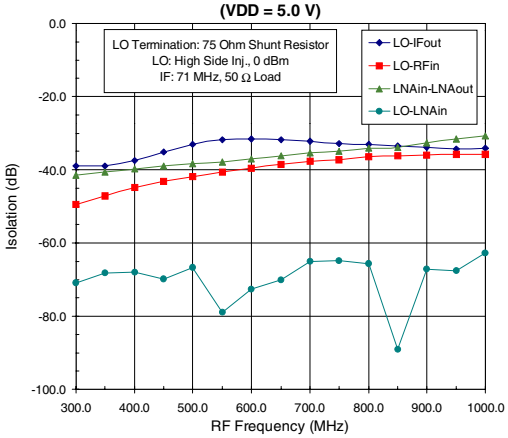
LNA + Mixer Input IP3, Attenuator On (914.95/915.05 MHz, -35 dBm per tone)



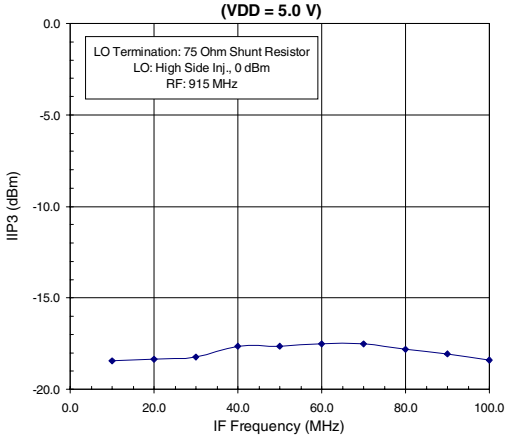
LNA + Mixer Power Gain versus IF Frequency (VDD = 5.0 V)



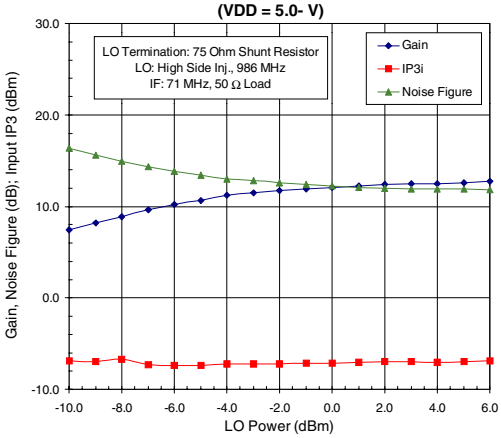
Isolation (VDD = 5.0 V)



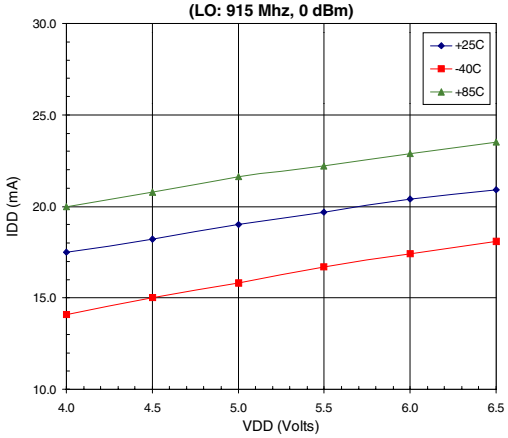
LNA + Mixer Input IP3 versus IF Frequency (VDD = 5.0 V)



Mixer Performance versus LO Power (VDD = 5.0- V)



IDD versus VDD (LO: 915 Mhz, 0 dBm)



8

FRONT-ENDS

RF2401

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RF2406

CDMA/FM LOW NOISE AMPLIFIER/MIXER

Typical Applications

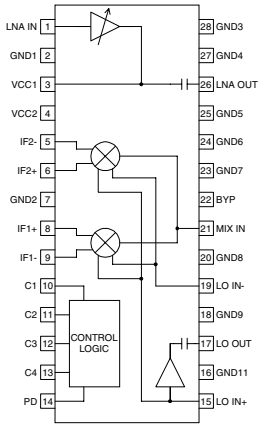
- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

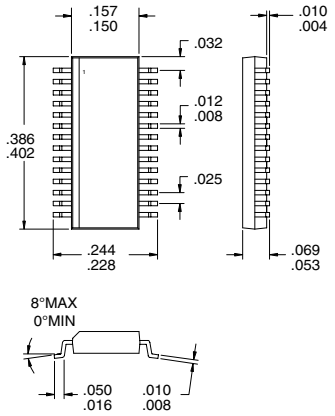
The RF2406 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals while providing 30dB of stepped gain control range and features digital control of LNA gain, IF output selection, LO buffer enable, power down mode, and low current "lazy" mode. The digitally selected "lazy" mode reduces current drain by approximately 10mA, putting the IC in a lower current drain, noise and IP3 state. This gives the receiver designer added flexibility to dynamically optimize these downconverter parameters. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-28.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-28

Features

- Complete Receiver Front-End
- Stepped LNA Gain Control
- Low Current-Drain "Lazy" Mode
- Buffered LO Output
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation

Ordering Information

RF2406	CDMA/FM Low Noise Amplifier/Mixer
RF2406 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

RF2406

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=881MHz, LO=966MHz @-3dBm RF2=882 MHz for IIP3 Measurements See Mode Control Logic Table
RF Frequency Range		500 to 1100		MHz	
LO Frequency Range		500 to 1100		MHz	
IF Frequency Range		0.1 to 250		MHz	
Power Supply					
Voltage		2.7 to 4.0		V	
Current Consumption		20		mA	FM
		25		mA	CDMA Max. Gain
		26		mA	CDMA Nom. Gain
		18		mA	CDMA Min. Gain
		adds 4		mA	LO Buffer ON
		subtracts 10		mA	"Lazy" Mode
		< 20		µA	Power Down
Max Dynamic Range Mode					
Cascaded Perform. to IF1					1kΩ balanced load, 3.0dB Image Filter Loss CDMA Max. Gain
Cascade Conversion Gain		24		dB	
Cascade Input IP3 to IF1		-4		dBm	
Cascade Noise Figure		4.3		dB	
Cascaded Perform. to IF2					870Ω load, 3dB Image Filter Loss FM
Cascade Conversion Gain		18		dB	
Cascade Input IP3		-4		dBm	
Cascade Noise Figure		4.3		dB	
First Section (LNA)					
Gain		14.5		dB	FM and CDMA Max. Gain
		7.5		dB	CDMA Nom. Gain
		-5		dB	CDMA Min. Gain
Noise Figure		2.5		dB	FM and CDMA Max. Gain
		4.5		dB	CDMA Nom. Gain
		9.0		dB	CDMA Min. Gain
Input IP3		+7		dBm	FM and CDMA Max. Gain
		>+14		dBm	CDMA Nom. Gain
		>+20		dBm	CDMA Min. Gain
Input P1dB		-11		dBm	FM and CDMA Max. Gain
Reverse Isolation		25		dB	FM and CDMA Max. Gain
Input VSWR		<4:1			Internally matched for optimum noise figure from 50Ω source
Output VSWR		<1.5:1			With external match (partial)

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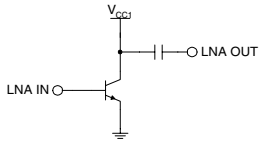
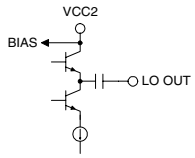
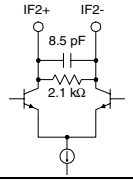
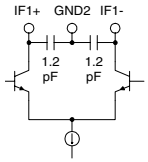
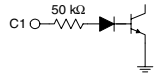
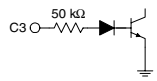
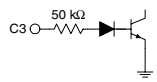
Second Section (Mixer, IF1 or IF2 Output)					
Conversion Gain		16		dB	IF 1, 1kΩ balanced load.
		7		dB	IF 2, 870Ω load.
Noise Figure		11.5		dB	Single sideband.
Input VSWR		<1.5:1			With external matching network
Input IP3 to IF1		+7		dBm	
Input IP3 to IF2		+7		dBm	
Input P1dB, IF2		-4		dBm	
Input P1dB, IF1		-8		dBm	
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
LO Input					
LO Input Range		-6 to 0		dBm	
LO Output Level		0		dBm	Buffer ON, 0dBm input
LO Output Level		-35		dBm	Buffer OFF, 0dBm input
LO IN to LNA Input Rejection		37		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			With external matching network
"Lazy" Mode					
Cascaded Perform. to IF1					1kΩ balanced load, 3.0dB Image Filter Loss. CDMA Max. Gain
Cascade Conversion Gain		21		dB	
Cascade Input IP3 to IF1		-8		dBm	
Cascade Noise Figure		4.1		dB	
Cascaded Perform. to IF2					870Ω load, 3dB Image Filter Loss. FM
Cascade Conversion Gain		15.3		dB	
Cascade Input IP3		-8		dBm	
Cascade Noise Figure		4.0		dB	
First Section (LNA)					
Gain		9.0		dB	FM and CDMA Max. Gain
		6.2		dB	CDMA Nom. Gain
		-5		dB	CDMA Min. Gain
Noise Figure		2.4		dB	FM and CDMA Max. Gain
		4.8		dB	CDMA Nom. Gain
		9.0		dB	CDMA Min. Gain
Input IP3		+1		dBm	FM and CDMA Max. Gain
		>+6		dBm	CDMA Nom. Gain
		>+20		dBm	CDMA Min. Gain
Input P1dB		-16		dBm	FM and CDMA Max. Gain
Reverse Isolation		25		dB	FM and CDMA Max. Gain
Input VSWR		<4:1			Internally matched for optimum noise figure from 50Ω source
Output VSWR		<1.5:1			With external match (partial)

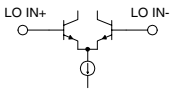
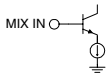
Second Section (Mixer, IF1 or IF2 Output)					
Conversion Gain		14		dB	IF 1, 1kΩ balanced load.
		5.5		dB	IF 2, 870Ω load.
Noise Figure		9.5		dB	Single sideband.
Input VSWR		<1.5:1			With external matching network
Input IP3 to IF1		+2		dBm	
Input IP3 to IF2		+2		dBm	
Input P1dB, IF2		-9		dBm	
Input P1dB, IF1		-6		dBm	
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
LO Input					
LO Input Range		-6 to 0		dBm	
LO Output Level		0		dBm	Buffer On, 0dBm input
LO Output Level		-35		dBm	Buffer Off, 0dBm input
LO IN to LNA Input Rejection		30		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			With external matching network

Mode Control Logic

MODE	C1	C2	C3	C4	PD
FM (IF2)	L	H	X	H	H
CDMA Max. Gain (IF1)	H	H	X	H	H
CDMA Nom. Gain (IF1)	H	L	X	H	H
CDMA Min. Gain (IF1)	L	L	X	H	H
Lazy FM (IF2)	L	H	X	L	H
Lazy CDMA Max. Gain (IF1)	H	H	X	L	H
Lazy CDMA Nom. Gain (IF1)	H	L	X	L	H
Lazy CDMA Min. Gain (IF1)	L	L	X	L	H
LO Buffer ON	X	X	H	X	H
LO Buffer OFF	X	X	L	X	X
Power Down	L	X	X	X	L

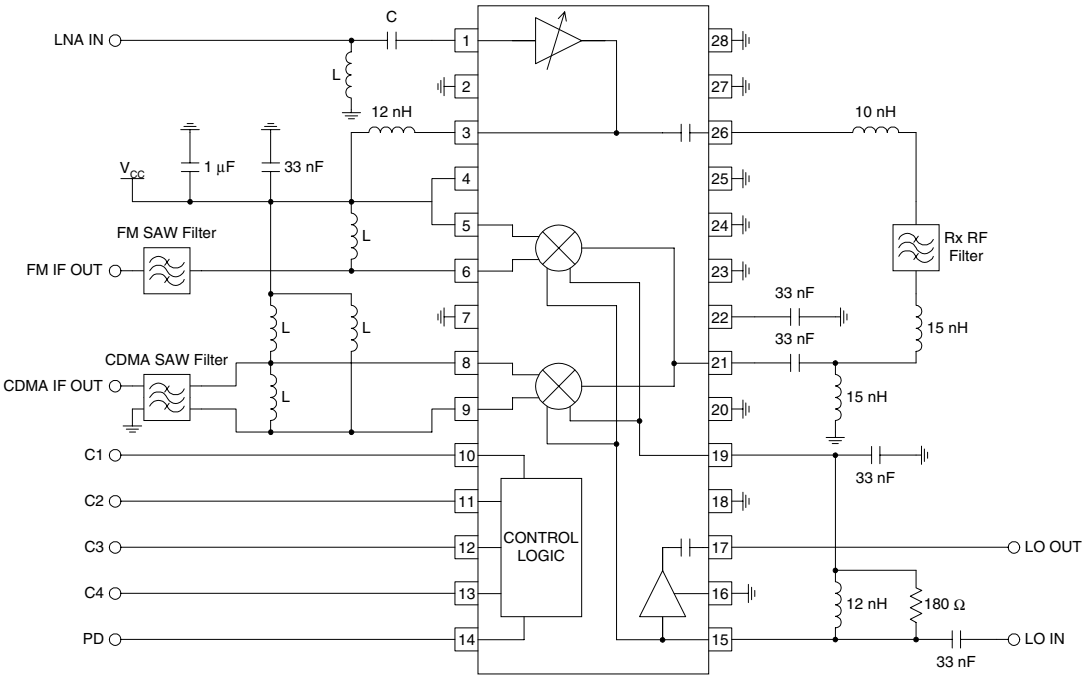
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Pin	Function	Description	Interface Schematic
1	LNA IN	RF Input pin. This pin is internally matched for optimum noise figure from a 50Ω source. This pin is internally DC biased and, if connected to a device with DC present, should be DC blocked with a capacitor suitable for the frequency of operation.	
2	GND1	Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VCC1	Supply Voltage for the LNA. External inductance, ~12nH, is required in addition to internal inductance to achieve optimum LNA performance. This extra inductance can be easily achieved with a thin microstrip line. The value of this inductance will change with the frequency of operation. RF and IF bypassing is required on the supply side of the inductance. The ground side of the bypass capacitors should connect immediately to ground plane.	See pin 1.
4	VCC2	Supply Voltage for the LO buffer amplifier, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	IF2-	Same as pin 6, except complementary output. For typical single ended operation, this pin is connected directly to V_{CC}.	See pin 6.
6	IF2+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85MHz. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
7	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
8	IF 1+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
9	IF 1-	Same as pin 8, except complementary output.	See pin 8.
10	C1	Control line for mode/gain select. See specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
11	C2	Control line for mode/gain select. See specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
12	C3	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" turns the buffer amplifier on, and the current consumption increases by 4mA (with 0dBm LO input). A logic "low" turns the buffer amplifier off. The threshold voltage is approximately 1.6V.	

13	**C4**	Enable pin for “Lazy Mode”. This is a digitally controlled input. A logic "high" maintains the part in full performance mode. A logic "low" places the part in a reduced-current/reduced performance mode. See the specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50µA when selected.	
14	**PD**	Power down pin. A logic “low” turns the part off. A logic “high” (>1.6V) turns the part on. In addition, pin 10 (C1) should also be taken low during power down.	
15	**LO IN+**	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 18 is bypassed to ground.	
16	**GND11**	Ground connection for LO buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
17	**LO OUT**	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 12.	See pin 4.
18	**GND9**	Die flag ground. Keep traces physically short and connect immediately to ground plane for best performance.	
19	**LO IN-**	Mixer LO bypass.	See pin 15.
20	**GND8**	Ground connection for the mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
21	**MIX IN**	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
22	**BYP**	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
23	**GND7**	Same as pin 2.	
24	**GND6**	Same as pin 2.	
25	**GND5**	Same as pin 2.	
26	**LNA OUT**	LNA Output pin. This pin is internally DC blocked and externally matched to 50Ω at pin 3 in order to facilitate an easy interface to a 50Ω Image Filter.	See pin 1.
27	**GND4**	Same as pin 25.	
28	**GND3**	Same as pin 25.	

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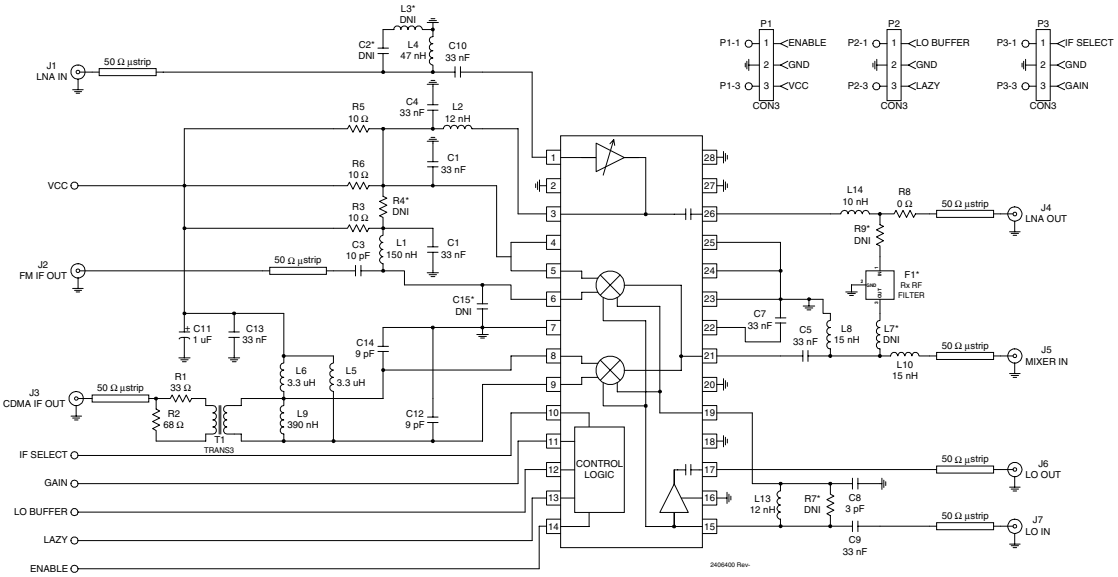
Application Schematic



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Evaluation Board Schematic

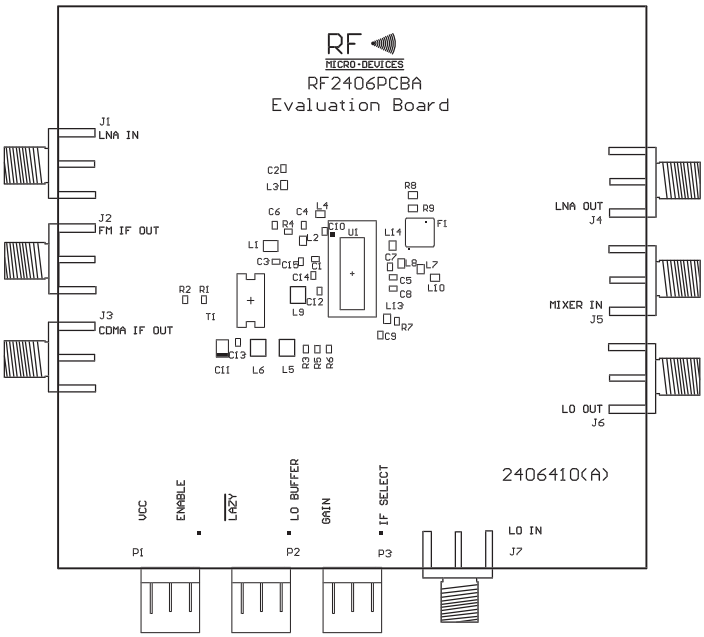
(Download Bill of Materials from www.rfmd.com.)

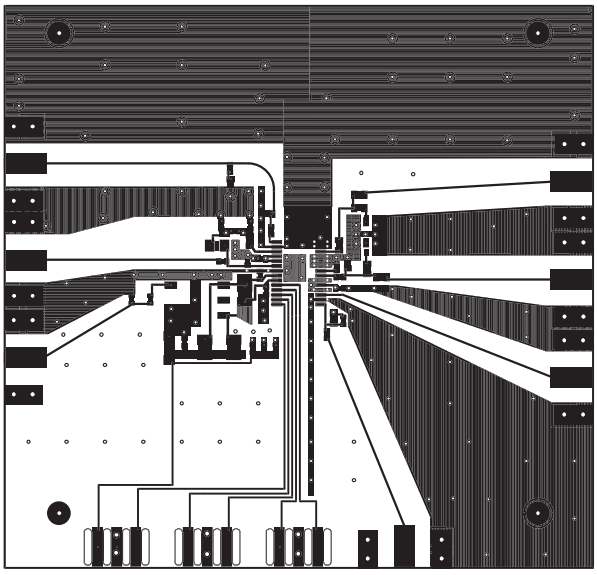


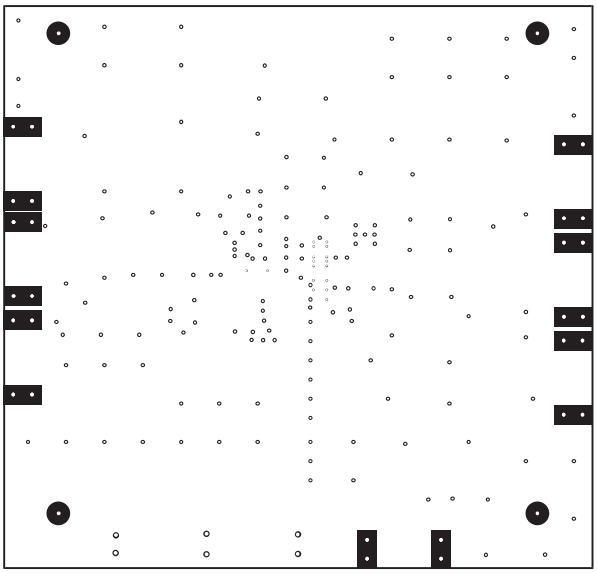
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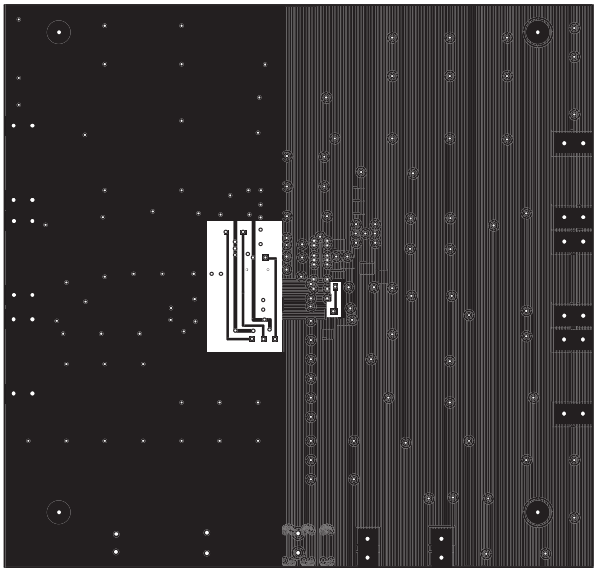
Evaluation Board Layout
Board Size 3.088" x 2.948"

Board Thickness 0.056”, Board Material FR-4, Multi-Layer









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RF2411

LOW NOISE AMPLIFIER/MIXER

Typical Applications

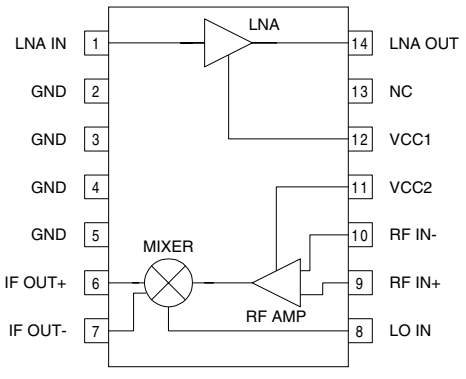
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

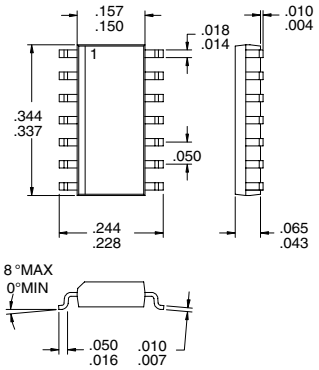
The RF2411 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, and a balanced mixer which can drive a single-ended or balanced load. The output of the LNA is made available as a pin to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA output is buffered to permit a wide range of choices for the interstage filter without altering the VSWR or noise figure at the LNA input and to provide high isolation from the LO to the input port. The LNA section may be disabled to conserve power.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Single 3V to 6.5V Power Supply
- 500MHz to 1900MHz Operation
- 25dB Small Signal Gain
- 2.5dB Cascaded Noise Figure
- 8.5mA DC Current Consumption
- -8dBm Input IP_3

Ordering Information

RF2411	Low Noise Amplifier/Mixer
RF2411 PCBA-L	Fully Assembled Evaluation Board (850MHz)
RF2411 PCBA-H	Fully Assembled Evaluation Board (1800MHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

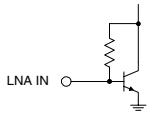
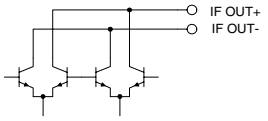
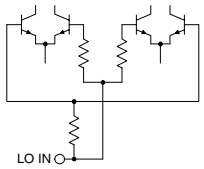
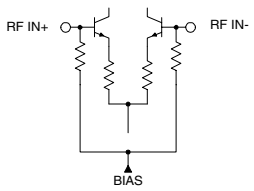
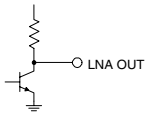
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter (850MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=850MHz, LO=0dBm, IF=50MHz, Application Schematic 2 configuration
RF Frequency Range		500 to 1900		MHz	
IF Frequency Range		DC to 150		MHz	
Cascade Gain		27		dB	IF=10MHz
	21	25	29		IF=50MHz
		20			IF=150MHz
Cascade IP3		-8		dBm	Referenced to the input
Cascade Noise Figure		2.4		dB	Single sideband, IF=10MHz
		2.4			Single sideband, IF=50MHz
		3.4			Single sideband, IF=150MHz
First Section (LNA)					
Noise Figure		1.6		dB	
Input VSWR		1.5:1			
Input IP3		-3.5		dBm	
Gain		14		dB	
Reverse Isolation		30		dB	
Output VSWR		2.0:1			
Second Section (RF Amp, Mixer, IF1)					
Noise Figure		11.0		dB	Single Sideband
Input VSWR		2.0:1			
Input IP3		+6		dBm	
Conversion Gain		11		dB	
Output Impedance		4		kΩ	Open Collector
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		30		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.5:1			
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		8		mA	V_{CC}=3.0V
		20		mA	V_{CC}=5.0V

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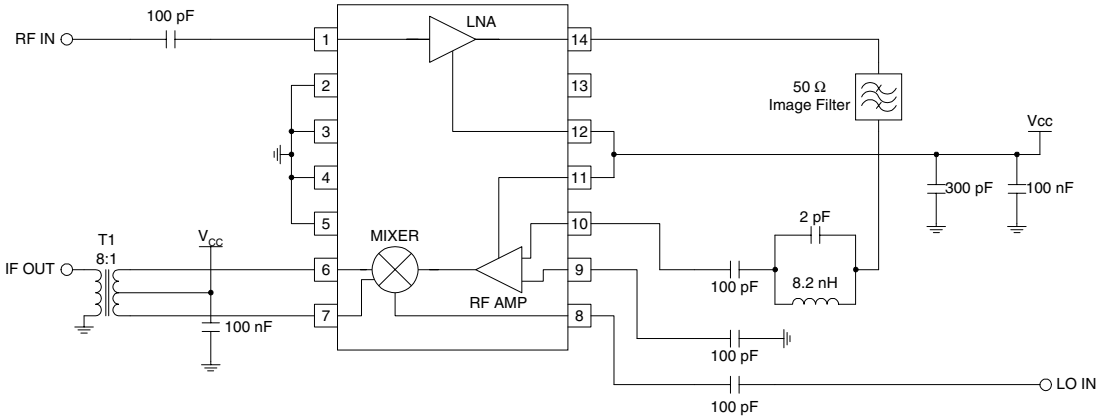
Parameter (1800MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=1800MHz, LO=0dBm, IF=50MHz, Application Schematic 2 configuration
RF Frequency Range		500 to 1900		MHz	
IF Frequency Range		DC to 100		MHz	
Cascade Gain		22		dB	IF=10MHz
		21			IF=50MHz
		17			IF=150MHz
Cascade IP3		-7		dBm	Referenced to the input
Cascade Noise Figure		4.0		dB	Single sideband, IF=10MHz
		4.0			Single sideband, IF=50MHz
		4.8			Single sideband, IF=150MHz
First Section (LNA)					
Noise Figure		2.6		dB	
Input VSWR		1.2:1			
Input IP3		-3.5		dBm	
Gain		10		dB	
Reverse Isolation		25		dB	
Output VSWR		1.5:1			
Second Section (RF Amp, Mixer, IF1)					
Noise Figure		10.0		dB	Single Sideband
Input VSWR		2.0:1			
Input IP3		+3		dBm	
Conversion Gain		11		dB	
Output Impedance		4		kΩ	Open Collector
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		30		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.2:1			

RF2411

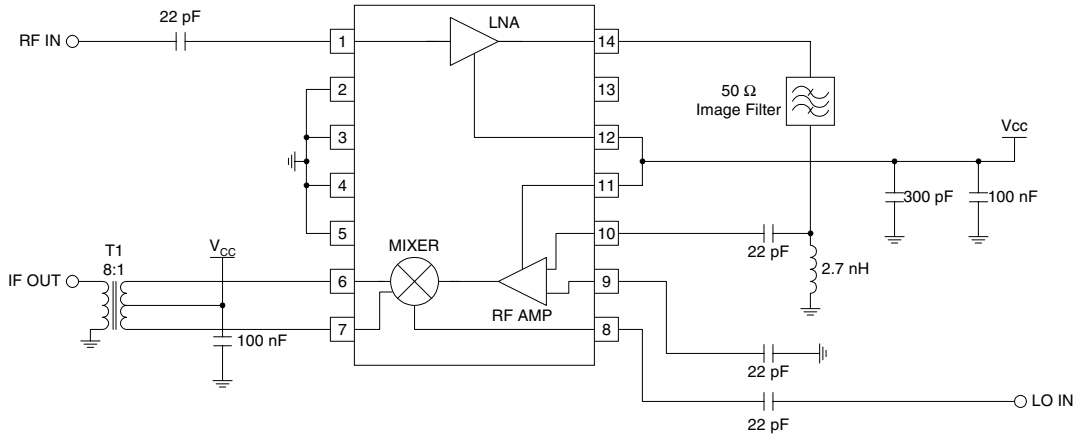
Pin	Function	Description	Interface Schematic
1	LNA IN	This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	IF OUT+	Balanced open collector output of the mixer. External bias needs to be supplied to this pin. This can be done with a resistor to V_{CC} (see application schematic 1), with a Bolan (see application schematic 2) or when used in a single-ended configuration by connecting directly to V_{CC} (see application schematic 3). When using a resistor to V_{CC} the resistor value will set the output impedance. Typical values for this resistor are 200Ω to 1kΩ. A shunt inductor/capacitor resonator to V_{CC} is needed to maintain proper DC voltage at the mixer. At low resistor values the resonator may be omitted at the expense of gain, output power and IP3. To obtain maximum gain and output power a Bolan as shown in application schematics 2 and 4 is recommended. Using both outputs and matching them correctly to a single ended load will result in a 6dB gain improvement over the plain single ended configuration.	
7	IF OUT-	Same as pin 6 except complementary output.	See pin 6.
8	LO IN	50Ω mixer LO input. This pin has an internal pull-up resistor to V_{CC} and is not DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz.	
9	RF IN+	Balanced mixer RF Input port. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz. Matching is required; see the applications schematics. To minimize the noise figure it is recommended to have a bandpass filter before this input. This will prevent noise at the image frequency from being converted to the IF.	
10	RF IN-	Same as pin 9 except complementary input.	See pin 9.
11	VCC2	Supply voltage for the mixer bias circuits.	
12	VCC1	Supply Voltage for the LNA only. A 47pF external bypass capacitor is required and an optional 0.01µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
13	NC	No connection.	
14	LNA OUT	50Ω output. An external DC blocking capacitor is required when this pin is connected to a DC path.	

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Application Schematic
850MHz, Output Matching with Balun



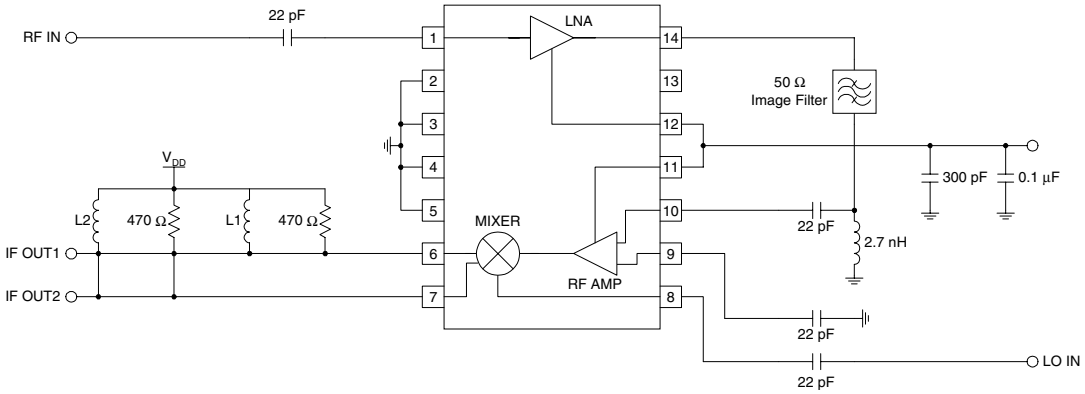
Application Schematic
1800MHz, Output Matching with Balun



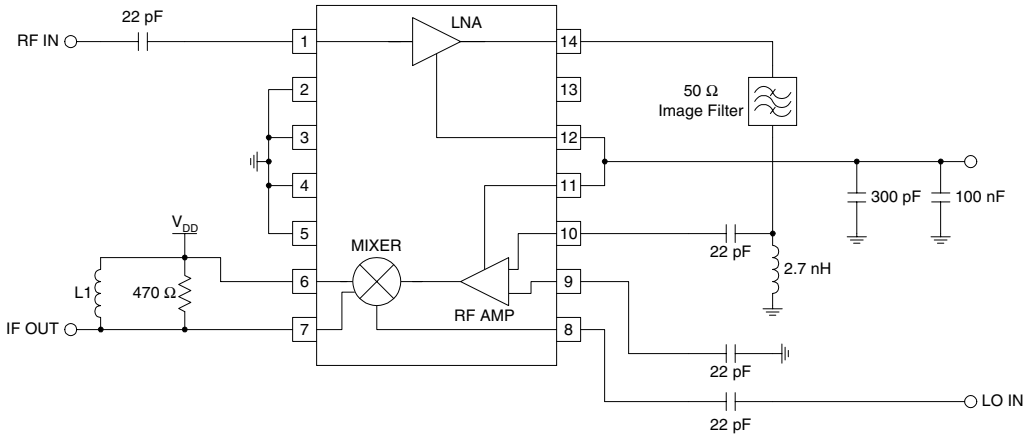
8

FRONT-ENDS

Application Schematic
1800MHz, Balanced Resistive Output Matching



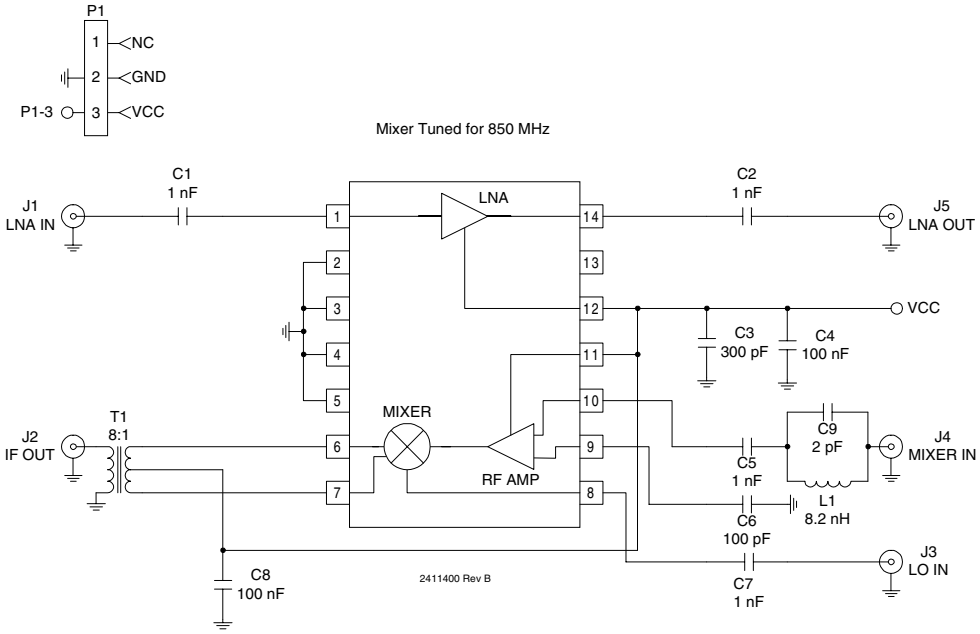
Application Schematic
1800MHz, Single-Ended Resistive Output Matching

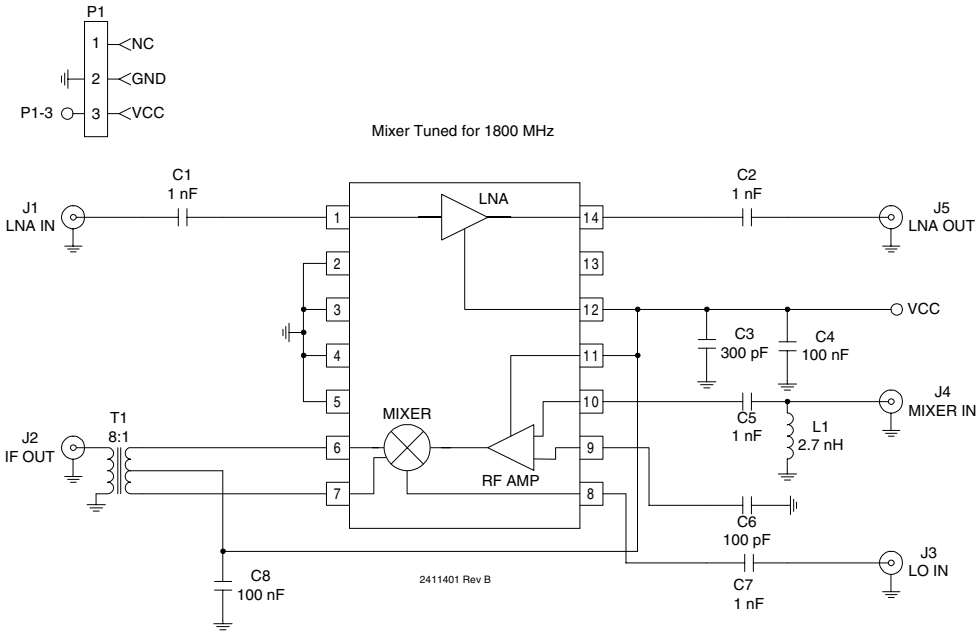


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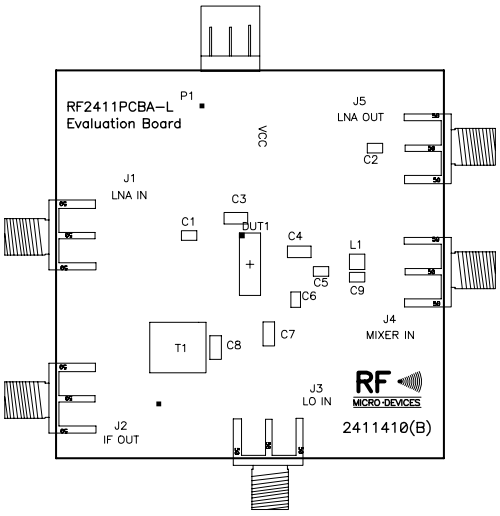
Evaluation Board Schematics

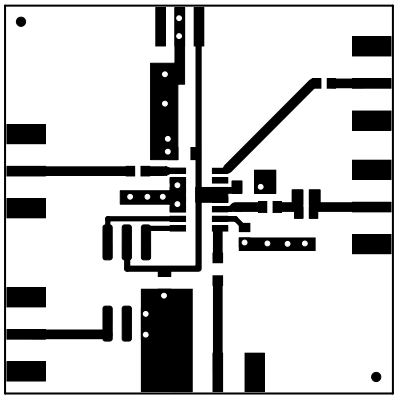
(Download Bill of Materials from www.rfmd.com.)





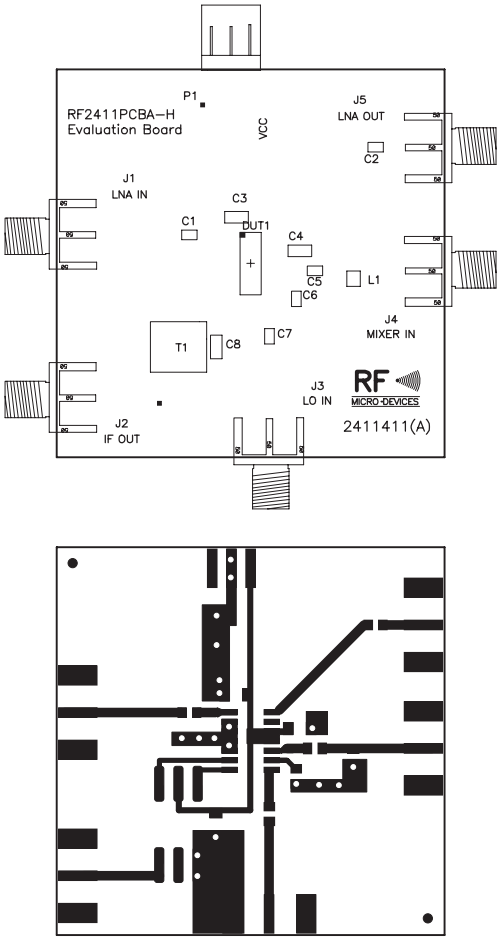
Evaluation Board Layout 850MHz
Board Size 2.0” x 2.0”

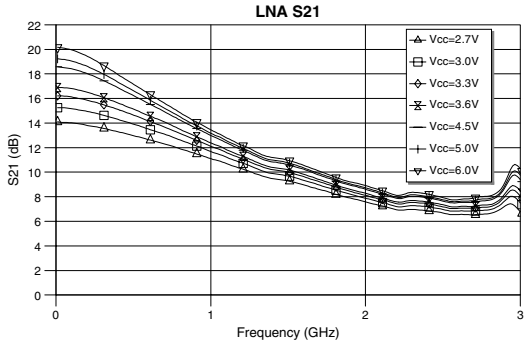


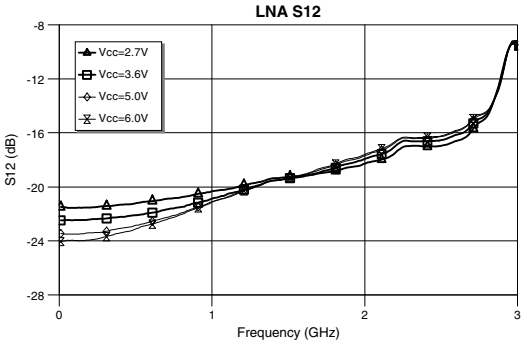


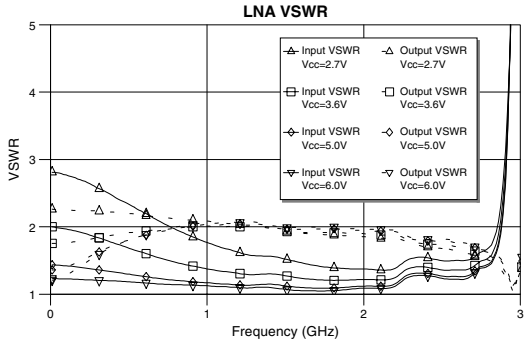
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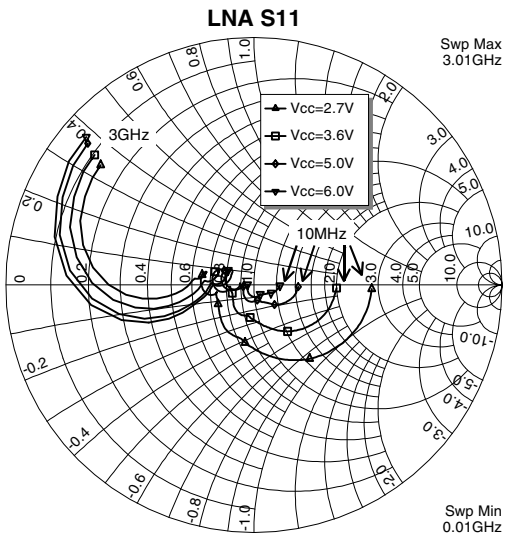
Evaluation Board Layout 1800MHz
Board Size 2.0” x 2.0”

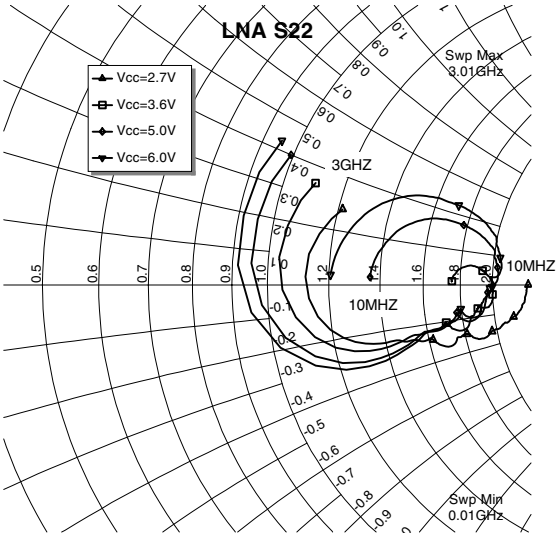



LNA S21
S21 (dB)
Frequency (GHz)
Vcc=2.7V
Vcc=3.0V
Vcc=3.3V
Vcc=3.6V
Vcc=4.5V
Vcc=5.0V
Vcc=6.0V


LNA S12
S12 (dB)
Frequency (GHz)
Vcc=2.7V
Vcc=3.6V
Vcc=5.0V
Vcc=6.0V


LNA VSWR
VSWR
Frequency (GHz)
Input VSWR Vcc=2.7V
Output VSWR Vcc=2.7V
Input VSWR Vcc=3.6V
Output VSWR Vcc=3.6V
Input VSWR Vcc=5.0V
Output VSWR Vcc=5.0V
Input VSWR Vcc=6.0V
Output VSWR Vcc=6.0V


LNA S11
Swp Max
3.01GHz
Swp Min
0.01GHz
3GHz
10MHz
Vcc=2.7V
Vcc=3.6V
Vcc=5.0V
Vcc=6.0V

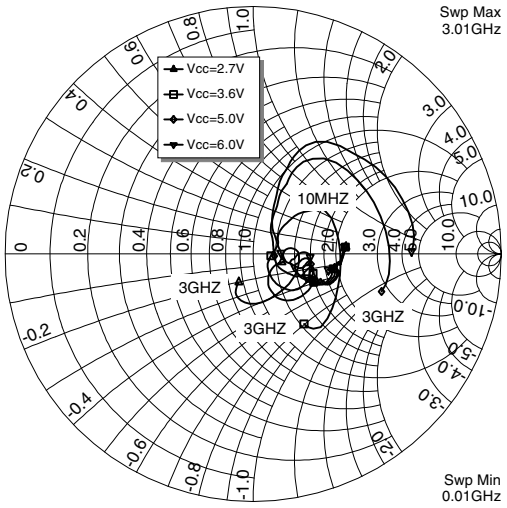

LNA S22
Swp Max
3.01GHz
Swp Min
0.01GHz
3GHZ
10MHZ
10MHZ
Vcc=2.7V
Vcc=3.6V
Vcc=5.0V
Vcc=6.0V

8

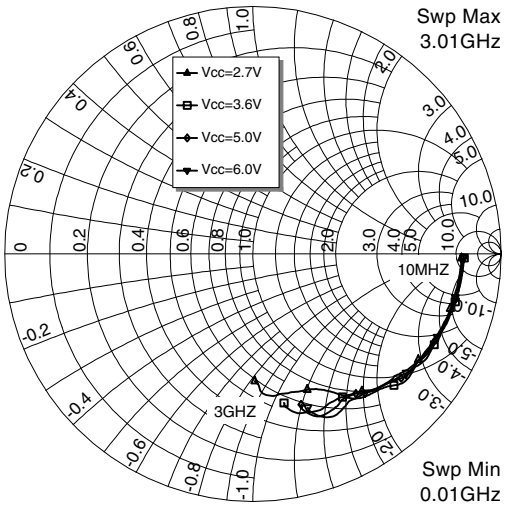
FRONT-ENDS

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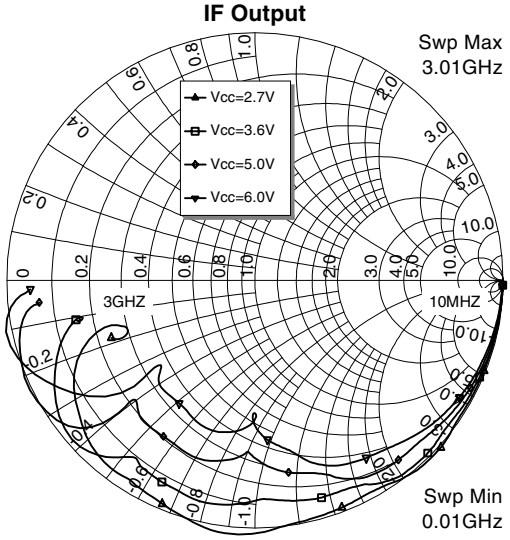
LO Input



RF Input (single ended)



IF Output



8

FRONT-ENDS

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RF2418

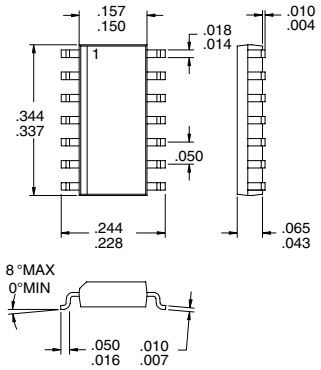
LOW CURRENT LNA/MIXER

Typical Applications

- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- 433MHz and 915MHz ISM Band Receivers
- General Purpose Frequency Conversion

Product Description

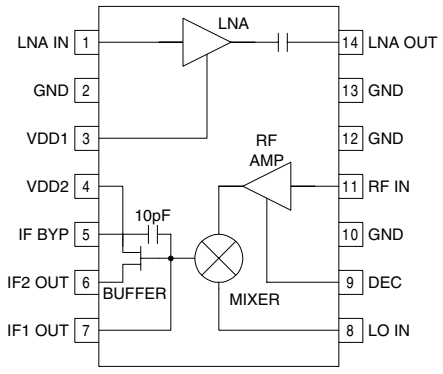
The RF2418 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, a dual-gate GaAs FET mixer, and an IF output buffer amplifier which will drive a 50Ω load. In addition, the IF buffer amplifier may be disabled and a high impedance output is provided for easy matching to IF filters with high impedances. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA section may be disabled by removing the VDD1 connection to the IC.



Package Style: SOP-14

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V to 6.5V Power Supply
- High Dynamic Range
- Low Current Drain
- High LO Isolation
- LNA Power Down Mode for Large Signals

Ordering Information

RF2418	Low Current LNA/Mixer
RF2418 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2418

Absolute Maximum Ratings

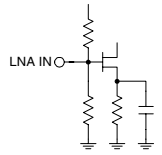
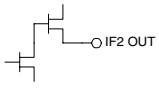
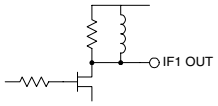
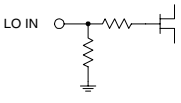
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

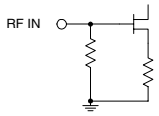
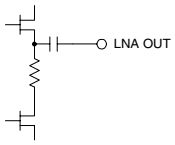
Caution! ESD sensitive device.

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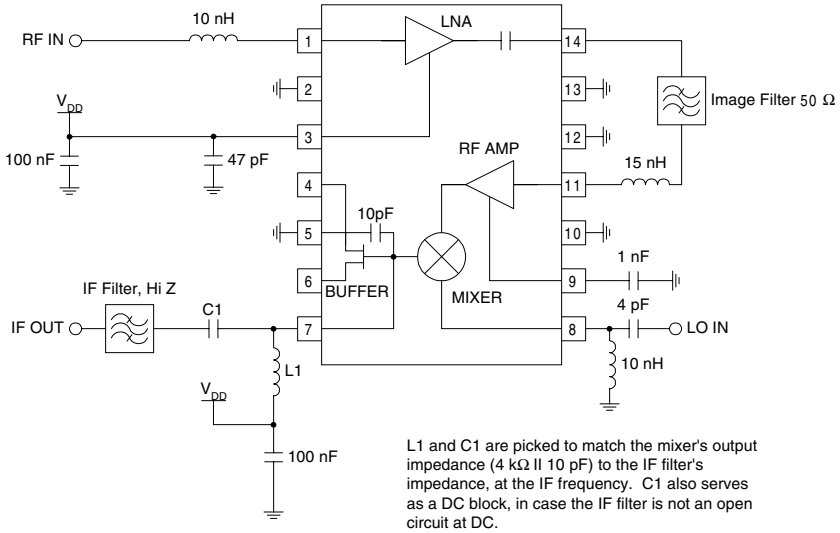
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=900MHz, LO=971MHz
RF Frequency Range		400 to 1100		MHz	
Cascade Power Gain		30		dB	High impedance output
Cascade IP_3		-13		dBm	Referenced to the input
Cascade Noise Figure		2.4		dB	Single sideband, includes image filter with 1.0dB insertion loss
First Section (LNA)					
Noise Figure		1.8		dB	
Input VSWR		1.5:1			With external series matching inductor
Input IP_3		+4		dBm	
Gain		14		dB	
Reverse Isolation		40		dB	
Output VSWR		1.5:1			
Second Section (RF Amp, Mixer, IF1)					High impedance output
Noise Figure		9.5		dB	Single Sideband
Input VSWR		1.5:1			With external series matching inductor
Input IP_3		+1		dBm	
Conversion Power Gain		9		dB	
Output Impedance		4000‖10pF		Ω	Open Collector
Second Section (RF Amp, Mixer, IF2)					Buffered output, 50Ω load
Noise Figure		10		dB	Single Sideband
Input VSWR		1.5:1			With external series matching inductor
Input IP_3		0		dBm	
Conversion Gain		6		dB	
Output Impedance		30		Ω	
LO Input					
LO Frequency		300 to 1200		MHz	
LO Level		-6 to +6		dBm	
LO to RF Rejection		15		dB	
LO to IF Rejection		40		dB	With pin 5 connected to ground.
LO Input VSWR		1.3:1			In order to achieve a low VSWR match at this input, an 82Ω resistor to ground is placed in parallel with this port.
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		14		mA	V_{CC}=5.0V, LNA On, Mixer On, Buffer Off
		20		mA	V_{CC}=5.0V, LNA On, Mixer On, Buffer On
		9		mA	V_{CC}=5.0V, LNA Off, Mixer On, Buffer Off

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Pin	Function	Description	Interface Schematic
1	LNA IN	A series 10nH matching inductor is necessary to achieve specified gain and noise figure at 900MHz. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VDD1	Supply Voltage for the LNA only. A 22pF external bypass capacitor is required and an additional 0.01µF is required if no other low frequency bypass capacitors are near by. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. For large input signals, VDD1 may be disconnected, resulting in the LNA's gain changing from +11dB to -26dB and current drain decreasing by 4mA. If the LNA is never required for use, then this pin can be left unconnected or grounded, and Pin 11 is used as the first input.	
4	VDD2	Power supply for the IF buffer amplifier. If the high impedance mixer output is being used, then this pin is not connected.	
5	IF BYP	If this pin is connected to ground, an internal 10pF capacitor is connected in parallel with the mixer output. This capacitor functions as an LO trap, which reduces the amount of LO to IF bleed-through and prevents high LO voltages at the mixer output from degrading the mixer's dynamic range. At higher IF frequencies, this capacitance, along with parasitic layout capacitance, should be parallel resonated out by the choice of the bias inductor value at pin 7. If the internal capacitor is not connected to ground, the buffer amplifier could become unstable. A ~10pF capacitor should be added at the output to maintain the buffer's stability, but the gain will not be significantly affected.	
6	IF2 OUT	50Ω buffered (open source) output port, one of two output options. Pin 7 must have a bias resistor to V_{DD} and pin 6 must have a bias resistor to ground (see Buffered Output Application Schematic) in order to turn the buffer amplifier on. Current drain will increase by approximately 8mA at 5V, and by approximately 5mA at 3V. It is recommended that these bias resistors be less than 1kΩ.	
7	IF1 OUT	High impedance (open drain) output port, one of two output options. This pin must be connected to V_{DD} through a resistor or inductor in order to bias the mixer, even when using IF2 Output. In addition, a 0.01µF bypass capacitor is required at the other end of the bias resistor or inductor. The ground side of the bypass capacitor should connect immediately to ground plane. This output is intended to drive high impedance IF filters. The recommended matching network is shunt L, series C (see the application schematic, high impedance output). This topology will provide matching, bias, and DC blocking.	
8	LO IN	Mixer LO input. A high-pass matching network, such as a single shunt inductor (as shown in the application schematics), is the recommended topology because it also rejects IF noise at the mixer input. This filtering is required to achieve the specified noise figures. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
9	RF BYP	Connection for the external bypass capacitor for the mixer RF input preamp. 1000pF is recommended. The trace length between the pin and the capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
10	GND	Same as pin 2.	

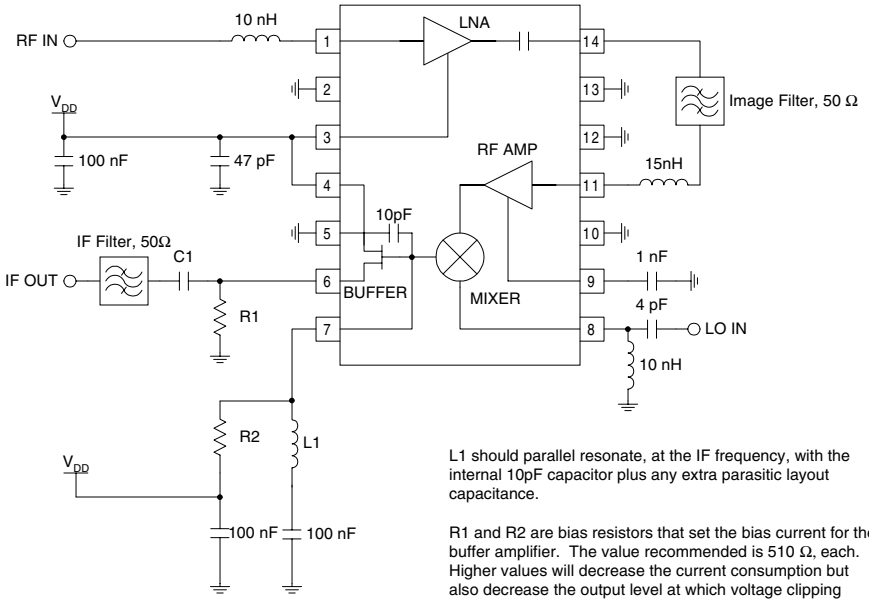
11	**RF IN**	Mixer RF Input port. For a 50Ω match at 900MHz use a 15nH series inductor. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.To minimize the mixer's noise figure, it is recommended to have a RF bandpass filter before this input. This will prevent the noise at the image frequency from being converted to the IF.	
12	**GND**	Same as pin 2.	
13	**GND**	Same as pin 2.	
14	**LNA OUT**	50Ω output. Internally DC Blocked.	

Application Schematic
High Impedance Output Configuration
915MHz



L1 and C1 are picked to match the mixer's output impedance (4 kΩ II 10 pF) to the IF filter's impedance, at the IF frequency. C1 also serves as a DC block, in case the IF filter is not an open circuit at DC.

Applications Schematic
Buffered Output Configuration
915MHz



L1 should parallel resonate, at the IF frequency, with the internal 10pF capacitor plus any extra parasitic layout capacitance.

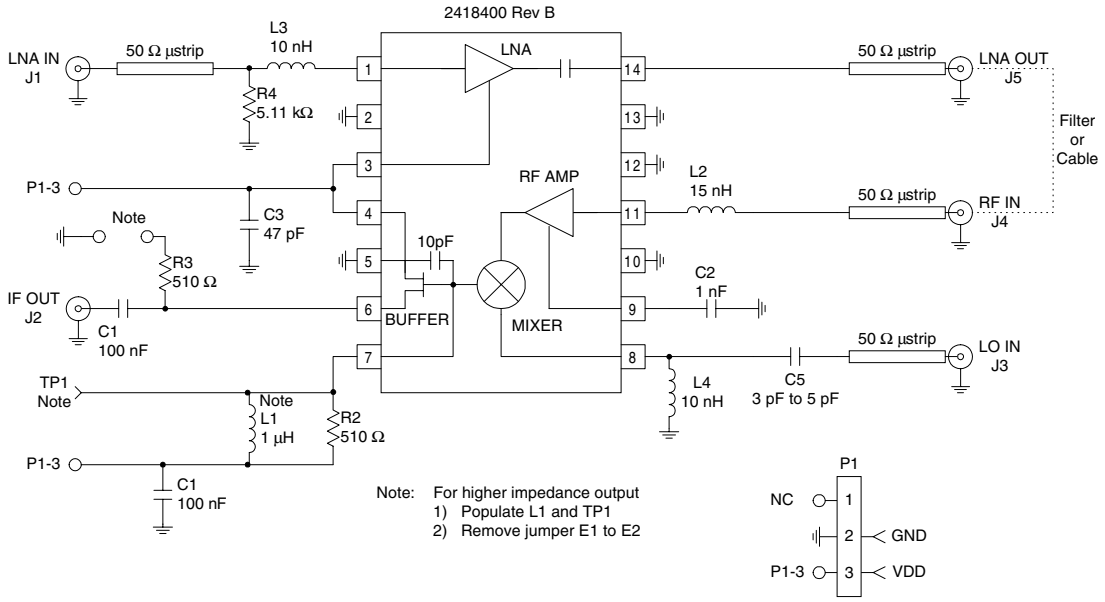
R1 and R2 are bias resistors that set the bias current for the buffer amplifier. The value recommended is 510 Ω, each. Higher values will decrease the current consumption but also decrease the output level at which voltage clipping begins to occur. At lower IF frequencies, where the internal 10 pF capacitor does not roll off the conversion gain, L1 may be eliminated.

C1 is a blocking capacitor, in case the IF filter's input is not an open circuit at DC.

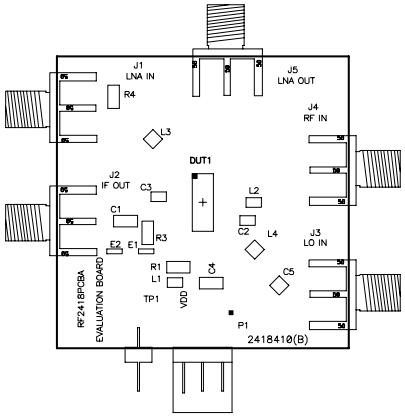
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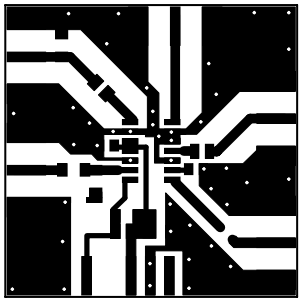
Evaluation Board Schematic
915MHz

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout





RF2418

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RF2431

HIGH FREQUENCY LNA/MIXER

Typical Applications

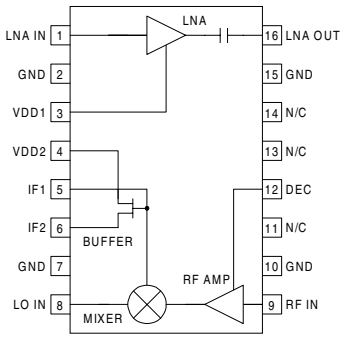
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

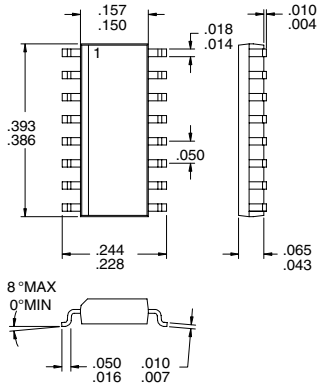
The RF2431 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, a dual-gate GaAs FET mixer, and an IF output buffer amplifier which will drive a 50Ω load. Alternatively, the IF output may be matched to a higher impedance at significantly reduced current. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA output is buffered to permit a wide range of choices for the interstage filter without altering the VSWR or noise figure at the LNA input and to provide high isolation from the LO to the input port.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-16

Features

- Single 3V to 6.5V Power Supply
- 1500MHz to 2500MHz Operation
- 23dB Small Signal Gain
- 3.5dB Cascaded Noise Figure
- 13mA DC Current Consumption
- -14dBm Input IP_3

Ordering Information

RF2431	High Frequency LNA/Mixer
RF2431 PCBA-L	Fully Assembled Evaluation Board (1.8GHz)
RF2431 PCBA-H	Fully Assembled Evaluation Board (2.5GHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

RF2431

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

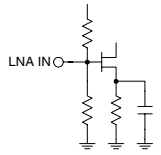
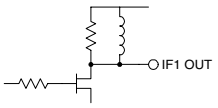
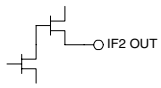
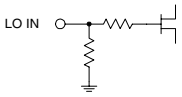
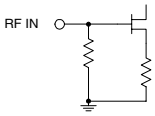
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

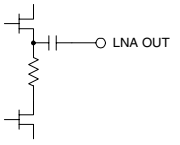
Parameter (1800MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=1800MHz, LO=0dBm
RF Frequency Range		1500 to 2500		MHz	
IF Frequency Range		DC to 400		MHz	
Cascade Gain		23		dB	IF=100MHz, 50Ω load
	15	19		dB	IF=350MHz, 50Ω load
Cascade IP3		-14		dBm	Referenced to the input
Cascade Noise Figure		3.5		dB	Single sideband
First Section (LNA)					
Noise Figure		2.6		dB	
Input VSWR		2.5:1			No external matching
Input IP3		+2		dBm	
Gain		13		dB	
Reverse Isolation		30		dB	
Output VSWR		1.5:1			No external matching
Second Section (RF Amp, Mixer, IF1)					High impedance output, 1.3kΩ load
Noise Figure		9.5		dB	Single sideband
Input VSWR		1.7:1			
Input IP3		-1		dBm	
Conversion Gain		6		dB	
Output Impedance		4		kΩ	Open drain
Second Section (RF Amp, Mixer, IF2)					Buffered output, 50Ω load
Noise Figure		9.5		dB	Single sideband
Input VSWR		1.7:1			
Input IP3		-1		dBm	
Conversion Gain		6		dB	
Output VSWR		1.2:1			
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		15		dB	
LO to IF Rejection		25		dB	
LO Input VSWR		1.5:1			
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		19	25	mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer On
		13		mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer Off

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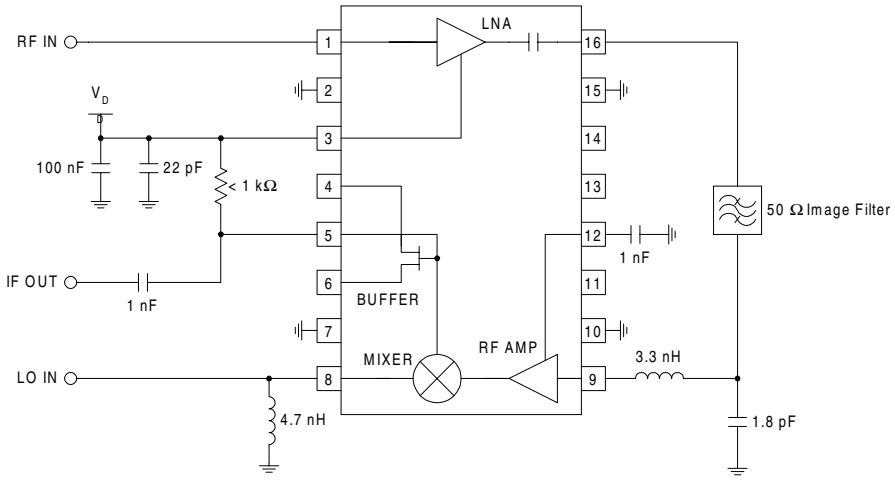
Parameter (2400MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=2400MHz, LO=0dBm
RF Frequency Range		2.0 to 2.5		GHz	
IF Frequency Range		DC to 400		MHz	
Cascade Gain		13		dB	IF=100MHz, 50Ω load
		10		dB	IF=350MHz, 50Ω load
Cascade IP_3		-11		dBm	Referenced to the input
Cascade Noise Figure		4.5		dB	Single sideband
First Section (LNA)					
Noise Figure		2.9		dB	
Input VSWR		1.8:1			No external matching
Input IP3		0		dBm	
Gain		10		dB	
Reverse Isolation		25		dB	
Output VSWR		1.6:1			No external matching
Second Section (RF Amp, Mixer, IF1)					High impedance output, 1.3kΩ load
Noise Figure		10		dB	Single sideband
Input VSWR		1.5:1			
Input IP_3		-1		dBm	
Conversion Gain		3		dB	
Output Impedance		4		kΩ	Open drain
Second Section (RF Amp, Mixer, IF2)					Buffered output, 50Ω load
Noise Figure		10		dB	Single sideband
Input VSWR		1.5:1			
Input IP_3		-1		dBm	
Conversion Gain		3		dB	
Output VSWR		1.2:1			
LO Input					
LO Level		-6 to +6		dBm	
LO to RF Rejection		15		dB	
LO to IF Rejection		20		dB	
LO Input VSWR		1.4:1			
Power Supply					
Voltage		3 to 6.5		V	
Current Consumption		19		mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer On
		13		mA	V_{DD}=5.0V, LNA On, Mixer On, Buffer Off

RF2431

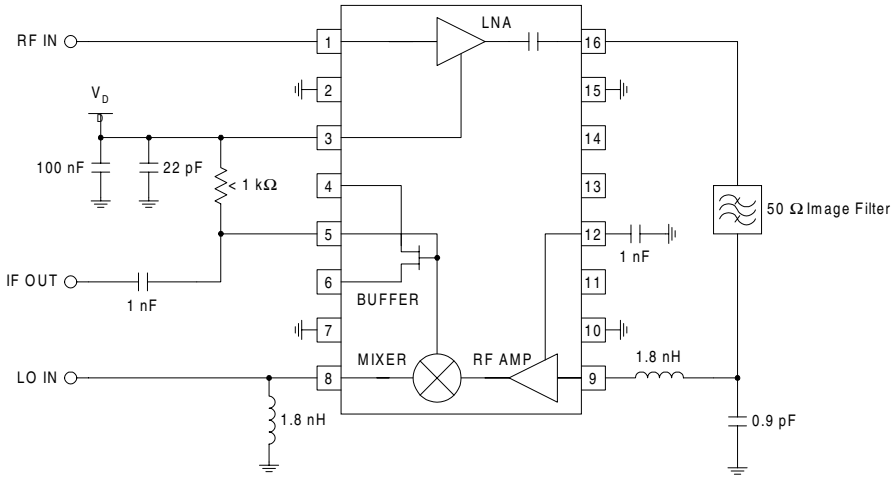
Pin	Function	Description	Interface Schematic
1	LNA IN	This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VDD1	Supply voltage for the LNA only. A 22pF external bypass capacitor is required and an additional 0.01µF is required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
4	VDD2	Power supply for the IF buffer amplifier. If the high impedance mixer output is being used, then this pin is not connected.	
5	IF1 OUT	Open drain output port, one of the two output options. This pin must be connected to V_{DD} through a resistor in order to bias the mixer, even when using the IF2 Output. In addition, a 0.1µF bypass capacitor is required at the other end of the bias resistor. This output is intended to drive high impedance IF filters. The intrinsic output impedance is about 4kΩ, which means that the actual impedance is set by the external resistor to V_{DD}.	
6	IF2 OUT	50Ω buffered output port, one of the two output options. This is an open drain output, therefore a resistor to ground is needed. The typical value for this resistor is 470Ω. Pin 4 must be connected to V_{DD} in order to turn the buffer amplifier on. Current drain will increase by approximately 6mA at 5V; by approximately 3mA at 3V.This pin is not connected when using the high impedance port.	
7	GND	Same as pin 2.	
8	LO IN	Mixer LO input. An high-pass matching network, such as a single shunt inductor (as shown in the application schematics), is the recommended topology because it also rejects IF noise at the mixer input. The value of this inductor is depending on the frequency, see the application schematics. This filtering is required to achieve the specified noise figures. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
9	RF IN+	Mixer RF Input port. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended. Matching is required; see the applications schematics.To minimize the noise figure it is recommended to have a bandpass filter before this input. This will prevent the noise at the image frequency from being converted to the IF.	
10	GND	Same as pin 2.	
11	NC	No connection	
12	RF BYP	Connection for the external bypass capacitor for the mixer input buffer amplifier. 1nF is recommended. The trace length between the pin and the capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
13	NC	No connection.	
14	NC	No connection.	
15	GND	Same as pin 2.	

16	LNA OUT	50Ω output. Internally DC blocked.	

Application Schematic
1800MHz, High Impedance Output



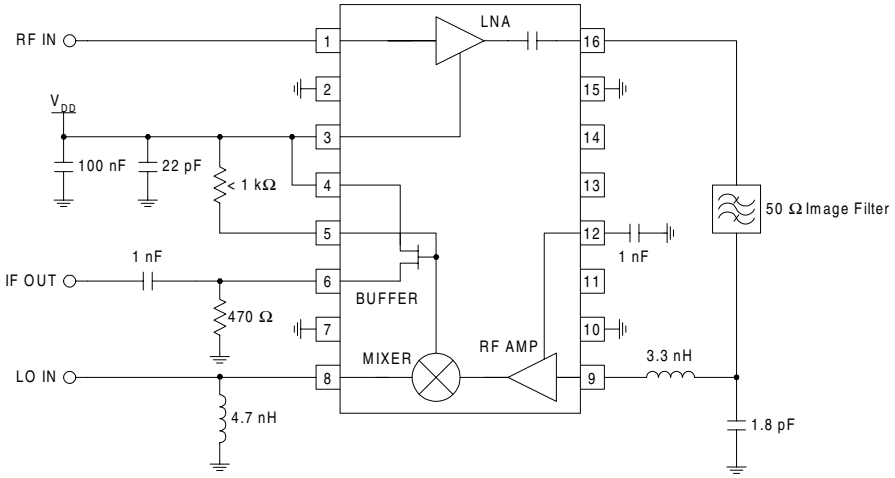
Application Schematic
2400MHz, High Impedance Output



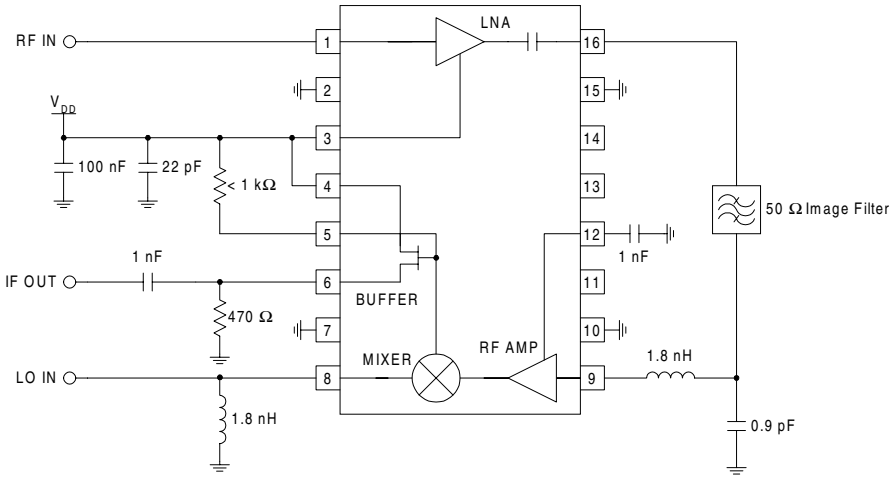
8

FRONT-ENDS

Application Schematic
1800MHz, Buffered Output

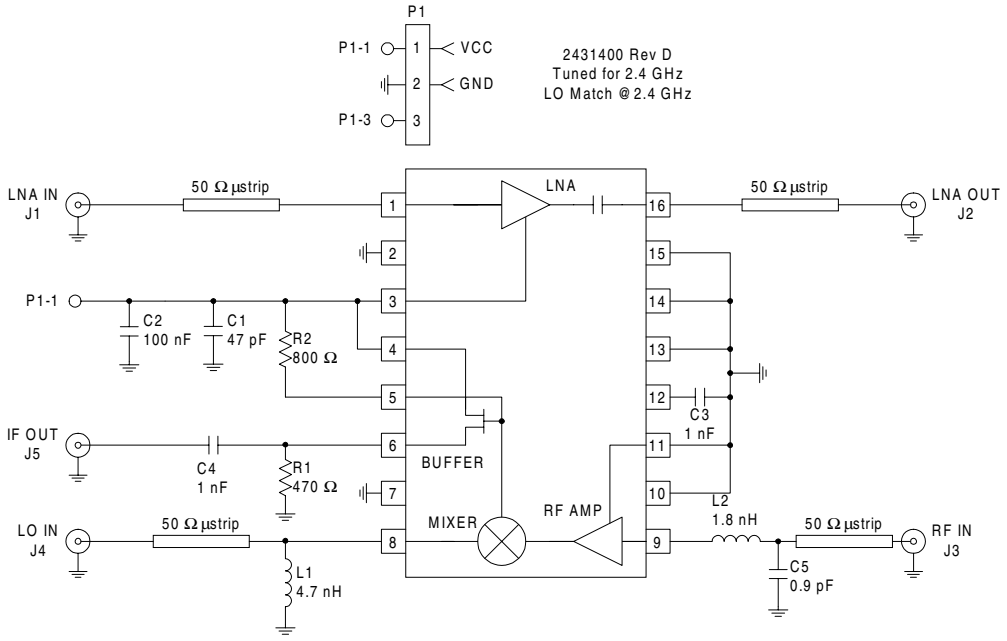


Application Schematic
2400MHz, Buffered Output



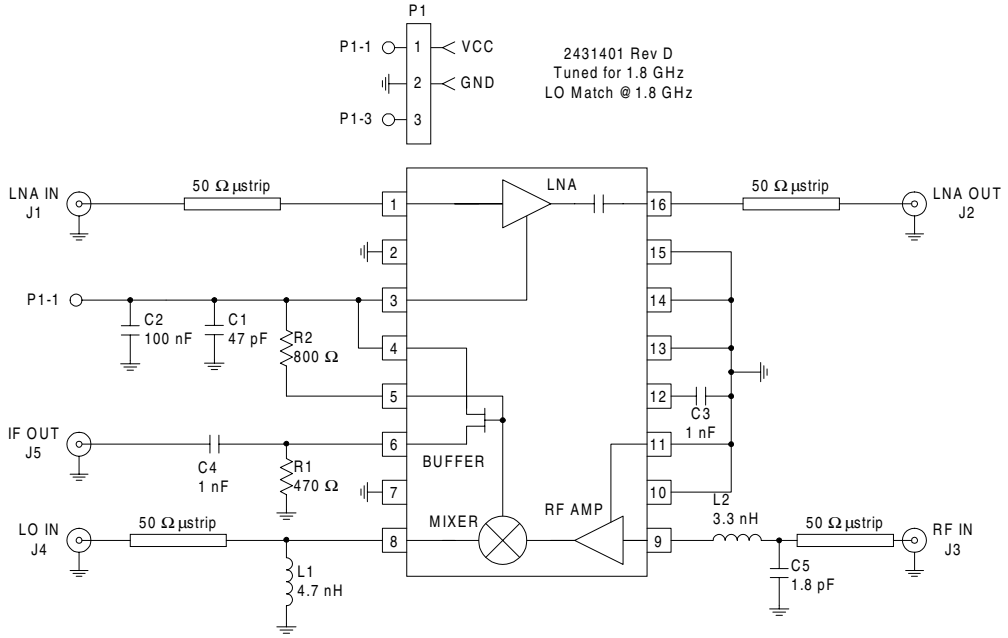
Evaluation Board Schematic
2400MHz

(Download Bill of Materials from www.rfmd.com.)



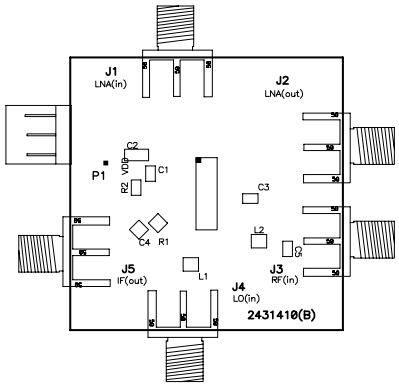
Evaluation Board Schematic
1800MHz

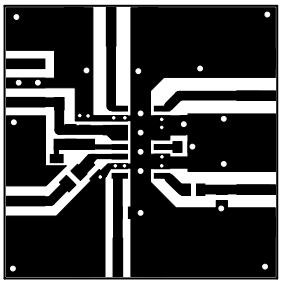
(Download Bill of Materials from www.rfmd.com.)



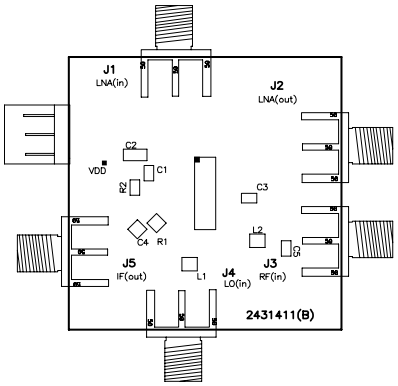
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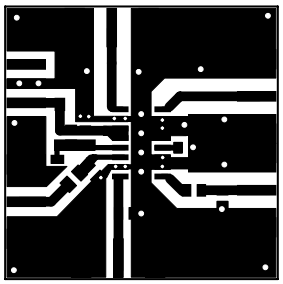
Evaluation Board Layout
2400MHz





Evaluation Board Layout
1800MHz





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RF MICRO·DEVICES

Preliminary

RF2444

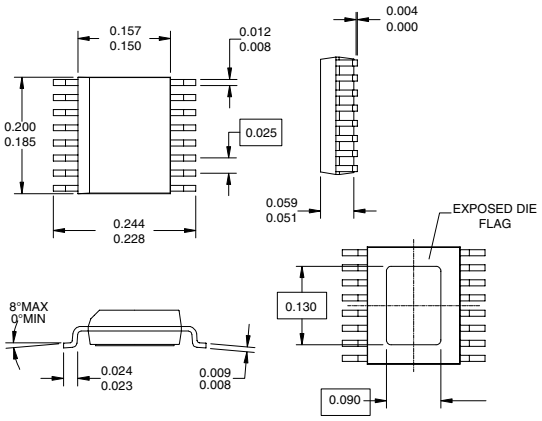
HIGH FREQUENCY LNA/MIXER

Typical Applications

- WLAN or Wireless Local Loop
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Part of 2.4GHz Chip Set
- Portable Battery Powered Equipment
- UHF Digital and Analog Receivers

Product Description

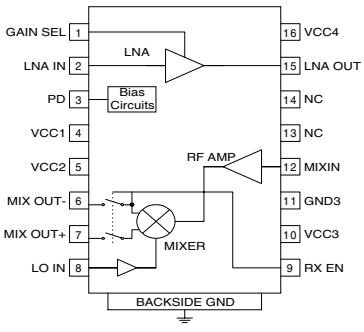
The RF2444 is a monolithic integrated UHF receiver front end suitable for 2.4GHz ISM band applications. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier and a doubly balanced mixer. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The mixer outputs can be selectively disabled to allow for the IF filter to be used in the transmit mode.



Package Style: SSOP-16 EPP

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2.7V to 3.6V Power Supply
- 2400MHz to 2500MHz Operation
- Two Gain Settings: 28dB or 12dB
- 4.5dB Cascaded NF, High Gain Mode
- 20mA DC Current Consumption
- Input IP_3: -23dBm or -8dBm

Ordering Information

RF2444	High Frequency LNA/Mixer
RF2444 PCBA-H	Fully Assembled Evaluation Board (2.5GHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 3.6	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC Level 5	

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

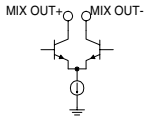
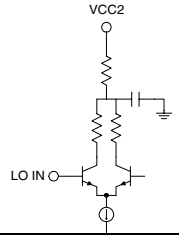
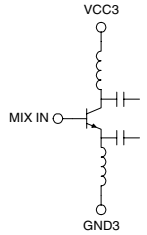
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

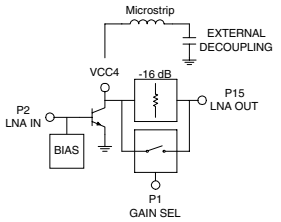
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.3V, RF=2400 MHz, LO=2120 MHz, -10 dBm
RF Frequency Range		2400 to 2500		MHz	
IF Frequency Range	10	280	500	MHz	
Cascade Gain		28		dB	IF=280MHz, GAIN SEL = 1
		12		dB	IF=280MHz, GAIN SEL = 0
Cascade IP3		-23		dBm	Referenced to the input, GAIN SEL = 1
		-8		dBm	Referenced to the input, GAIN SEL = 0
Cascade Noise Figure		4.5		dB	Single sideband, GAIN SEL = 1
		18		dB	Single sideband, GAIN SEL = 0
Input P1dB		-28		dBm	GAIN SEL = 1
		-14		dBm	GAIN SEL = 0
LNA					
Noise Figure		2.3		dB	GAIN SEL = 1
		7		dB	GAIN SEL = 0
Input VSWR			2:1		No external matching
Input IP3		-3		dBm	GAIN SEL = 1
		-3		dBm	GAIN SEL = 0
Gain		10		dB	GAIN SEL = 1
		-6		dB	GAIN SEL = 0
Reverse Isolation		22		dB	
Output Impedance		50		Ω	
RF Amp and Mixer					
Noise Figure		10		dB	Single sideband
Input Impedance		50		Ω	
Input IP3		-17		dBm	
Conversion Power Gain		18		dB	With Current Combiner (1kΩ between open collectors and 250Ω single ended load)
Output Impedance		4		kΩ	Open Collector
LO Input					
LO Level	-15	-10	0	dBm	
LO to RF Rejection		42		dB	LO input to LNA input
LO to IF Rejection		15		dB	LO input to IF output
LO Input VSWR			2:1		
Power Down Control					
Logic Controls "ON"	V_{CC}-0.3			V	Voltage at the input of RX EN, PD
Logic Controls "OFF"			300	mV	and GAIN SEL
Turn on Time		400	1000	nS	From PD Going high.
Turn on Time		100	200	nS	From RX EN Going high. PD = "1"

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Power Supply					
Voltage	2.7	3.3	3.6	V	
Current Consumption		20	26	mA	GAIN SEL = 1, RX EN =1, PD = 1
		20	25	mA	GAIN SEL = 0, RX EN =1, PD = 1
		12	16	mA	GAIN SEL = X, RX EN =0, PD = 1
			1	µA	GAIN SEL = X, RX EN =X, PD = 0

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Pin	Function	Description	Interface Schematic
1	GAIN SEL	LNA gain control. When GAIN SEL is >V_{CC}-300mV, LNA gain is at 10 dB. When GAIN SEL is <300mV, the LNA gain is -6dB.	See pin 16.
2	LNA IN	This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. If a blocking capacitor is required, a value of 2pF is recommended.	See pin 16.
3	PD	The power enable pin. When PD is >V_{CC}-300mV, the part is biased on. When PD is <300mV, then the part is turned off and typically draws less than 1μA.	
4	VCC1	Supply voltage for bias circuits and logic control. A 10pF external bypass capacitor is required and an additional 0.01μF is required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	VCC2	Supply voltage for LO_Buffer. A 10pF bypass capacitor is required and an additional 0.01μF is required if there is no other low frequency bypass capacitor in the area. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	See pin 8.
6	MIXOUT-	The inverting open collector output of the mixer. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun, with MIXOUT+, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, MIXOUT+ may be used alone to drive a SAW single-ended, with an RF choke (high Z at IF) from VCC to MIXOUT-.	
7	MIXOUT+	The non-inverting open collector output of the mixer. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun, with MIXOUT+, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, MIXOUT+ may be used alone to drive a SAW single-ended, with an RF choke (high Z at IF) from VCC to MIXOUT+.	See pin 6.
8	LO IN	LO input pin. This input needs a DC blocking cap. External matching is recommended to 50Ω.	
9	RX EN	This control pin allows the mixer output pins to be put into a high impedance state. This allows the transmit signal path to share the same IF filter as the receiver.	
10	VCC3	Supply voltage for mixer preamp.	See pin 12.
11	GND3	Ground pin for mixer preamp. This lead inductance is intended to be similar to VCC3 lead inductance.	See pin 12.
12	MIX IN	Mixer RF Input port. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A value of >22pF is recommended. To minimize the noise figure it is recommended to have a bandpass filter before this input. This will prevent the noise at the image frequency from being converted to the IF.	

13	**NC**		
14	**NC**		
15	**LNA OUT**	RF signal output for external 50Ω filtering.The use of a filter here is optional but does provide for lower noise floor and better out-of-band rejection.	See pin 16.
16	**VCC4**	Supply voltage for the LNA. This pin should be bypassed with a 10 pF capacitor to ground as close to the pin as possible. The shunt inductance from this pin to ground via the supply decoupling must be tuned to match the LNA output to 50Ω at the desired operating frequency.	

Theory of Operation

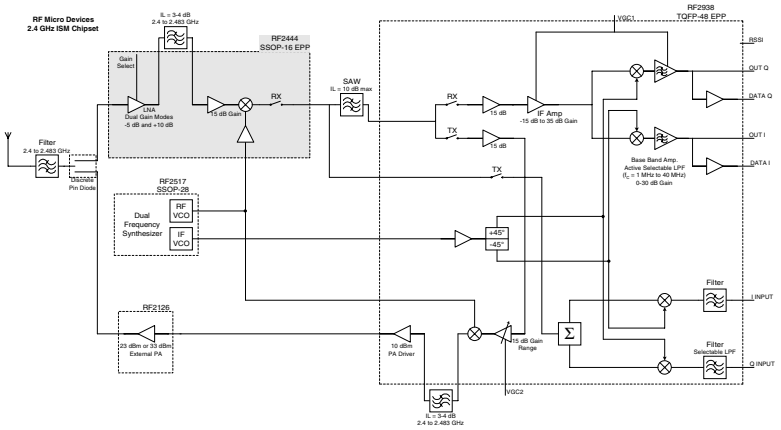


Figure 1. Entire Chipset Functional Block Diagram

The RF2444 contains the LNA/Mixer for this chipset. The LNA is made from two stages including a common emitter amplifier stage with a power gain of 13dB and an attenuator which has an insertion loss of 3dB in high gain mode, and 17dB in low gain mode. The attenuator was put after the LNA so that system noise figure degradation would be minimized. A single gain stage was used prior to the image filter to maximize IP3 which minimizes the risk of large out-of-bad signals jamming the desired signal.

The mixer on the RF2444 is also two stages. The first stage is a common emitter amp used to boost the total power gain prior to the lossy SAW filter, to convert to a differential signal to the input of the mixer, and to improve the noise figure of the mixer. The second stage is a double balanced mixer whose output is differential open collector. It is recommended that a "current combiner" is used (as shown in figure 2) at the mixer output to maximize conversion gain, but other loads can also be used. The current combiner is used to do a differential to single ended conversion for the SAW filter. C1, C2 and L1 are used to tune the circuit for a specific IF frequency. L2 is a choke to supply DC current to the mixer that is also used as a tuning element, along with C3, to match to the SAW filter's input impedance. RL is the SAW filter's input impedance.

The mixer power conversion gain is +19dB when R1 is set to 1kΩ. The conversion gain can be adjusted up ~5dB or down ~7dB by changing the value of R1. Once R1 is chosen, L2 and C3 can be used to tune the output for the SAW filter.

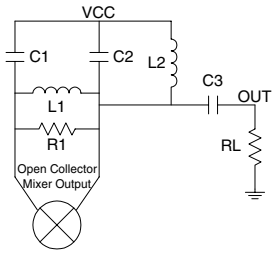


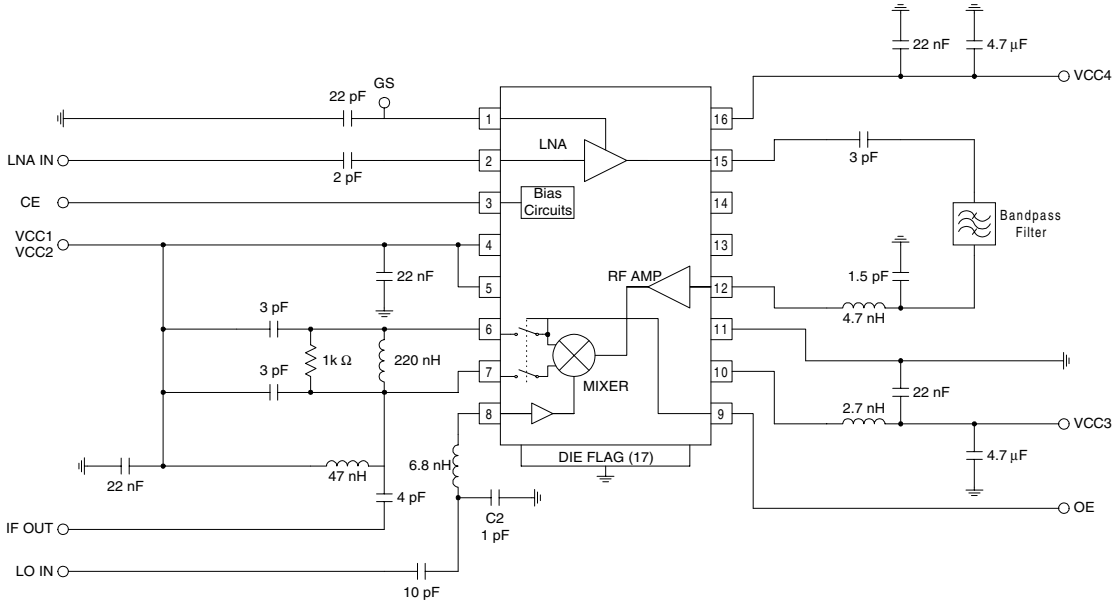
Figure 2. Current Combiner for Mixer Load

The cascaded power gain of the LNA/Mixer is 29dB, which after insertion loss in the image filter (~3dB) and IF SAW filter (~10dB), still gives 16dB of gain prior to the IF amps. Because of this, the noise figure of the IF amps should not significantly degrade system noise figure.

The LNA input should be matched for a good return loss for optimum gain and noise figure. To allow the designer to match each of these ports, 2-port s-parameter data is available for the LNA, and 1-port data is available for MIXER IN and LO IN.

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Application Schematic



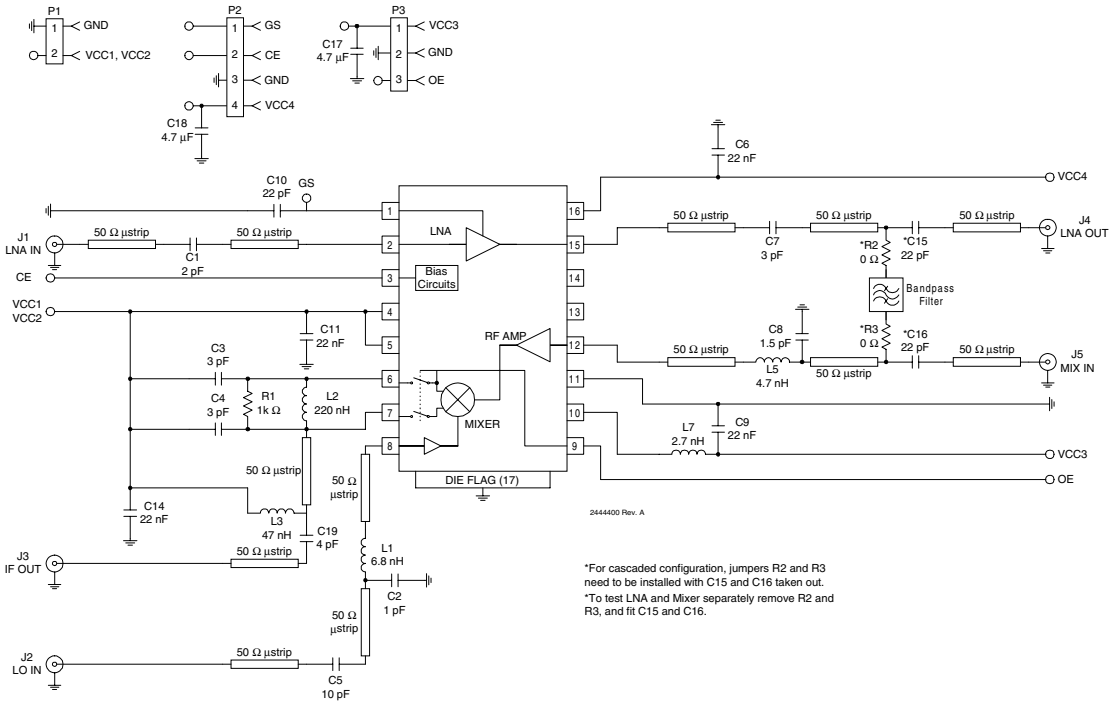
8

FRONT-ENDS

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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

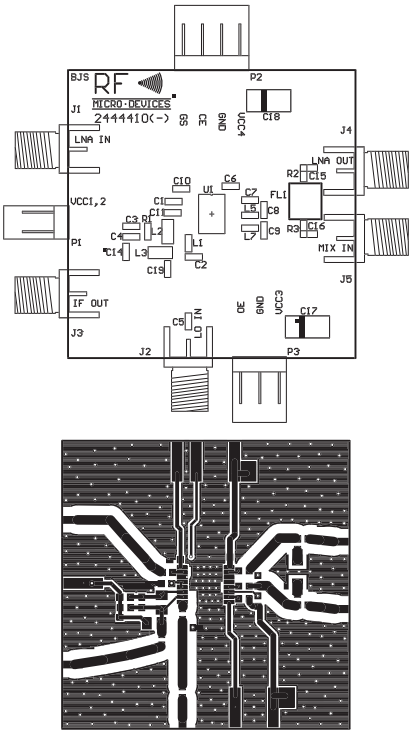


*For cascaded configuration, jumpers R2 and R3 need to be installed with C15 and C16 taken out.
*To test LNA and Mixer separately remove R2 and R3, and fit C15 and C16.

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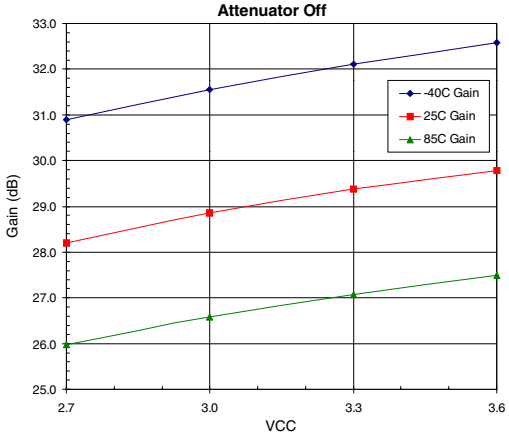
Evaluation Board Layout

Board Thickness .031", Board Material FR-4

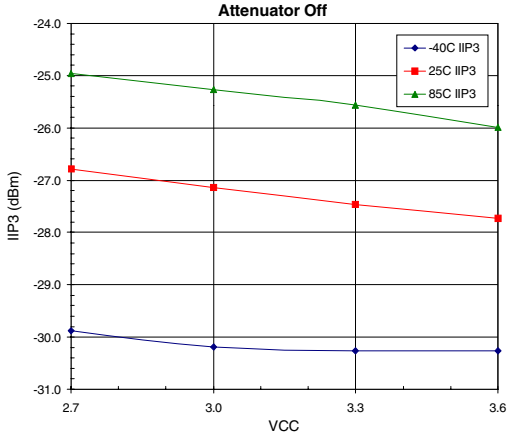


NOTE: In the following charts, all cascaded data measured with a bandpass filter inserted between LNA OUT and MIX IN, having cut frequencies: f_L=TBD, f_M=TBD, and insertion loss=TBD.

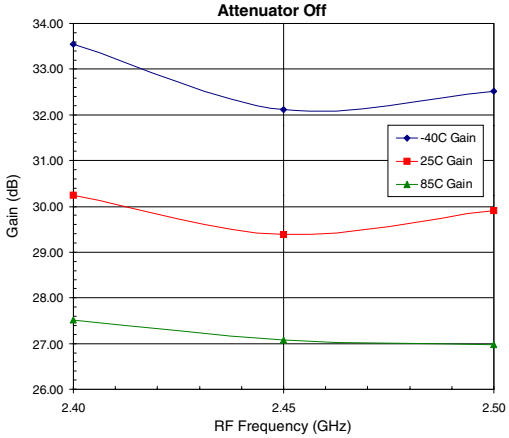
LNA + Mixer Gain versus VCC (2.45 GHz), Attenuator Off



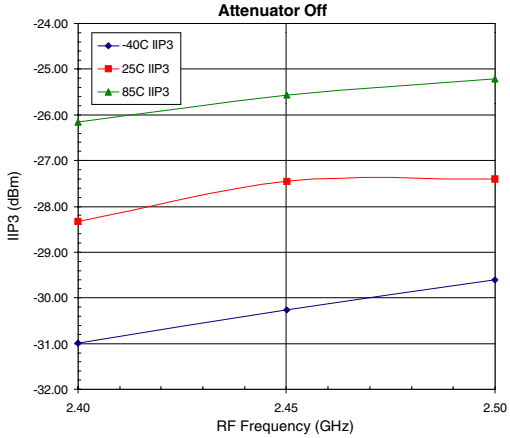
LNA + Mixer IIP3 versus VCC (2.45 GHz), Attenuator Off



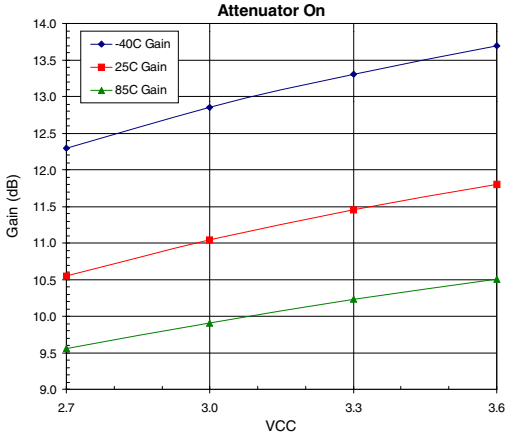
LNA + Mixer Gain versus RF Frequency (3.3 V), Attenuator Off



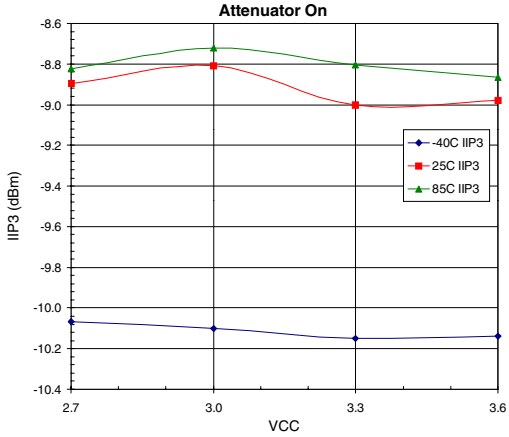
LNA + Mixer IIP3 versus RF Frequency (3.3V), Attenuator Off



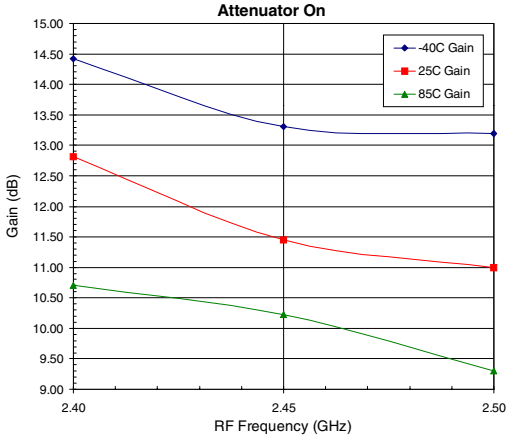
LNA + Mixer Gain versus VCC (2.45 GHz), Attenuator On



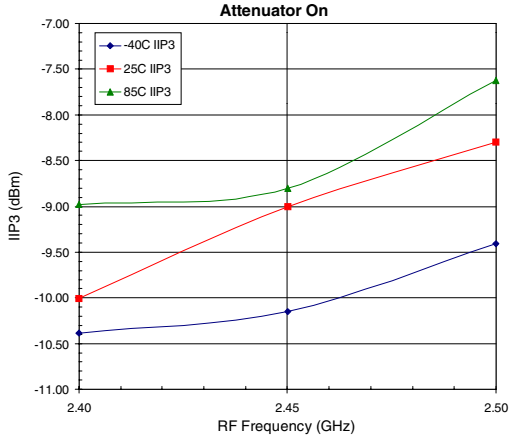
LNA + Mixer IIP3 versus VCC (2.45 GHz), Attenuator On



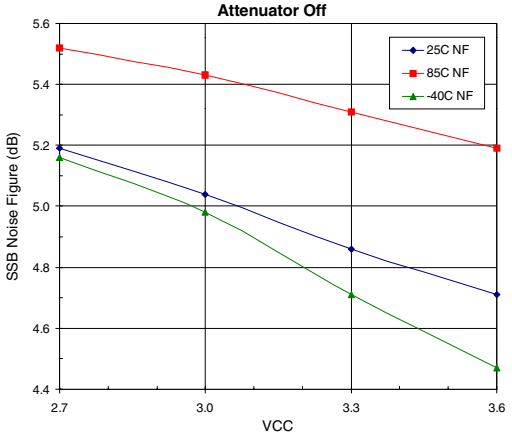
LNA + Mixer Gain versus RF Frequency (3.3 V), Attenuator On



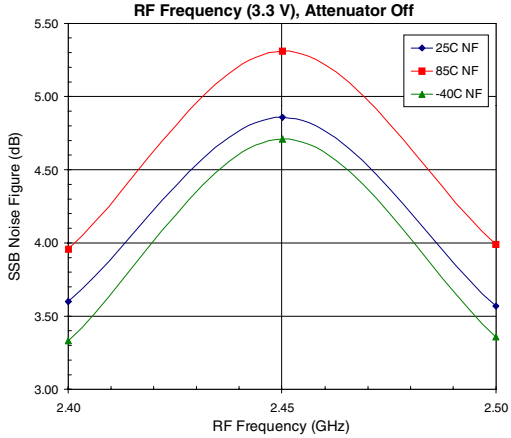
LNA + Mixer IIP3 versus RF Frequency (3.3 V), Attenuator On



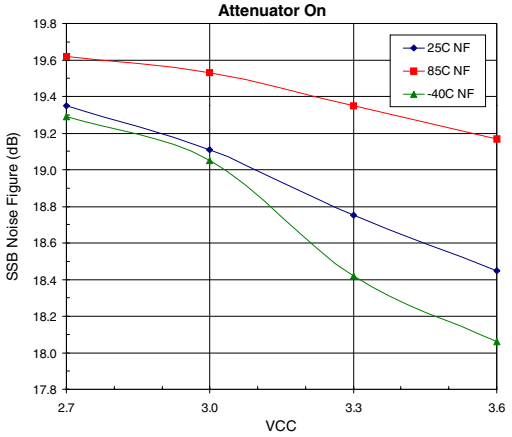
LNA + Mixer SSB Noise Figure versus VCC (2.45 GHz), Attenuator Off



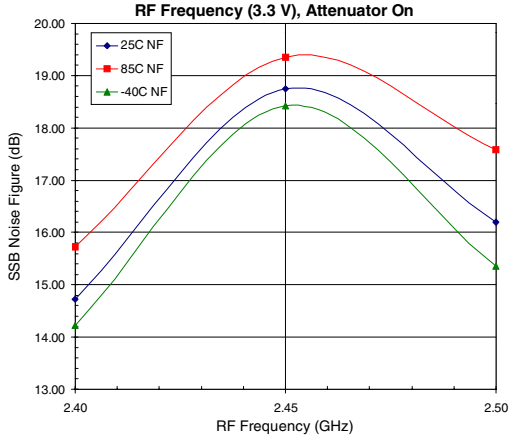
LNA + Mixer SSB Noise Figure versus RF Frequency (3.3 V), Attenuator Off



LNA + Mixer SSB Noise Figure versus VCC (2.45 GHz), Attenuator On

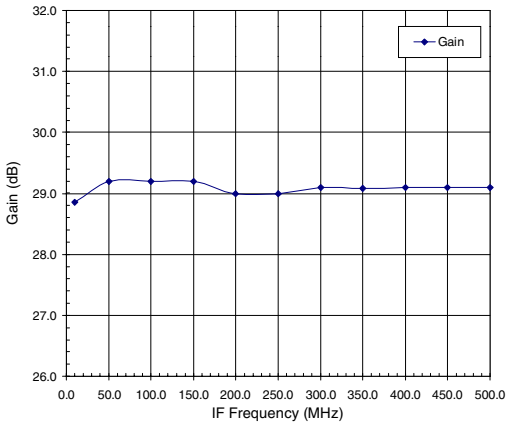


LNA + Mixer SSB Noise Figure versus RF Frequency (3.3 V), Attenuator On

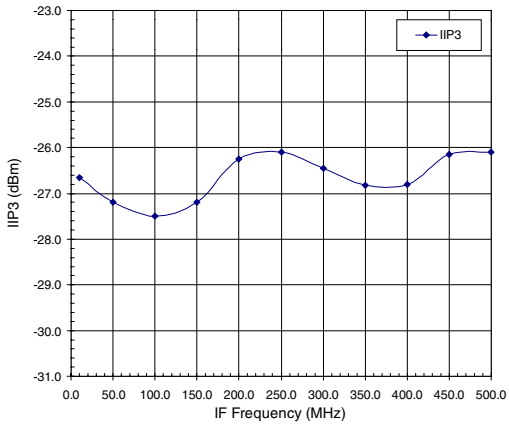


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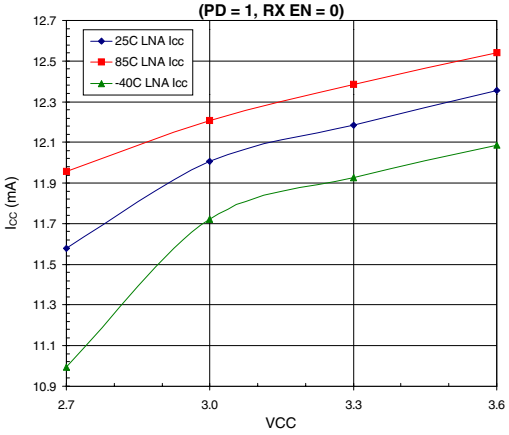
LNA + Mixer Gain versus IF Frequency (3.3 V)



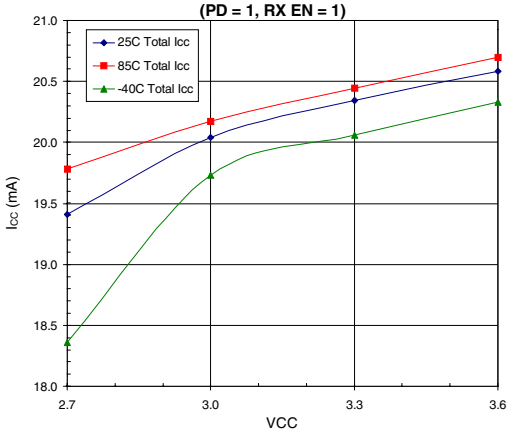
LNA + Mixer IIP3 versus IF Frequency (3.3 V)



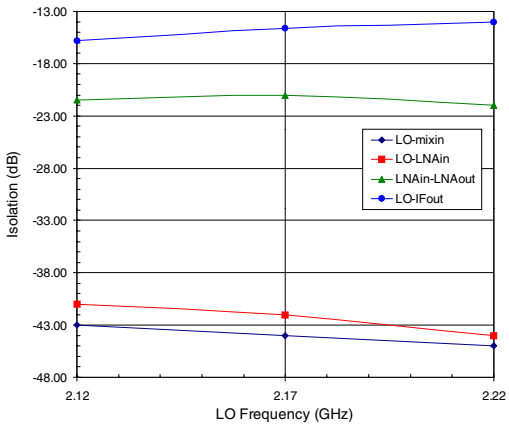
LNA I_{CC} versus VCC (PD = 1, RX EN = 0)



Total I_{CC} versus VCC (PD = 1, RX EN = 1)

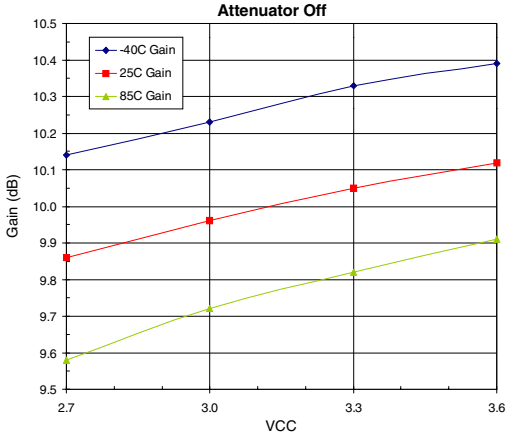


Isolation

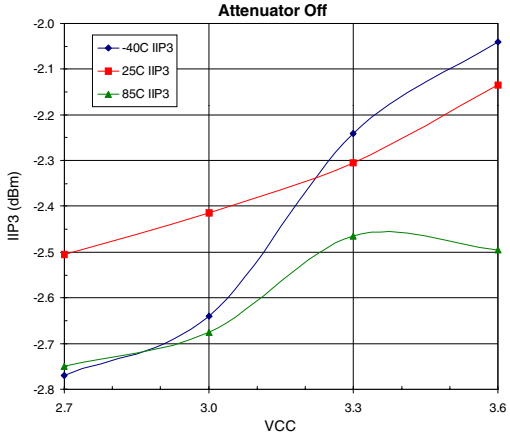


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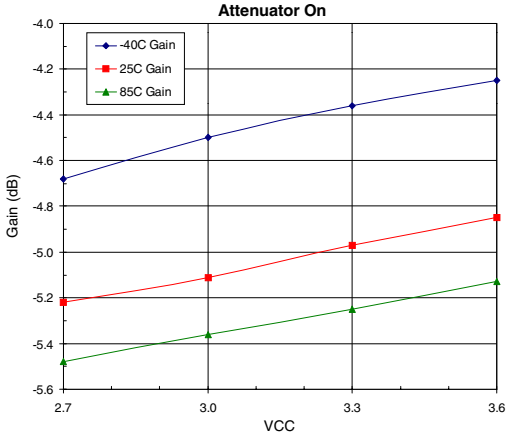
LNA Gain versus VCC (2.45 GHz), Attenuator Off



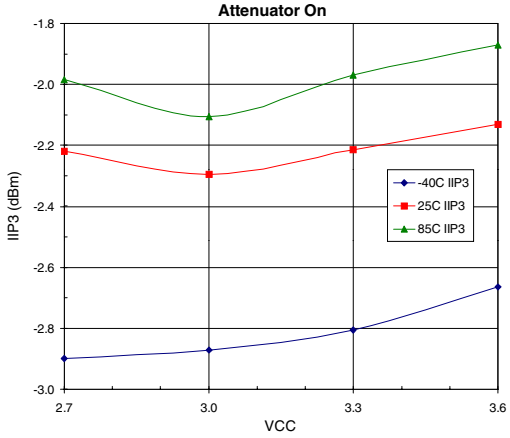
LNA IIP3 versus VCC (2.45 GHz), Attenuator Off



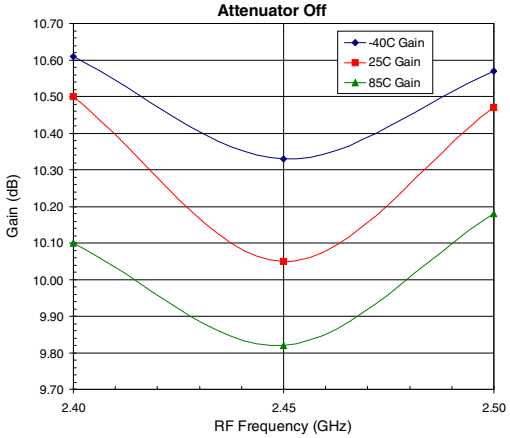
LNA Gain versus VCC (2.45 GHz), Attenuator On



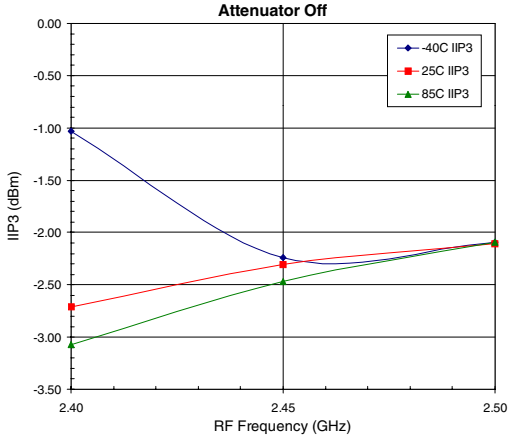
LNA IIP3 versus VCC (2.45 GHz), Attenuator On



LNA Gain versus RF Frequency (3.3 V), Attenuator Off

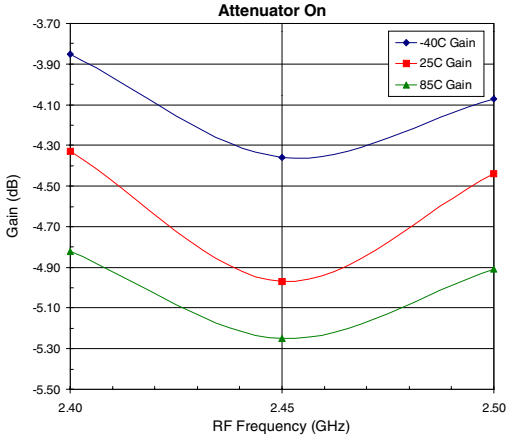


LNA IIP3 versus RF Frequency (3.3 V), Attenuator Off

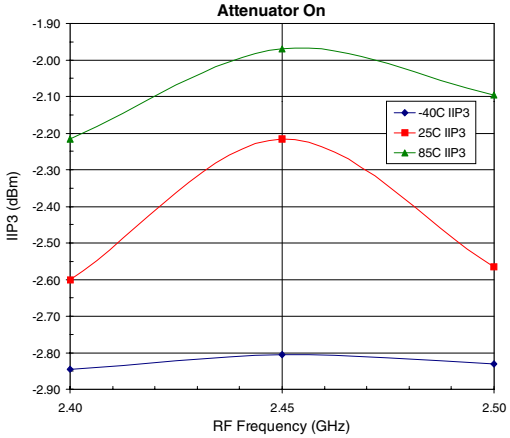


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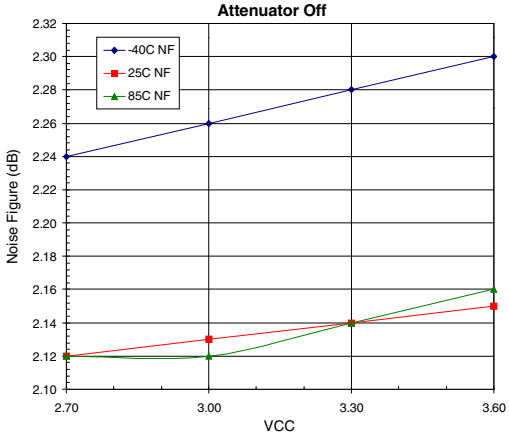
LNA Gain versus RF Frequency (3.3 V), Attenuator On



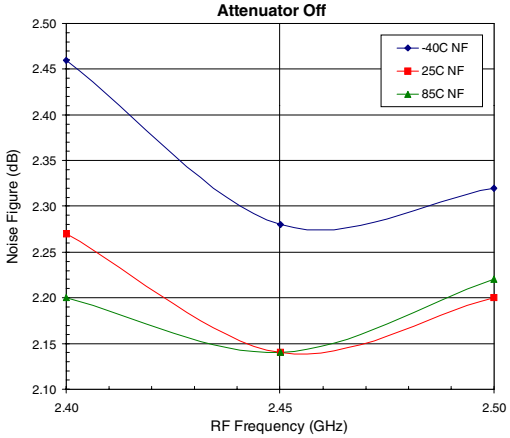
LNA IIP3 versus RF Frequency (3.3 V), Attenuator On



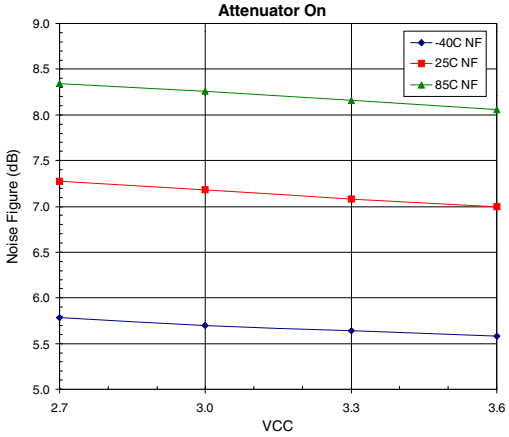
LNA Noise Figure versus VCC (2.45 GHz), Attenuator Off



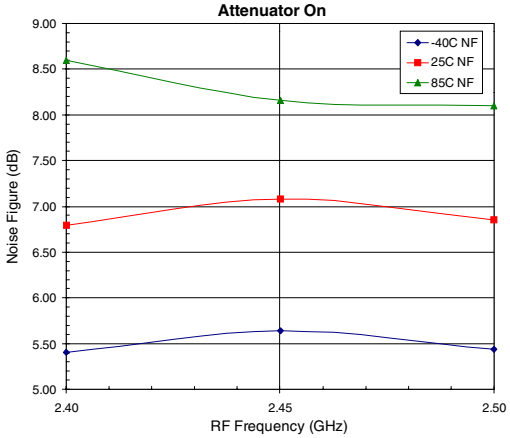
LNA Noise Figure versus RF Frequency (3.3 V), Attenuator Off



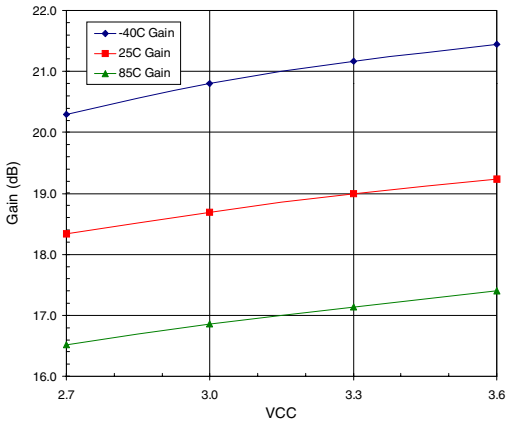
LNA Noise Figure versus VCC (2.45 GHz), Attenuator On



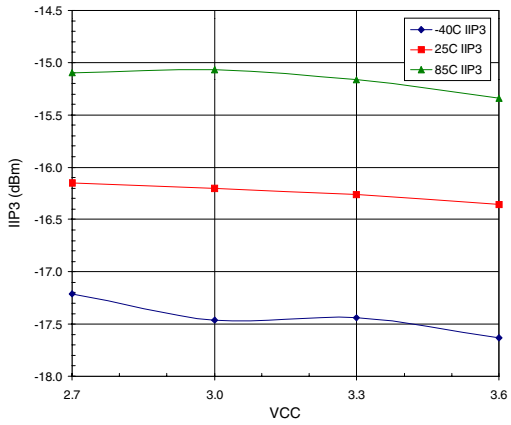
LNA Noise Figure versus RF Frequency (3.3 V), Attenuator On



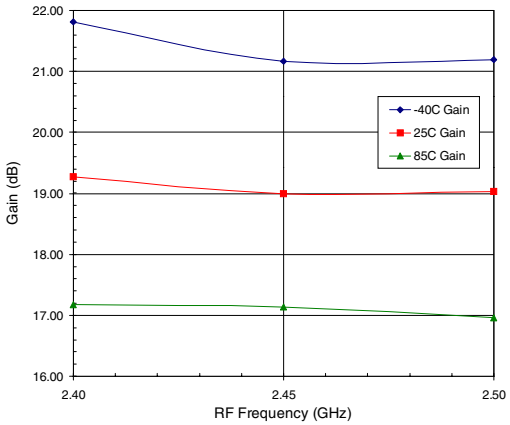
Mixer Gain versus VCC (2.45 GHz)



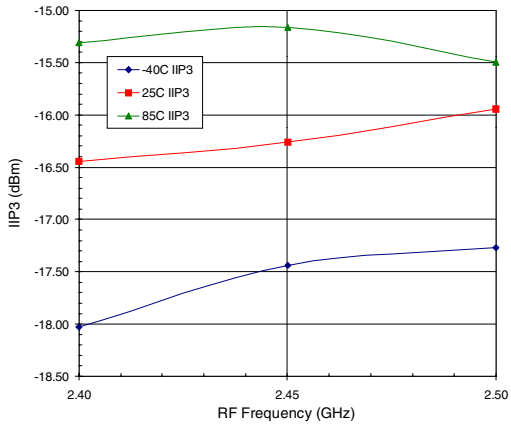
Mixer IIP3 versus VCC (2.45 GHz)



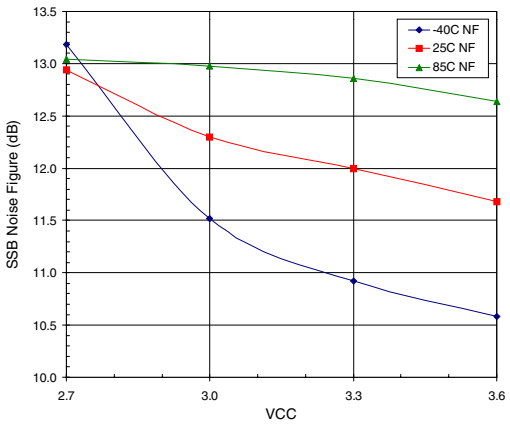
Mixer Gain versus RF Frequency (3.3 V)



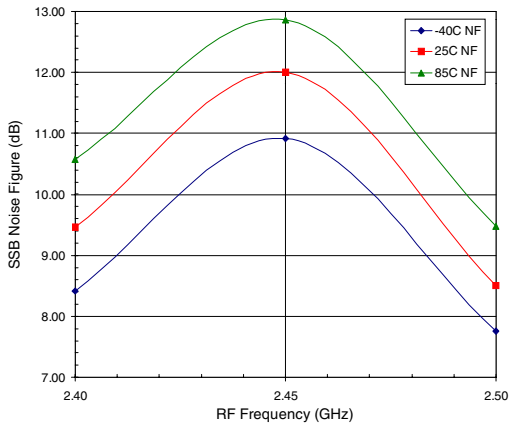
Mixer IIP3 versus RF Frequency (3.3 V)



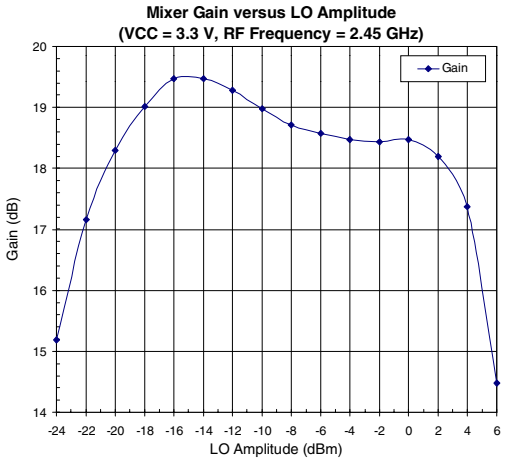
Mixer SSB Noise Figure versus VCC (2.45 GHz)

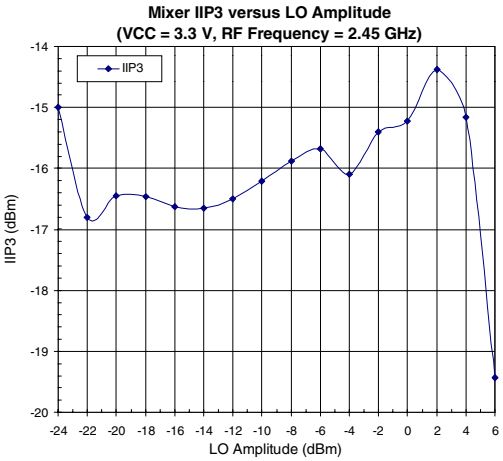


Mixer SSB Noise Figure versus RF Frequency (3.3 V)



8 FRONT-ENDS


Mixer Gain versus LO Amplitude
(VCC = 3.3 V, RF Frequency = 2.45 GHz)
Gain
Gain (dB)
LO Amplitude (dBm)


Mixer IIP3 versus LO Amplitude
(VCC = 3.3 V, RF Frequency = 2.45 GHz)
IIP3
IIP3 (dBm)
LO Amplitude (dBm)

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RF2448

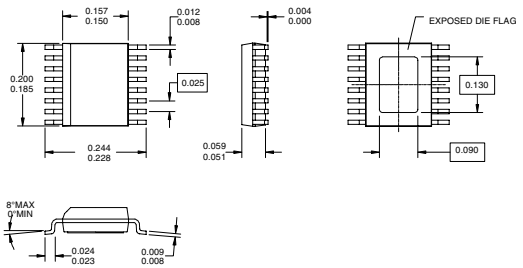
PCS CDMA LOW NOISE AMPLIFIER/MIXER 1500MHZ TO 2200MHZ DOWNCONVERTER

Typical Applications

- CDMA PCS Handsets
- TDMA PCS Handsets
- GSM PCS Handsets
- General Purpose Receiver Front-End
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

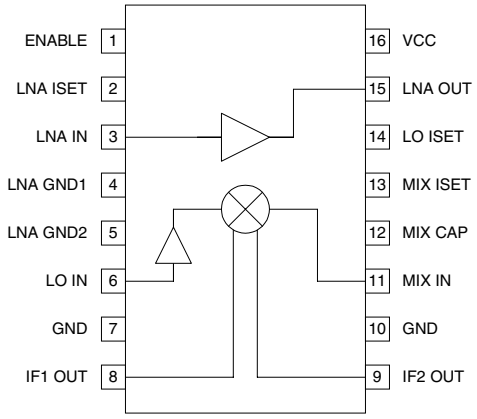
The RF2448 is a receiver front-end designed for the receive section of PCS CDMA, TDMA and GSM applications. It is designed to amplify and downconvert RF signals. A further feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. The LNA IIP3 can be digitally controlled between two levels to reduce current draw in standby and other conditions where high IIP3 is not required. Noise Figure, IP3, and other specs are designed to be compatible with the CDMA, TDMA and GSM PCS communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-16 with an exposed die flag.



Package Style: SSOP-16EDF

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Adjustable LNA/Mixer Bias Current
- Adjustable LNA/Mixer IIP3

Ordering Information

RF2448	PCS CDMA Low Noise Amplifier/Mixer 1500MHz to 2200MHZ Downconverter
RF2448 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

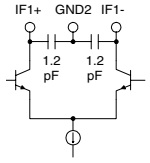
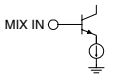
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

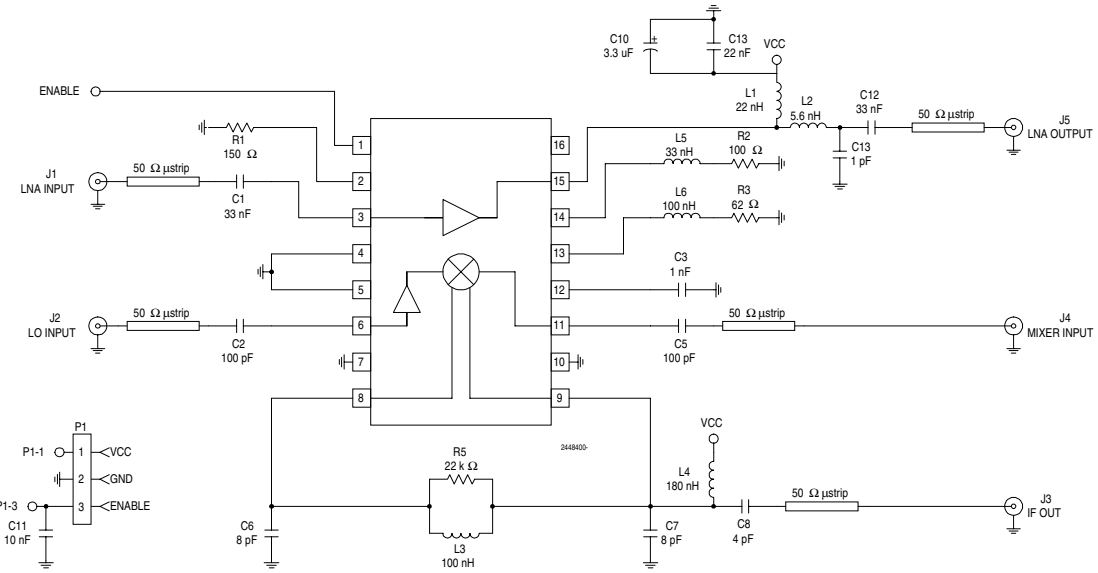
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.75V, RF=1959MHz, LO=1749MHz @ -2dBm
RF Frequency Range		1500 to 2200		MHz	
LO Frequency Range		1200 to 2200		MHz	
IF Frequency Range		0.1 to 250		MHz	
LNA					
Gain	13	14	15	dB	
Noise Figure		2.3		dB	
IIP3		+5.0		dBm	
Current at Max IIP3		5.0		mA	
Mixer					1kΩ balanced load.
Gain		7.8		dB	
Noise Figure		11.5		dB	
IIP3		7.0		dBm	
RF to IF Isolation	40			dB	
Current		8.0		mA	
Local Oscillator Input					
Input Level	-10	-6	-4	dBm	
LO to IF Isolation	36			dB	
LO to LNA Isolation	35			dB	Any gain state.
Power Supply					
Voltage	2.65	2.75	3.9	V	

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Pin	Function	Description	Interface Schematic
1	ENABLE	Power down control. This is a CMOS input. When this pin is CMOS "high" the device is enabled. When the level is CMOS "low" the device is shut off and a controlled attenuator is turned on.	
2	LNA ISET	This pin sets the current for the device. A resistor to ground of 1kΩ provides a current of 17.5mA. The condition for optimal IP3 is to use the internal current setting option and leave this pin open (no connect).	
3	LNA IN	RF input pin. This pin is not internally DC blocked and requires an external blocking capacitor.	
4	LNA GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA GND2	Ground connection for the bias circuits.	
6	LO IN	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 18 is bypassed to ground.	
7	GND	Ground connection.	
8	IF1 OUT	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 210MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
9	IF2 OUT	Same as pin 8, except complementary output.	See pin 8.
10	GND	Ground connection.	
11	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
12	MIX CAP	Bypass capacitor for mixer.	
13	MIX ISET	This pin is used to set the bias current and IIP3 of the mixer buffer amplifier using a resistor to ground.	
14	LO ISET	This pin is used to set the bias current for the LO buffer amplifier using a resistor to ground.	
15	LNA OUT	LNA Output pin. This pin is internally DC blocked and externally matched to 50Ω in order to facilitate an easy interface to a 50Ω Image Filter.	See pin 2.
16	VCC	Power supply for the bias circuits.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

Evaluation Board Schematic

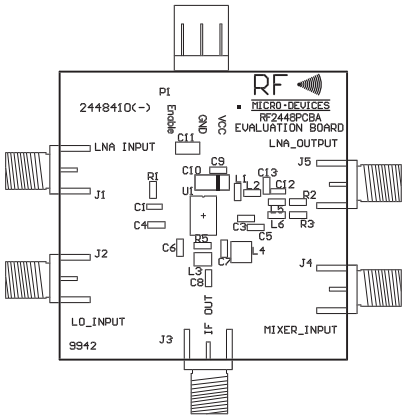
(Download Bill of Materials from www.rfmd.com.)

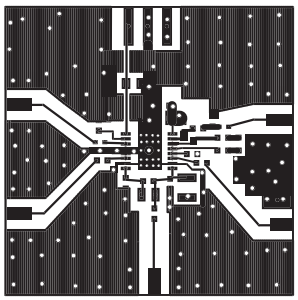


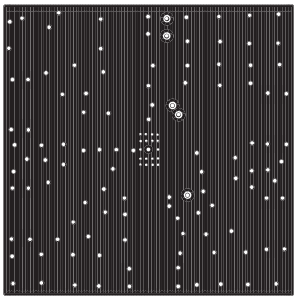
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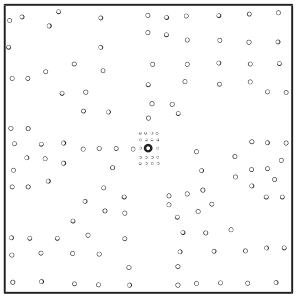
Evaluation Board Layout
Board Size 1.5” x 1.5”

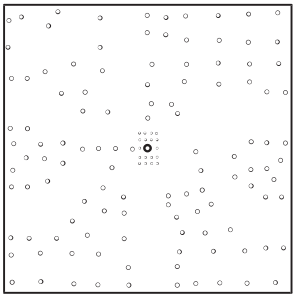
Board Thickness 0.056”, Board Material FR-4, Multi-Layer











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CDMA/FM LOW NOISE AMPLIFIER/MIXER 900MHZ DOWNCONVERTER

Typical Applications

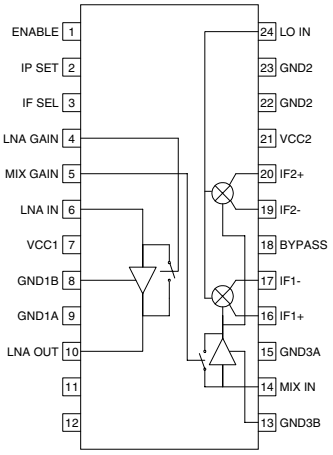
- CDMA/FM Cellular Systems
- Supports Dual-Mode CDMA/AMPS
- Supports Dual-Mode CDMA/TACS
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

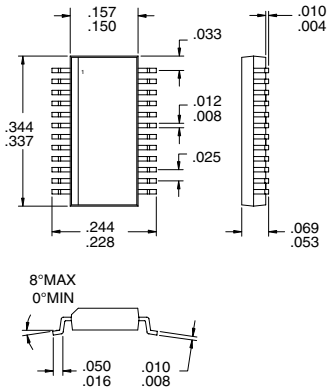
The RF2449 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals, while providing 30dB of stepped gain control range. Features include digital control of LNA gain, mixer gain, LNA IIP3, and power down mode. Another feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. The LNA IIP3 can be digitally controlled between two levels to reduce current draw in CDMA standby and other conditions where high IIP3 is not required. Noise Figure, IP3, and other specs are designed to be compatible with the IS-98 specification for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-24.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-24

Features

- Complete Receiver Front-End
- Stepped LNA/Mixer Gain Control
- Adjustable LNA/Mixer Bias Current
- Adjustable LNA/Mixer IIP3
- Digital LNA IIP3 Control
- Meets IS-98 IMD and Single Tone

Ordering Information

RF2449	CDMA/FM Low Noise Amplifier/Mixer 900MHz Downconverter
RF2449 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

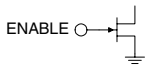
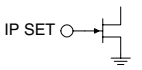
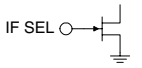
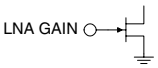
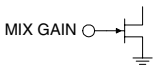
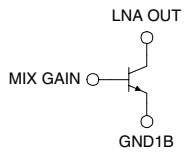
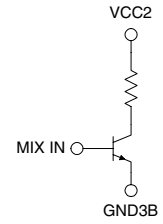
Caution! ESD sensitive device.

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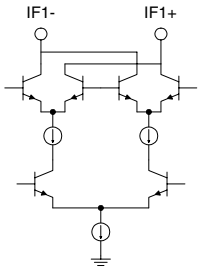
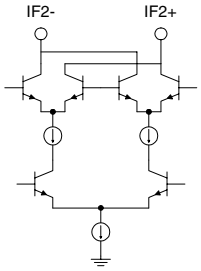
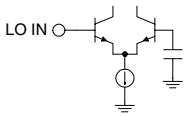
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.75V, RF=880MHz, LO=990MHz@0dBm, IF = 110MHz, V_{IPSET}<1.0V
RF Frequency Range		869 to 894		MHz	
LO Frequency Range		760 to 1010		MHz	
IF Frequency Range		0.1 to 250		MHz	
LNA - High Gain Mode					
Gain	14	15		dB	
Noise Figure		2.3	2.5	dB	
IIP3		+6		dBm	IIP3 is adjustable.
LNA Out to Mixer in Isolation		40		dB	
Current		3.5		mA	
LNA Bypass					
Gain		-6.3		dB	
Noise Figure		6.3		dB	
IIP3		20		dBm	
Current		0		mA	
Mixer - High Gain Mode					3kΩ balanced load.
Gain	12	13		dB	
Noise Figure		6.5	7.5	dB	
IIP3	+2	+3		dBm	IIP3 is adjustable - See Data Plots.
RF to IF Isolation	40			dB	
Current		21		mA	
Mixer - Low Gain Mode					3kΩ balanced load.
Gain	3	4		dB	
Noise Figure		13	14	dB	
IIP3	+12	+13		dBm	IIP3 is adjustable - See Data Plots.
RF to IF Isolation	40			dB	
Current		16		mA	
Local Oscillator Input					
Input Level	-10	-3	0	dBm	
LO to IF Isolation	36			dB	
LO to LNA Input Isolation	35			dB	Any gain state.
Cascade (Mode 1)					(LNA Gain High, Mix Gain High) With -3dB image rejection filter.
Gain	24	25	27	dB	3kΩ balanced IF load.
Noise Figure		2.9		dB	Single sideband.
IIP3	-10	-9		dBm	
Cascade (Mode 2)					(LNA Gain High, Mix Gain Low) With -3dB image rejection filter.
Gain		16.0		dB	3kΩ balanced IF load.
Noise Figure		4.7		dB	Single sideband.
IIP3		0		dBm	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Cascade (Mode 3)					(LNA Gain Low, Mix Gain High) With -3dB image rejection filter.
Gain		3.5		dB	3kΩ balanced IF load.
Noise Figure		16		dB	Single sideband.
IIP3		+11.8		dBm	
Cascade (Mode 4)					(LNA Gain Low, Mix Gain Low) With -3dB image rejection filter.
Gain		-5		dB	3kΩ balanced IF load.
Noise Figure		22.5		dB	Single sideband.
IIP3	+16.0	+18.0		dBm	
Power Supply					
Voltage	2.65	2.75	3.9	V	
Power Down Current			10	μA	Enable<1.0V

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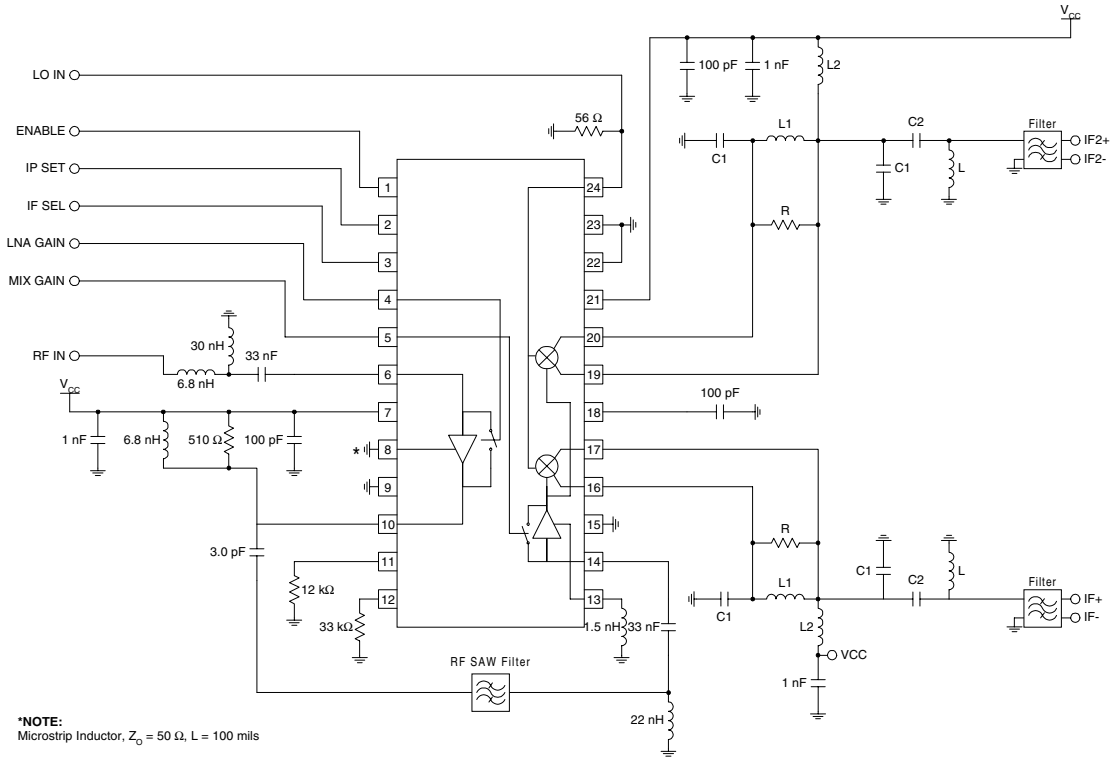
Pin	Function	Description	Interface Schematic
1	ENABLE	This pin is used to enable or disable the RF2449. A logic high (>2.0V) enables the circuitry. A logic low (<1.0V) disables the circuitry.	
2	IP SET	Controls the setting of the LNA current. A logic low (<1.0V) selects the internal resistance (49.5kΩ), resulting in an LNA current of 3.5mA. A logic high (>2.0V) selects the external resistance at pin 12.	
3	IF SEL	Determines which IF port is active. A logic low (<1.0V) activates IF1 and deactivates IF2. A logic high (>2.0V) activates IF2 and deactivates IF1.	
4	LNA GAIN	Controls the bypass feature of the LNA. A logic low (<1.0V) selects the bypass mode. A logic high (>2.0V) turns on the LNA.	
5	MIX GAIN	Controls the bypass feature of the mixer pre-amp. A logic low (<1.0V) selects the bypass mode. A logic high (>2.0V) turns on the pre-amp.	
6	LNA IN	LNA input pin.	
7	VCC1	VCC pin for all circuits except the LO.	
8	GND1B	LNA ground pin.	See pin 6.
9	GND1A	Package ground pin.	
10	LNA OUT	LNA output pin.	See pin 6.
11	ISET2	An external resistor connected to this pin sets the current of the pre-amp and the mixer.	
12	ISET1	An external resistor connected to this pin sets the current of the LNA when IP SET is high (see pin 2).	
13	GND3B	Ground pin for pre-amp circuit.	
14	MIX IN	Mixer pre-amp input pin.	See pin 13.
15	GND3A	Ground pin for the mixer circuits.	

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Pin	Function	Description	Interface Schematic
16	IF1+	First differential output pin for the first mixer.	
17	IF1-	Second differential output pin for the first mixer.	See pin 16.
18	BYPASS	Bypass pin for the LO bias reference.	
19	IF2+	First differential output pin for the second mixer.	
20	IF2-	Second differential output pin for the second mixer.	See pin 20.
21	VCC2	VCC pin for the LO circuits.	
22	GND2	Ground pin for the LO circuits.	
23	GND2	Ground pin for the LO circuits.	
24	LO IN	Local oscillator input pin.	

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Application Schematic



***NOTE:**
Microstrip Inductor, Z_O = 50 Ω, L = 100 mils

Suggested component values for 85.38 MHz IF and R_{OUT} = 1 kΩ:
L1 = 470 nH C1 = 10 pF R = 7.5 kΩ

Output Interface Network

L1, C1 and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C1 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 16 and 17. An average value to use for C_{EQ} is 2.5pF.

R may then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L1.

C1 should be chosen as high as possible, while maintaining an R_P of L1 that allows for the desired R_{OUT}.

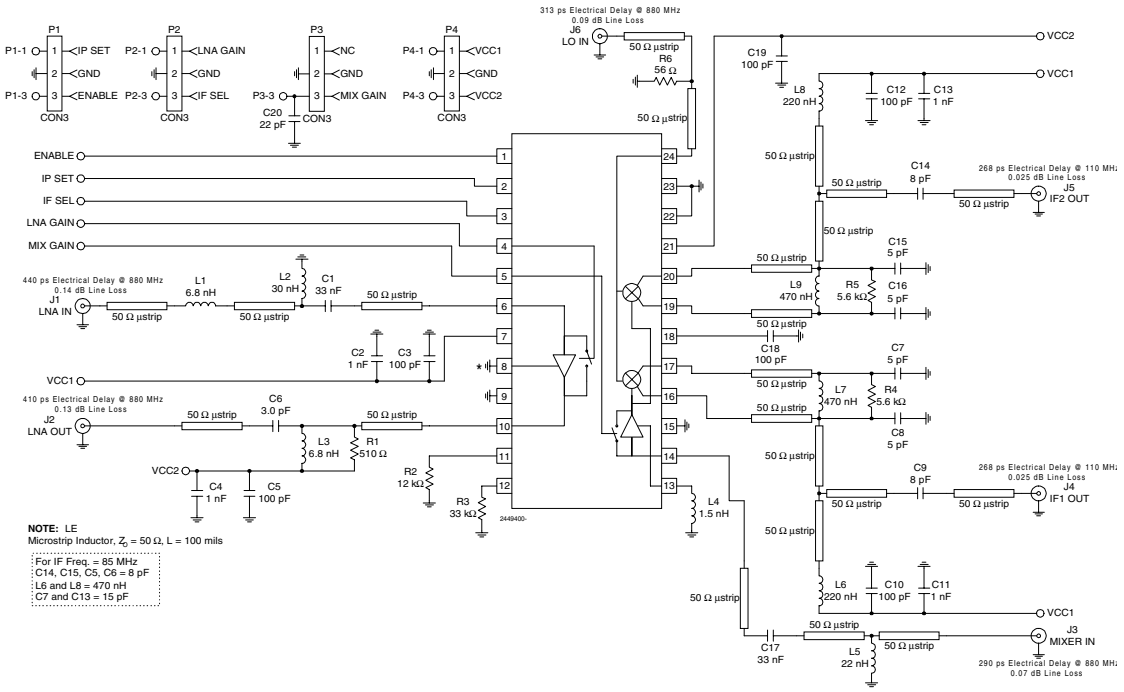
L2 and C2 serve dual purposes. L2 serves as an output bias choke, and C2 serves as a series DC block.

In addition, L2 and C2 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to ROUT. Otherwise, L2 is chosen to be large and C2 is chosen to be large if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

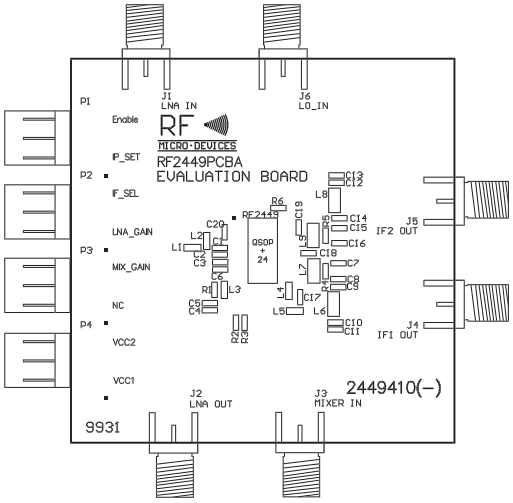


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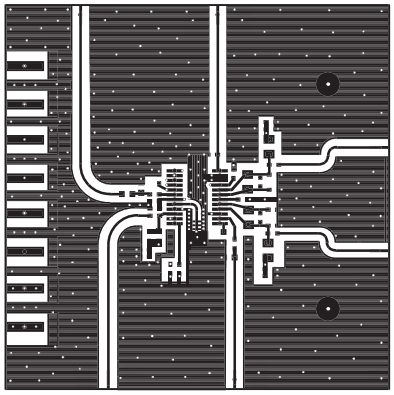
Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.040", Board Material FR-4, Multi-Layer

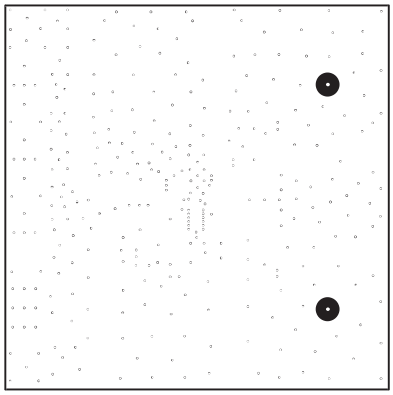
Assembly



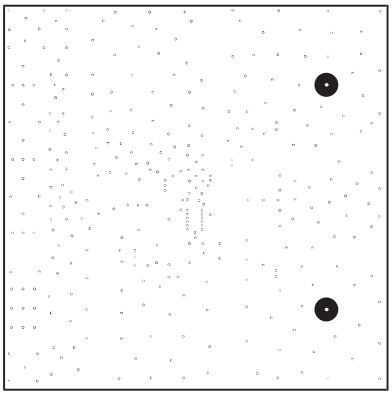
Top



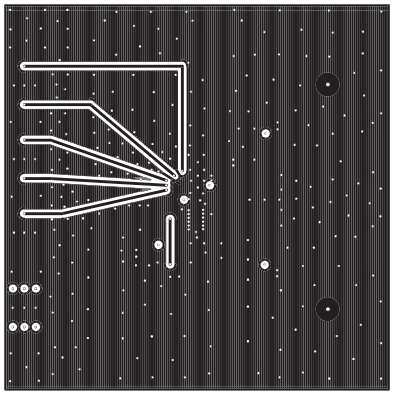
Inner 1



Inner 2



Back



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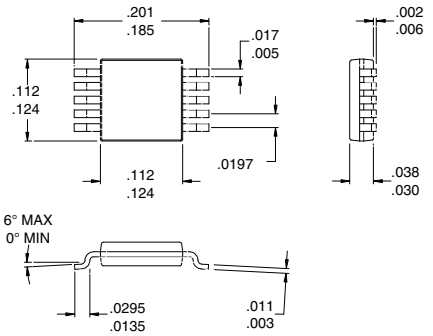
900MHZ 3V LOW CURRENT LNA/MIXER

Typical Applications

- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- General Purpose Frequency Conversion

Product Description

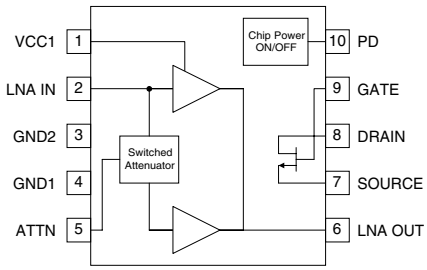
The RF2457 is a front-end receiver IC chip developed for the handset/portable battery-powered equipment markets. The chip contains an RF 15dB attenuator, an LNA and a passive mixer. By using a state-of-the-art Si Bi-CMOS process, the LNA has high dynamic range under very low DC operating conditions and the passive mixer requires no DC bias at all. Packaged in the industry-standard MSOP-10 package, the device is well-suited for limited board space applications.



Package Style: MSOP-10

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single Supply 3V Operation
- 2.2dB LNA NF
- -3.0dBm IIP3
- Small MSOP-10 Package
- Very Low Current Drain (5mA maximum)
- Very Low Cost

Ordering Information

RF2457	900MHz 3V Low Current LNA/Mixer
RF2457 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

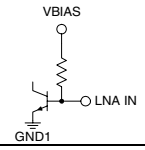
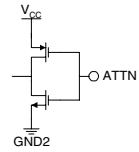
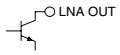
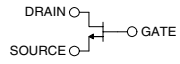
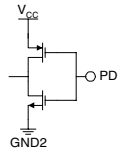
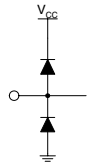
Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.8V, RF=915MHz
RF/LO Frequency Range		902 to 928		MHz	Specifications
		800 to 1000		MHz	Usable range
LNA					
Gain	14.0	15.0		dB	High gain state
	0.9	1.9		dB	Low gain state
Input IP3	-4.0	-3.0		dBm	High gain state, RF IN=-25dBm
	+5.5	+6.5		dBm	Low gain state, RF IN=-15dBm
Noise Figure		2.2	2.4	dB	High gain state
		15		dB	Low gain state
Input VSWR			2.2:1		
Output VSWR			2.0:1		
Mixer					
Conversion Gain	-7.5	-6.5		dB	With LO=+2dBm
LO Input Level	-2.0	0	+2.0	dBm	
IIP3	+10.0	+12.0		dBm	With LO=+2dBm
Attenuation					
Attn enable		>1.6		V	Low gain state
Attn disable		0		V	High gain state
Power Down					
Chip enable		>1.6		V	Voltage applied to PD pin
Chip disable		0		V	Voltage applied to PD pin
Noise figure		6.5		dB	With LO=+2dBm
Power Supply					
Voltage		2.8		V	Specifications
		2.7 to 3.3		V	Operating limits
Current Consumption		5	6.5	mA	Chip enabled
		<1	1.0	uA	Chip disabled

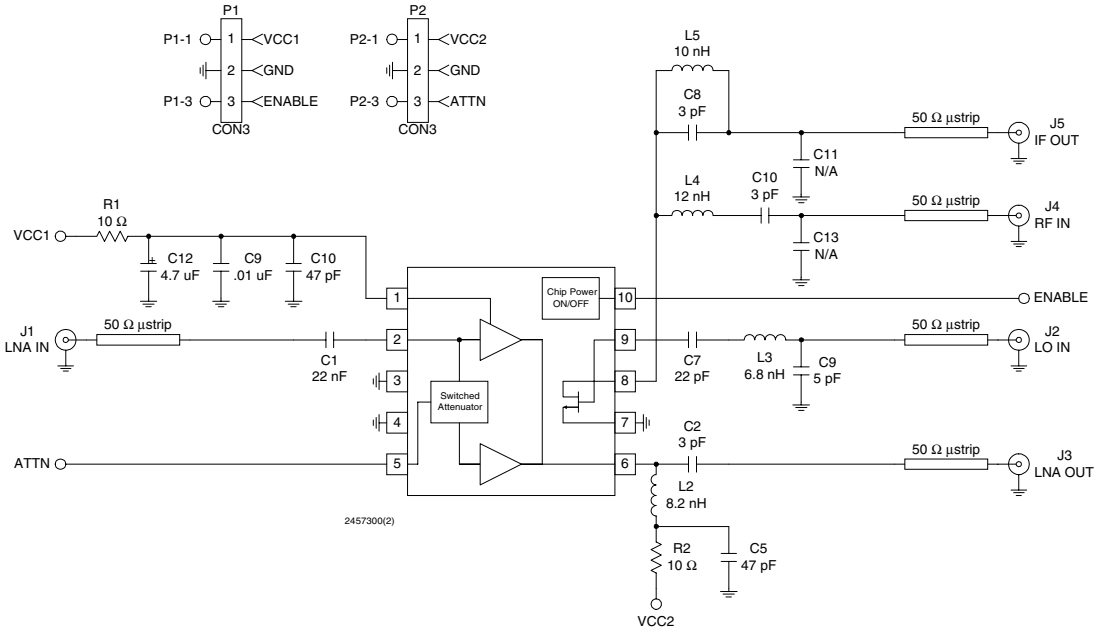
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Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LNA, bias circuits, and control logic. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
2	LNA_IN	RF Input pin. This pin is internally matched for optimum noise figure from a 50Ω source. This pin is internally DC biased and, if connected to a device with DC present, should be blocked with a capacitor suitable for the frequency of operation.	
3	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND1	Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance.	See pin 2.
5	ATTN	Attenuation pin. A logic high reduces LNA gain by 15dB.	
6	LNA OUT	LNA Output pin. This pin requires a connection to V_{CC} through an inductor.	
7	SOURCE	Connection to source of MOSFET transistor used as mixer. Drain and source are symmetric.	
8	DRAIN	Connection to drain of MOSFET transistor used as mixer.	See pin 7.
9	GATE	Connection to gate of MOSFET transistor used as mixer. Internally DC biased. Use DC blocking capacitor.	See pin 7.
10	PD	Power control. A logic “low” turns the part off. A logic “high” (>1.6V) turns the part on.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 9, 10.	

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Evaluation Board Schematic

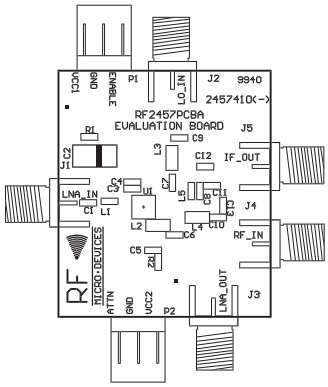
(Download Bill of Materials from www.rfmd.com.)

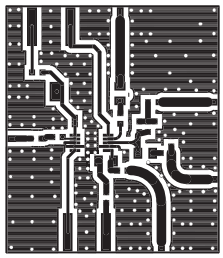


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Evaluation Board Layout
Board Size 1.108" x 1.282"

Board Thickness 0.031”, Board Material FR-4







8

FRONT-ENDS

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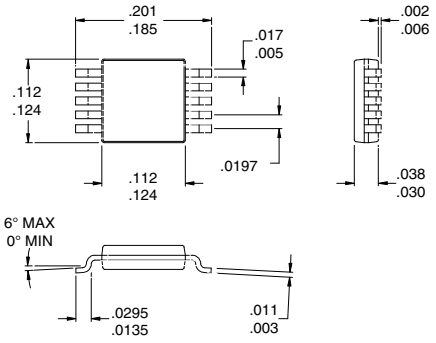
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Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- General Purpose Downconverter
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

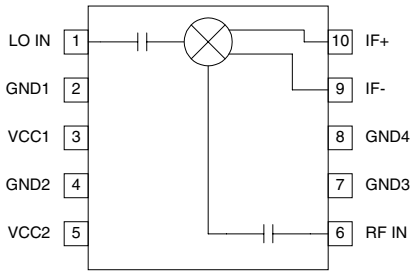
The RF2458 is a monolithic integrated downconverter for PCS, PHS, and WLAN applications. The IC contains all of the required components to implement the RF functions of the downconverter. It contains a double-balanced Gilbert cell mixer and a balanced IF output. The high gain makes it ideal for front end applications. The IC is designed to operate from a single 3V power supply.



Package Style: MSOP-10

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Extremely High Dynamic Range
- Single 3V Power Supply
- 1500MHz to 2500MHz Operation

Ordering Information

RF2458	3V PCS Downconverter
RF2458 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

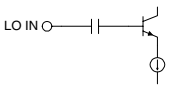
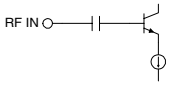
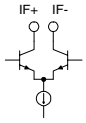
Parameter	Ratings	Unit
Supply Voltage		V_{DC}
Input LO and RF Levels		dBm
Ambient Operating Temperature		°C
Storage Temperature		°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

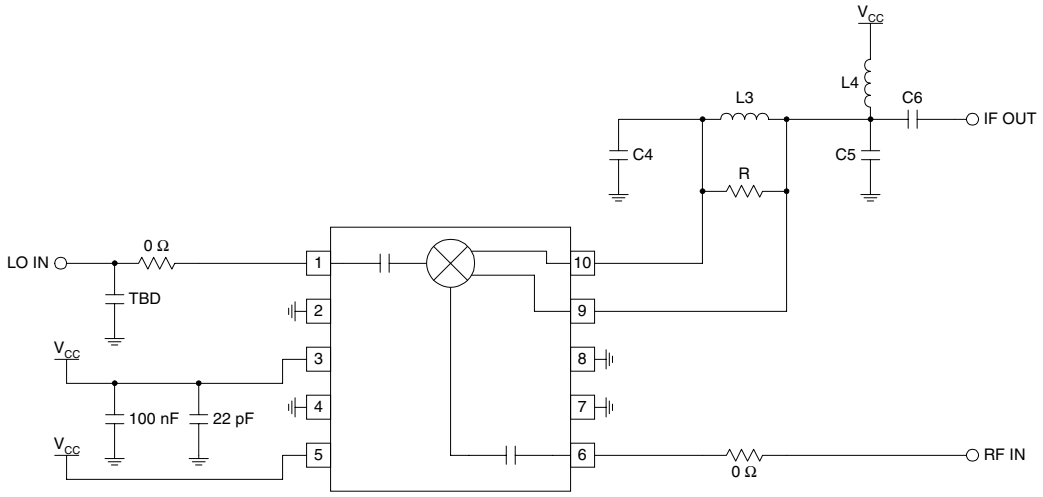
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=1959MHz, LO=1749MHz @ -2dBm
Usable RF Frequency Range	1500		2500	MHz	
Typical RF Frequency Range		1930 to 1990		MHz	
Usable LO Frequency Range	1200		2500	MHz	
Typical LO Frequency Range		1430 to 1990		MHz	
IF Frequency Range		DC to 500		MHz	
Noise Figure		10		dB	
Input VSWR		<2:1			Single-ended with external matching network.
Input IP3		+3		dBm	
Gain		+14		dB	
Output Impedance			1000	Ω	Single-ended with external matching network.
LO Input					
LO Input Range		-5 to +3		dBm	
LO to RF (Mix In) Rejection		45		dB	
LO to IF		47		dB	
LO Input VSWR		<2:1			Single-ended with external matching network.
Power Supply					
Voltage	2.7	3.0	3.6	V	
Current Consumption		38		mA	

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Pin	Function	Description	Interface Schematic
1	LO IN	Mixer LO single-ended input. The pin is internally DC blocked. External matching sets impedance.	
2	GND1	Ground for downconverter. Keep traces physically short and connect directly to ground plane for best performance.	
3	VCC1	Supply voltage for downconverter. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
4	GND2	Same as pin 2.	
5	VCC2		
6	RF IN	Mixer RF single-ended input. The pin is internally DC blocked. External matching sets input impedance.	
7	GND3	Same as pin 2.	
8	GND4	Same as pin 2.	
9	IF-	IF output pin. The output is balanced. A current combiner external network performs a differential to single-ended conversion and sets the output impedance. There must be a DC path from V_{CC} to this pin. this is normally achieved with the current combiner network. A DC blocking cap must be present if the IF filter input has a DC path to ground.	
10	IF+	Same as pin 7, except complementary output.	

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Application Schematic



Output Interface Network

L3, C4, C5, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C1 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 9 and 10. An average value to use for C_{EQ} is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L3.

C4 should be chosen as high as possible, while maintaining an R_P of L3 that allows for the desired R_{OUT}.

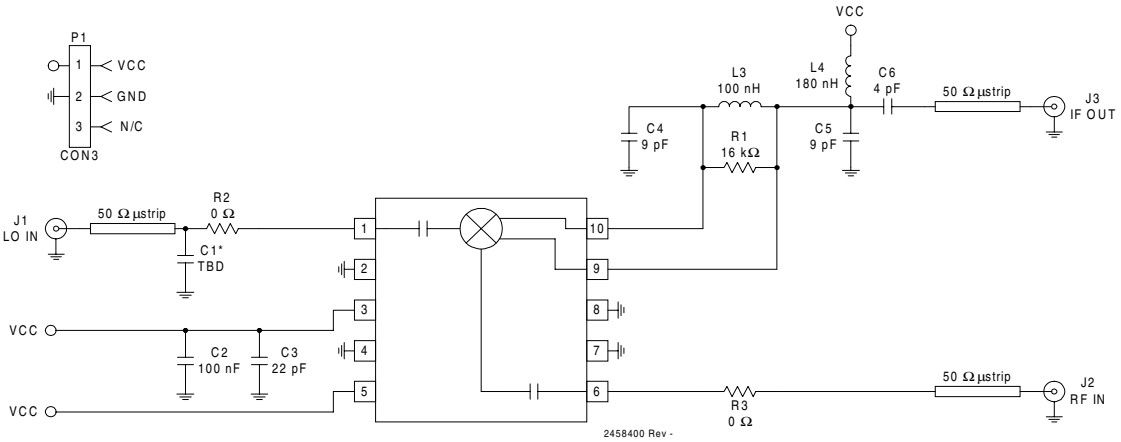
L2 and C2 serve dual purposes. L2 serves as an output bias choke, and C2 serves as a series DC block.

In addition, L2 and C2 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to ROUT. Otherwise, L2 is chosen to be large (suggested 8.2nH) and C2 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

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Evaluation Board Schematic
RF=1.959MHz, IF=210MHz

(Download Bill of Materials from www.rfmd.com.)



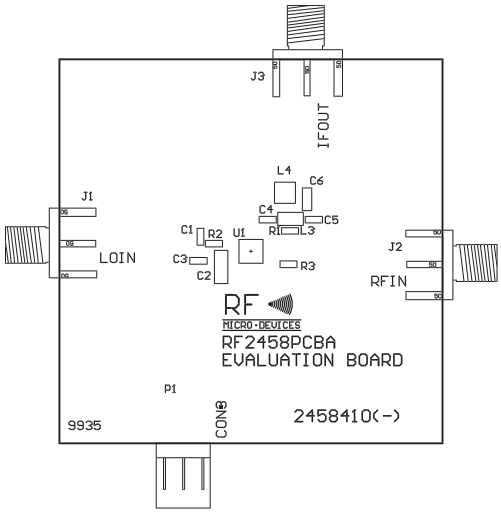
NOTES:
1) R1, L3, C4, and C5 are chosen to produce an output impedance, R_{OUT}, of 1000 Ω @ 210 MHz.
2) L4 and C7 are chosen to match the 1000 Ω output impedance to 50 Ω for testing purposes.

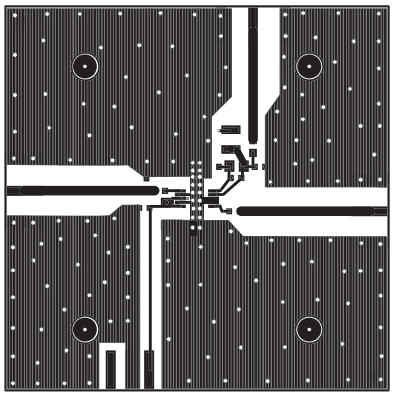
* Denotes component not populated on evaluation board.

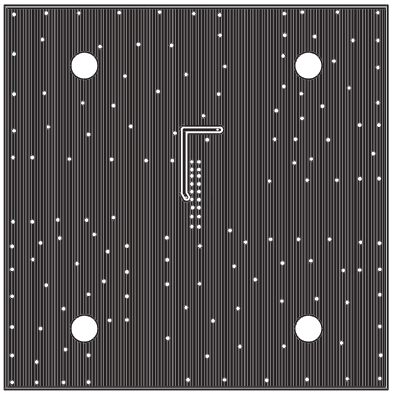
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Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.031", Board Material G-10







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RF MICRO·DEVICES

Preliminary

RF2459

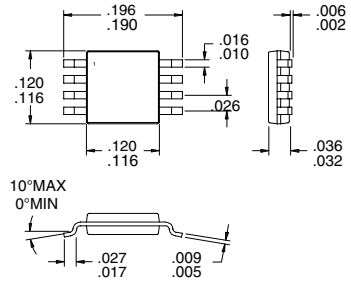
3V PCS DOWNCONVERTER

Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- General Purpose Downconverter
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

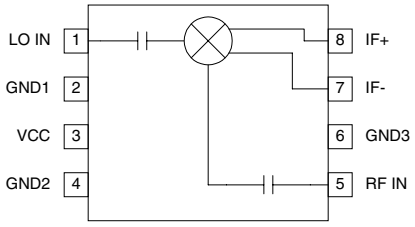
The RF2459 is a monolithic integrated downconverter for PCS, PHS, and WLAN applications. The IC contains all of the required components to implement the RF functions of the downconverter. It contains a double-balanced Gilbert cell mixer and a balanced IF output. The mixer's high third-order intercept point makes it ideal for digital cellular applications. The IC is designed to operate from a single 3V power supply.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: MSOP-8



Functional Block Diagram

Features

- Extremely High Dynamic Range
- Single 3V Power Supply
- 1500MHz to 2500MHz Operation

Ordering Information

RF2459	3V PCS Downconverter
RF2459 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8

FRONT-ENDS

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Absolute Maximum Ratings

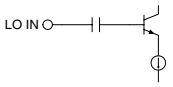
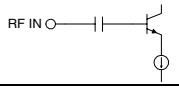
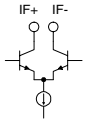
Parameter	Ratings	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

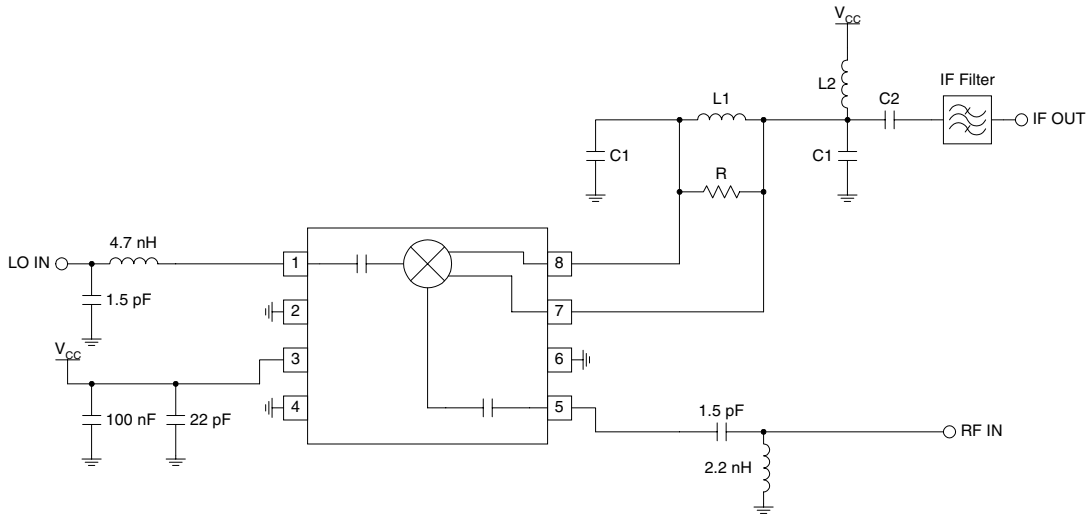
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=1960MHz, LO=1750MHz@-2dBm
Usable RF Frequency Range	1500		2500	MHz	
Typical RF Frequency Range		1930 to 1990		MHz	
Usable LO Frequency Range	1200		2500	MHz	
Typical LO Frequency Range		1430 to 1990		MHz	
IF Frequency Range		DC to 500		MHz	
Noise Figure		14		dB	
Input VSWR		<2:1			Single-ended with external matching network.
Input IP3		+7		dBm	
Gain	8.6	10		dB	
Output Impedance			1000	Ω	Single-ended with external matching network.
Input P1dB		-7.5		dBm	
LO Input					
LO Input Range		-5 to +3		dBm	
LO to RF (Mix In) Rejection		30		dB	
LO to IF		40		dB	
LO Input VSWR		<2:1			Single-ended with external matching network.
Power Supply					
Voltage	2.7	3.0	3.6	V	
Current Consumption		20		mA	

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Pin	Function	Description	Interface Schematic
1	LO IN	Mixer LO single-ended input. The pin is internally DC blocked. External matching sets impedance.	
2	GND1	Ground for downconverter. Keep traces physically short and connect directly to ground plane for best performance.	
3	VCC	Supply voltage for downconverter. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
4	GND2	Same as pin 2.	
5	RF IN	Mixer RF single-ended input. The pin is internally DC blocked. External matching sets input impedance.	
6	GND3	Same as pin 2.	
7	IF-	IF output pin. The output is balanced. A current combiner external network performs a differential to single-ended conversion and sets the output impedance. There must be a DC path from V_{CC} to this pin. this is normally achieved with the current combiner network. A DC blocking cap must be present if the IF filter input has a DC path to ground.	
8	IF+	Same as pin 7, except complementary output.	

Application Schematic



Output Interface Network

L1, C1 and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C1 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 7 and 8. An average value to use for C_{EQ} is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L1.

C1 should be chosen as high as possible, while maintaining an R_P of L1 that allows for the desired R_{OUT}.

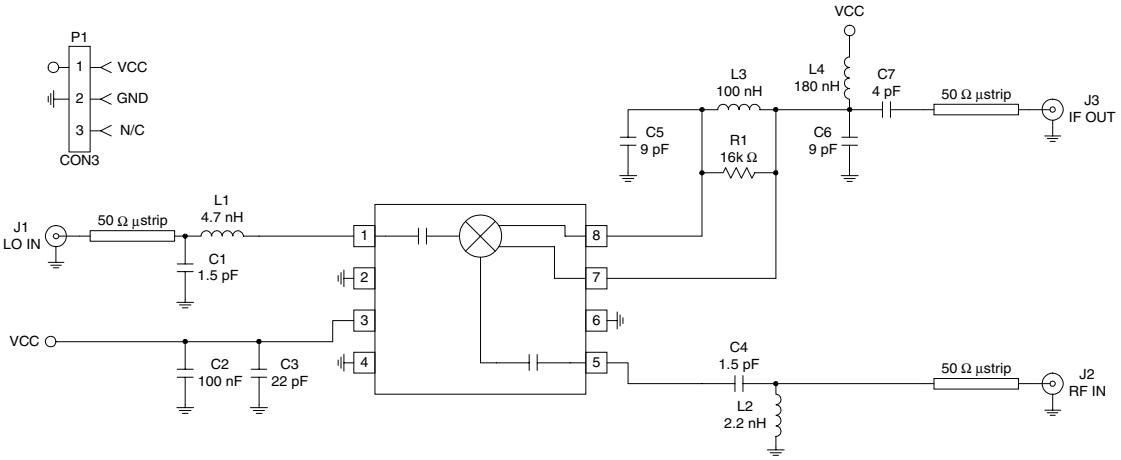
L2 and C2 serve dual purposes. L2 serves as an output bias choke, and C2 serves as a series DC block.

In addition, L2 and C2 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to ROUT. Otherwise, L2 is chosen to be large (suggested 8.2nH) and C2 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

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Evaluation Board Schematic
RF=1.959MHz, IF=210MHz

(Download Bill of Materials from www.rfmd.com.)

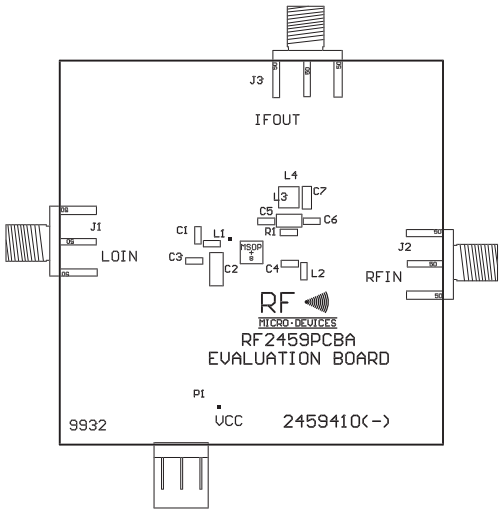


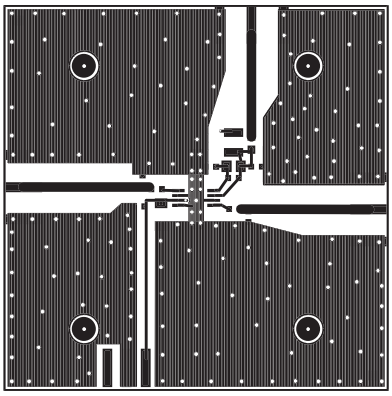
NOTES:
1) R1, L3, C5, and C6 are chosen to produce an output impedance, R_{OUT}, of 1000Ω @ 210 MHz.
2) L4 and C7 are chosen to match the 1000Ω output impedance to 50Ω for testing purposes.

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Evaluation Board Layout 900MHz
Board Size 2.0" x 2.0"

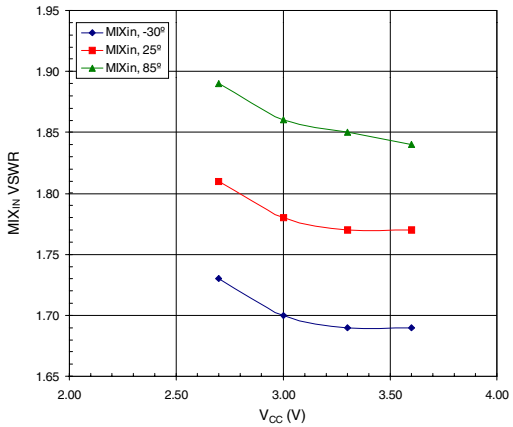
Board Thickness 0.031", Board Material FR-4



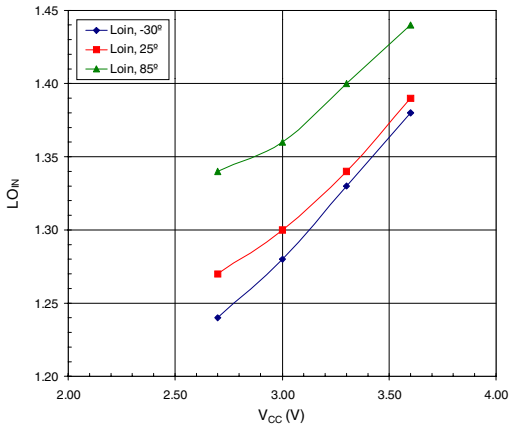


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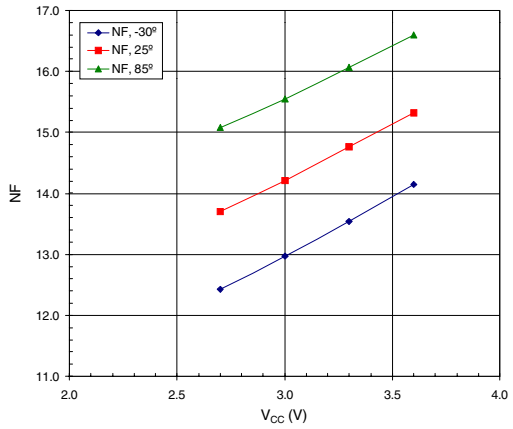
MIX_{IN} VSWR versus V_{CC}



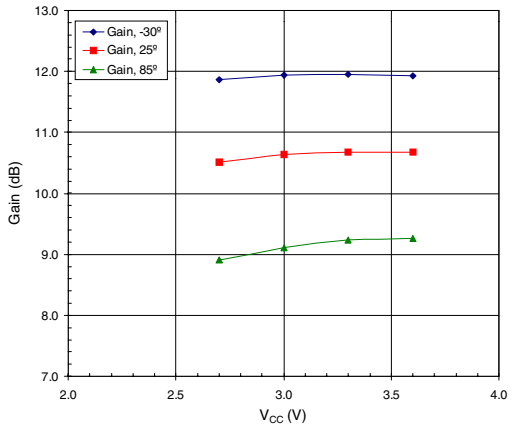
LO_{IN} VSWR versus V_{CC}



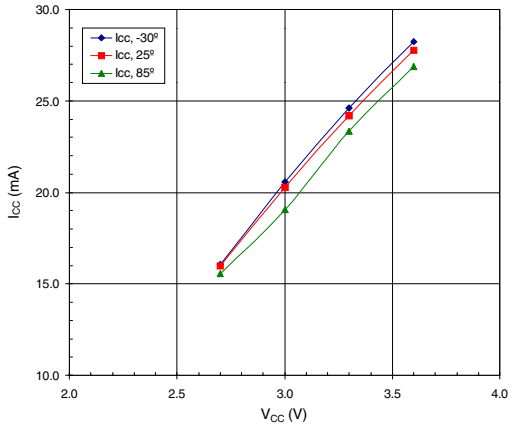
NF versus V_{CC}



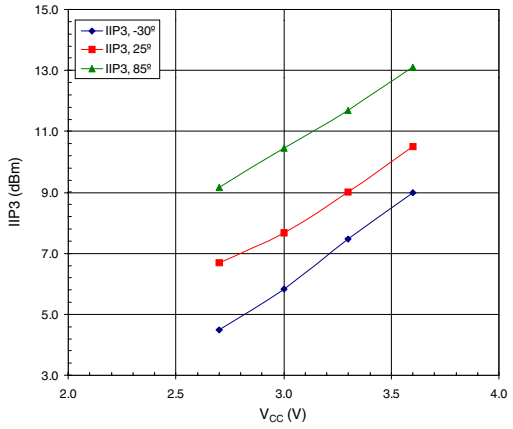
Gain versus V_{CC}



I_{CC} versus V_{CC}



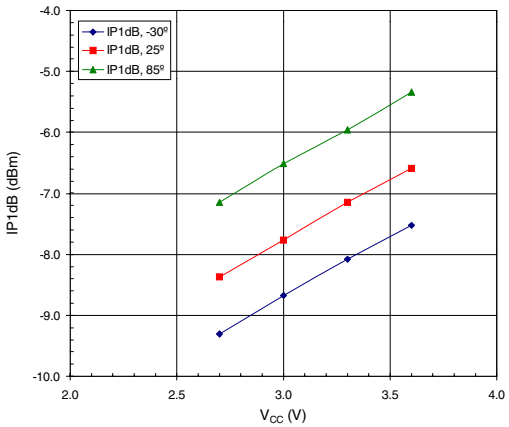
IIP3 versus V_{CC}



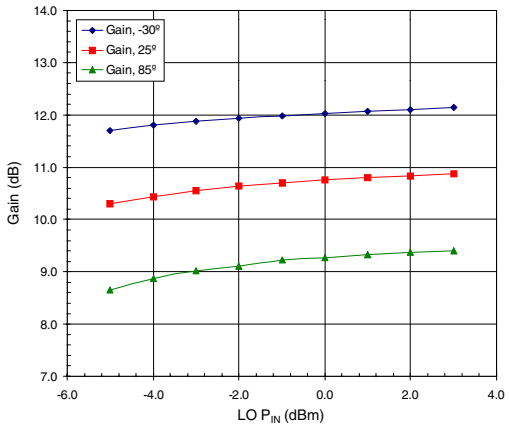
8

FRONT-ENDS

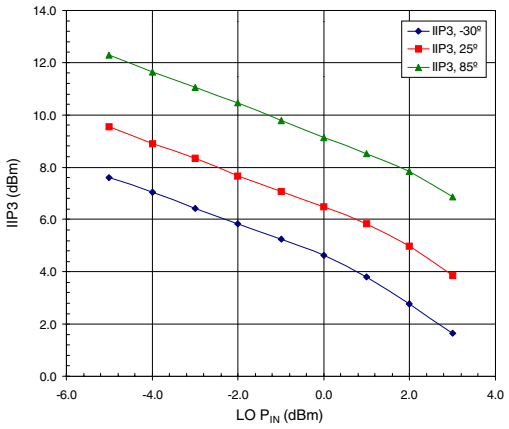
IP1dB versus V_{CC}



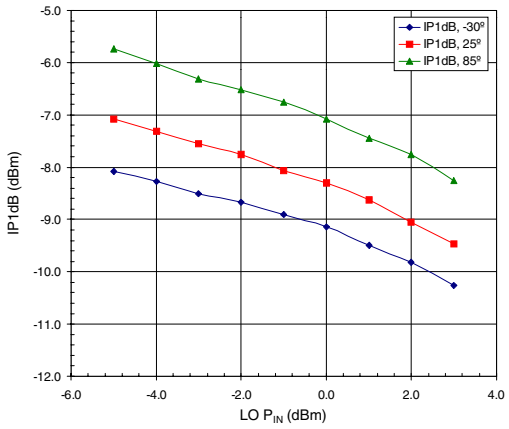
Gain versus LO P_{IN}



IIP3 versus LO P_{IN}



IP1dB versus LO P_{IN}



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RF2486

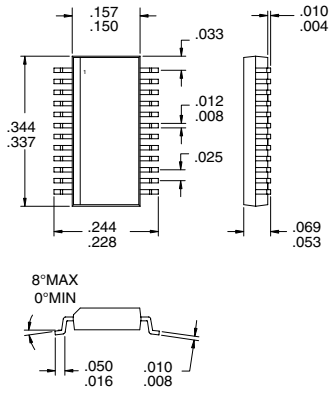
PCS LOW NOISE AMPLIFIER/MIXER

Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- General Purpose Down Converter
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

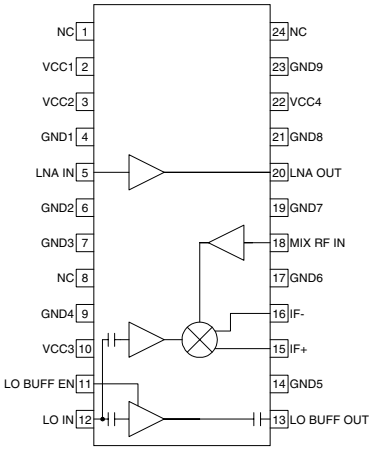
The RF2486 is a monolithic integrated receiver front-end for PCS, PHS, and WLAN applications. The IC contains all of the required components to implement the RF functions of the receiver front-end except for the passive filtering and LO generation. It contains an LNA (low-noise amplifiers), a double-balanced Gilbert cell mixer, a balanced IF output, an LO isolation buffer amplifier, and an LO output buffer amplifier for providing the buffered LO signal as an output. The IC is designed to operate from a single 3.6V power supply.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- High Dynamic Range
- Single 3.6V Power Supply
- External LNA IP3 Adjustment
- 1500MHz to 2500MHz Operation

Ordering Information

RF2486	PCS Low Noise Amplifier/Mixer
RF2486 PCBA-L	Fully Assembled Evaluation Board 1.96GHz
RF2486 PCBA-H	Fully Assembled Evaluation Board 2.4GHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

RF2486

Absolute Maximum Ratings

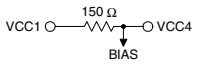
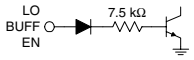
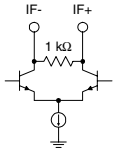
Parameter	Rating	Unit
Supply Voltage	-0.5 to 5.5	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

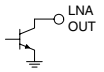
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

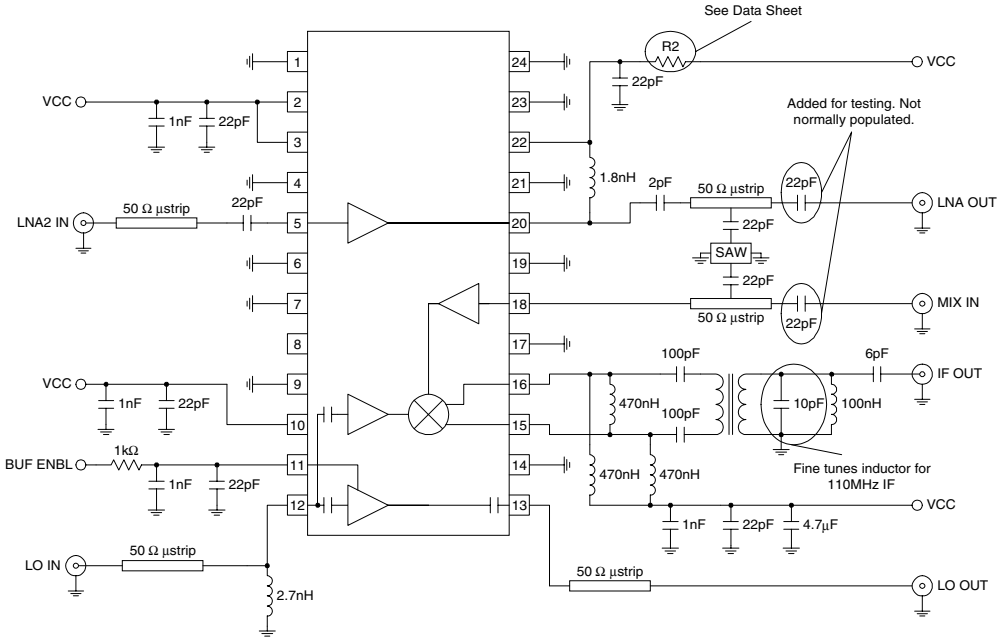
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=1959MHz, LO=1749MHz @ +1dBm
RF Frequency Range		1500 to 2500		MHz	
LO Frequency Range		1200 to 2500		MHz	
IF Frequency Range		DC to 500		MHz	
Cascaded Performance					1kΩ balanced load, 2.5dB Image Filter Loss.
Cascade Conversion Gain		26		dB	
Cascade Input IP3		-15		dBm	
Cascade Noise Figure		4.0		dB	Single Sideband
First Section (LNA)					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.8		dB	
Input VSWR		1.5:1	2.0:1		Input is internally matched for optimum noise figure from a 50Ω source.
Input IP3		+4		dBm	IP3 may be increased 10dB by connecting pin 22 to V_{CC} through the matching inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made. See pin description for pin 20. R2=Open
		+8.5		dBm	R2=Short
Gain		13.5		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			
Second Section (Mixer)					With 1kΩ balanced load.
Noise Figure		10		dB	Single Sideband
Input VSWR		1.5:1			
Input IP3		-5		dBm	
Conversion Gain		16		dB	
Output Impedance		1		kΩ	Balanced
LO Input					
LO Input Range		-3 to +3		dBm	
LO Output Level		-3		dBm	Buffer On, +1dBm input
		-22		dBm	Buffer Off, +1dBm input
LO to RF (Mix In) Rejection		30		dB	
LO to IF1, IF2 Rejection		20		dB	
LO Input VSWR		1.5:1			Single ended
Power Supply					
Voltage		2.7 to 5.0		V	
Current Consumption		7		mA	LNA only
		52		mA	LNA + Mixer, LO Buffer On
		48		mA	LNA + Mixer, LO Buffer Off

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Pin	Function	Description	Interface Schematic
1	NC	No Connection. This pin may be grounded (recommended) or left open.	
2	VCC1	Supply Voltage for the Mixer and RF Buffer Amplifier. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
3	VCC2	Supply Voltage for the LNA. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
4	GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA IN	RF Input pin for the LNA. This pin is internally matched for minimum noise figure (NOT for minimum VSWR), given a 50Ω source impedance.	
6	GND2	Same as pin 4.	
7	GND3	Ground connection for the RF Buffer Amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
8	NC	No Connection. This pin may be grounded (recommended) or left open.	
9	GND4	Same as pin 7.	
10	VCC3	Supply voltage for both LO buffer amplifiers. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	LO BUFF EN	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" (≥3.1V) turns the buffer amplifier on, and the current consumption increases by 3mA (with -2dBm LO input). A logic "low" (≤0.5V) turns the buffer amplifier off.	
12	LO IN	Mixer LO Input pin. This pin is internally DC blocked and matched to 50Ω.	
13	LO BUFF OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 11.	
14	GND5	Ground connection for both LO buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance.	
15	IF+	Open-collector IF Output pin. This is a balanced output. The output impedance is set by an internal 1000Ω resistor to pin 16. Thus the differential IF output impedance is 1000Ω. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
16	IF-	Same as pin 15, except complementary output.	See pin 15.
17	GND6	Ground connection for the Mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
18	MIX RF IN	Mixer RF Input Pin. This pin is internally DC blocked and matched to 50Ω.	
19	GND7	Same as pin 17.	

Pin	Function	Description	Interface Schematic
20	LNA OUT	LNA Output pin. This is an open-collector output. This pin is typically connected to pin 22 through a bias/matching inductor. This inductor, in conjunction with a series blocking/matching capacitor, forms a matching network to the 50Ω image filter and provides bias (see Application Example). The LNA's IP3 may be increased 10dB by connecting pin 20 to V_{CC} through the inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made by connecting resistance values between V_{CC} and the matching inductor. The two reference points for consideration are with 150Ω used, which is what connection to pin 22 achieves, the Input IP3 is +5.5dBm and the LNA I_{CC} is 5mA. Using no resistance, the Input IP3 is +15.5 dBm and the LNA I_{CC} is 15 mA. Desired operating points in between these values may be interpolated, roughly.	
21	GND8	Same as pin 17.	
22	VCC4	Output supply voltage for the LNA Output (pin 20). This pin is typically connected to pin 20 through a bias/matching inductor (see Application Example). External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	See pin 2.
23	GND9	Same as pin 17.	
24	NC	No Connection. This pin may be grounded (recommended) or left open.	

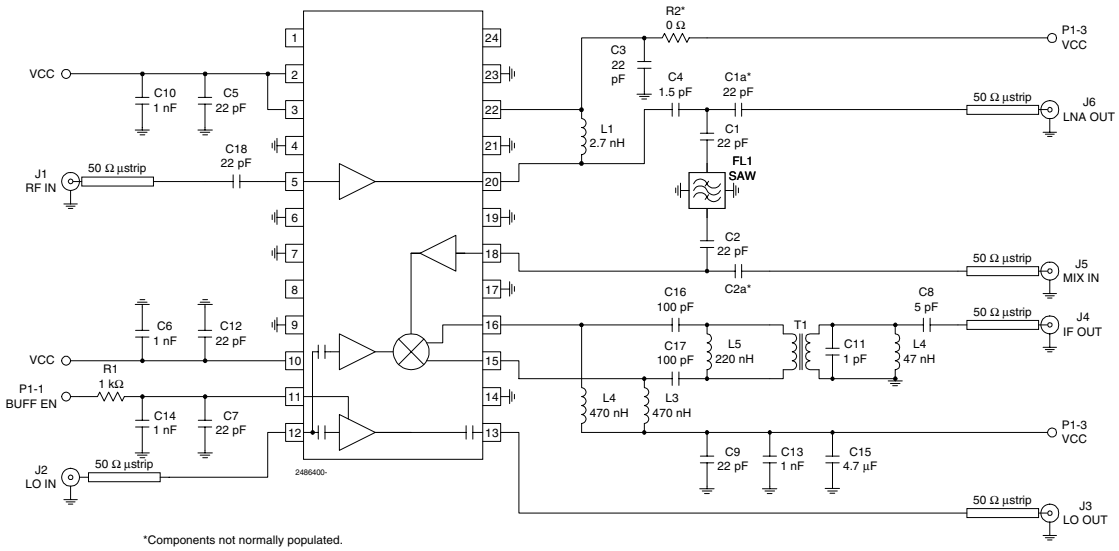
Application Schematic
1.96GHz, 210MHz IF



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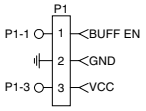
Evaluation Board Schematic
1.96GHz, 210MHz IF

(Download Bill of Materials from www.rfmd.com.)



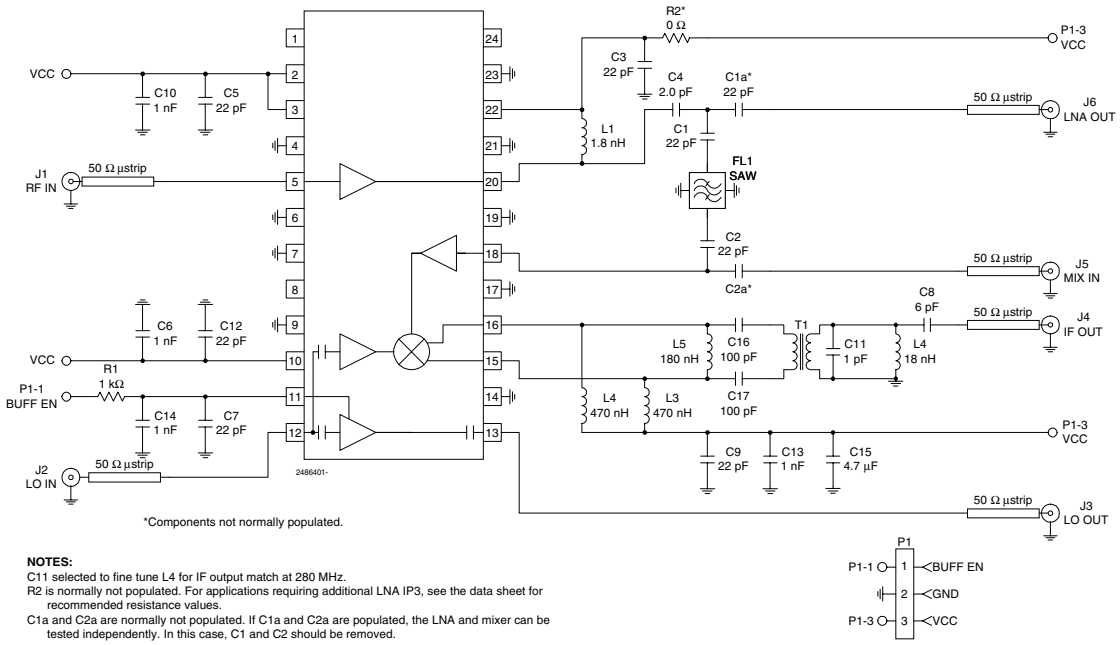
*Components not normally populated.

NOTES:
C11 selected to fine tune L4 for IF output match at 210 MHz.
R2 is normally not populated. For applications requiring additional LNA IP3, see the data sheet for recommended resistance values.
C1a and C2a are normally not populated. If C1a and C2a are populated, the LNA and mixer can be tested independently. In this case, C1 and C2 should be removed.



Evaluation Board Schematic
2.4GHz, 280MHz IF

(Download Bill of Materials from www.rfmd.com.)



*Components not normally populated.

NOTES:

C11 selected to fine tune L4 for IF output match at 280 MHz.

R2 is normally not populated. For applications requiring additional LNA IP3, see the data sheet for recommended resistance values.

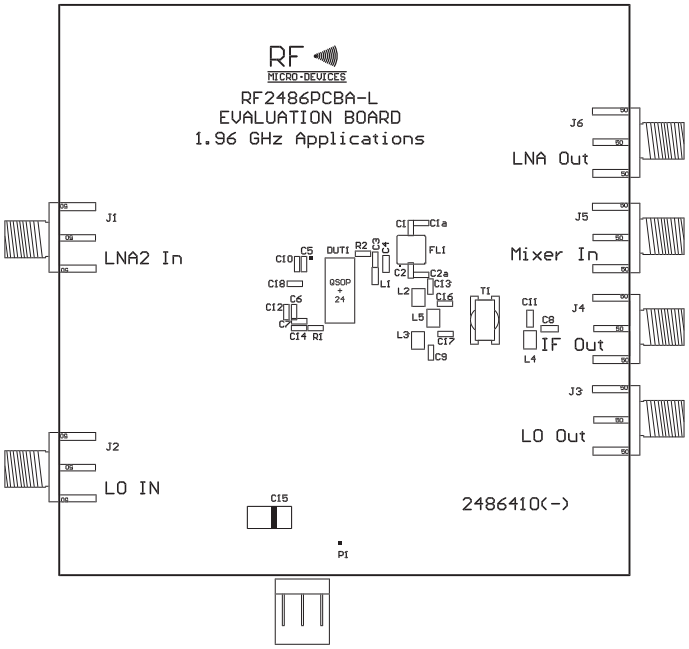
C1a and C2a are normally not populated. If C1a and C2a are populated, the LNA and mixer can be tested independently. In this case, C1 and C2 should be removed.

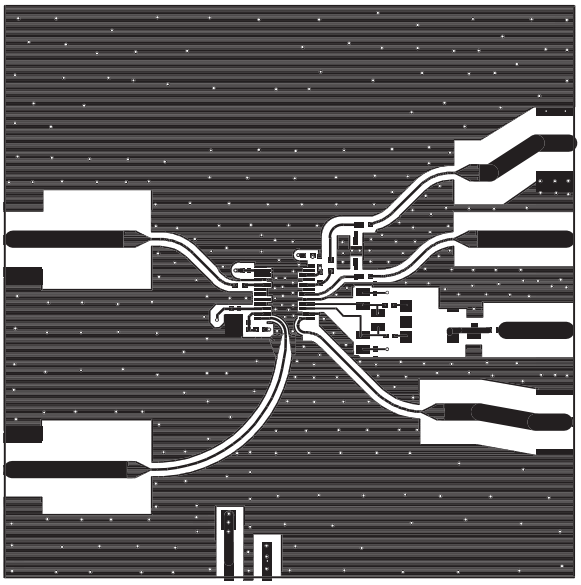
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Evaluation Board Layout 1.96GHz
Board Size 3.0” x 3.0”

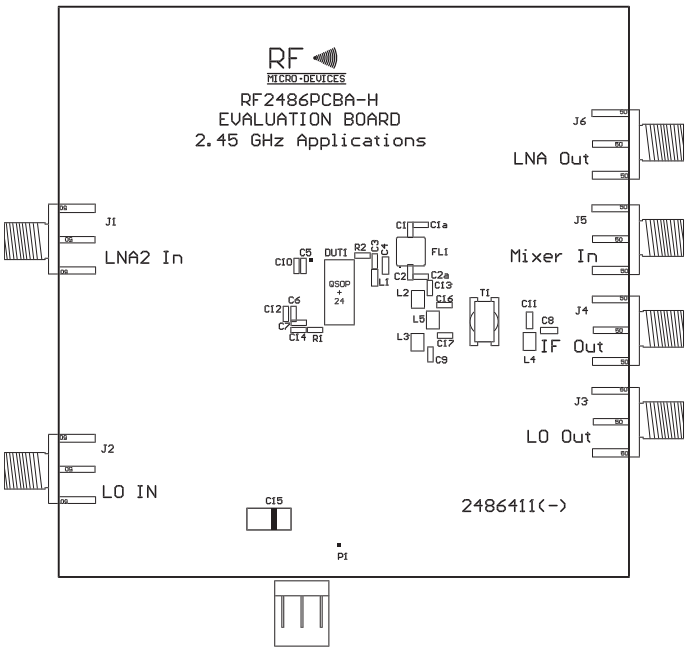
Board Thickness 0.075.6”, Board Material FR-4, Multi-Layer

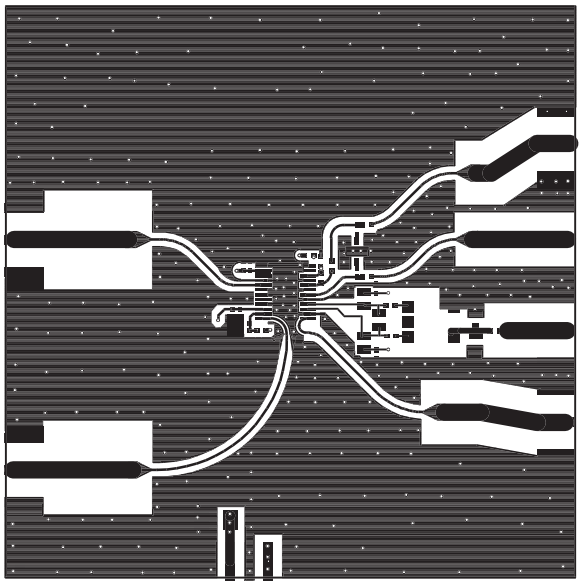
(8 mils between Layers 1 and 2, 31 mils between Layers 2 and 3, 1 ounce copper all layers)





Evaluation Board Layout 2.4GHz
Board Size 3.0” x 3.0”





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RF9906

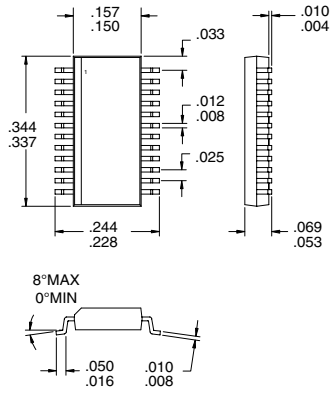
CDMA/FM LOW NOISE AMPLIFIER/MIXER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

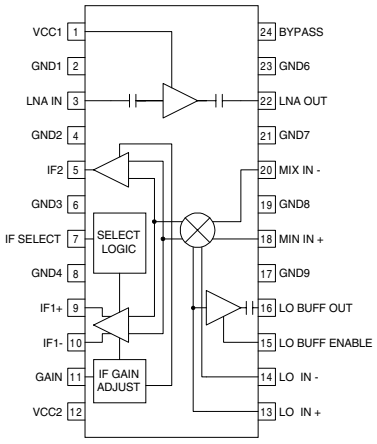
The RF9906 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals while providing 9dB of gain control range. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Receive LNA/Mixer, a Receive IF AGC Amp, a Transmit IF AGC Amp, and a Transmit Upconverter. The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and is packaged in a standard miniature 24-lead plastic SSOP package.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Analog Gain Control
- Single 3.6V Power Supply
- Buffered LO Output
- Digitally Selectable IF Outputs
- 500MHz to 1500MHz Operation

Ordering Information

RF9906	CDMA/FM Low Noise Amplifier/Mixer
RF9906 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF9906

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+3	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

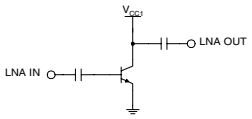
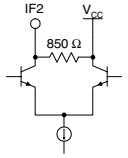
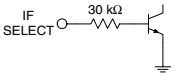
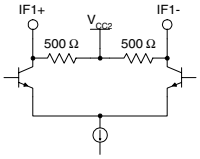
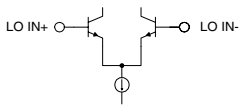
Caution! ESD sensitive device.

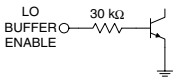
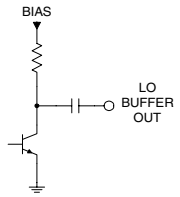
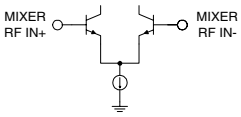
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=881MHz, LO=966MHz @ -5dBm
RF Frequency Range		500 to 1500		MHz	
LO Frequency Range		500 to 1500		MHz	
IF Frequency Range		0.1 to 250		MHz	
Cascaded Performance to IF1					CDMA Mode, IF SEL.=2.9V, 1kΩ balanced load, 2.5dB Image Filter Loss. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made.
Cascade Conversion Gain, Maximum	27.5	30	33	dB	V_G≤0.2V
Cascade Conversion Gain, Minimum		21		dB	V_G≥2.5V
Cascade IP3	-15	-13		dBm	Referenced to input at Maximum Gain
Cascade Noise Figure		2.6	3.4	dB	Single sideband, at Maximum Gain Setting
Cascaded Performance to IF2					FM Mode, IF SEL.=0V, 850Ω load, 2.5dB Image Filter Loss. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made.
Cascade Conversion Gain, Maximum	18.5	21	24	dB	V_G≤0.2V
Cascade Conversion Gain, Minimum		12		dB	V_G≥2.5V
Cascade IP3	-15	-12.5		dBm	Referenced to input at Maximum Gain
Cascade Noise Figure		3.0	4.0	dB	Single sideband, at Maximum Gain Setting
First Section (LNA)					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.5		dB	
Input VSWR		<1.5:1			
Input IP3		-8		dBm	
Gain		16		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			

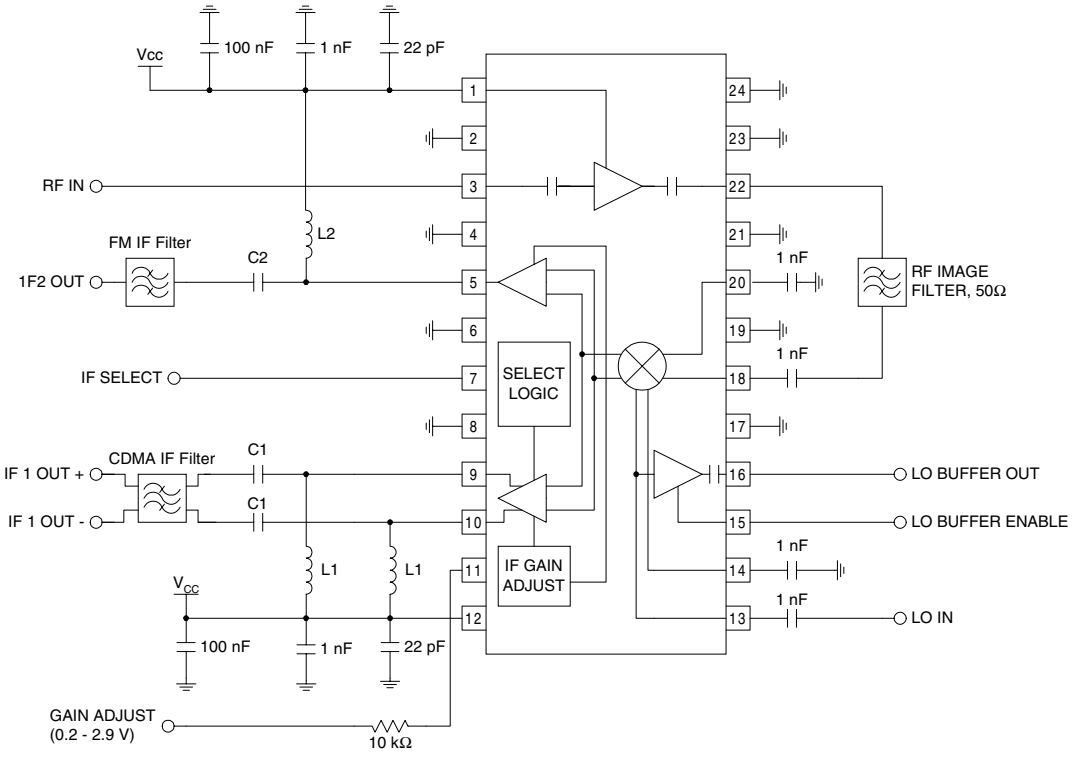
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Second Section (Mixer, IF1 Output)					With 1kΩ balanced load. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. Please see data plots.
Noise Figure		9.5		dB	Single Sideband
Input VSWR		1.5:1			Single-ended
Input IP3		+2		dBm	At maximum gain
Conversion Gain, Maximum		16.5		dB	$V_G \leq 0.2V$
Conversion Gain, Minimum		5.5		dB	$V_G \geq 2.5V$
Output Impedance		1		kΩ	Balanced
Second Section (Mixer, IF2 Output)					With 850Ω load. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. Please see data plots.
Noise Figure		11		dB	Single Sideband
Input VSWR		1.5:1			Single ended
Input IP3		+2		dBm	At maximum gain
Conversion Gain, Maximum		7.5		dB	$V_G \leq 0.2V$
Conversion Gain, Minimum		-4.5		dB	$V_G \geq 2.5V$
Output Impedance		850		Ω	Single ended
LO Input					
LO Input Range		-6 to 0		dBm	
LO Output Level	-7.5	-5	-2.5	dBm	Buffer On, -5dBm input
LO Output Level		-35	-30	dBm	Buffer Off, -5dBm input
LO to RF (Mix In) Rejection		27		dB	
LO to IF1, IF2 Rejection		20		dB	
LO Input VSWR		<2:1			Single ended
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		7		mA	LNA only
		41.5	58	mA	LNA + Mixer, IF1, LO Buffer On
		39	55	mA	LNA + Mixer, IF1, LO Buffer Off
		32.5	45	mA	LNA + Mixer, IF2, LO Buffer On
		30	42	mA	LNA + Mixer, IF2, LO Buffer Off

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LNA. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	LNA IN	RF input pin. This pin is internally DC blocked and matched to 50Ω.	
4	GND	Same as pin 2.	
5	IF2	FM IF output pin. This is a single-ended output with an output impedance set by an internal 850Ω resistor to V_{CC}. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to correctly bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
6	GND	Same as pin 2.	
7	IF SELECT	Selects which IF output (IF1 or IF2) is used. This is a digitally controlled input. A logic "high" selects IF1. A logic "low" selects IF2. The threshold voltage is approximately 1.3V.	
8	GND	Same as pin 2.	
9	IF 1+	CDMA IF output pin. This is a balanced output. The output impedance is set by an internal 500Ω resistor to V_{CC}. Thus the output impedance of each pin is 500Ω, whereas the differential output impedance is 1000Ω. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to correctly bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
10	IF 1-	Same as pin 9 except complementary input.	See pin 9.
11	GC	Analog gain adjustment for both IF output buffer amplifiers. A 10kΩ source impedance is required for proper operation of the gain control circuitry. Valid control voltages, on the source side of the 10kΩ resistor, are from 0V to 2.9V. Minimum gain is selected with 2.4V to 2.9V. Maximum gain is selected with 0V to 0.2V. When operating the RF9906 at fixed maximum gain, this pin should be grounded through a 10kΩ resistor. Do not connect this pin directly to ground (see Application Schematic for example).	
12	VCC2	Supply Voltage for the Mixer, LO Buffer Amplifier, and IF Buffer Amplifiers. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
13	LO IN+	Mixer LO Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other mixer LO input is AC coupled to ground. The single-ended input impedance is 50Ω.	
14	LO IN-	Same as pin 13, except complementary input.	See pin 13.

15	**LO BUFFER ENABLE**	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" turns the buffer amplifier on, and the current consumption increases by 3mA (with -3dBm LO input). A logic "low" turns the buffer amplifier off. The threshold voltage is approximately 1.3V.	
16	**LO BUFFER OUT**	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 15.	
17	**GND**	Same as pin 2.	
18	**MIXER RF IN+**	Mixer RF Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other mixer RF input is bypassed to ground. In order to minimize the mixer's noise figure, the bypass capacitor must be a low input impedance at the IF frequency. The single-ended input impedance is 50Ω.	
19	**GND**	Same as pin 2.	
20	**MIXER RF IN-**	Same as pin 18, except complementary input.	See pin 18.
21	**GND**	Same as pin 2.	
22	**LNA OUT**	LNA Output pin. This pin is internally DC blocked and matched to 50Ω in order to facilitate an easy interface to a 50Ω Image Filter.	See pin 3.
23	**GND**	Same as pin 2.	
24	**BYPASS**	IF circuitry bypass pin. This pin should be well bypassed at the IF frequency in order to achieve specified FM (IF2) noise figure. The ground side of the bypass capacitor should connect immediately to ground plane. 1000pF is the suggested value. Smaller values will begin to slightly degrade noise figure. Larger values will slow down the IF1 to IF2 switching times.	

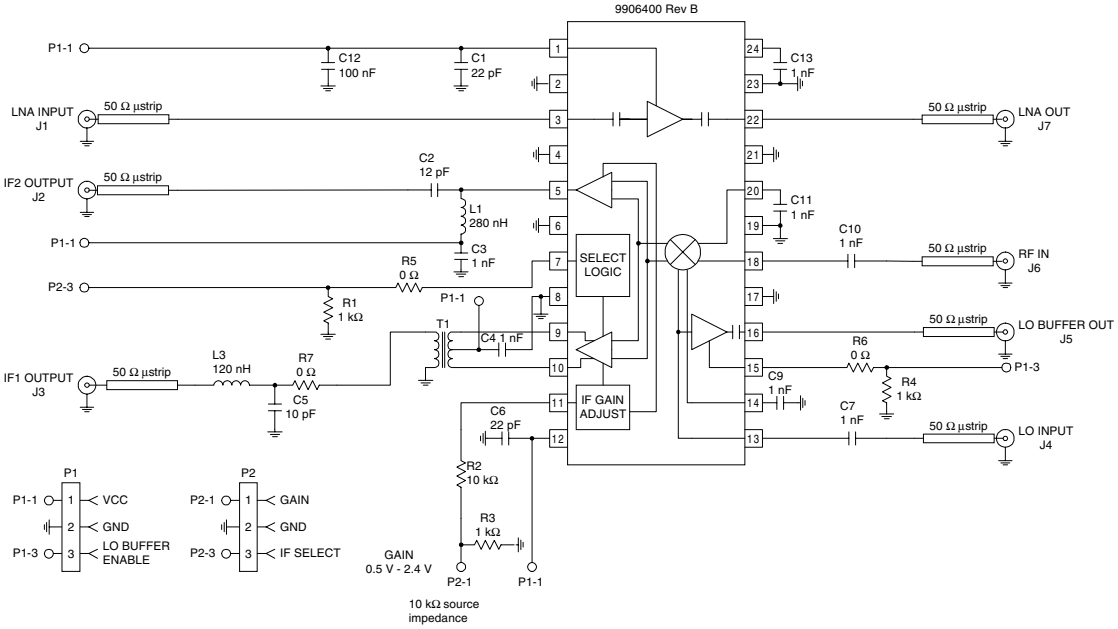
Application Schematic



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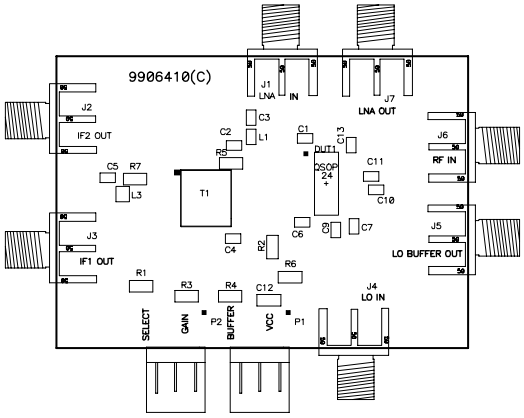
Evaluation Board Schematic

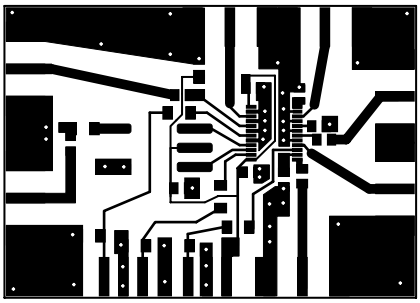
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout

Board Thickness 0.014”; Board Material FR-4 ????





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RF9936

PCS LOW NOISE AMPLIFIER/MIXER

Typical Applications

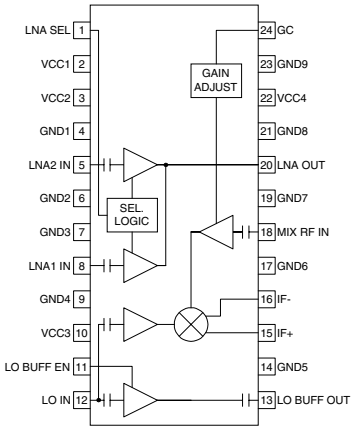
- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- Receivers Employing Diversity Antennas
- General Purpose Down Converter
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

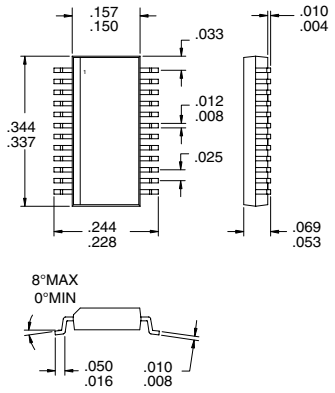
The RF9936 is a monolithic integrated receiver front-end for PCS applications. The IC contains all of the required components to implement the RF functions of the receiver front-end except for the passive filtering and LO generation. It contains two LNAs (low-noise amplifiers), a double-balanced Gilbert cell mixer, a balanced IF output, an LO isolation buffer amplifier, and an LO output buffer amplifier for providing the buffered LO signal as an output. On-chip digital logic is used to enable the appropriate LNA. The LNAs share a common output that permits insertion of a bandpass filter between the LNA output and the Mixer section. Analog gain adjustment is provided which allows 10dB variation in gain. The IC is designed to operate from a single 3.6V power supply.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-24

Features

- Complete Receiver Front-End
- Analog RF Gain Control
- Single 3.6V Power Supply
- Digitally Selectable LNA Inputs
- Digitally Selectable Buffered LO Output
- 1500MHz to 2500MHz Operation

Ordering Information

RF9936	PCS Low Noise Amplifier/Mixer
RF9936 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

8 FRONT-ENDS

RF9936

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

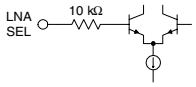
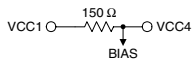
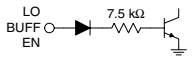
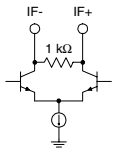
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

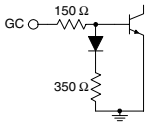
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=1959MHz, LO=1749MHz @ -2dBm
RF Frequency Range		1500 to 2500		MHz	
LO Frequency Range		1200 to 2500		MHz	
IF Frequency Range		DC to 500		MHz	
Cascaded Performance					1kΩ balanced load, 2.5dB Image Filter Loss. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made.
Cascade Conversion Gain, Maximum		27.5		dB	$V_G \leq 0.5V$
Cascade Conversion Gain, Minimum		15.5		dB	$V_G \geq 2.5V$
Cascade Input IP3		-14		dBm	Maximum Gain
		-9		dBm	Minimum Gain
Cascade Noise Figure		2.5		dB	Single sideband, at Maximum Gain Setting
		5.1		dB	Single sideband, at Minimum Gain Setting
First Section (LNA)					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.4		dB	
Input VSWR		<2.5:1			Input is internally matched for optimum noise figure from a 50Ω source.
Input IP3		+2		dBm	IP3 may be increased 10dB by connecting pin 22 to V_{CC} through the matching inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made. See pin description for pin 20.
Gain		13.5		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			
Second Section (Mixer)					With 1kΩ balanced load. By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. Please see data plots.
Noise Figure		6.5		dB	Single Sideband, at maximum gain
		13.5		dB	Single Sideband, at minimum gain
Input VSWR		1.5:1			
Input IP3		-3		dBm	At maximum gain
		+2		dBm	At minimum gain
Conversion Gain, Maximum		16		dB	$V_G \leq 0.2V$
Conversion Gain, Minimum		6		dB	$V_G \geq 2.5V$
Output Impedance		1		kΩ	Balanced

LO Input					
LO Input Range		-5 to +3		dBm	
LO Output Level		-5		dBm	Buffer On, -2dBm input
		-25		dBm	Buffer Off, -2dBm input
LO to RF (Mix In) Rejection		30		dB	
LO to IF1, IF2 Rejection		20		dB	
LO Input VSWR		<2:1			Single ended
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		5		mA	LNA only
		46	50	mA	LNA + Mixer, LO Buffer On
		43	47	mA	LNA + Mixer, LO Buffer Off

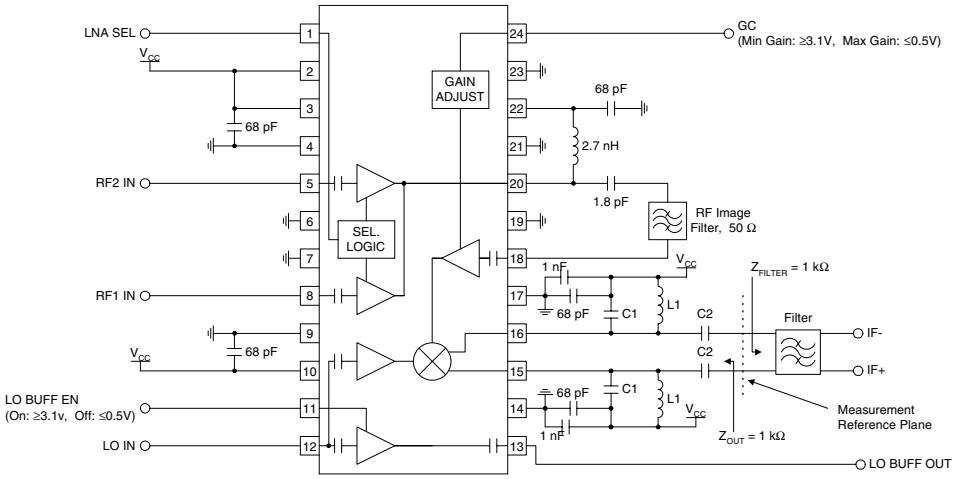
RF9936

Pin	Function	Description	Interface Schematic
1	LNA SEL	Selects which LNA (LNA1 or LNA2) is active. This is a digitally controlled input. A logic "high" (≥3.1V.) selects LNA2. A logic "low" (≤0.5V.) selects LNA1.	
2	VCC1	Supply Voltage for the Mixer and RF Buffer Amplifier. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
3	VCC2	Supply Voltage for the LNAs and associated select logic. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
4	GND1	Ground connection for LNA2. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA2 IN	RF Input pin for LNA2. This pin is internally DC blocked and internally matched for minimum noise figure (NOT for minimum VSWR), given a 50Ω source impedance.	
6	GND2	Same as pin 4.	
7	GND3	Ground connection for LNA1. Keep traces physically short and connect immediately to ground plane for best performance.	
8	LNA1 IN	RF Input pin for LNA1. This pin is internally DC blocked and internally matched for minimum noise figure (NOT for minimum VSWR), given a 50Ω source impedance.	
9	GND4	Same as pin 7.	
10	VCC3	Supply voltage for both LO buffer amplifiers. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	LO BUFF EN	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" (≥3.1V.) turns the buffer amplifier on, and the current consumption increases by 3mA (with -2dBm LO input). A logic "low" (≤0.5V.) turns the buffer amplifier off.	
12	LO IN	Mixer LO Input pin. This pin is internally DC blocked and matched to 50Ω.	
13	LO BUFF OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 11.	
14	GND5	Ground connection for both LO buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance.	
15	IF+	Open-collector IF Output pin. This is a balanced output. The output impedance is set by an internal 1000Ω resistor to pin 16. Thus the differential IF output impedance is 1000Ω. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
16	IF-	Same as pin 15, except complementary output.	See pin 15.
17	GND6	Ground connection for the Mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
18	MIX RF IN	Mixer RF Input Pin. This pin is internally DC blocked and matched to 50Ω.	
19	GND7	Same as pin 17.	

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20	**LNA OUT**	LNA Output pin. This is an open-collector output. This pin is typically connected to pin 22 through a bias/matching inductor. This inductor, in conjunction with a series blocking/matching capacitor, forms a matching network to the 50Ω image filter and provides bias (see Application Example). The LNA's IP3 may be increased 10dB by connecting pin 20 to V_{CC} through the inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made by connecting resistance values between V_{CC} and the matching inductor. The two reference points for consideration are with 150Ω used, which is what connection to pin 22 achieves, the Input IP3 is +2dBm and the LNA I_{CC} is 5mA. Using no resistance, the Input IP3 is +12 dBm and the LNA I_{CC} is 15 mA. Desired operating points in between these values may be interpolated, roughly.	
21	**GND8**	Same as pin 17.	
22	**VCC4**	Output supply voltage for the LNA Output (pin 20). This pin should NOT be connected to a voltage supply. This pin should be connected to pin 20 through a bias/matching inductor (see Application Example). External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	See pin 2.
23	**GND9**	Same as pin 17.	
24	**GC**	Analog gain adjustment for RF buffer amplifier. Minimum gain is selected with 2.5V to 3.0V. Maximum gain is selected with 0V to 0.5 V. When operating the RF9936 at fixed maximum gain, this pin may be grounded.	

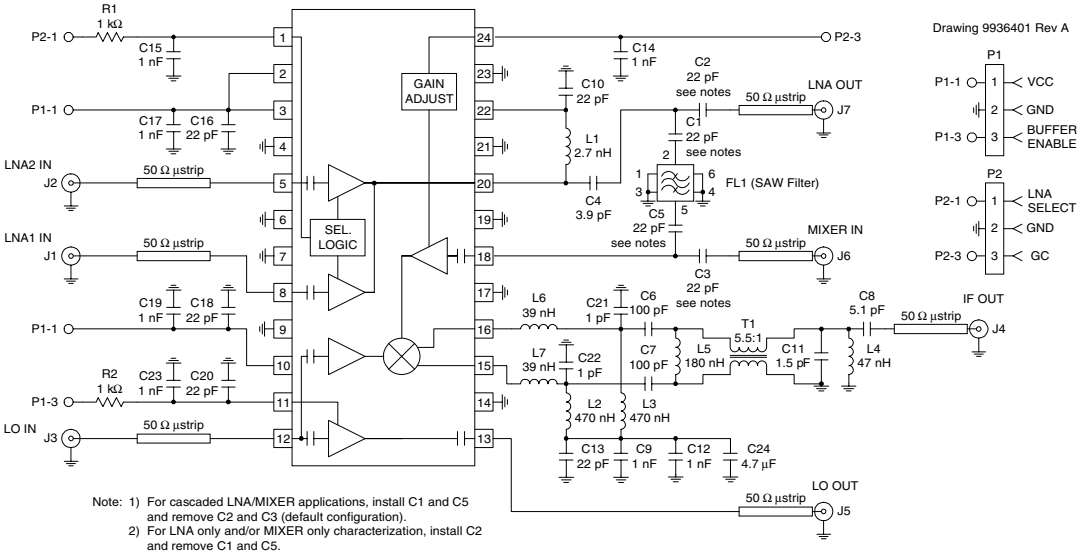
Application Schematic



L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the IF filter's input impedance is not 100 Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 100 Ω.

Evaluation Board Schematic
IF 210MHz

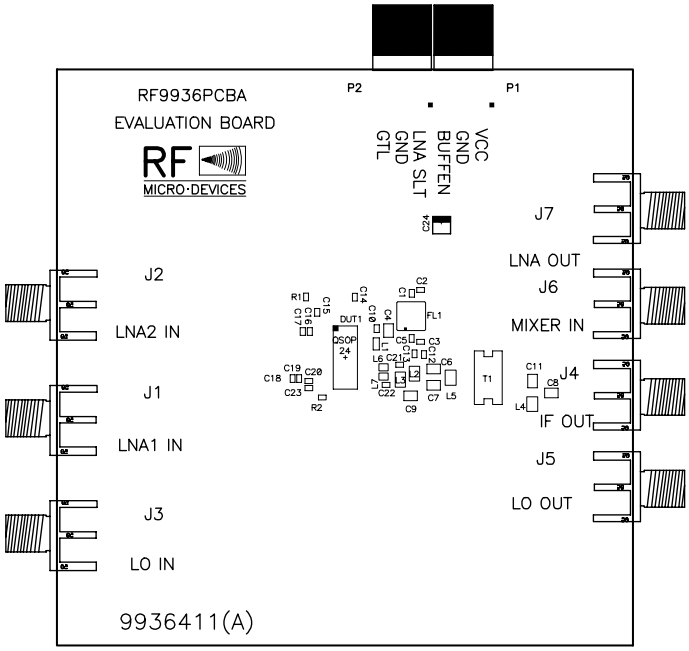
(Download Bill of Materials from www.rfmd.com.)

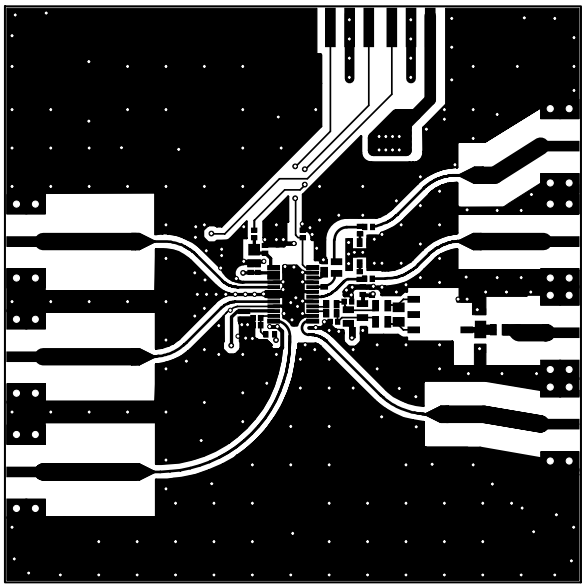


Note: 1) For cascaded LNA/MIXER applications, install C1 and C5 and remove C2 and C3 (default configuration).
2) For LNA only and/or MIXER only characterization, install C2 and remove C1 and C5.
3) L5 select value 180 nH to 220 nH.
4) Do not install C2, C3 in normal cascade operation.

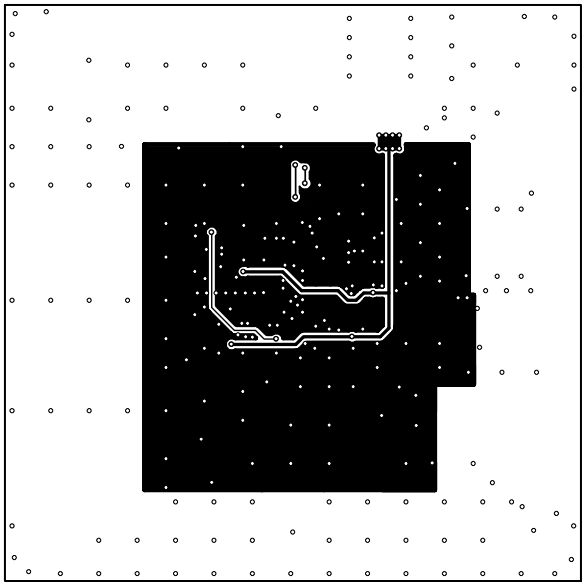
Evaluation Board Layout

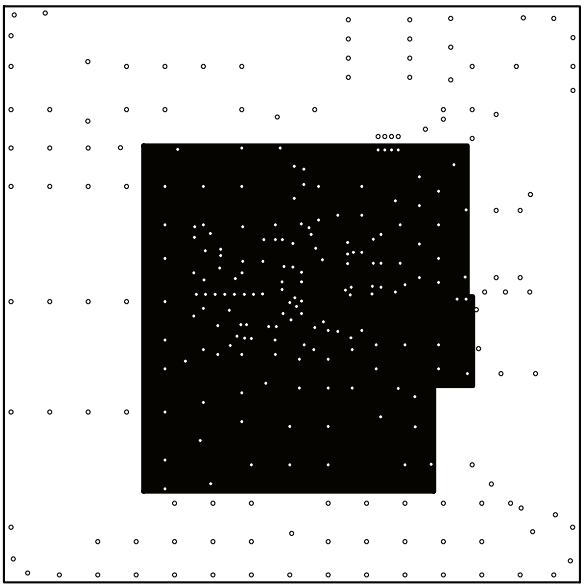
(Assembly, Top layer, Mid-signal layer, Internal Ground layer)





Evaluation Board Layout cont'd





RF9936

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RF9986

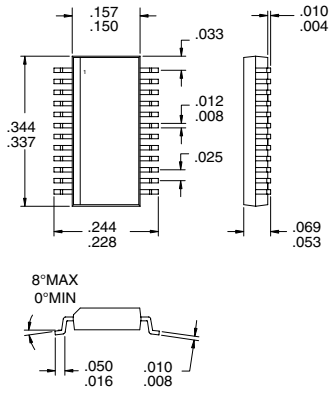
PCS LOW NOISE AMPLIFIER/MIXER

Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- General Purpose Down Converter
- Micro-Cell PCS Base Stations
- Portable Battery Powered Equipment

Product Description

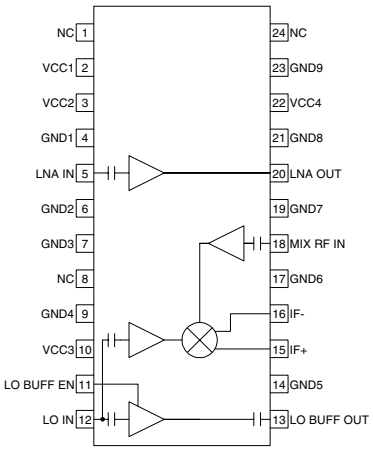
The RF9986 is a monolithic integrated receiver front-end for PCS, PHS, and WLAN applications. The IC contains all of the required components to implement the RF functions of the receiver front-end except for the passive filtering and LO generation. It contains an LNA (low-noise amplifiers), a double-balanced Gilbert cell mixer, a balanced IF output, an LO isolation buffer amplifier, and an LO output buffer amplifier for providing the buffered LO signal as an output. The IC is designed to operate from a single 3.6V power supply.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Extremely High Dynamic Range
- Single 3.6V Power Supply
- External LNA IP3 Adjustment
- 1500MHz to 2500MHz Operation

Ordering Information

RF9986	PCS Low Noise Amplifier/Mixer
RF9986 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF9986

Absolute Maximum Ratings

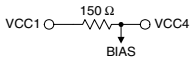
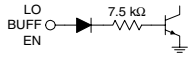
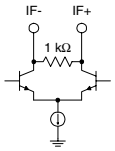
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

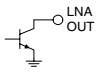
Caution! ESD sensitive device.

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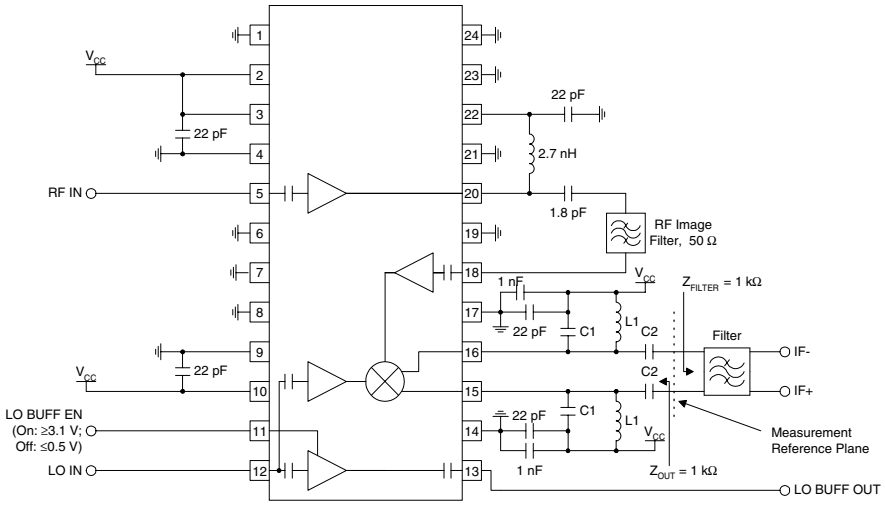
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, RF=1959MHz, LO=1749MHz @ -2dBm
RF Frequency Range		1500 to 2500		MHz	
LO Frequency Range		1200 to 2500		MHz	
IF Frequency Range		DC to 500		MHz	
Cascaded Performance					1kΩ balanced load, 2.5dB Image Filter Loss.
Cascade Conversion Gain		25		dB	
Cascade Input IP3		-10		dBm	
Cascade Noise Figure		2.5		dB	Single Sideband
First Section (LNA)					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.4		dB	
Input VSWR		<2:1			Input is internally matched for optimum noise figure from a 50Ω source.
Input IP3		+5.5		dBm	IP3 may be increased 10dB by connecting pin 22 to V_{CC} through the matching inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made. See pin description for pin 20.
Gain		12		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			
Second Section (Mixer)					With 1kΩ balanced load.
Noise Figure		5.5		dB	Single Sideband
Input VSWR		1.5:1			
Input IP3		-0.5		dBm	
Conversion Gain		15.5		dB	
Output Impedance		1		kΩ	Balanced
LO Input					
LO Input Range		-5 to +3		dBm	
LO Output Level		-4		dBm	Buffer On, -2dBm input
		-25		dBm	Buffer Off, -2dBm input
LO to RF (Mix In) Rejection		30		dB	
LO to IF1, IF2 Rejection		20		dB	
LO Input VSWR		<2:1			Single ended
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		5		mA	LNA only
		52		mA	LNA + Mixer, LO Buffer On
		48		mA	LNA + Mixer, LO Buffer Off

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Pin	Function	Description	Interface Schematic
1	NC	No Connection. This pin may be grounded (recommended) or left open.	
2	VCC1	Supply Voltage for the Mixer and RF Buffer Amplifier. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
3	VCC2	Supply Voltage for the LNA. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
4	GND1	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA IN	RF Input pin for the LNA. This pin is internally DC blocked and internally matched for minimum noise figure (NOT for minimum VSWR), given a 50Ω source impedance.	
6	GND2	Same as pin 4.	
7	GND3	Ground connection for the RF Buffer Amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
8	NC	No Connection. This pin may be grounded (recommended) or left open.	
9	GND4	Same as pin 7.	
10	VCC3	Supply voltage for both LO buffer amplifiers. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	LO BUFF EN	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" (≥3.1V) turns the buffer amplifier on, and the current consumption increases by 3mA (with -2dBm LO input). A logic "low" (≤0.5V) turns the buffer amplifier off.	
12	LO IN	Mixer LO Input pin. This pin is internally DC blocked and matched to 50Ω.	
13	LO BUFF OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 11.	
14	GND5	Ground connection for both LO buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance.	
15	IF+	Open-collector IF Output pin. This is a balanced output. The output impedance is set by an internal 1000Ω resistor to pin 16. Thus the differential IF output impedance is 1000Ω. The resistor sets the operating impedance, but an external choke or matching inductor to V_{CC} must be supplied in order to bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
16	IF-	Same as pin 15, except complementary output.	See pin 15.
17	GND6	Ground connection for the Mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
18	MIX RF IN	Mixer RF Input Pin. This pin is internally DC blocked and matched to 50Ω.	
19	GND7	Same as pin 17.	

20	**LNA OUT**	LNA Output pin. This is an open-collector output. This pin is typically connected to pin 22 through a bias/matching inductor. This inductor, in conjunction with a series blocking/matching capacitor, forms a matching network to the 50Ω image filter and provides bias (see Application Example). The LNA's IP3 may be increased 10dB by connecting pin 20 to V_{CC} through the inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I_{CC} trade-offs may be made by connecting resistance values between V_{CC} and the matching inductor. The two reference points for consideration are with 150Ω used, which is what connection to pin 22 achieves, the Input IP3 is +5.5dBm and the LNA I_{CC} is 5mA. Using no resistance, the Input IP3 is +15.5 dBm and the LNA I_{CC} is 15 mA. Desired operating points in between these values may be interpolated, roughly.	
21	**GND8**	Same as pin 17.	
22	**VCC4**	Output supply voltage for the LNA Output (pin 20). This pin is typically connected to pin 20 through a bias/matching inductor (see Application Example). External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	See pin 2.
23	**GND9**	Same as pin 17.	
24	**NC**	No Connection. This pin may be grounded (recommended) or left open.	

Application Schematic

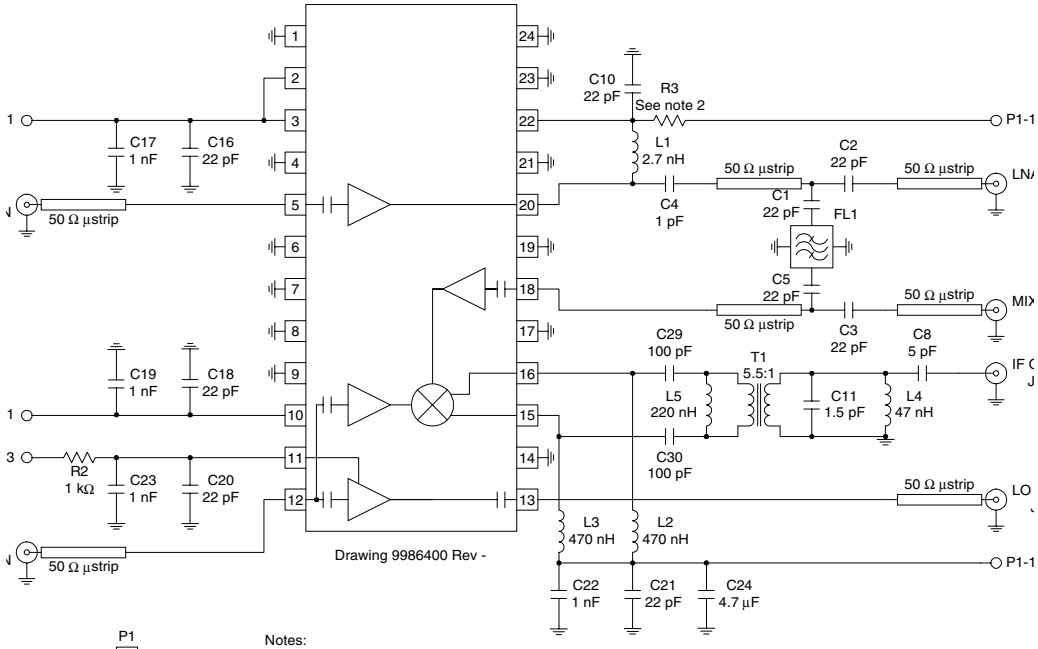


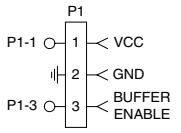
L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the IF filter's input impedance is not 100Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circut at the IF when the IF filter's input impedance is 1000Ω.

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Evaluation Board Schematic (IF=210MHz)

(Download Bill of Materials from www.rfmd.com.)



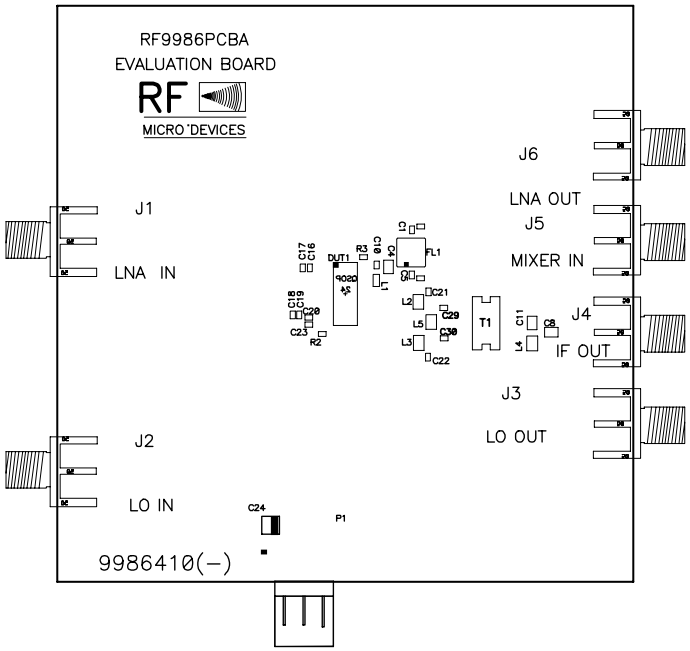


Notes:

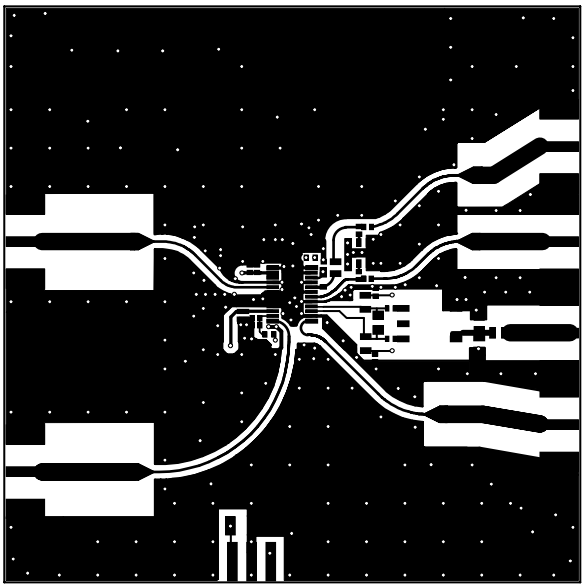
1. C11 is selected to fine tune L4 for IF output match at 210 MHz.
2. R3 is not normally populated. For applications requiring additional LNA IP3, see the data sheet for recommended resistance values.
3: C2 and C3 are not normally populated. If C2 and C3 are populated, the LNA and mixer can be tested independently; in this case, C1 and C5 should be removed.

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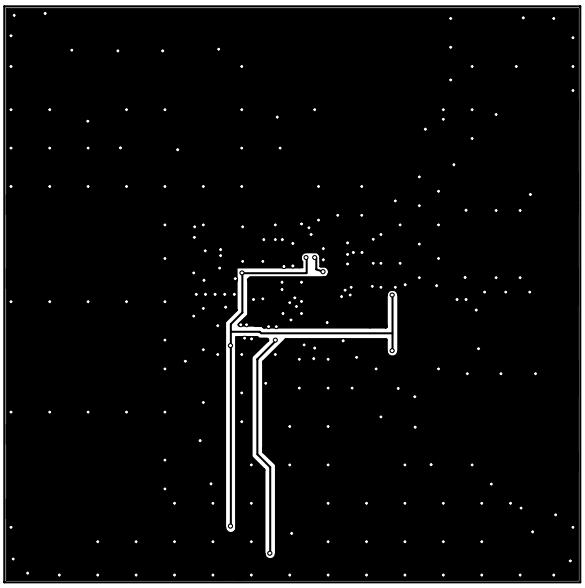
Evaluation Board Layout
3” x 3”
Assembly



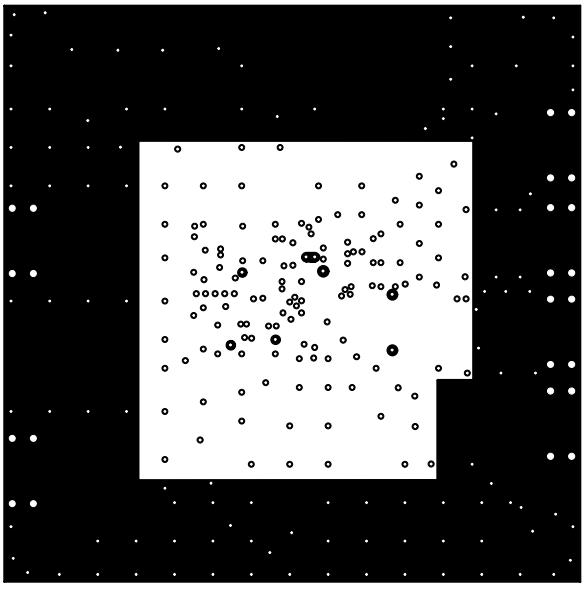
Top layer



Bottom Layer



Internal Ground



RF9986

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9 Attenuators and Switches

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Ins. Loss (dB)	Attn. Range/ Isolation (dB)	Attn. Step (dB)	Package	Page
RF2410	UHF Programmable Attenuator	500 to 2100	5	6	4.0	38	2	SOP-16	9-1
RF2420	Programmable Attenuator	DC to 950	3 to 6	4	4.0	44	2	SOP-16	9-9
RF2421	10dB Switched Attenuator	500 to 3000	2.7 to 6	0.5	1.0	10	10	SOP-8	9-15
RF2425	4-Port Transfer Switch	800 to 2000	2.7 to 6	1.5	0.6	23	n/a	SOP-8	9-19
RF2436	Transmit/Receive Switch	100 to 2500	2.7 to 6	1.5	0.5	24	n/a	SOT-23-5	9-23

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RF2410

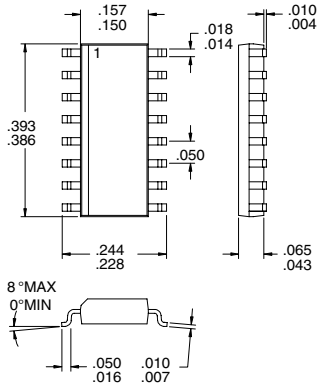
UHF PROGRAMMABLE ATTENUATOR

Typical Applications

- Power Control in Communication Systems
- CMOS Compatible Programmable Attenuators
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

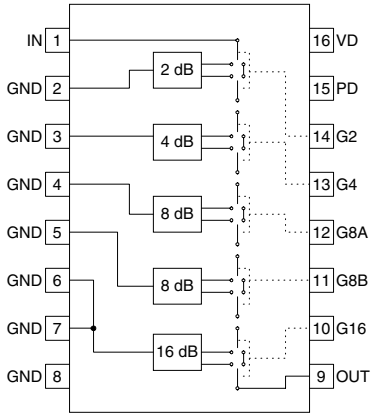
The RF2410 is a multistage monolithic programmable attenuator. The device is built using a Gallium Arsenide process technology and has an attenuation programmability over a 38dB range in 2dB steps. The attenuation is set by five bits of digital data. The input and output of the device have a low VSWR 50Ω match. The RF output can drive up to +10dBm. This unit is intended for use in systems that require RF transmit power control by digital means. A typical application is in dual mode IS-54/55 compatible cellular transceivers. No negative supply voltages are required, and the unit has a power down feature which reduces the current consumption to less than 0.5mA.



Package Style: SOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 5V Supply
- 0dB to 38dB Attenuation Range
- 4 dB Insertion Loss
- 5-bit Digitally Controlled Attenuation
- Digitally Controlled Power Down Mode
- 500MHz to 2100MHz Operation

Ordering Information

RF2410	UHF Programmable Attenuator
RF2410 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2410

Absolute Maximum Ratings

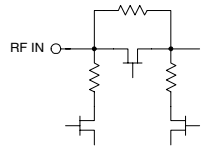
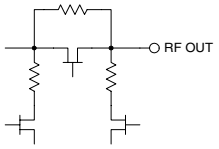
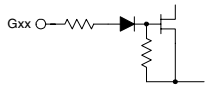
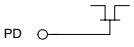
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Power Down Voltage	-0.5 to V_{DD}+0.4	V_{DC}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C and 5V at 900MHz
Frequency Range		500 to 1000		MHz	0dB to 38dB Attenuation Range
Frequency Range		500 to 2100		MHz	0dB to 20dB Attenuation Range
Insertion Loss		4	5.5	dB	
Attenuation Range		0 to 38		dB	
Gain Flatness		0.25		dB	In any 50MHz band
Input					
Input Impedance		50		Ω	
Input VSWR		1.3:1			
Input 1dB Compression	10	14		dBm	
Attenuation					
Attenuation Settings		2, 4, 8, 8, 16		dB	CMOS Level, 5 bits
Accuracy	1.0	2.0	3.2	dB	2dB Step
	2.9	4.0	5.4	dB	4dB Step
	6.7	8.0	9.8	dB	8dB Step (A)
	6.4	8.0	10.5	dB	8dB Step (B)
	14.1	16.0	19.3	dB	16dB Step
	35.0	38.0	42.0	dB	All bits on
Attenuation Control					
Attenuation "ON" Voltage	2.5	V_{DD}		V	Voltage Supplied to input
Attenuation "OFF" Voltage			0.3	V	Voltage Supplied to input
Current		0.4	1.0	mA	Into each control line
Response Time		<10		ns	
Output					
IM3	-30			dBc	With 0dBm output in each of 2 tones
Harmonic Output	-40			dBc	
Output Impedance		50		Ω	
Output VSWR		1.3:1			
Power Supply					
Voltage		5		V	Specifications
		4.5 to 6.0		V	Operating Limits
Current		6	12	mA	Operating
		0.4	0.75	mA	Power Down
Power Down					
Power "ON" Voltage	2.5	V_{DD}		V	Voltage supplied to input; device is "ON"
Power "OFF" Voltage			0.3	V	Voltage supplied to input; device is "OFF"

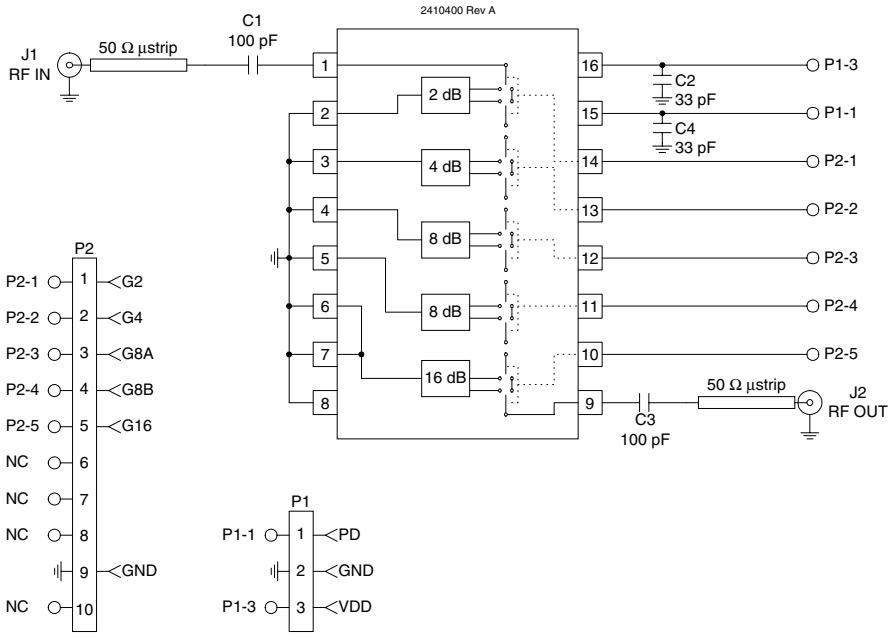
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Pin	Function	Description	Interface Schematic
1	RF IN	RF Input. This pin is not DC blocked, and an external blocking capacitor is recommended. The value depends on the frequency used.	
2	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance. Each ground pin should be connected to the ground plane individually, rather than using one trace and/or via for all ground pins. This will give better step accuracy.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	GND	Same as pin 2.	
9	RF OUT	RF Output. This pin is not DC blocked, and an external blocking capacitor is recommended. The value depends on the frequency used.	
10	G16	Control pin for the 16dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off. For operating frequencies above 1GHz this bit should always be left "off".	
11	G8B	Control pin for the 8dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
12	G8A	Control pin for the 8dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
13	G4	Control pin for the 4dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
14	G2	Control pin for the 2dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
15	PD	Power Down control pin. This pin has an internal pull-up resistor to VDD of 10kΩ. When this pin is "low" the circuits are turned off. A "low" means as close to 0V as possible, to ensure minimum current consumption when turned off.	
16	VDD	Power supply pin. An external RF bypass capacitor is recommended.	

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Evaluation Board Schematic

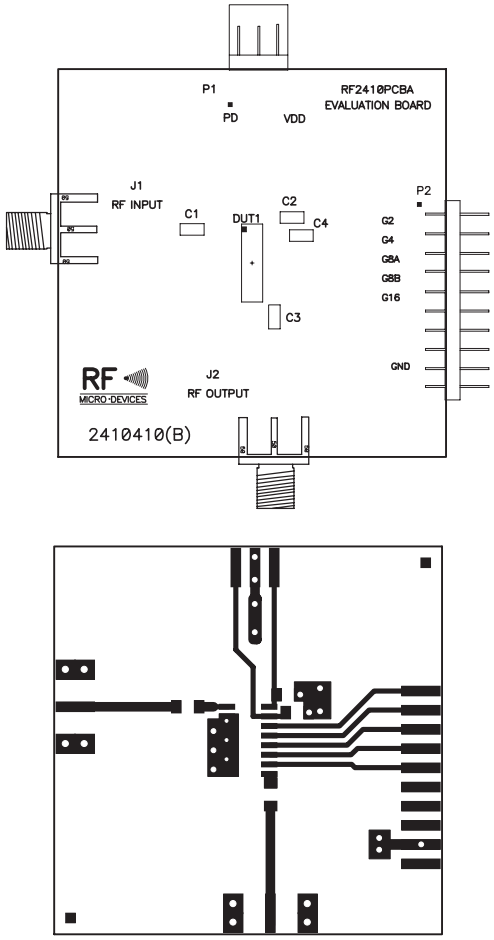
(Download Bill of Materials from www.rfmd.com.)



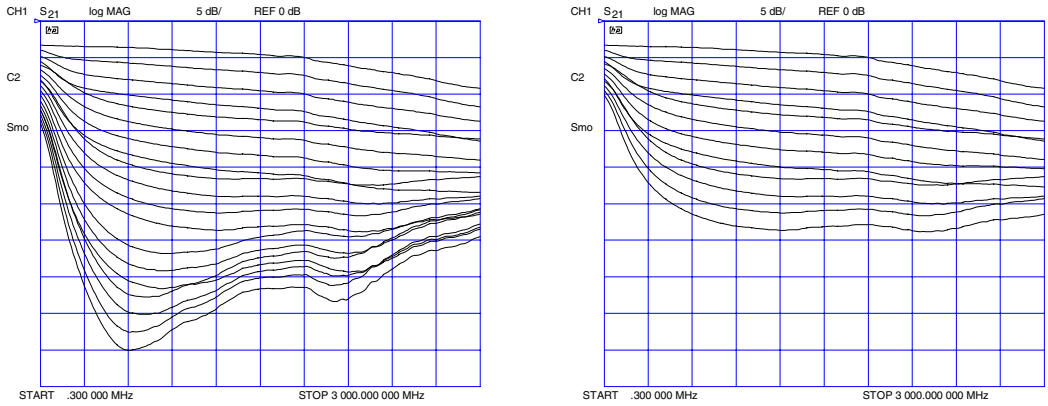
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Evaluation Board Layout
Board Size 2.020” x 2.020”

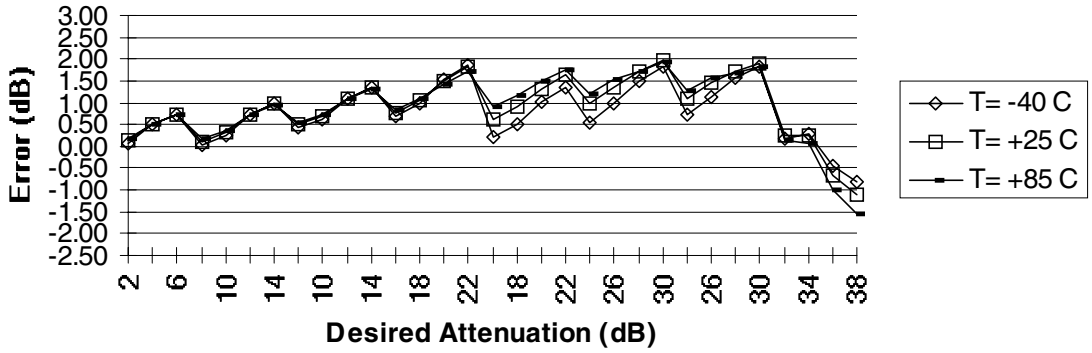
Board Thickness 0.031”, Board Material FR-4



Attenuation vs. Frequency
1. Using All Bits, 2. Not Using G16

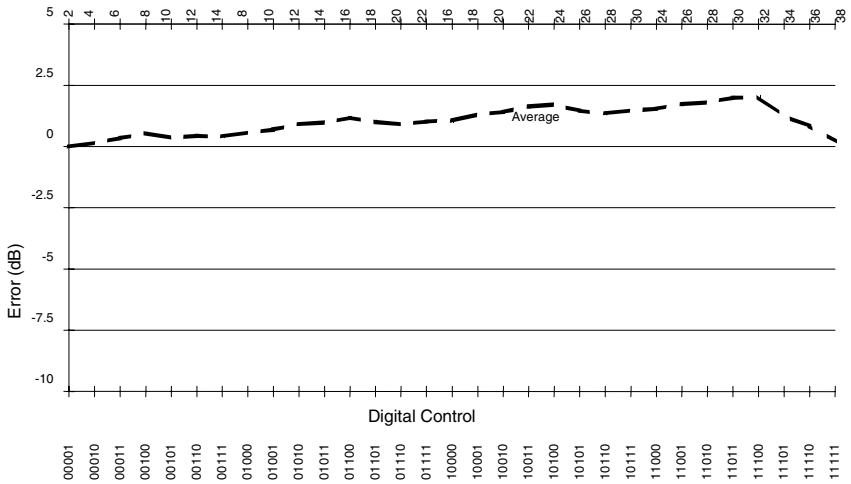


RF2410 Attenuation Error from Ideal over Temperature
900 MHz

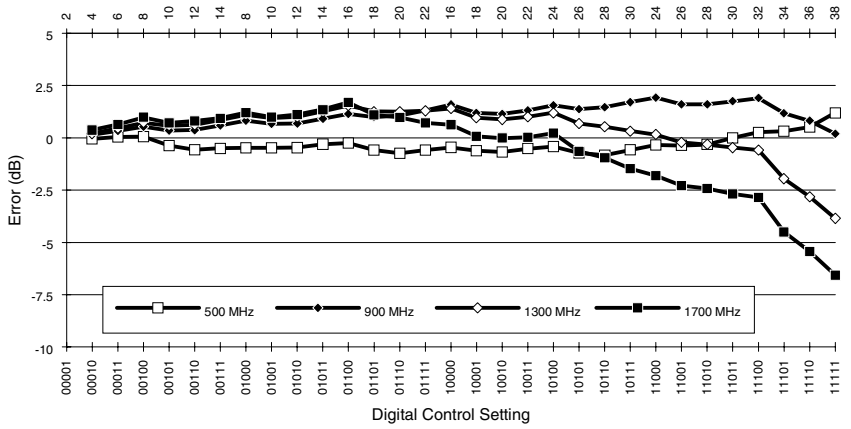


Typical Characteristics at 900MHz

Attenuation Variation from Ideal



Typical Attenuation Error



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RF MICRO·DEVICES

RF2420

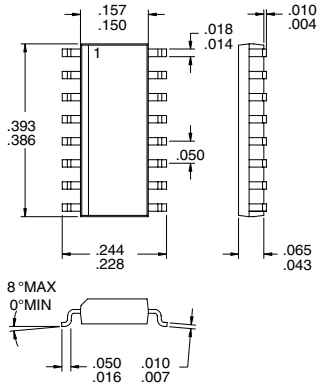
PROGRAMMABLE ATTENUATOR

Typical Applications

- Power Control in Communication Systems
- CMOS Compatible Programmable Attenuators
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

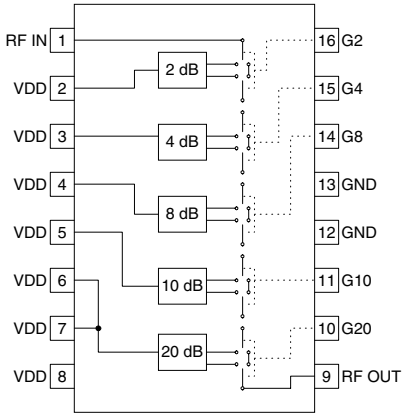
The RF2420 is a multistage monolithic programmable attenuator. The device is built using an advanced Gallium Arsenide process technology and has an attenuation programmability over a 44dB range in 2dB steps. The attenuation is set by five bits of digital data. The input and output of the device have a low VSWR 50Ω match. This unit is intended for use in systems that require RF transmit power control by digital means. Typical applications are in dual mode IS-54/55 compatible cellular transceivers and TETRA systems. No negative supply voltages are required.



Package Style: SOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V to 6V Supply
- 0dB to 44dB Attenuation Range
- 4dB Insertion Loss
- 5-bit Digitally Controlled Attenuation
- Digitally Controlled Power Down Mode
- DC to 950MHz Frequency Range

Ordering Information

RF2420	Programmable Attenuator
RF2420 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2420

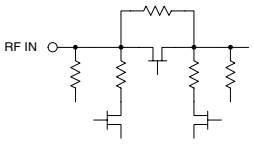
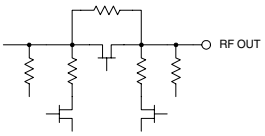
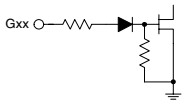
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
RF Input Power	+17	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

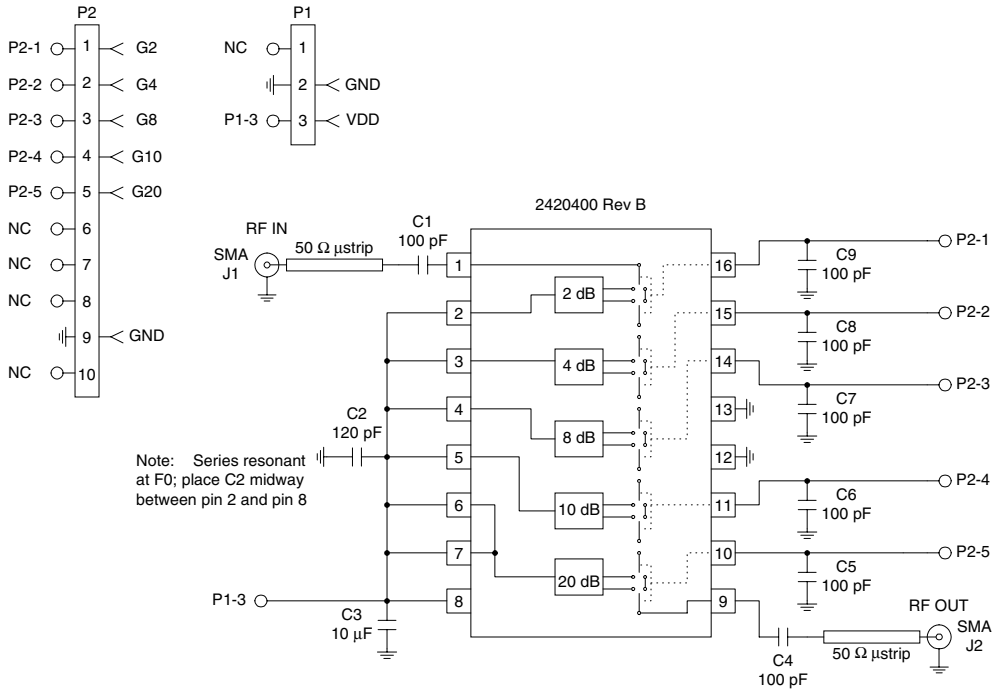
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C and 5V at 420MHz
Frequency Range		DC to 950		MHz	Tuning of bypass capacitors is required for shifting the center frequency. See the evaluation board schematic for details.
Insertion Loss		4	6	dB	
Attenuation Range		0 to 44		dB	
Gain Flatness			3	dB	In any 50MHz band, at max attenuation
3dB Bandwidth		500		MHz	At 26dB attenuation
		50		MHz	At maximum attenuation
Input					
Input Impedance		50		Ω	
Input VSWR		1.2:1	1.5:1		
Input 1dB Compression	+13	+15		dBm	
Attenuation					
Attenuation Settings		2, 4, 8, 10, 20		dB	CMOS Level, 5 bits
Accuracy			±0.5	dB	2dB step
			±1.0	dB	4dB through 20dB steps
Attenuation Control					
Attenuation "ON" Voltage	2.5	V_{DD}		V	Voltage Supplied to input
Attenuation "OFF" Voltage			0.3	V	Voltage Supplied to input
Current		0.4	1.0	mA	Into each control line
Response Time		<10		ns	
Output					
IM3	-30			dBc	With 0dBm output in each of 2 tones
Harmonic Output	-40			dBc	
Output Impedance		50		Ω	
Output VSWR		1.2:1	1.5:1		
Power Supply					
Voltage		5		V	Specifications
		3 to 6		V	Operating Limits
Current		4	8	mA	Operating
		0.4	0.75	mA	Power Down

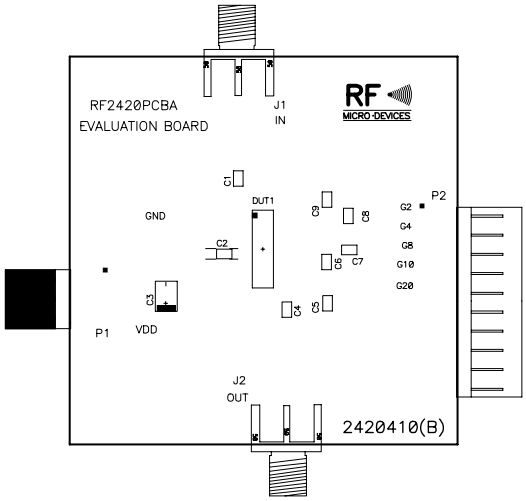
Pin	Function	Description	Interface Schematic
1	RF IN	RF Input. This pin is not DC blocked, and an external blocking capacitor is required. The value depends on the frequency used. The DC value on this pin is approximately equal to VDD.	
2	VDD	VDD supply connection. Bypassing is critical: To achieve maximum attenuation range the magnitude of the impedance at the operation frequency, as seen from the package pins, needs to be less than 0.5Ω. The DC source to the pin may be a logic driver gate to implement a Power Down function.	
3	VDD	Same as pin 2.	
4	VDD	Same as pin 2.	
5	VDD	Same as pin 2.	
6	VDD	Same as pin 2.	
7	VDD	Same as pin 2.	
8	VDD	Same as pin 2.	
9	RF OUT	RF Output. Same as pin 1. Pin 1 and 9 are interchangeable.	
10	G20	Control pin for the 20dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	
11	G10	Control pin for the 10dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
12	GND	Ground.	
13	GND	Ground.	
14	G8	Control pin for the 8dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
15	G4	Control pin for the 4dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.
16	G2	Control pin for the 2dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	Same as pin 10.

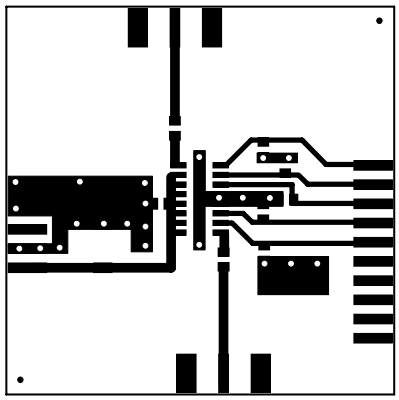
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout





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RF2421

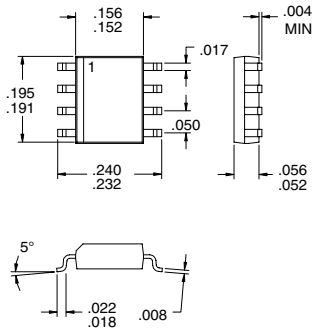
10dB SWITCHED ATTENUATOR

Typical Applications

- Power Control in Communication Systems
- CMOS Compatible Programmable Attenuator
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

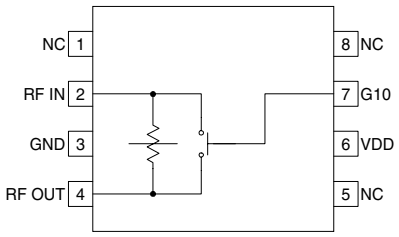
The RF2421 is a monolithic switched attenuator. The device is built using a Gallium Arsenide process technology and has a single step attenuation of 10dB. The input and output of the device has a low VSWR 50Ω match. The RF output can drive up to +16dBm. This unit is intended for use in systems that require RF power control by digital means. No negative supply voltages are required, and the current consumption is less than 1μA when the attenuator is off.



Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 2.7V to 6V Supply
- 10dB Single Step Attenuation
- 1 dB Insertion Loss
- 1-bit Digitally Controlled Attenuation
- Digitally Controlled Power Down Mode
- 500MHz to 3000 MHz Operation

Ordering Information

RF2421	10dB Switched Attenuator
RF2421 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2421

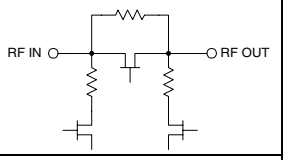
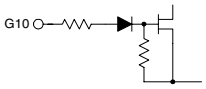
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Control Voltage	-0.5 to +6.0	V
Input RF Power	+20	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

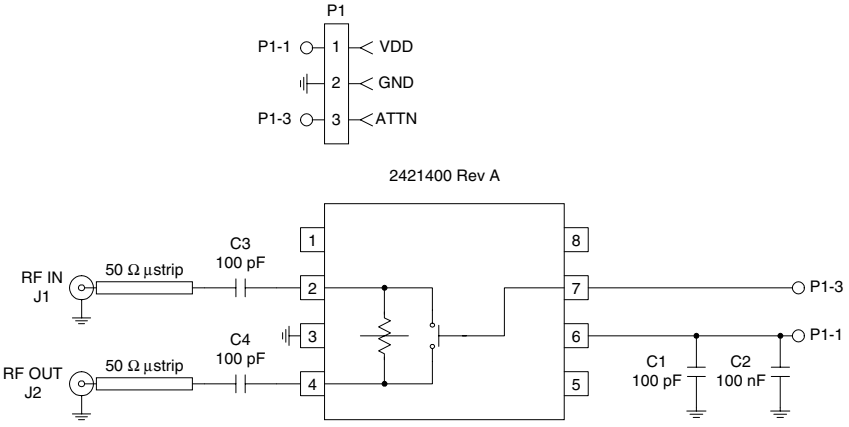
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=5.0V, Freq=915MHz
Frequency Range		500 to 3000		MHz	
Insertion Loss		1.0	1.5	dB	V_{G10}=0V_{DC}
Insertion Loss	9.5	10	10.5	dB	V_{G10}=V_{DD}
Gain Flatness		0.25		dB	In any 50MHz band
Input					
Input Impedance		50		Ω	
Input VSWR			1.3:1		
Input 1dB Compression	+17			dBm	
Attenuation Control					
Attenuation "ON" Voltage	2.5	V_{DD}		V	Voltage supplied to input
Attenuation "OFF" Voltage			0.3	V	Voltage supplied to input
Current		0.4	0.5	mA	Into control line, V_{G10}=5V_{DC}
Response Time		<10		ns	
Output					
IM_3	-60			dBc	With 0dBm output in each of 2 tones
Harmonic Output	-40			dBc	
Output Impedance		50		Ω	
Output VSWR			1.3:1		
Power Supply					
Voltage		5		V	Specifications
	2.7	5	6.0	V	Operating Limits
Current			0.5	mA	Attenuation "ON"
			1	μA	Attenuation "OFF"

Pin	Function	Description	Interface Schematic
1	NC	Not internally connected. This pin can be grounded.	
2	RF IN	RF Input. This pin is not DC blocked, and an external blocking capacitor is recommended. The value depends on the frequency used.	
3	GND	Ground connection. Keep trace physically short and connect immediately to the ground plane for best performance.	
4	RF OUT	RF Output. This pin is not DC blocked, and an external blocking capacitor is recommended. The value depends on the frequency used.	See pin 2.
5	NC	Not internally connected. This pin can be grounded.	
6	VDD	Power supply pin. An external RF bypass capacitor is recommended.	
7	G10	Control pin for the 10dB attenuator. This pin has an internal pull-down resistor, so when the pin is not connected the attenuator will be turned off.	
8	NC	Not internally connected. This pin can be grounded.	

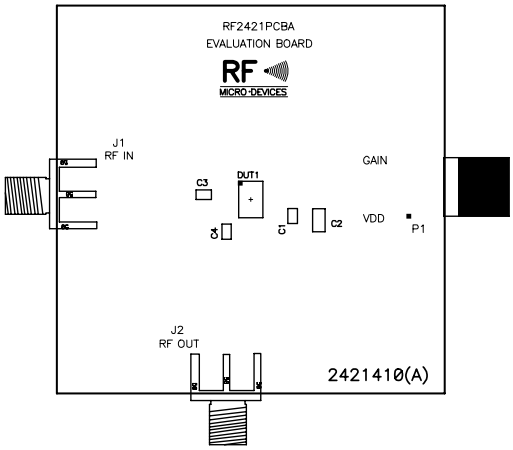
Evaluation Board Schematic

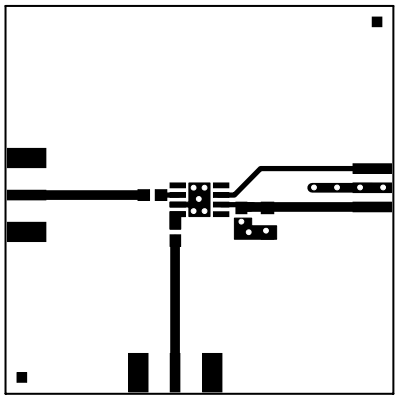
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout

Board Thickness 0.031"; Board Material FR-4





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RF2425

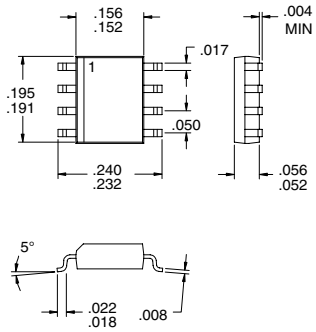
4-PORT TRANSFER SWITCH

Typical Applications

- Cordless Phones
- Wireless Computer Peripherals
- Wireless Security Systems
- General Purpose RF Switching
- Commercial and Consumer Systems

Product Description

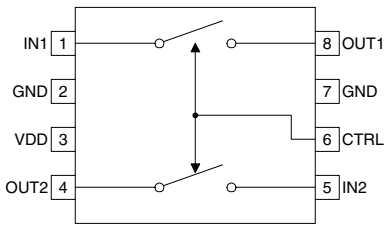
The RF2425 is a very low-cost single-throw, double-pole GaAs MESFET switch. There are two bidirectional input/output channels which can be turned off or on by a single logic control line. Two of the ports may be tied together externally to make a transmit/receive switch. The device can handle power levels as high as +32dBm and spans a frequency range from DC to 2000MHz. The switch will operate from power supply voltages as low as 1.5V and as high as 6V with a CMOS logic driver for the control input.



Package Style: SOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single Power Supply of 1.5V to 6.0V
- Low Current Consumption
- 0.5dB Insertion Loss at 900MHz
- 24dB Crosstalk Isolation at 900MHz
- +31dBm Output P1dB

Ordering Information

RF2425	4-Port Transfer Switch
RF2425 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2425

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Control Voltage	-1.0 to +6.0	V_{DC}
Input RF Power	+33	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

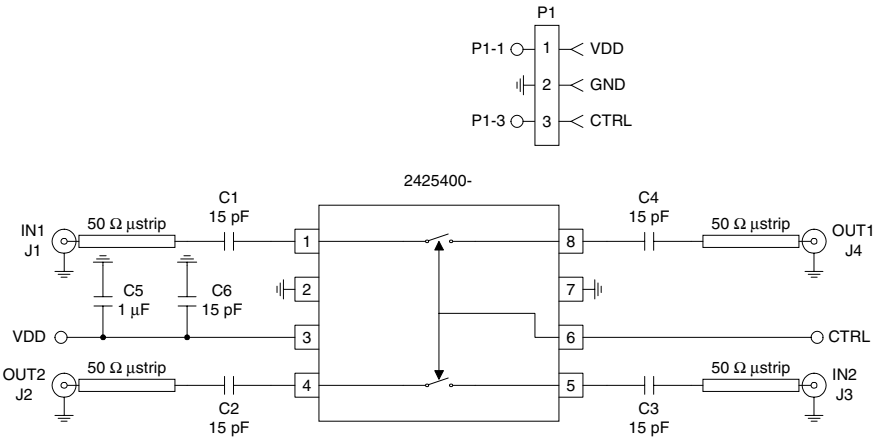
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=3.0V, Freq=900MHz
Frequency Range		DC to 2000		MHz	
Insertion Loss		0.5	1	dB	
Isolation	20	24		dB	CTRL="Low;" IN1 to OUT2 crosstalk
	20	24		dB	CTRL="High;" IN2 to OUT1 crosstalk
"On" Input VSWR		1:1			Input of active channel
"Off" Input VSWR		100:1			Input of inactive channel (open circuit)
Output P1dB		+31		dBm	
Control Logic					
CTRL Logic "Low" Voltage		0		V	Channel 1 On, Channel 2 Off
CTRL Logic "High" Voltage		0.7		V	Channel 2 On, Channel 1 Off
Power Supply					
Voltage		3		V	Specifications
		1.5 to 6		V	Operating Limits
Current		1	2	mA	CTRL="Low"
		2	2.5	mA	CTRL="High"

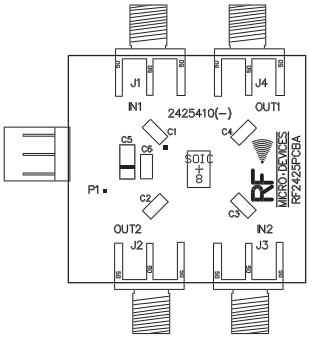
Pin	Function	Description	Interface Schematic
1	IN1	Input pin for Channel 1. Channel 1 is chosen with a logic level “Low” on pin 6, CTRL. The input VSWR is 1:1 when this channel is active and highly capacitive (open circuit) when this channel is inactive. Since both channels of the switch are bidirectional, this pin may be used as an output with OUT1 as its input depending on layout preference.	
2	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	VDD	Power supply. An external RF bypass capacitor is recommended.	
4	OUT2	Output pin for Channel 2. This pin may be used as the channel 2 input instead; see pin 5 description.	
5	IN2	Input pin for Channel 2. Channel 2 is chosen with a logic level “High” on pin 6, CTRL. The input VSWR is 1:1 when this channel is active and highly capacitive (open circuit) when this channel is inactive. Since both channels of the switch are bidirectional, this pin may be used as an output with OUT2 as its input depending on layout preference.	
6	CTRL	Control pin. This pin chooses which channel is active. A “Low” level chooses Channel 1; a “High” level chooses Channel 2. CMOS logic may be used to drive the control input.	
7	GND	Same as pin 2.	
8	OUT1	Output pin for Channel 1. This pin may be used as the channel 1 input instead; see pin 1 description.	

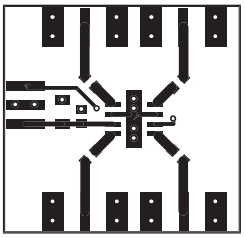
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 1.236” x 1.186”





RF MICRO·DEVICES

RF2436

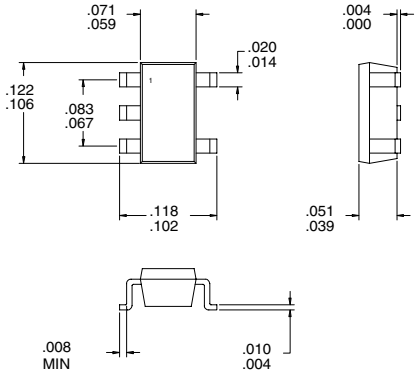
TRANSMIT/RECEIVE SWITCH

Typical Applications

- Cordless Phones
- Wireless Computer Peripherals
- Wireless Security Systems
- General Purpose RF Switching
- Commercial and Consumer Systems

Product Description

The RF2436 is a very low-cost transmit/receive GaAs MESFET switch. The device can handle power levels as high as +28dBm and spans a frequency range from DC to 2000MHz. The switch will operate from power supply voltages as low as 1.5V and as high as 6V with a CMOS logic driver for the control input. No negative voltage is required, and current consumption is very low. VSWR for the active channel (transmit or receive) is 1:1. The device is housed in a very small industry-standard SOT-23 5-lead plastic package.



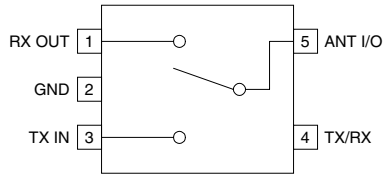
Package Style: SOT-23-5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS

Features

- Single Positive Power Supply
- Low Current Consumption
- 0.5dB Insertion Loss at 900MHz
- 24dB Crosstalk Isolation at 900MHz
- +27dBm Output P1dB



Functional Block Diagram

Ordering Information

RF2436	Transmit/Receive Switch
RF2436 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2436

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	0 to +8.0	V_{DC}
Control Voltage	-1.0 to +6.0	V
Input RF Power	+30	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

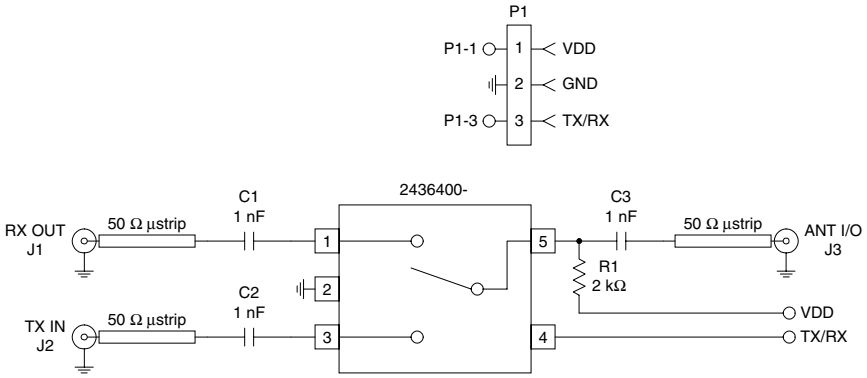
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=3.0V, Freq=900MHz
Frequency Range		DC to 2000		MHz	
Insertion Loss		1	2	dB	Transmit or receive mode.
Isolation	20	22		dB	Receive mode; ANT I/O to TX IN crosstalk
	20	24		dB	Transmit mode; ANT I/O to RXOUT crosstalk
RX OUT VSWR		1:1			Receive mode.
		100:1			Transmit mode.
TX IN VSWR		1:1			Transmit mode.
		100:1			Receive mode.
Output P1dB		+27		dBm	
Output IP3		+39		dBm	
Control Logic					
CTRL Logic "Low" Voltage		0		V	Receive mode.
CTRL Logic "High" Voltage		0.7		V	Transmit mode.
Power Supply					
Voltage		3		V	Specifications
		1.5 to 6		V	Operating Limits
Current		5	10	µA	Receive mode.
		0.5	1	mA	Transmit mode.

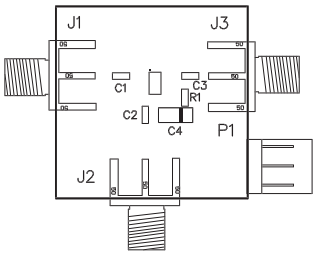
Pin	Function	Description	Interface Schematic
1	RX OUT	Output pin for Receive mode. VSWR is 1:1 when Receive Mode is selected and highly capacitive when Transmit Mode is selected.	
2	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	TX IN	Input pin for Transmit mode. The input VSWR is 1:1 when Transmit Mode is selected and highly capacitive when Receive Mode is selected.	
4	TX/RX	Transmit Mode/Receive Mode Control pin. A “Low” level chooses Receive Mode; a “High” level chooses Transmit Mode. CMOS logic may be used to drive the control input.	
5	ANT I/O	Input/Output pin from/to antenna and power supply pin. This pin must be biased with VDD through a resistor.	

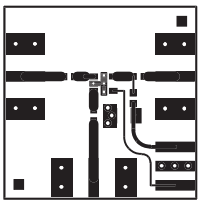
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout





10 IF Amplifiers

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Gain (dB, Max)	Gain Control (dB)	RSSI	Package	Page
RF2607	CDMA/FM Receive AGC Amplifier	12 to 285	3.6	14	48	96	no	SSOP-16	10-1
RF2609	CDMA/FM Transmit AGC Amplifier	12 to 175	3.6	23	42	90	no	SSOP-16	10-9
RF2617	3V CDMA/FM Receive AGC Amplifier	12 to 285	3.0	14	48	96	no	SSOP-16	10-17
RF2619	3V CDMA/FM Transmit AGC Amplifier	12 to 175	3.0	23	42	90	no	SSOP-16	10-25
RF2627	3V CDMA Receive AGC Amplifier	12 to 285	2.7 to 3.3	14	48	96	no	MSOP-8	10-33
RF2629	3V CDMA/FM Transmit AGC Amplifier	12 to 175	2.7 to 3.3	23	42	90	no	MSOP-8	10-39
RF2670	8MHz Dual Baseband AGC with Programmable Low Pass Filtering	0.01 to 8	2.7 to 3.6	13	80	70	yes	SSOP-24	10-45
RF2903	Integrated Spread Spectrum Receiver	150 to 1000	3.0 to 6.0	23	90	90	yes	SSOP-24	10-57

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RF2607

CDMA/FM RECEIVE AGC AMPLIFIER

Typical Applications

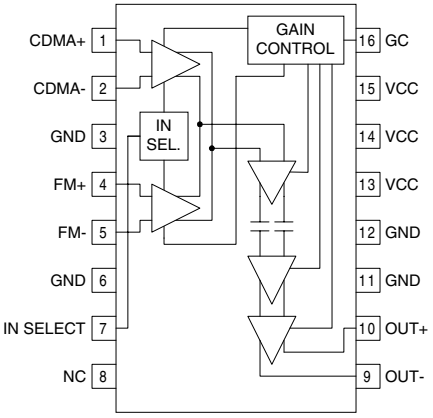
- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Linear IF Amplifier
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

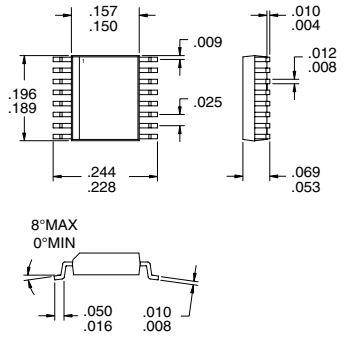
The RF2607 is a complete AGC amplifier designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify IF signals while providing more than 90dB of gain control range. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and this Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process, and is packaged in a standard miniature 16-lead plastic SSOP package.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-16

Features

- Supports Dual Mode Operation
- -48dB to +48dB Gain Control Range
- IS95 CDMA Compatible
- Digitally Selectable Inputs
- -2dBm Input IP_3
- 12MHz to 285MHz Operation

Ordering Information

RF2607	CDMA/FM Receive AGC Amplifier
RF2607 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2607

Absolute Maximum Ratings

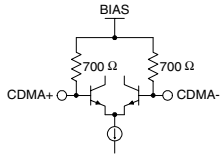
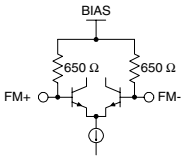
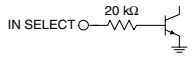
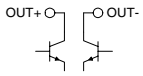
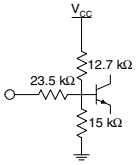
Parameter	Value	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

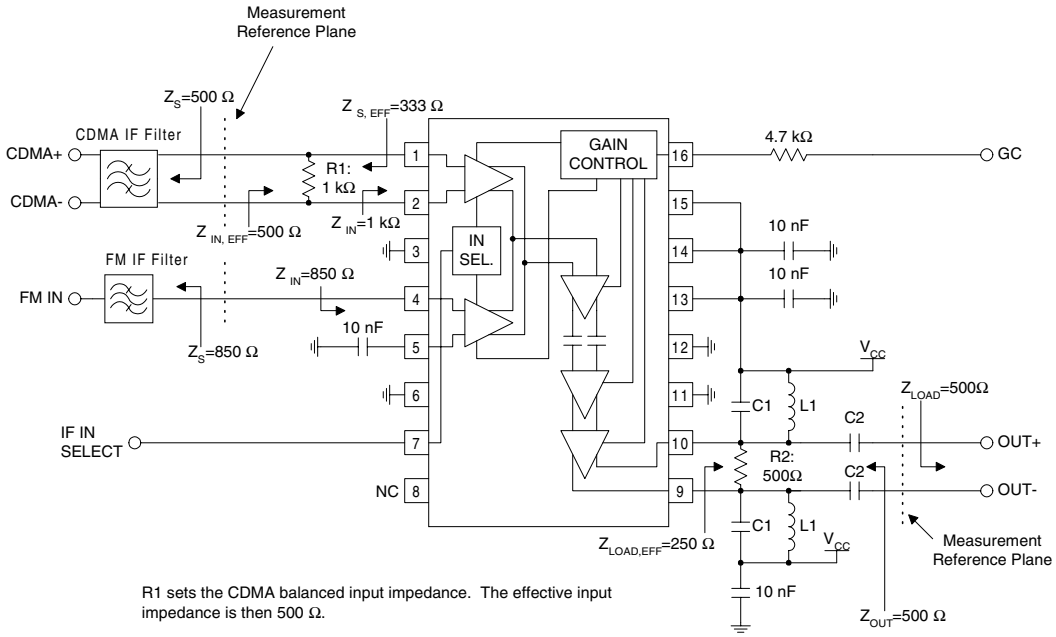
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 85MHz, V_{CC}=3.6V, Z_S =500Ω, Z_L=500Ω, 500Ω External CDMA Input Terminating Resistor, 500Ω External Output Terminating Resistor (Effective Z_S=333Ω, Effective Z_L=250Ω) (See Application Example)
Frequency Range		12 to 285		MHz	
CDMA Maximum Gain	+45	+48		dB	V_{GC}=2.9V
CDMA Minimum Gain		-48	-45	dB	V_{GC}=0.2V
FM Maximum Gain	+45	+49		dB	V_{GC}=2.9V
FM Minimum Gain		-48	-45	dB	V_{GC}=0.2V
Gain Slope		47		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V_{DC}	Source impedance of 4.7kΩ
Gain Control Input Impedance		30		kΩ	
Noise Figure		5		dB	At maximum gain and 85MHz
Input IP_3	-44	-40		dBm	At +40dB gain, referenced to 500Ω
		-2		dBm	At minimum gain, referenced to 500Ω
Stability (Max VSWR)	10:1				Spurious<-70dBm
IF Input					
Input Impedance		1		kΩ	CDMA, differential
Input Impedance		850		Ω	FM, single-ended
CDMA to FM Isolation		30		dB	
Power Supply					
Voltage		3.3 to 3.6		V	
Current Consumption		13		mA	Minimum gain
Current Consumption		14	17	mA	Maximum gain

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Pin	Function	Description	Interface Schematic
1	CDMA+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level other than V_{CC} present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	CDMA-	Same as pin 2, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	FM+	FM Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other FM input is AC coupled to ground. The balanced input impedance is 1.7kΩ, while the single-ended input impedance is 850Ω.	
5	FM-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Same as pin 3.	
7	IN SELECT	Selects which IF input (CDMA or FM) is used. This is a digitally controlled input. A logic "high" selects the CDMA input amplifier. A logic "low" selects the FM input amplifier. The threshold voltage is approximately 1.3V.	
8	NC	No Connection pin. This pin is internally biased and should not be connected to any external circuitry, including ground or V_{CC}.	
9	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 250Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
10	OUT+	Same as pin 9, except complementary output.	See pin 9.
11	GND	Same as pin 3.	
12	GND	Same as pin 3.	
13	VCC	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
14	VCC	Same as pin 13.	
15	VCC	Same as pin 13.	
16	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are only valid for a 4.7kΩ DC source impedance.	

Application Schematic



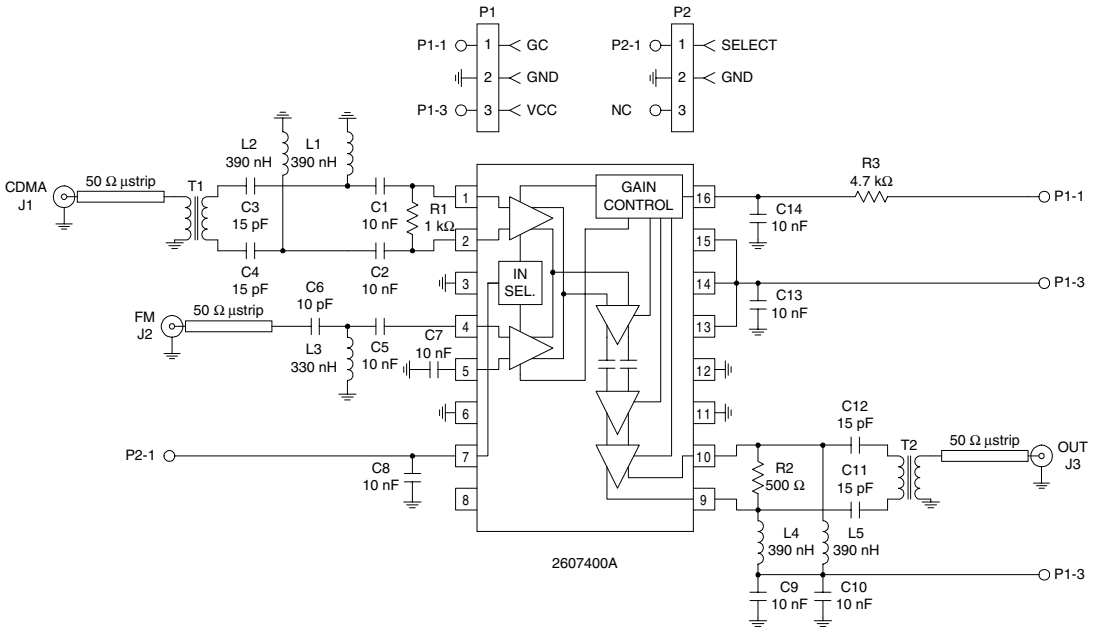
R1 sets the CDMA balanced input impedance. The effective input impedance is then 500 Ω.

R2 sets the balanced output impedance to 500 Ω. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network of the load impedance is not 500 Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the load impedance is 500 Ω.

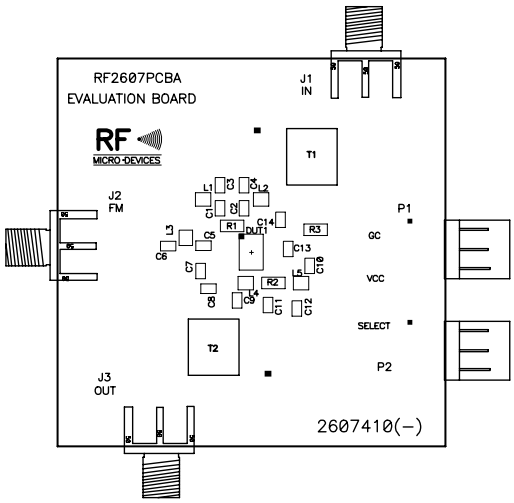
Db00.bk Page 5 Thursday, January 6, 2000 6:50 PM

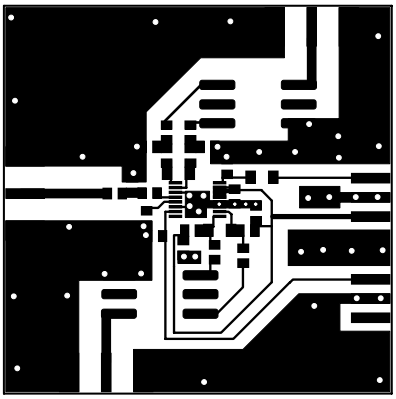
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

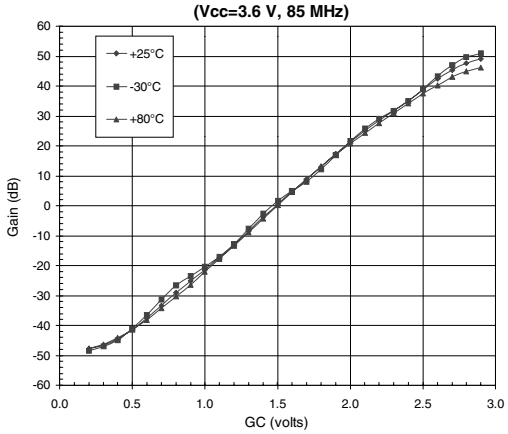


Evaluation Board Layout

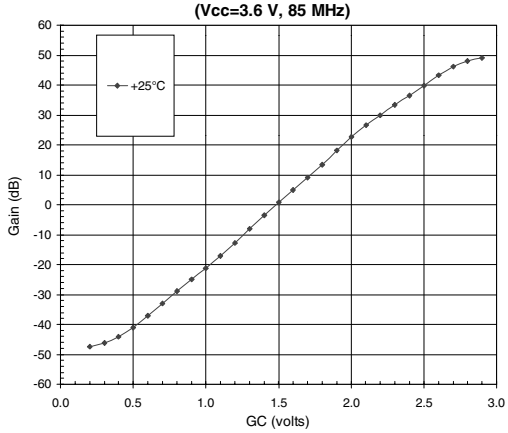




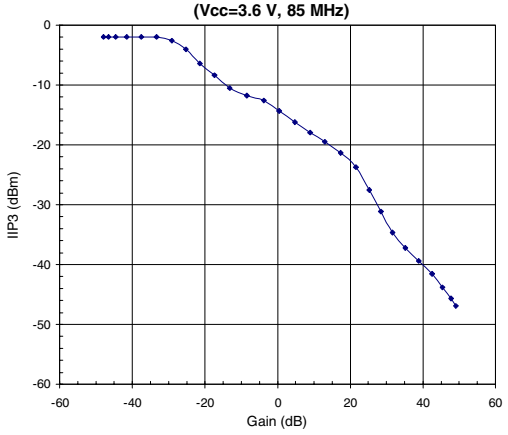
RF2607 CDMA Gain vs. Gain Control Voltage
(Vcc=3.6 V, 85 MHz)



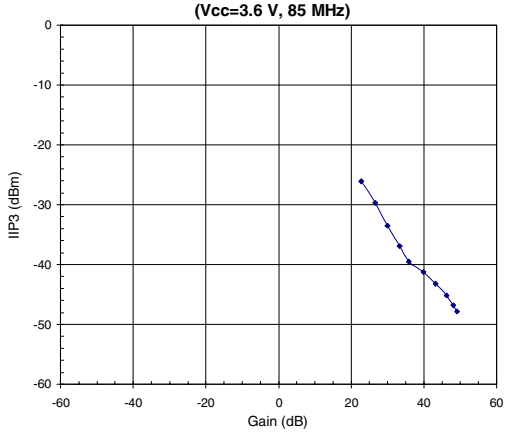
RF2607 FM Gain vs. Gain Control Voltage
(Vcc=3.6 V, 85 MHz)



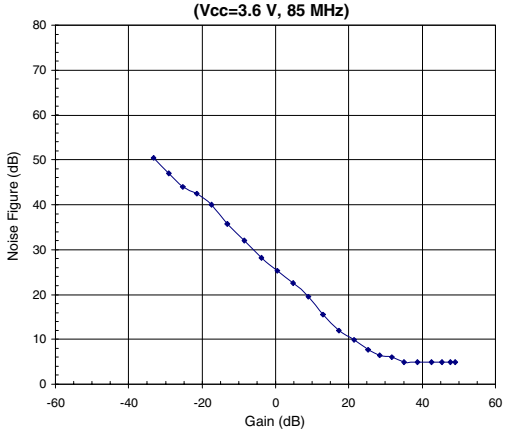
RF2607 CDMA IIP3 vs. Gain
(Vcc=3.6 V, 85 MHz)



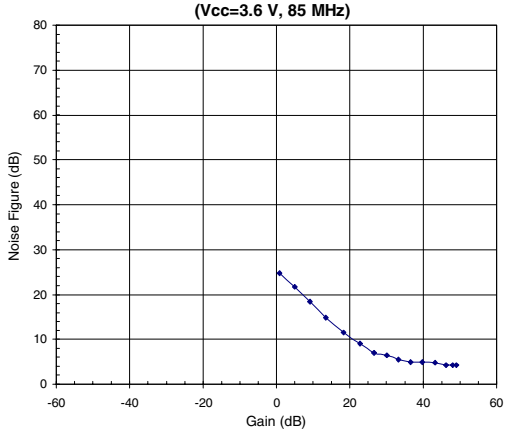
RF2607 FM IIP3 vs. Gain
(Vcc=3.6 V, 85 MHz)



RF2607 CDMA Noise Figure vs. Gain
(Vcc=3.6 V, 85 MHz)



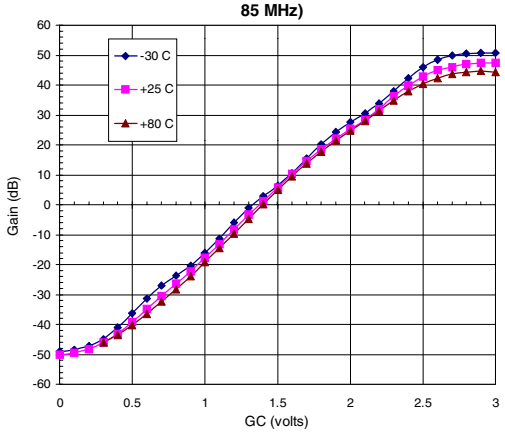
RF2607 FM Noise Figure vs. Gain
(Vcc=3.6 V, 85 MHz)



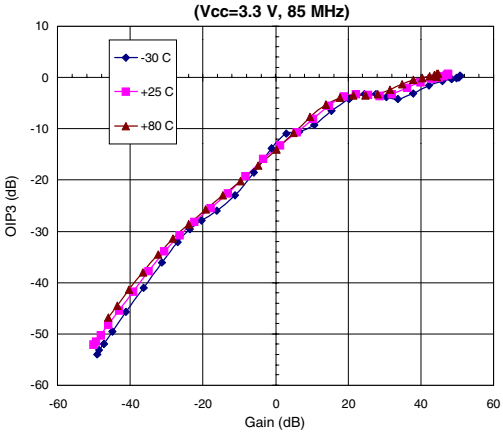
10

IF AMPLIERS

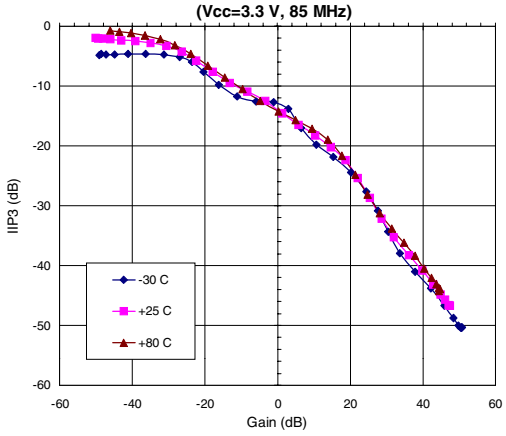
RF2607 CDMA Gain vs. Gain Control Voltage (Vcc=3.6V, 85 MHz)



RF2607 CDMA OIP3 vs. Gain (Vcc=3.3 V, 85 MHz)



RF2607 CDMA IIP3 vs. Gain (Vcc=3.3 V, 85 MHz)



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RF2609

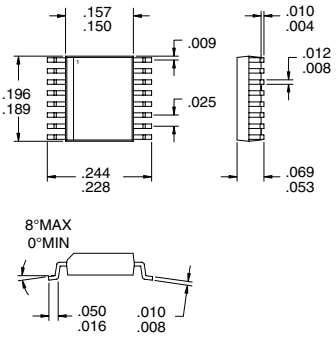
CDMA/FM TRANSMIT AGC AMPLIFIER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Linear IF Amplifier
- Portable Battery Powered Equipment
- Commercial and Consumer Systems

Product Description

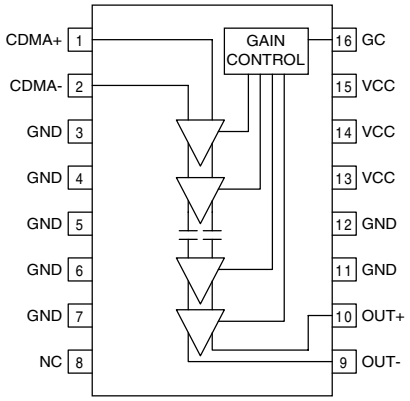
The RF2609 is a complete AGC amplifier designed for the transmit section of dual-mode CDMA/FM cellular applications. It is designed to amplify IF signals while providing more than 84dB of gain control range. Noise Figure, IP3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process and is packaged in a standard miniature 16-lead plastic SSOP package.



Package Style: SSOP-16

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation
- -48dB to +42dB Gain Control Range
- IS-95 CDMA Compatible
- Monolithic Construction
- 12MHz to 175MHz Operation
- Miniature Surface Mount Package

Ordering Information

RF2609	CDMA/FM Transmit AGC Amplifier
RF2609 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

10 IF AMPLIERS

RF2609

Absolute Maximum Ratings

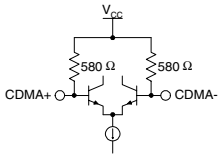
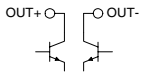
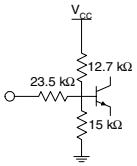
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V
Input Power Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

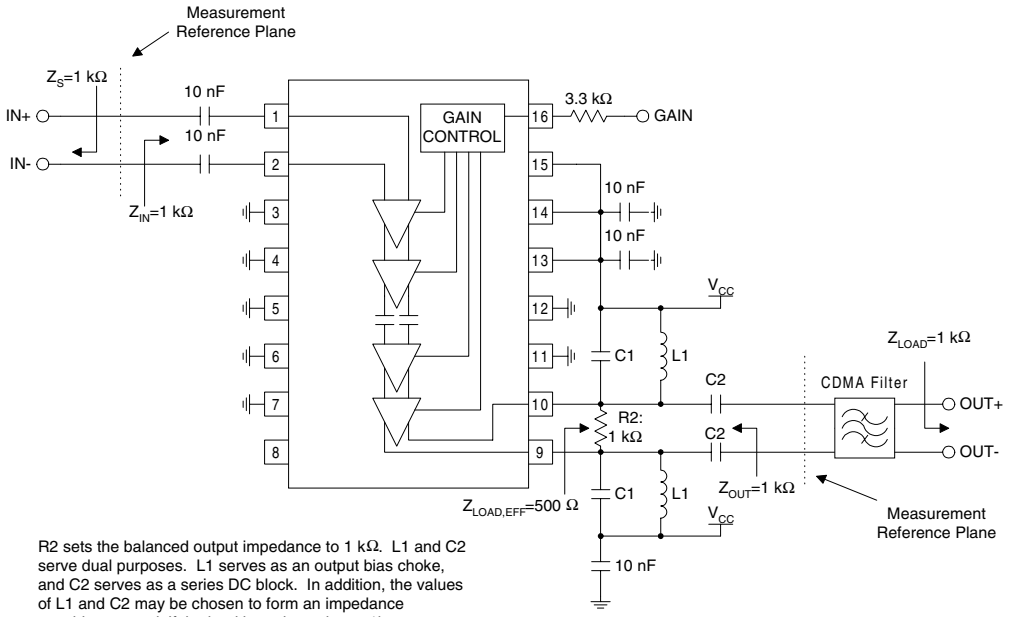
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 130MHz, V_{CC}=3.6V, Z_S=1kΩ, Z_L=1kΩ, 1kΩ External Output Terminating Resistor (Effective Z_L=500Ω) (See Application Example)
Frequency Range		12 to 175		MHz	
Maximum Gain	+39	+42		dB	V_{GC}=2.76V
Minimum Gain		-48	-45	dB	V_{GC}=0.2V
Gain Slope		47		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V_{DC}	
Gain Control Input Impedance		30		kΩ	
Noise Figure		10		dB	At maximum gain and 130MHz
Input IP3	-26	-25		dBm	At +10 gain and referenced to 1kΩ
Input Impedance		1		kΩ	Differential
Stability (Max VSWR)	10:1				Spurious<-70dBm
Power Supply					
Voltage		3.3 to 3.6		V	
Current Consumption		23	25	mA	Maximum gain
Current Consumption		22		mA	Minimum gain

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Pin	Function	Description	Interface Schematic
1	CDMA+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level, other than V_{CC}, present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	CDMA-	Same as pin 2, except complementary input.	See pin 1 schematic.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND	Same as pin 3.	
5	GND	Same as pin 3.	
6	GND	Same as pin 3.	
7	GND	Same as pin 3.	
8	NC	No Connection pin. This pin is internally biased and should not be connected to any external circuitry, including ground or V_{CC}.	
9	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 500Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
10	OUT+	Same as pin 9, except complementary output.	See pin 9 schematic.
11	GND	Same as pin 3.	
12	GND	Same as pin 3.	
13	VCC	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Pins 13, 14, and 15 may share one bypass capacitor if trace lengths are kept minimal.	
14	VCC	Same as pin 13.	
15	VCC	Same as pin 13.	
16	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are valid only for a 3.3kΩ DC source impedance.	

Application Schematic

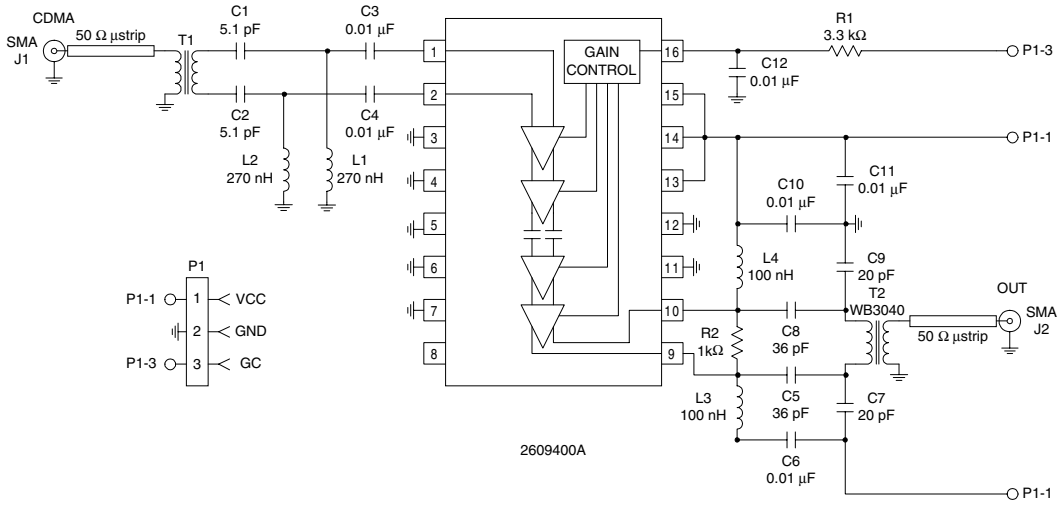


R2 sets the balanced output impedance to 1 kΩ. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the load impedance is not 1kΩ. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 1 kΩ.

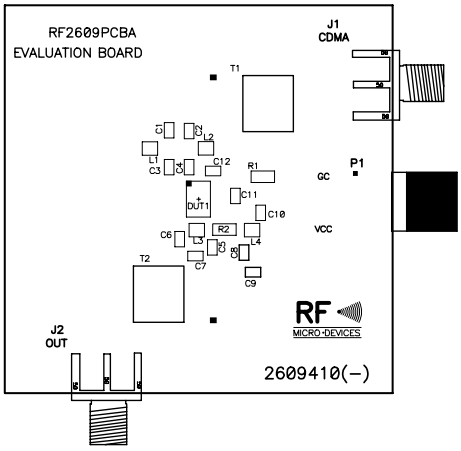
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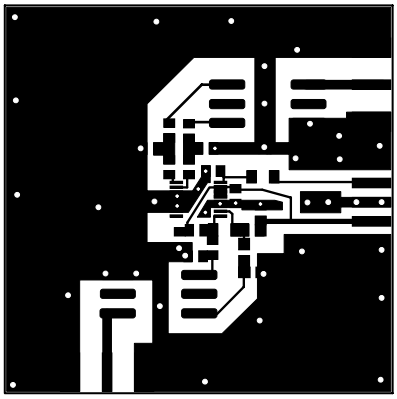
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

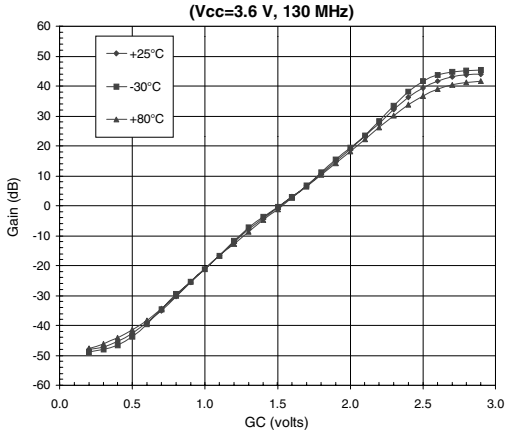


Evaluation Board Layout

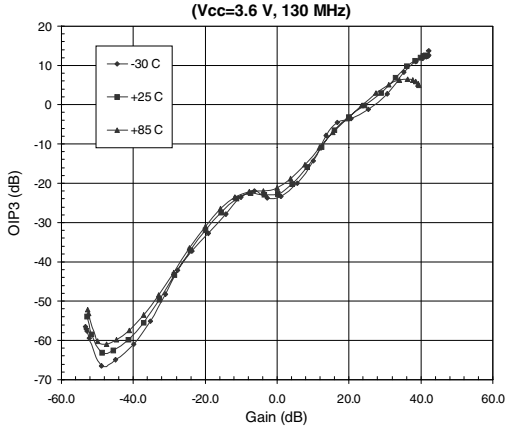




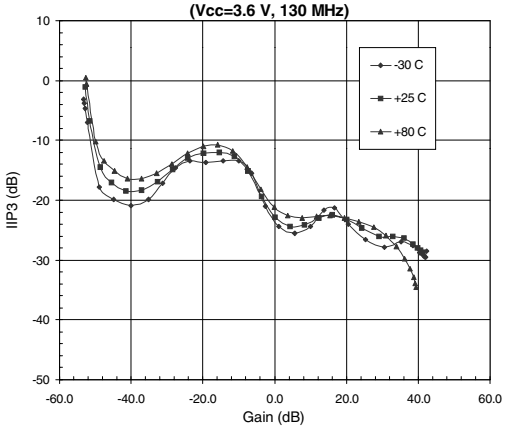
RF2609 Gain vs. Gain Control Voltage
(Vcc=3.6 V, 130 MHz)



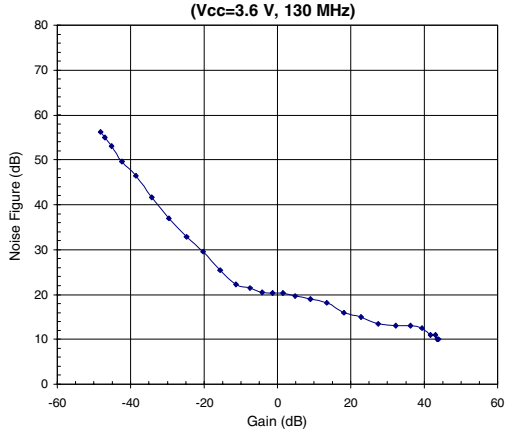
RF2609 OIP3 vs. Gain
(Vcc=3.6 V, 130 MHz)



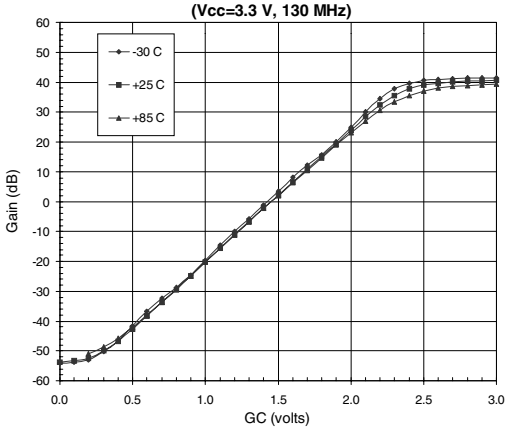
RF2609 IIP3 vs. Gain
(Vcc=3.6 V, 130 MHz)



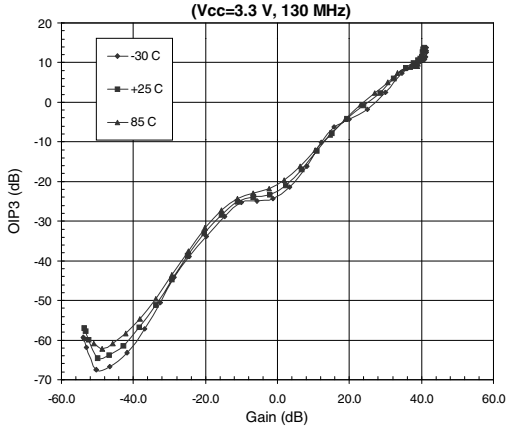
RF2609 Noise Figure vs. Gain
(Vcc=3.6 V, 130 MHz)



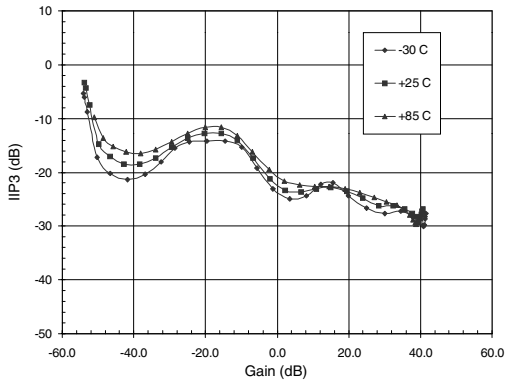
RF2609 Gain vs. Gain Control Voltage
(Vcc=3.3 V, 130 MHz)



RF2609 OIP3 vs. Gain
(Vcc=3.3 V, 130 MHz)



RF2609 IIP3 vs. Gain
(Vcc=3.3 V, 130 MHz)



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RF2617

3V CDMA/FM RECEIVE AGC AMPLIFIER

Typical Applications

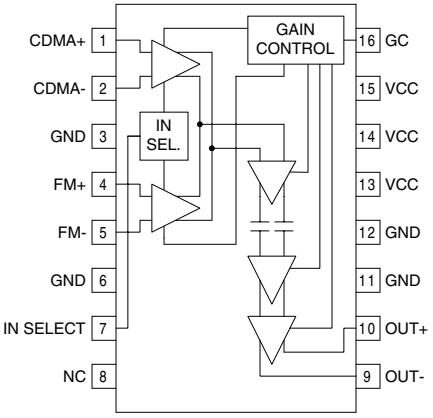
- 3V CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Linear IF Amplifier
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

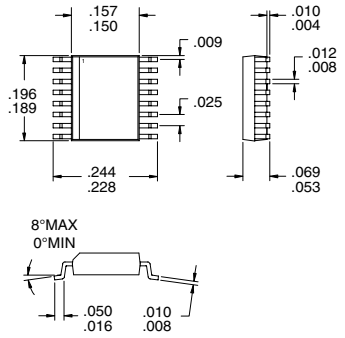
The RF2617 is a complete AGC amplifier designed for the receive section of 3V dual-mode CDMA/FM cellular applications. It is designed to amplify IF signals while providing more than 90dB of gain control range. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and this Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process, and is packaged in a standard miniature 16-lead plastic SSOP package.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-16

Features

- Supports Dual Mode Operation
- -48dB to +48dB Gain Control Range
- Single 3V Power Supply
- Digitally Selectable Inputs
- -2dBm Input IP_3
- 12MHz to 285MHz Operation

Ordering Information

RF2617	3V CDMA/FM Receive AGC Amplifier
RF2617 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

10 IF AMPLIERS

RF2617

Absolute Maximum Ratings

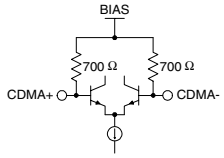
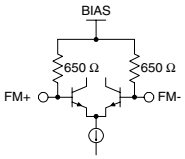
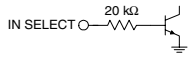
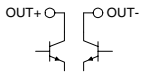
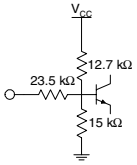
Parameter	Value	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

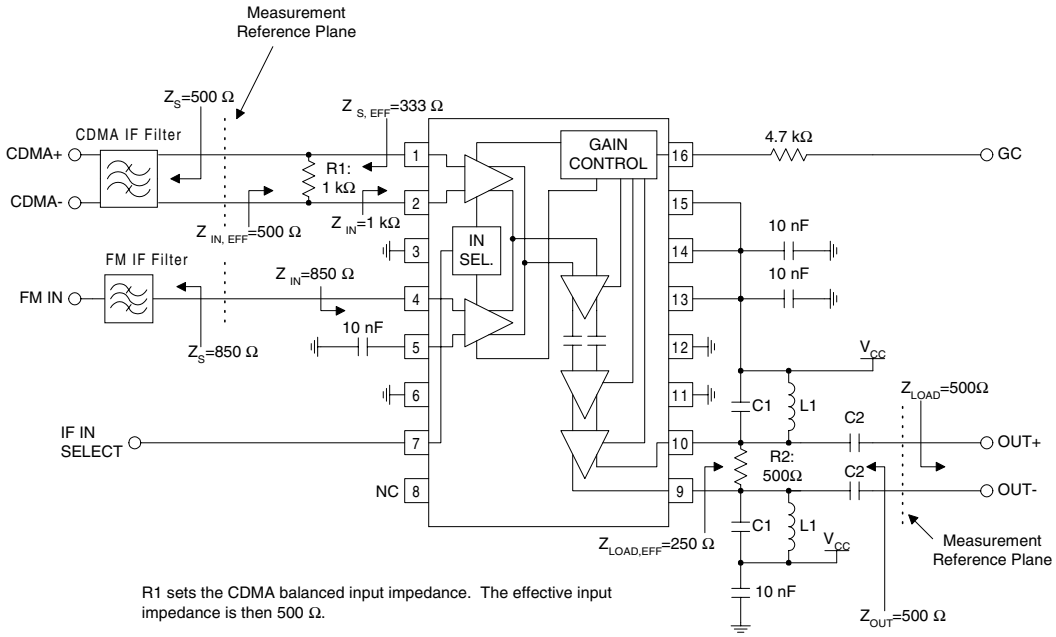
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 85MHz, V_{CC}=3.0V, Z_S =500Ω, Z_L=500Ω, 500Ω External CDMA Input Terminating Resistor, 500Ω External Output Terminating Resistor (Effective Z_S=333Ω, Effective Z_L=250Ω) (See Application Example)
Frequency Range		12 to 285		MHz	
CDMA Maximum Gain	+45	+48		dB	V_{GC}=2.4V
CDMA Minimum Gain		-48	-45	dB	V_{GC}=0.3V
FM Maximum Gain	+45	+49		dB	V_{GC}=2.4V
FM Minimum Gain		-48	-45	dB	V_{GC}=0.3V
Gain Slope		57		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V_{DC}	Source impedance of 4.7kΩ
Gain Control Input Impedance		30		kΩ	
Noise Figure		5	8	dB	At maximum gain and 85MHz
Input IP_3	-44	-40		dBm	At +40dB gain, referenced to 500Ω
	-4	-2		dBm	At minimum gain, referenced to 500Ω
Stability (Max VSWR)	10:1				Spurious<-70dBm
IF Input					
Input Impedance		1		kΩ	CDMA, differential
Input Impedance		850		Ω	FM, single-ended
CDMA to FM Isolation		30		dB	
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		13	15	mA	Minimum gain, V_{CC}=3.0V
Current Consumption		14	16	mA	Maximum gain, V_{CC}=3.0V

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Pin	Function	Description	Interface Schematic
1	CDMA+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level other than V_{CC} present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	CDMA-	Same as pin 2, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	FM+	FM Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other FM input is AC coupled to ground. The balanced input impedance is 1.7kΩ, while the single-ended input impedance is 850Ω.	
5	FM-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Same as pin 3.	
7	IN SELECT	Selects which IF input (CDMA or FM) is used. This is a digitally controlled input. A logic "high" selects the CDMA input amplifier. A logic "low" selects the FM input amplifier. The threshold voltage is approximately 1.3V.	
8	NC	No Connection pin. This pin is internally biased and should not be connected to any external circuitry, including ground or V_{CC}.	
9	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 250Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
10	OUT+	Same as pin 9, except complementary output.	See pin 9.
11	GND	Same as pin 3.	
12	GND	Same as pin 3.	
13	VCC	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
14	VCC	Same as pin 13.	
15	VCC	Same as pin 13.	
16	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are only valid for a 4.7kΩ DC source impedance.	

Application Schematic



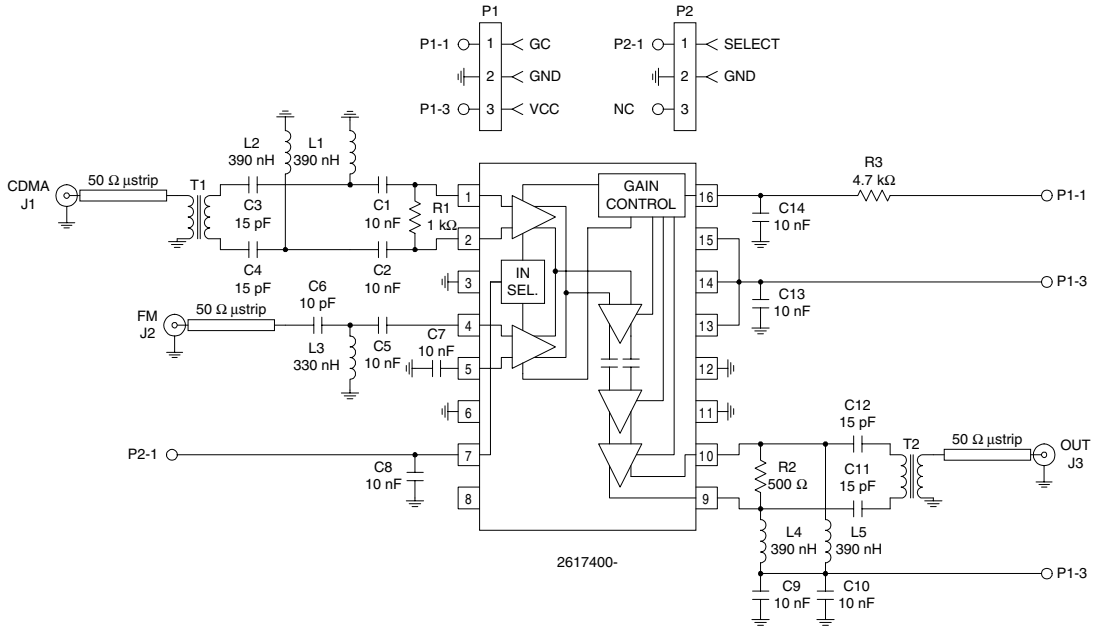
R1 sets the CDMA balanced input impedance. The effective input impedance is then 500 Ω.

R2 sets the balanced output impedance to 500 Ω. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network of the load impedance is not 500 Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the load impedance is 500 Ω.

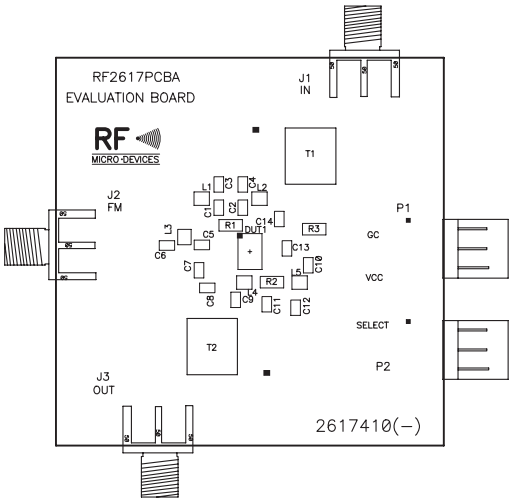
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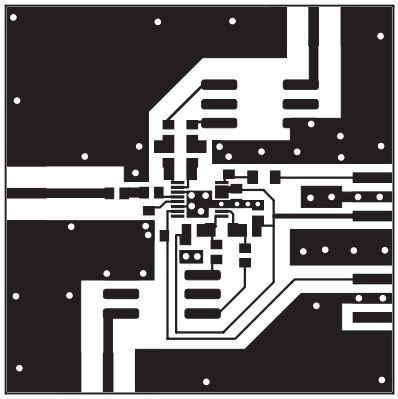
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

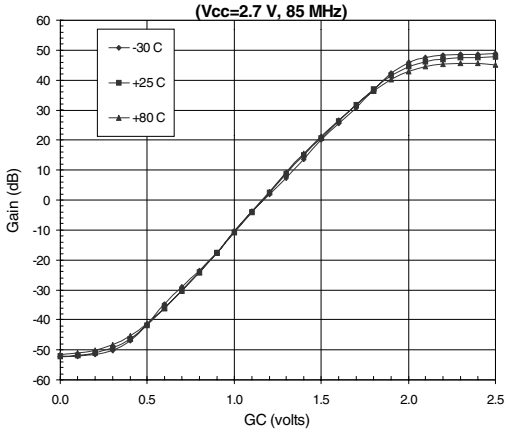


Evaluation Board Layout

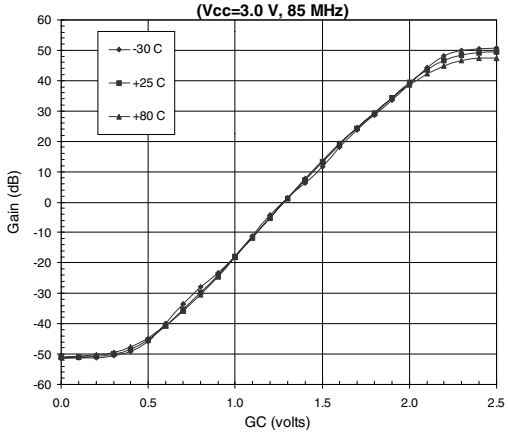




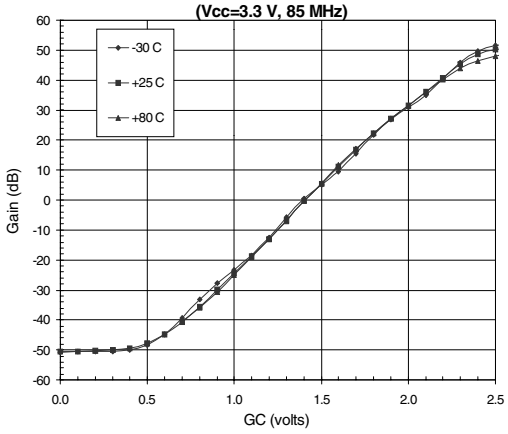
RF2617 Gain vs. Gain Control Voltage (Vcc=2.7 V, 85 MHz)



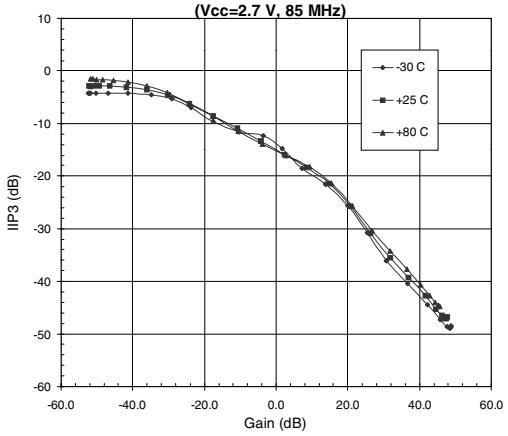
RF2617 Gain vs. Gain Control Voltage (Vcc=3.0 V, 85 MHz)



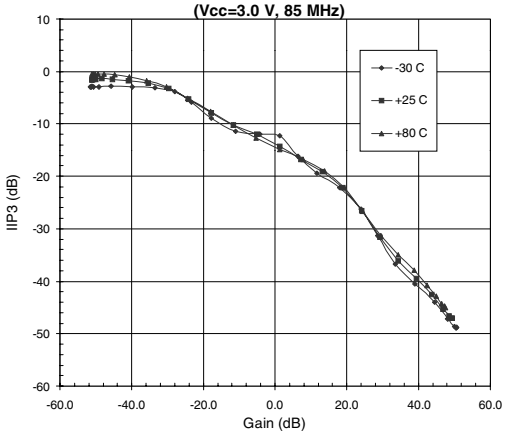
RF2617 Gain vs. Gain Control Voltage (Vcc=3.3 V, 85 MHz)



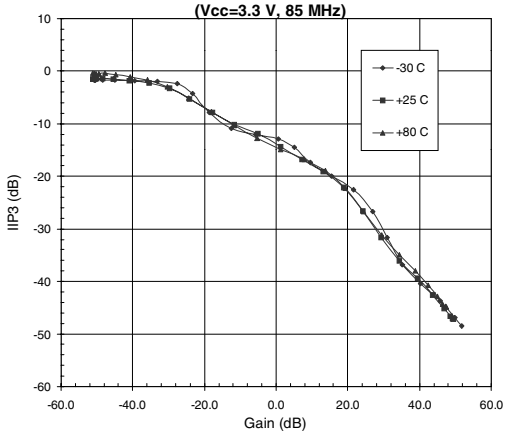
RF2617 IIP3 vs. Gain (Vcc=2.7 V, 85 MHz)



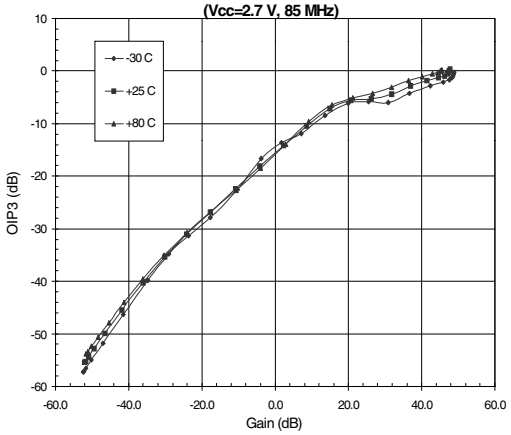
RF2617 IIP3 vs. Gain (Vcc=3.0 V, 85 MHz)



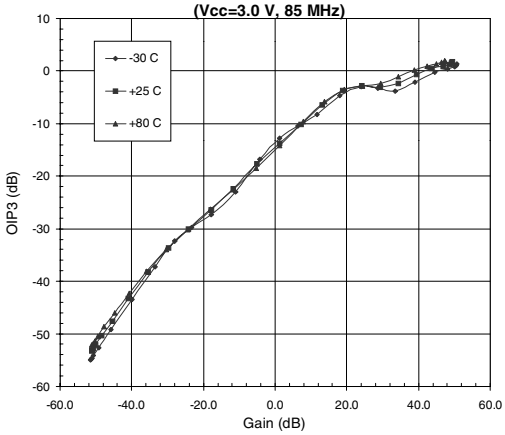
RF2617 IIP3 vs. Gain (Vcc=3.3 V, 85 MHz)



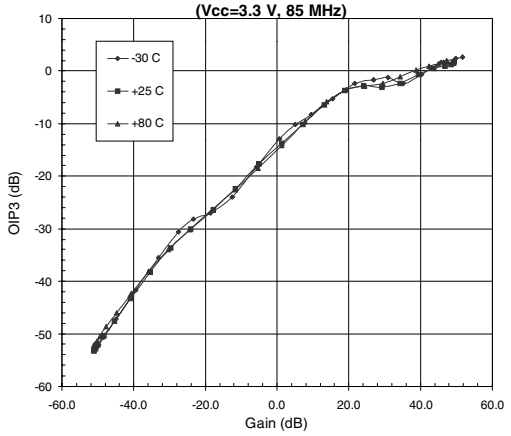
RF2617 OIP3 vs. Gain (Vcc=2.7 V, 85 MHz)



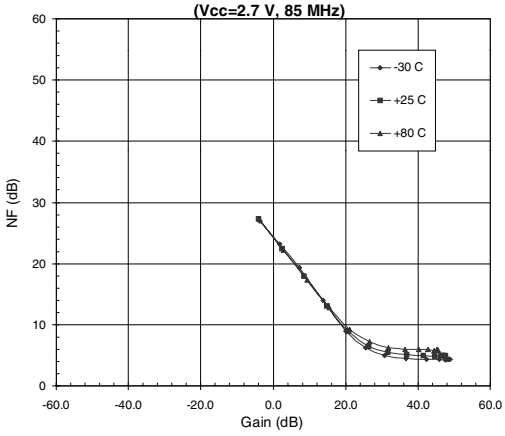
RF2617 OIP3 vs. Gain (Vcc=3.0 V, 85 MHz)



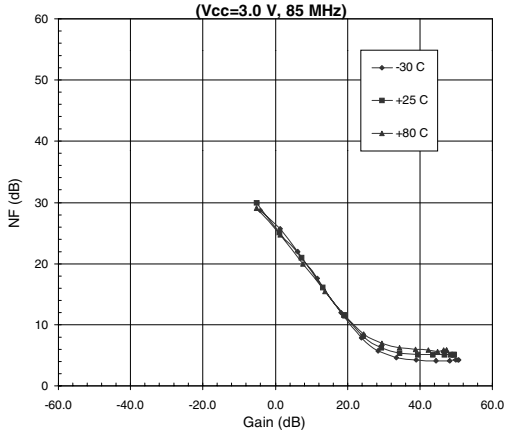
RF2617 OIP3 vs. Gain (Vcc=3.3 V, 85 MHz)



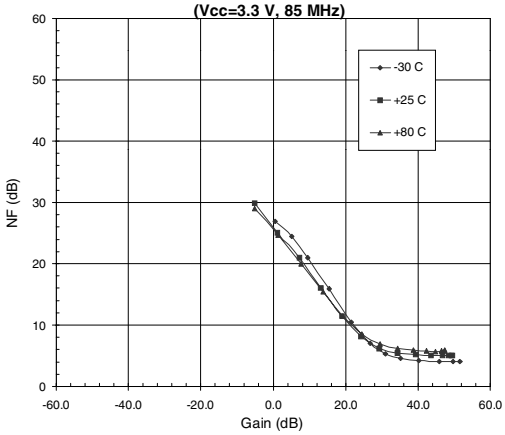
RF2617 NF vs. Gain (Vcc=2.7 V, 85 MHz)



RF2617 NF vs. Gain (Vcc=3.0 V, 85 MHz)



RF2617 NF vs. Gain (Vcc=3.3 V, 85 MHz)



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RF2619

3V CDMA/FM TRANSMIT AGC AMPLIFIER

Typical Applications

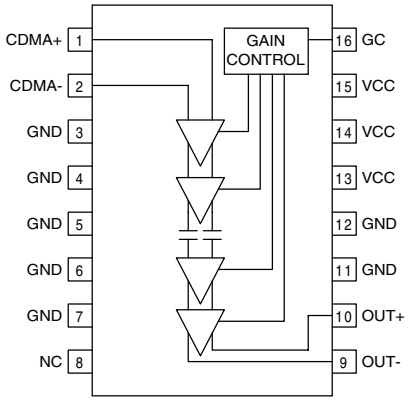
- 3V CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Linear IF Amplifier
- Portable Battery Powered Equipment
- Commercial and Consumer Systems

Product Description

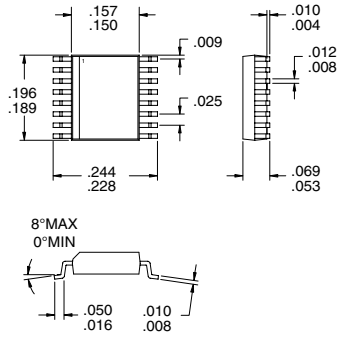
The RF2619 is a complete AGC amplifier designed for the transmit section of 3V dual-mode CDMA/FM cellular applications. It is designed to amplify IF signals while providing more than 84dB of gain control range. Noise Figure, IP3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process and is packaged in a standard miniature 16-lead plastic SSOP package.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-16

Features

- Supports Dual Mode Operation
- -48dB to +42dB Gain Control Range
- Single 3V Power Supply
- Monolithic Construction
- 12MHz to 175MHz Operation
- Miniature Surface Mount Package

Ordering Information

RF2619	3V CDMA/FM Transmit AGC Amplifier
RF2619 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2619

Absolute Maximum Ratings

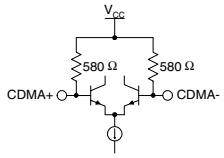
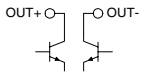
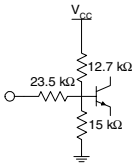
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V
Input Power Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

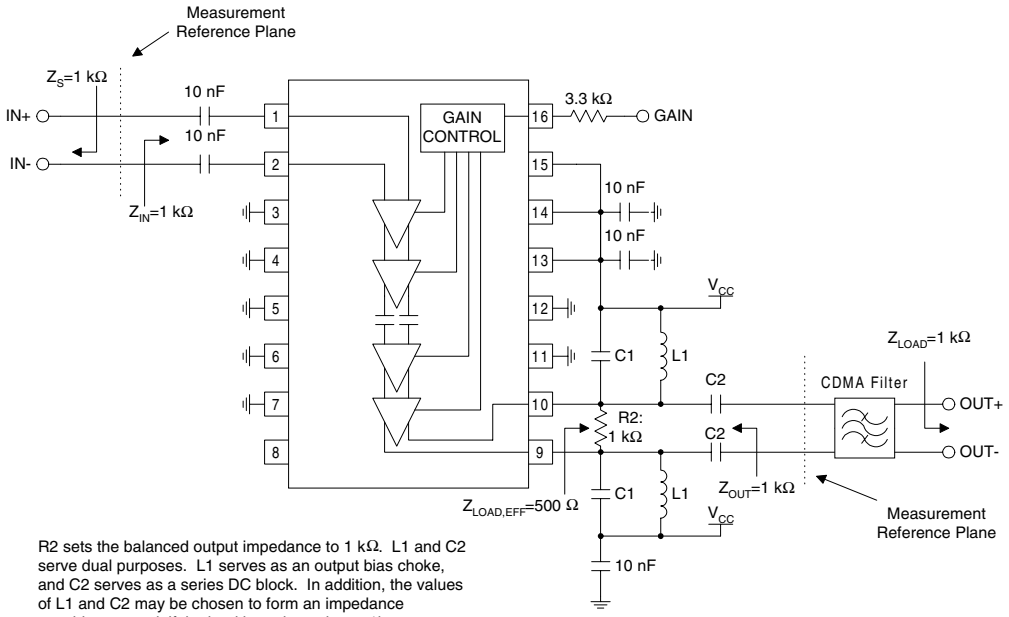
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 130MHz, V_{CC}=3.0V, Pin=-40dBm, Z_S=1kΩ, Z_L=1kΩ, 1kΩ External Output Terminating Resistor (Effective Z_L=500Ω) (See Application Example)
Frequency Range		12 to 175		MHz	
Maximum Gain	+39	+42		dB	V_{GC}=2.4V
Minimum Gain		-48	-45	dB	V_{GC}=0.3V
Gain Slope		57		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V_{DC}	
Gain Control Input Impedance		30		kΩ	
Noise Figure		10.5	13	dB	At maximum gain and 130MHz
Input IP3	-26	-25		dBm	At +10 gain and referenced to 1kΩ, Pin=-45dBm per tone
Input Impedance		1		kΩ	Differential
Stability (Max VSWR)	10:1				Spurious<-70dBm
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		23	25	mA	Maximum gain, V_{CC}=3.0V
Current Consumption		22	24	mA	Minimum gain, V_{CC}=3.0V

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Pin	Function	Description	Interface Schematic
1	CDMA+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level, other than V_{CC}, present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	CDMA-	Same as pin 2, except complementary input.	See pin 1 schematic.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND	Same as pin 3.	
5	GND	Same as pin 3.	
6	GND	Same as pin 3.	
7	GND	Same as pin 3.	
8	NC	No Connection pin. This pin is internally biased and should not be connected to any external circuitry, including ground or V_{CC}.	
9	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 500Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
10	OUT+	Same as pin 9, except complementary output.	See pin 9 schematic.
11	GND	Same as pin 3.	
12	GND	Same as pin 3.	
13	VCC	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Pins 13, 14, and 15 may share one bypass capacitor if trace lengths are kept minimal.	
14	VCC	Same as pin 13.	
15	VCC	Same as pin 13.	
16	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are valid only for a 3.3kΩ DC source impedance.	

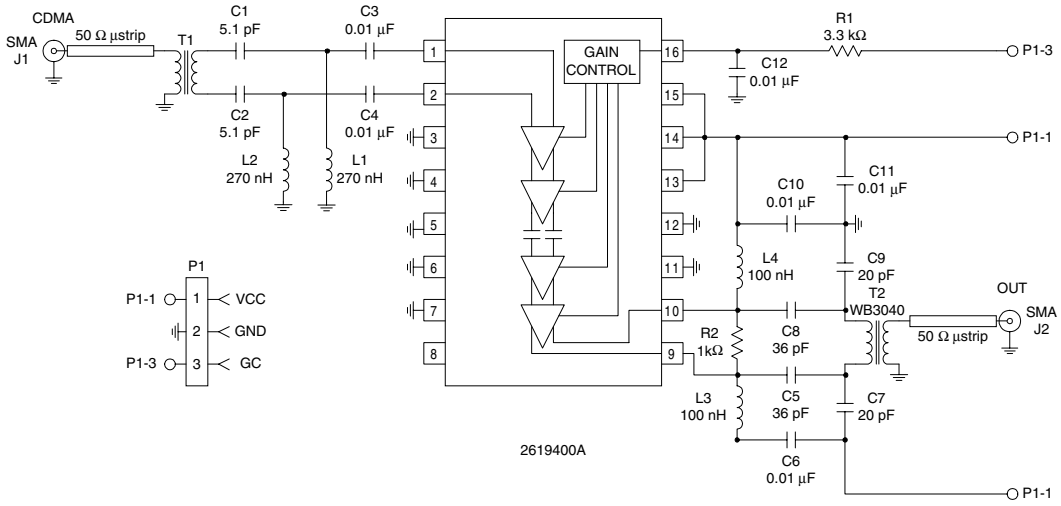
Application Schematic



R2 sets the balanced output impedance to 1 kΩ. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the load impedance is not 1kΩ. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 1 kΩ.

Evaluation Board Schematic

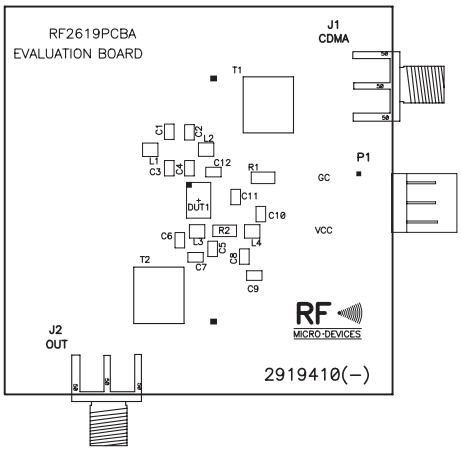
(Download Bill of Materials from www.rfmd.com.)

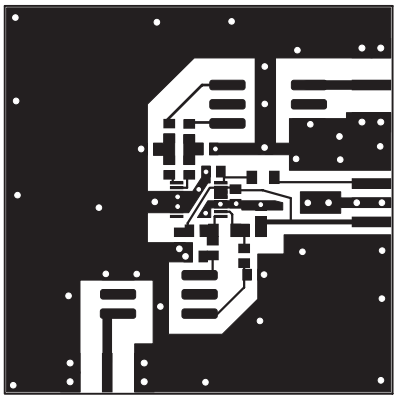


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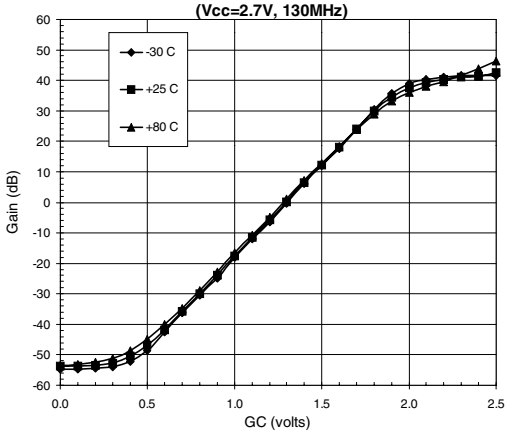
IF AMPLIERS

Evaluation Board Layout

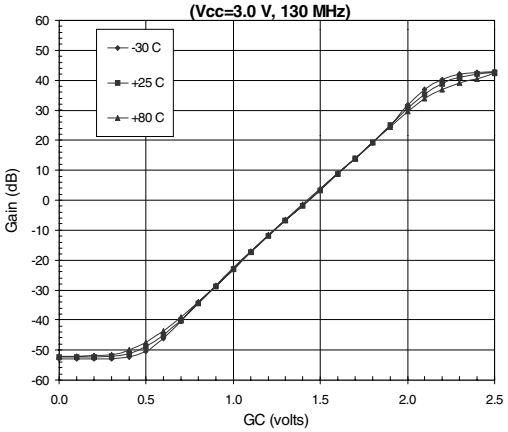




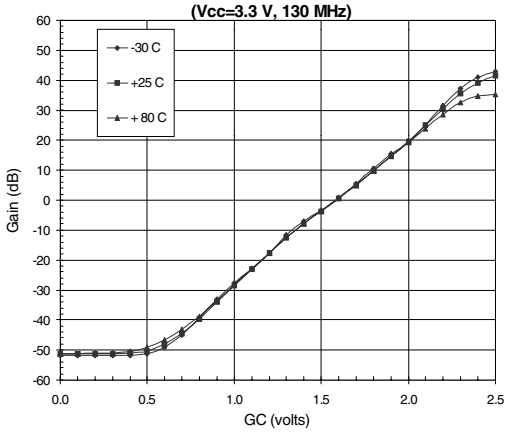
RF2619 Gain vs. Gain Control Voltage (Vcc=2.7V, 130MHz)



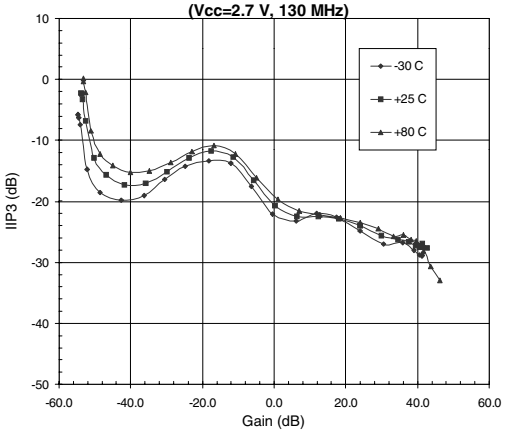
RF2619 Gain vs. Gain Control Voltage (Vcc=3.0 V, 130 MHz)



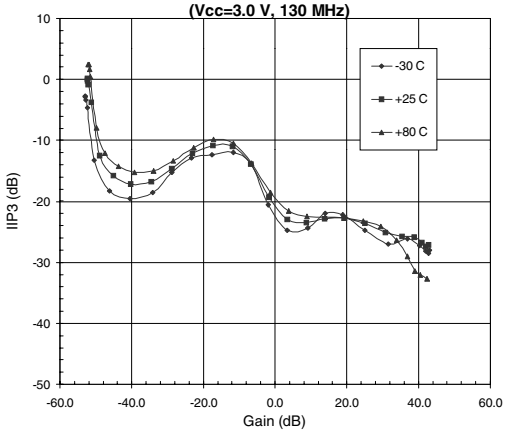
RF2619 Gain vs. Gain Control Voltage (Vcc=3.3 V, 130 MHz)



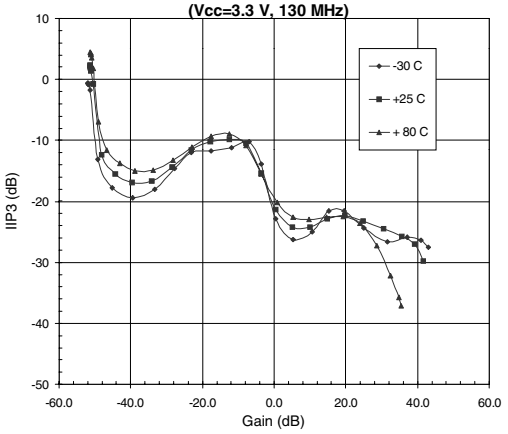
RF2619 IIP3 vs. Gain (Vcc=2.7 V, 130 MHz)



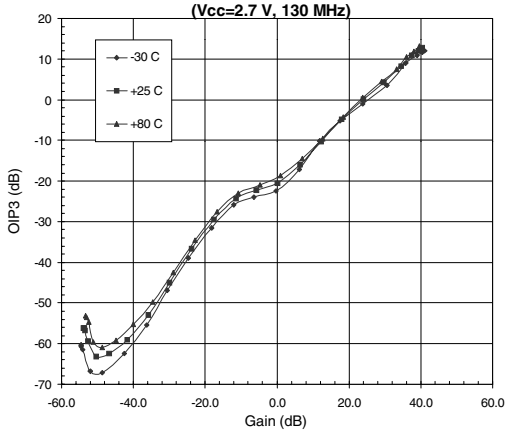
RF2619 IIP3 vs. Gain (Vcc=3.0 V, 130 MHz)



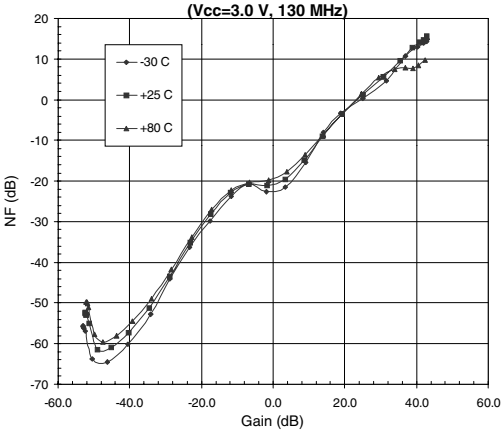
RF2619 IIP3 vs. Gain (Vcc=3.3 V, 130 MHz)



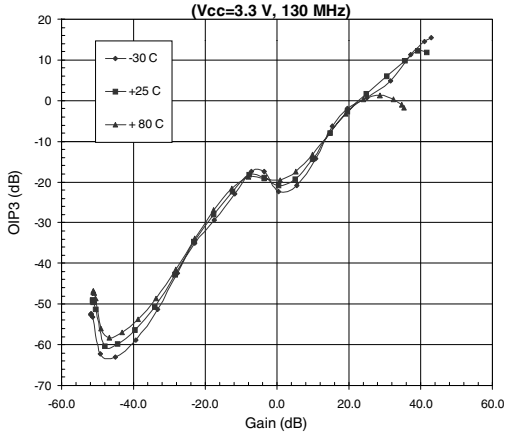
RF2619 OIP3 vs. Gain (Vcc=2.7 V, 130 MHz)



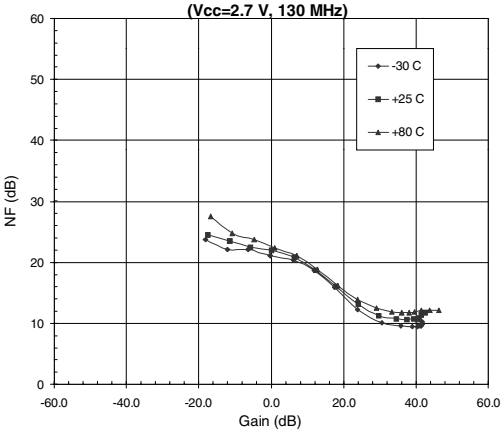
RF2619 OIP3 vs. Gain (Vcc=3.0 V, 130 MHz)



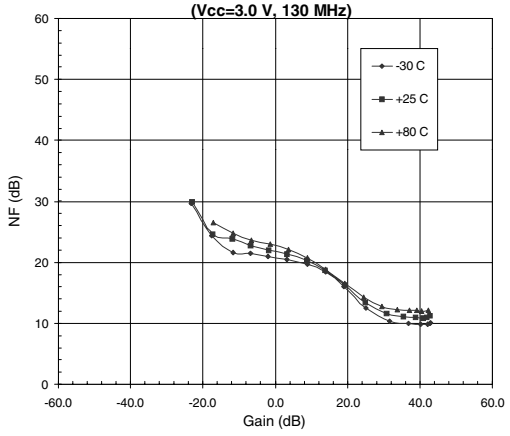
RF2619 OIP3 vs. Gain (Vcc=3.3 V, 130 MHz)



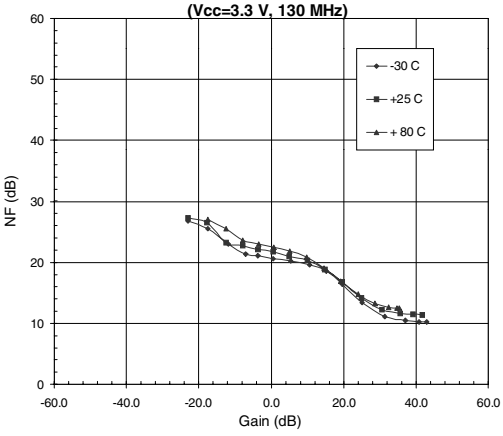
RF2619 NF vs. Gain (Vcc=2.7 V, 130 MHz)



RF2619 NF vs. Gain (Vcc=3.0 V, 130 MHz)



RF2619 NF vs. Gain (Vcc=3.3 V, 130 MHz)



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RF2627

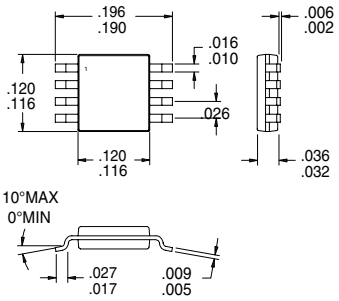
3V CDMA RECEIVE AGC AMPLIFIER

Typical Applications

- 3V CDMA Cellular Systems
- 3V CDMA PCS Systems
- 3V TDMA Cellular/PCS Systems
- General Purpose Linear IF Amplifier
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

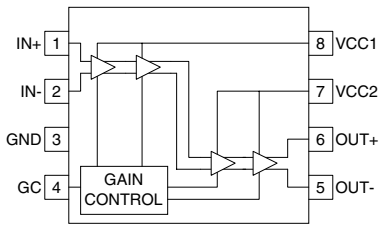
The RF2627 is a complete AGC amplifier designed for the receive section of 3V CDMA cellular and PCS applications. It is designed to amplify IF signals while providing more than 90dB of gain control range. Noise Figure, IP_3, and other specifications are designed for CDMA handsets. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and this Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process, and is packaged in a standard miniature 8-lead plastic MSOP package.



Package Style: MSOP-8

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports PCS and Cellular Applications
- -48dB to +48dB Gain Control Range
- Single 3V Power Supply
- -2dBm Input IP_3
- 12MHz to 285MHz Operation
- Monolithic Construction

Ordering Information

RF2627	3V CDMA Receive AGC Amplifier
RF2627 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

10 IF AMPLIERS

RF2627

Absolute Maximum Ratings

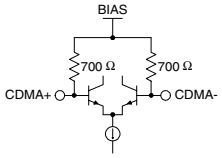
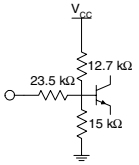
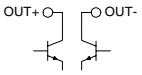
Parameter	Value	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

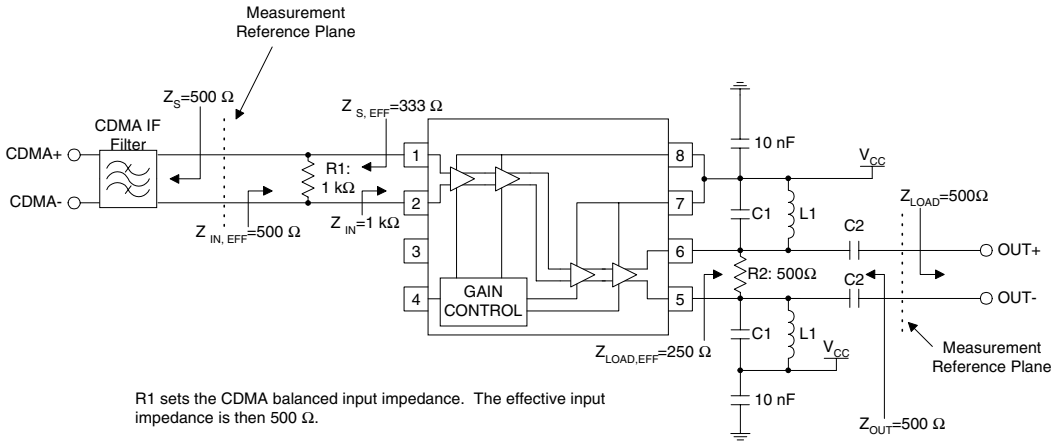
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 85MHz, V_{CC}=3.0V, Z_S =500Ω, Z_L=500Ω, 500Ω External Input Terminating Resistor, 500Ω External Output Terminating Resistor (Effective Z_S=333Ω, Effective Z_L=250Ω) (See Application Example)
Frequency Range		12 to 285		MHz	
Maximum Gain	+45	+48		dB	V_{GC}=2.4V
Minimum Gain		-48	-45	dB	V_{GC}=0.3V
Gain Slope		57		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V_{DC}	Source impedance of 4.7kΩ
Gain Control Input Impedance		30		kΩ	
Noise Figure		5	8	dB	At maximum gain and 85MHz
Input IP_3	-44	-40		dBm	At +40dB gain, referenced to 500Ω
	-4	-2		dBm	At minimum gain, referenced to 500Ω
Stability (Max VSWR)	10:1				Spurious<-70dBm
IF Input					
Input Impedance		1		kΩ	CDMA, differential
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		13	15	mA	Minimum gain, V_{CC}=3.0V
Current Consumption		14	16	mA	Maximum gain, V_{CC}=3.0V

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Pin	Function	Description	Interface Schematic
1	IN+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level other than V_{CC} present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	IN-	Same as pin 2, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are only valid for a 4.7kΩ DC source impedance.	
5	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 250Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
6	OUT+	Same as pin 5, except complementary output.	See pin 5.
7	VCC1	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	VCC2	Same as pin 7.	

Application Schematic

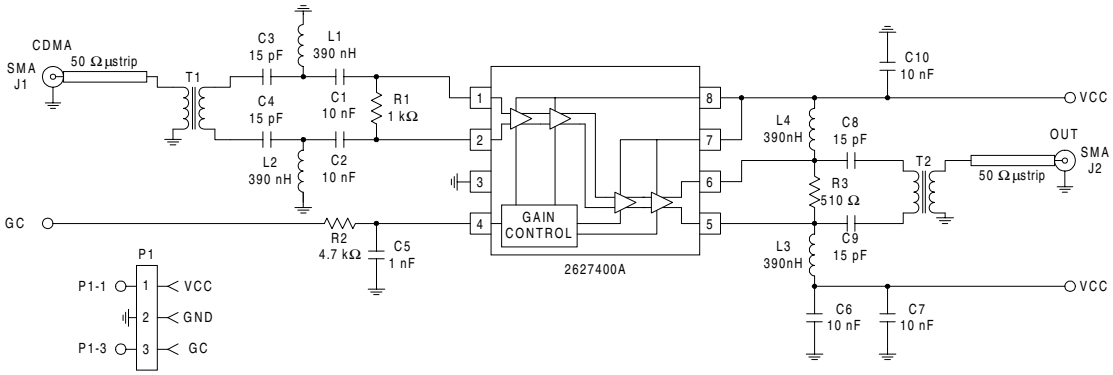


R1 sets the CDMA balanced input impedance. The effective input impedance is then 500 Ω.

R2 sets the balanced output impedance to 500 Ω. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network of the load impedance is not 500 Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the load impedance is 500 Ω.

Evaluation Board Schematic

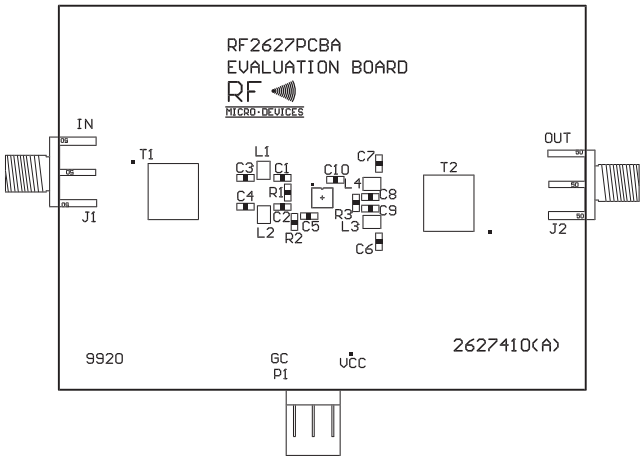
(Download Bill of Materials from www.rfmd.com.)

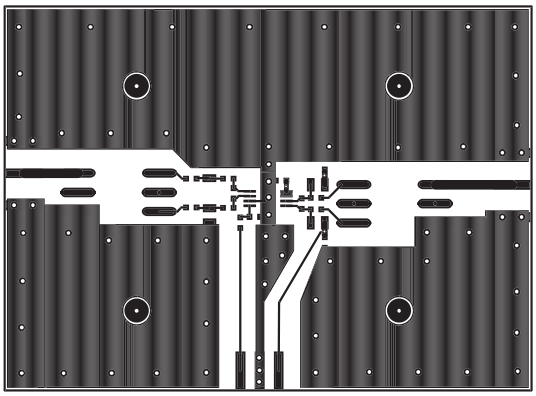


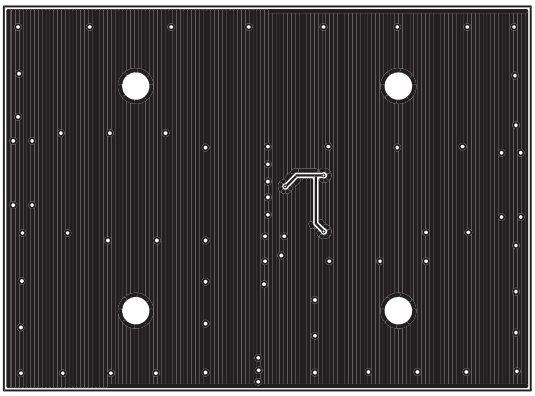
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Evaluation Board Layout
Board Size 2.750" x 2.000"

Board Thickness 0.031”, Board Material FR-4







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RF2629

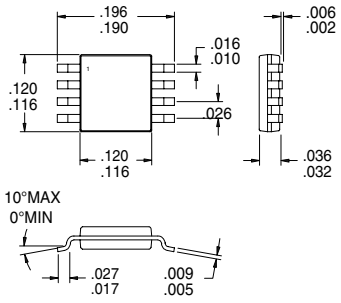
3V CDMA/FM TRANSMIT AGC AMPLIFIER

Typical Applications

- 3V CDMA/FM Cellular Systems
- 3V CDMA PCS Systems
- 3V TDMA Cellular/PCS Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- Portable Battery Powered Equipment

Product Description

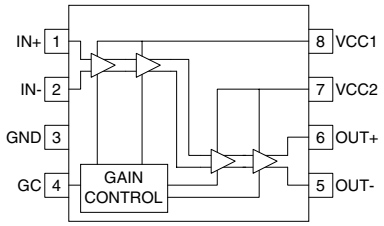
The RF2629 is a complete AGC amplifier designed for the transmit section of 3V dual-mode CDMA/FM cellular and PCS applications. It is designed to amplify IF signals while providing more than 84dB of gain control range. Noise Figure, IP3, and other specifications are designed for CDMA and dual mode CDMA/AMPS handsets. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process and is packaged in a standard miniature 8-lead plastic MSOP package.



Package Style: MSOP-8

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation
- Supports PCS and Cellular Applications
- -48dB to +38dB Gain Control Range
- Single 3V Power Supply
- 12MHz to 175MHz Operation
- Miniature Surface Mount Package

Ordering Information

RF2629	3V CDMA/FM Transmit AGC Amplifier
RF2629 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

10 IF AMPLIERS

RF2629

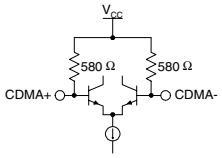
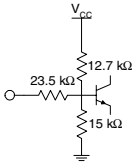
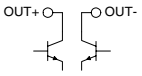
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V
Input Power Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

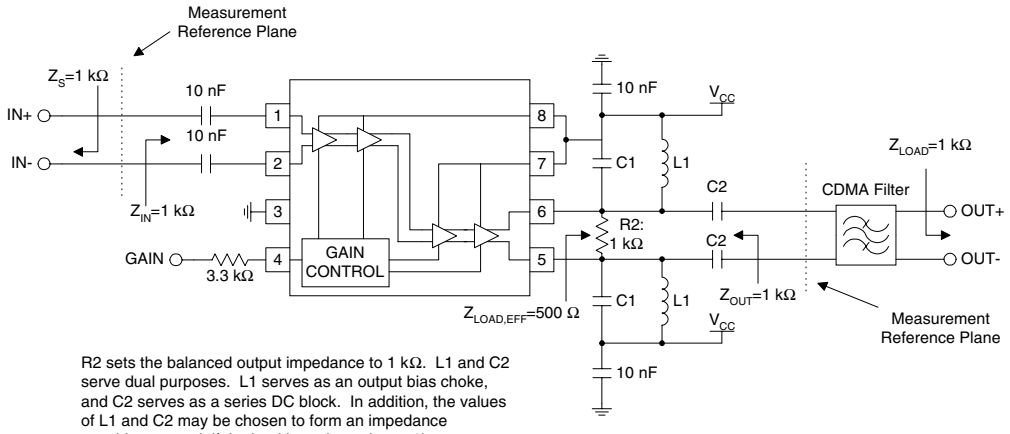
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 130MHz, V_{CC}=3.0V, Pin=-40dBm, Z_S=1kΩ, Z_L=1kΩ, 1kΩ External Output Terminating Resistor (Effective Z_L=500Ω) (See Application Example)
Frequency Range		12 to 175		MHz	
Maximum Gain	+35	+38		dB	V_{GC}=2.3V
Minimum Gain		-48	-45	dB	V_{GC}=0.3V
Gain Slope		57		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 2.4		V_{DC}	
Gain Control Input Impedance		30		kΩ	
Noise Figure		10.5	13	dB	At maximum gain and 130MHz
Input IP3	-26	-25		dBm	At +10dB gain and referenced to 1kΩ, Pin=-45dBm per tone
	-28	-26		dBm	At +35dB gain and referenced to 1kΩ, Pin=-45dBm per tone
Input Impedance		1		kΩ	Differential
Stability (Max VSWR)	10:1				Spurious<-70dBm
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		23	25	mA	Maximum gain, V_{CC}=3.0V
Current Consumption		22	24	mA	Minimum gain, V_{CC}=3.0V

Pin	Function	Description	Interface Schematic
1	IN+	Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level, other than V_{CC}, present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	IN-	Same as pin 2, except complementary input.	See pin 1 schematic.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are valid only for a 3.3kΩ DC source impedance.	
5	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 500Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
6	OUT+	Same as pin 5, except complementary output.	See pin 5 schematic.
7	VCC1	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Pins 7 and 8 may share one bypass capacitor if trace lengths are kept minimal.	
8	VCC2	Same as pin 7.	

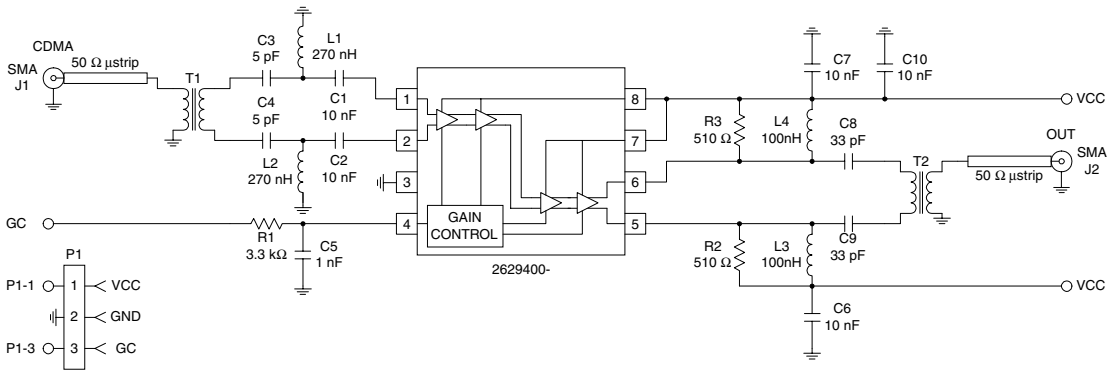
Application Schematic



R2 sets the balanced output impedance to 1 kΩ. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the load impedance is not 1kΩ. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 1 kΩ.

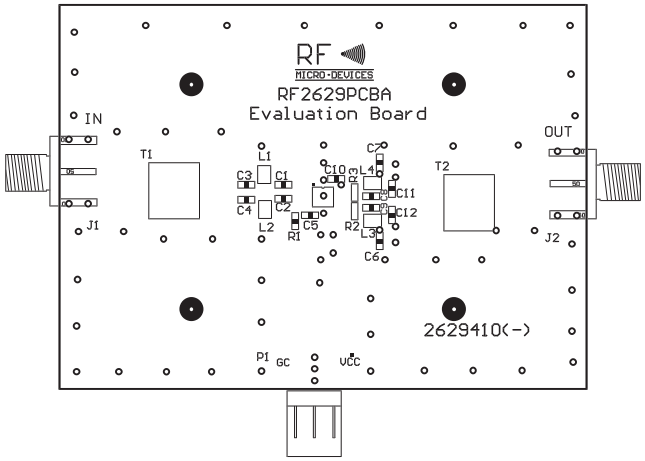
Evaluation Board Schematic

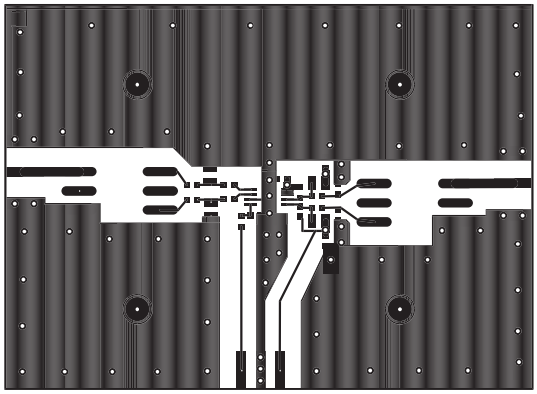
(Download Bill of Materials from www.rfmd.com.)

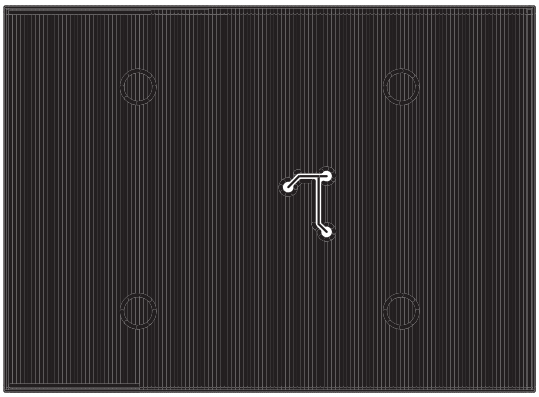


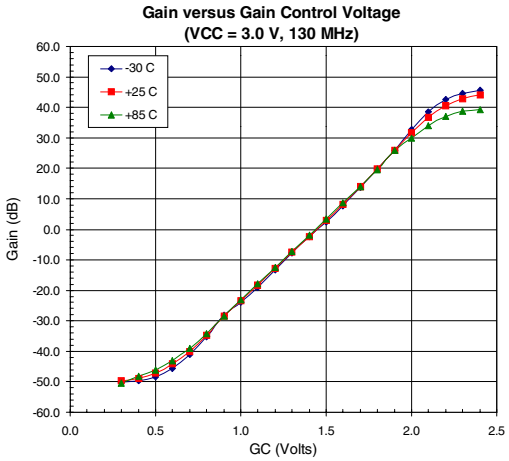
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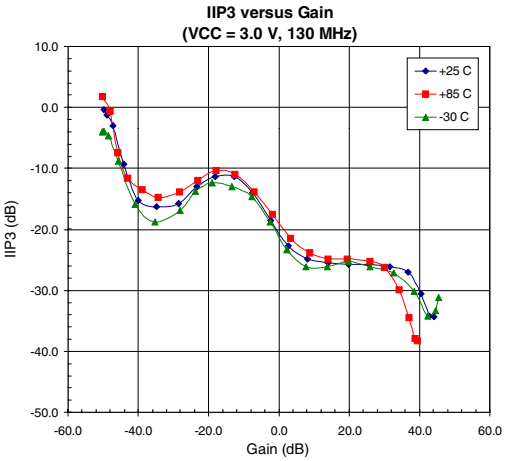
Evaluation Board Layout
Board Size 2.750" x 2.000"








Gain versus Gain Control Voltage
(VCC = 3.0 V, 130 MHz)
-30 C
+25 C
+85 C
Gain (dB)
GC (Volts)
60.0
50.0
40.0
30.0
20.0
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
0.0
0.5
1.0
1.5
2.0
2.5


IIP3 versus Gain
(VCC = 3.0 V, 130 MHz)
+25 C
+85 C
-30 C
IIP3 (dB)
Gain (dB)
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-40.0
-20.0
0.0
20.0
40.0
60.0

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RF MICRO·DEVICES

Preliminary

RF2670

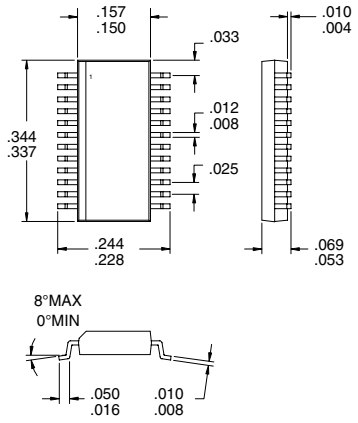
8MHZ DUAL BASEBAND AGC WITH PROGRAMMABLE LOW PASS FILTERING

Typical Applications

- Digital Cordless Telephones
- Secure Communication Links
- Wireless LANs
- Inventory Tracking
- Wireless Security
- Battery Powered Applications

Product Description

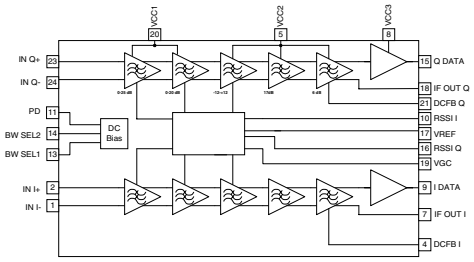
The RF2670 is a monolithic integrated circuit specifically designed for direct conversion to baseband QPSK receivers. The part provides dual baseband amplifiers with a 70dB gain range (single pin analog input) and separate I and Q RSSI. On-chip programmable baseband filters are incorporated into each amplifier providing 1MHz, 2MHz, 4MHz, or 8MHz bandwidth with a 5-pole Bessel response. I and Q output are available in digital or analog form. The data comparators use a self generated DC reference to track DC offsets in the received signal. The analog outputs have a 500mVpp swing with approximately 1.7V DC offset. A 2.0V reference voltage is also available for A/D converters changing DC bias.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- I/Q Baseband Receivers
- 10dB to 80dB Gain Range
- Digital and Analog Outputs
- On-Chip Selectable IF Bandwidths
- Reference Voltage for A/D Converter
- 2.7V to 3.6V Operation

Ordering Information

RF2670	8MHz Dual Baseband AGC with Programmable Low Pass Filtering
RF2670PCBA	Fully Assembled Eval Board.

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+20	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Baseband Amplifiers					T=25°C, V_{CC}=3.0V
Frequency Range	0.01		8	MHz	Minimum frequency is dependent upon input blocking cap, DC feedback cap, and gain setting. Recommended components yields a minimum frequency of less than 10kHz.
Voltage Gain	77	80	83	dB	
Noise Figure		5		dB	At maximum gain setting
		35		dB	At minimum gain setting
Input IP3		-65		dBm	At maximum gain setting
		+2		dBm	At minimum gain setting
Output DC offset		0	25	mV	
Gain Control Range	65	70		dB	
Gain Control Voltage Range	1.2		2.0	V	
Gain Control Sensitivity		-0.08		dB/mV	
VGA Output Voltage		500		mV_{PP}	
VGA DC Output Voltage		1.7		V	
Output P1dB	1	1.64		V_{PP}	Driving a 5kΩ load
RSSI Range	55	60		dB	At maximum gain setting
RSSI Output Voltage Compliance		0.5 to 2.4		V	Maximum RSSI is 2.5V or V_{CC}-0.3, whichever is less.
Input Impedance	1.5	2	2.5	kΩ	Differential
Integrated Filters					
Characteristics		Five pole Bessel			Five pole Bessel internal LPF. Three pole external LPF.
Bandwidth		1, 2, 4, 8		MHz	Selectable from 1MHz, 2MHz, 4MHz, and 8MHz.
Passband Ripple			1	dB	
Group Delay			100	ns	At 8MHz, increasing as bandwidth decreases.
Ultimate Rejection	50	80		dB	
Data Amplifiers					
Voltage Gain		100		dB	
Bandwidth	8			MHz	
Rise and Fall Time		2	5	ns	5pF Load
Logic High Output	V_{CC}-0.3V			V	Can sink/source 1mA and maintain these logic levels.
Logic Low Output			0.3	V	Can sink/source 1mA and maintain these logic levels.
Hysteresis		40		mV	
Power Down Control					
Logical Controls “ON”	V_{CC}-0.3V			V	Voltage supplied to the input
Logical Controls “OFF”			0.3	V	Voltage supplied to the input
Control Input Impedance		>1		MΩ	
Turn on Time		10	13	ms	With recommended DC feedback cap (270nF)

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Voltage	2.7	3.0	3.6	V	
Current Consumption		13	17	mA	V_{CC}=3.0V; PD=High
			1	µA	V_{CC}=3.0V; Sleep Mode, PD=Low

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Pin	Function	Description	Interface Schematic
1	IN I-	Complementary input for the in-phase IF channel.	
2	IN I+	Input for the in-phase IF channel.	
3	GND2	Ground for VCC2.	
4	DCFB I	DC feedback capacitor for in-phase channel.	
5	VCC2	Power supply for VGA amplifier 3, differential to single-ended converter, and post filter.	
6	GND3	Ground for VCC3.	
7	IF OUT I	Analog signal IF output for in-phase channel.	
8	VCC3	Power supply for data amplifier.	
9	I DATA	Logic-level data output for the in-phase channel. This is a digital output signal obtained from the output of a Schmitt trigger.	
10	RSSI I	Received signal strength indicator for the in-phase channel.	
11	PD	Enable pin for the receiver circuits. PD>2.0V powers up all of the functions. PD<1.0V turns off all of the functions.	
12	GND1	Ground for VCC1 for both the in-phase and quadrature channels.	
13	BW SEL1	Bandwidth select logic input. Pin 13 and pin 14 provide a two bit control word for the setting of the IF bandwidth. See Table1. Additional filtering should be used at the amplifiers to precisely control the 3dB bandwidth of the system. See design information details about differential input filters.	
14	BW SEL2	See pin 13.	
15	Q DATA	Logic-level data output for the quadrature channel. This is a digital output signal obtained from the output of a Schmitt trigger.	
16	RSSI Q	Received signal strength indicator for the quadrature channel.	
17	VREF	Gain control reference voltage.	
18	IF OUT Q	Analog signal IF output for quadrature channel.	
19	VGC	Gain control voltage.	
20	VCC1	Power supply for bias circuits and VGA amplifiers for both the in-phase and quadrature channels.	
21	DCFB Q	DC feedback capacitor for quadrature channel.	
22	GND1	Ground for VCC1 for both the in-phase and quadrature channels.	
23	IN Q+	Plus input for quadrature channel	
24	IN Q-	Minus input for quadrature channel	

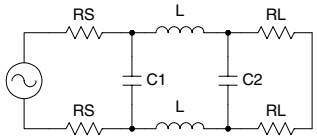
Table 1: Bandwidth Selection Controls

BWSEL1	BWSEL2	IF_{-3dB} Frequency
0	0	1MHz
0	1	2MHz
1	0	4MHz
1	1	8MHz

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Differential Filter Design Information

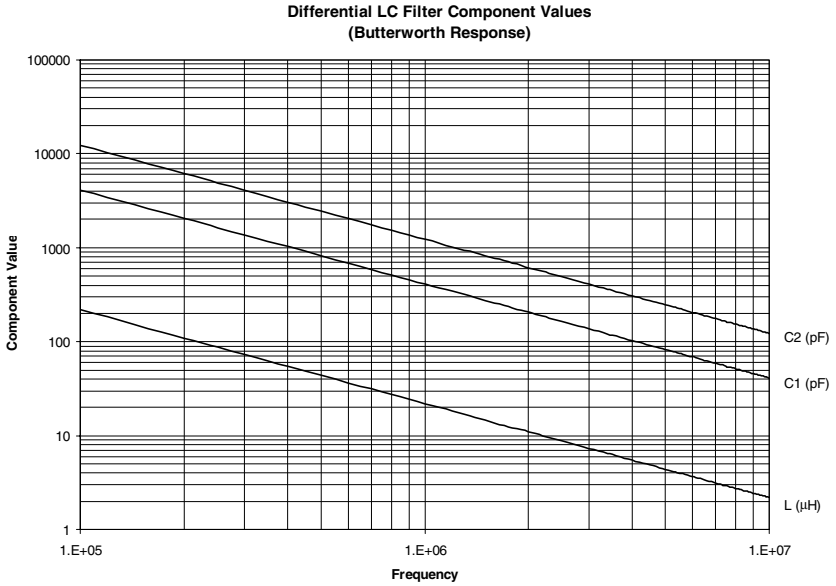
Butterworth Response



$$C1 = \frac{C1bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; C2 = \frac{C2bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; L = \frac{Lbw \cdot RL \cdot 10^{6}}{2 \cdot \pi \cdot fc}$$

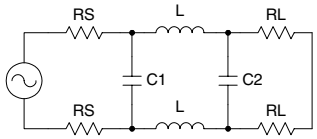
$$C1bw = 5.1672; C2bw = 15.4554; Lbw = 0.1377$$

$$RS = 125; RL = 1000; \frac{RS}{RL} = 0.125$$



Differential Filter Design Information (Cont.)

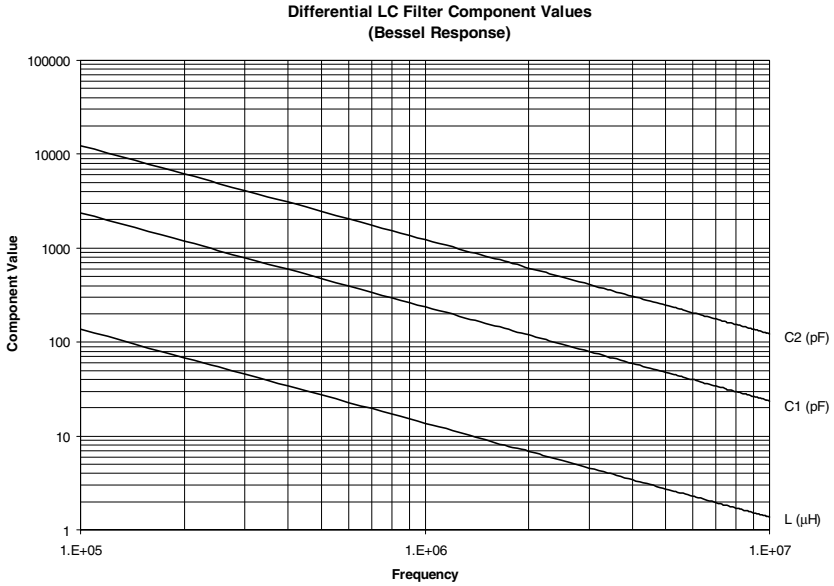
Bessel Response



$$C1 = \frac{C1bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; C2 = \frac{C2bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; L = \frac{Lbw \cdot RL \cdot 10^{6}}{2 \cdot \pi \cdot fc}$$

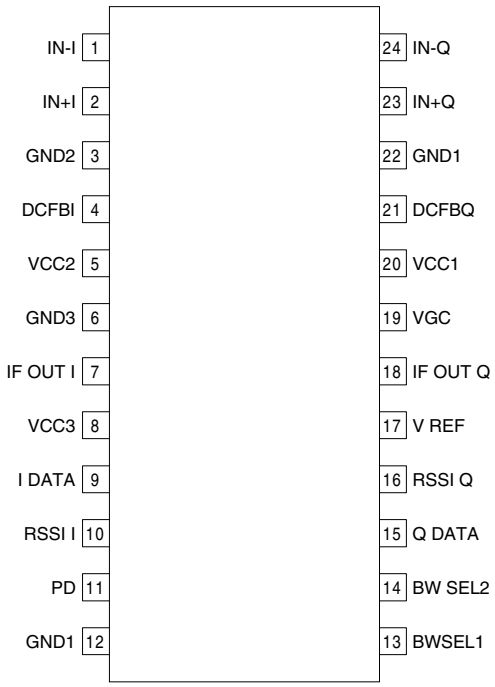
$$C1bw = 2.9825; C2bw = 15.4697; Lbw = 0.0860$$

$$RS = 125; RL = 1000; \frac{RS}{RL} = 0.125$$



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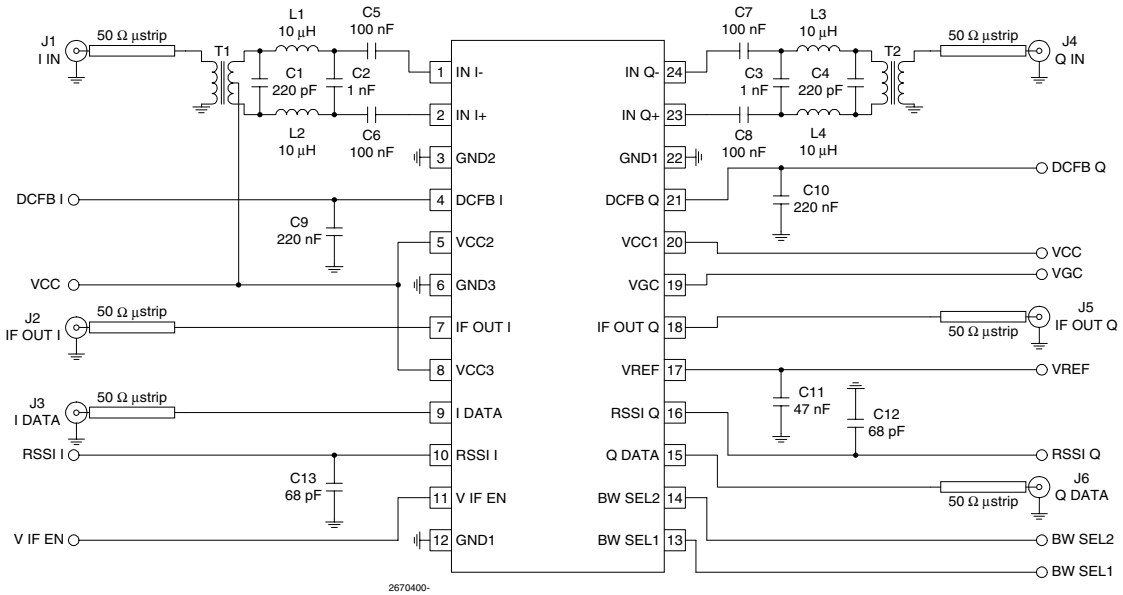
Pin Out

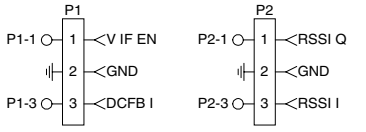


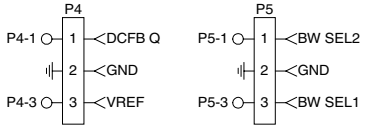
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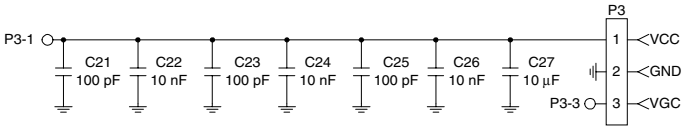
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)







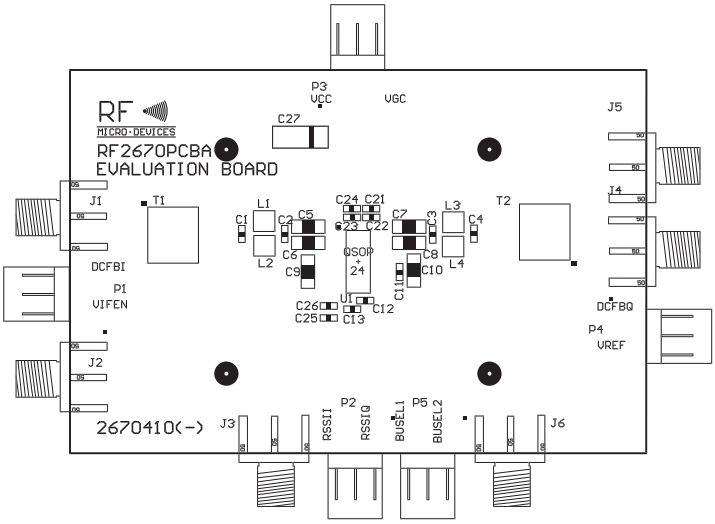


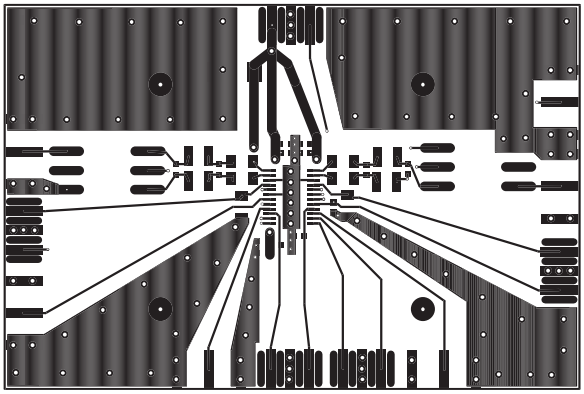
L1-L4 and C1-C4 make two LPFs. The fc of the RF2670 is variable; therefore the L and C components must be variable. The following table gives recommended component values ("std" indicates standard eval board value).

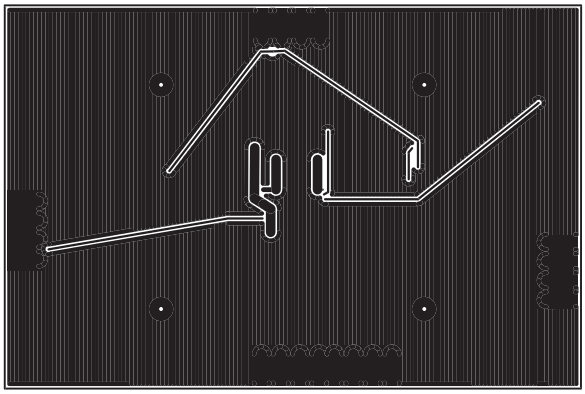
Desired BW	BW1, BW2	C1, C4 (pF)	C2, C3 (pF)	L1-L4 (μH)
700 kHz	0 0	330	1800	22
1.4 MHz	0 1	220 (std)	1000 (std)	10
2.8 MHz	1 0	100	470	4.7
7.0 MHz	1 1	33	180	2.2

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Evaluation Board Layout
Board Size 3.0” x 2.0”



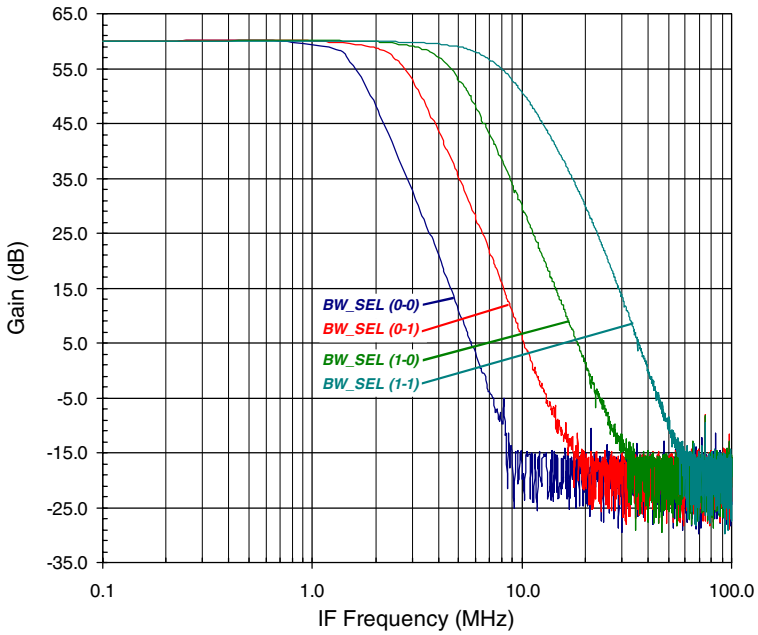




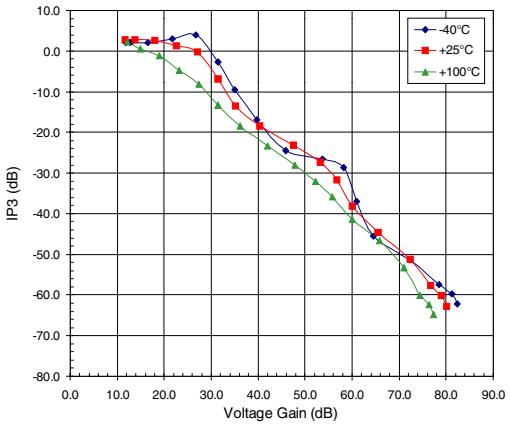
10

IF AMPLIERS

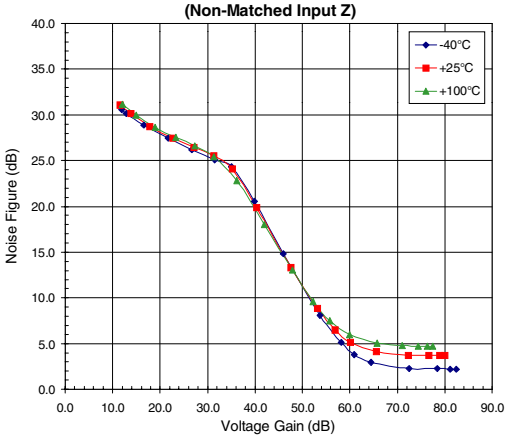
RF2670 IF Bandwidth Response



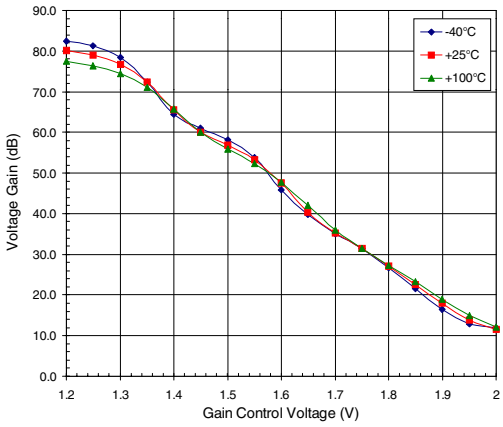
IIP3 versus Voltage Gain



Noise Figure versus Voltage Gain (Non-Matched Input Z)



Voltage Gain versus Gain Control Voltage



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RF2903

INTEGRATED SPREAD SPECTRUM RECEIVER

Typical Applications

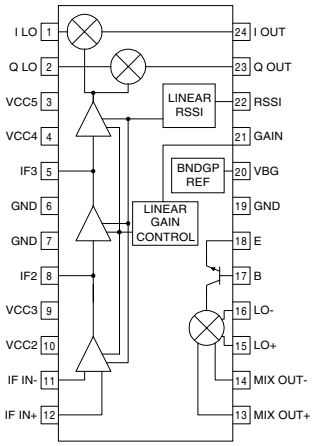
- Spread Spectrum Systems
- Dual-IF Strip for PCS and 2.4 GHz ISM Band Receivers
- Dual Mode Digital/Analog Receivers
- POS Terminals
- Commercial Handheld Systems

Product Description

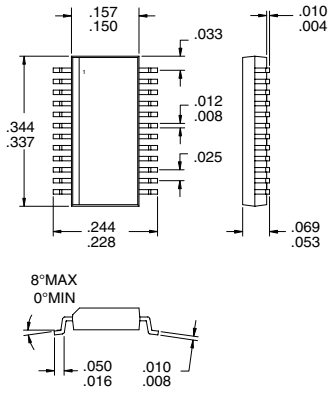
The RF2903 spread spectrum receiver IC includes an RF front-end with an RF pre-amp and mixer, a variable-gain IF section with RSSI, and a demodulator section. The front-end can accept inputs from 150MHz to 1000MHz and is suitable for ISM band receivers and the first IF stage in superheterodyne receivers. The IF amplifier provides up to 90dB of gain up to 200MHz, controlled with an analog voltage. A Received Signal Strength Indicator (RSSI) is present for power level detection. Two double-balanced mixers are provided which may be configured for quadrature demodulation, FM/FSK discrimination, or AM detection. AM detection is accomplished with an external detector circuit. An internal band-gap reference maintains consistent performance over temperature and power supply voltage.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-24

Features

- 3V to 6V Operation
- FM, PM, or Quadrature Demodulation
- Linear Analog Gain Control and RSSI
- DC to 50MHz I/Q Frequency
- 10 to 200MHz IF, 150 to 1000MHz RF
- Stable Biasing Via Band-Gap Reference

Ordering Information

RF2903	Integrated Spread Spectrum Receiver
RF2903 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2903

Absolute Maximum Ratings

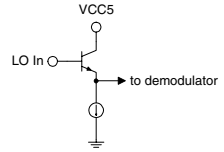
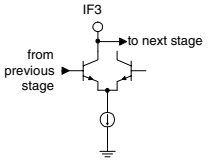
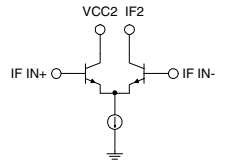
Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.5	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

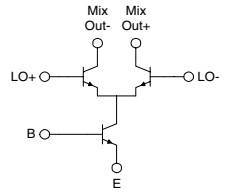
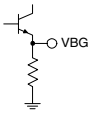
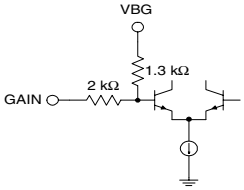
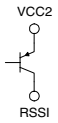
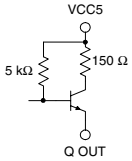
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=350MHz, L01=400MHz, LO2=55MHz
Conversion Gain	87	90	100	dB	RF=350MHz
		84		dB	RF=900MHz
Input IP_3		-10		dBm	Common emitter configuration
Input IP_3		0		dBm	Common base configuration
Cascade Noise Figure		5		dB	RF=300MHz, CE configuration
		14		dB	RF=900MHz, CE configuration
Input Section					
Frequency Range		150 to 1000		MHz	
Conversion Gain		11		dB	RF=350MHz
		5		dB	RF=900MHz
Noise Figure		4		dB	RF=350MHz
		13.5		dB	RF=900MHz
Input VSWR		2:1			
First LO					
Frequency Range		10 to 1200		MHz	
Input Level		0		dBm	Driven single-ended, resistively matched
LO Input Impedance	set by external components			Ω	
IF Section					
Frequency Range		10 to 200		MHz	
Input Impedance		>5 || <2pF		kΩ	
Noise Figure		10		dB	50MHz, 500Ω source impedance, max gain
Input IP3		+3		dBm	50MHz, minimum gain
Gain Range		0 to 79		dB	Driven single-ended
Gain Control Voltage Range		0.6 to 1.6		V	
Gain Control Speed		100		ns	Minimum gain to maximum gain
RSSI DC Output Range		0.6 to 2		V	
RSSI Input Resolvable Range		80		dB	
RSSI Sensitivity		20		mV/dB	
RSSI Linearity		±3		dB	
I/Q Demodulator					
LO Input Level		0		dBm	Resistively matched
LO Input Impedance	set by external components			Ω	
Output Frequency Range		DC to 90		MHz	
Saturated Output Voltage		1.5		V_{PP}	
Amplitude Balance		0.2	1.0	dB	This performance will also be affected by the accuracy of the external phase shift network.
Phase Error		1		°	This performance will also be greatly affected by the accuracy of the external phase shift network.
DC Offset		20		mV	Between I and Q
Power Supply					
Voltage		5		V	Specifications
		3 to 6		V	Operating limits
Band-Gap Reference Voltage	1.58	1.63	1.68	V	
Current	15	23	25	mA	V_{CC}=5.0V

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Pin	Function	Description	Interface Schematic
1	I LO	I-Channel demodulation mixer LO input (High Impedance). This pin is NOT internally DC blocked. This pin must be connected to V_{CC} through a matching inductor or resistor (see the application schematic). An external blocking capacitor should be supplied if a DC voltage, other than V_{CC}, is present on the device driving this input. In order to cause this mixer to operate in a "pass through" mode (no mixing), this pin is DC biased with an external resistor divider that applies a voltage at least 1.4V below V_{CC}, and then I OUT (pin 24) will be the same signal as is present at the IF3 amplifier output.	
2	Q LO	Q Channel demodulation mixer LO input (High Impedance). This pin is NOT internally DC blocked. This pin must be connected to V_{CC} through a matching inductor or resistor (see the application schematic). Otherwise, an external blocking capacitor should be supplied if a DC voltage, other than V_{CC}, is present on the device driving this input. In order to cause this mixer to operate in a "pass through" mode (no mixing), this pin may be connected to ground, and Q OUT (pin 23) will be the same signal as is present at the IF3 amplifier output.	See pin 1.
3	VCC5	Voltage supply for the I and Q demodulation mixers. This pin should be well bypassed at IF and Baseband frequencies.	
4	VCC4	Voltage supply for the IF3 amplifier stage. This pin should be well bypassed at IF frequencies.	
5	IF3	IF2 Output/ IF3 Input pin. This pin must be connected to V_{CC} through an inductor to provide DC bias for IF2's output and IF3's input. The inductance at this pin should be parallel resonated with a capacitor in order to form a noise band-limiting tank circuit. A resistor may be placed in parallel with the tank circuit in order to adjust the tank's bandwidth, but the net gain of the device may be reduced if the value of the resistor is too small.	
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	GND	Same as pin 6.	
8	IF2	IF1 Output/ IF2 Input pin. This pin must be connected to V_{CC} through an inductor to provide DC bias for IF1's output and IF2's input. The inductance at this pin should be parallel resonated with a capacitor in order to form a noise band-limiting tank circuit. A resistor may be placed in parallel with the tank circuit in order to adjust the tank's bandwidth, but the net gain of the device may be reduced if the value of the resistor is too small.	See pin 5.
9	VCC3	Voltage supply for the IF2 amplifier stage. This pin should be well bypassed at IF frequencies. Pins 9 and 10 can share common bypass capacitors.	
10	VCC2	Voltage supply for the IF1 amplifier stage. This pin should be well bypassed at IF frequencies. Pins 9 and 10 can share common bypass capacitors.	
11	IF IN-	IF1 Amplifier differential input (High Impedance). This pin must be connected to V_{CC} through an inductor to provide DC bias to IF1's input. If an IF filter is not used before this input, then a single inductor may be used to bias pins 11 and 14, and the inductance at this pin should be parallel resonated with a capacitor in order to form a noise band-limiting tank circuit (see the application circuit). For single-ended input operation, the unused balanced input pin must be connected to V_{CC} and well bypassed at the IF frequency.	
12	IF IN+	Same as pin 11, except complementary input.	See pin 11.

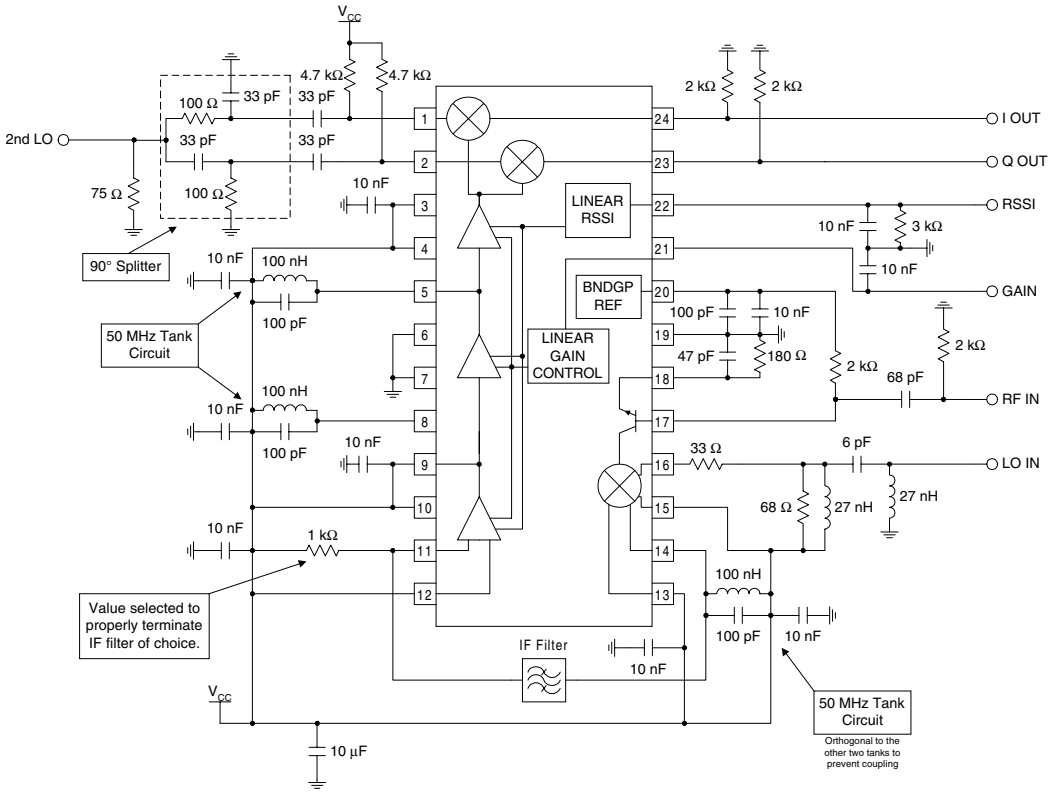
RF2903

Pin	Function	Description	Interface Schematic
13	MIX OUT+	RF mixer output. Pins 13 and 14 are open-collector, complementary outputs. This pin must be connected to V_{CC} through an inductor to provide DC bias for the mixer. If operating in the single-ended mode, either output may be used, but both must be DC connected to V_{CC}. The unused output should be bypassed at LO and IF frequencies. Keep in mind that for single-ended operation, the mixer's gain is 6dB lower (1/2 of the output voltage is not used).	
14	MIX OUT-	Same as pin 13, except complementary output.	See pin 13.
15	LO+	RF Mixer LO differential input (High Impedance). This pin must be connected to V_{CC} through an inductor or a resistor to provide DC bias for the mixer. If operating in the single-ended mode, either LO input may be used, but both must be DC connected to V_{CC}. The unused input should be bypassed at RF, LO, and IF frequencies.	See pin 13.
16	LO-	Same as pin 15, except complementary input.	See pin 13.
17	B	RF input pin (High Impedance). This is the base of an RF transistor used as a pre-amplifier. This pin must be properly biased. In most applications, biasing is accomplished by resistively connecting this pin to the band-gap reference at pin 20 though a ~2kΩ resistor.	See pin 13.
18	E	Emitter of the RF transistor. This pin should be AC coupled to ground with a RF bypass capacitor. In most applications, a 180Ω resistor to ground is used for the appropriate biasing and DC feedback level.	See pin 13.
19	GND	Same as pin 6.	
20	BG OUT	Band Gap voltage reference output. This voltage output (1.6V) is held constant over variations in supply voltage and operating temperature and may be used as a reference for other external circuitry. This pin should not be loaded such that the sourced current exceeds 1mA. This pin should be well bypassed.	
21	GC	Analog gain control pin. The DC voltage applied to this pin determines the gain of all three IF amplifiers. Minimum gain occurs when 0V is applied. Maximum gain occurs when approximately 2.5V is applied (for V_{CC}=5V).	
22	RSSI	Received Signal Strength Indicator. The DC voltage at this pin is proportional to the level of signal (in dB) present in all three IF amplifiers. A capacitor should be placed on this pin to eliminate ripple. A resistor is required to generate the RSSI voltage.	
23	Q OUT	Q Channel demodulation mixer Baseband output. This is an emitter-follower output with an open emitter. DC resistance to ground must be provided by the load. If the load has DC present, a series DC blocking capacitor and a shunt loading resistor must be provided. The single-ended output impedance is ~50Ω. These outputs are designed, however, to drive high impedance loads, and the total voltage gain of the part will be higher for larger values of a loading resistor.	

Pin	Function	Description	Interface Schematic
24	I OUT	I Channel demodulation mixer Baseband output. This is an emitter-follower output with an open emitter. DC resistance to ground must be provided by the load. If the load has DC present, a series DC blocking capacitor and a shunt loading resistor must be provided. The single-ended output impedance is ~50Ω. These outputs are designed, however, to drive high impedance loads, and the total voltage gain of the part will be higher for larger values of a loading resistor.	See pin 23.

Application Schematic

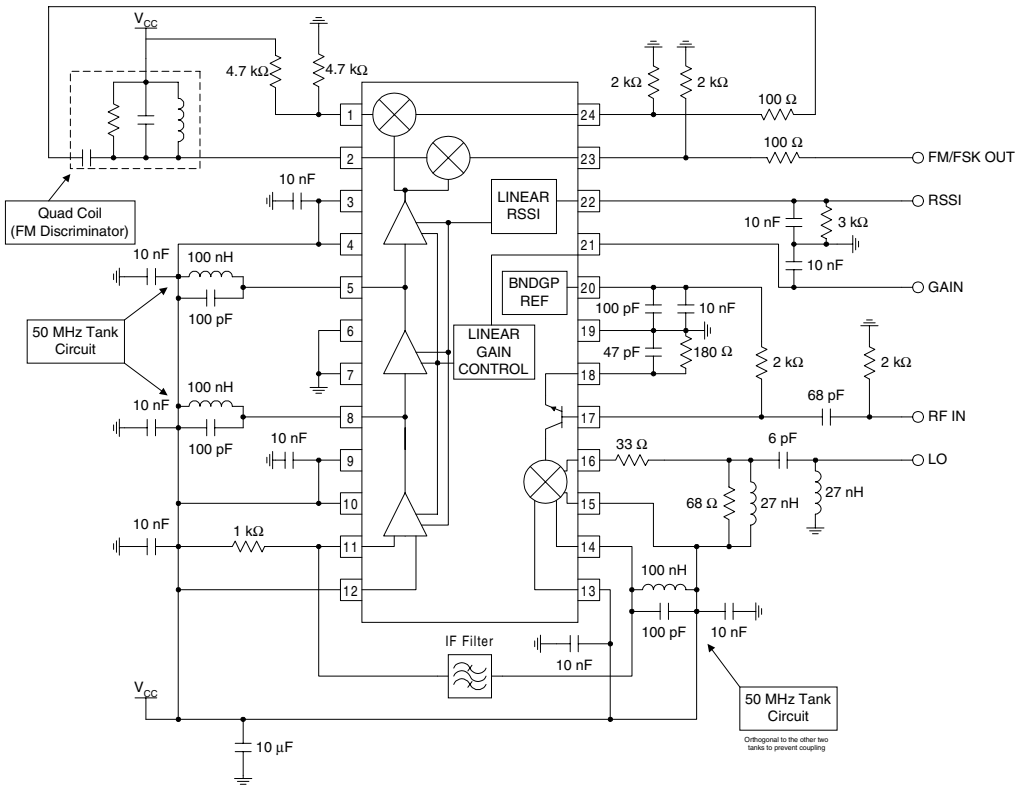
Quadrature Demodulation
900MHz RF and 50MHz IF Operation



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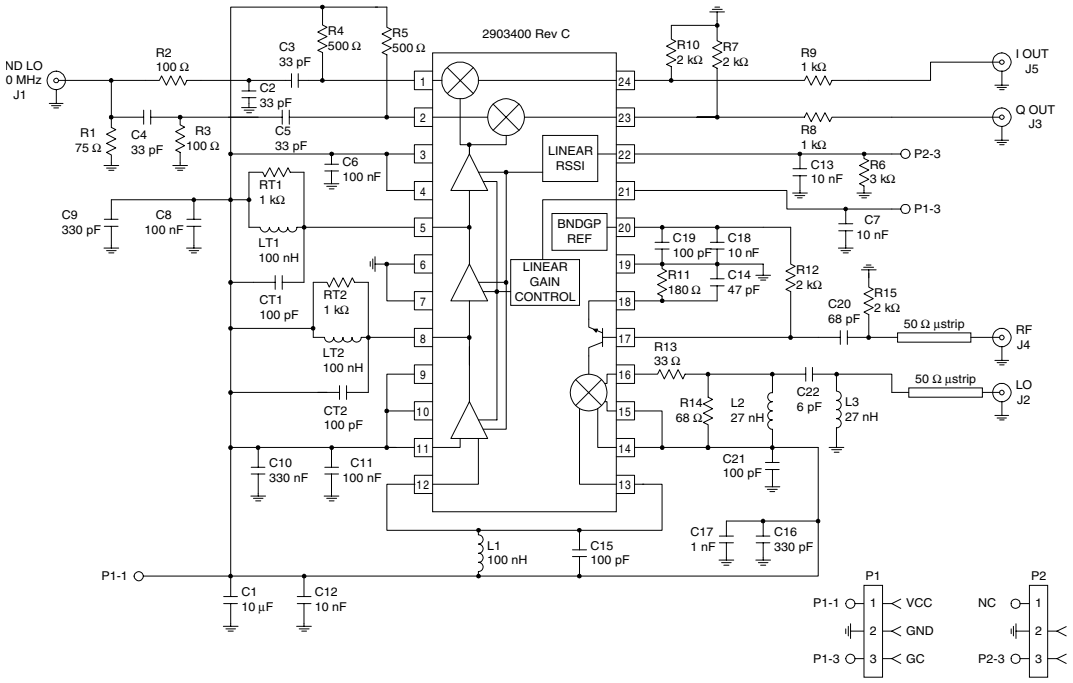
Application Schematic

FM/FSK Demodulation
900MHz RF and 50MHz IF Operation



Evaluation Board Schematic

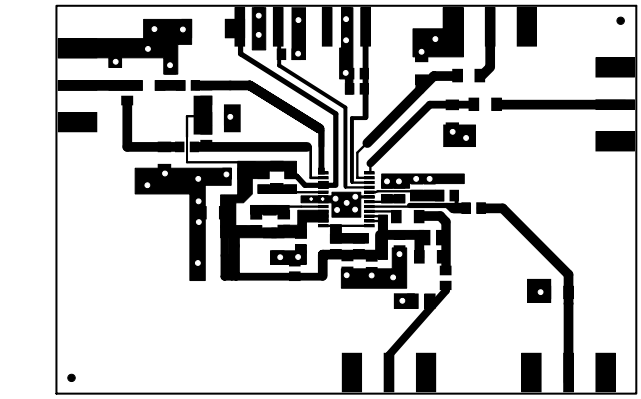
(Download Bill of Materials from www.rfmd.com.)

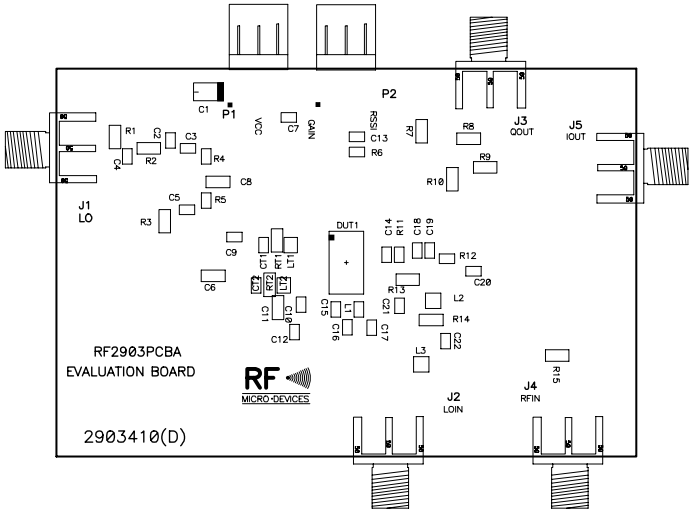


Evaluation Board Layout

Scale 1:1, Board size 2” x 3”

Board Thickness 0.031”; Board Material FR-4





RF2903

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11 Transceivers

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc-Rx (mA)	Icc-Tx (mA)	TX Power (dBm)	RX Sensitivity (dBm)	Package	Page
RF2510	VHF/UHF Transmitter	300 to 1000	2.4 to 5.0	n/a	13	-4	n/a	SSOP-16	11-1
RF2512	UHF Transmitter	300 to 1000	2.7 to 5.0	n/a	25	+10	n/a	SSOP-24	11-11
RF2513	UHF Transmitter	300 to 1000	2.7 to 5.0	n/a	25	+6	n/a	SSOP-24	11-23
RF2516	VHF/UHF Transmitter	100 to 960	2.0 to 3.6	n/a	10.5	+10	n/a	SSOP-16	11-35
RF2905	433/868/915MHz FM/FSK/ASK/OOK Transceiver	300 to 1000	2.7 to 5.0	9	25	+10	-101	LQFP-48	11-53
RF2907	433/868/915MHz AM/ASK/OOK Transceiver	300 to 1500	2.7 to 5.0	11.5	20	+7.0	-97	SSOP-28	11-75
RF2908	915MHz Spread Spectrum Receiver with PLL Frequency Synthesizer	700 to 1100	2.7 to 3.6	50	n/a	n/a	TBD	LQFP-48	11-85
RF2909	3V 915MHz Spread-Spectrum Transmitter IC	100 to 1100	2.7 to 5.0	n/a	30 to 175	17	n/a	SSOP-24	11-103
RF2915	433/868/915MHz FSK/ASK/OOK Transceiver	300 to 1000	2.4 to 5.0	5.6	22	+8.5	-99	LQFP-32	11-111
RF2917	433/868/915MHz FM/FSK Receiver	300 to 1000	2.7 to 5.0	9	n/a	n/a	-101	LQFP-32	11-129
RF2919	433/868/915MHz ASK/OOK Receiver	300 to 1000	2.7 to 5.0	10	n/a	n/a	-104	LQFP-32	11-143
RF2925	433/868/915MHz FM/FSK/ASK/OOK Transceiver	300 to 1000	2.7 to 5.0	9	25	+10	-101	LQFP-48	11-161
RF2926	UHF Dual Conversion Transceiver	300 to 1000	2.7 to 5.0	10	37	+8.5	-99	LQFP-48	11-185
RF2938	2.4GHz Spread Spectrum Transceiver	45 to 500 and 2.4 to 2.5GHz	2.7 to 3.6	65	105	+6	n/a	TQFP-48 EPP	11-193
RF2945	433/868/915MHz FSK/ASK/OOK Transceiver	300 to 1000	2.4 to 5.0	6.1	22	+8.5	-96	LQFP-32	11-215
RF9901	FSK Transmitter	400 to 930	3.0 to 5.0	n/a	30	+2	n/a	SOP-16	11-231
RF9902	FSK Receiver	400 to 930	3.0 to 5.0	25	n/a	n/a	-85	SOP-16	11-239

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RF MICRO·DEVICES

Preliminary

RF2510

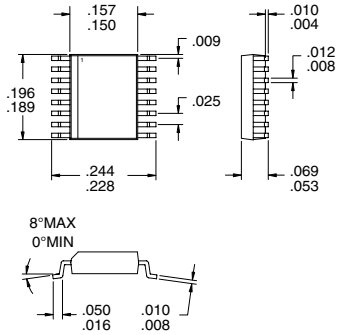
VHF/UHF TRANSMITTER

Typical Applications

- Local Oscillator Source
- FM/FSK Transmitter
- Wireless Data Transmitters
- 433/868/915MHz ISM Band Systems
- Low Cost Single Frequency LO Source
- Wireless Security Systems

Product Description

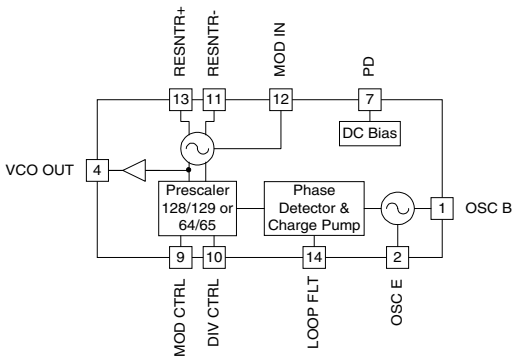
The RF2510 is a monolithic integrated circuit intended for use as a low-cost Frequency Synthesizer. The device is provided in a 16 pin SSOP package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in FM or FSK applications in the U.S. 915MHz ISM band and European 433MHz and 868MHz ISM band. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) pre-scaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator.



Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: SSOP-16



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- Integrated VCO and Reference Oscillator
- 2.4V to 5.0V Supply Voltage
- Low Current and Power Down Capability
- 300MHz to 1000MHz Frequency Range
- Narrowband and Wideband FM

11

TRANSCEIVERS

Ordering Information

RF2510	VHF/UHF Transmitter
RF2510 PCBA-L	Fully Assembled Evaluation Board 433MHz
RF2510 PCBA-M	Fully Assembled Evaluation Board 868MHz
RF2510 PCBA-H	Fully Assembled Evaluation Board 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
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Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

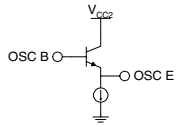
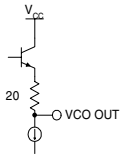
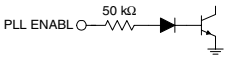
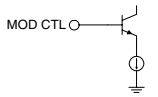
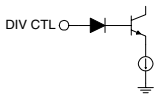
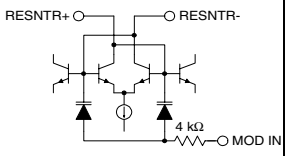
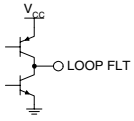
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

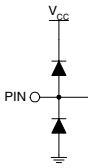
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		300 to 1000		MHz	
Modulation		FM/FSK			
Modulation Frequency			2	MHz	Modulation frequency and deviation dependent on VCO components L2, L3, C11, and D1.
Maximum FM Deviation	200			kHz	
Output Power		-2.5		dBm	50Ω load, no output attenuator
Output Load VSWR			2:1		To maintain PLL lock
Add 1 dB pad			3:1		
Add 2 dB pad			6:1		
Add 3 dB pad			20:1		
PLL and Prescaler					
Prescaler Divide Ratio		64/65 or 128/129			
VCO Gain, K_{VCO}					Dependent upon external components,
		70		MHz/V	Freq=915MHz, 868Mhz
		25		MHz/V	Freq=433MHz
PLL Phase Noise		-72		dBc/Hz	10kHz Offset, 5kHz loop bandwidth
		-98		dBc/Hz	100kHz Offset, 5kHz loop bandwidth
Harmonics		-15		dBc	Without filtering.
Reference Frequency			17	MHz	
Crystal Frequency Spurs		-62		dBc	5kHz PLL loop bandwidth
Max Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Power Down Control					
Power Down "ON"	2.0			V	Voltage supplied to the input; device is "ON"
Power Down "OFF"			1.0	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	25k			Ω	
Turn On Time		2	4	ms	Crystal start-up, 7.15MHz crystal. PLL lock time additional 4/(loop bandwidth) sec.
Power Supply					
Voltage		3.6		V	Specifications
	2.4		5	V	Operating limits over temp
	2.2			V	T<+40°C
Current Consumption	7	10.5	13.5	mA	
			1	µA	Sleep mode

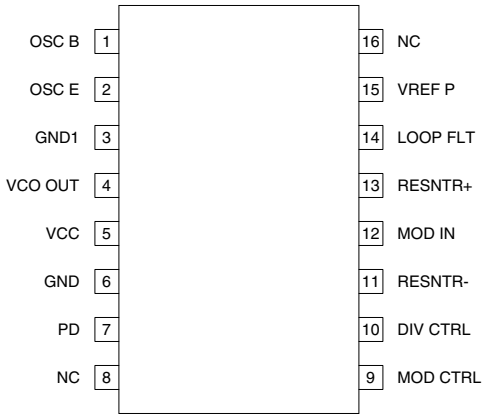
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Pin	Function	Description	Interface Schematic
1	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 1 and pin 2.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. An appropriate capacitor as chosen by the customer should be connected from this pin to ground.	See pin 1.
3	GND1	Ground connection for the VCO OUT buffer amp.	
4	VCO OUT	Buffered output of the VCO	
5	VCC	This pin is used to supply DC bias to the entire IC. ARF Bypass capacitor should be connected directly to ground.	
6	GND	Ground connection.	
7	PD	Power Down control for all circuitry. When this pin is a logic “low” all circuits are turned off.	
8	NC	Not internally connected.	
9	MOD CTRL	This pin is used to select the prescaler modulus. A logic “high” selects 64 or 128 for the prescaler divisor. A logic “low” selects 65 or 129 for the prescaler divisor.	
10	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic “high” selects the 64/65 divisor. A logic low selects the 128/129 divisor.	
11	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 13.	
12	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is recommended. Because the modulation varactors are part of the resonator tank, the deviation is slightly dependent upon the components used in the external tank.	See pin 11.
13	RESNTR+	See pin 11.	See pin 11.
14	LOOP FLT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth.	

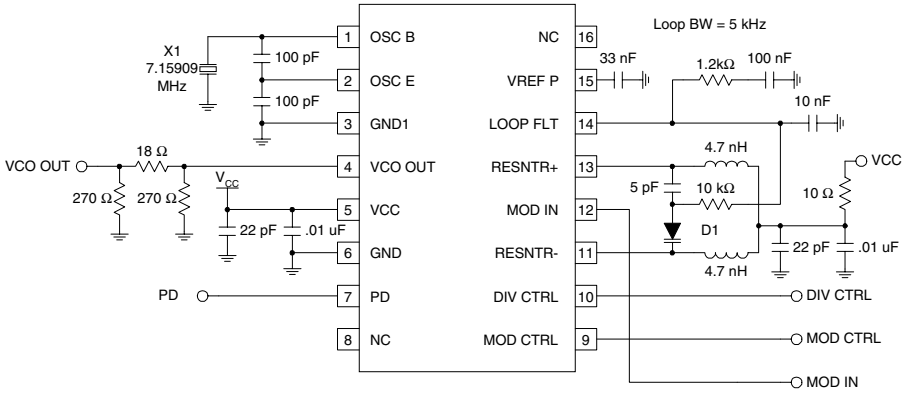
Pin	Function	Description	Interface Schematic
15	VREF P	Bias voltage reference pin for bypassing the prescaler and phase detector. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin.	
16	NC	Not internally connected.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the human body model. the following pins are protected: 1, 2, 3, 5, 6, 7, 9, 10, 14, and 15.	

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Pin Out



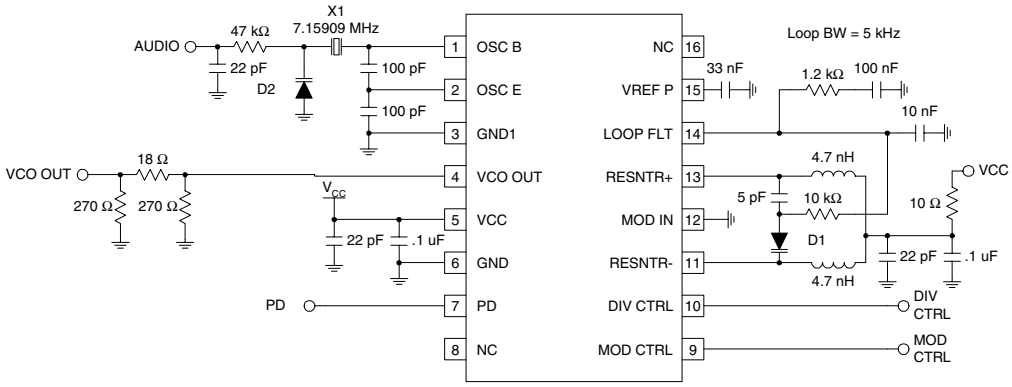
Application Schematic (915MHz)



D1 : SMV1233-011

Application Schematic (915MHz)

RF2510 Audio Transmitter



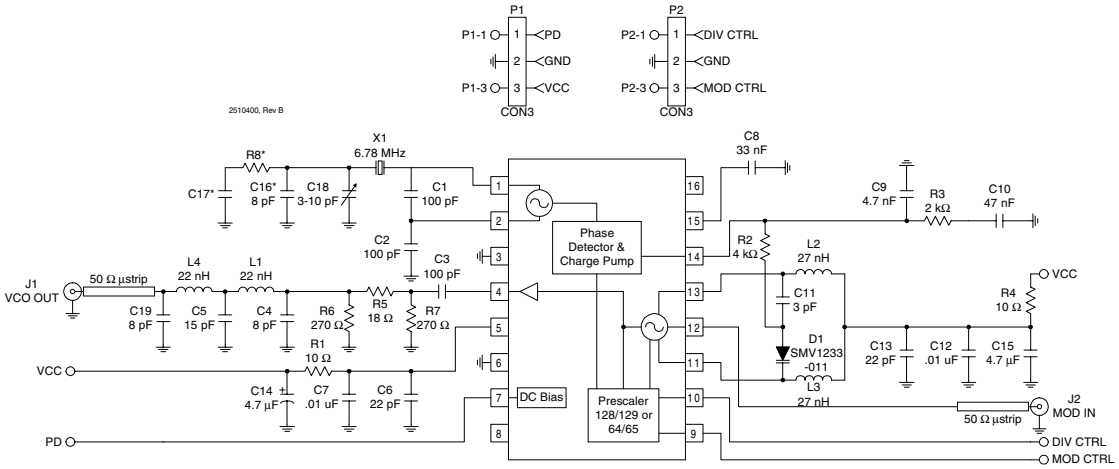
D1, D2 : SMV1233-011

11 TRANSCEIVERS

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Evaluation Board Schematic
433 MHz

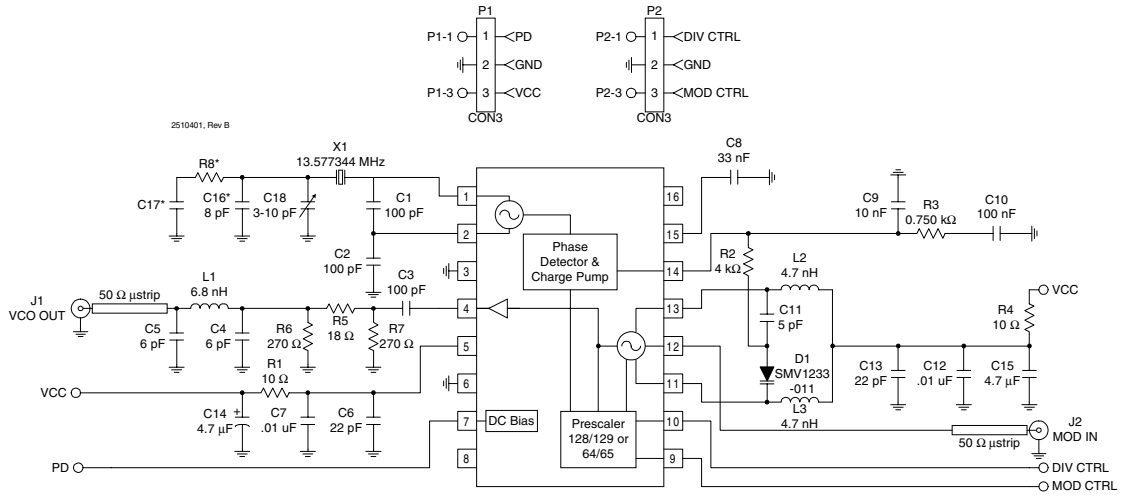
(Download Bill of Materials from www.rfmd.com.)



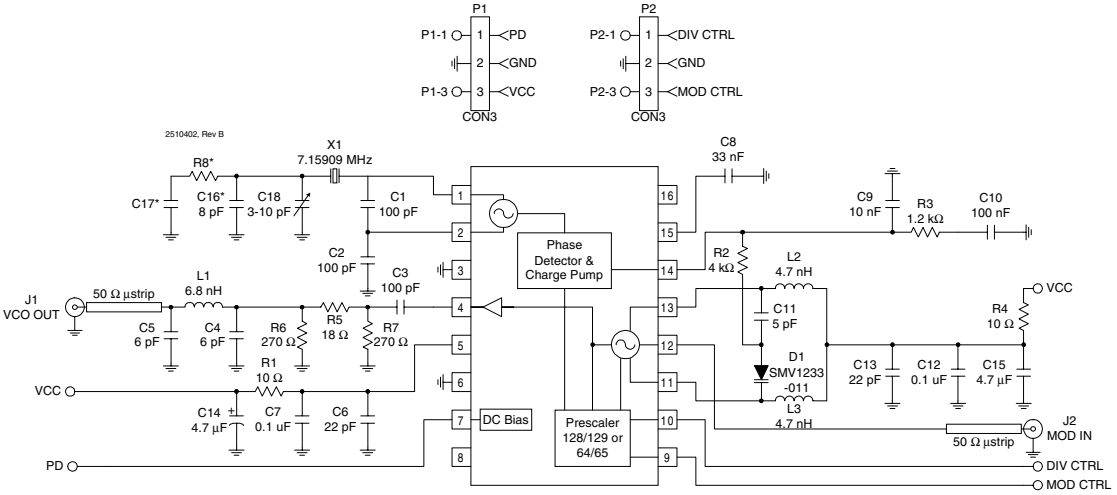
11 TRANSCEIVERS

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Evaluation Board Schematic
868 MHz



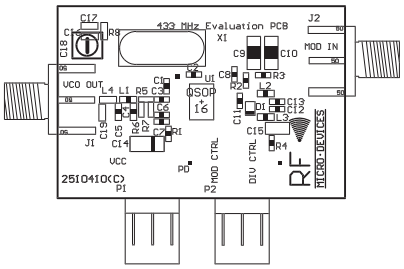
Evaluation Board Schematic
915 MHz

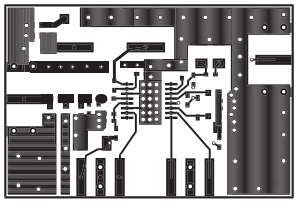


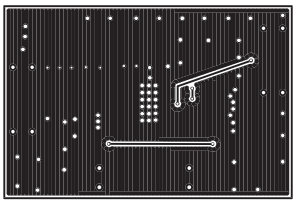
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Evaluation Board Layout 433MHz
Board Size 1.500” x 1.000”

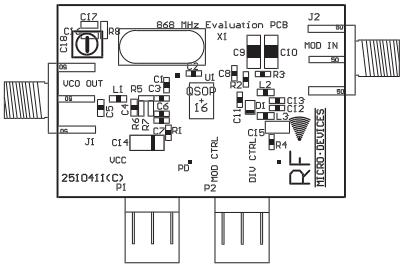
Board Thickness 0.031”, Board Material FR4

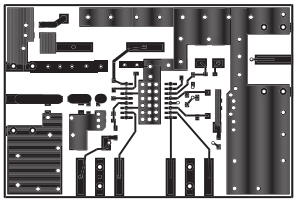


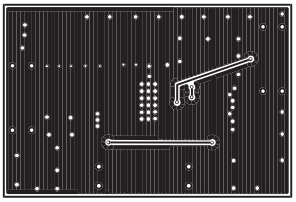




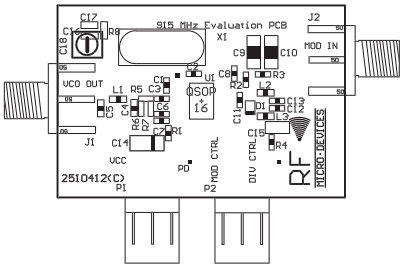
Evaluation Board Layout 868MHz
Board Size 1.500” x 1.000”

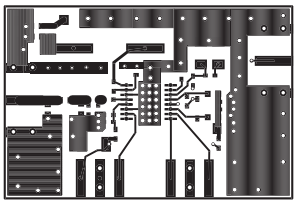


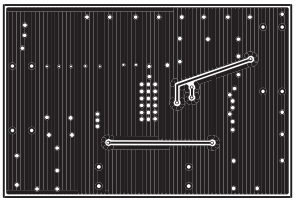




Evaluation Board Layout 915MHz
Board Size 1.500” x 1.000”

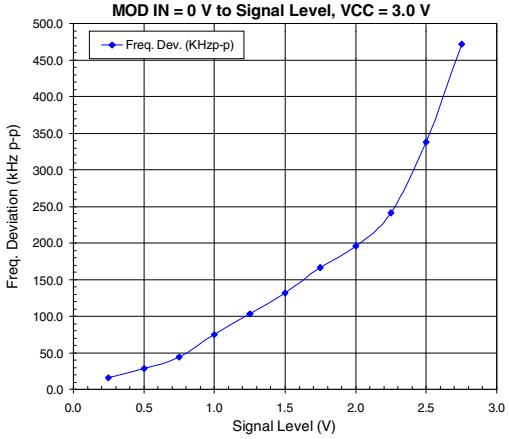




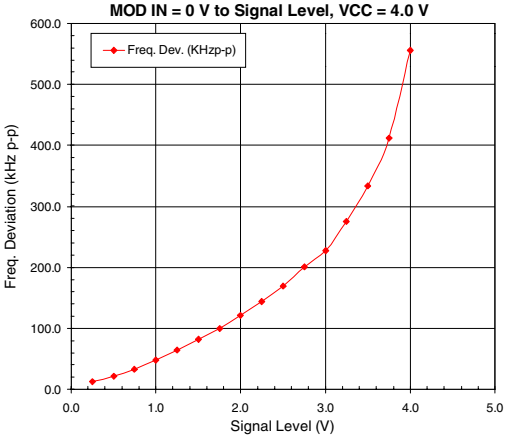


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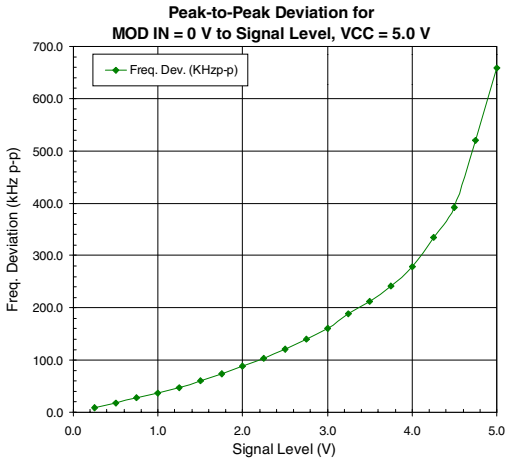
Peak-to-Peak Deviation for MOD IN = 0 V to Signal Level, VCC = 3.0 V



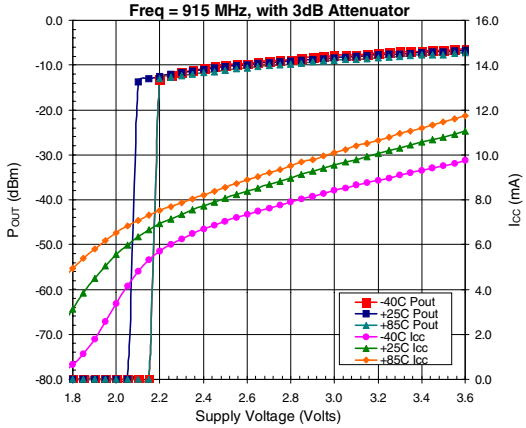
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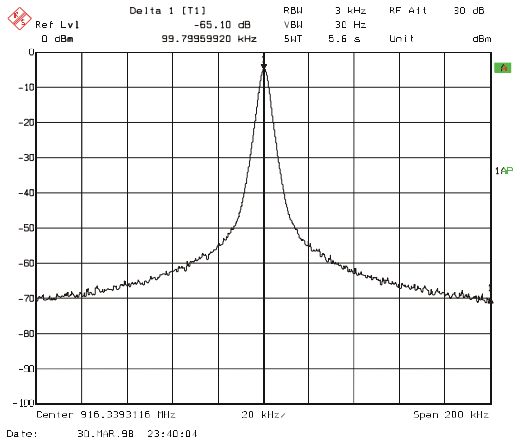


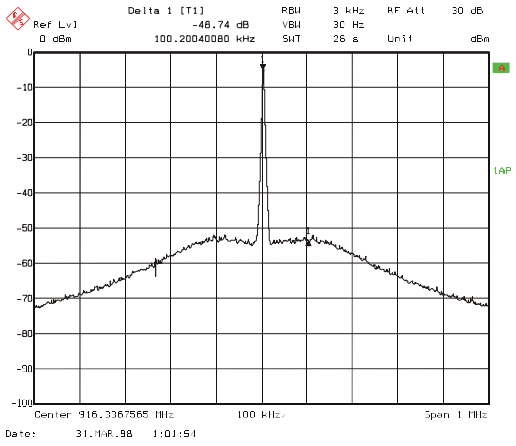
Peak-to-Peak Deviation for MOD IN = 0 V to Signal Level, VCC = 5.0 V



Output Power and I_{CC} versus Voltage, Freq = 915 MHz, with 3dB Attenuator







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RF MICRO·DEVICES

Preliminary

RF2512

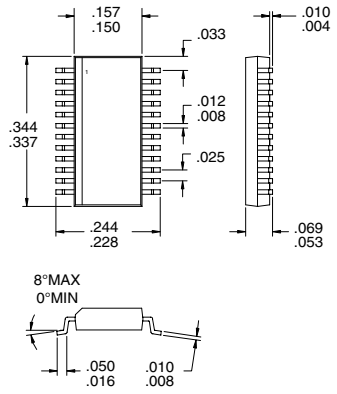
UHF TRANSMITTER

Typical Applications

- Single or Dual Channel LO Source
- FM/FSK Transmitter
- Wireless Data Transmitters
- 433/868/915MHz ISM Band Systems
- Wireless Security Systems

Product Description

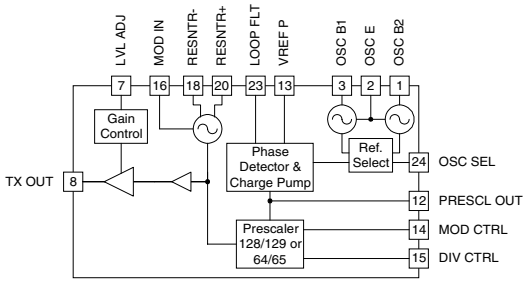
The RF2512 is a monolithic integrated circuit intended for use as a low-cost Frequency Synthesizer and Transmitter. The device is provided in a 24 pin SSOP package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in FM or FSK applications in the U.S. 915MHz ISM band and European 433MHz or 868MHz ISM band. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator. A second reference oscillator is available to support two channel applications.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- 15mW Output Power at 433MHz
- 2.7V to 5.0V Supply Voltage
- Low Current and Power Down Capability
- 300MHz to 1000MHz Frequency Range
- Narrowband and Wideband FM

11

TRANSCEIVERS

Ordering Information

RF2512	UHF Transmitter
RF2512 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2512 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2512 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

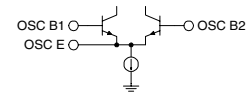
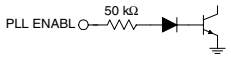
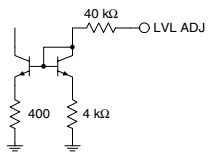
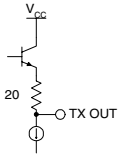
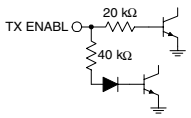
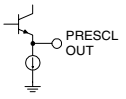
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

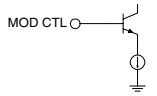
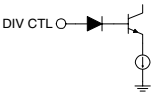
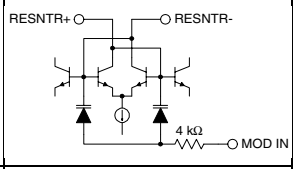
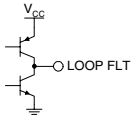
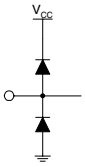
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		300 to 1000		MHz	
Modulation		FM/FSK			
Modulation Frequency			2	MHz	
Maximum FM Deviation	200			kHz	Dependent upon Supply Voltage
PLL and Prescaler					
Prescaler Divide Ratio		64/65 or 128/129			
PLL Lock TIme		4/PLL BW		ms	The PLL lock time, from power up, is set externally by the bandwidth of the loop filter.
PLL Phase Noise		-80		dBc/Hz	10kHz Offset, 10kHz loop bandwidth
		-100		dBc/Hz	100kHz Offset, 10kHz loop bandwidth
Reference Frequency			17	MHz	
Max Crystal R_S	TBD		100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Maximum Power Level	+7	+12		dBm	Freq=433MHz
		+6		dBm	Freq=915MHz
Power Control Range	15			dB	
Power Control Sensitivity		10		dB/V	
Antenna Port Impedance		50		Ω	TX ENABL="1"
Antenna Port Impedance		TBD		Ω	TX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Power Down Control					
Logic Controls "ON"	2.0			V	Voltage supplied to the input; device is "ON"
Logic Controls "OFF"			1.0	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	25			kΩ	
Turn On Time			5+4/PLL BW	ms	From Change in OSC SEL,7.075MHz XTAL
Turn Off Time			TBD	ms	From Change in OSC SEL,7.075MHz XTAL
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		28		mA	TX Mode, LVL ADJ=3.6V
		10		mA	TX Mode, LVL ADJ=0V
		8		mA	PLL Only

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Pin	Function	Description	Interface Schematic
1	OSC B2	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 1 and pin 2.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. An appropriate capacitor as chosen by the customer should be connected from this pin to ground.	See pin 1.
3	OSC B1	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 3 and pin 2.	See pin 1.
4	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
5	GND1	Ground connection for the PA buffer amp. Keep traces physically short and connect immediately to ground plane for best performance.	
6	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
7	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
8	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
9	GND2	Ground connection for the Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
10	VCC1	This pin is used to supply DC bias to the PA buffer amp. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
11	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
12	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
13	VREF P	Bias voltage reference pin for bypassing the prescaler and phase detector. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin.	

Pin	Function	Description	Interface Schematic
14	MOD CTRL	This pin is used to select the prescaler modulus. A logic “high” selects 64 or 128 for the prescaler divisor. A logic “low” selects 65 or 129 for the prescaler divisor.	
15	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic “high” selects the 64/65 divisor. A logic low selects the 128/129 divisor.	
16	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. Because the modulation varactors are part of the resonator tank, the deviation is slightly dependent upon the components used in the external tank.	See pin 18.
17	VCC2	This pin is used to is supply DC bias to the VCO, prescaler, and PLL.	
18	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 20.	
19	NC	Not internally connected.	
20	RESNTR+	See pin 18.	See pin 18.
21	GND3	GND is the ground shared on chip by the VCO, prescaler, and PLL electronics. Keep traces physically short and connect immediately to ground plane for best performance.	
22	NC	Not internally connected.	
23	LOOP FLT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth.	
24	OSC SEL	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1-3, 9, 10, 12-15, 17, 21, 23.	

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RF2512 Theory of Operation

Introduction

The RF2512 is a low cost FM/FSK UHF transmitter designed for applications operating within the frequency range of 300MHz to 1000MHz. In particular, it is intended for 315/433/868MHz band systems, remote keyless entry systems, and FCC Part 15.231 periodic transmitters. It can also be used as a single or dual channel local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop.

The RF2512 is provided in a 24-pin SSOP-24 package and is designed to operate from a supply voltage ranging from 2.2V to 5.0V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to 15mW output power into a 50Ω load (+11.8dBm) and is intended to comply with FCC requirements for unlicensed remote control transmitters.

RF2512 Functional Blocks

A PLL consists of a reference oscillator, a phase detector, a loop filter, a voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2512 includes all of these internally except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillators** are Colpitts type oscillators. Pin 1 (OSC B2), pin 2 (OSC E), and pin 3 (OSC B1) provide connections to the internal transistors that are used as the reference oscillators. The Colpitts configuration is a low parts count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of either transistor. The drive level should, in either case, be around 500mV$_{PP}$ This level prevents overdriving the device and keeps the phase noise and reference spurs to a minimum.

The user sets which oscillator is operational by setting pin 24 (OSC SEL) either high or low. This allows the implementation of two channel systems.

The **prescaler** divides the Voltage Controlled Oscillator (VCO) frequency down by either 64/65 or 128/129, using a series of flip-flops, depending upon the logic level present at pin 15 (DIV CTRL). A high logic level will select the 64/65 divisor. A low logic level will select the 128/129 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

In addition to the DIV CTRL setting, one also sets the prescaler modulus by setting pin 14 (MOD CTRL) either high or low. A high logic level will select the 64/128 divisor. A low logic level will select the 65/129 divisor.

Pin 12 (PRESCL OUT) provides access to the prescaler output. This is used for interfacing to an external PLL IC.

The RF2512 contains an onboard phase detector and charge pump. The **phase detector** compares the phase of the reference oscillator to the phase of the VCO. The phase detector is implemented using flip-flops in a topology referred to as either "digital phase/frequency detector" or "digital tri-state comparator". The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency.

When both inputs of the flip-flops are identical, the signals are both frequency and phase locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter or enter into a high impedance state. This is where the name "tri-state comparator" comes from.

The main benefit of this type of detector it's ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it will use the frequency error for correction. This type of detector will lock under all conditions.

The prescaler and the phase detector bias voltage is brought out through pin 13 (VREF P). This allows bypassing of the of these two circuits to filter the reference crystal frequency.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. It's inputs are the outputs of the phase detector flip-flops. Since there are two flip-flops, there are four possible states. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. The

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state where both inputs are high will not occur. The other states are either charging or discharging the loop filter. The loop filter integrates the pulses coming from the charge pump to create a control voltage for the voltage controlled oscillator.

The **voltage controlled oscillator** (VCO) is a tuned differential amplifier with the bases and collectors cross coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors. It is comprised an external varactor, a capacitor and external inductors. The designer selects the inductors for the desired frequency of operation. These inductors also provide DC bias for the VCO. The output of the VCO is buffered and applied to the prescaler circuit, where it is divided down and compared to the reference oscillator frequency.

The PLL and VCO circuitry can be enabled by setting applying a "high" logic level to pin 4 (PLL ENABL). Conversely, the PLL and VCO circuitry will be turned off if the level is tied "low".

The **transmit amplifier** is a two stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 12dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The output power is adjustable by the setting of pin 7 (LVL ADJ). This analog input allows the designer a 12dB range of output power. As the LVL ADJ voltage is reduced, the output power and current consumption are reduced. LVL ADJ must be low when the transmitter is disabled.

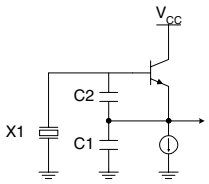
Additionally, the transmitter circuitry can be disabled entirely by applying a "low" logic level to pin 11 (TX ENABL). During transmission, this pin should be tied "high". This pin controls all circuitry except for the PLL circuitry.

During transmission the transmitter is enabled and the impedance of the output pin, pin 8 (TX OUT), is low. When the transmitter is not enabled, the impedance becomes high.

The RF2512 contains onboard band gap reference voltage circuitry which provides a stable **DC bias** over varying temperature and supply voltages.

Designing with the RF2512

The **reference oscillator** is built around the onboard transistor at pins 1, 2 and 3. The intended topology is of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low cost solutions. The topology of this type of oscillator is as seen in the following figure.



This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C1 and C2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations.

$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

The load capacitance is usually 32pF. The variable *freq* is the oscillator frequency in MHz. The frequency can be adjusted by either changing C_2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

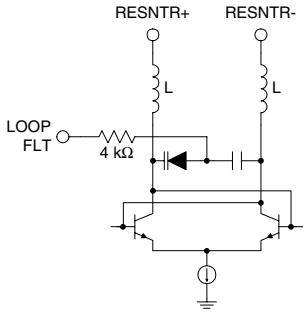
These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at pin 2 (OSC E). It has been found that the level at this pin should generally be around 500mV$_{PP}$ or less. This will reduce the reference spur levels and reduce noise from distortion. If this level is higher than 500mV$_{PP}$ then decrease the value of C_1. The values of these capacitors are usually tweaked during design to meet performance goals, such as minimizing the start-up time.

Additionally, by placing a variable capacitor in series with the crystal, one is able to adjust the frequency. This will also alter the drive level, so it should be checked again.

An important part of the overall design is the **voltage controlled oscillator**. The VCO is configured as a differential amplifier. The VCO is tuned via the external inductors, capacitor, and varactor. The varactor capaci-

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tance is set by the loop filter output voltage through a 4kΩ resistor.



To tune the VCO the designer only needs to calculate the value of the inductors connected to pins 18 and 20 (RESNTR- and RESNTR+). The inductor value is determined by the following equation.

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C} \cdot \frac{1}{2}$$

In this equation, *f* is the desired operating frequency and *L* is the value of the inductor required. The value *C* is the amount of capacitance presented by the varactor, capacitor and parasitics. The factor of one-half is due to the inductors being in each leg.

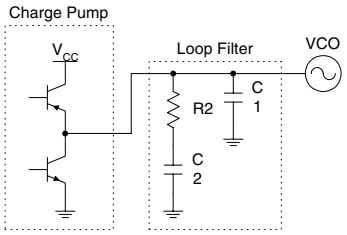
The setup of the VCO can be summarized as follows. First, open the loop. Next, get the VCO to run on the desired frequency by selecting the proper inductor and capacitor values. The capacitor value will need to include the varactor and circuit parasitics. After the VCO is running at the desired frequency, then set the VCO sensitivity.

The sensitivity is determined by connecting the control voltage input point to ground and noting the frequency. Then connect the same point to the supply and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sensitivity expressed in Hz/V. Increasing the inductor value while decreasing the capacitor value will increase the sensitivity. Decreasing the inductor value while increasing the capacitor value will lower the sensitivity.

When increasing or decreasing component values, make sure that the center frequency remains constant. Finally, close the loop.

External to the part, the designer needs to implement a **loop filter** to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through a 4kΩ resistor. The loop filter is then connected in parallel to this point at pin 23 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC. A passive filter is most common, as it is a low cost and low noise design. An additional pole could be used for reducing the reference spurs, however there is not a way to add the series resistor. This should not be a reason for concern however.

The schematic of the loop filter is



The transfer function is

$$F(s) = R_2 \cdot \left[\frac{s \cdot \tau_2 + 1}{s \cdot \tau_2 \cdot (s \cdot \tau_1 + 1)}\right]$$

where the time constants are defined as

$$\tau_2 = R_2 \cdot C_2 \quad \text{and} \quad \tau_1 = R_2 \cdot \left[\frac{C_1 \cdot C_2}{C_1 + C_2}\right]$$

The frequency at which unity gain occurs is given by

$$\omega_{LBW} = \frac{1}{\sqrt{\tau_1 \cdot \tau_2}}$$

This is also the loop bandwidth.

If the phase margin (PM) and the loop bandwidth (ω_{LBW}) are known, it is possible to calculate the time constants. These are found using the equations

$$\tau_1 = \frac{\sec(PM) - \tan(PM)}{\omega_{LBW}} \quad \text{and} \quad \tau_2 = \frac{1}{\omega^2_{LBW} \cdot \tau_1}$$

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With these known, it is then possible to determine the values of the filter components.

$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_{PD} \cdot K_{VCO}}{\omega^2_{LBW} \cdot N} \cdot \sqrt{\frac{1 + (\omega_{LBW} \cdot \tau_2)^2}{1 + (\omega_{LBW} \cdot \tau_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1\right)$$

$$R_2 = \frac{\tau_2}{C_2}$$

As an example, consider a loop bandwidth of 50kHz, a phase margin of 45°, a divide ratio of 64, a K_{VCO} of 20MHz/V, and a K_{PD} of 0.01592mA/2πrad. Time constant τ_1 is 1.31848µs, time constant τ_2 is 7.68468µs, C_1 is 131.15pF, C_2 is 633.26pF, and R_2 is 12.14kΩ.

In order to perform these calculations, one will need to know the value of two constants, K_{VCO} and K_{PD}. K_{PD} is calculated by dividing the charge pump current by 2π. For the RF2512, the charge pump current is 40µA. K_{VCO} is best found empirically as it will change with frequency and board parasitics. By briefly connecting pin 23 (LOOP FLT) to VCC and then to ground, the frequency tuning range of the VCO can be seen. Dividing the difference between these two frequencies by the difference in the voltage gives K_{VCO} in MHz/V.

The control lines provide an **interface** for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 16 (MOD IN), pin 15 (DIV CTRL), pin 14 (MOD CTRL) and pin 7 (LVL ADJ) as control pins whose voltage level can be set.

General **RF bypassing** techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias for connection to the ground plane allows one to connect to ground as close as possible to ground pins. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

Pre-compliance testing should be performed during the design process. This can be done with a GTEM cell or at a compliance testing laboratory. It is recommended that pre-compliance testing be performed so that there are no surprises during final compliance testing. This will help keep the product development and release on schedule.

Working with a laboratory offers the benefit of years of compliance testing experience and familiarity with the regulatory issues. Also, the laboratory can often provide feedback that will help the designer make the product compliant.

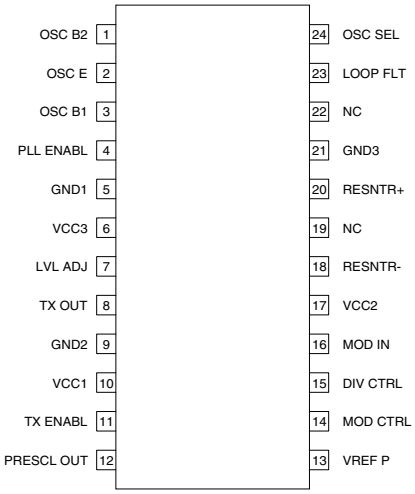
On the other hand, having a GTEM cell or an open air test site locally offers the designer the ability to rapidly determine whether or not design changes impact the product's compliance. Set-up of an open air test site and the associated calibration is not trivial. An alternative is to use a GTEM test cell.

After the design has been completed and passes compliance testing, application will need to be made with the respective regulatory bodies for the geographic region in which the product will be operated to obtain final certifications.

Conclusions

The RF2512 is an AM/OOK UHF transmitter that features a phase-locked output. This device is suitable for use in a CFR Part 15.231 compliant product as well as a local oscillator signal source. Further, the RF2512 is packaged in a low cost SSOP-24 plastic package and requires few external parts, thus making it suitable for low cost designs.

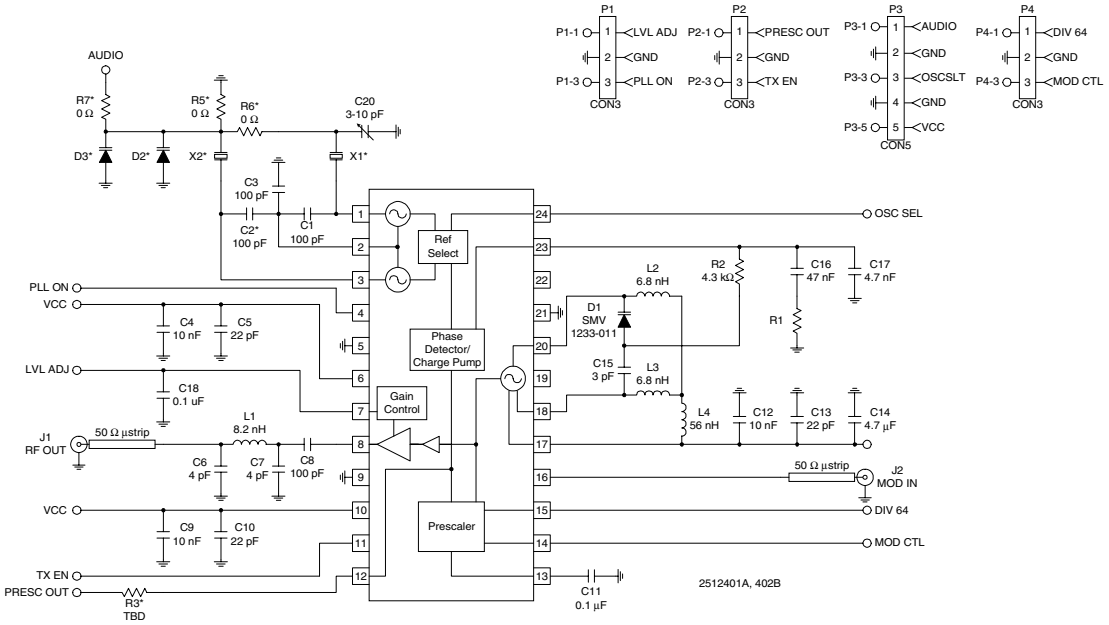
Pin Out


OSC B2 1
OSC E 2
OSC B1 3
PLL ENABL 4
GND1 5
VCC3 6
LVL ADJ 7
TX OUT 8
GND2 9
VCC1 10
TX ENABL 11
PRESCL OUT 12
24 OSC SEL
23 LOOP FLT
22 NC
21 GND3
20 RESNTR+
19 NC
18 RESNTR-
17 VCC2
16 MOD IN
15 DIV CTRL
14 MOD CTRL
13 VREF P

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Evaluation Board Schematic
H (915MHz) and M (868MHz) Boards

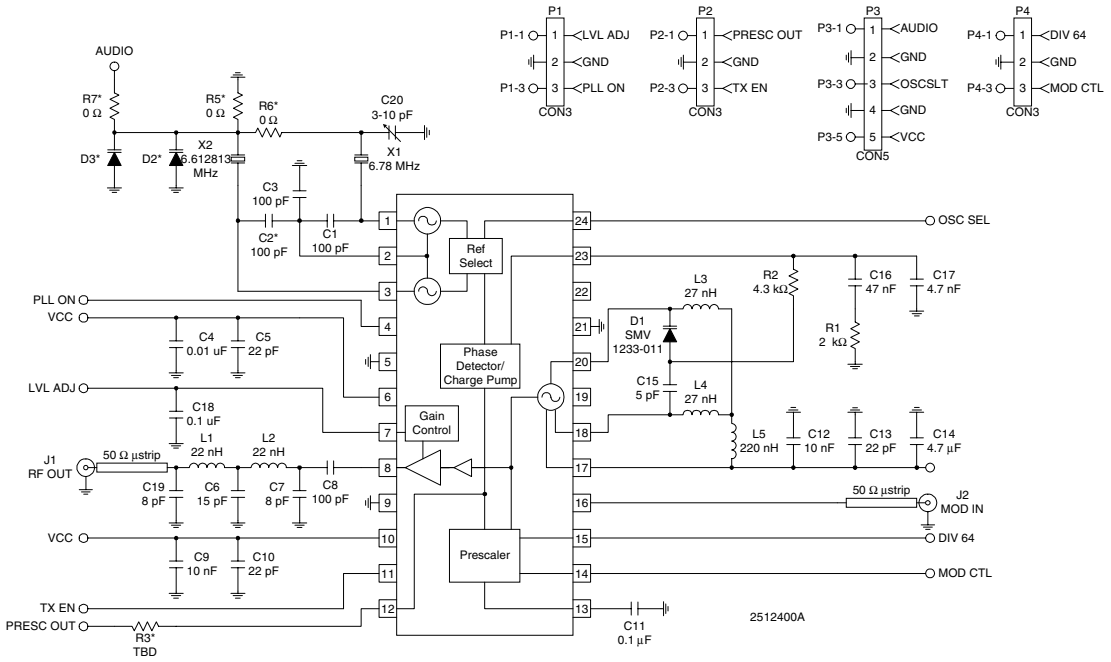
(Download Bill of Materials from www.rfmd.com.)



Board	X1 (MHz)	X2 (MHz)	R1 (kΩ)	L2 (nH)	L3 (nH)
M (868MHz)	13.57734	13.41015	1.2	6.8	6.8
H (915MHz)	7.15909	7.07549	2.2	4.7	4.7

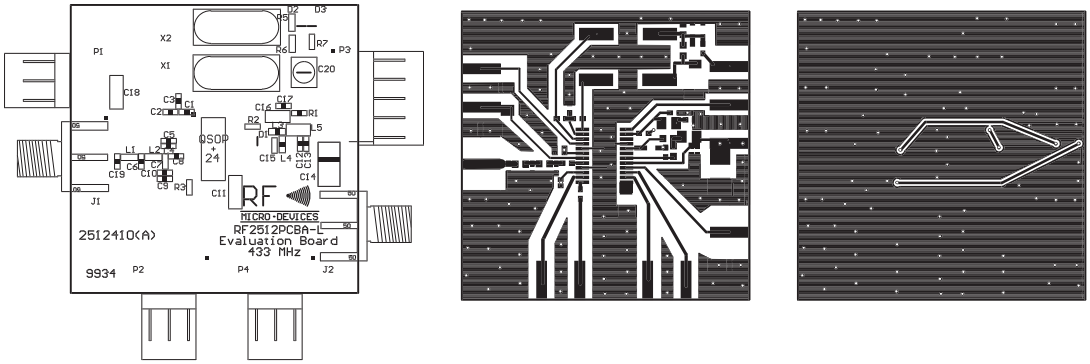
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Evaluation Board Schematic
L (433MHz) Board

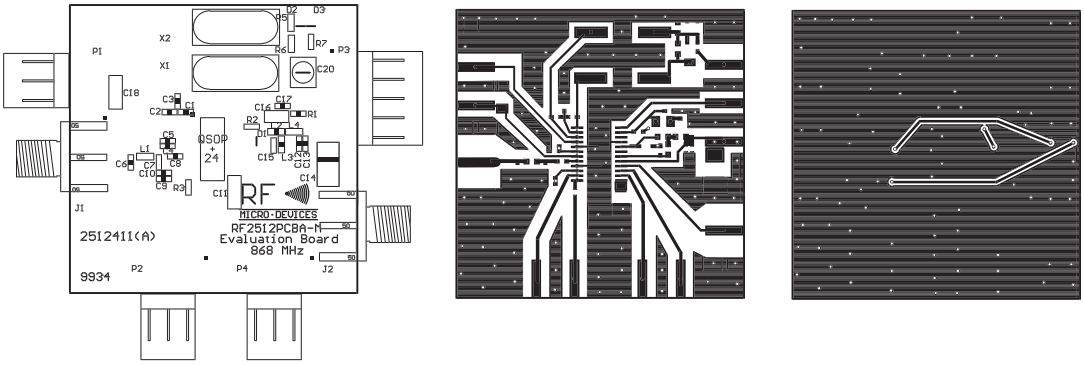


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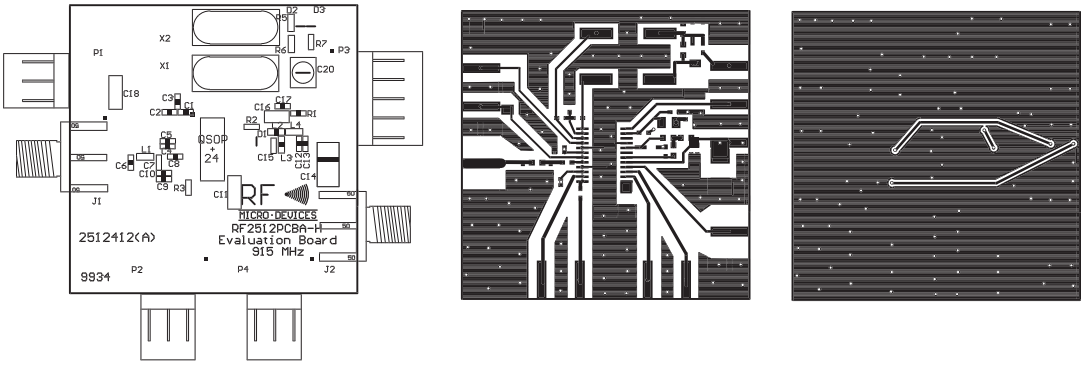
Evaluation Board Layout 433MHz
Board Size 1.5” x 1.5”



Evaluation Board Layout 868MHz
Board Size 1.5” x 1.5”



Evaluation Board Layout 915MHz
Board Size 1.5” x 1.5”



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RF MICRO·DEVICES

Preliminary

RF2513

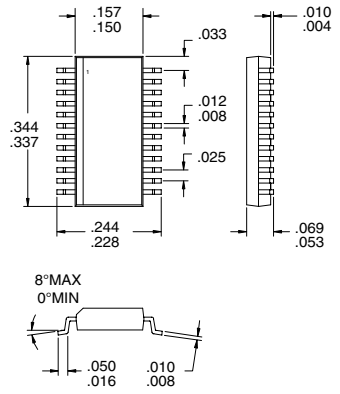
UHF TRANSMITTER

Typical Applications

- Single or Dual Channel LO Source
- FM/FSK Transmitter
- Wireless Data Transmitters
- 433/868/915MHz ISM Band Systems
- Wireless Security Systems

Product Description

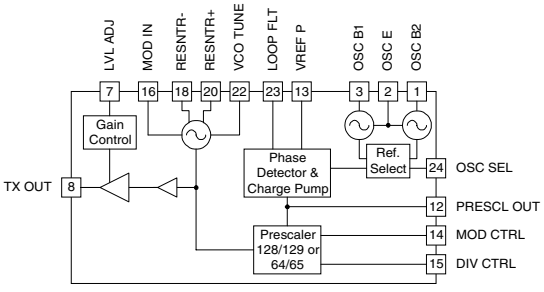
The RF2513 is a monolithic integrated circuit intended for use as a low-cost Frequency Synthesizer and Transmitter. The device is provided in a 24 pin SSOP package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in FM or FSK applications in the U.S. 915MHz ISM band and European 433MHz or 868MHz ISM band. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator. A second reference oscillator is available to support two channel applications.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- 10mW Output Power at 433MHz
- 2.7V to 5.0V Supply Voltage
- Low Current and Power Down Capability
- 300MHz to 1000MHz Frequency Range
- Narrowband and Wideband FM

11

TRANSCEIVERS

Ordering Information

RF2513	UHF Transmitter
RF2513 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2513 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2513 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

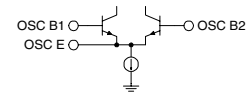
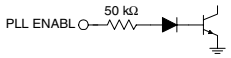
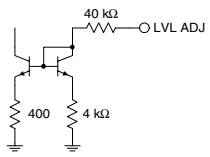
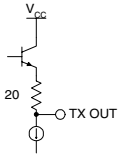
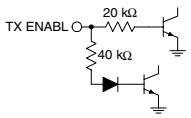
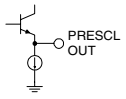
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

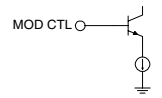
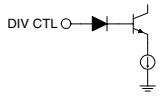
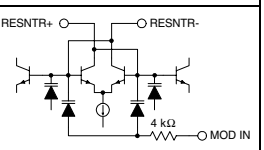
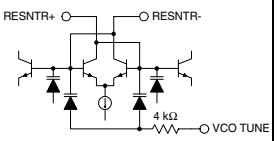
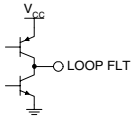
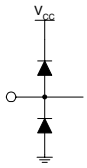
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		300 to 1000		MHz	
Modulation		FM/FSK			
Modulation Frequency			2	MHz	
Maximum FM Deviation	200			kHz	Dependent upon Supply Voltage
PLL and Prescaler					
Prescaler Divide Ratio		64/65 or 128/129			
PLL Lock TIme		4/PLL BW		ms	The PLL lock time, from power up, is set externally by the bandwidth of the loop filter.
PLL Phase Noise		-72		dBc/Hz	10kHz Offset, 10kHz loop bandwidth
		-95		dBc/Hz	100kHz Offset, 10kHz loop bandwidth
Reference Frequency			17	MHz	
Max Crystal R_S	TBD		100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Maximum Power Level	+3	+8		dBm	Freq=433MHz
		+2		dBm	Freq=915MHz
Power Control Range	15			dB	
Power Control Sensitivity		10		dB/V	
Antenna Port Impedance		50		Ω	TX ENABL="1"
Antenna Port Impedance		TBD		Ω	TX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Power Down Control					
Logic Controls "ON"	2.0			V	Voltage supplied to the input; device is "ON"
Logic Controls "OFF"			1.0	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	25			kΩ	
Turn On Time			5 + 4/PLL BW	ms	From Change in OSC SEL,7.075MHz XTAL
Turn Off Time			4	ms	From Change in OSC SEL,7.075MHz XTAL
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		27		mA	TX Mode, LVL ADJ=3.6V
		10		mA	TX Mode, LVL ADJ=0V
		8		mA	PLL Only

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Pin	Function	Description	Interface Schematic
1	OSC B2	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 1 and pin 2.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. An appropriate capacitor as chosen by the customer should be connected from this pin to ground.	See pin 1.
3	OSC B1	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 3 and pin 2.	See pin 1.
4	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
5	GND1	Ground connection for the PA buffer amp. Keep traces physically short and connect immediately to ground plane for best performance.	
6	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
7	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
8	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
9	GND2	Ground connection for the Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
10	VCC1	This pin is used to supply DC bias to the PA buffer amp. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
11	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
12	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
13	VREF P	Bias voltage reference pin for bypassing the prescaler and phase detector. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin.	

Pin	Function	Description	Interface Schematic
14	MOD CTRL	This pin is used to select the prescaler modulus. A logic “high” selects 64 or 128 for the prescaler divisor. A logic “low” selects 65 or 129 for the prescaler divisor.	
15	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic “high” selects the 64/65 divisor. A logic low selects the 128/129 divisor.	
16	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. Because the modulation varactors are part of the resonator tank, the deviation is slightly dependent upon the components used in the external tank.	See pin 18.
17	VCC2	This pin is used to is supply DC bias to the VCO, prescaler, and PLL.	
18	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 20.	
19	NC	Not internally connected.	
20	RESNTR+	See pin 18.	See pin 18.
21	GND3	GND is the ground shared on chip by the VCO, prescaler, and PLL electronics. Keep traces physically short and connect immediately to ground plane for best performance.	
22	VCO TUNE	Loop filter input to VCO.	
23	LOOP FLT OUT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth.	
24	OSC SEL	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1-3, 9, 10,12-15, 17, 21-23.	

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RF2513 Theory of Operation

Introduction

The RF2513 is a low-cost FM/FSK UHF transmitter designed for applications operating within the 300MHz to 1000MHz frequency range. It is particularly intended for 315/433/868MHz band systems, remote keyless entry systems, and FCC Part 15.231 periodic transmitters. It can also be used as a single or dual-channel local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop.

The RF2513 is provided in a 24-pin SSOP-24 package and is designed to operate from a supply voltage ranging from 2.2V to 5.0V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to 10mW output power into a 50Ω load (+10dBm) and is intended to comply with FCC requirements for unlicensed remote control transmitters.

RF2513 Functional Blocks

A PLL consists of a reference oscillator, phase detector, loop filter, voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2513 includes all of these internally, except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillators** are Colpitts type oscillators. Pins 1 (OSC B2), 2 (OSC E), and 3 (OSC B1) provide connections to the internal transistors used as reference oscillators. The Colpitts configuration is a low parts-count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of either transistor. In either case, the drive level should be around $500mV_{PP}$ This level prevents overdriving the device and keeps phase noise and reference spurs minimal.

The user sets which oscillator is operational by setting pin 24 (OSC SEL) either high or low. This allows the implementation of two channel systems.

The **prescaler** divides the Voltage Controlled Oscillator (VCO) frequency down by either 64/65 or 128/129, using a series of flip-flops, depending upon the logic level present at pin 15 (DIV CTRL). A high logic level will select the 64/65 divisor. A low logic level will select the 128/129 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

In addition to the DIV CTRL setting, one also sets the prescaler modulus by setting pin 14 (MOD CTRL) either high or low. A high logic level will select the 64/128 divisor. A low logic level will select the 65/129 divisor.

Pin 12 (PRESCL OUT) provides access to the prescaler output. This is used for interfacing to an external PLL IC.

The RF2513 contains an onboard phase detector and charge pump. The **phase detector** compares the phase of the reference oscillator to the phase of the VCO. The phase detector is implemented using flip-flops in a topology referred to as either "digital phase/frequency detector" or "digital tri-state comparator". The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency.

When both inputs of the flip-flops are identical, the signals are both frequency and phase locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter or enter into a high impedance state. This is where the name "tri-state comparator" comes from.

The main benefit of this type of detector it's ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it will use the frequency error for correction. This type of detector will lock under all conditions.

The prescaler and the phase detector bias voltage is brought out through pin 13 (VREF P). This allows bypassing of the of these two circuits to filter the reference crystal frequency.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. It's inputs are the outputs of the phase detector flip-flops. Since there are two flip-flops, there are four possible states. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. The state where both inputs are high will not occur. The other states are either charging or discharging the loop filter. The loop filter integrates the pulses coming from

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the charge pump to create a control voltage for the voltage controlled oscillator.

The **voltage controlled oscillator (VCO)** is a tuned differential amplifier with the bases and collectors cross-coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors. It is comprised of internal varactors and two external inductors. The designer selects the inductors for the desired frequency of operation. These inductors also provide DC bias for the VCO. The output of the VCO is buffered and applied to the prescaler circuit, where it is divided down and compared to the reference oscillator frequency.

The PLL and VCO circuitry can be enabled by setting applying a “high” logic level to pin 4 (PLL ENABL). Conversely, the PLL and VCO circuitry will be turned off if the level is tied “low”.

The **transmit amplifier** is a two stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 8dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The output power is adjustable by the setting of pin 7 (LVL ADJ). This analog input allows the designer a 15dB range of output power. As the LVL ADJ voltage is reduced, the output power and current consumption are reduced. LVL ADJ must be low when the transmitter is disabled.

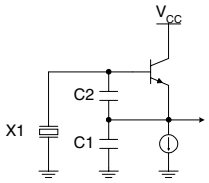
Additionally, the transmitter circuitry can be disabled entirely by applying a “low” logic level to pin 11 (TX ENABL). During transmission, this pin should be tied “high”. This pin controls all circuitry except for the PLL circuitry.

During transmission the transmitter is enabled and the impedance of the output pin, pin 8 (TX OUT), is low. When the transmitter is not enabled, the impedance becomes high.

The RF2513 contains onboard band gap reference voltage circuitry which provides a stable **DC bias** over varying temperature and supply voltages.

Designing with the RF2513

The **reference oscillator** is built around the onboard transistor at pins 1, 2 and 3. The intended topology is of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low cost solutions. The topology of this type of oscillator is as seen in the following figure.



This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C_1 and C_2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations.

$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

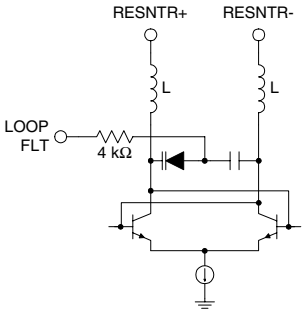
The load capacitance is usually 32pF. The variable *freq* is the oscillator frequency in MHz. The frequency can be adjusted by either changing C_2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at pin 2 (OSC E). It has been found that the level at this pin should generally be around 500mV$_{PP}$ or less. This will reduce the reference spur levels and reduce noise from distortion. If this level is higher than 500mV$_{PP}$ then decrease the value of C_1. The values of these capacitors are usually tweaked during design to meet performance goals, such as minimizing the start-up time.

Additionally, by placing a variable capacitor in series with the crystal, one is able to adjust the frequency. This will also alter the drive level, so it should be checked again.

An important part of the overall design is the voltage controlled oscillator (VCO). The VCO is configured as a differential amplifier. The VCO is tuned via the external inductors, capacitor and varactor. The varactor capacitance is set by the loop filter output voltage through a 4kΩ resistor.

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To tune the VCO the designer only needs to calculate the value of the inductors connected to pins 18 and 20 (RESNTR- and RESNTR+). The inductor value is determined by the following equation.

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C} \cdot \frac{1}{2}$$

In this equation, *f* is the desired operating frequency and *L* is the value of the inductor required. The value *C* is the amount of capacitance presented by the varactor, capacitor and parasitics. The factor of one half is due to the inductors being in each leg.

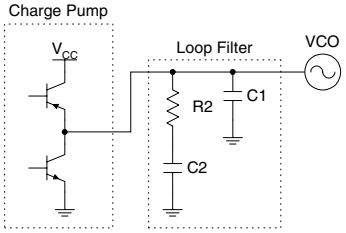
The setup of the VCO can be summarized as follows. First, open the loop. Next, get the VCO to run on the desired frequency by selecting the proper inductor and capacitor values. The capacitor value will need to include the varactor and circuit parasitics. After the VCO is running at the desired frequency, then set the VCO sensitivity.

The sensitivity is determined by connecting the control voltage input point to ground and noting the frequency. Then connect the same point to the supply and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sensitivity expressed in Hz/V. Increasing the inductor value while decreasing the capacitor value will increase the sensitivity. Decreasing the inductor value while increasing the capacitor value will lower the sensitivity.

When increasing or decreasing component values, make sure that the center frequency remains constant. Finally, close the loop.

External to the part, the designer needs to implement a **loop filter** to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through an internal 4kΩ resistor. The loop filter is then connected in parallel to this point at pin 23 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC. A passive filter is most common, as it is a low cost and low noise design. An additional pole could be used for reducing the reference spurs, however there is not a way to add the series resistor. This should not be a reason for concern however.

The schematic of the loop filter is as follows.



The transfer function is

$$F(s) = R_2 \cdot \left[\frac{s \cdot \tau_2 + 1}{s \cdot \tau_2 \cdot (s \cdot \tau_1 + 1)}\right]$$

where the time constants are defined as

$$\tau_2 = R_2 \cdot C_2 \quad \text{and} \quad \tau_1 = R_2 \cdot \left[\frac{C_1 \cdot C_2}{C_1 + C_2}\right]$$

The frequency at which unity gain occurs is given by

$$\omega_{LBW} = \frac{1}{\sqrt{\tau_1 \cdot \tau_2}}$$

This is also the loop bandwidth.

If the phase margin (PM) and the loop bandwidth (ω_{LBW}) are known, it is possible to calculate the time constants. These are found using the following equations.

$$\tau_1 = \frac{\sec(PM) - \tan(PM)}{\omega_{LBW}} \quad \text{and} \quad \tau_2 = \frac{1}{\omega^2_{LBW} \cdot \tau_1}$$

With these known, it is then possible to determine the values of the filter components.

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$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_{PD} \cdot K_{VCO}}{\omega^2_{LBW} \cdot N} \cdot \sqrt{\frac{1 + (\omega_{LBW} \cdot \tau_2)^2}{1 + (\omega_{LBW} \cdot \tau_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1\right)$$

$$R_2 = \frac{\tau_2}{C_2}$$

As an example, consider a loop bandwidth of 50kHz, a phase margin of 45°, a divide ratio of 64, a K_{VCO} of 20MHz/V, and a K_{PD} of 0.01592mA/2πrad. Time constant τ_1 is 1.31848µs, time constant τ_2 is 7.68468µs, C_1 is 131.15pF, C_2 is 633.26pF, and R_2 is 12.14kΩ.

In order to perform these calculations, one will need to know the value of two constants, K_{VCO} and K_{PD}. K_{PD} is calculated by dividing the charge pump current by 2π. For the RF2513, the charge pump current is 40µA. K_{VCO} is best found empirically as it will change with frequency and board parasitics. By briefly connecting pin 23 (LOOP FLT) to VCC and then to ground, the frequency tuning range of the VCO can be seen. Dividing the difference between these two frequencies by the difference in the voltage gives K_{VCO} in MHz/V.

The control lines provide an **interface** for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 16 (MOD IN), pin 15 (DIV CTRL), pin 14 (MOD CTRL), pin 24 (OSC SEL), and pin 7 (LVL ADJ) as control pins whose voltage level can be set.

General **RF bypassing** techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias for connection to the ground plane allows one to connect to ground as close as possible to ground pins. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

Pre-compliance testing should be performed during the design process. This can be done with a GTEM cell or at a compliance testing laboratory. It is recommended that pre-compliance testing be performed so that there are no surprises during final compliance testing. This will help keep the product development and release on schedule.

Working with a laboratory offers the benefit of years of compliance testing experience and familiarity with the regulatory issues. Also, the laboratory can often provide feedback that will help the designer make the product compliant.

On the other hand, having a GTEM cell or an open air test site locally offers the designer the ability to rapidly determine whether or not design changes impact the product's compliance. Set-up of an open air test site and the associated calibration is not trivial. An alternative is to use a GTEM test cell.

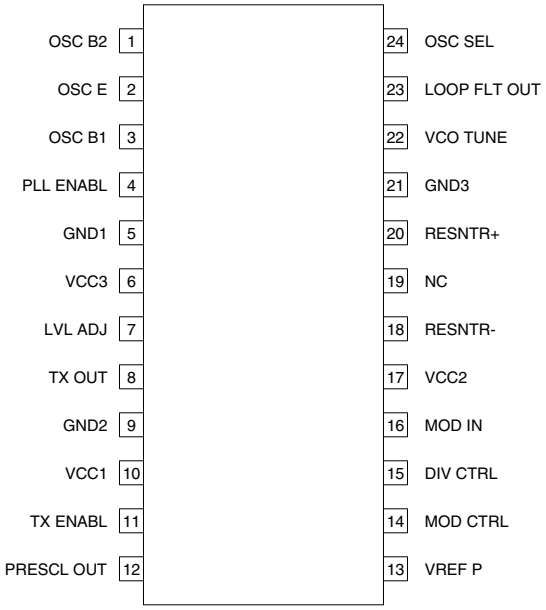
After the design has been completed and passes compliance testing, application will need to be made with the respective regulatory bodies for the geographic region in which the product will be operated to obtain final certifications.

Conclusions

The RF2513 is an FM/FSK UHF transmitter that features a phase-locked output. This device is suitable for use in a CFR Part 15.231 compliant product as well as a local oscillator signal source. Two examples of showing these applications have been provided. Further, the RF2513 is packaged in a low cost SSOP-24 plastic package and requires few external parts, thus making it suitable for low cost designs.

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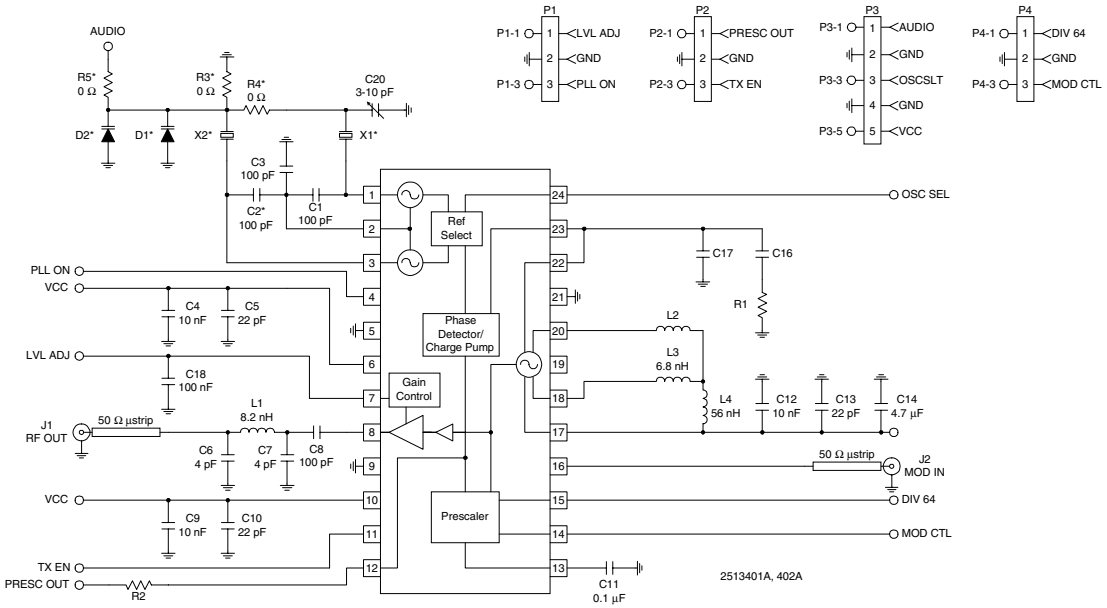
Pin Out



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Evaluation Board Schematic
H (915MHz) and M (868MHz) Boards

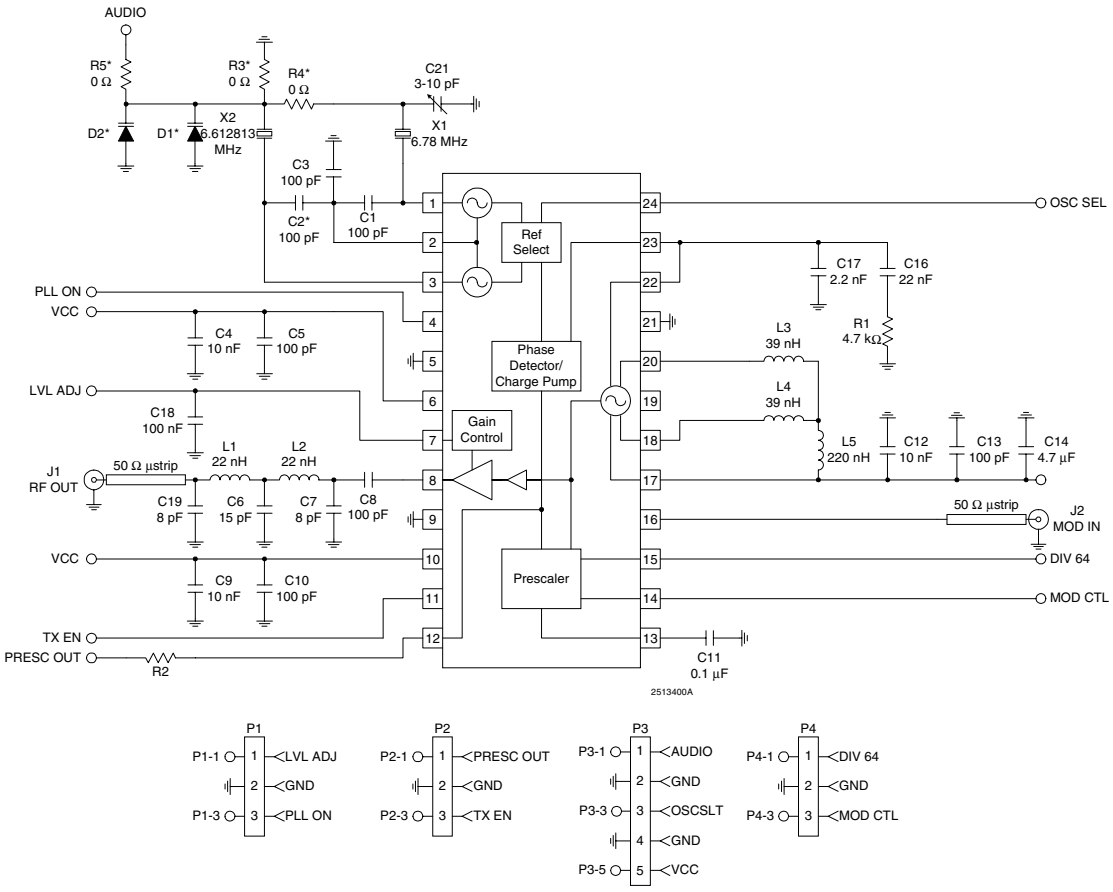
(Download Bill of Materials from www.rfmd.com.)



Board	X1 (MHz)	X2 (MHz)	R1 (kΩ)	L2 (nH)	C16 (nF)	C17 (nF)
M (868MHz)	13.57734	13.41015	2.2	8.2	47 nF	4.7
H (915MHz)	7.15909	7.07549	5.1	6.8	22 nF	2.2

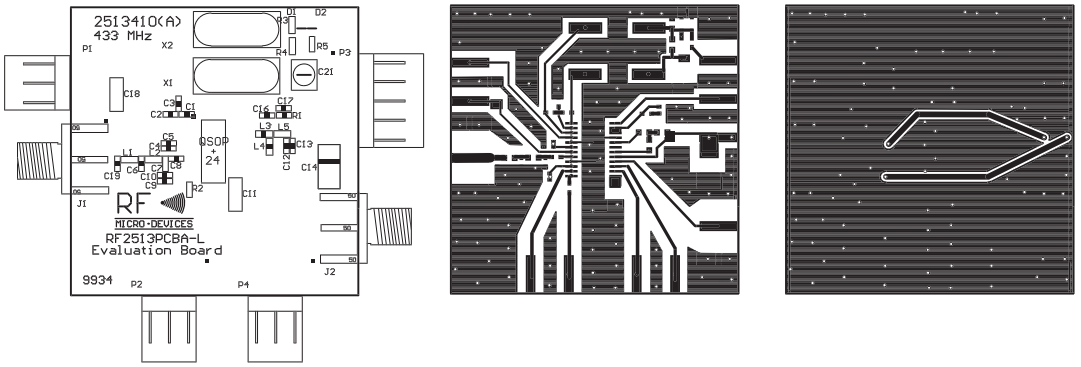
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Evaluation Board Schematic
L (433MHz) Board

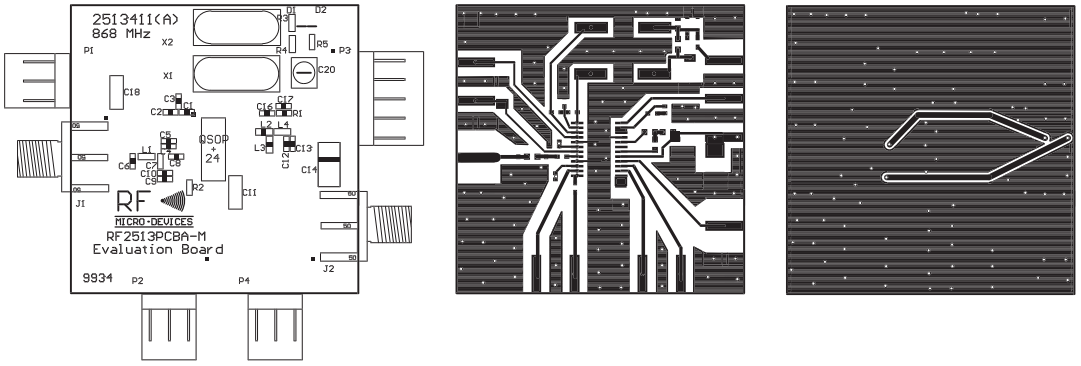


Evaluation Board Layout 433MHz
Board Size 2.0” x 2.0”

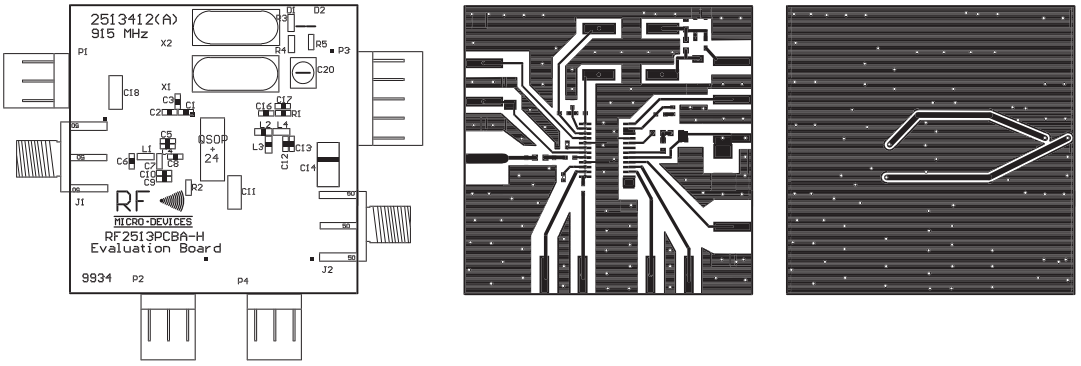
Board Thickness 0.031”, Board Material FR-4



Evaluation Board Layout 868MHz
Board Size 2.0” x 2.0”



Evaluation Board Layout 915MHz
Board Size 2.0” x 2.0”



RF MICRO·DEVICES

Preliminary

RF2516

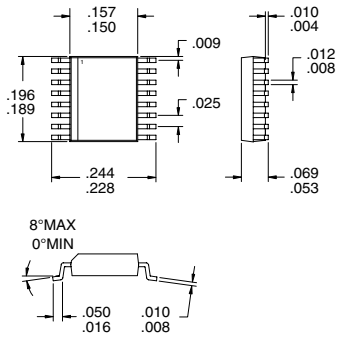
VHF/UHF TRANSMITTER

Typical Applications

- 315/433MHz Band Systems
- Local Oscillator Source
- Part 15.231 Applications
- Remote Keyless Entry
- Wireless Security Systems
- AM/ASK/OOK Transmitter

Product Description

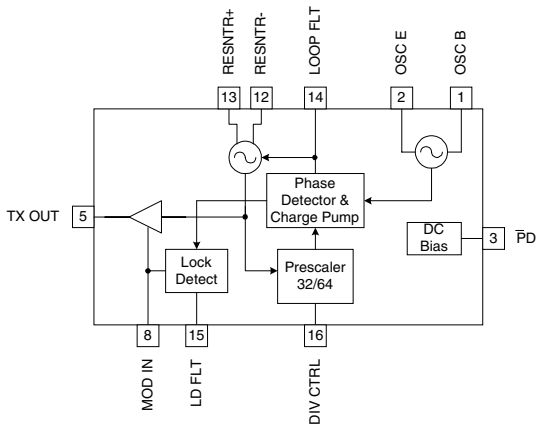
The RF2516 is a monolithic integrated circuit intended for use as a low-cost AM/ASK transmitter. The device is provided in a 16-pin SSOP-16 package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in applications in the North American and European VHF/UHF bands. The integrated VCO, phase detector, prescaler, and reference oscillator transistor require only the addition of an external crystal to provide a complete phase-locked loop. In addition to the standard power-down mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when the PLL is out-of-lock. Currently not recommended for Part 15.249 applications.



Package Style: SSOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- Integrated VCO and Reference Oscillator
- 2.0V to 3.6V Supply Voltage
- Low Current and Power Down Capability
- 100MHz to 960MHz Frequency Range
- Out-of-Lock Inhibit Circuit

11

TRANSCEIVERS

Ordering Information

RF2516	VHF/UHF Transmitter
RF2516 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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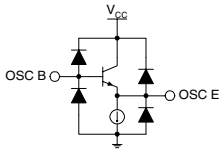
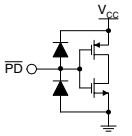
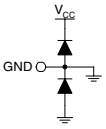
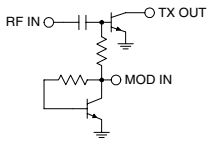
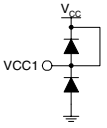
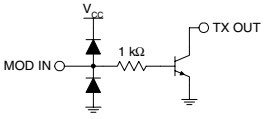
Absolute Maximum Ratings

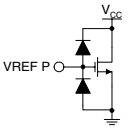
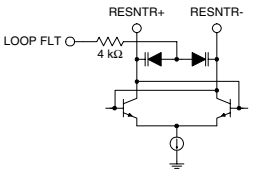
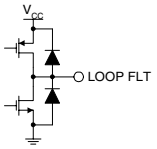
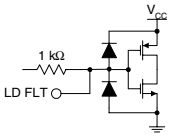
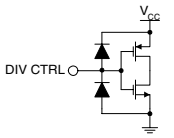
Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
MOD IN	-0.5 to 1.1	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.8V, Freq=433MHz, R_{MODIN}=3kΩ
Frequency Range		100 to 960		MHz	
Modulation		AM/ASK			
Modulation Frequency			1	MHz	
Incidental FM			15	kHz p-p	
Output Power	+8.5	+10		dBm	50Ω load
ON/OFF Ratio		75		dB	
PLL and Prescaler					
Prescaler Divide Ratio		32/64			
VCO Gain, K_{VCO}		20		MHz/V	Frequency and board layout dependent.
PLL Phase Noise		-97		dBc/Hz	10kHz Offset, 50kHz loop bandwidth
		-102		dBc/Hz	100kHz Offset, 50kHz loop bandwidth
Harmonics		-60		dBc	With output tuning.
Reference Frequency			17	MHz	
Crystal Frequency Spurs		-50		dBc	50kHz PLL loop bandwidth
Max Crystal R_S	TBD	35	50	Ω	For a typ. 1ms turn-on time.
Max Crystal Motional Inductance		60		mH	For a typ. 1ms turn-on time.
Charge Pump Current		100		µA	K_{PD}=100µA/2π=0.0159mA/rad
Power Down Control					
Power Down "ON"	Vcc- 0.3V			V	Voltage supplied to the input; device is "ON"
Power Down "OFF"			+0.3	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	100k			Ω	
Turn On Time		1	2	ms	Crystal start-up, 13.57734MHz crystal.
Turn Off Time		1	2	ms	
Power Supply					
Voltage		2.8		V	Specifications
	2.0		3.6	V	Operating limits
Current Consumption (Avg.)	6	10.5		mA	50% Duty Cycle 10kHz Data applied to the MOD IN input. R_{MODIN} (R10)=3kΩ. Output power/DC current consumption externally adjustable by modulation input resistor (see applicable Application Schematic).

Pin	Function	Description	Interface Schematic
1	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 68pF capacitor should be connected between pin 1 and pin 2. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 33pF capacitor should be connected from this pin to ground. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	See pin 1.
3	$\overline{PD}$	Power Down control for all circuitry. When this pin is a logic "low" all circuits are turned off. When this pin is a logic "high", all circuits are operating normally. A "high" is V_{CC}. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
4	GND	Ground connection for the TX OUT amp. Keep traces physically short and connect immediately to ground plane for best performance. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
5	TXOUT	Transmitter output. This output is an open collector and requires a pull-up inductor for bias/matching and a tapped capacitor for matching.	
6	GND1	Ground connection for the TX output buffer amplifier. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	See pin 4.
7	VCC1	This pin is used to supply bias to the TX buffer amplifier. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
8	MOD IN	AM analog or digital modulation can be imparted to the carrier by an input to this pin. An external resistor is used to bias the output amplifiers through this pin. The voltage at this pin must not exceed 1.1V. Higher voltages may damage the device. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
9	VCC2	This pin is used to supply DC bias to the VCO, crystal oscillator, prescaler, phase detector, and charge pump. An IF bypass capacitor should be connected directly to this pin and returned to ground. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	See pin 7.
10	GND2	Digital PLL ground connection. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	See pin 4.

Pin	Function	Description	Interface Schematic
11	VREF P	Bias voltage reference pin for bypassing. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
12	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 13.	
13	RESNTR+	See pin 12.	
14	LOOP FLT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
15	LD FLT	This pin is used to set the threshold of the lock-detect circuit. A shunt capacitor should be used to set an RC time constant with the on-chip series 1k resistor. This signal is used to clamp (enable or disable) the MOD IN circuitry. The time constant should be approximately 10 times the reference period. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
16	DIV CTRL	Logic “High” input selects divide-by-64 prescaler. Logic “Low” input selects divide-by-32 prescaler. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	

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RF2516 Theory of Operation

Introduction

Short range radio devices are becoming commonplace in today's environment. The most common examples are the remote keyless entry systems popular on many new cars and trucks, and the ubiquitous garage door opener. Other applications are emerging with the growth in home security, automation and the advent of various remote control applications. Typically these devices have been simplex, or one-way, links. They are also typically built using surface acoustic wave (SAW) devices as the frequency control elements. This approach has been attractive because the SAW devices have been readily available and a transmitter, for example, could be built with only a few additional components. Recently however, RF Micro Devices, Inc. (RFMD), has introduced several new components that enable a new class of short-range radio devices based on the use of crystals and phase-locked loops for frequency control. These devices are superior in performance and comparable in cost to the traditional SAW-based designs. The RF2516 is an example of such a device. The RF2516 is targeted for applications such as 315MHz and 433MHz band remote keyless entry systems and wireless security systems, as well as other remote control applications.

The RF2516 Transmitter

The RF2516 is a low-cost AM/ASK VHF/UHF transmitter designed for applications operating within the frequency range of 100MHz to 1000MHz. In particular, it is intended for 315MHz to 433MHz band systems, remote keyless entry systems, and FCC Part 15.231 periodic transmitters. It can also be used as a local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop. In addition to the standard power-down mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when the PLL is out-of-lock.

The device is manufactured on a 25GHz Silicon Bipolar-CMOS process and packaged in an industry standard SSOP-16 plastic package. This, combined with the low external parts count, enables the designer to achieve small-footprint, high-performance, low-cost designs.

The RF2516 is designed to operate from a supply voltage ranging from 2.0V to 3.6V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to +10dBm output power into a 50Ω load, and is intended to comply with FCC requirements for unlicensed remote control transmitters. ESD protection is provided on all pins except VCO and TX OUT.

The RF2516 Functional Blocks

A PLL consists of a reference oscillator, a phase detector, a loop filter, a voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2516 includes all of these internally, except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillator** is a Colpitts type oscillator. Pins 1 (OSC B) and 2 (OSC E) provide connections to a transistor that is used as the reference oscillator. The Colpitts configuration is a low parts count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of the transistor. The drive level should, in either case, be around 500mV$_{PP}$ This level prevents overdriving the device and keeps the phase noise and reference spurs to a minimum.

The **prescaler** divides the VCO frequency by either 64 or 32, using a series of flip-flops, depending upon the logic level present at the DIV CTRL pin. A high logic level will select the 64 divisor. A low logic level will select the 32 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

The RF2516 contains an onboard phase detector and charge pump. The **phase detector** compares the phase of the reference oscillator to the phase of the VCO. The phase detector is implemented using flip-flops in a topology referred to as either "digital phase/frequency detector" or "digital tri-state comparator". The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency.

When both inputs of the flip-flops are identical, the signals are both frequency- and phase-locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter, or enter into a high impedance state. The name "tri-state comparator" comes from this.

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The main benefit of this type of detector is the ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it uses frequency error for correction. This type of detector will lock under all conditions.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. Its inputs are the outputs of the phase detector flip-flops. Since there are two flip-flops, there are four possible states. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. The state where both inputs are high will not occur. The other states are either charging or discharging the loop filter. The loop filter integrates the pulses coming from the charge pump to create a control voltage for the voltage controlled oscillator.

The **VCO** is a tuned differential amplifier with the bases and collectors cross-coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors, and is comprised of internal varactors and external inductors. The designer selects the inductors for the desired frequency of operation. These inductors also provide DC bias for the VCO.

The output of the VCO is buffered and applied to the prescaler circuit, where it is divided by either 32 or 64, as selected by the designer, and compared to the reference oscillator frequency.

The **transmit amplifier** is a two-stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 10dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The **lock-detect circuitry** connects to the output of the phase detector circuitry and is used to disable the transmitter when the VCO is not phase-locked to the reference oscillator. This is necessary to avoid unwanted out-of-band transmission and to provide compliance with regulatory limits during an unlocked condition.

There are many possible reasons for the PLL not to be locked. For instance, there is a short period during the start of any VCO in which the VCO begins oscillating and the reference oscillator builds up to full amplitude. During this period, the frequency will likely be outside the authorized band. Typically, the VCO starts much faster than the reference oscillator. Once both VCO and reference oscillators are running, the phase detector can start slewing the VCO to the correct frequency, slowly sliding across 200MHz of occupied spectrum. In competitive devices, the VCO radiates at full power under all of these conditions.

The lock protection circuit in the RF2516 is intended to stabilize quickly after power is applied to the chip, and to disable the base drive to the transmit amplifier. This attenuates the output to levels that will be generally acceptable to regulatory boards as spurious emissions. Once the phase detector has locked the oscillators, then the lock circuit enables the MOD IN pin for transmission of the desired data. There is no need for an external microprocessor to monitor the lock status, although that can be done with a low current A/D converter in a system micro, if needed. The lock-detect circuitry contains an internal resistor which, combined with a designer-chosen capacitor for a particular RC time constant, filters the lock-detect signal. This signal is then passed through an internal Schmitt trigger and used to enable or disable the transmit amplifier.

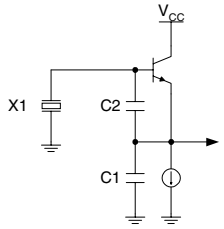
If the oscillator unlocks, even momentarily, the protection circuit quickly disables the output until the lock is stable. These unlocks can be caused by low battery voltage, poor power supply regulation, severe shock of the crystal or VCO, antenna loading, component failure, or a myriad of unexpected single-point failures.

The RF2516 contains onboard band gap reference voltage circuitry which provides a stable **DC bias** over varying temperature and supply voltages. Additionally, the device features a power-down mode, eliminating battery disconnect switches.

Designing With the RF2516

The **reference oscillator** is built around the onboard transistor at pins 1 and 2. The intended topology is that of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low-cost solutions. The topology of this type of oscillator is as seen in the following figure.

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This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C_1 and C_2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations[6]:

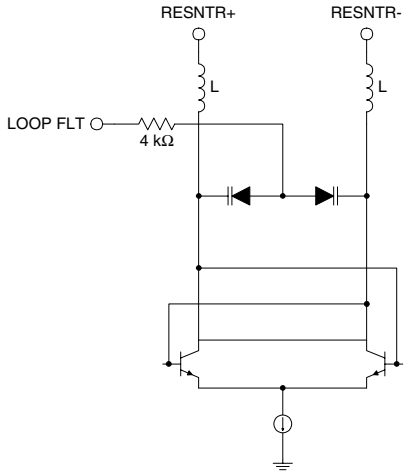
$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

The load capacitance is usually 32pF. The variable freq is the oscillator frequency in MHz. The frequency can be adjusted by either changing C_2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at pin 2 (OSC E). It has been found that the level at this pin should generally be around 500mV$_{PP}$ or less. This will reduce the reference spur levels and reduce noise from distortion. If this level is higher than 500mV$_{PP}$ then decrease the value of C_1. The values of these capacitors are usually tweaked during design to meet performance goals, such as minimizing the start-up time.

Additionally, by placing a variable capacitor in series with the crystal, one is able to adjust the frequency. This will also alter the drive level, so it should be checked again.

An important part of the overall design is the **voltage controlled oscillator**. The VCO is configured as a differential amplifier. The VCO is tuned via internal varactors. The varactors are tuned by the loop filter output voltage through a 4kΩ resistor.



As mentioned earlier, the inductors and the varactors are tuning a differential amplifier. To tune the VCO the designer only needs to calculate the value of the inductors connected to pins 12 and 13 (RESNTR- and RESNTR+). The inductor value is determined by the equation:

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C} \cdot \frac{1}{2}$$

In this equation, *f* is the desired operating frequency and *L* is the value of the inductor required. The value *C* is the amount of capacitance presented by the varactors and parasitics. For calculation purposes 1.5pF should be used. The factor of one-half is due to the inductors being in each leg. As an example, assume an operating frequency of 433MHz. The calculated value of each inductor is 45nH. A 47nH inductor would be appropriate as the closest available value.

The setup of the VCO can be summarized as follows. First, open the loop. Next, get the VCO to run on the desired frequency by selecting the proper inductor and capacitor values. The capacitor value will need to include the varactor and circuit parasitics.

After the VCO is running at the desired frequency, set the VCO sensitivity. The sensitivity is determined by connecting the control voltage input point to ground and noting the frequency.

Connect the same point to the supply, and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sen-

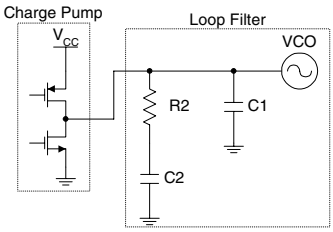
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sitivity expressed in Hz/V. Increasing the inductor value while decreasing the capacitor value will increase the sensitivity. Decreasing the inductor value while increasing the capacitor value will lower the sensitivity.

When increasing or decreasing component values, make sure that the center frequency remains constant. Finally, close the loop.

External to the part, the designer needs to implement a **loop filter** to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through a 4kΩ resistor. The loop filter is then connected in parallel to this point at pin 14 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC. A passive filter is most common, as it is a low-cost and low-noise design. An additional pole could be used for reducing the reference spurs, however there is not a way to add the series resistor. However, this should not be a reason for concern.

The schematic of the loop filter is:



The transfer function is:

$$F(s) = R_2 \cdot \left[\frac{s \cdot \tau_2 + 1}{s \cdot \tau_2 \cdot (s \cdot \tau_1 + 1)} \right]$$

where the time constants are defined as:

$$\tau_2 = R_2 \cdot C_2 \text{ and } \tau_1 = R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2} \right)$$

The frequency at which unity gain occurs is given by:

$$\omega_{LBW} = \frac{1}{\sqrt{\tau_1 \cdot \tau_2}}$$

This is also the loop bandwidth.

If the phase margin (PM) and the loop bandwidth (ω_{LBW}) are known, it is possible to calculate the time constants. These are found using the equations[4]:

$$\tau_1 = \frac{\sec(PM) - \tan(PM)}{\omega_{LBW}} \text{ and } \tau_2 = \frac{1}{\omega_{LBW}^2 \cdot \tau_1}$$

With these known, it is then possible to determine the values of the filter components.[4]

$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_{PD} \cdot K_{VCO}}{\omega_{LBW}^2 \cdot N} \cdot \sqrt{\frac{1 + (\omega_{LBW} \cdot \tau_2)^2}{1 + (\omega_{LBW} \cdot \tau_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1 \right) \qquad R_2 = \frac{\tau_2}{C_2}$$

As an example, consider a loop bandwidth of 50kHz, a phase margin of 45°, a divide ratio of 64, a K_{VCO} of 20MHz/V, and a KPD of 0.01592mA/2πrad. Time constant τ1 is 1.31848µs, time constant τ2 is 7.68468µs, C_1 is 131.15pF, C_2 is 633.26pF, and R_2 is 12.14kΩ.

In order to perform these calculations, one will need to know the value of two constants, K_{VCO} and K_{PD}. K_{PD} is calculated by dividing the charge pump current by 2π. For the RF2516, the charge pump current is 100µA. K_{VCO} is best found empirically as it will change with frequency and board parasitics. By briefly connecting pin 14 (LOOP FLT) to VCC and then to ground, the frequency tuning range of the VCO can be seen. Dividing the difference between these two frequencies by the difference in the voltage gives K_{VCO} in MHz/V.

The control lines provide an **interface** for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 8 (MOD IN), pin 16 (DIV CTRL), and pin 3 (PD) as control pins whose voltage level can be set. The lock-detect voltage at pin 15 (LD FLT) is an output that can be monitored by the microcontroller.

Pin 15 (LD FLT) is used to set the threshold of the **lock-detect circuit**. A shunt capacitor is used to set an RC time constant with an on-chip series 1kΩ resistor. The time constant should be approximately 10 times the reference period.

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General **RF bypassing** techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias for connection to the ground plane allows one to connect to ground as close as possible to ground pins. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

Pre-compliance testing should be performed during the design process. This can be done with a GTEM cell or at a compliance testing laboratory. It is recommended that pre-compliance testing be performed so that there are no surprises during final compliance testing. This will help keep the product development and release on schedule.

Working with a laboratory offers the benefit of years of compliance testing experience and familiarity with the regulatory issues. Also, the laboratory can often provide feedback that will help the designer make the product compliant.

On the other hand, having a GTEM cell or an open air test site locally offers the designer the ability to rapidly determine whether or not design changes impact the product's compliance. Set-up of an open air test site and the associated calibration is not trivial. An alternative is to use a GTEM test cell.

After the design has been completed and passes compliance testing, application will need to be made with the respective regulatory bodies for the geographic region in which the product will be operated to obtain final certifications.

RF2516 Typical Applications
FCC Part 15.231 Periodic Transmitter - 315MHz Automotive Keyless Entry Transmitter

The following information is taken or paraphrased from the Code of Federal Regulations Title 47, Part 15, Section 231 (47 CFR 15.231). Part 15 discusses radio frequency devices and section 231 discusses periodic transmissions. Please refer to the regulation itself as the final authority. Additional information may be found on the Internet at www.fcc.gov.

To highlight the main guidelines outlined by this section, there are five main limitations: operating frequency, transmission content, transmission duration, emission bandwidth, and spurious emissions.

Part 15.231 allows operation in two bands: 40.66MHz to 40.70MHz and above 70MHz. Transmission is limited to control signals such as alarm systems, door openers, remote switches, etc. Radio control of toys is not permitted, nor is continuous transmission such as voice or video. Data transmission other than a recognition code is not permitted. Transmission time is limited to 5 seconds (paragraph a) or for 1 second with greater than ten seconds off (paragraph e).

Emission bandwidth between 70MHz and 900MHz can not be more than 0.25% of the center frequency. Above 900MHz, the emission bandwidth cannot be greater than 0.50% of the center frequency. The emission bandwidth is determined from the points that are 20dB down from the modulated carrier. This corresponds to an occupied bandwidth of 4.5MHz at a center frequency of 902MHz, 1.1MHz at 433MHz, and 788kHz at 315MHz.

Spurious emissions limits are listed in tabular form for various frequency ranges in the Section 231. Above 470MHz with a manually activated transmitter, the fundamental field strength at a distance of 3 meters shall not exceed 12,500microvolts/meter. The spurious emissions shall not exceed 1,250microvolt/meter at a distance of 3meters above 470MHz. Refer to Appendix A for a method of converting field strength to power.

In the frequency range of 260MHz to 470MHz, one needs to linearly interpolate the maximum emissions level for both the fundamental and spurious emissions. The equation for this line is given by:

$$E_{\frac{\mu V}{m}} = 41\frac{2}{3} \cdot Freq_{MHz} - 7083\frac{1}{3}$$

This equation is derived from the endpoints of the frequency range and their respective field strengths. Note that the field strength is in microvolts per meter and the frequency is in megahertz. To determine the spurious level, divide the level calculated above for the spurious frequency by ten.

As an example, assume the fundamental is 315MHz and the reference frequency is 9.8MHz. The field strengths of the fundamental, the reference spurs, and the harmonics of the fundamental up through the tenth harmonic are calculated in the following table The

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occupied bandwidth limit is 787.5kHz. As shown in Table A, the fifth, seventh, and ninth harmonics fall into restricted bands as called out in section 15.205. The limits for these restricted bands are called out in section 15.209. The power level in the last column is the level if the output is connected directly to a spectrum analyzer. Refer to Appendix A as to how this column was calculated.

Local Oscillator Source

Since the RF2516 has a phase-locked VCO, it can be used as a signal source. The device is an ASK/OOK transmitter, with the data provided at the MOD IN pin. When the MOD IN is a high logic level, the carrier is transmitted. When MOD IN is a low logic level, then the carrier is not transmitted. Therefore, to use the RF2516 as signal source, simply tie the MOD IN pin to the supply voltage, through a suitable series resistor (minimum 3kΩ).

Conclusions

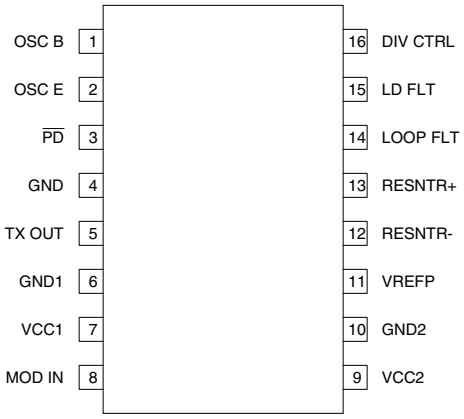
The RF2516 is an AM/OOK VHF/UHF transmitter that features a phase-locked output. This device is suitable for use in a CFR Part 15.231 compliant product as well as a local oscillator signal source. Two examples showing these applications were discussed.

The RF2516 is packaged in a low-cost plastic package and requires few external parts, thus making it suitable for low-cost designs.

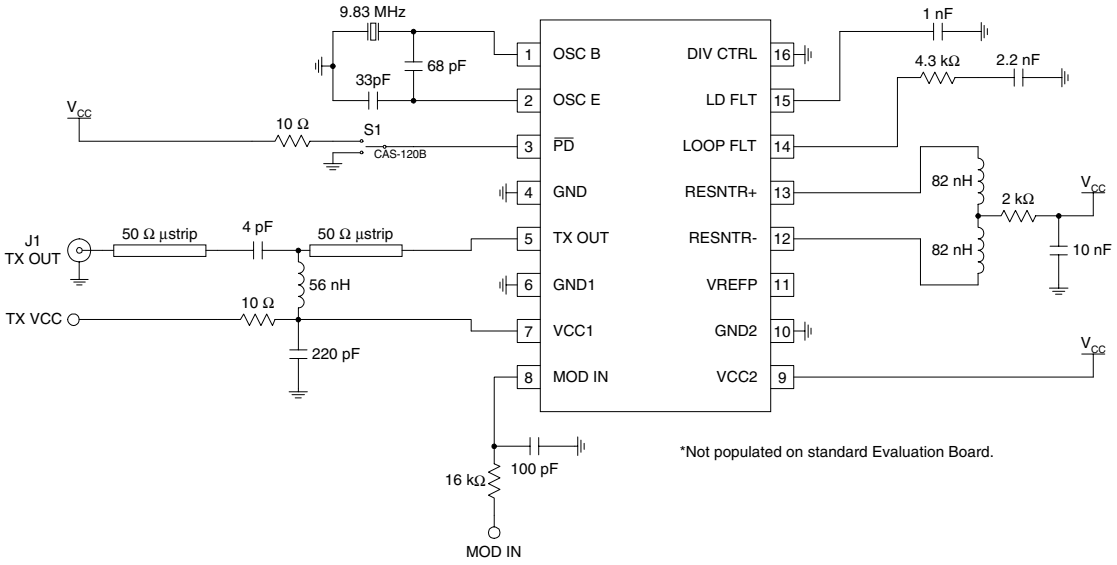
	Frequency (MHz)	15.205 Limits (μV/m @ 3m)	15.231 Limits (μV/m @ 3m)	Final FCC Mask (μV/m @ 3m)	Final FCC Mask (μV/m @ 3m)	Power Level (dBm, 50Ω)
Ref Spur	305.2	-	604.17	604.17	55.62	-39.61
1	315.0	-	6041.67	6041.67	75.62	-19.61
Ref Spur	324.8	-	604.17	604.17	55.62	-39.61
2	630.0	-	604.17	604.17	55.62	-39.61
3	945.0	-	604.17	604.17	55.62	-39.61
4	1260.0	-	604.17	604.17	55.62	-39.61
5	1575.0	500	-	500.00	53.98	-41.25
6	1890.0	-	604.17	604.17	55.62	-39.61
7	2205.0	500	-	500.00	53.98	-41.25
8	2520.0	-	604.17	604.17	55.62	-39.61
9	2835.0	500	-	500.00	53.98	-41.25
10	3150.0	-	604.17	604.17	55.62	-39.61

Table A

Pin Out


OSC B 1
OSC E 2
PD 3
GND 4
TX OUT 5
GND1 6
VCC1 7
MOD IN 8
16 DIV CTRL
15 LD FLT
14 LOOP FLT
13 RESNTR+
12 RESNTR-
11 VREFP
10 GND2
9 VCC2

Application Schematic
315MHz

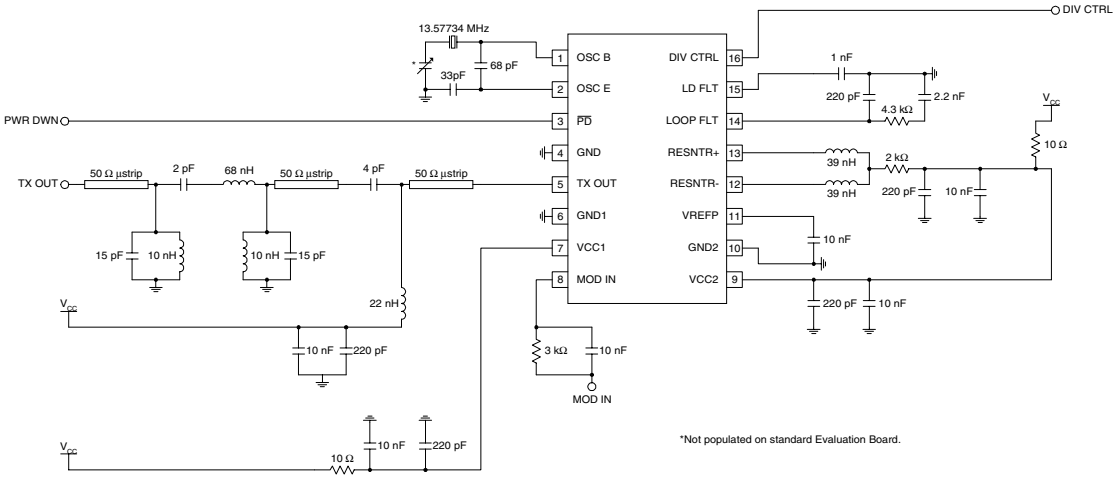


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TRANSCEIVERS

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Application Schematic
433MHz



*Not populated on standard Evaluation Board.

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
2.0	1k	11.08	-6.23
	3k	10.83	-4.40
	5k	4.61	-5.61
	7k	4.00	-6.66
	9k	3.63	-8.08
	11k	3.42	-8.93
	13k	3.26	-10.04
	15k	3.15	-10.71
	17k	3.07	-11.58
	19k	3.01	-12.32
	21k	2.95	-13.10

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
2.4	1k	14.05	7.94
	3k	9.00	7.63
	5k	7.48	5.95
	7k	6.73	4.64
	9k	6.16	3.35
	11k	5.79	2.40
	13k	5.53	1.47
	15k	5.29	0.75
	17k	5.13	0.05
	19k	4.98	-0.60
	21k	4.86	-1.26

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
2.8	1k	17.38	7.45
	3k	10.51	8.78
	5k	8.68	7.23
	7k	7.82	6.00
	9k	7.18	4.73
	11k	6.75	3.81
	13k	6.45	2.98
	15k	6.18	2.30
	17k	5.99	1.63
	19k	5.80	1.00
	21k	5.66	0.35

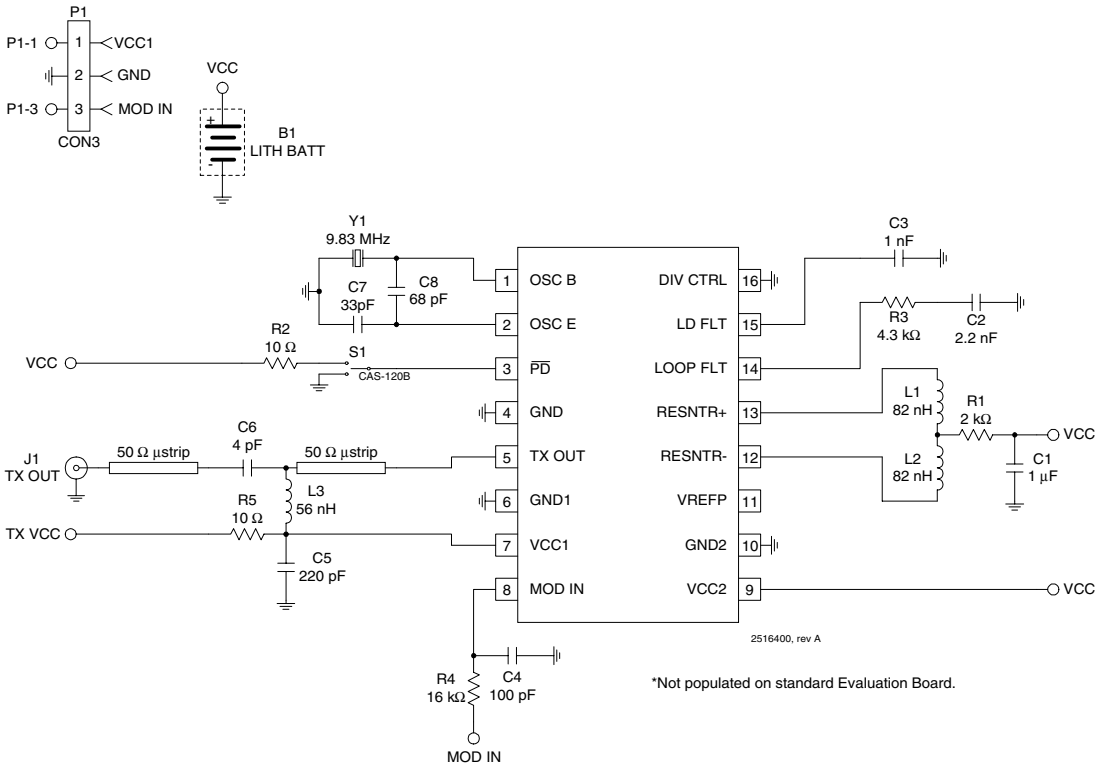
V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
3.2	1k	20.90	6.77
	3k	12.12	9.70
	5k	9.66	8.30
	7k	8.95	7.11
	9k	8.23	5.91
	11k	7.75	5.02
	13k	7.42	4.16
	15k	7.10	3.51
	17k	6.89	2.89
	19k	6.68	2.26
	21k	6.52	1.66

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
3.6	1k	24.68	5.78
	3k	13.88	10.42
	5k	10.94	9.18
	7k	10.14	8.08
	9k	9.34	6.88
	11k	8.81	6.02
	13k	8.44	5.19
	15k	8.09	4.52
	17k	7.86	3.93
	19k	7.63	3.35
	21k	7.44	2.72

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Evaluation Board Schematic
315MHz

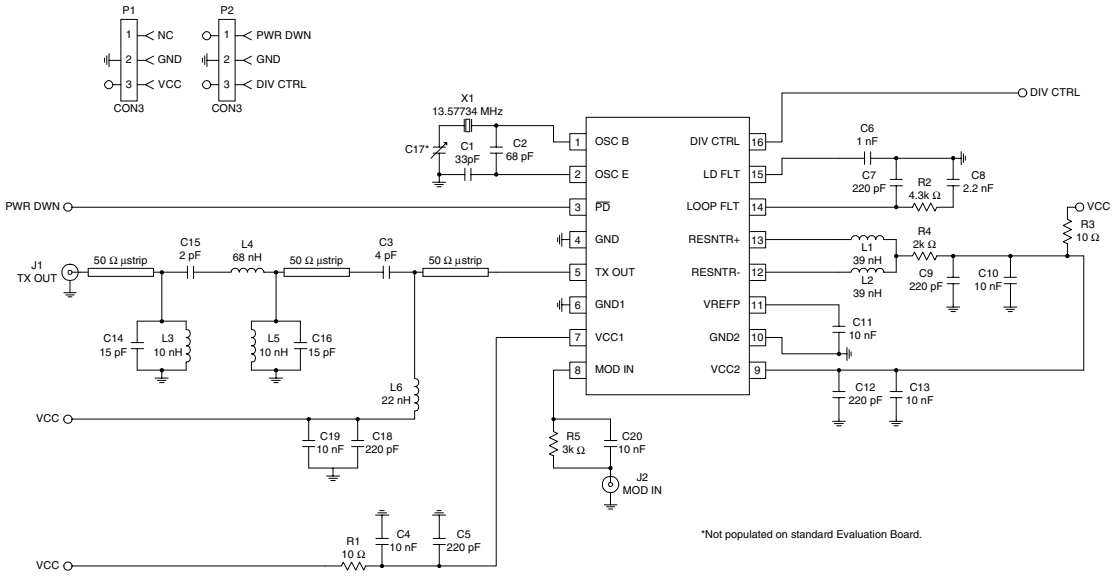
(Download Bill of Materials from www.rfmd.com.)



*Not populated on standard Evaluation Board.

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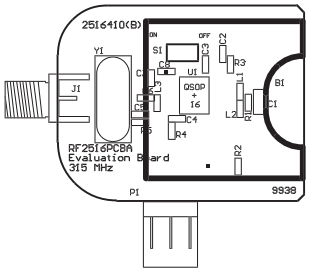
Evaluation Board Schematic
433MHz

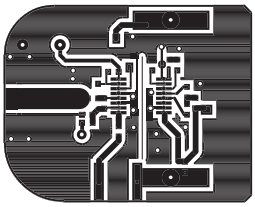


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Evaluation Board Layout (315MHz)
Board Size 1.285” x 1.018”

Board Thickness 0.062”, Board Material FR-4

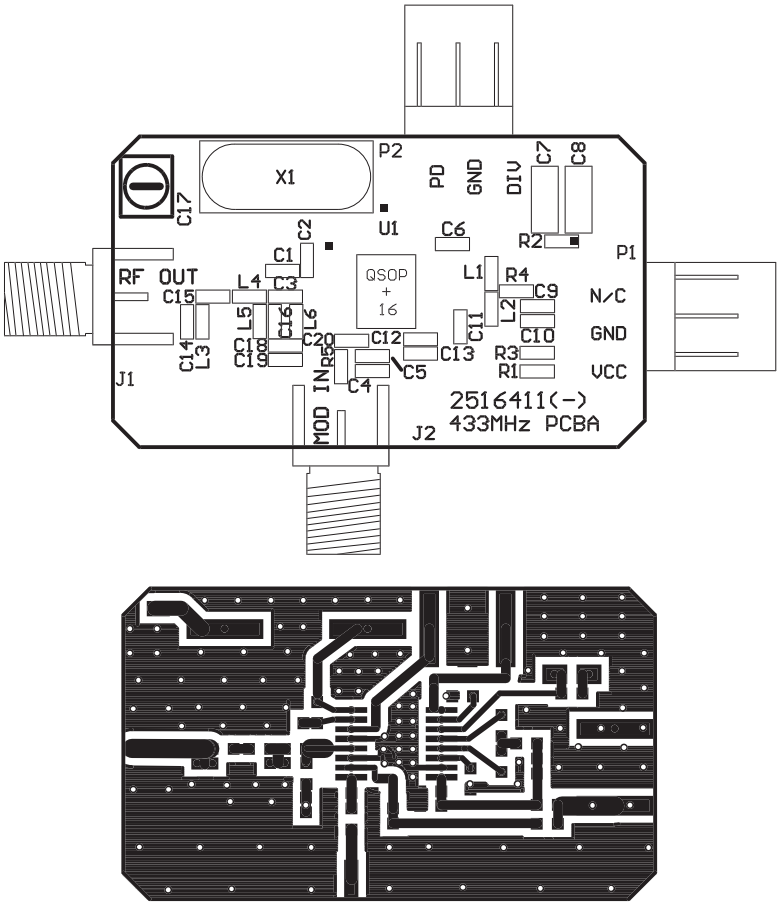




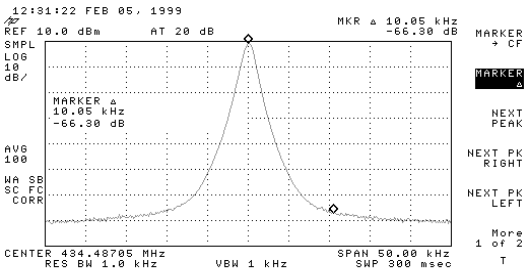
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Evaluation Board Layout (433MHz)
Board Size 1.392” x 1.392”

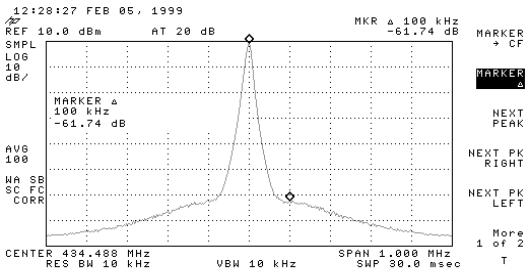
Board Thickness 0.031”, Board Material FR-4



433MHz Phase Noise

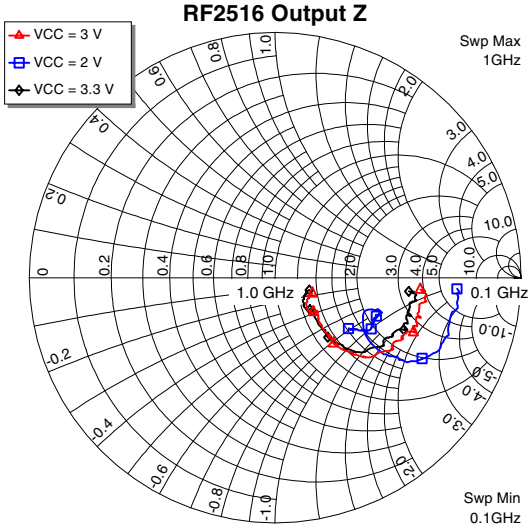


3.5V Phase Noise MODIN=3k



3.5V Phase Noise MODIN=3k

RF2516 Output Z



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RF2905

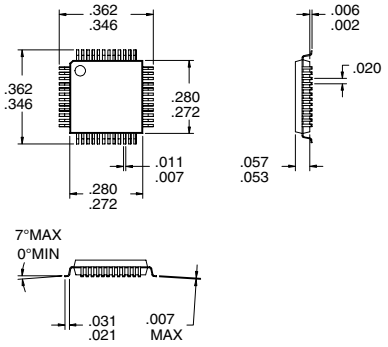
433/868/915MHZ FM/FSK/ASK/OOK TRANSCEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

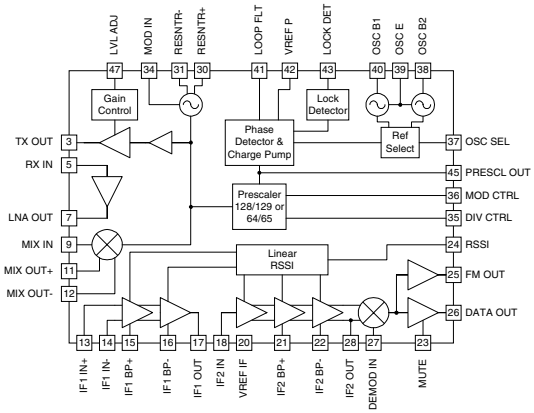
The RF2905 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 48-lead plastic LQFP packaging and is designed to provide a fully functional FM transceiver. The chip is intended for linear (AM, FM) or digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433MHz and 868MHz ISM bands. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Transceiver
- 2.7V to 5.0V Supply Voltage
- Narrow Band and Wide Band FM/FSK
- 300MHz to 1000MHz Frequency Range
- 10dB Cascaded Noise Figure
- 10mW Output Power at 433MHz

Ordering Information

RF2905	433/868/915MHz FM/FSK/ASK/OOK Transceiver
RF2905 PCBA-L	Fully Assembled Evaluation Board (433MHz)
RF2905 PCBA-M	Fully Assembled Evaluation Board (868MHz)
RF2905 PCBA-H	Fully Assembled Evaluation Board (915MHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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RF2905

Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
Prescaler divide ratio		64/65 or 128/129			
Prescaler Output Impedance		50		Ω	
PLL Phase Noise		-75		dBc/Hz	Freq=915MHz, 10kHz Offset, 5kHz Loop Bandwidth
		-100		dBc/Hz	Freq=915MHz, 100kHz Offset, 5kHz loop Bandwidth
Reference Frequency	TBD		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+10		dBm	Freq=433MHz
	0	+3	8	dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage
Antenna Port Impedance		50		Ω	TX ENABL="1". RX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity	-95	-101		dBm	IF BW=180kHz, Freq=915MHz, S/N=8dB
LO Leakage			-70	dBm	
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		25		mV/dB	
RSSI Dynamic Range	70	80		dB	

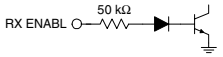
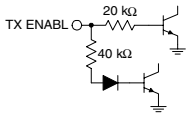
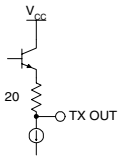
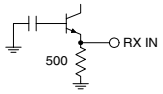
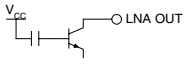
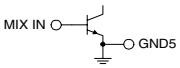
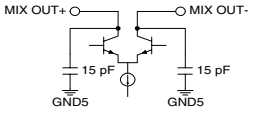
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1". TX ENABL="0"
Antenna Port VSWR			1.5:1		RX Mode
Output Impedance		Open Collector		Ω	433MHz
		Open Collector		Ω	915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		10		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
Maximum Output Voltage				V_{PP}	Balanced
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin
Demod Input Impedance		10		kΩ	
FM Output Impedance		500		Ω	
Data Output Impedance		>1		MΩ	
FM Output Bandwidth	500			kHz	3dB Bandwidth, Dependent upon IF bandwidth and Discriminator.
Data Output Bandwidth	500			kHz	3dB Bandwidth, Z_{LOAD}=1MΩ ‖ 3pF; Dependent upon IF bandwidth and Discriminator.
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ‖ 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	Z_{LOAD}>10kΩ
FM Output AC Level		200		mV_{PP}	Z_{LOAD}>10kΩ

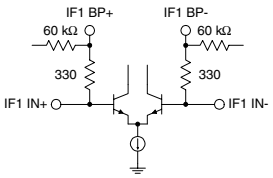
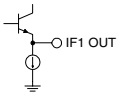
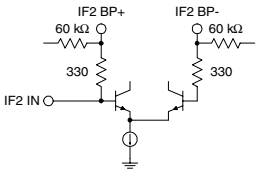
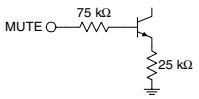
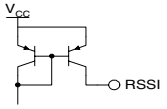
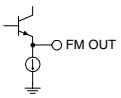
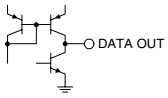
RF2905

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Turn On Time			4	ms	Reference Crystal=7.075MHz
Turn Off Time			4	ms	Dependent upon reference crystal. Higher
RX to TX and TX to RX Time			4	ms	frequencies reduce turn on/off times
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption	22	25	34.5	mA	TX Mode, LVL ADJ=3.6V
	8	10	13.5	mA	TX Mode, LVL ADJ=0V
	7	9	12	mA	RX Mode
			1	µA	Power Down Mode
	5.3	8	10	mA	PLL Only Mode

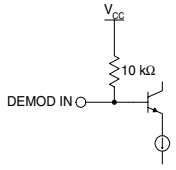
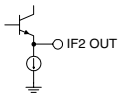
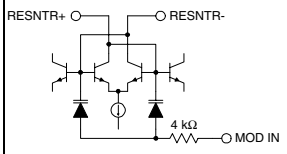
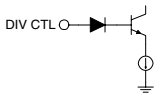
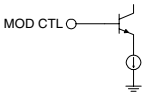
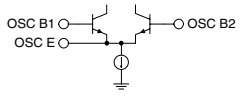
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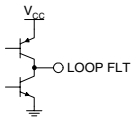
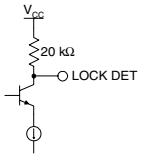
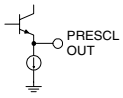
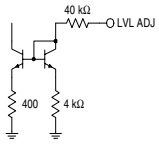
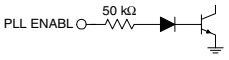
Pin	Function	Description	Interface Schematic
1	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	
2	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
3	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance (see output impedance plot in Figure TBD) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
4	GND2	Ground connection for the 40dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
5	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance (see input impedance plot in Figure TBD) when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
6	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
7	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output.	
8	GND3	Same as pin 4.	
9	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
10	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
11	MIX OUT+	Complementary (with respect to pin 12) IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
12	MIX OUT-	IF output from the RF mixer. For a balanced mixer output, pull-up inductors from pin 11 and 12 to V_{CC} and a capacitor between the pins should be used. The sum of the total pull-up inductance should be used to resonate the capacitor between pins 11 and 12. DC blocking capacitors of 10nF can then be used to connect the balanced output to IF1 IN+ (pin 13) and IF1 IN- (pin 14).	See pin 11.

RF2905

Pin	Function	Description	Interface Schematic
13	IF1 IN+	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
14	IF1 IN-	Functionally the same as pin 13 except inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 13.
15	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
16	IF1 BP-	Same as pin 15.	See pin 13.
17	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 IN	Balanced IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
19	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
20	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	
21	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 18.
22	IF2 BP-	Same as pin 21.	See pin 18.
23	MUTE	This pin is used to mute the data output (DATA OUT). MUTE>2.0V turns the DATA OUT signal on. MUTE<1.0V turns the DATA OUT signal off. The MUTE signal should be logic low in the Sleep Mode.	
24	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.5V, into 51kΩ load, and increases with increasing signal strength.	
25	FM OUT	Linear output from the FM demodulator. This pin is used in analog applications when signal fidelity is important. This output is inverted for low side injection of the LO and normal for high side injection.	
26	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater. When using a RF2905 transmitter and receiver back to back a data inversion will occur, when the LO is low side injected. A high side injection will add an inversion of the Rx data.	

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Pin	Function	Description	Interface Schematic
27	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
28	IF2 OUT	Balanced IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 27 through a 4pF (suggested) capacitor and an FM discriminator circuit.	
29	VCC6	This pin is used is supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
30	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 31 although a small imbalance can be used to tune in the proper frequency range.	
31	RESNTR-	See RESNTR+ description.	See pin 30.
32	VCC2	This pin is used is supply DC bias to the VCO, prescaler, and PLL. An RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
33	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	
34	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 30.
35	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic high (DIVCTRL>2.0V) selects the 64/65 divisor. A logic low (DIVCTRL<1.0V) selects the 128/129 divisor.	
36	MOD CTRL	This pin is used to select the prescaler modulus. A logic high (MOD CTRL>2.0V) selects 64 or 128 for the prescaler divisor. A logic low (MOD CTRL<1.0V) selects 65 or 129 for the prescaler divisor. Due to design timing constraints, the prescaler in the divide by 65 or 129 modes has a limited frequency range for accurate operation. These two modes are not recommended for use from 400MHz to 460MHz.	
37	OSC SEL	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
38	OSC B2	This pin is connected directly to the reference oscillator 2 transistor base. The intended reference oscillator configuration is a modified Colpitts.	

Pin	Function	Description	Interface Schematic
39	OSC E	This pin is connected directly to the emitter of the reference oscillator transistors.	See pin 38.
40	OSC B1	This pin is connected directly to the reference oscillator 1 transistor base. The intended reference oscillator configuration is a modified Colpitts.	See pin 38.
41	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
42	VREF P	Bypass pin for the prescaler reference voltage. A 33nF capacitor to ground is needed to suppress reference spurs in the device. This value may be different for different PCB arrangements.	
43	LOCK DET	This pin provides an analog output indicating the lock status of the PLL. The amplitude of this signal is typically 200mV_{PP} around a DC level of V_{CC}-0.1V.	
44	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
45	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
46	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
47	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
48	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLLENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLLENABL<1.0V) powers down the PLL and VCO.	

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RF2905 Theory of Operation and Application Information

The RF2905 is a part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433/868MHz ISM bands or 915MHz US ISM band.This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products.

In its basic form, the RF2905 can implement a two-way half duplex FSK transceiver with the addition of some crystals, filters, and passive components. There are two reference crystals that allow for the transmit carrier and the receiver LO to be independently generated with a common PLL and VCO. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters but has a -3dB bandwidth of 25MHz and can still be used (with lower gain) at higher frequency with the other type of filters. The PA output and LNA input are available on separate pins and are designed to be connected together through a DC blocking capacitor. In the Transmit mode, the PA will have a 50Ω impedance and the LNA will be a high impedance. In Receive mode, the LNA will have a 50Ω interface and the PA will have a high impedance. This eliminates the need for a TX/RX switch and allows a single RF filter to be used in transmit and receive modes. Separate access to the PA and LNA allow the RF2905 to interface with external components such as higher power PA's, lower NF LNA's, upconverters, and downconverters for a variety of implementations.

FM/FSK SYSTEMS

The MOD IN pin drives an internal varactor for modulating the VCO. This pin can be driven with a voltage level needed to generate the desired deviation. This voltage can be carried on a DC bias to select the desired slope (deviation/volt) for FM systems. Or, a resistor divider network referenced to Vcc or ground can divide down logic level signals to the appropriate level for a desired deviation in FSK systems.

On the receiver demod, two outputs are available, an analog FM output and a digital FSK output. The FM output is a buffered signal coming off of the quadrature demodulator. The digital output is generated by a data slicer that is DC coupled differentially to the demodulator. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesired 2xIF product. This balanced data slicer has a speed advantage over a conventional adaptive data slicer where a large capacitor is used to provide DC reference for bit decision. Since the balanced data slicer does not have to charge a large capacitor, the RF2905 exhibits a very fast response time. For best operation of the on-chip data slicer, FM deviation needs to exceed the carrier frequency error anticipated between the receiver and transmitter with margin.

The data slicer itself is a transconductance amp and the DATA OUT pin is capable of driving rail to rail output only into a very high impedance and small capacitance. The amount of capacitance will determine the bandwidth of the DATA OUT. At a 3pF load, the bandwidth is in excess of 500kHz. The rail to rail output of the data slicer is also limited by the frequency deviation and bandwidth of the IF filters. With the 180kHz bandwidth filters on the eval boards, the rail to rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation vs. data rate (mod index) is important in evaluating the applicability of the RF2905 for a given data rate.

While this type of data slicer is best for wideband deviation, it can also work for narrowband if care is taken to minimize frequency differences. By loading down the DATA OUT pin, the output will be limited to a small data signal on a DC carrier. With this signal, an external data slicer can be used to achieve higher data rates or improve performance in narrow deviations. Alternatively, an AFC loop can be added to correct for frequency errors with a few external components.

For FM or FSK modulation, an internal varactor is used to directly modulate the VCO with the baseband data. The primary consideration when directly modulating the VCO is the data rate verses PLL loop bandwidth. The PLL will track out the modulation to the extent of its loop bandwidth which distorts the modulating data. Therefore, the lower frequency components of the modulating data should be 5 to 10 times the loop bandwidth to minimize the distortion. The lower frequency components are generated by long strings of 1's or 0's in the data stream. By limiting the number of consecutive, same bits, the lower frequency component can be set. In addition, the data stream should be balanced to minimize distortion. Using a coding pattern such as Manchester is highly recommended to optimize system performance.

The PLL loop bandwidth is important in several other system parameters. For example, switching from transmit to receive requires the VCO to retune to another frequency. The switching speed is proportional to the loop bandwidth, the higher the loop bandwidth, the

faster the switching times. Phase noise of the VCO is another factor. Phase noise outside of the loop bandwidth is due to the noise of the VCO itself rather than the crystal reference. A design trade-off must be made here in selecting a PLL loop bandwidth with acceptable phase noise and switching characteristics and minimal distortion of the modulation data.

AM/ASK SYSTEMS

The transmitter of the RF2905 has an output power level adjustment (LVL ADJ) that can be used to provide approximately 18dB of power control for amplitude modulation. The RSSI output of the receiver section can be used to recover the modulation. The RSSI output is from a current source and needs to have a resistor to convert to a voltage. A 51kΩ resistive load will produce an RSSI voltage of 0.7V to 2.5V, typically. A parallel capacitor is suggested to limit the bandwidth and filter noise. For ASK applications, the 18dB range of the LVL ADJ does not produce enough voltage swing in the RSSI for reliable communication. The On-Off keying (OOK) is suggested to provide reliable communications. To achieve this, both the LVL ADJ and TX ENABL need to be controlled together (please note that LVL ADJ cannot be left high when TX ENABL is low). This will provide a on/off ratio of >50dB. One unfortunate consequence of modulating this way is VCO pulling by the power amp. This results in a spurious output outside the desired transmit band as the PLL momentarily loses lock and reacquires. This can be avoided by pulse shaping the TX data to slow the change in the VCO load to a pace that the PLL can track with its given loop bandwidth. The loop bandwidth can also be increased to allow it to track faster changes due to load pulling.

For the ASK/OOK receiver demodulator, an external data slicer is required. The RSSI output is used to provide both the filtered data and a very low pass filtered (relative to the data rate) DC reference to a data slicer. Because the very low pass filter has a slow time constant, a longer preamble may be required to allow for the DC reference to get to a stable state. Here, as in the case of the FSK transmitter, the data pattern also affects the DC reference and the reliability of the received data. Again, a coding scheme such as Manchester such should be used to improve data integrity.

APPLICATION AND LAYOUT CONSIDERATIONS

Both the RX IN and TX OUT have a DC bias on them. Therefore, DC blocking caps are required. If the RF filter has DC blocking characteristics like a ceramic dielectric filter, then only 1 DC blocking capacitor would be needed to separate the DC of RX IN and TX OUT. These are RF signals and care should be taken to route these signals keeping them physically short. Because of the 50Ω/high impedance nature of these two signals, they may be connected together into a signal 50Ω device such as a filter. An external LNA or PA can be used, if desired, but an external RX/TX switch may be required.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO either radiated or coupled by traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2905 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible. Figure 1 is a recommended layout pattern for the VCO components. When using loop bandwidths lower than the 5kHz shown on the eval board, better filtering of the Vcc at the resonators (and lower Vcc noise as well) will help reduce phase noise of the VCO. A series resistor of 100Ω to 200Ω and a 1μF or larger capacitor can be used.

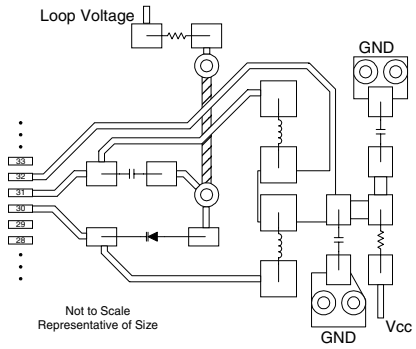


Figure 1. Recommended VCO Layout

For the interface between the LNA/mixer, the coupling capacitor should be as close to the RF2905 pins as possible with the bias inductor being further away. Once again, the value of the inductor can be changed to compensate to trace inductance. The output impedance of the LNA is in the order of several kΩ which makes matching to 50Ω very hard. If image filtering is desired, a high impedance filter is recommended.

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The quad tank of the discriminator can be implemented with ceramic discriminators available from a couple of sources. This design works well for wideband applications and where the temperature range is limited. The temperature coefficient of a ceramic discriminator can be in the order of +/- 50ppm per degree C. An automatic frequency control loop can be implemented using the DC level of the FM OUT for feedback to an external varactor on the reference crystal. An alternative to the ceramic discriminator is a LC tank. Figure 2 shows a schematic implementation of a LC tank.

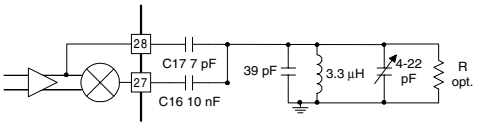


Figure 2. LC Type Discriminator Circuit

The DEMOD IN pin has a DC bias on it and must be DC blocked. This can be done either at the pin or at the ground side of the LC tank (this must also be done if a parallel resistor is used with a ceramic discriminator). The decision whether to used a LC or a ceramic discriminator should be based upon the frequency deviation in the system, discriminator Q needed, and frequency and temperature tolerances. Tuning of the LC tank is required to overcome the component tolerances in the tank.

PREDICTING AND MINIMIZING PLL LOCK TIME

The RF2905 implements a conventional PLL on chip, with a VCO followed by a prescaler dividing the output frequency down to be compared with a signal from the reference oscillator. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF29.5 is:

$$\text{Lock time} = D/fc + 35000 * C * dV$$

Where D is a factor to account for the loop damping. For loops with low phase margin (30° to 40°), use D=2 whereas for loops with better phase margin (50° to 60°), use D=1. fc is the loop cut frequency. C is the sum of all shunt capacitors in the loop filter. dV is the required step voltage change to produce the desired frequency change during the transient.

To lock faster, we need to minimize C.

1. To this end, use the divide by 128 rather than the 64, and a correspondingly lower frequency reference crystal to achieve the desired output frequency.
2. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.
3. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

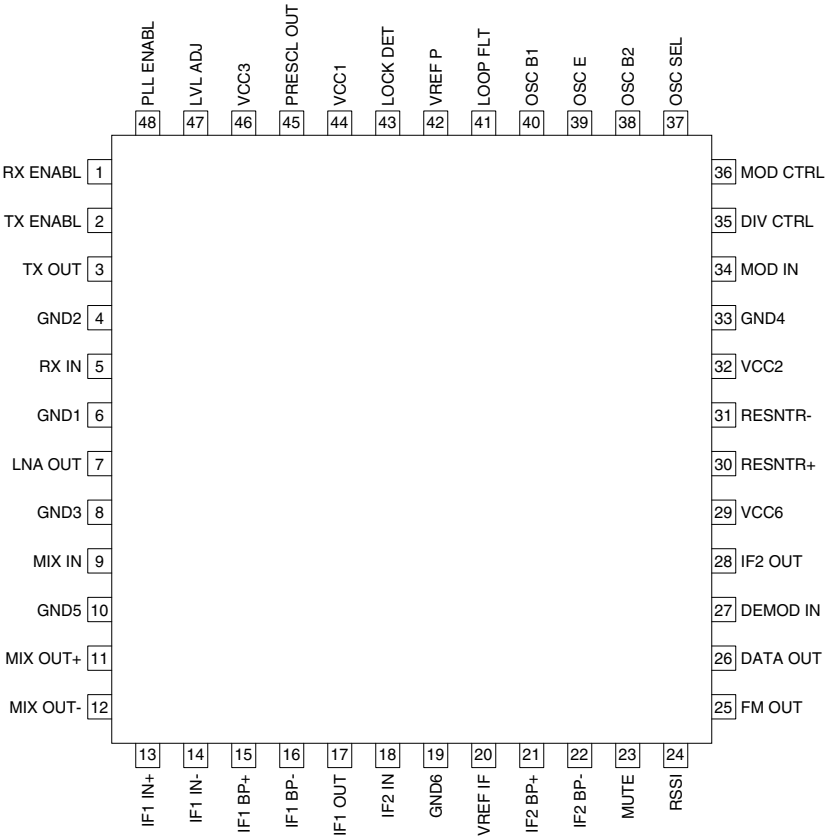
CRYSTAL SELECTION

Several issues arise in the selection of the crystals. Timing specifications such as start-up and switching are related to the crystal specifications, as well as external circuitry. The tolerance of the crystals are also an issue in optimum radio performance. In general, tighter tolerance crystals lead to better performance and are more critical to higher data rates. Frequency offsets between the TX crystal, RX crystal and discriminator generate duty cycle variations in the receive demodulator.

The crystals used on the RF2905 evaluation boards are specified as a parallel resonant, 30pF crystal with a maximum ESR of 80Ω. The initial tolerance is ±20ppm and temperature stability is ±30ppm for -10°C to 70°C. The transistor oscillator will work with a variety of different crystals and the final crystal specifications should be evaluated for each application.

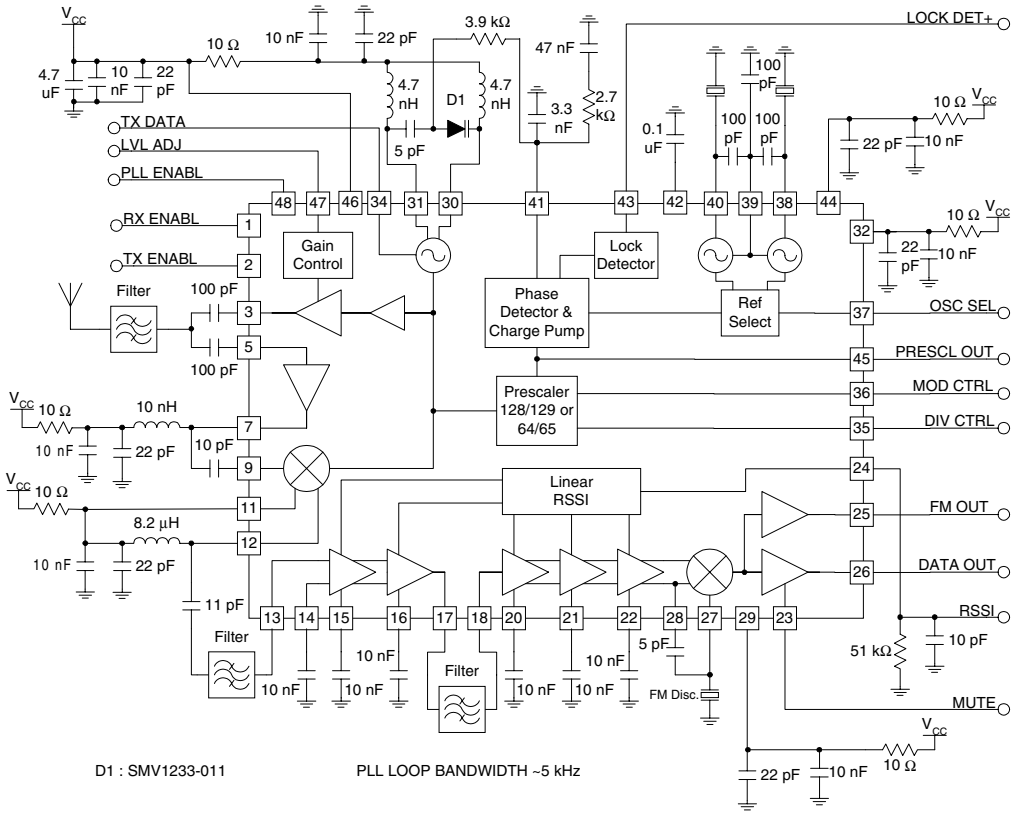
Faster start-up or switching times are achievable by specifying crystals with low motion inductance and low motional resistance. Additionally, the feedback caps of the oscillator can be changed to increase the voltage on the crystal. Generally, crystals in the leaded HC-49U packages will provide better start-up times than the smaller surface-mount types used on the evaluation board.

Pin Out


PLL ENABL 48
LVL ADJ 47
VCC3 46
PRESCL OUT 45
VCC1 44
LOCK DET 43
VREF P 42
LOOP FLT 41
OSC B1 40
OSC E 39
OSC B2 38
OSC SEL 37
RX ENABL 1
TX ENABL 2
TX OUT 3
GND2 4
RX IN 5
GND1 6
LNA OUT 7
GND3 8
MIX IN 9
GND5 10
MIX OUT+ 11
MIX OUT- 12
36 MOD CTRL
35 DIV CTRL
34 MOD IN
33 GND4
32 VCC2
31 RESNTR-
30 RESNTR+
29 VCC6
28 IF2 OUT
27 DEMOD IN
26 DATA OUT
25 FM OUT
13 IF1 IN+
14 IF1 IN-
15 IF1 BP+
16 IF1 BP-
17 IF1 OUT
18 IF2 IN
19 GND6
20 VREF IF
21 IF2 BP+
22 IF2 BP-
23 MUTE
24 RSSI

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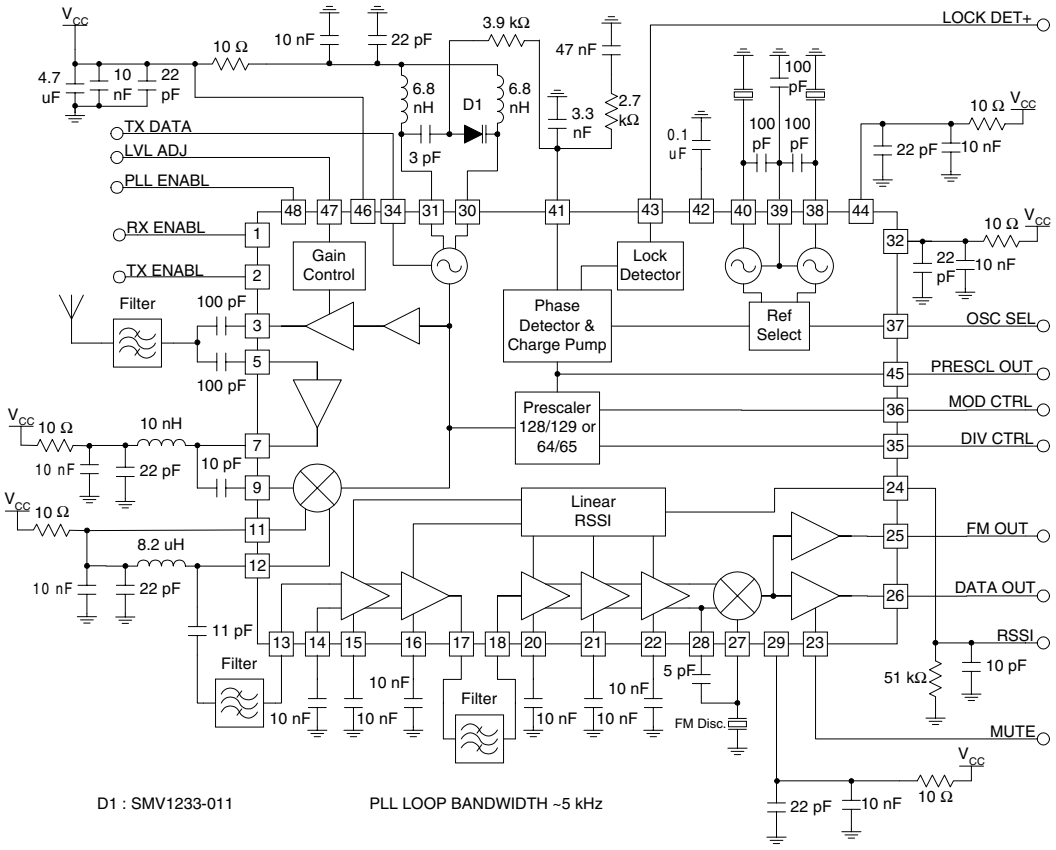
Application Schematic
915MHz



D1 : SMV1233-011

PLL LOOP BANDWIDTH ~5 kHz

Application Schematic
868MHz

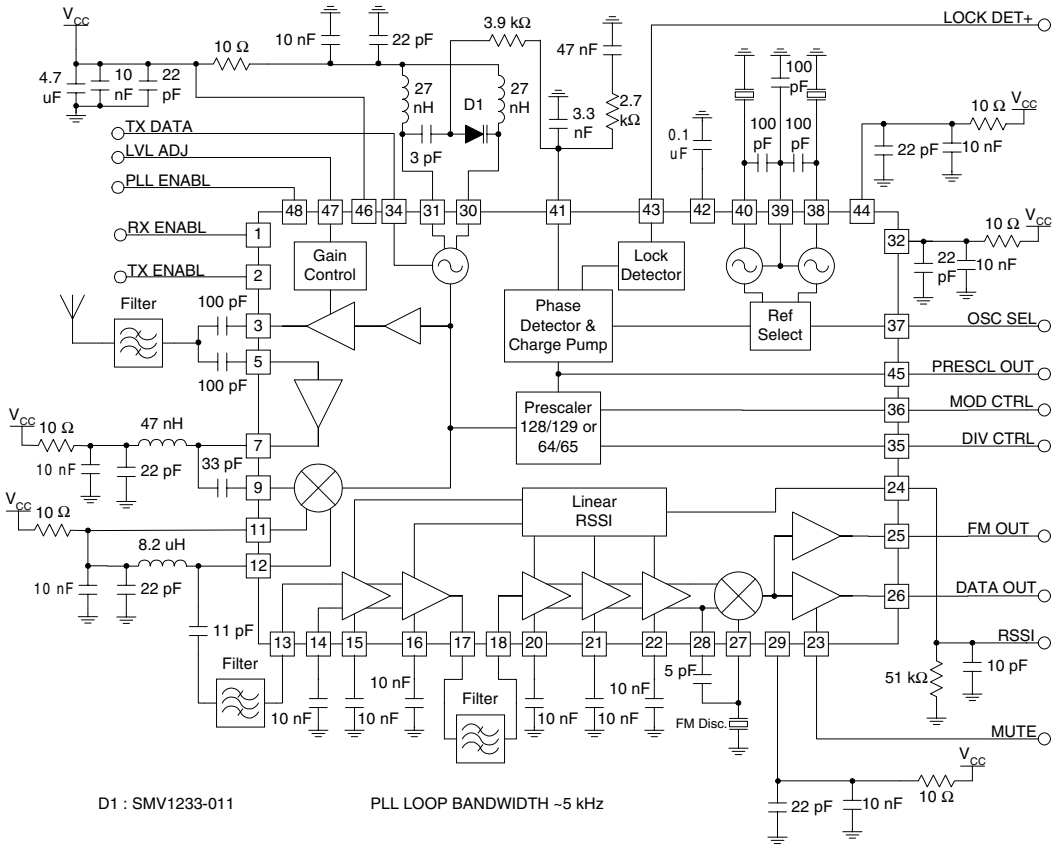


D1 : SMV1233-011

PLL LOOP BANDWIDTH ~5 kHz

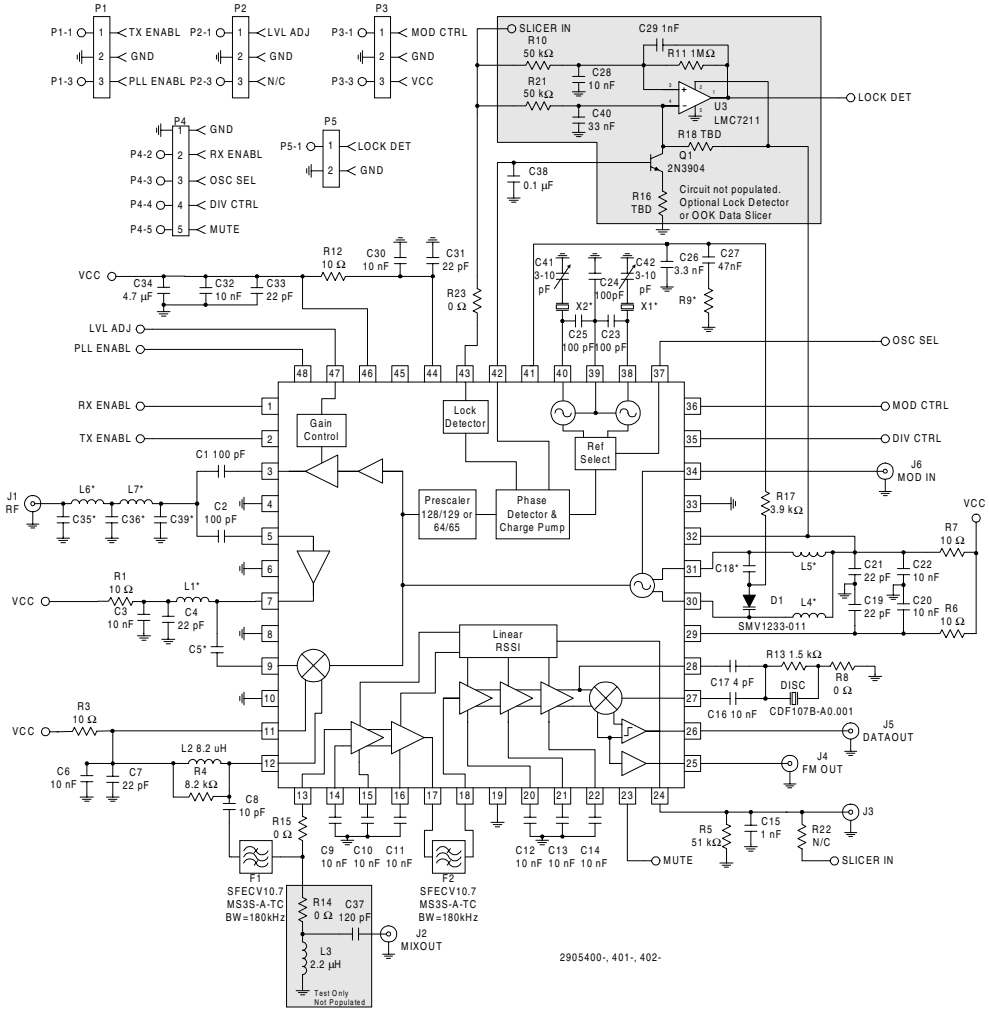
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Application Schematic
433MHz



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

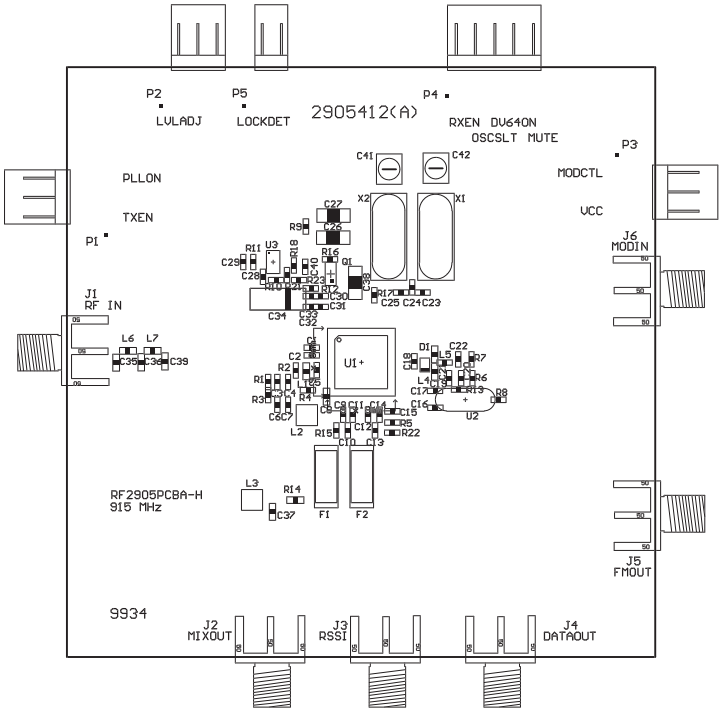


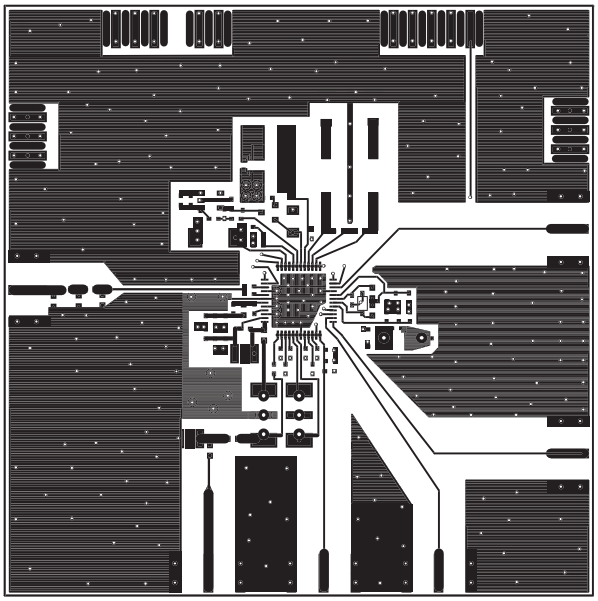
Board	C35 (pF)	L6 (nH)	L7 (nH)	C39 (pF)	L1 (nH)	C5 (pF)	C18 (pF)	L4,L5(nH)	R9 (kΩ)	X1 (MHz)	X2 (MHz)
L (433MHz)	8	22	22	8	47	35	3	27	2.4	6.78	6.612
M (868MHz)	4	8.2	Jumper	N/C	10	10	5	4.7	2.7	13.577344	13.410156
H (915MHz)	4	8.2	Jumper	N/C	10	10	5	4.7	2.7	7.15909	7.07549

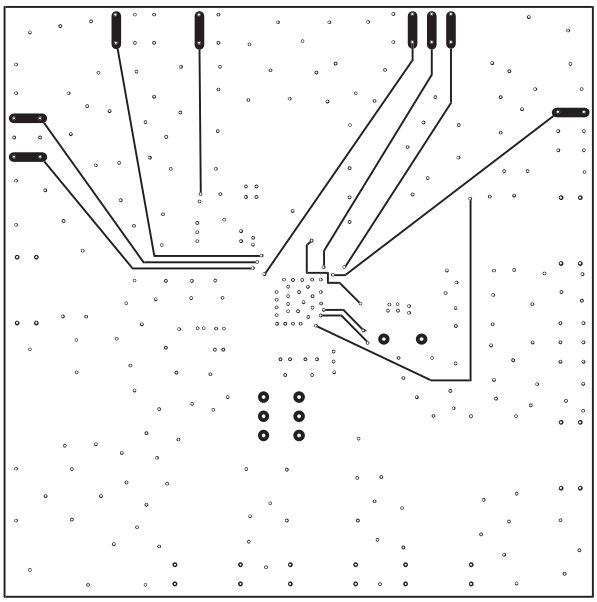
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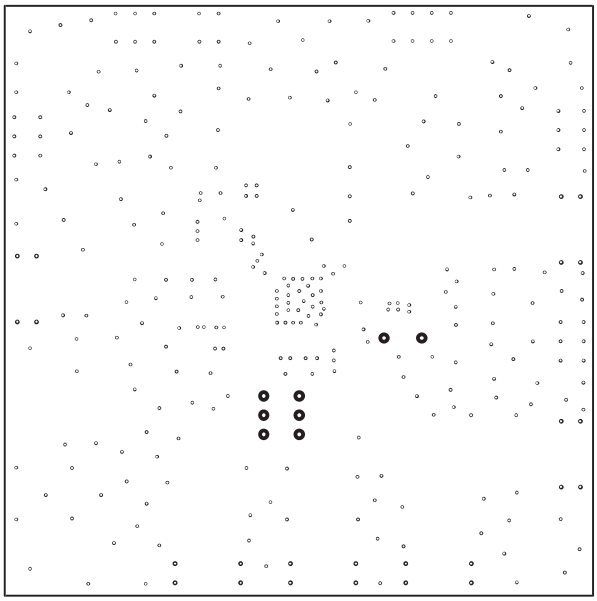
Evaluation Board Layout
Board Size 3.05” x 3.05”

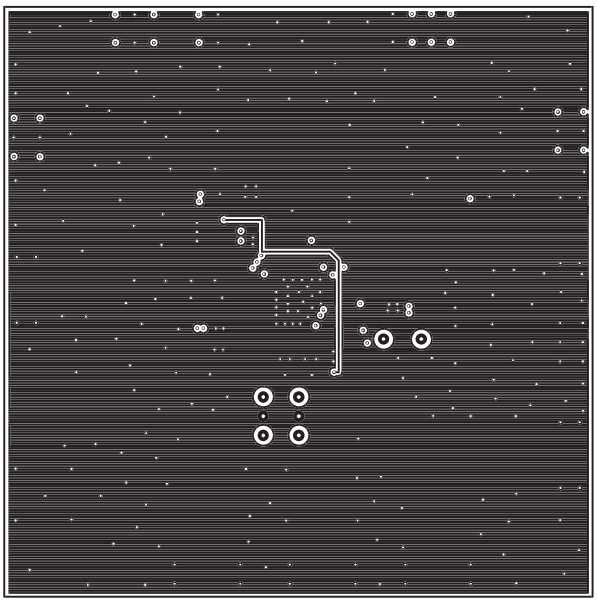
Board Thickness 0.031”, Board Material FR-4, Multi-Layer
(Same board layout is used for the -L, -M, and -H versions.)



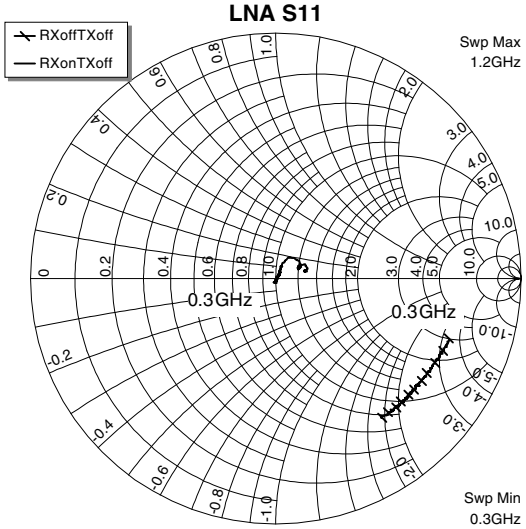




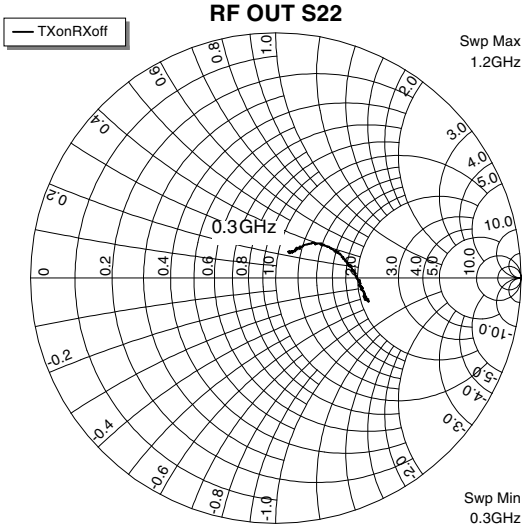




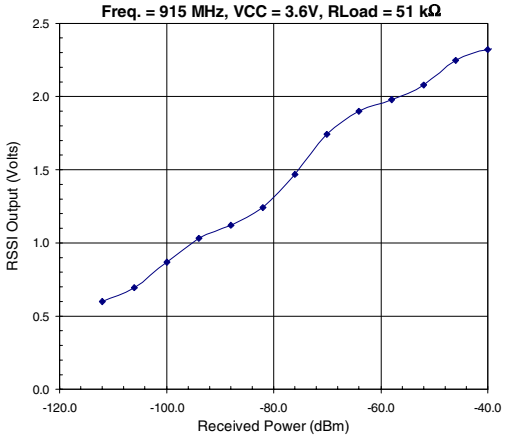
LNA S11



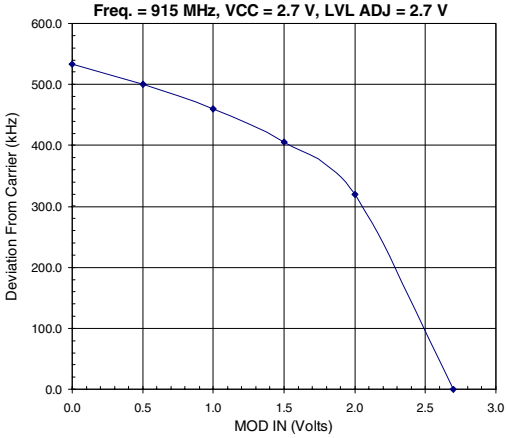
RF OUT S22



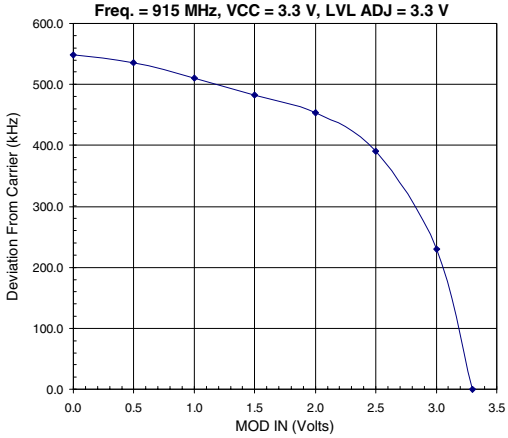
RSSI
Freq. = 915 MHz, VCC = 3.6V, RLoad = 51 kΩ



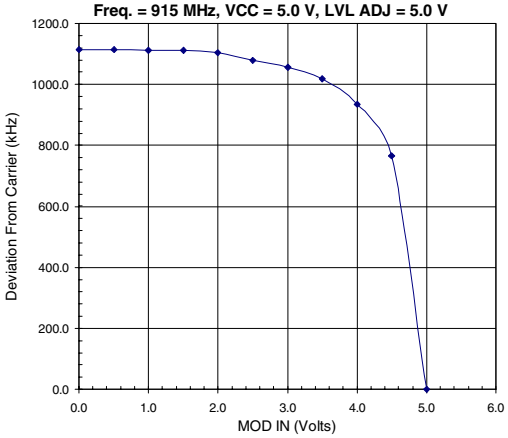
Modulation Deviation
Freq. = 915 MHz, VCC = 2.7 V, LVL ADJ = 2.7 V



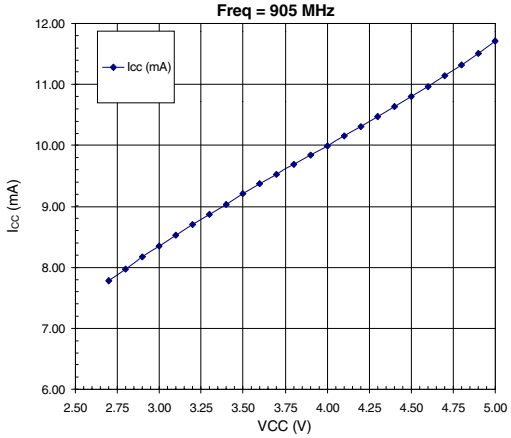
Modulation Deviation
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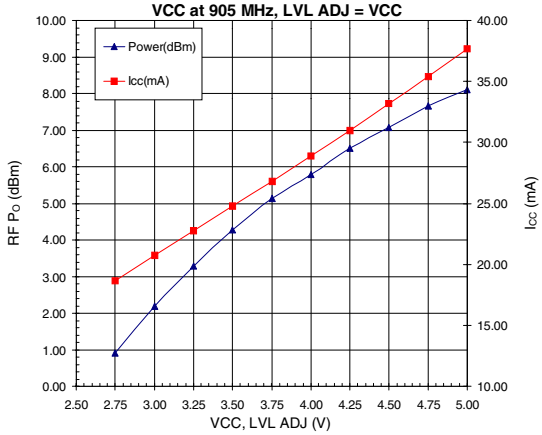
Modulation Deviation
Freq. = 915 MHz, VCC = 5.0 V, LVL ADJ = 5.0 V



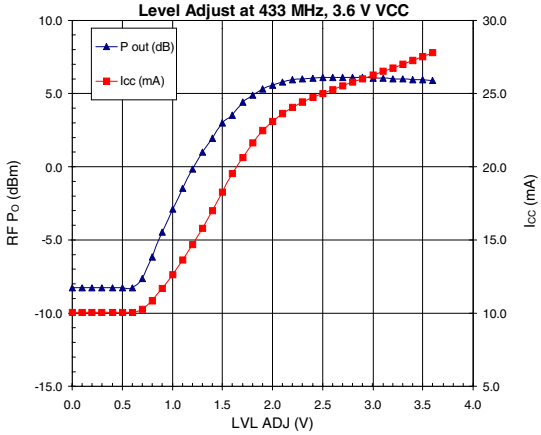
RX Mode Current versus VCC
Freq = 905 MHz



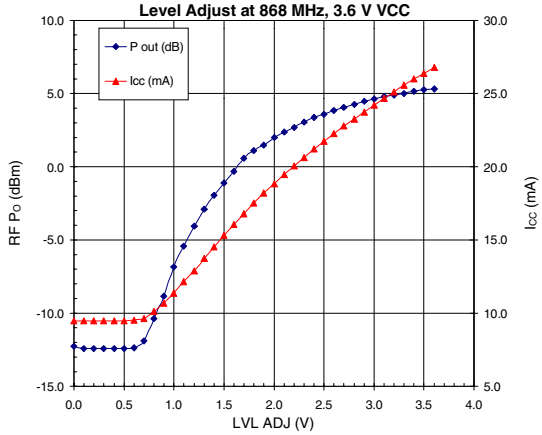
TX Power Output and I_{CC} versus
VCC at 905 MHz, LVL ADJ = VCC



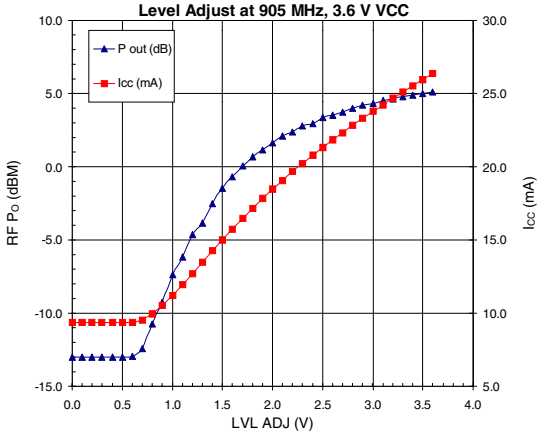
TX Power Output and I_{CC} versus
Level Adjust at 433 MHz, 3.6 V VCC



TX Power Output and I_{CC} versus
Level Adjust at 868 MHz, 3.6 V VCC



TX Power Output and I_{CC} versus
Level Adjust at 905 MHz, 3.6 V VCC



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RF2907

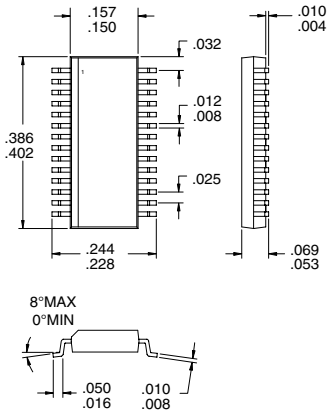
433/868/915MHZ AM/ASK/OOK TRANSCEIVER

Typical Applications

- Battery Powered AM Transceivers
- 915MHz ISM Applications
- 433MHz and 868MHz ISM Applications
- Wireless Data Transmitter/Receiver
- Wireless Security Systems
- Wireless Meter Reading

Product Description

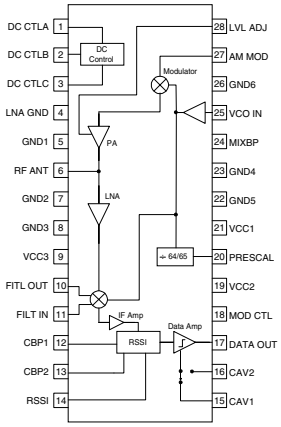
The RF2907 is a complete AM/ASK transceiver. This highly integrated device operates at frequencies in the 300MHz to 1500MHz range. This transceiver features an AM modulator/transmitter with analog-variable output power up to +7dBm, a dual modulus divide-by 64/65 prescaler, and a complete AM receiver. There is also a sleep mode provided so the device may be turned off to save battery life. Dual time constant control on the demodulator allows for faster settling for wake up mode. The RF2501or RF2502 VCO ICs are available to provide a high isolation, low cost LO source for the RF2907.



Package Style: SSOP-28

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Power Down Feature
- AM Modulation/Demodulation Capability
- Integrated 64/65 Dual Modulus Prescaler
- +7dBm Transmitter Output Power
- 7dB Typical Receiver Noise Figure
- Micropower Operation

Ordering Information

RF2907	433/868/915MHz AM/ASK/OOK Transceiver
RF2907 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

11 TRANSCEIVERS

RF2907

Absolute Maximum Ratings

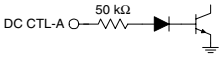
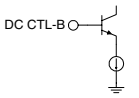
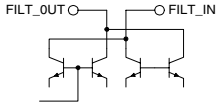
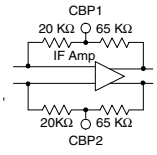
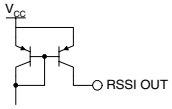
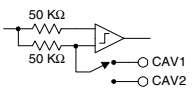
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5	V
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

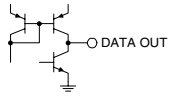
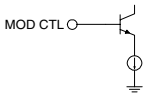
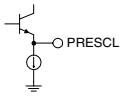
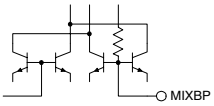
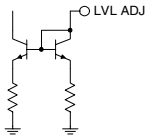
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
General Characteristics					T=25°C, V_{CC}=3.6V, LO=913.4MHz, Freq=915MHz
RX/TX Frequency Range	300	433, 868, 915	1500	MHz	
Modulation Type		ASK,AM			
Receiver RF Characteristics					
Conversion Gain		24		dB	
Cascaded Noise Figure		7		dB	
Cascaded IP3		-30		dBm	
RX Input VSWR		1.5:1			
LO Leakage (@RF_RX)			-50	dBm	
LO Input Level (VCO_IN pin)		-7		dBm	
Receiver IF Characteristics					
IF Bandwidth (-3dB)		3		MHz	
Sensitivity		-97		dBm	10^{-3} BER, 2kbps data rate
RSSI Dymanic Range	60			dB	
Data Out Bandwidth		1		MHz	
Data Output V_{OH}	V_{CC}-0.3			V	Z_{LOAD}=1MΩ||3pF
Data Output V_{OL}			0.3	V	Z_{LOAD}=1MΩ||3pF
Transmitter RF Characteristics					
TX Output Power	4	7		dBm	
TX Output Power Level Adjust Range	10			dB	
Modulation Rate			1	MHz	
TX Output VSWR		1.5:1			
LO Input Level (VCO_IN)		-7		dB	
Prescalar Characteristics					
Prescaler Divide Ratio		64/65			
Output Voltage Swing		1.3		V_{PP}	Output Load=2.5kΩ
Power Supply					
Operating Voltage	2.7	3.6	5	V	
I_{CC}, RX Mode		11.5	13.5	mA	
I_{CC}, RX Lock Mode		9.5	11.5	mA	
I_{CC}, TX Mode		20		mA	Avg. current with 50% duty cycle, AM_MOD square wave 1-2.4V, TX out=+7dBm
I_{CC}, Sleep Mode			1	µA	

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Pin	Function	Description	Interface Schematic
1	DC CTLA	DC control pin. This control signal is used as described in the modes of operation table to control the operating mode of the IC.	
2	DC CTLB	Same as pin 1.	
3	DC CTLC	Same as pin 1.	See pin 2.
4	LNA GND	Ground connection for the LNA. Keep traces physically short and connect immediately to ground plane for best performance.	
5	GND1	Ground connection for the RF mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
6	RF ANT	RF input/output pin. Provides RF input to the LNA when the receiver is enabled and the transmitter is disabled. Provides RF output from the PA when the receiver is disabled and the transmitter is enabled. This pin requires an external DC blocking capacitor.	
7	GND2	Ground connection for the TX PA and receiver IF functions. Keep traces physically short and connect immediately to ground plane for best performance.	
8	GND3	Same as pin 7.	
9	VCC3	This pin supplies DC bias to the TX PA. Requires a bypass capacitor close to the pin for RF bypassing. Recommended values are 100pF for 915MHz and 220pF for 433MHz.	
10	FILT OUT	RF Mixer output. Pins 10 and 11 are open collector, complementary outputs. These pins must be connected to VCC through an inductor to provide DC bias for the mixer. The inductance at these pins should be parallel resonated with a resistor and a capacitor to form a band-limiting tank circuit (see application circuit). The tank resistance will set the Q of the filter and the gain of the mixer.	
11	FILT IN	Same as pin 10.	See pin 10.
12	CBP1	Low-frequency bypass that allows the use of DC feedback to control the bias point of the IF amps.	
13	CBP2	Same as pin 12.	See pin 12.
14	RSSI	Output of the RSSI detector. The RSSI outputs a current, so an external RC circuit defines the output characteristic of the RSSI. Output current increases with increasing signal strength. This output is also used to provide the demodulated AM signal.	
15	CAV1	Averaging capacitor for the single bit A/D converter. Recommended value allows the receiver to setup in 5ms and will receive data from 300bps to 3kbps. Values can be changed to optimize for various data rates and receiver settling times.	
16	CAV2	Averaging capacitor for the single bit A/D converter. Recommended value allows Receiver to setup in 2ms and will receive data from 9kbps to 20kbps.	See pin 15.

RF2907

Pin	Function	Description	Interface Schematic
17	DATA OUT	Output of the receiver. Expects a load of at least 1MΩ.	
18	MOD CTL	Control pin for the modulus of the prescaler. This is a digital control pin. Input high (V>2V) results in divide by 64, input low (V<1V) results in divide by 65.	
19	VCC2	This pin supplies DC bias to the Prescaler. Requires a bypass capacitor close to the pin for RF bypassing. Recommended values are 100pF for 915MHz and 220pF for 433MHz.	
20	PRESCL	Prescaler output pin. Output level is 1.3V_{PP} into 2.5kΩ load. The parasitic capacitance on this pin should be minimized.	
21	VCC1	This pin supplies DC bias to the receiver electronics. Requires a bypass capacitor close to the pin for RF bypassing. Recommended values are 100pF for 915MHz and 220pF for 433MHz.	
22	GND5	Ground connection for the TX PA buffer. Keep traces physically short and connect immediately to ground plane for best performance.	
23	GND4	Ground connection for the prescaler. Keep traces physically short and connect immediately to ground plane for best performance.	
24	MIXBP	This pin supplies DC bias and an AC ground to the Mixer. Requires a bypass capacitor close to the pin for RF bypassing. Recommended values are 100pF for 915MHz and 220pF for 433MHz.	
25	VCO IN	50Ω input for LO signal, needs an external coupling capacitor. Input LO power should be about -12dBm.	
26	GND6	Ground connection for the LO buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
27	AM MOD	Data input for the transmitter. High impedance (Z_{IN}>40kΩ) pin. Characteristics are summarized in the performance summary.	
28	LVL ADJ	Transmitter level adjust control pin. Analog voltage control yields a minimum of 10dB transmitter output level control. Increasing voltage causes decreasing output power. Maximum output power is achieved with input voltage of 0V.	

Operation Mode	DC CTLA	DC CTLB	DC CTLC	Function
Sleep Mode	Low	Low	Low	Entire chip is powered down. Total current consumption is <1μA.
Transmit Mode	High	Low	Low	Transmitter, prescaler are on.
RX Data 1	High	High	Low	Receiver is on, prescaler is on. A/D converter uses CAV1 to set the output time constant.
RX Data 2	High	Low	High	Receiver, prescaler are on. A/D converter uses CAV2 to set the output time constant.
RX Lock	High	High	High	Mixer, prescaler are on. This mode allows time for a synthesizer loop to lock without spending current on the entire receiver.

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RF2907 Theory of Operation and Application Information

The RF2907 is an AM/ASK transceiver IC designed to provide a low cost, extremely low power half duplex link for a variety of applications. The different modes of operation allow the designer to develop systems based on burst data, time multiplexed, sleep/ awake, and/or receive and acknowledge architectures. These modes are controlled by three lines that are internally decoded according to descriptions in Table 1. The range of frequency and data rates make this a useful part for remote keyless entry systems, security systems, meter reading, remote monitoring, and much more.

The RF2907 is designed to interface with an external PLL IC and VCO. There is a dual modulus divide by 64/65 prescaler built-in which allows for a low cost, CMOS PLL IC such as the MC145158 from Motorola. Using the prescaler output minimizes the amount of High frequency signals that need to be routed on the PCB. The RF 2501 or RF2502 buffered VCO was designed to meet the LO requirements for the RF2907 by providing the added buffering to isolate the VCO from the AM modulator. There is a special mode of operation that allows you to power up the mixer and prescaler to let the synthesizer lock up and settle out before turning on the rest of the receiver. The length of time for this lock mode is dependent on the synthesizer design parameters.

The AM modulation is accomplished by modifying the bias current of the predriver amp. This varies the power delivered to the output amp in a linear fashion over a 20dB range. The modulator can also be driven by digital data, either driven directly which yields greater than 40dB of on-off ratio (OOK) or by limiting the voltage swing to produce a desired on-off ratio (ASK). A level adjust pin is also available on the transmitter to set the overall output power level. This is typically controlled by a current setting resistor or can actively be driven if a power ramp-up is desired.

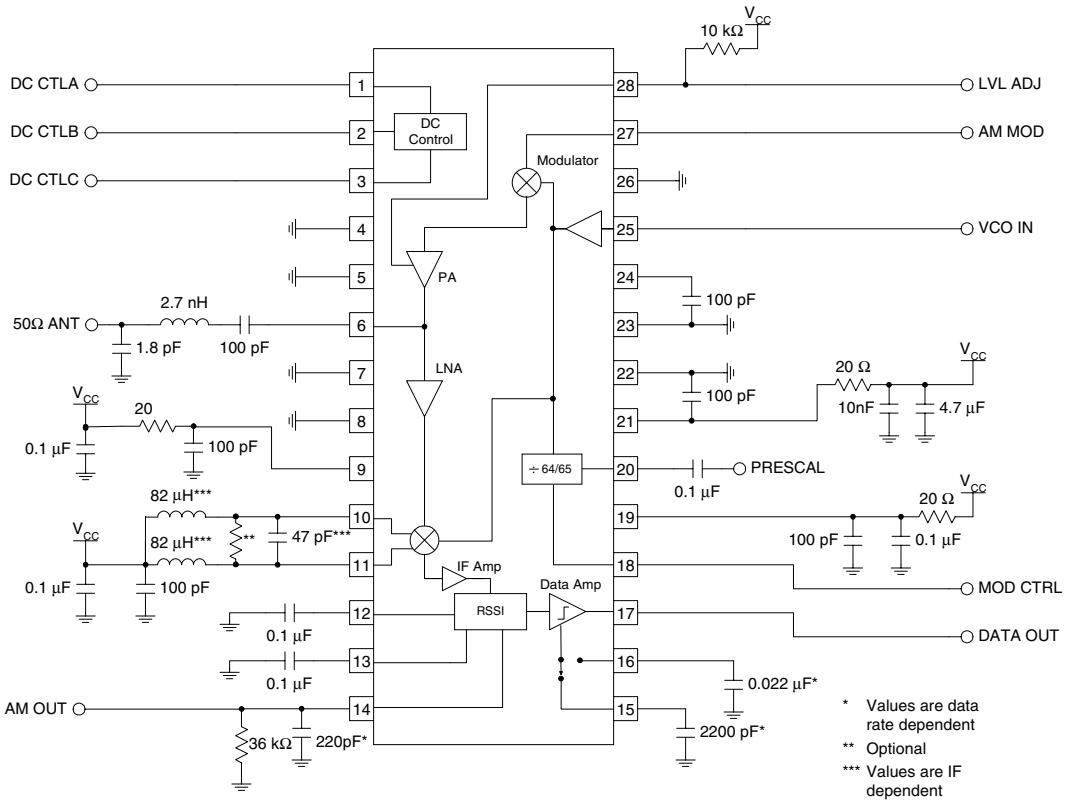
The PA output and LNA input are internally connected eliminating the need for a TX/RX switch. In transmit mode, the LNA is powered down and seen as a high impedance load on the node leaving just the external loading network on the PA. In receive mode, the opposite occurs with the PA seen as a high impedance and the LNA seen as a 50Ω load on the node. The control lines are decoded such that the PA and LNA are not on at the same time.

There are two available modes for receiving. These are based on the desire for the system to be in sleep mode for a period of time, then wake up and look for a desired transmission. Upon receipt of a valid preamble, the receiver switches into a receive data mode 2. Two charging capacitors are available for generating a reference voltage for the data comparator. A small value cap is used for the wake up and detection mode. Here, the reference voltage is generated fast to look for the preamble. If the preamble is not found, the receiver goes back to sleep. This will minimize the wake up time and extend battery life. When a valid preamble is received, the receiver can be switched into the second mode which would use a larger value cap for filtering out more of the modulation on the RSSI signal. This provides greater noise immunity in the receiver data.

To simplify the data recovery and reduce overall power and cost, this approach of filtering the RSSI data to produce a reference voltage was used. While the desired effects are worth while, there is a dependency on the DC value of the transmitted data stream that can produce undesired results. A long string of transmitted “1’s” will charge up the voltage on the filtering cap until the data comparator can no longer differentiate the received data. There are several ways to mitigate this problem. The most effective way is to use coding such as Manchester to guarantee a constant DC average. The cost of using such coding is in the increased data bandwidth. For low data rate systems this may be an advantage in that the size of the filtering cap need not be as big.

Spectral whitening or scrambling codes can be used to average out the DC value. These work well in terms of reducing the DC variations otherwise present in the data stream. These codes do not add to the required bandwidth but may need additional preambles or seeds to sync up on which can fractionally add to the transmission time dependent upon the coding overhead required.

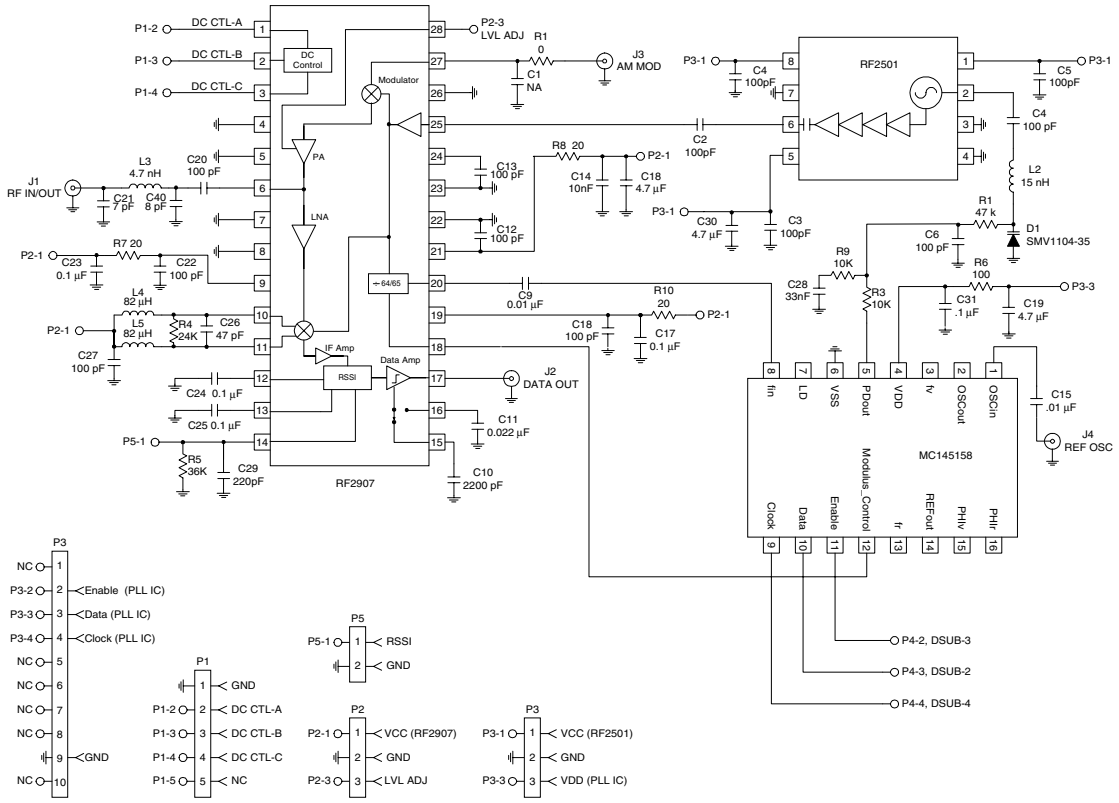
RF2907 Application Schematic For ASK Transceiver



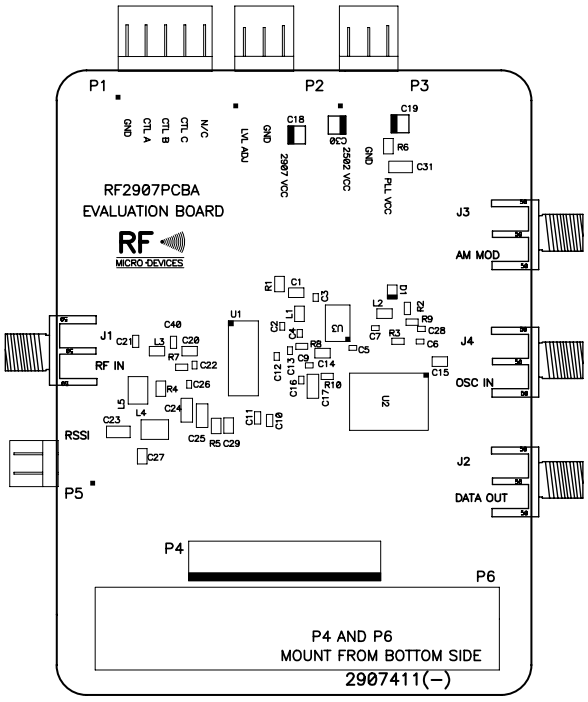
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Evaluation Board Schematics

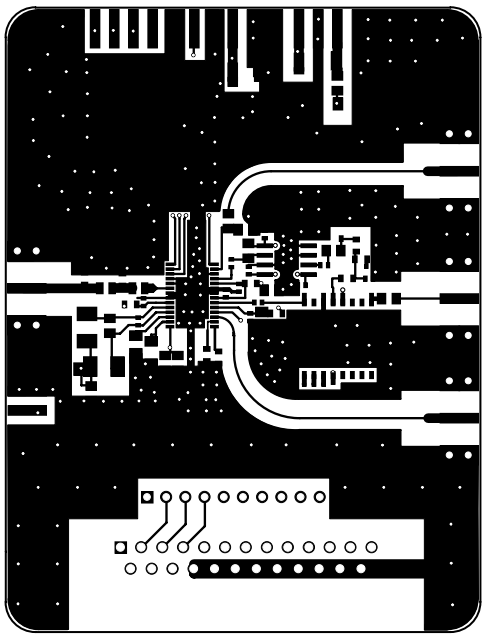
(Download Bill of Materials from www.rfmd.com.)



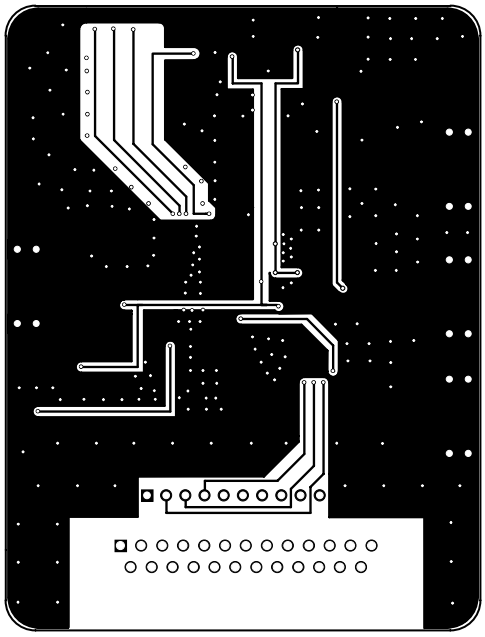
Evaluation Board Layout
2.472" x 3.242"
Assembly



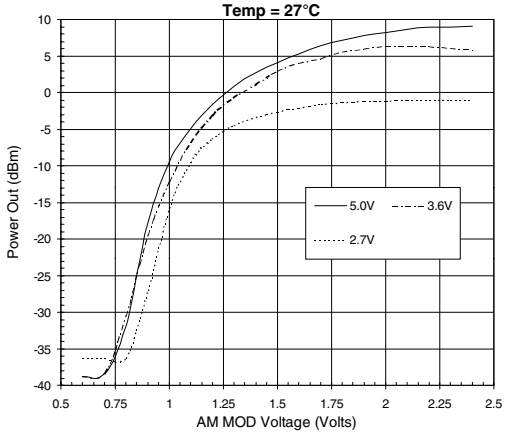
Evaluation Board Layout cont'd
Top Layer



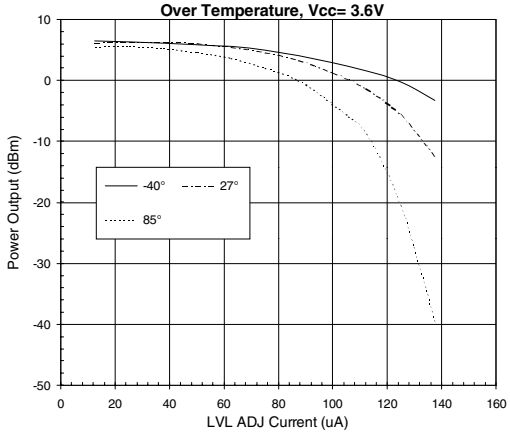
Mid layer



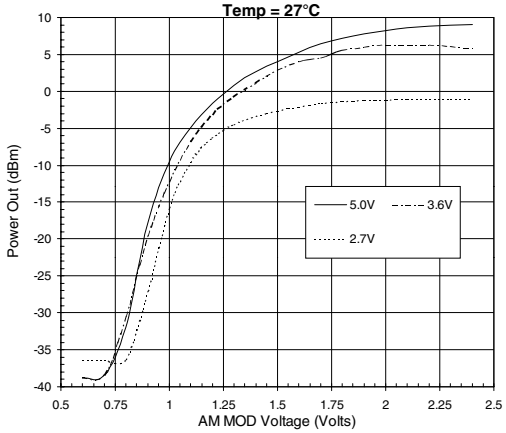
Output Power vs. AM MOD
Temp = 27°C



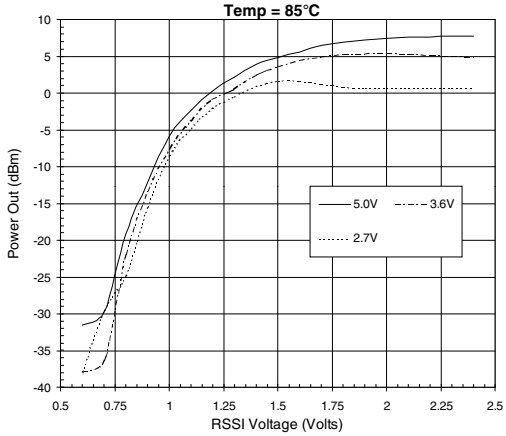
Power Output vs. Level Adjust
Over Temperature, Vcc= 3.6V



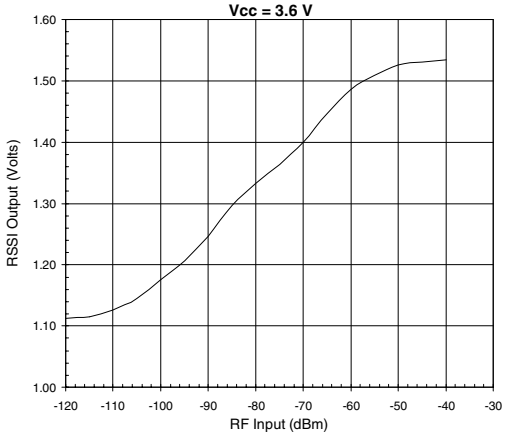
Output Power vs. AM MOD
Temp = 27°C



Output Power vs. AM MOD
Temp = 85°C



RSSI Output
Vcc = 3.6 V



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RF MICRO·DEVICES

Preliminary

RF2908

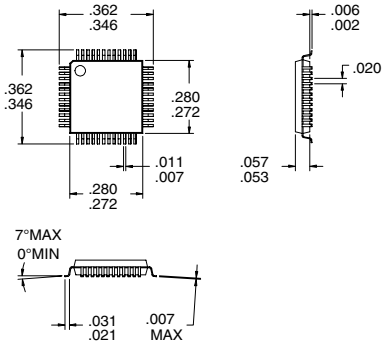
915MHZ SPREAD SPECTRUM RECEIVER WITH PLL FREQUENCY SYNTHESIZER

Typical Applications

- Digital Cordless Telephones
- Secure Communication Links
- Wireless LANs
- Inventory Tracking
- Wireless Security
- Battery Powered Applications

Product Description

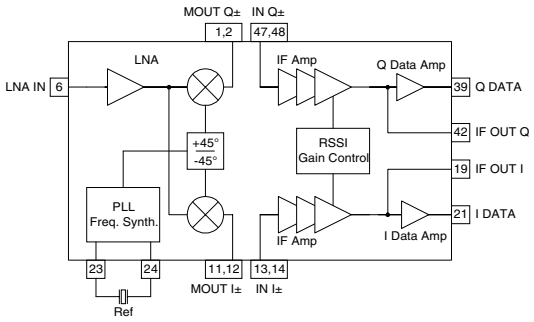
The RF2908 is a monolithic integrated circuit specifically designed for direct-sequence spread-spectrum systems operating in the 902MHz to 928MHz ISM band. The part includes a direct conversion receiver, quadrature demodulator, dual IF amplifiers with gain control and RSSI, on-chip programmable baseband filters, dual data comparators, and a serially programmable 86-channel PLL frequency synthesizer. Two cell or regulated three cell (3.6V maximum) battery applications are supported by the part. The part is also designed to operate in compliance with FCC Part 15.247. The device is provided in 48-lead plastic LQFP packaging.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Refer to the Detailed Functional Block Diagram for description of full functionality

Functional Block Diagram

Features

- FCC Part 15.247 Compliant
- Direct Conversion Receiver
- On-Chip 86 Channel Frequency Synthesizer
- On-Chip Selectable IF Bandwidths
- 2.7V to 3.6V Operation

Ordering Information

RF2908	915MHz Spread Spectrum Receiver with PLL Frequency Synthesizer

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+20	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		902 to 928		MHz	
Cascaded Voltage Gain		100		dB	
Cascaded Noise Figure		6.0	8.0	dB	
Cascaded Input IP_3		-12		dBm	High Gain
		+5.5		dBm	Low Gain
RX Sensitivity		-100		dBm	IF BW=960kHz, Freq=915MHz, S/N=8dB
LO Leakage		-65		dBm	At LNA IN
RSSI DC Output Range		0.35 to 3.1		V	R_{LOAD}=51kΩ
RSSI Sensitivity		30		mV/dB	
RSSI Dynamic Range	60	65		dB	
LNA and Mixer					
Operating Frequency Range		902 to 928		MHz	
Voltage Gain		22		dB	
Noise Figure		6.0	8.0	dB	
RF Input Impedance		50		Ω	
RF Input VSWR			2:1		
Input IP_3	-20	-12		dBm	At maximum gain. ATTN=LOW
		+5.5		dBm	At minimum gain. ATTN=HIGH
Quadrature Phase Balance		±3	±5	°	With expected LO amplitude and harmonic content.
Quadrature Amplitude Balance		±1		dB	
Mixer Output Impedance	150	200	250	Ω	Differential
DC Current Consumption	26	33	39	mA	Operating at a 3.3V supply voltage.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
IF and Data Amplifiers					
IF Frequency Range	Note 1		9.6	MHz	
Voltage Gain	77	80	83	dB	
Noise Figure		5		dB	At maximum gain setting
		35		dB	At minimum gain setting
Input IP3		-65		dBm	At maximum gain setting
		+2		dBm	At minimum gain setting
Output DC Offset		0	25	mV	
Gain Control Range	65	70		dB	
Gain Control Voltage Range	1.2		2.0	V	
Gain Control Sensitivity		-0.08		dB/mV	
VGA Output Voltage		500		mV_{PP}	
VGA DC Output Voltage		1.7		V	
Output P1dB	1	1.64		V_{PP}	Driving a 5kΩ load
RSSI Range		60		dB	At maximum gain setting
RSSI Output Voltage Compliance	55	0.5 to 2.4		V	Maximum RSSI is 2.5V or V_{CC}-0.3, whichever is less.
Input Impedance	1.5	2	2.5	kΩ	Differential
					Note 1. The lower cutoff frequency is a function of: a) input DC blocking cap size; b) DC feedback capacitor; and, c) gain setting. But, recommended component values will yield a cutoff of <10kHz.
Filters					
Characteristics		Five pole Bessel			Five pole Bessel internal LPF. Three pole external LPF.
Bandwidth		1, 2, 4, 8		MHz	Selectable from 1, 2, 4, and 8MHz. Refer to "IF Bandwidth Response" chart.
Passband Ripple			1	dB	
Group Delay			100	ns	At 8MHz, increasing as bandwidth decreases.
Ultimate Rejection	80	100		dB	
Data Amplifiers					
Voltage Gain		100		dB	
Bandwidth	10			MHz	
Rise and Fall Time		2	5	ns	
Logic High Output	V_{CC}-0.3V			V	Can sink/source 1mA and maintain these logic levels.
Logic Low Output			0.3	V	Can sink/source 1mA and maintain these logic levels.
PLL, Synthesizer, VCO and LO					
VCO Tuning Range		800 to 1200		MHz	
VCO Sensitivity	20	30	40	MHz/V	Determined by external resistor.
Charge Pump Current		100		μA	KPD=100μA/2π=0.0159ma/2π rad
Reference Frequency Crystal		9.6	20	MHz	
Reference Crystal Rs		60	80	Ω	
Phase Noise		-66		dBc/Hz	10kHz offset.
		-96		dBc/Hz	100kHz offset.
LO Output Level		-10		dBm	Into 100Ω differential load
Lock Time		1.5		ms	From sleep mode.
Step Size		300		kHz	86 channels in the 902MHz to 928MHz ISM band.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls "ON"	V_{CC}-0.3V		V_{CC}+0.3V	V	Voltage supplied to the input
Logical Controls "OFF"	0		0.3	V	Voltage supplied to the input
Control Input Impedance		>1		MΩ	
Turn On Time		1		ms	Reference Crystal=9.6MHz. Dependent on reference crystal. Higher frequencies reduce turn on/off times.
Turn Off Time		1		ms	Reference Crystal=9.6MHz. Dependent on reference crystal. Higher frequencies reduce turn on/off times.
RX to TX and TX to RX Time		100		µs	
Power Supply					
Voltage	2.7	3.3	3.6	V	
Current Consumption		50	62	mA	V_{CC}=3.3V; RX ENABL=HIGH; PLL ENABL=HIGH
		50		µA	V_{CC}=3.3V; Sleep Mode
		45	57	mA	V_{CC}=3.3V; RX ENABL=LOW; PLL ENABL=HIGH

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Pin	Function	Description	Interface Schematic
1	MOUT Q-	The complementary quadrature phase signal output from the front-end mixer. See pin 2.	
2	MOUT Q+	The quadrature phase signal output from the front-end mixer.	
3	MIX VCC	Supply voltage for the front-end quadrature mixers.	
4	MIX GND	Ground connection for the front-end quadrature mixers.	
5	LNA GND	Ground connection for the low noise amplifier (LNA).	
6	LNA IN	Input to the attenuator and LNA.	
7	SW GND	Ground connection for the input attenuator.	
8	LNA VCC	Supply voltage for the LNA.	
9	SW GND2	Ground connection for the input attenuator.	
10	ATTN	Input attenuator control point. When connected “high”, the attenuator adds 20dB of series attenuation. When connected “low”, the attenuator adds 0dB of series attenuation.	
11	MOUT I+	The in-phase signal output from the front-end mixer.	
12	MOUT I-	The complementary in-phase signal output from the front-end mixer. See pin 12.	
13	IN I+	Input for the in-phase IF channel.	
14	IN I-	Complementary input for the in-phase IF channel.	
15	GND2	Ground for VCC2.	
16	DCFB I	DC feedback capacitor for in-phase channel.	
17	VCC2	Power supply for VGA amplifier 3, differential to single-ended converter, and post filter.	
18	GND3	Ground for VCC3.	
19	IF OUT I	Analog signal IF output for in-phase channel.	
20	VCC3	Power supply for data amplifier.	
21	I DATA	Logic-level data output for the in-phase channel. This is a digital output signal obtained from the output of a Schmitt trigger.	
22	RSSI I	Received signal strength indicator for the in-phase channel.	
23	OSC B	Base connection point for external reference crystal. The reference crystal is connected between this pin and ground.	
24	OSC E	Emitter connection point for external reference crystal. Feedback capacitors are connected between this pin and ground.	
25	LE	Latches data entered into the serial port. Data is clocked into the latch on the rising edge of LE. See table and timing diagram.	
26	PLL CLK	PLL shift register clock. The rising edges of this clocking signal load in the serial data present at the PLL DATA input pin into the internal latch. See table and timing diagram.	
27	PLL DATA	Input data for loading the counters. Clocked, serial data at this port is presented to the shift register, then to the latch, and finally to the counter. Each clock transition sends a single bit to the on-board 7-bit shift register. The MSB is loaded first. See table and timing diagram.	
28	PLL GND	Ground connection for the PLL.	
29	PLLD VCC	Supply voltage for the PLL.	
30	LO OUT B	Complementary local oscillator output. See pin 33.	
31	RESNTR+	This port is used to supply DC voltage to the VCO as well as tune the center frequency of the VCO.	
32	RESNTR-	This is the complementary port to pin 31. Refer to pin 31.	
33	LO OUT	Local oscillator output.	
34	DO	Connection point for the loop filter.	

Pin	Function	Description	Interface Schematic
35	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL circuitry. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
36	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	
37	BW SEL2	Bandwidth select logic input. Pin 37 and pin 38 provide a two bit control word for the setting of the IF bandwidth. See Table1.	
38	BW SEL1	Bandwidth select logic input. Pin 37 and pin 38 provide a two bit control word for the setting of the IF bandwidth. See Table1.	
39	Q DATA	Logic-level data output for the quadrature channel. This is a digital output signal obtained from the output of a Schmitt trigger.	
40	RSSI Q	Received signal strength indicator for the quadrature channel.	
41	VREF	Gain control reference voltage.	
42	IF OUT Q	Analog signal IF output for quadrature channel.	
43	VGC	Gain control voltage.	
44	VCC1	Power supply for bias circuits and VGA amplifiers for both the in-phase and quadrature channels.	
45	DCFB Q	DC feedback capacitor for quadrature channel.	
46	GND1	Ground for VCC1 for both the in-phase and quadrature channels.	
47	IN Q-	Minus input for quadrature channel	
48	IN Q+	Plus input for quadrature channel	

Table 1: Bandwidth Selection Controls

BWSEL1	BWSEL2	IF_{-3dB} Frequency
0	0	1MHz
0	1	2MHz
1	0	4MHz
1	1	8MHz

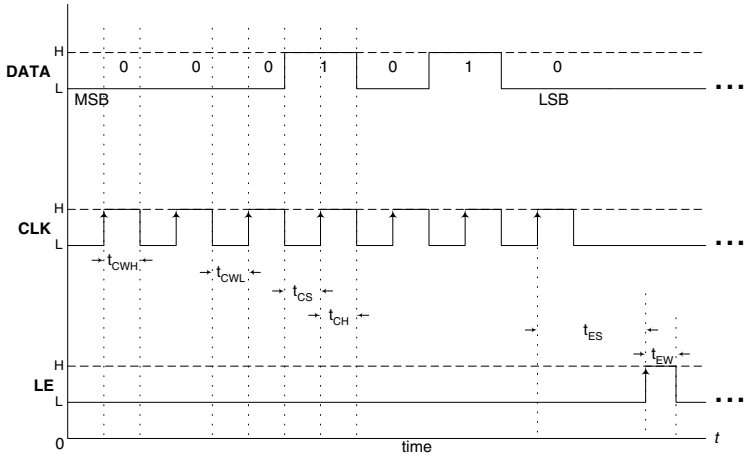
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Table 2: Channel Plan

Data	f, MHz	Data	f, MHz	Data	f, MHz	Data	f, MHz
0	902.4	22	909	44	915.6	66	922.2
1	*	23	909.3	45	915.9	67	922.5
2	903	24	909.6	46	916.2	68	922.8
3	903.3	25	909.9	47	916.5	69	923.1
4	903.6	26	910.2	48	916.8	70	923.4
5	903.9	27	910.5	49	917.1	71	923.7
6	904.2	28	910.8	50	917.4	72	924
7	904.5	29	911.1	51	917.7	73	924.3
8	904.8	30	911.4	52	918	74	924.6
9	905.1	31	911.7	53	918.3	75	924.9
10	905.4	32	912	54	918.6	76	925.2
11	905.7	33	912.3	55	918.9	77	925.5
12	906	34	912.6	56	919.2	78	925.8
13	906.3	35	912.9	57	919.5	79	926.1
14	906.6	36	913.2	58	919.8	80	926.4
15	906.9	37	913.5	59	920.1	81	926.7
16	907.2	38	913.8	60	920.4	82	927
17	907.5	39	914.1	61	920.7	83	927.3
18	907.8	40	914.4	62	921	84	927.6
19	908.1	41	914.7	63	921.3	85	927.9
20	908.4	42	915	64	921.6		
21	908.7	43	915.3	65	921.9		

*Data 1 is invalid.

Timing Diagram



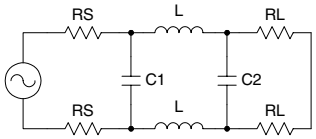
Minimum Times:
t_{CWH} = 143 ns
t_{CWL} = 143 ns
t_{EW} = 74 ns
t_{ES} = 143 ns
t_{CS} = 36 ns
t_{CH} = 36 ns

Example: Load Sequence for Channel #10 (905.4 MHz)
Decimal 10 = 0 0 0 1 0 1 0 Binary
MSB LSB

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Differential Filter Design Information

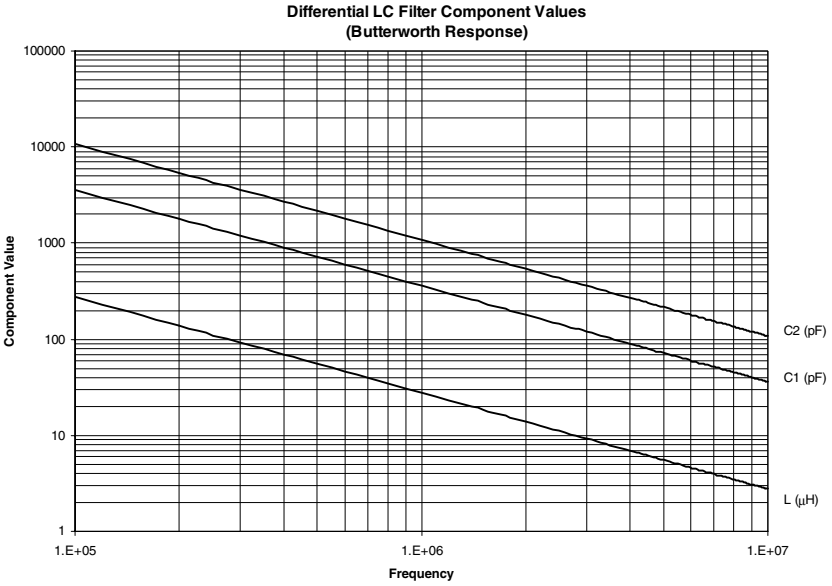
Butterworth Response



$$C1 = \frac{C1bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; C2 = \frac{C2bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; L = \frac{Lbw \cdot RL \cdot 10^{6}}{2 \cdot \pi \cdot fc}$$

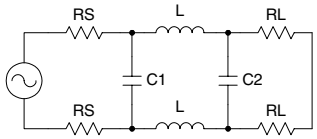
$$C1bw = 4.5325; C2bw = 13.5691; Lbw = 0.1743$$

$$RS = 125; RL = 1000; \frac{RS}{RL} = 0.125$$



Differential Filter Design Information (Cont.)

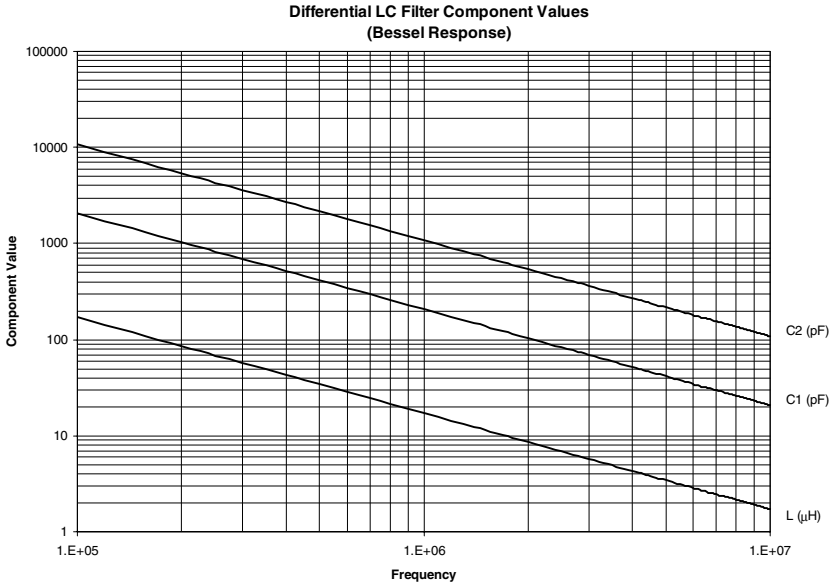
Bessel Response



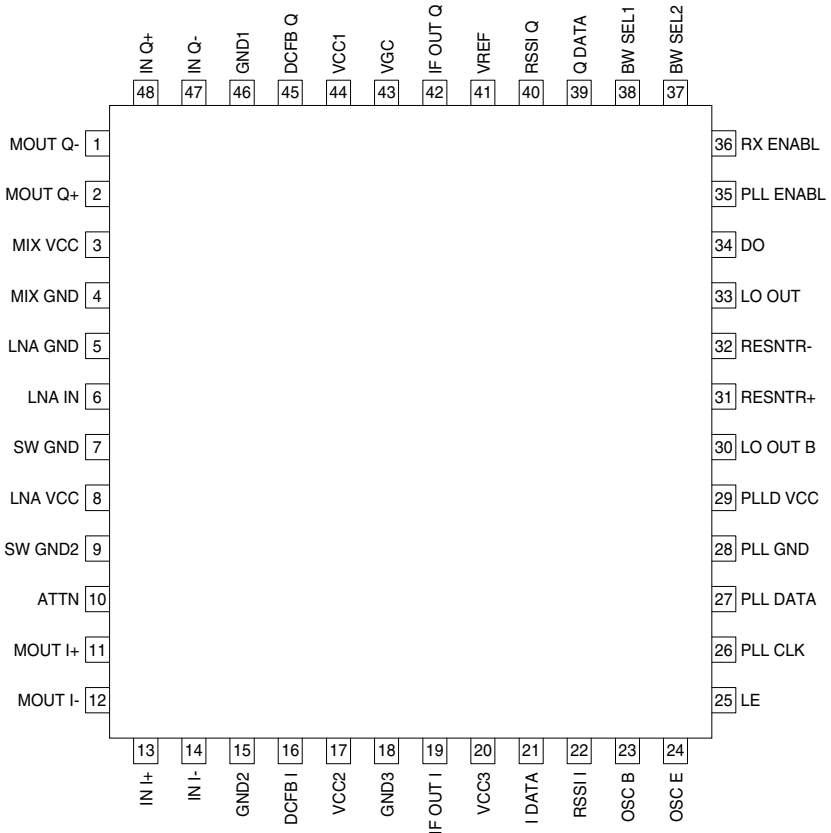
$$C1 = \frac{C1bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; C2 = \frac{C2bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; L = \frac{Lbw \cdot RL \cdot 10^{6}}{2 \cdot \pi \cdot fc}$$

$$C1bw = 2.6163; C2bw = 13.6373; Lbw = 0.1083$$

$$RS = 125; RL = 1000; \frac{RS}{RL} = 0.125$$



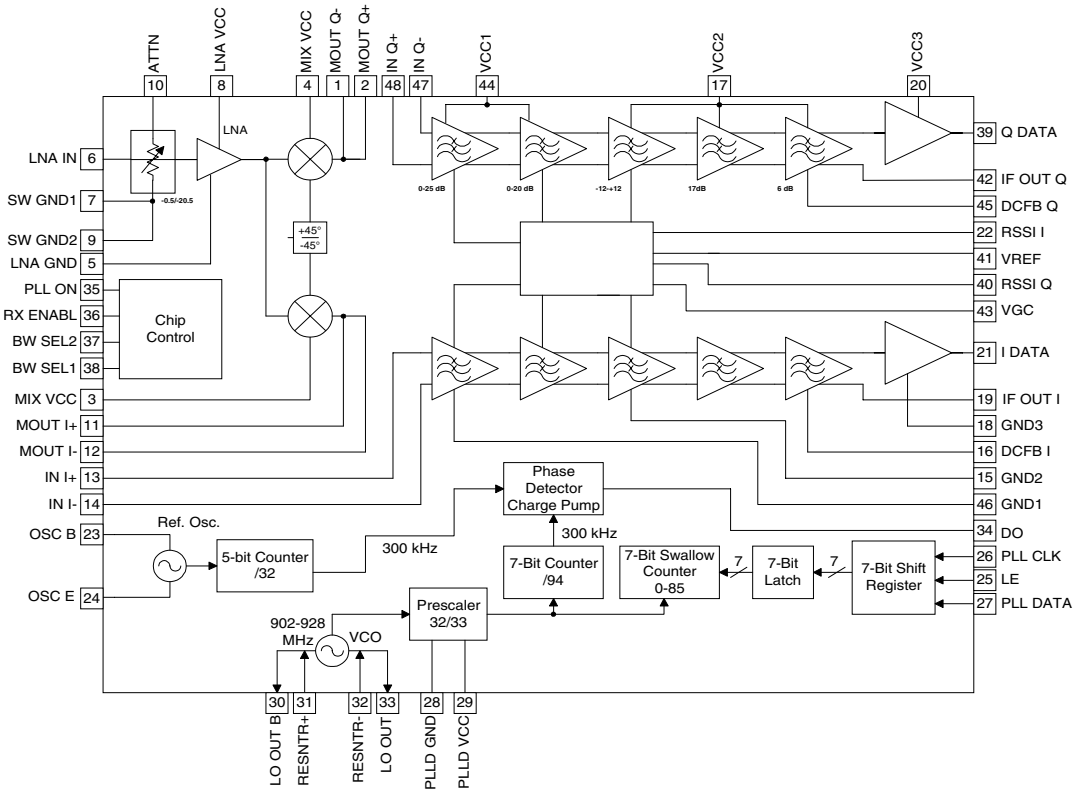
Pin Out



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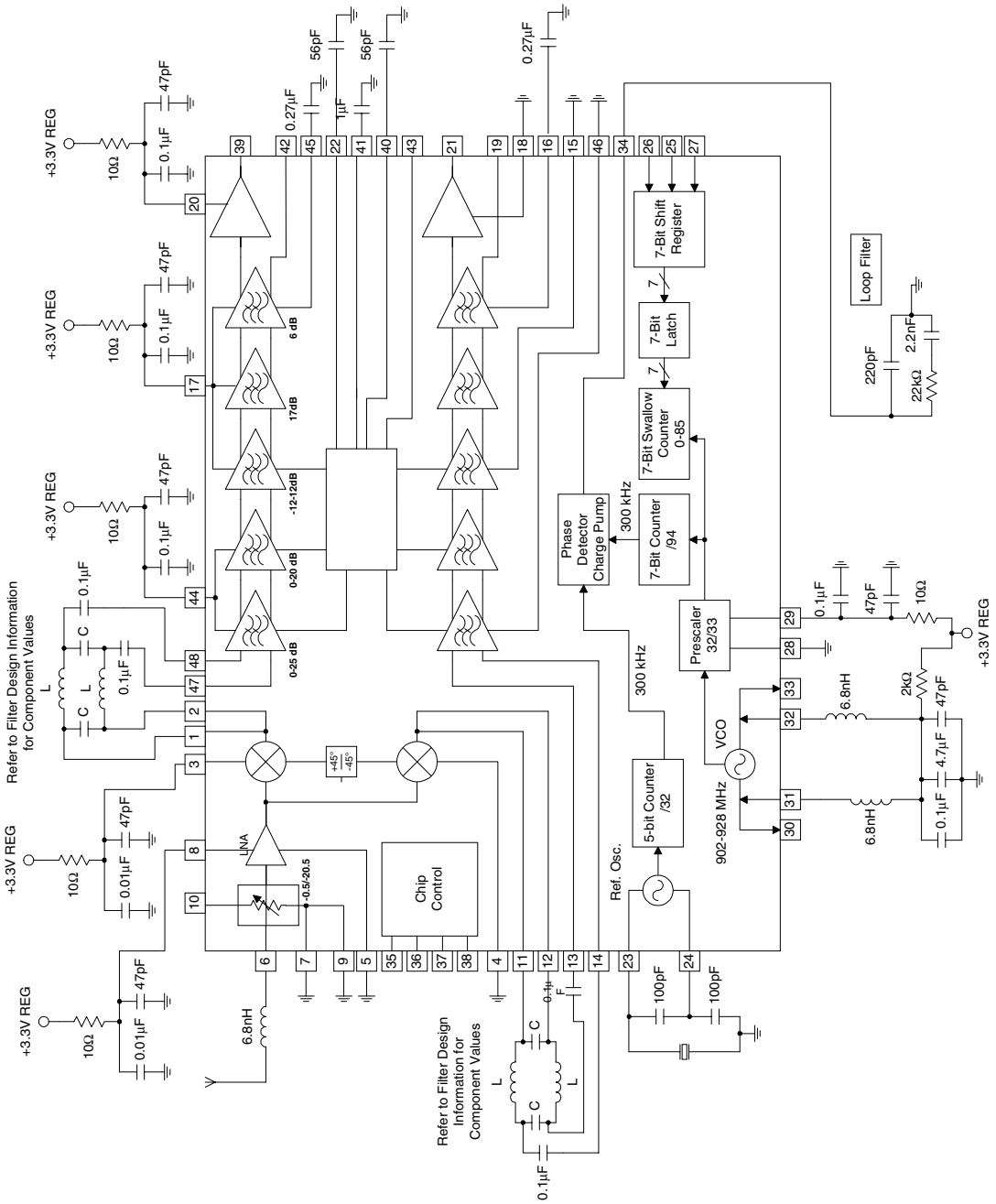
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Detailed Functional Block Diagram



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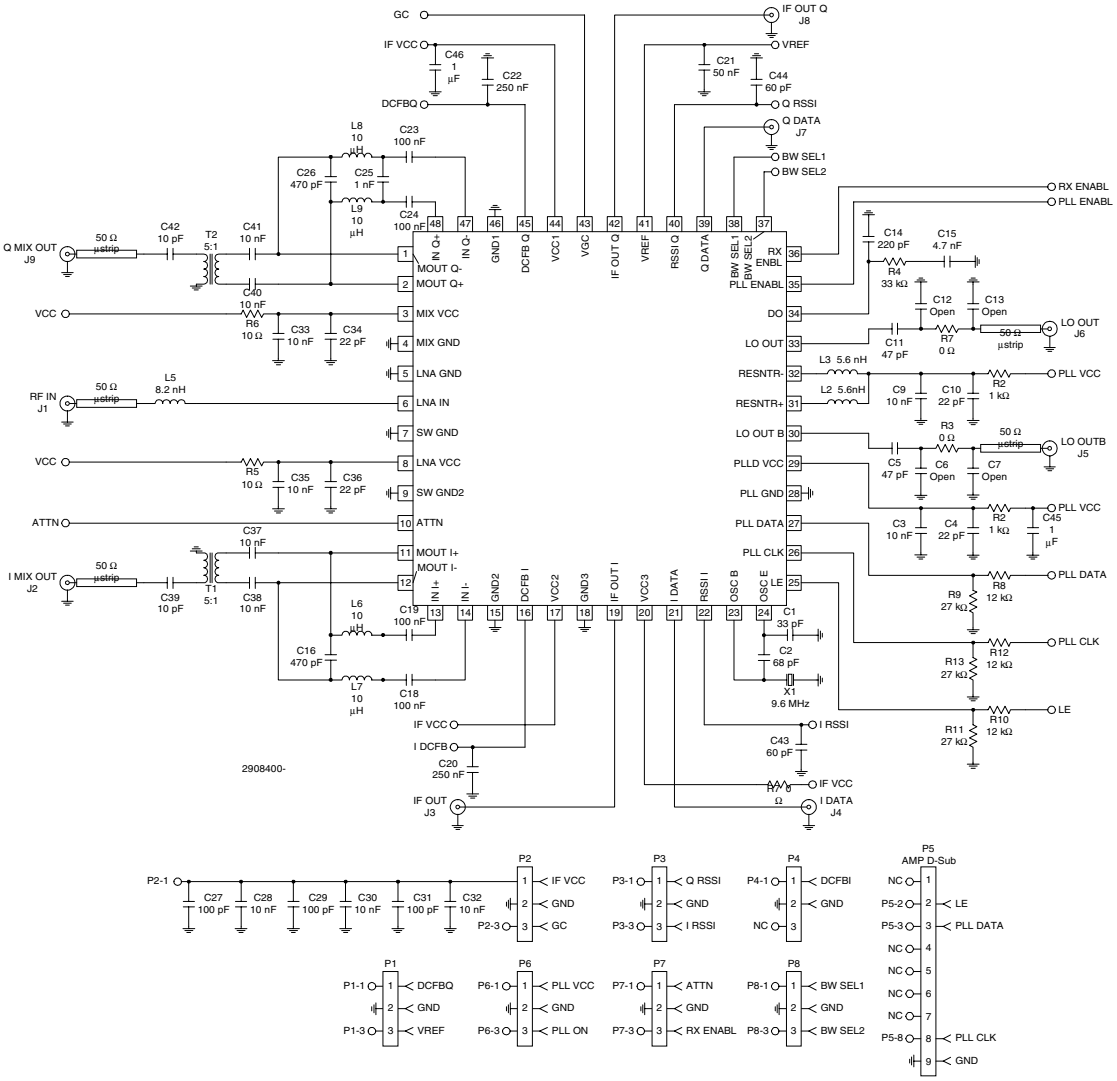
Application Schematic
915MHz



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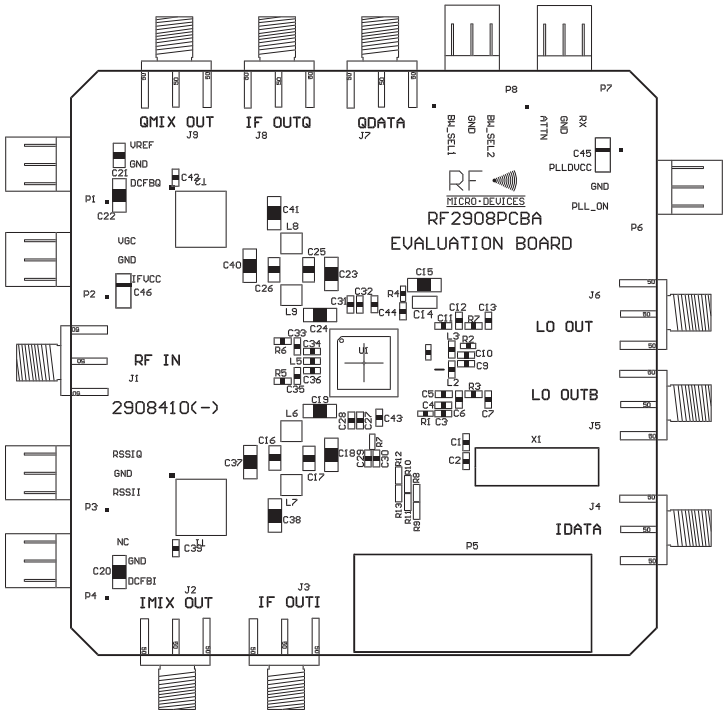
Evaluation Board Schematic

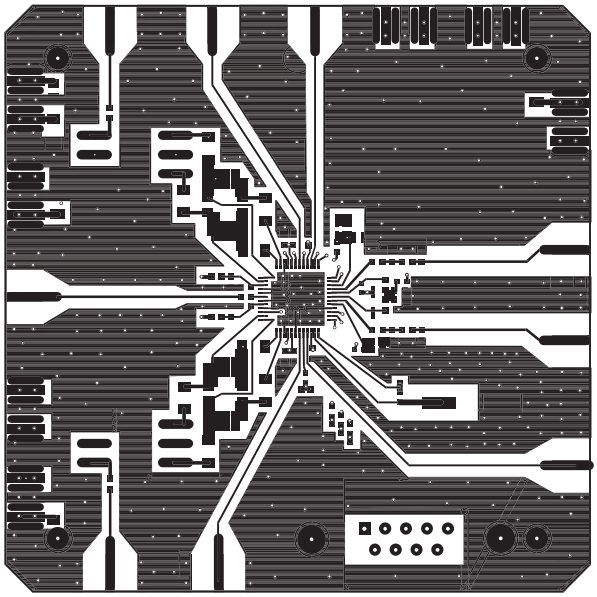
(Download Bill of Materials from www.rfmd.com.)



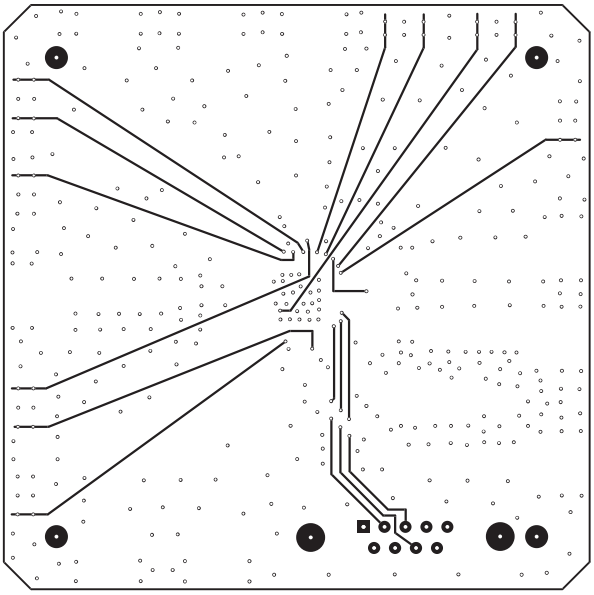
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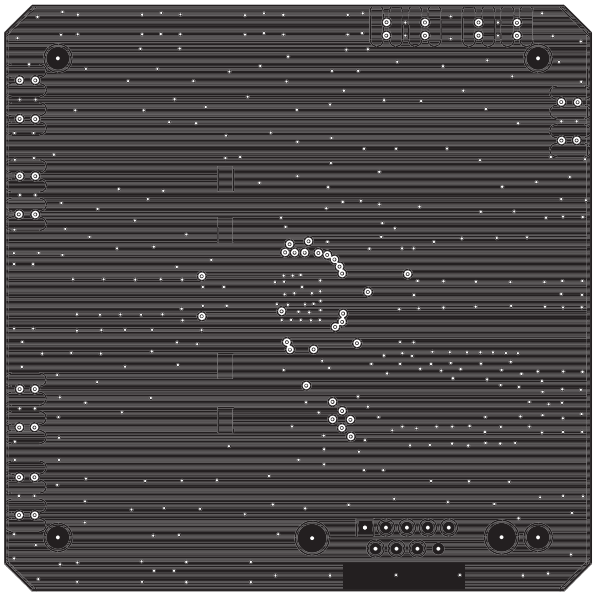
Evaluation Board Layout
Board Size 3.050” x 3.050”



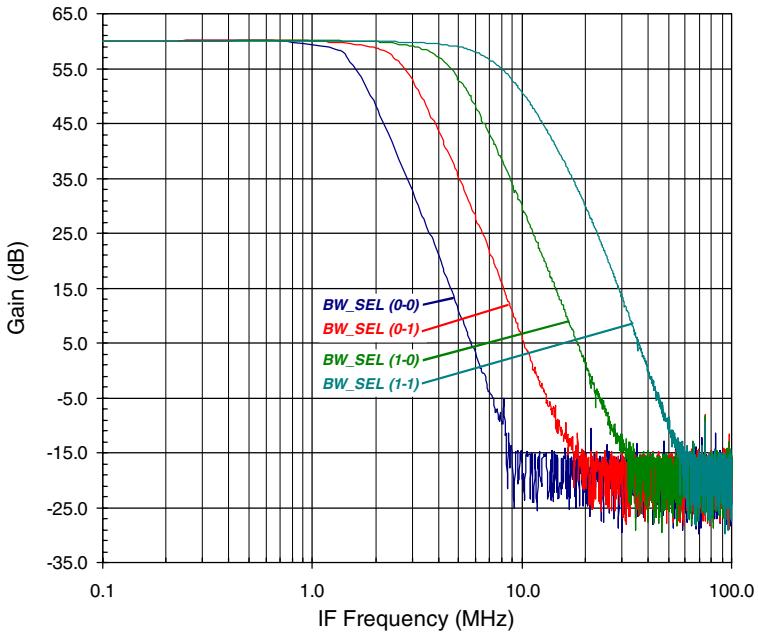


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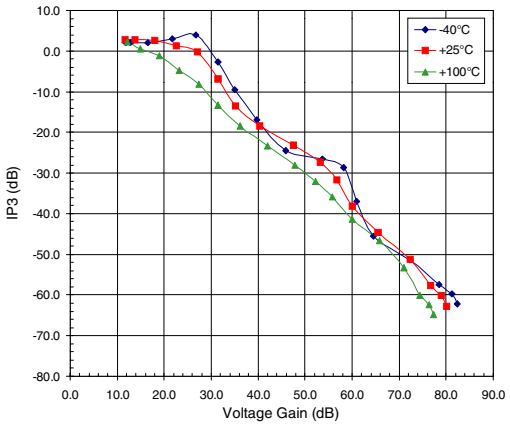




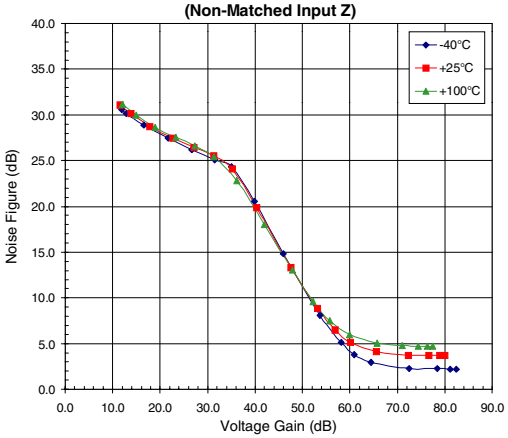
RF2908 IF Bandwidth Response



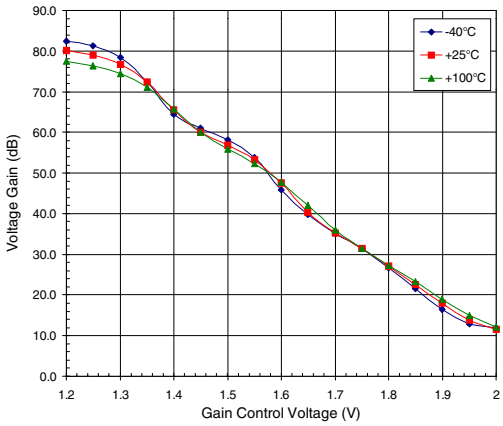
IIP3 versus Voltage Gain



Noise Figure versus Voltage Gain (Non-Matched Input Z)



Voltage Gain versus Gain Control Voltage



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RF MICRO·DEVICES

Preliminary

RF2909

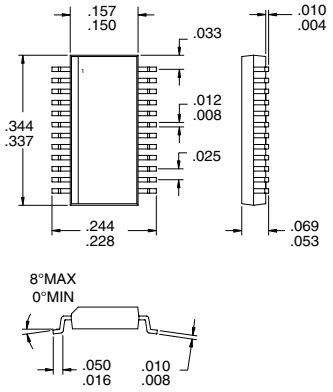
3V 915MHZ SPREAD-SPECTRUM TRANSMITTER IC

Typical Applications

- Direct Sequence Spread Spectrum
- Spread Spectrum Cordless Phones
- Portable Battery Powered Equipment
- GMSK, QPSK, DQPSK, QAM Modulation
- 915MHz ISM Applications

Product Description

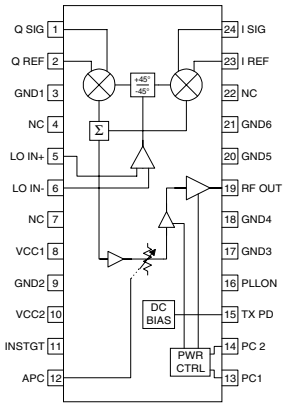
The RF2909 is a monolithic integrated transmitter IC capable of universal direct modulation. The quadrature modulator allows for a variety of modulation formats and compound carriers. The transmitter has two power control modes. Two inputs can be controlled digitally for stepping output power 1mW, 10mW, or 70mW output power. Or, the output level can be adjusted by an analog input from 1mW to 80mW. The quadrature mixers have differential inputs, and are internally biased; a DC blocking capacitor is required if external DC levels are present. The LO is split with a passive network tuned for 915MHz.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 2.7V to 5V Power Supply
- 1mW, 10mW, 70mW Digital Output Power
- 20dB Analog Power Control Range
- Excellent Phase & Amplitude Balance
- Compatible with the RF2908

Ordering Information

RF2909	3V 915MHz Spread-Spectrum Transmitter IC
RF2909 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

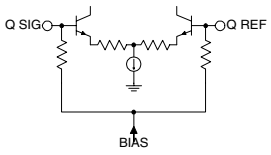
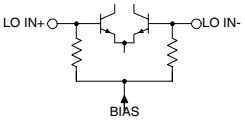
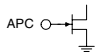
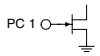
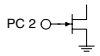
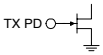
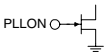
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input (LO IN)					T=25°C, V_{DD}=3.3V
Frequency Range	100	902-928	1100	MHz	Phase shift optimized for 915MHz
Power Level		-10		dBm	Differential
Input Impedance		50		Ω	915MHz
Modulation Input					
Frequency Range	DC	10	500	MHz	50Ω source, I,Q=500mV_{p-p}
Reference Voltage (V_{REF})		1.7		V	
Modulation for P_{OUT} Power (I & Q)		500		mV_p	Differential, 1V_p single ended
Maximum Modulation (I & Q)		1		V_p	Differential, 1.5Vp single ended
Quadrature Phase Error		3	5	°	
I/Q Amplitude Imbalance		.35		db	
Input Impedance		3		kΩ	Differential
RF Output					V_{DD}=3.3V, LO power=-10dBm, LO frequency=915MHz, SSB, I/Q=1V_{PP} sine wave, 100KHz
Digital Output Power		1, 10, 70		mW	See Table I for control logic
Output Impedance		50		Ω	
Output VSWR			1.5:1		With external matching (see app. schematic)
Second Harmonic Output		-25		dBc	
Other Harmonics Output		-30		dBc	
Sideband Suppression		30		dB	P_{OUT}=10mW
Carrier Suppression		27		dB	Modulation DC offset can be externally adjusted for optimum suppression. Carrier suppression is then typically better than 40dB.
Output Level Control					
Analog Power Control Range	20			dB	
Analog Power Control Voltage (APC)	0		3.6	V	Input voltage to pin 12 must be less than 3.6V or V_{CC} (whichever is less).
Analog Power Control Input Current			1	µA	
Analog Power Output		80		mW	V_{APC}=2.8V, PC1="0", PC2="0"
Digital Power Output, High		70		mW	APC=0V, PC 1="0", PC 2="1"
Digital Power Output, Med		10		mW	APC=0V, PC 1="1", PC 2="0"
Digital Power Output, Low		1		mW	APC=0V, PC 1="0", PC 2="0"
PC 1/PC 2 "ON"			1		Threshold Voltage
PC 1/PC 2 "OFF"	2				Threshold Voltage
Standby Mode					
Turn On/Off Time		0.15	1	µS	
Power Down "ON"	2			V	Threshold voltage; Part is turned "ON"
Power Down "OFF"			1	V	Threshold voltage; Part is turned "OFF"

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Voltage		3.3		V	Specifications
	2.7		5.0	V	Operating limits
Current		175	200	mA	Total, Digital High Power, V_{APC}, V_{PC1}=0V, V_{PC2}=V_{CC}
		45	60		Total, Digital Medium Power, V_{APC}, V_{PC2}=0V, V_{PC1}=V_{CC}
		30	40	mA	Total, Digital Low Power, V_{APC}, V_{PC1}, V_{PC2}=0V
		130	180	mA	Total, Linear Power, V_{APC}=2.8V, V_{PC1}, V_{PC2}=0V
		1.5	5	mA	PLL Buffer amp on.
			1	µA	Standby mode

Pin	Function	Description	Interface Schematic
1	Q SIG	Baseband input to the Q mixer. A DC bias of approximately 1.7V is present at this pin.A DC blocking capacitor is needed if the signal has a different DC level. Maximum output power is obtained when the input signal has a peak-to-peak amplitude of 1V. The input impedance of this pin is 3kΩ. The REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven deferentially to increase conversion gain.	
2	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3 kΩ.	See pin 1.
3	GND 1	Ground connection for the modulator circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
4	NC		
5	LO IN+	Balanced LO Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The balanced input impedance is 100Ω. The single-ended input impedance is 50Ω.	
6	LO IN-	Same as pin 4, except complementary input.	See pin 5.
7	NC		
8	VCC1	This pin is used to supply V_{cc} to the modulator circuits. A RF bypass capacitor should be connected directly to this and ground.	
9	GND2	Ground connection. This pin is used for RF ground of the power control circuitry and the PA driver amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
10	VCC2	This pin is used to supply V_{cc} to the power control and pre amp circuitry. A RF bypass capacitor should be connected directly to this and ground.	
11	INSTGT	Interstage bias point between pre amp and power amp. This pin should be pulled up to V_{cc} with an 8.2nH inductor for 915MHz.	See pin 18.
12	APC	Analog power control input. This pin can be used as a linear power output control with a range of 20 dB. Maximum output power is achieved when APC is high. APC is"wire-or'd" with the digital controls, therefore should be low when using the digital control. The DC input voltage to the pin should always be less than 3.6V.	
13	PC 1	This digital power control input sets the medium current and power output, 10mW. It is "wire-or'd" with APC and PC 2 and can be overcome by either. Therefore, APC and PC 2 must be low to use this setting.	
14	PC 2	This digital power control input set the high current and power output, 100mW. It is "wire-or'd" with APC and PC 1 and can override both of those controls. Therefore, PC 2 must be low to use other settings.	
15	TX PD	Enables all of the IC except for the LO buffer when > 2V.	
16	PLLON	Enables the LO buffer amp when > 2V.This can be switched on and off independently of the rest of the IC. This amp draws 1.5mA typically.This can be used to minimize load pulling of the VCO when the transmitter is turned on. Buffer amp is off when < 1V.	
17	GND3	Ground connection for RF Power Amp. Keep traces physically short and connect immediately to ground plane for best performance.	
18	GND4	Same as pin16.	

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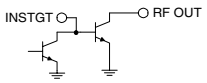
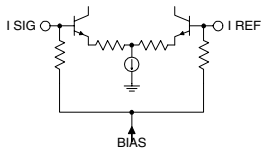
Pin	Function	Description	Interface Schematic
19	RF OUT	Power Amp output, open collector output.	
20	GND5	Same as pin 17.	
21	GND6	Same as pin 17.	
22	NC		
23	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is 3kΩ.	
24	I SIG	Baseband input to the I mixer. A DC bias of approximately 1.7V is present at this pin.A DC blocking capacitor is needed if the signal has a different DC level. Maximum output power is obtained when the input signal has a peak to peak amplitude of 1V. The input impedance of this pin is about 3 kΩ. The REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. The SIG and REF pins may be driven differentially to increase conversion gain.	See pin 23.

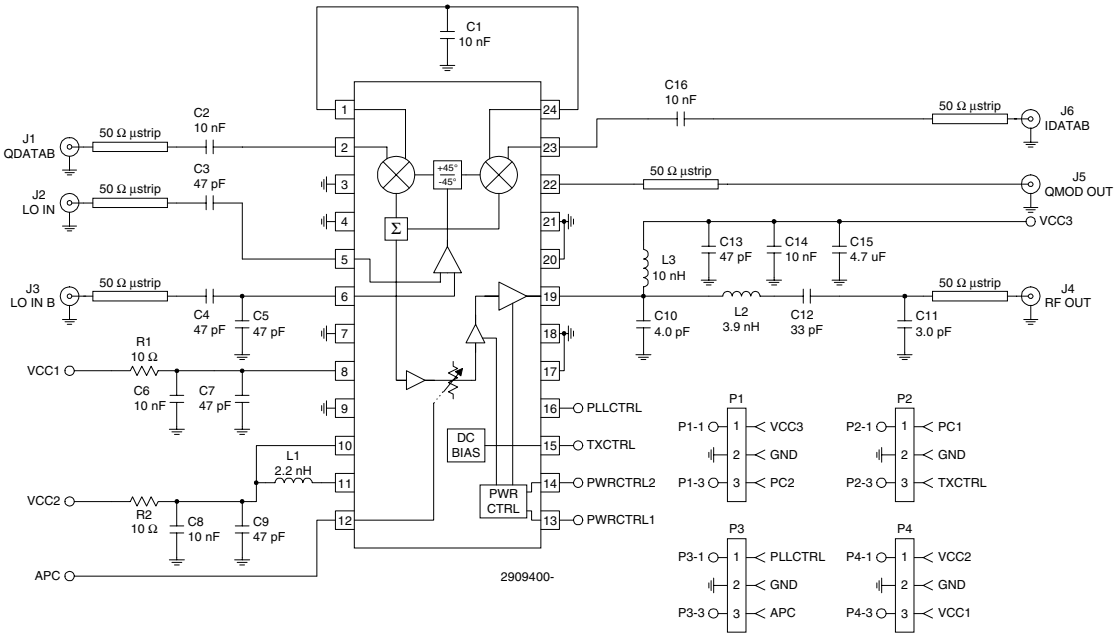
Table I

Operation Mode	TX PD	PLL ON	PC 1	PC 2	APC	Function
Sleep Mode	Low	Low	Low	Low	0V	Entire chip is powered down. Total I_{cc}<1μA.
PLL Buffer	Low	High	Low	Low	0V	LO Buffer is on. I_{cc}=1.5mA
Linear Po Mode	High	High	Low	Low	0-V_{cc}V	Transmitter in on. Power output is proportional to APC.
Digital Po Mode	High	High	Low	Low	0V	Transmitter is on. Power out is 1mW.
Medium Power	High	High	High	Low	0V	Transmitter is on. Power out is 10mW.
High Power	High	High	Low	High	0V	Transmitter is on. Power out is 70mW.

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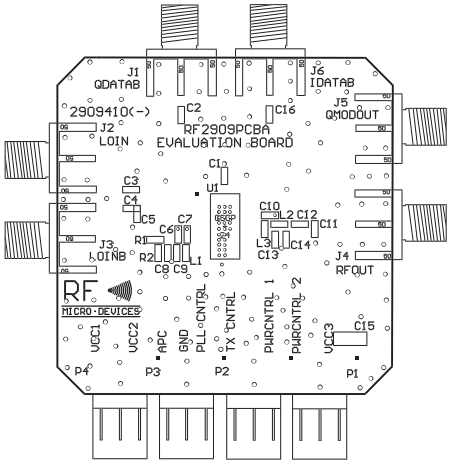
Evaluation Board Schematic

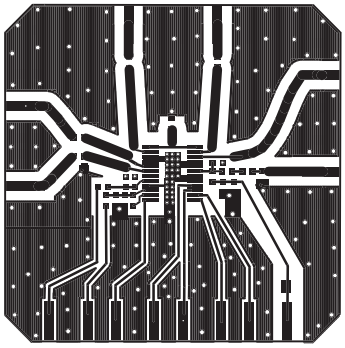
(Download Bill of Materials from www.rfmd.com.)



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Evaluation Board Layout
Board Size 1.7440" x 1.7480"





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RF2915

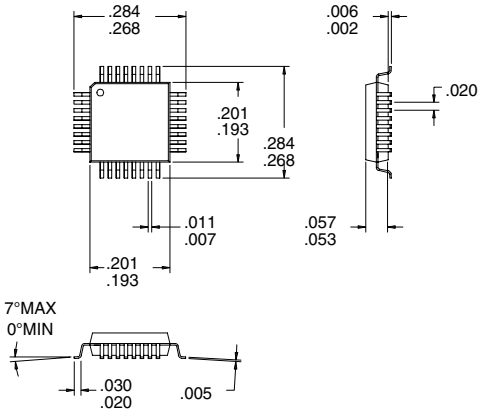
433/868/915MHZ FSK/ASK/OOK TRANSCEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433MHz/868MHz/915MHz ISM Band
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

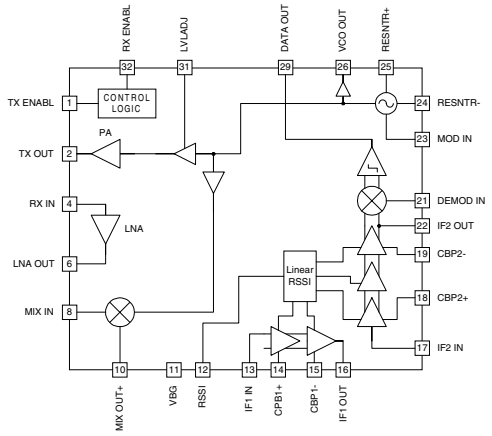
The RF2915 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 32-lead plastic TQFP packaging and is designed to be used with a PLL IC to provide a fully functional FM transceiver. The chip is intended for digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433MHz/868MHz ISM band. The integrated VCO has a buffered output to feed the RF signal back to the PLL IC to form the frequency synthesizer. Internal decoding of the RX ENABL and TX ENABL lines allow for half duplex operation as well as turning on the VCO to give the synthesizer time to settle and complete power down mode.



Package Style: LQFP-32

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Transceiver
- 2.4V to 5.0V Supply Voltage
- Narrow Band and Wide Band FSK
- 300MHz to 1000MHz Frequency Range
- 10dB Cascaded Noise Figure
- 10mW Output Power With Power Control

11

TRANSCEIVERS

Ordering Information

RF2915	433/868/915MHz FSK/ASK/OOK Transceiver
RF2915 PCBA-L	Fully Assembled Evaluation Board (433MHZ)
RF2915 PCBA-M	Fully Assembled Evaluation Board (868MHZ)
RF2915 PCBA-H	Fully Assembled Evaluation Board (915MHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF2915

Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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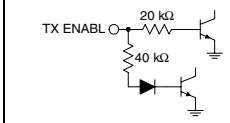
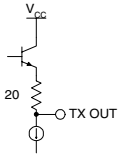
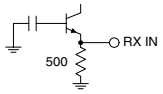
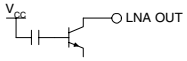
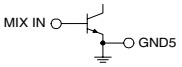
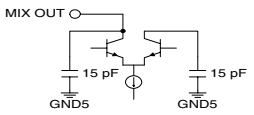
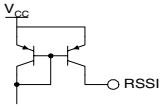
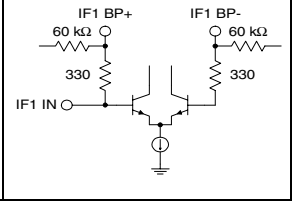
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
VCO OUT Impedance		50		Ω	
VCO OUT Level		-20		dBm	Freq=915MHz
VCO/PLL Phase Noise		-72		dBc/Hz	10kHz offset, Loop BW=5kHz
		-98		dBc/Hz	100kHz offset, Loop BW=5kHz
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+8.5		dBm	Freq=433MHz
	0	+3	6	dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage. Dependent upon external circuitry.
Antenna Port Impedance		50		Ω	TX ENABL="1", RX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-38		dBc	Freq=915MHz, with eval board filter
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity	-95	-99		dBm	IF BW=180kHz, Freq=915MHz, S/N=8dB
LO Leakage		-55		dBm	Freq=915MHz
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		22.5		mV/dB	
RSSI Dynamic Range	70	80		dB	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1", TX ENABL="0"
Antenna Port VSWR			1.5:1		RX Mode
Output Impedance		Open Collector		Ω	433MHz/915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		10		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
Maximum Output Voltage				V_{PP}	Balanced
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT pin
Demod Input Impedance		10		kΩ	
Data Output Impedance		1		MΩ	
Data Output Bandwidth	500			kHz	3 dB Bandwidth, Z_{LOAD}=1MΩ ‖ 3pF
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ‖ 3pF; Output voltage is proportional with the instantaneous frequency deviation.

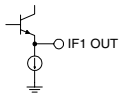
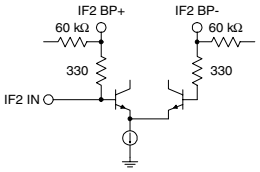
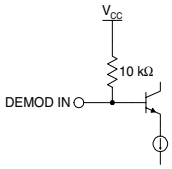
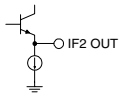
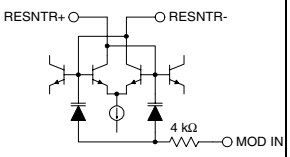
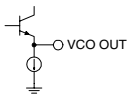
RF2915

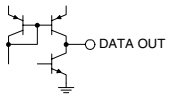
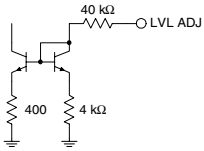
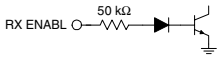
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Turn On Time			1	ms	Turn on/off times are dependent upon PLL loop parameters.
Turn Off Time			1	ms	Turn on/off times are dependent upon PLL loop parameters.
RX to TX and TX to RX Time			100	µs	
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits Temperature range -40°C to +85°C
		2.4		V	Operating limits Temperature range +10°C to +40°C
Current Consumption	18	22	27.4	mA	TX Mode, LVLADJ=3.6V
	4.8	6.1	7.2	mA	TX Mode, LVLADJ=0V
	4.4	5.6	6.8	mA	RX Mode
			1	µA	Power Down Mode
		3.6		mA	PLL Only Mode

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Pin	Function	Description	Interface Schematic
1	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
2	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance (see output impedance plot) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
3	GND2	Ground connection for the 40 dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance (see input impedance plot) when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
5	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
6	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
7	GND3	Same as pin 3.	
8	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
9	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
10	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
11	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	.
12	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.3V and increases with increasing signal strength.	
13	IF1 IN	IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	

RF2915

Pin	Function	Description	Interface Schematic
14	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
15	IF1 BP-	Same as pin 14.	See pin 13.
16	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330 Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 IN	IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330 Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 17.
19	IF2 BP-	Same as pin 18.	See pin 17.
20	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
21	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
22	IF2 OUT	IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 21 through a 5pF capacitor and an FM discriminator circuit.	
23	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 24.
24	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 25 although a small imbalance can be used to tune in the proper frequency range.	
25	RESNTR-	See RESNTR+ description.	See pin 24.
26	VCO OUT	This pin is used is supply a buffered VCO output to go to the PLL chip. This pin has a DC bias and needs to be AC coupled.	
27	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

Pin	Function	Description	Interface Schematic
28	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22 pF capacitor is recommended for 915 MHz applications. A 68 pF capacitor is recommended for 433 MHz applications.	
29	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1 MΩ or greater. When using a RF2915 transmitter and receiver back to back a data inversion will occur with low side LO injection.	
30	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22 pF capacitor is recommended for 915 MHz applications. A 68 pF capacitor is recommended for 433 MHz applications.	
31	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12 dB is provided through analog voltage control of this pin. DC current of the transmitter power amp is also reduced with output power. NOTE: This pin MUST be low when the transmitter is disabled.	
32	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0 V powers up all receiver functions. RX ENABL<1.0 V turns off all receiver functions except the PLL functions and the RF mixer.	

Operation Mode	TX ENABL	RX ENABL	Function
Sleep Mode	Low	Low	Entire chip is powered down. Total current consumption is <1 µA. *
Transmit Mode	High	Low	Transmitter, VCO are on.
Receive Mode	Low	High	Receiver, VCO are on. *
PLL Lock	High	High	VCO is on. This mode allows time for a synthesizer loop to lock without spending current on the transmitter or receiver.

* LVL ADJ pin must be low to disable transmitter.

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RF2915 Theory of Operation and Application Information

The RF2915 is part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433MHz to 868MHz ISM band, and 915MHz U.S. ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products.

In its basic form, the RF2915 can be implemented as a two-way half-duplex FSK transceiver with the addition of some crystals, filters, and passive components. The RF2915 is designed to interface with common PLL IC's to form a multi-channel radio. The receiver IF section is optimized to interface with low-cost 10.7MHz ceramic filters and has a 3dB bandwidth of 25MHz and can still be used (with lower gain) at higher frequencies with other types of filters. The PA output and LNA input are available on separate pins and are designed to be connected together through a DC blocking capacitor. In the transmit mode, the PA will have a 50Ω impedance and the LNA will have a high impedance. In the receive mode, the LNA will have a 50Ω impedance and the PA will have a high impedance. This eliminates the need for a TX/RX switch, and allows for a single RF filter to be used in transmit and receive modes. Separate access to the PA and LNA allows the RF2915 to interface with external components such as a high power PA, lower NF LNA, upconverters, and downconverters, for a variety of implementations.

FM/FSK SYSTEMS

The MOD IN pin drives an internal varactor for modulating the VCO. This pin can be driven with a voltage level needed to generate the desired deviation. This voltage can be carried on a DC bias to select desired slope (deviation/volt) for FM systems. Or, a resistor divider network referenced to VCC or ground can divide down logic level signals to the appropriate level for a desired deviation in FSK systems.

On the receiver demodulator, the DATA OUT pin is generally used as a data slicer providing logic level outputs. However, by lightly loading the output with a resistive load, the bandwidth of the data slicer can be limited, and an analog signal recovered. A resistance value of around 10kΩ to 15kΩ is sufficient. The digital output is generated by a data slicer that is DC-coupled differentially to the demodulator. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesirable 2xIF product. This balanced data slicer has a speed advantage over a conventional adapter data slicer where a large capacitor is used to provide DC reference for the bit decision. Since a balanced data slicer does not have to charge a large capacitor, the RF2915 exhibits a very fast response time. For best operation of the on-chip data slicer, FM deviation needs to exceed the carrier frequency error anticipated between the receiver and transmitter with margin.

The data slicer itself is a transconductance amplifier, and the DATA OUT pin is capable of driving rail-to-rail output only into a very high impedance and a small capacitance. The amount of capacitance will determine the bandwidth of DATA OUT. In a 3pF load, the bandwidth is in excess of 500kHz. The rail-to-rail output of the data slicer is also limited by the frequency deviation and bandwidth of IF filters. With the 180kHz bandwidth filters on the evaluation boards, the rail-to-rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation versus data rate (mod index) is important in evaluating the applicability of the RF2915 for a given data rate.

The primary consideration when directly modulating the VCO is the data rate versus PLL bandwidth. The PLL will track out the modulation to the extent of its bandwidth, which distorts the modulating data. Therefore, the lower frequency components of the modulating data should be five to 10 times the loop bandwidth to minimize the distortion. The lower frequency components are generated by long strings of 1's and 0's in data stream. By limiting the number of consecutive, same bits, lower frequency components can be set. In addition, the data stream should be balanced to minimize distortion. Using a coding pattern such as Manchester is highly recommended to optimize system performance.

The PLL loop bandwidth is important in several system parameters. For example, switching from transmit to receive requires the VCO to retune to another frequency. The switching speed is proportional to the loop bandwidth: the higher the loop bandwidth, the faster the switching times. Phase noise of the VCO is another factor. Phase noise outside the bandwidth is because of the VCO itself, rather than a crystal reference. The design trade-offs must be made here in selecting a PLL loop bandwidth with acceptable phase noise and switching characteristics, as well as minimal distortion of the modulation data.

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ASK/OOK SYSTEMS

The transmitter of the RF2915 has an output power level adjust (LVL ADJ) that can be used to provide approximately 18dB of power control for amplitude modulation. The RSSI output of the receiver section can be used to recover the modulation. The RSSI output is from a current source, and needs to have a resistor to convert to a voltage. A 51kΩ resistor load typically produces an output of 0.7V to 2.5V. A parallel capacitor is suggested to the band limit of the signal. For ASK applications, the 18dB range of the LVL ADJ does not produce enough voltage swing in the RSSI for reliable communications. The on/off keying (OOK) is suggested to provide reliable communications. To achieve this, the LVL ADJ and TX ENABL need to be controlled together (please note that LVL ADJ cannot be left high when TX ENABL is low). This will provide an on/off ratio of greater than 50dB. One of the unfortunate consequences of modulating in this manner is VCO pulling by the PA. This results in a spurious output outside the desired transmit band, as the PLL momentarily loses lock and reacquires. This may be avoided by pulse-shaping TX data to slow the change in the VCO load to a pace which the PLL can track with its given loop bandwidth. The loop bandwidth may also be increased to allow it to track faster changes brought about by load pulling.

For the ASK/OOK receiver demodulator, an external data slicer is required. The RSSI output is used to provide both the filter data and a very low pass filter (relative to the data rate) DC reference to the data slicer. Because the very low pass filter has a slow time constant, a longer preamble may be required to allow for the DC reference to acquire a stable state. Here, as in the case of the FSK transmitter, the data pattern also affects the DC reference and the reliability of the receive data. Again, a coding scheme such as Manchester should be used to improve data integrity.

APPLICATION AND LAYOUT CONSIDERATIONS

Both the RX IN and the TX OUT have a DC bias on them. Therefore, a DC blocking cap is required. If the RF filter has DC blocking characteristics (such as a ceramic dielectric filter), then only one DC blocking cap would be needed to separate the DC of the RX and TX. These are RF signals and care should be taken to run the signal keeping them physically short. Because of the 50Ω/high impedance nature of these two signals, they may be connected together into a single 50Ω device (such as a filter). An external LNA or PA may be used, if desired, but an external RX/TX switch may be required.

The VCO is a very sensitive block in the system. RF signals feeding back into the VCO (either radiated or coupled by traces) may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonator and varactor are very important. The capacitor and varactor should be close to the RF2915 pins, and the trace length should be as short as possible. The inductors may be placed further away, and reducing the value of the inductors can compensate any trace inductance. Printed inductors may also be used with careful design. For best results, physical layout should be as symmetrical as possible. Figure 1 is a recommended layout pattern for the VCO components. When using the loop bandwidth lower than 5kHz shown on the evaluation board, better filtering of the VCC at the resonators (and lower VCC noise, as well) will help reduce phase noise of the VCO. A series resistor of 100Ω to 200Ω, and a 1μF or larger capacitor may be used.

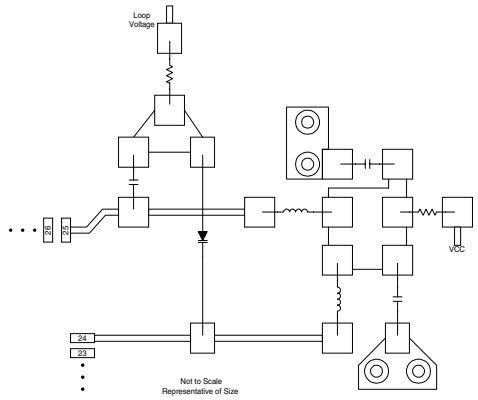


Figure 1. Recommended VCO Layout

For the interface between the LNA/mixer, the coupling capacitor should be as close to the RF2915 pins as possible, with the bias inductors further away. Once again, the value of the inductor may be changed to compensate for trace inductance. The output impedance of the LNA is in the order of several kΩ, which makes matching to 50Ω very difficult. If image filtering is desired, a high impedance filter is recommended.

The quad tank of the discriminator may be implemented with ceramic discriminator available from a couple of sources. This design works well for wideband applications where temperature range is limited. The temperature coefficient of ceramic discriminators may be in the order of +50ppm/°C. The alternative to the

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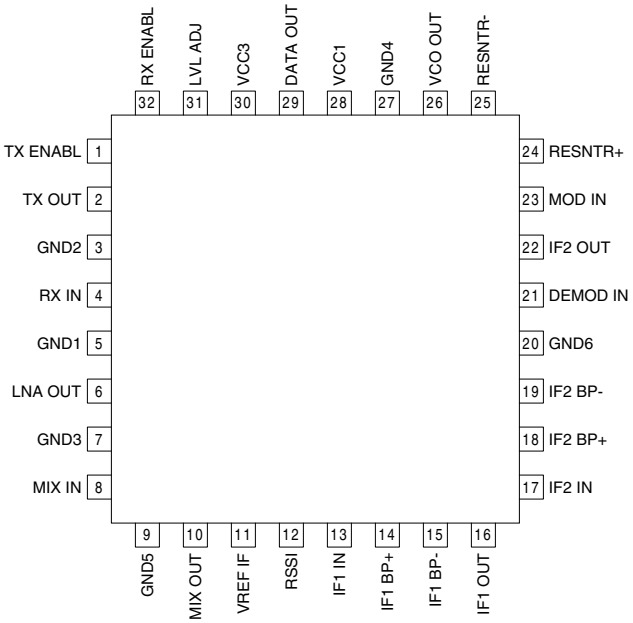
ceramic discriminator is the LC tank, which provides a broadband discriminator more useful for high data rates.

PLL Synthesizer

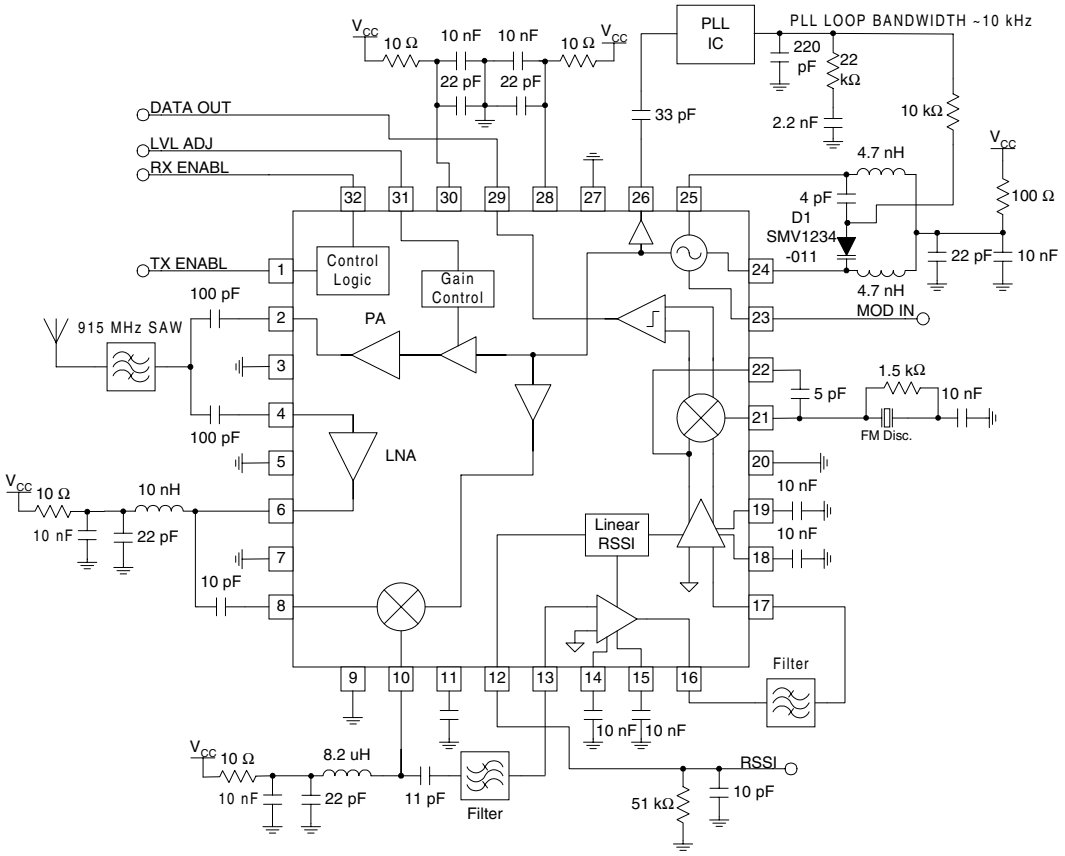
The RF2915 evaluation board uses an LMX2315 PLL IC from National Semiconductor. This PLL IC may be programmed from the software available from National Semiconductor (codeloader at www.national.com/appinfo/wireless/). An external reference oscillator is required for the PLL IC allowing for the evaluation of different reference frequencies or step sizes. The National Semiconductor software also has a calculator for determining the R and C component values for a given loop bandwidth.

The RF2915 is controlled by RX ENABL and TX ENABL which are decoded to put the RF2915 into one of four states. It may be put into a PLL-only mode with TX ENABL and RX ENABL both high. This condition is used to provide time for the synthesizer to turn on an obtained lock before turning on the receiver or transmitter. Note that LVL ADJ needs to be held low for PLL-only mode. Sometimes, it is desirable to ramp up the power amplifier to minimize load pulling on the VCO. To do this with the RF2915, first put the RF2915 into PLL mode by putting TX ENABL and RX ENABL high. Then, ramp up LVL ADJ to turn on the transmitter and PA. The rate at which LVL ADJ is allowed to ramp up is dependent on the PLL loop bandwidth. VCC pushing also affects the VCO frequency. A good low pass filter on VCC will minimize the VCC pushing effects.

Pin Out


RX ENABL 32
LVL ADJ 31
VCC3 30
DATA OUT 29
VCC1 28
GND4 27
VCO OUT 26
RESNTR- 25
TX ENABL 1
TX OUT 2
GND2 3
RX IN 4
GND1 5
LNA OUT 6
GND3 7
MIX IN 8
24 RESNTR+
23 MOD IN
22 IF2 OUT
21 DEMOD IN
20 GND6
19 IF2 BP-
18 IF2 BP+
17 IF2 IN
9 GND5
10 MIX OUT
11 VREF IF
12 RSSI
13 IF1 IN
14 IF1 BP+
15 IF1 BP-
16 IF1 OUT

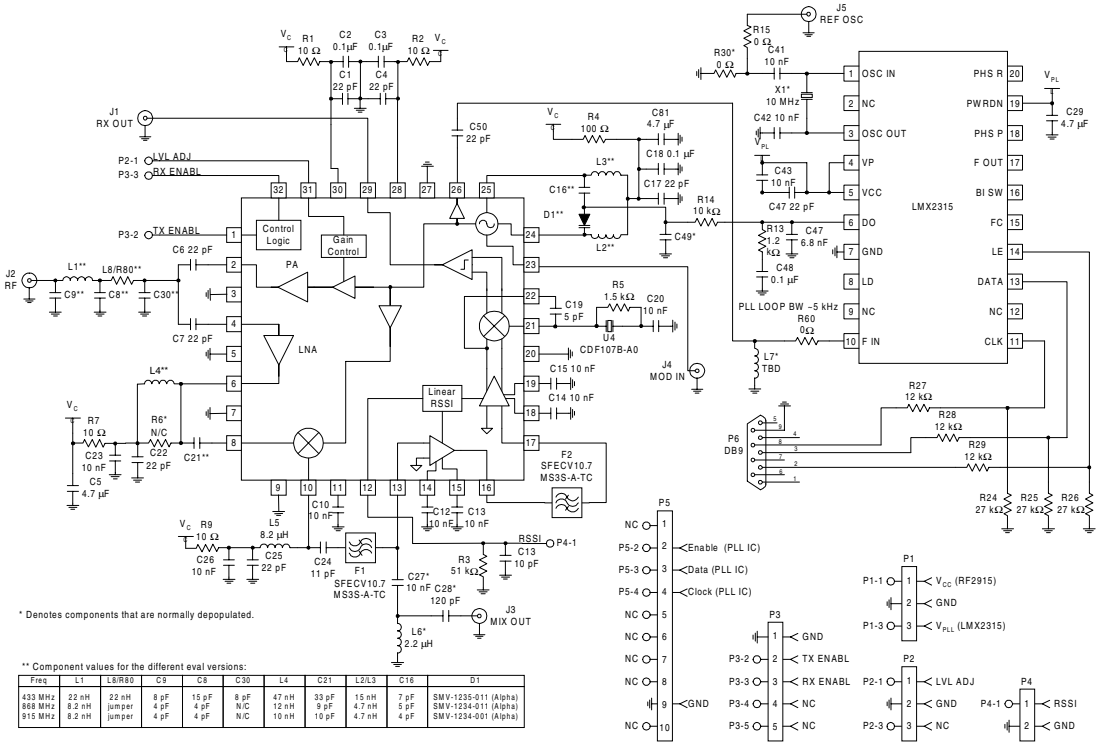
915 MHz Application Schematic



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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



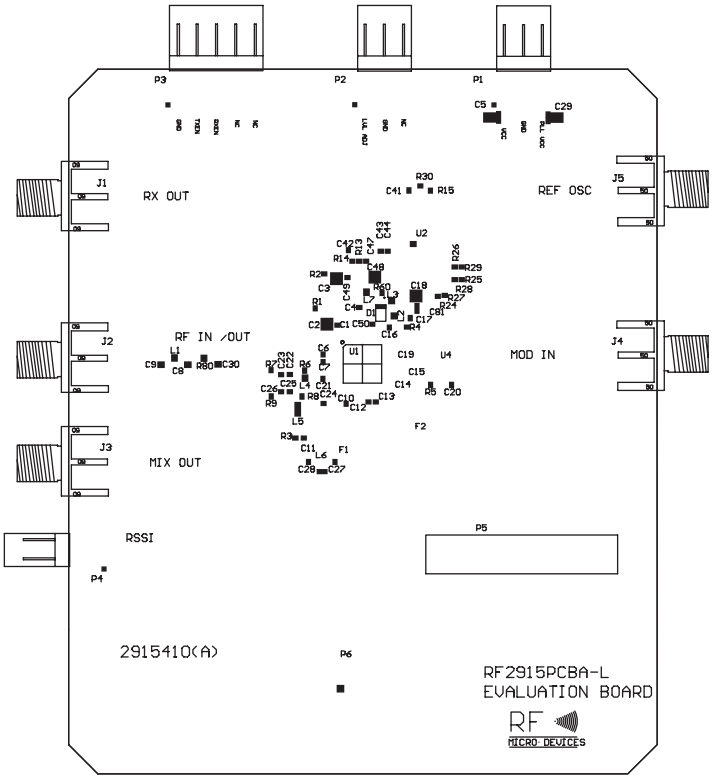
* Denotes components that are normally depopulated.

** Component values for the different eval versions:

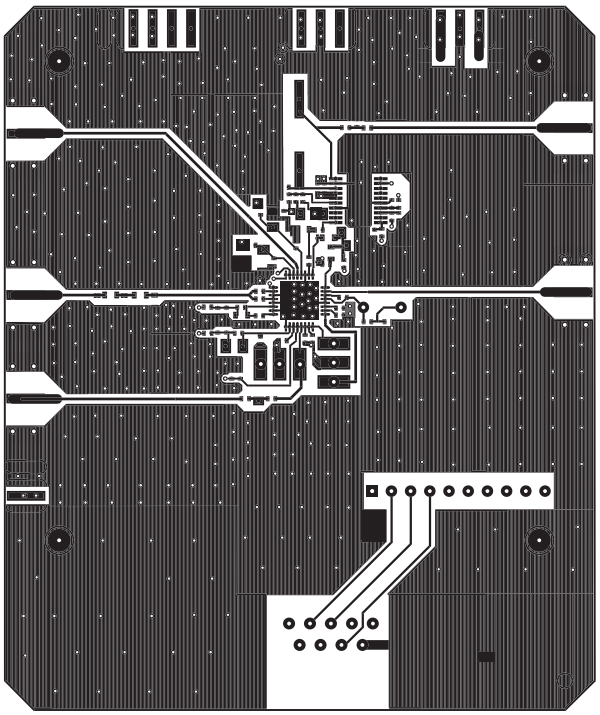
Freq	L1	L8/R80	C9	C8	C30	L4	C21	L2/L3	C16	D1
433 MHz	22 nH	22 nH	8 pF	15 pF	8 pF	47 nH	33 pF	15 nH	7 pF	SMV-1235-011 (Alpha)
868 MHz	8.2 nH	jumper	4 pF	4 pF	N/C	12 nH	9 pF	4.7 nH	5 pF	SMV-1234-011 (Alpha)
915 MHz	8.2 nH	jumper	4 pF	4 pF	N/C	10 nH	10 pF	4.7 nH	4 pF	SMV-1234-001 (Alpha)

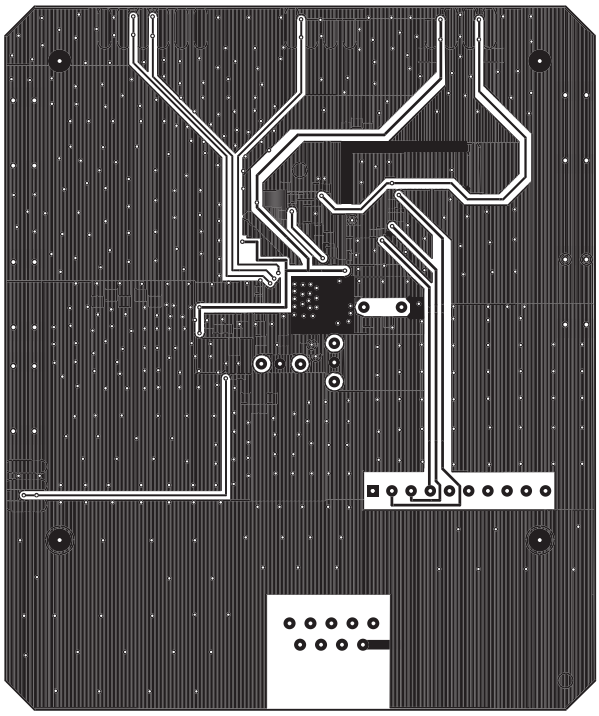
Evaluation Board Layout
Board Size 3.070" x 3.670"

Same board layout is used for the -L, -M, and -H versions

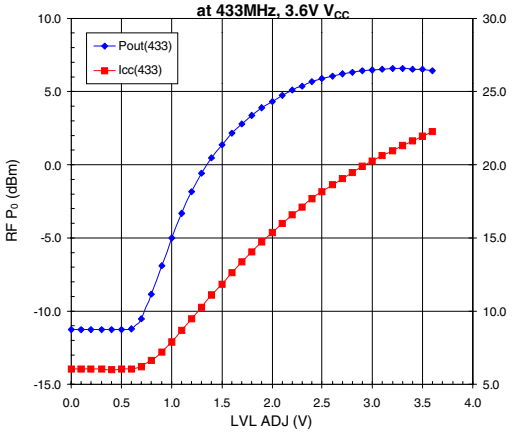


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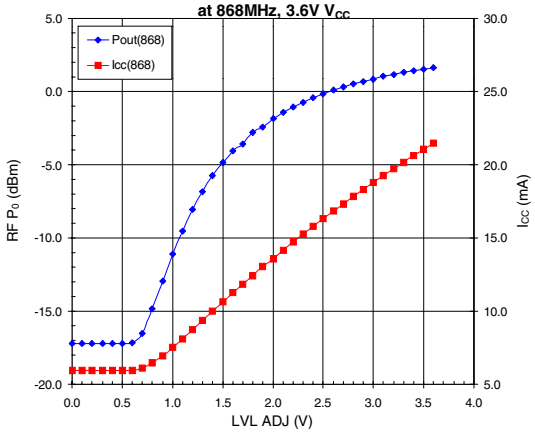




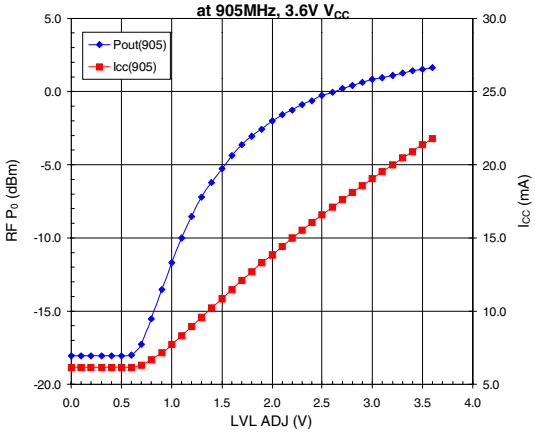
TX Power Output and I_{CC} versus Level Adjust at 433MHz, 3.6V V_{CC}



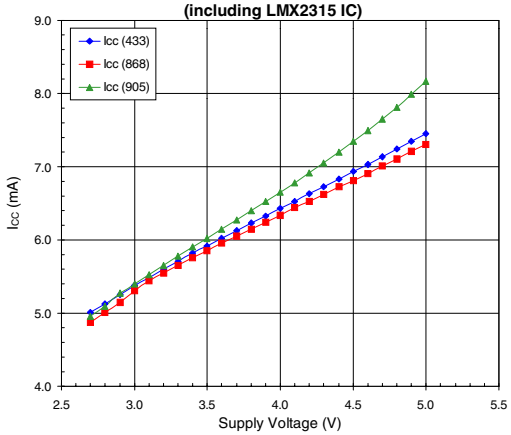
TX Power Output and I_{CC} versus Level Adjust at 868MHz, 3.6V V_{CC}



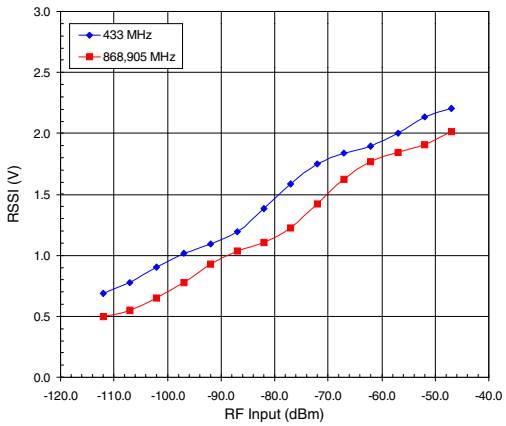
TX Power Output and I_{CC} versus Level Adjust at 905MHz, 3.6V V_{CC}



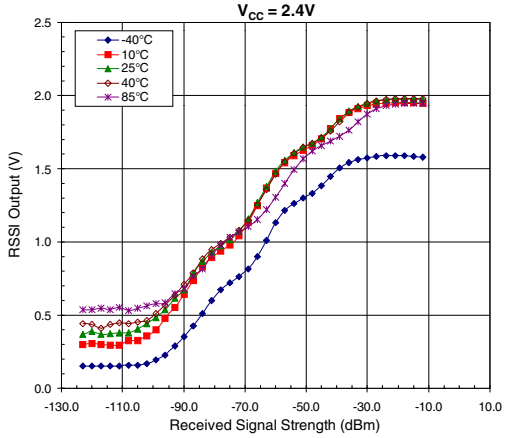
Receive Current versus V_{CC} (including LMX2315 IC)



RSSI versus RF Input



RSSI Output versus Temperature V_{CC} = 2.4V



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MICRO·DEVICES

Preliminary

RF2917

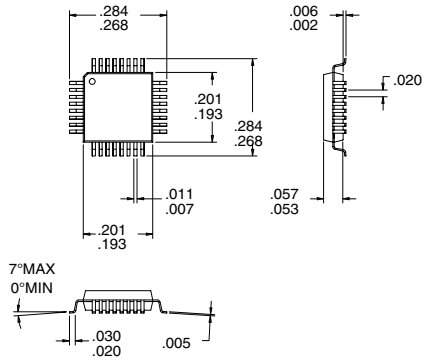
433/868/915MHZ FM/FSK RECEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Remote Data Transfers
- Wireless Security Systems

Product Description

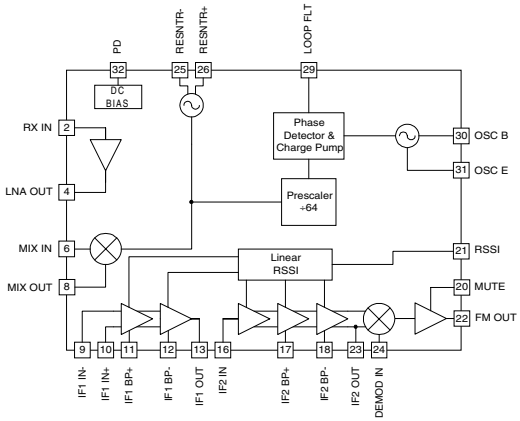
The RF2917 is a monolithic integrated circuit intended for use as a low cost FM or FSK receiver. The device is provided in 32-lead plastic packaging and is designed to provide a fully functional FM receiver. The chip is intended for analog or digital applications in the North American 915MHz ISM band and European 433MHz and 868 MHz ISM bands. The integrated VCO, ÷64 prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator for single channel applications. The selection of linear FM output or digital FSK output is done with the mute pin.



Package Style: LQFP-32

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Receiver
- 2.7V to 5.0V Supply Voltage
- Narrow Band and Wide Band FSK
- 300MHz to 1000MHz Frequency Range
- Power Down Capability
- Analog or Digital Output

11

TRANSCEIVERS

Ordering Information

RF2917	433/868/915MHz FM/FSK Receiver
RF2917 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2917 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2917 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

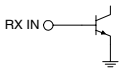
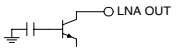
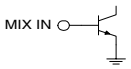
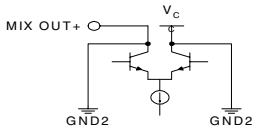
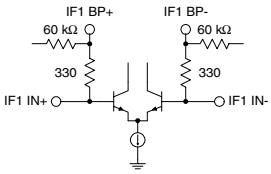
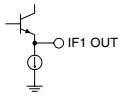
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

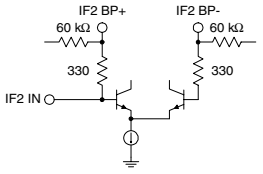
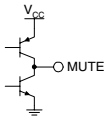
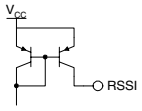
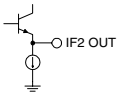
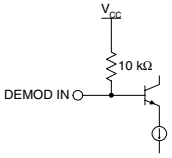
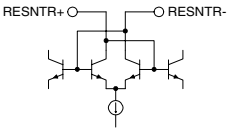
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
PLL Lock Time		10		ms	The PLL lock time is set externally by the bandwidth of the loop filter and start up of the crystal.
PLL Phase Noise		-74		dBc/Hz	915MHz, 5kHz loop BW, 10kHz offset
		-98		dBc/Hz	915MHz, 5kHz loop BW, 100kHz offset
Reference Frequency	0.5		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
RX Sensitivity	-98	-101		dBm	IF BW=180kHz, Freq=915MHz, S/N=8dB
LO Leakage		-55		dBm	
RSSI DC Output Range		0.8 to 1.5		V	MUTE = 0; R_L = 51kΩ
RSSI Sensitivity		13		mV/dB	MUTE = 0
RSSI Dynamic Range		60		dB	MUTE = 0
LNA					
Power Gain		18		dB	433MHz, Matched to 50Ω
		16		dB	915MHz, Matched to 50Ω
Noise Figure		3.6		dB	433MHz
		3.8		dB	915MHz
Input IP_3		-8		dBm	915MHz
Input P_{1dB}		-15		dBm	915MHz
RX IN Impedance		82-j86		Ω	433MHz (see Plots)
		77-j43			915MHz (see Plots)
Output Impedance		Open Collector		Ω	
Mixer					Single-ended configuration
Conversion Power Gain		15		dB	433MHz, Matched to 50Ω
		8		dB	915MHz, Matched to 50Ω
Noise Figure (SSB)		17		dB	433MHz, SSB Measurement
		17		dB	915MHz, SSB Measurement
Input IP_3		-20		dBm	433MHz
Input IP_3		-15.5		dBm	915MHz
Input P_{1dB}		-30		dBm	433MHz
Input P_{1dB}		-26		dBm	915MHz
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	

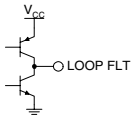
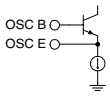
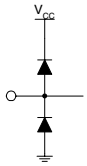
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
Noise Figure		13		dB	
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin 23
Demod Input Impedance		10		kΩ	Pin 24
Data Output Impedance		6.3 - j25.7		kΩ	
Data Output Bandwidth		500		kHz	Z_{LOAD}=1MΩ ll 3pF; 3dB dependent on IF and discriminator BW
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ll 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	
FM Output AC Level		200		mV_{PP}	
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25			kΩ	
Turn On Time		10.2		ms	From PD=1 to valid data out, current eval board
Power Supply					
Voltage		3.6		V	Specifications
	2.7		5.0	V	Operating limits
	2.4			V	Temp>0°C
Current Consumption	8.1	9	12.3	mA	RX Mode, MUTE=“1”
			1	µA	Power Down Mode

Pin	Function	Description	Interface Schematic
1	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 100pF capacitor is recommended for 433MHz applications.	
2	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance when enabled. RX IN is a high impedance when the receiver is disabled.	
3	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
5	GND2	GND2 is connection for the 40 dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
6	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
7	GND3	GND3 is the ground connection for the receiver RF mixer.	
8	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
9	IF1 IN-	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
10	IF1 IN+	Functionally the same as pin 9 except non-inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 9.
11	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 100nF bypass capacitor from this pin to ground is required.	See pin 9.
12	IF2 BP-	See pin 11.	See pin 9.
13	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
14	VREF IF	DC voltage reference for the IF limiting amplifiers. A 0.1µF capacitor from this pin to ground is required.	
15	GND5	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	

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Pin	Function	Description	Interface Schematic
16	IF2 IN	Inverting input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 100nF bypass capacitor from this pin to ground is required.	See pin 16.
18	IF2 BP-	See pin 17.	See pin 16.
19	VCC3	This pin is used to supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
20	MUTE	This pin is used to select FM, FSK, or mute at the FM OUT pin. MUTE>Vcc - 0.4V turns the FM OUT signal off. MUTE<0.4V turns the FM OUT signal on for FSK digital data. When MUTE is left floating, the FM OUT signal is linear FM.	
21	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage increases with increasing signal strength.	
22	FM OUT	Demodulated output from the discriminator/demodulator. Output levels on this are CMOS compatible in FSK mode (see pin 20). In linear FM mode, the demodulated signal level is approximately 240mVpp on a DC voltage offset. The magnitude of the load impedance is intended to be 1MΩ or greater.	
23	IF2 OUT	IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 24 through a 5pF capacitor (for 10.7MHz IF applications). This capacitor in conjunction with a tank resonant at the IF frequency connected from pin 24 to ground is used to form an FM discriminator.	
24	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid a DC path to ground. A DC blocked LC tank resonant at the IF or ceramic discriminator should be connected to this pin.	
25	RESNTR-	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 26.	
26	RESNTR+	See pin 25.	See pin 25.
27	VCC2	This pin is used to supply DC bias to the VCO, prescaler, and PLL. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
28	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

Pin	Function	Description	Interface Schematic
29	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
30	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 100pF capacitor should be connected between pin 30 and pin 31.	
31	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 100pF capacitor should be connected from this pin to ground.	See pin 30.
32	PD	This pin is used to power up or down the RF2917. A logic high (PWR DWN >2.0 V) powers up the receiver and PLL. A logic low (PWR DWN <1.0 V) powers down circuit to standby mode.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 7-19, 21-24, 27-31.	

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RF2917 Theory of Operation and Application Information

The RF2917 is part of a family of low-power RF transceiver IC's developed for wireless data communication devices operating in the European 433/868MHz ISM bands or the U.S. 915MHz ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products. The RF2917 realizes a highly integrated, single-conversion FM/FSK receiver with the addition of a reference crystal, intermediate frequency (IF) filtering, and a few passive components. The LNA (low noise amplifier) input of the RF2917 is easily matched to a front-end filter or antenna by means of a DC blocking capacitor and reactive components. The receiver local oscillator (LO) is generated by an internalized VCO, PLL and phase discriminator in conjunction with the external reference crystal, loop filter and VCO resonator components. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters, and its -3dB bandwidth of 25MHz also allows it to be used (with lower gain) at higher frequencies with other types of filters.

FM/FSK SYSTEMS

The receiver output functionality is determined by the tri-state MUTE input. The three output configurations are linear FM, FSK and mute. An on-chip 1.6MHz RC filter, which follows the demodulator output, filters the harmonics of the IF signal from the output data.

When in the FM mode, the FM OUT signal is the buffered output from the quadrature demodulator. The output signal has a fixed DC offset of V_{CC}-1.0V, while the AC level is dependent on the FM deviation, with a maximum level of 240mV_{P-P} For optimum operation in either FM or FSK mode, FM deviation needs to exceed (with margin) the carrier frequency error anticipated between the receiver and transmitter.

When in the FSK mode, the FM OUT signal is clipped, having a rail-to-rail output level. The FM OUT pin is only capable of driving rail-to-rail output into a very high impedance and small capacitance, with the amount of capacitance determining the FM OUT bandwidth. For a 3pF load, the bandwidth is in excess of 500kHz. The rail-to-rail output is also limited by the frequency deviation and bandwidth of the IF filters. With the 180kHz bandwidth filters on the evaluation boards, the rail-to-rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation versus data rate (modulation index) is important in evaluating the applicability of the RF2917 for a given data rate.

AM SYSTEMS

The RF2919 is recommended for use in ASK/OOK applications, however, the RF2917 may be utilized in an AM system by using the RSSI (received signal strength indicator) output to recover the modulation. The FM output mode should be selected for AM operation because of the higher RSSI resolution in FM mode.

RSSI

The RSSI output signal is supplied from a current source and therefore requires a resistor to convert it to a voltage. The RSSI is linear over the same range of input power for both FM and FSK modes, but the FM mode has higher RSSI resolution. For a 51kΩ resistive load, the RSSI will range from 1.0V to 2.6V in FM mode and from 0.8V to 1.5V in FSK mode (3.6V supply). A small parallel capacitor is suggested to limit the bandwidth and filter noise.

APPLICATION AND LAYOUT CONSIDERATIONS

The RX IN pin is DC-biased, requiring a DC blocking capacitor. If the RF filter has DC blocking characteristics, such as a ceramic dielectric filter, then a DC blocking capacitor is not necessary. When in power down mode, the RX IN impedance increases. Therefore, in a half-duplex application, the RF2917 RX IN may share the RF filter with a transmitter output having a similar high impedance power down characteristic. Care must be taken in this case to account for loading effects of the transmitter on the receiver, and vice versa, in matching the filter to both the transmitter and receiver.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO by either radiation or coupling of traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2917 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible.

When using loop bandwidths lower than the 5kHz shown on the evaluation board, better supply filtering at the resonators (and lower V_{CC} noise as well) will help reduce the phase noise of the VCO; a series resistor of 100Ω to 200Ω and a 1μF or larger capacitor

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may be used. Phase noise is generally more critical in narrowband applications where adjacent channel selectivity is a concern, but it can also contribute to raising the noise floor of the receiver, thereby degrading sensitivity.

For the interface between the LNA and mixer, the coupling capacitor should be as close to the RF2917 pins as possible, with the bias inductor being further away. Once again, the value of the inductor may be changed to compensate for trace inductance. The output impedance of the LNA is on the order of several kΩ, which makes matching to 50Ω difficult. If image filtering is desired, a high impedance filter is recommended. If no filtering is used, the match to the mixer input need not be a good conjugate match, because of the high gain of the IF amplifier stages. In fact, a conjugate match between the LNA and mixer will not significantly improve sensitivity, but will have an adverse effect on system IIP3 and increase the likelihood of IF instability.

Because of the high gain of the IF section, care should be taken in laying out the IF filtering and discriminator components to minimize the possibility of instability. In particular, inductive feedback may occur between the inductor of a discrete (LC) discriminator and any inductor(s) in the IF interstages. Orthogonal placement of inductors will generally minimize coupling. Indicators that an instability may exist include poor sensitivity and a high RSSI level when no input signal is present.

The quadrature tank of the discriminator may be implemented with ceramic discriminators available from a variety of sources. This design works well for wideband applications, and where the temperature range is limited. The temperature coefficient of a ceramic discriminator may be on the order of ±50ppm/°C. An automatic frequency control loop may be implemented using the DC level of the FM OUT for feedback to an external varactor on the reference crystal. An alternative to the ceramic discriminator is an LC tank. The DEMOD IN pin has a DC bias and must be DC-blocked. This can be done either at the pin or at the ground side of the LC tank (this must also be done if a parallel resistor is used with a ceramic discriminator). The decision whether to use an LC or a ceramic discriminator should be based on the frequency deviation in the system, discriminator Q needed, and frequency and temperature tolerances. Tuning of the LC tank is required to overcome the component tolerances in the tank.

PREDICTING AND MINIMIZING PLL LOCK TIME

The RF2917 implements a conventional on-chip PLL. The VCO is followed by a prescaler, which divides down the output frequency for comparison with the reference oscillator frequency. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current, combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF2917 is:

$$LockTime = \frac{D}{F_C} + 35000 \cdot C \cdot dV$$

where D is a factor to account for the loop damping, F_C is the loop cut frequency, C is the sum of all shunt capacitors in the loop filter, and dV is the required step voltage change to produce the desired frequency change during the transient. For loops with low phase margin (30° to 40°), use D=2, whereas for loops with better phase margin (50° to 60°), use D=1.

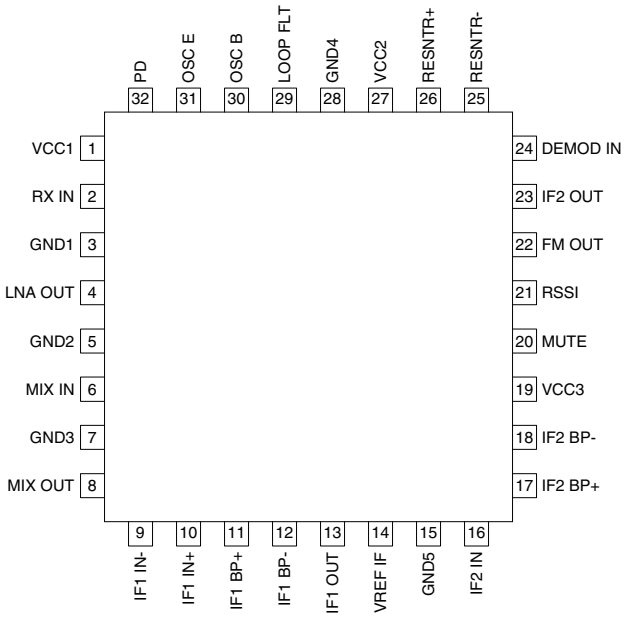
To lock faster, C needs to be minimized.

1. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.

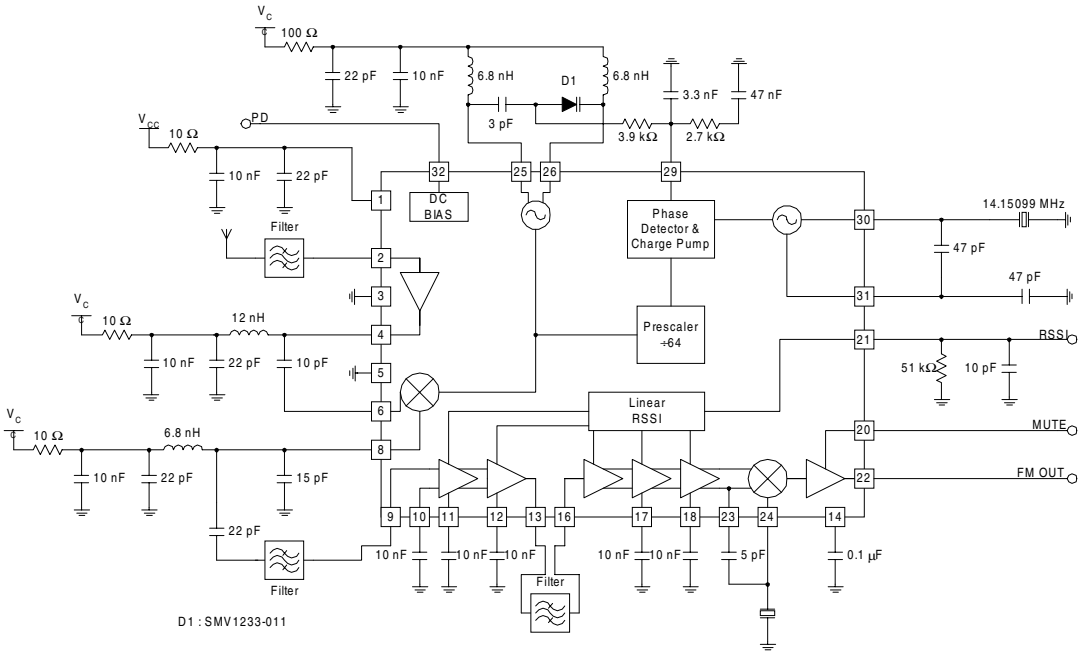
2. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

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Pin Out



915MHz Application Schematic



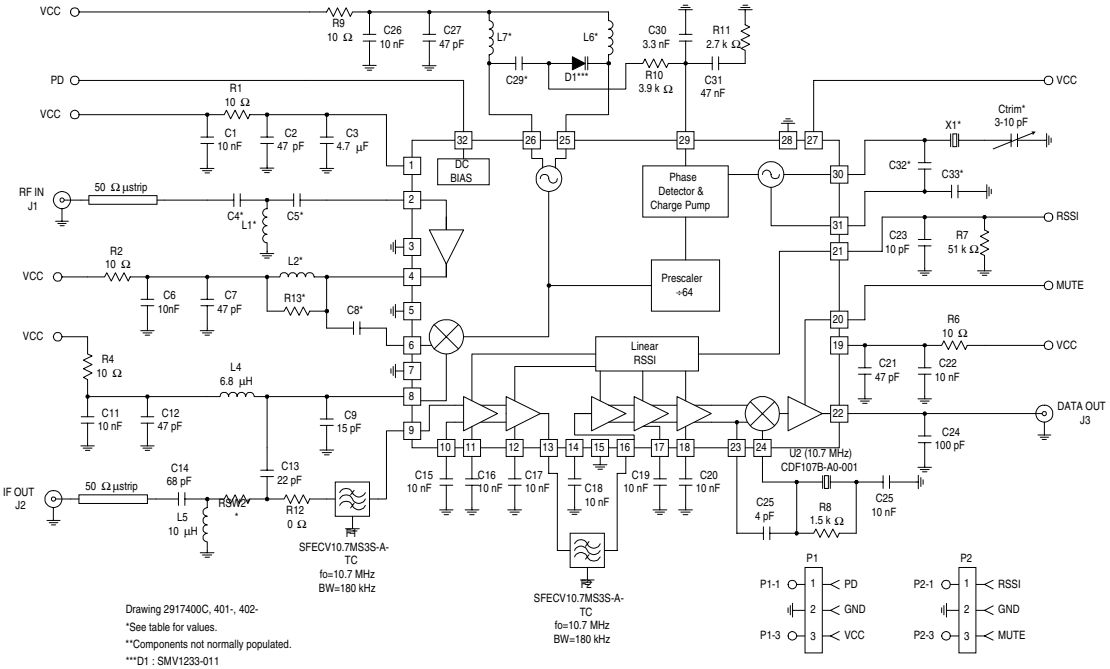
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Evaluation Board Schematic
H (915MHz), M (868MHz), L (433MHz) boards

(Download Bill of Materials from www.rfmd.com.)



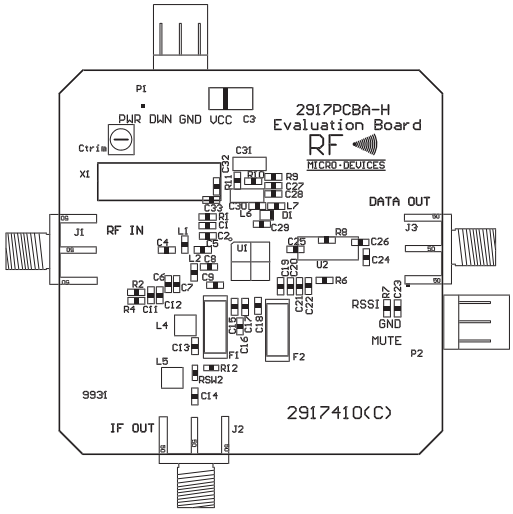
Drawing 2917400C, 401-, 402-
*See table for values.
**Components not normally populated.
***D1 : SMV1233-011

Board	C4 (pF)	L1 (nH)	C5 (pF)	L2 (nH)	R13 (Ω)	C8 (pF)	L6 (nH)	L7 (nH)	C29 (pF)	X1 (MHz)	C32 (pF)	C33 (pF)
L (433MHz)	2	27	100	33	510	9	18	18	9	6.612813	100	100
M (868MHz)	1.5	8.2	100	12	-	1	6.8	6.8	3	13.41015	100	100
H (915MHz)	2	6.8	22	12	-	1	6.8	6.8	3	14.15099	47	47

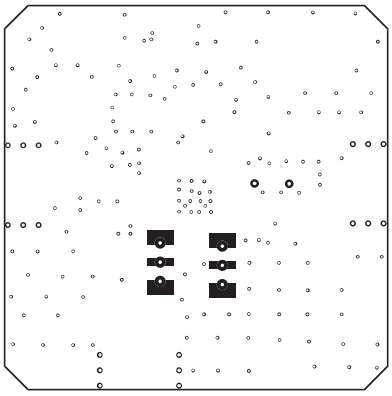
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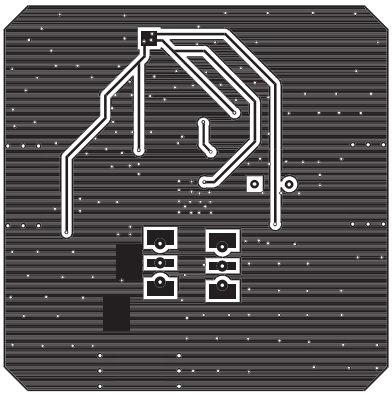
Evaluation Board Layout - M and H
Board Size 2.0” x 2.0”

Board Thickness 0.040”, Board Material FR-4, Multi-Layer
(Same board layout is being used for the -M and -H versions.)





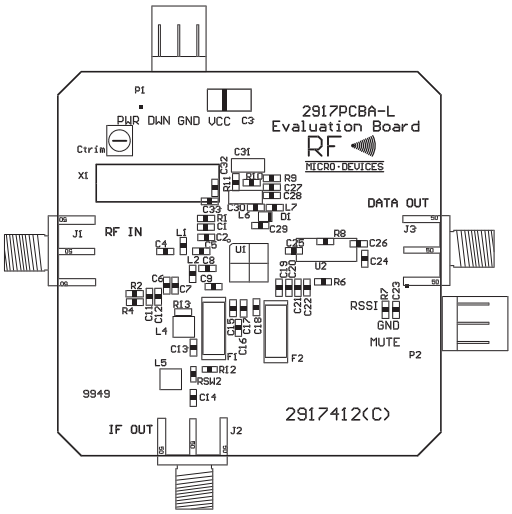


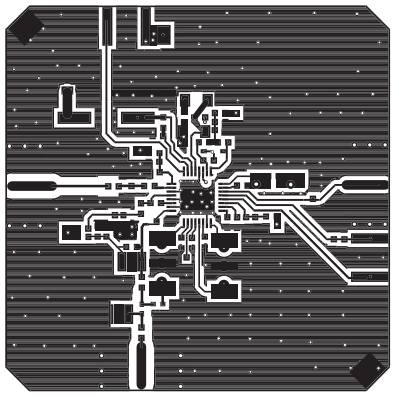


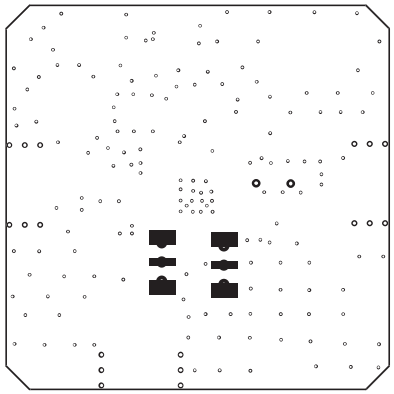
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Evaluation Board Layout - L
Board Size 2.0” x 2.0”

Board Thickness 0.048”, Board Material FR-4, Multi-Layer

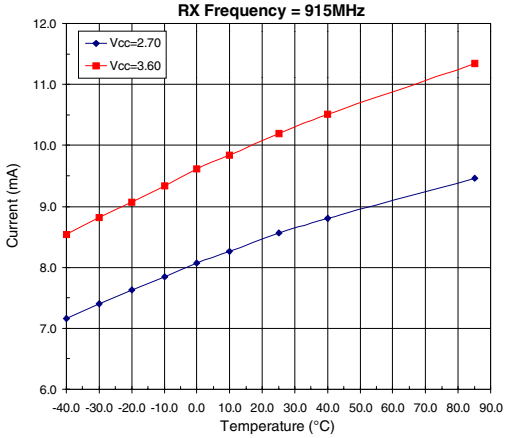




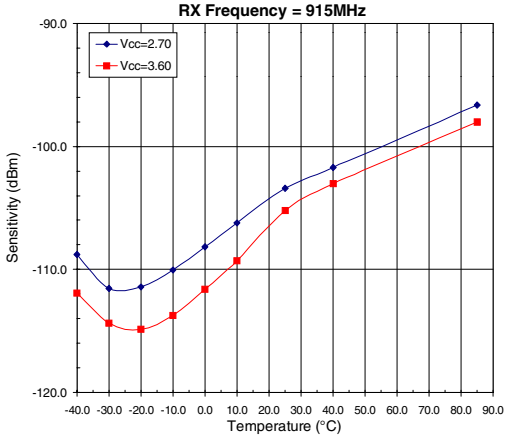




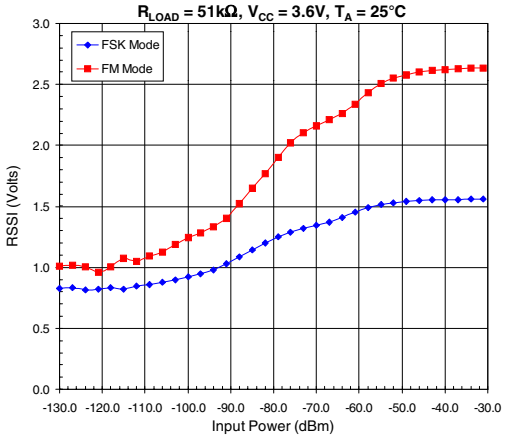
Current versus Temperature
RX Frequency = 915MHz



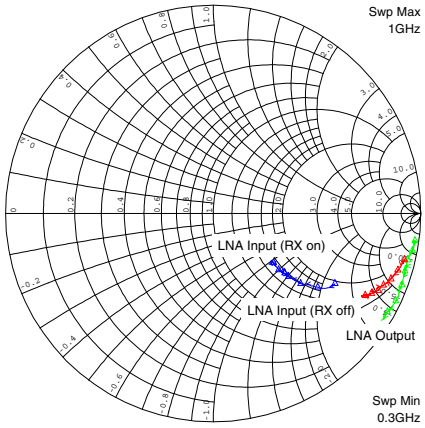
Sensitivity versus Temperature
RX Frequency = 915MHz



RSSI versus Input Power
R_{LOAD} = 51kΩ, V_{CC} = 3.6V, T_A = 25°C



LNA Impedance



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RF MICRO·DEVICES

Preliminary

RF2919

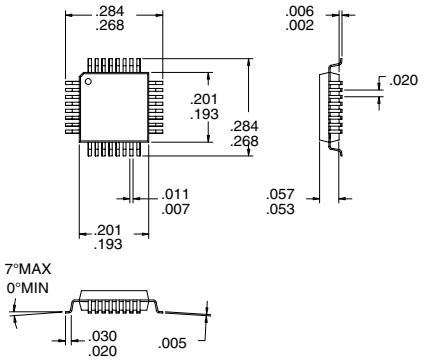
433/868/915MHZ ASK/OOK RECEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Bands Systems
- Remote Data Transfers
- Wireless Security Systems
-

Product Description

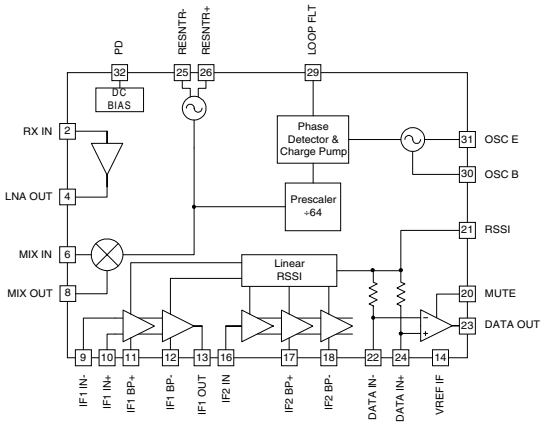
The RF2919 is a monolithic integrated circuit intended for use as a low cost ASK/OOK receiver. The device is provided in 32-lead plastic packaging and is designed to provide a fully functional AM receiver. The chip is intended for applications in the North American 915MHz ISM band and European 433MHz and 868MHz ISM bands. The integrated VCO, +64 prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator for single channel applications. A data comparator is included to provide logic level outputs.



Package Style: LQFP-32

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Receiver
- 2.7V to 5.0V Supply Voltage
- Up to 256kbps Data Rates
- 300MHz to 1000MHz Frequency Range
- Power Down Capability
- Analog or Digital Output

Ordering Information

RF2919	433/868/915MHz ASK/OOK Receiver
RF2919 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2919 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2919 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

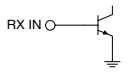
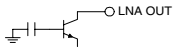
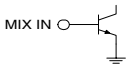
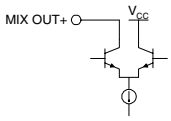
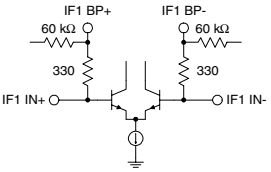
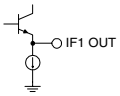
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
PLL Lock Time		10		ms	The PLL lock time is set externally by the bandwidth of the loop filter and start-up of the crystal.
PLL Phase Noise		-74		dBc/Hz	915MHz, 5kHz loop BW, 10kHz offset
		-98		dBc/Hz	915 MHz, 5kHz loop BW, 100kHz offset
Reference Frequency	0.5		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current		40		µA	Sink and source current
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
RX Sensitivity	-100	-104		dBm	IF BW=150kHz, Freq=915MHz, S/N=8dB
LO Leakage			-70	dBm	
RSSI DC Output Range		0.4 to 1.5		V	R_L=24kΩ
RSSI Sensitivity		13		mV/dB	MUTE = 0
RSSI Dynamic Range		60		dB	MUTE = 0
LNA					
Power Gain		18		dB	433MHz, Matched to 50Ω
		16		dB	915MHz, Matched to 50Ω
Noise Figure		3.6		dB	433MHz
		3.7		dB	915MHz
Input IP_3		-8		dBm	915 MHz
Input P_{1dB}		-15		dBm	915 MHz
RX IN Impedance		82-j86		Ω	433MHz (see Plots)
		77-j43		Ω	915MHz (see Plots)
Output Impedance		Open Collector		Ω	
Mixer					Single-ended configuration
Conversion Power Gain		15		dB	433MHz, Matched to 50Ω
		7.5		dB	915MHz, Matched to 50Ω
Noise Figure (SSB)		17		dB	433MHz, SSB Measurement
		17		dB	915MHz, SSB Measurement
Input IP_3		-20		dBm	433MHz
Input IP_3		-15		dBm	915MHz
Input P_{1dB}		-30		dBm	433MHz
Input P_{1dB}		-26		dBm	915MHz
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	

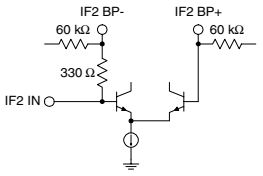
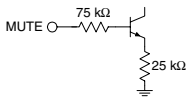
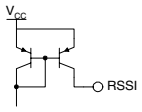
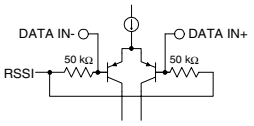
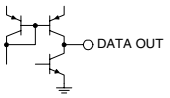
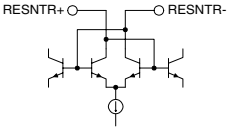
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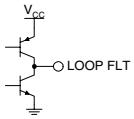
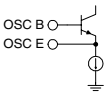
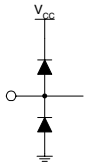
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz, internal to demod
Noise Figure		13		dB	
Input IP_3				mV_{PP}	
IF2 Input Impedance		330		Ω	
Data Output Impedance		6.3 - j25.7		kΩ	
Data Output Bandwidth		500		kHz	Z_{LOAD}=1MΩ ll 3pF; 3dB BW dependent on IF BW
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ll 3pF; Output voltage is proportional with the instantaneous frequency deviation.
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25			kΩ	
Turn On Time		4		ms	f_{XTAL}=14.318MHz. Dependent on configuration.
Turn Off Time		4		ms	
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption	8	10	12	mA	RX Mode
			1	μA	Power Down Mode

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Pin	Function	Description	Interface Schematic
1	VCC1	This pin is used to supply DC bias to the receiver RF circuits. An RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
2	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance when enabled. RX IN is a high impedance when the receiver is disabled.	
3	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output.	
5	GND2	GND2 is connection for the 40 dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
6	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
7	GND3	GND3 is the ground connection for the receiver RF mixer.	
8	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
9	IF1 IN-	Balanced IF input to the 40dB limiting amplifier strip. A DC blocking capacitor is required on this input, 10nF is recommended.	
10	IF1 IN+	Functionally the same as pin 9 except non-inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 9.
11	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is recommended.	See pin 9.
12	IF1 BP-	See pin 11.	See pin 9.
13	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
14	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is recommended.	
15	GND5	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	

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Pin	Function	Description	Interface Schematic
16	IF2 IN	Inverting input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 16.
18	IF2 BP-	See pin 17.	See pin 16.
19	VCC3	This pin is used is supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
20	MUTE	This pin is used to mute the data output (DATA OUT). MUTE>2.0V turns the DATA OUT signal on. MUTE<1.0V turns the DATA OUT signal off.	
21	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range increases with increasing signal strength.	
22	DATA IN-	The inverting input of the data comparator. The RSSI is fed to this pin via a 50kΩ resistor. This input is available for a data filtering capacitor that provides noise and 2x IF rejection. The value of the capacitor can be calculated by C= 1/(2πF*50kΩ) where F is the desired 3dB bandwidth.	
23	DATA OUT	The data comparator output which contains the modulating data recovered from the RSSI signal. Hysteresis can be added to the comparator by placing a very large (<1MΩ) resistor between pins 23 and 24.The magnitude of the load impedance is intended to be 1MΩ or greater.	
24	DATA IN+	The non-inverting input of the data comparator. The RSSI is fed to this pin via a 50kΩ resistor. This input is available for a large filtering capacitor such that the modulation signal can be filtered out leaving a DC reference signal for the comparator.	See pin 22.
25	RESNTR-	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 26.	
26	RESNTR+	See pin 25.	See pin 25.
27	VCC2	This pin is used is supply DC bias to the VCO, prescaler, and PLL. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
28	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

Pin	Function	Description	Interface Schematic
29	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
30	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 100pF capacitor should be connected between pin 30 and pin 31.	
31	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 100pF capacitor should be connected from this pin to ground.	See pin 30.
32	PD	This pin is used to power up or down the RF2919. A logic high (PWR DWN >2.0 V) powers up the receiver and PLL. A logic low (PWR DWN <1.0 V) powers down circuit to standby mode.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 7-19, 21-24, 27-31.	

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RF2919 Theory of Operation and Application Information

The RF2919 is a part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433MHz/868MHz ISM bands or U.S. 915MHz ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products. The RF2919 realizes a highly integrated, single-conversion ASK/OOK receiver with the addition of a reference crystal, intermediate frequency (IF) filtering, and a few passive components. The LNA (low-noise amplifier) input of the RF2919 is easily matched to a front-end filter or antenna by means of a DC blocking capacitor and reactive components. The receiver local oscillator (LO) is generated by an internalized VCO, PLL and phase discriminator in conjunction with the external reference crystal, loop filter and VCO resonator components. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters, and its -3dB bandwidth of 25MHz also allows it to be used (with lower gain) at higher frequencies with other types of filters.

OPERATION

The ASK/OOK demodulation is accomplished by an on-chip data comparator. The RSSI output is internally routed through 50kΩ resistors to provide the inputs (DATA IN+ and DATA IN-) to the data comparator. Either input may be used as the data input with the other input used as the reference. A shunt capacitor can be added to the data input to provide filtering of noise and the second IF harmonic. The value of the data filtering capacitor is calculated by

$$C = \frac{1}{2\pi F \cdot 50k\Omega}$$

where F is the desired 3dB bandwidth. A large filtering capacitor may be used on the reference input to remove the modulation signal, leaving a DC reference for the comparator. Because this reference filter may have a long time constant, a longer preamble may be required to allow the DC reference to stabilize. The data pattern also affects the stability of the DC reference and the reliability of the received data. Since a string of consecutive data 'ones' (or 'zeroes') will result in a change to the DC reference, a coding scheme such as Manchester should be used to improve data integrity. Hysteresis can be added by placing a resistor between the input and the output.

The DATA OUT pin is only capable of driving rail-to-rail output into a very high impedance and small capacitance, with the amount of capacitance affecting the DATA OUT bandwidth. For a 3pF load, the bandwidth is in excess of 500kHz. The rise and fall times of the RSSI are limited by the bandwidth of the IF filters, thereby limiting the effective data rate.

The RSSI output signal is supplied from a current source and therefore requires a resistor to convert it to a voltage. For a 24kΩ resistive load, the RSSI will typically range from 0.4V to 1.5V (3.6V supply). A small parallel capacitor is suggested to limit the bandwidth and filter noise.

APPLICATION AND LAYOUT CONSIDERATIONS

The RX IN pin is DC biased, requiring a DC blocking capacitor. If the RF filter has DC blocking characteristics, such as a ceramic dielectric filter, then a DC blocking capacitor is not necessary. When in power down mode, the RX IN impedance increases. Therefore in a half-duplex application, the RF2919 RX IN may share the RF filter with a transmitter output having a similar high impedance power down characteristic. Care must be taken in this case to account for loading effects of the transmitter on the receiver and vice versa in matching the filter to both the transmitter and receiver.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO by either radiation or coupling of traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2919 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible.

When using loop bandwidths lower than the 5kHz shown on the evaluation board, better supply filtering at the resonators (and lower V_{CC} noise as well) will help reduce phase noise of the VCO; a series resistor of 100Ω to 200Ω and a 1μF or larger capacitor can be used. Phase noise is generally more critical in narrowband applications where adjacent channel selectivity is a concern, but it can also contribute to raising the noise floor of the receiver, thereby degrading sensitivity.

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For the interface between the LNA and mixer, the coupling capacitor should be as close to the RF2919 pins as possible with the bias inductor being further away. Once again, the value of the inductor can be changed to compensate for trace inductance. The output impedance of the LNA is on the order of several kΩ which makes matching to 50Ω difficult. If image filtering is desired, a high impedance filter is recommended. If no filtering is used, the match to the mixer input need not be a good conjugate match due to the high gain of the IF amplifier stages. In fact, a conjugate match between the LNA and mixer will not significantly improve sensitivity, but will have an adverse effect on system IIP3 and increase the likelihood of IF instability.

Predicting and Minimizing PLL Lock Time

The RF2919 implements a conventional PLL on chip. The VCO is followed by a prescaler, which divides down the output frequency for comparison with the reference oscillator frequency. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF2919 is:

$$LockTime = \frac{D}{F_C} + 35000 \cdot C \cdot dV$$

where D is a factor to account for the loop damping, F_C is the loop cut frequency, C is the sum of all shunt capacitors in the loop filter, and dV is the required step voltage change to produce the desired frequency change during the transient. For loops with low phase margin (30° to 40°), use D=2 whereas for loops with better phase margin (50° to 60°), use D=1.

To lock faster, C needs to be minimized.

1. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.

2. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

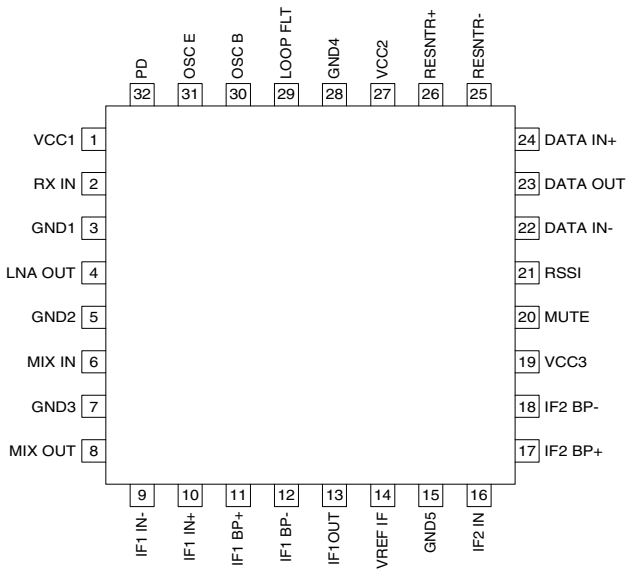
For additional applications information, refer to the following technical articles.

TA0031 "Frequency Synthesis Using the RF2510"

DK1000 "ASK Transmit and Receive Chip Set"

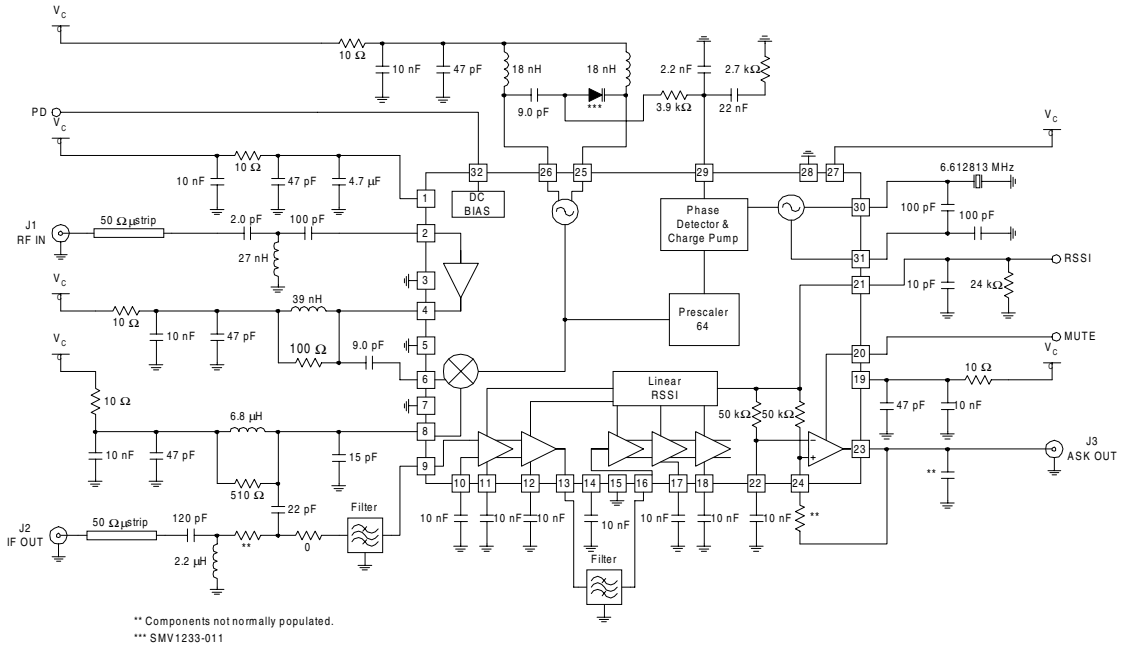
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Pin Out



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Application Schematic
433MHz

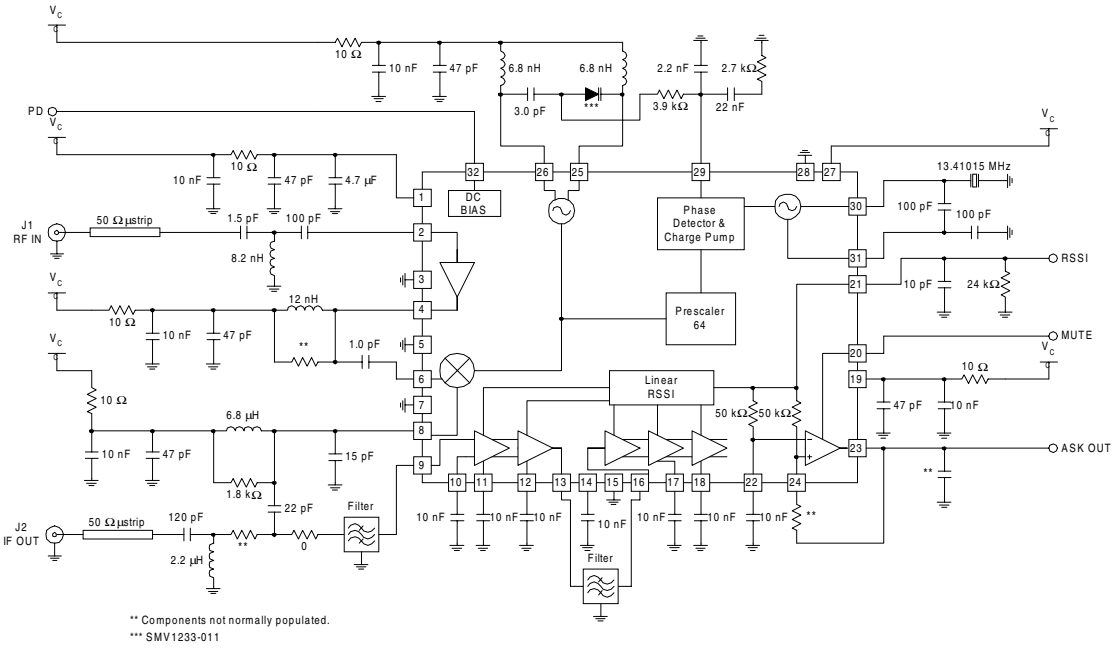


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TRANSCEIVERS

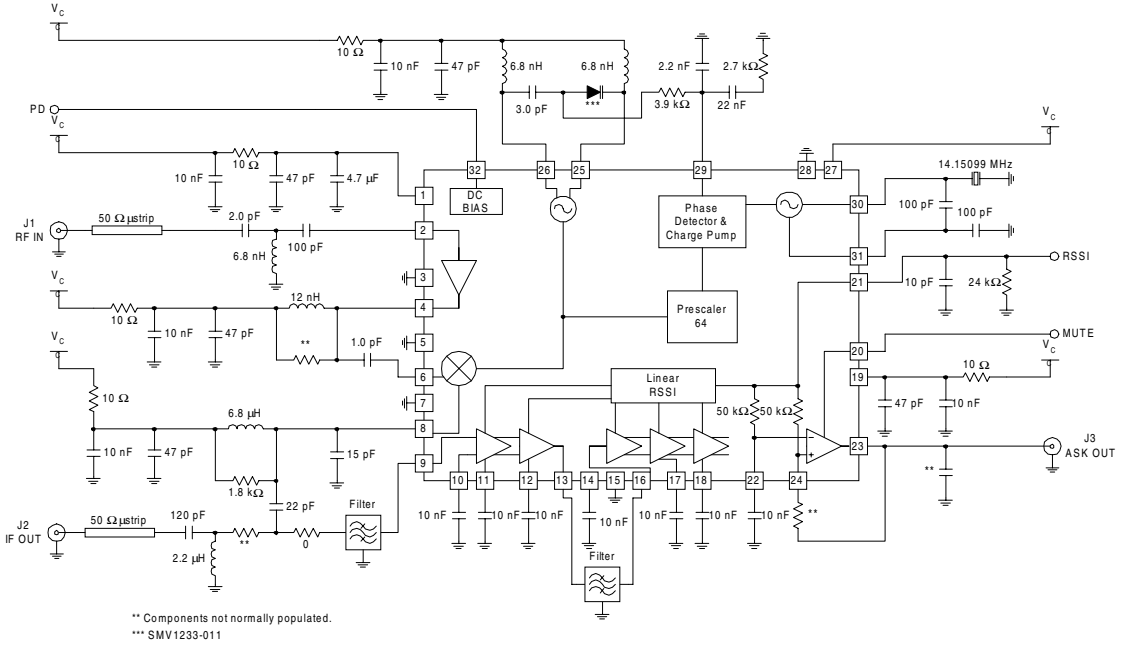
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Application Schematic
868MHz



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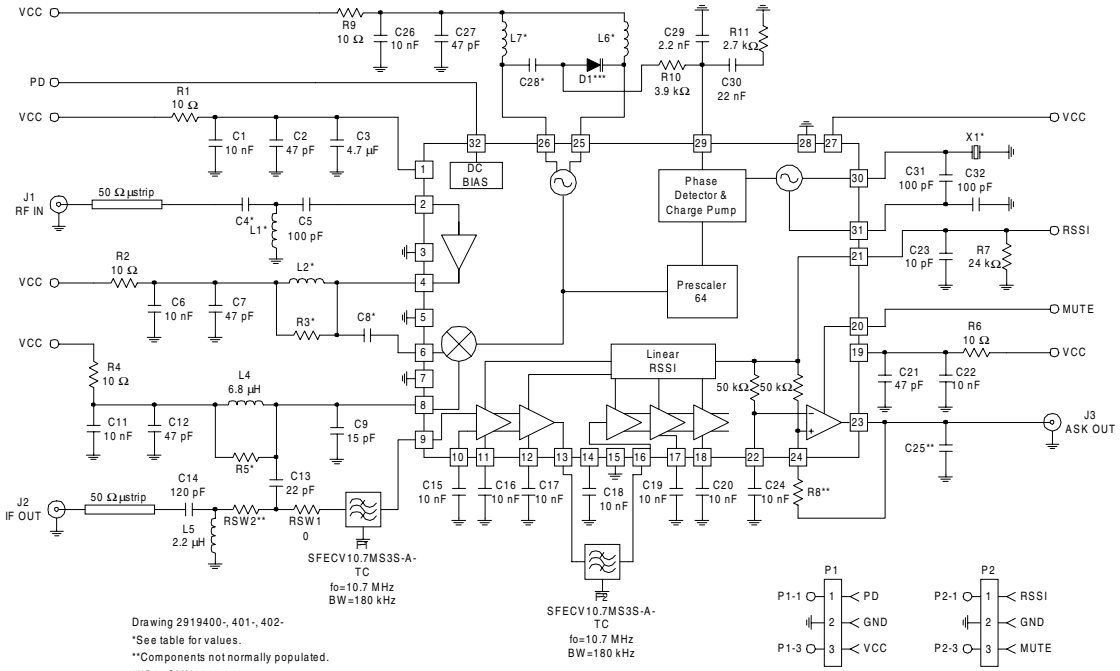
Application Schematic
915MHz



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Evaluation Board Schematic
H (915MHz), M (868MHz), L (433MHz) Boards

(Download Bill of Materials from www.rfmd.com.)



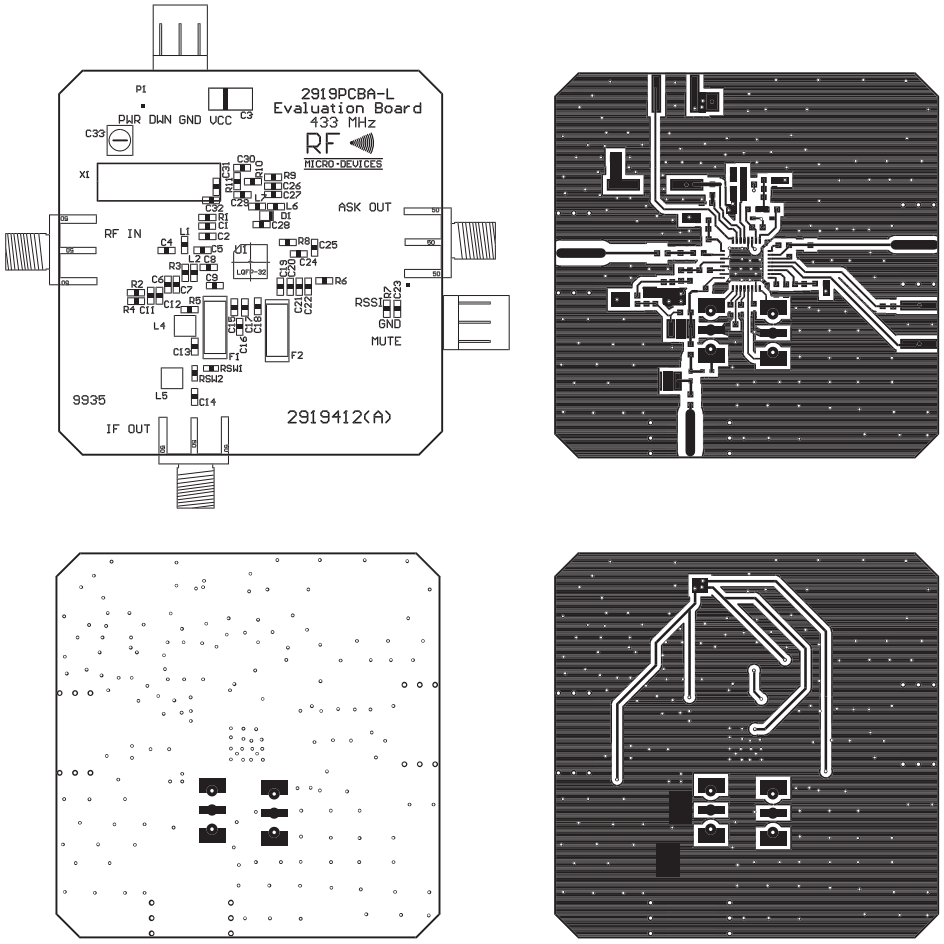
Drawing 2919400-, 401-, 402-
*See table for values.
**Components not normally populated.
***D1 : SMV1233-011

Board	C4 (pF)	L1 (nH)	L2 (nH)	C8 (pF)	L6 (nH)	L7 (nH)	C28 (pF)	X1 (MHz)	R3 (Ω)	R5 (Ω)
L (433MHz)	2.0	27	39	9.0	18	18	9.0	6.612813	100	510
M (868MHz)	1.5	8.2	12	1.0	6.8	6.8	3.0	13.41015	**	1.8 k
H (915MHz)	2.0	6.8	12	1.0	6.8	6.8	3.0	14.15099	**	1.8 k

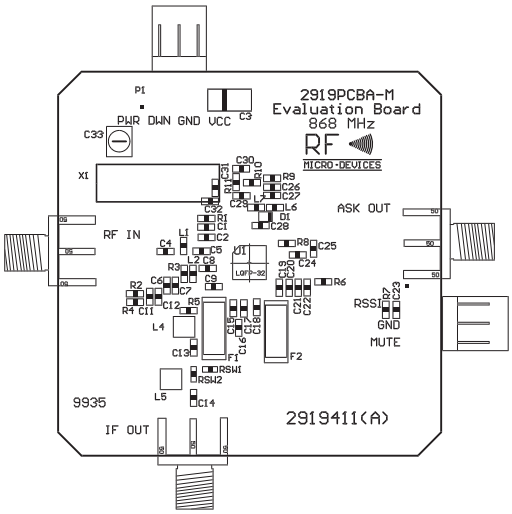
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Evaluation Board Layout - 433MHz
Board Size 2.0” x 2.0”

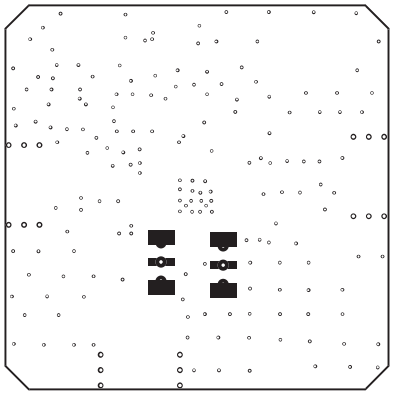
Board Thickness 0.040”, Board Material FR-4, Multi-Layer



Evaluation Board Layout - 868MHz

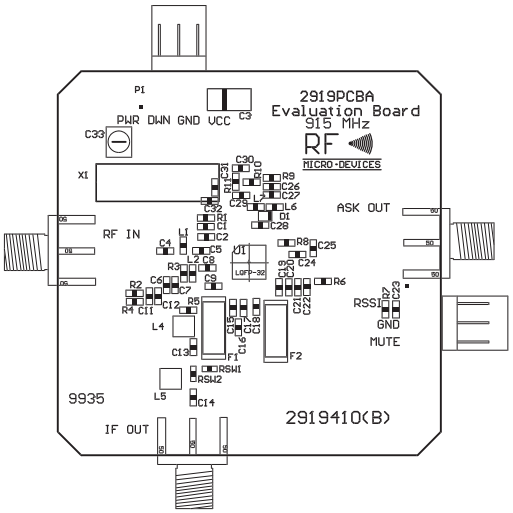




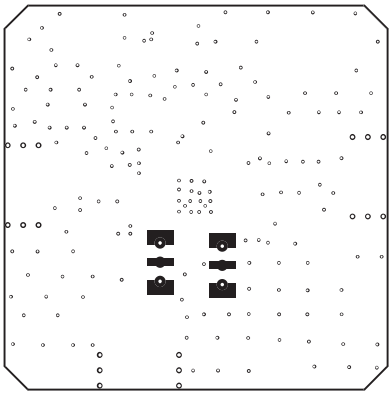




Evaluation Board Layout - 915MHz

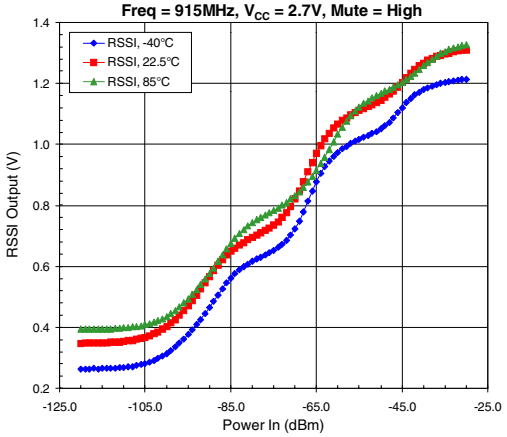




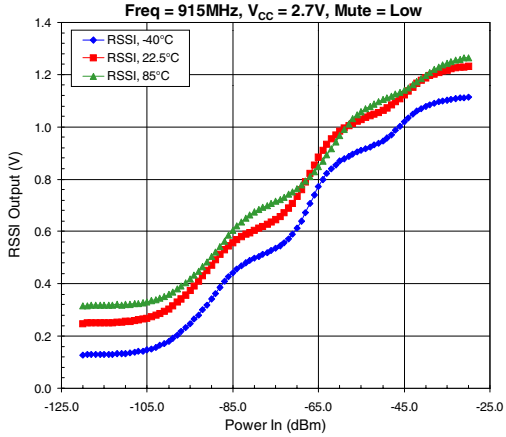




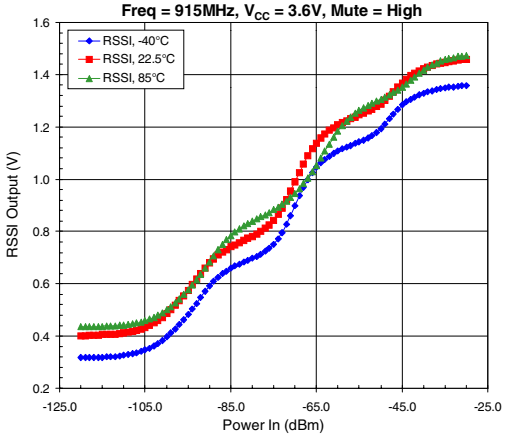
RSSI
Freq = 915MHz, V_{CC} = 2.7V, Mute = High



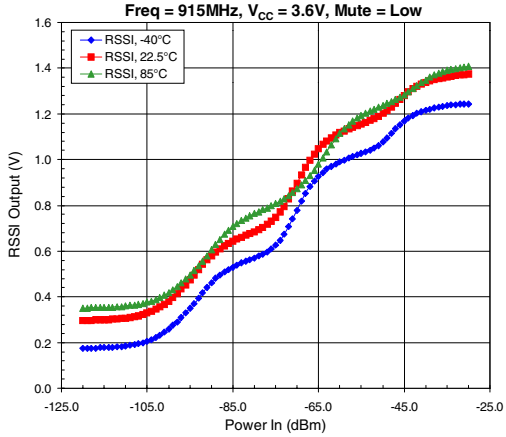
RSSI
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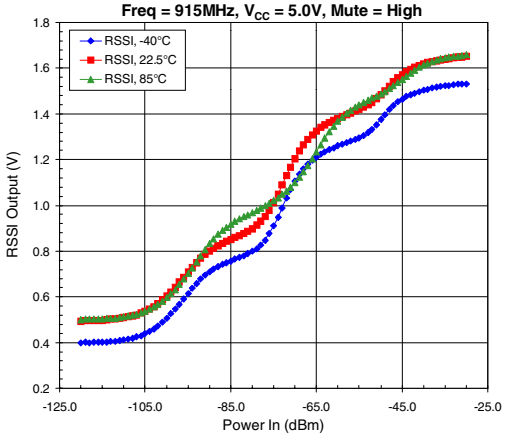
RSSI
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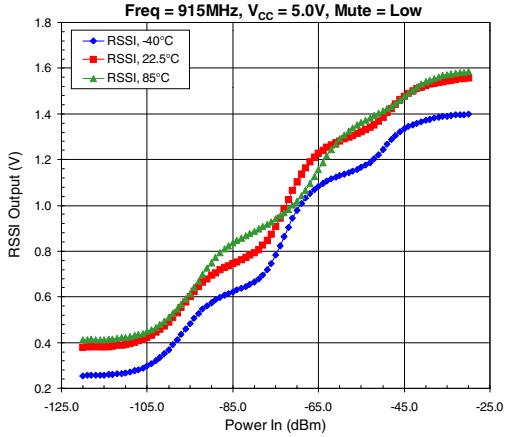
RSSI
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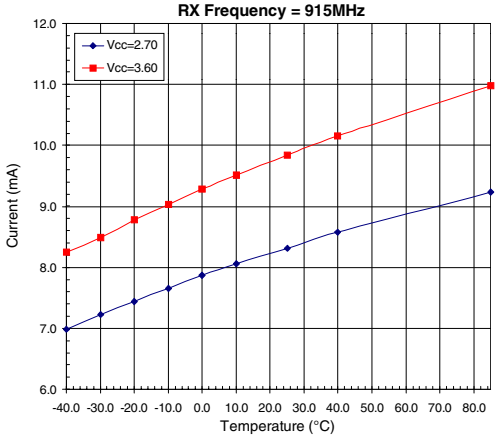
RSSI
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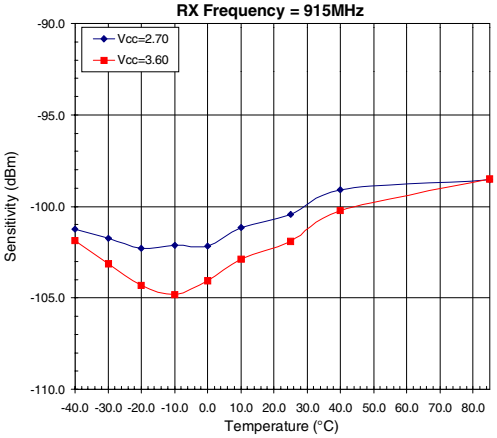
RSSI
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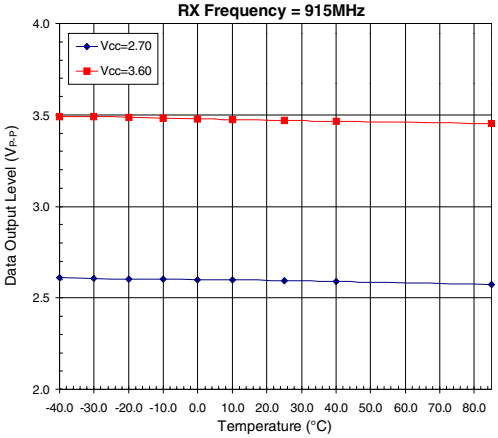
Current versus Temperature
RX Frequency = 915MHz



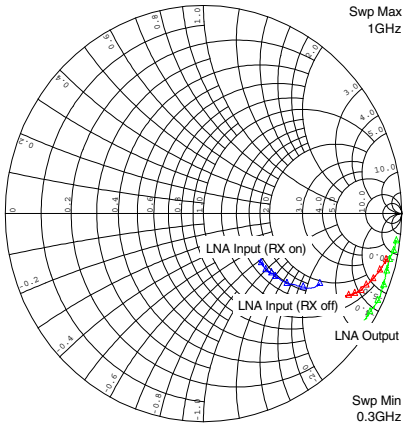
Sensitivity versus Temperature
RX Frequency = 915MHz



Data Output Level versus Temperature
RX Frequency = 915MHz



LNA Impedance



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MICRO·DEVICES

Preliminary

RF2925

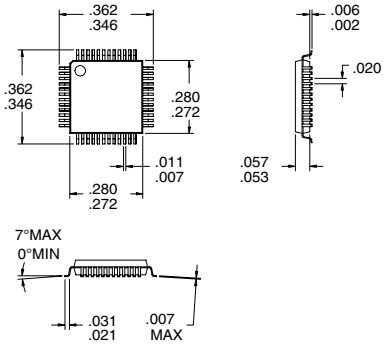
433/868/915MHZ FM/FSK/ASK/OOK TRANSCEIVER

Typical Applications

- Wireless Meter Reading
- TDD Systems
- 433/868/915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

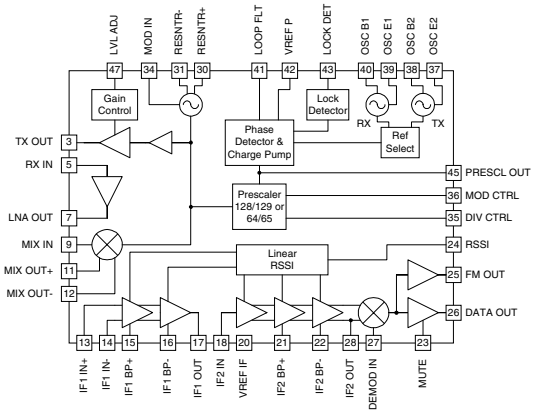
The RF2925 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 48-lead plastic LQFP packaging and is designed to provide a fully functional FM transceiver. The chip is intended for linear (AM, FM) or digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433MHz and 868MHz ISM bands. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) prescaler, and reference oscillators require only the addition of an external crystal to provide a complete phase-locked oscillator. The RF2925 differs from the RF2905 in that both reference oscillators are always on when the PLL is enabled which decreases start-up time when switching between transmit and receive oscillators.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Transceiver
- Fast Switching from Transmit to Receive
- Narrow Band and Wide Band FM/FSK
- 300MHz to 1000MHz Frequency Range
- 2.7V to 5.0V Supply Voltage
- 10mW Output Power at 433MHz

Ordering Information

RF2925	433/868/915MHz FM/FSK/ASK/OOK Transceiver
RF2925 PCBA-L	Fully Assembled Evaluation Board (433MHz)
RF2925 PCBA-M	Fully Assembled Evaluation Board (868MHz)
RF2925 PCBA-H	Fully Assembled Evaluation Board (915MHz)

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

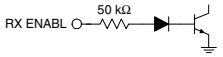
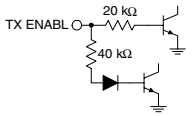
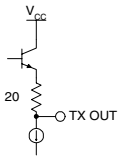
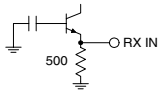
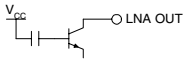
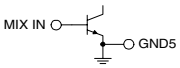
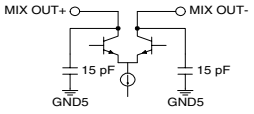
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=433MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
Prescaler divide ratio		64/65 or 128/129			
Prescaler Output Impedance		50		Ω	
PLL Phase Noise		-80		dBc/Hz	Freq=915MHz, 10kHz Offset
		-100		dBc/Hz	Freq=915MHz, 100kHz Offset
Reference Frequency			17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current		40		µA	Source and sink current
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+10		dBm	Freq=433MHz
		+3		dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage
Antenna Port Impedance		50		Ω	TX ENABL="1". RX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity		-101		dBm	IF BW=180kHz, Freq=433MHz, S/N=8dB
LO Leakage			-70	dBm	
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		25		mV/dB	
RSSI Dynamic Range	70	80		dB	

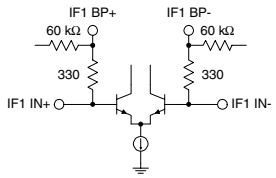
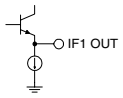
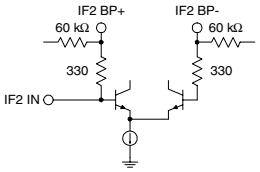
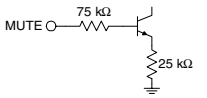
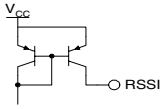
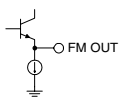
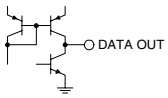
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1". TX ENABL="0"
Antenna Port VSWR			1.5:1		Freq=433MHz, RX Mode
Output Impedance		Open Collector		Ω	433MHz
		Open Collector		Ω	915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		10		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
Maximum Output Voltage				V_{PP}	Balanced
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330MΩ
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin
Demod Input Impedance		10		kΩ	
FM Output Impedance		500		Ω	
Data Output Impedance		>1		MΩ	
FM Output Bandwidth	500			kHz	3dB Bandwidth, Dependent upon IF bandwidth and Discriminator.
Data Output Bandwidth	500			kHz	3dB Bandwidth, Z_{LOAD}=1MΩ ‖ 3pF; Dependent upon IF bandwidth and Discriminator.
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ‖ 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	Z_{LOAD}>10kΩ
FM Output AC Level		200		mV_{PP}	Z_{LOAD}>10kΩ

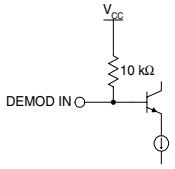
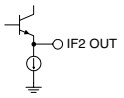
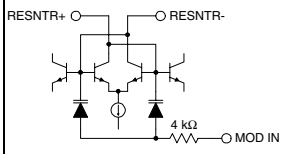
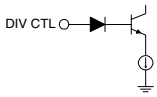
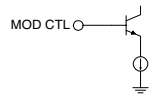
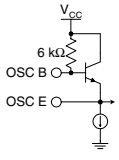
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25			kΩ	
Turn On Time			4	ms	Reference Crystal=7.075MHz
Turn Off Time			4	ms	Dependent upon reference crystal. Higher frequencies reduce turn on/off times.
RX to TX and TX to RX Time			100	µs	Dependent upon loop bandwidth.
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		25		mA	TX Mode, LVL ADJ=3.6V
		10		mA	TX Mode, LVL ADJ=0V
		9		mA	RX Mode
			1	µA	Power Down Mode
		8		mA	PLL Only Mode

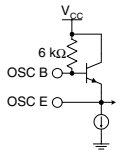
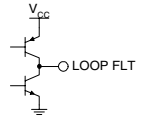
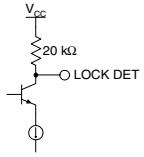
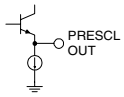
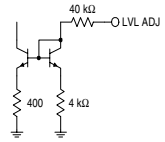
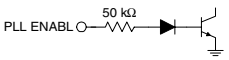
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Pin	Function	Description	Interface Schematic
1	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer. When RX ENABL is high the receive LO frequency is set by reference oscillator 1.	
2	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions. When TX ENABL is high the transmit frequency is set by reference oscillator 2.	
3	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance (see output impedance plot) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
4	GND2	Ground connection for the 40dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
5	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance (see input impedance plot) when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
6	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
7	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output.	
8	GND3	Same as pin 4.	
9	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
10	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
11	MIX OUT+	Complementary (with respect to pin 12) IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
12	MIX OUT-	IF output from the RF mixer. For a balanced mixer output, pull-up inductors from pin 11 and 12 to V_{CC} and a capacitor between the pins should be used. The sum of the total pull-up inductance should be used to resonate the capacitor between pins 11 and 12. DC blocking capacitors of 10nF can then be used to connect the balanced output to IF1 IN+ (pin 13) and IF1 IN- (pin 14).	See pin 11.

Pin	Function	Description	Interface Schematic
13	IF1 IN+	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
14	IF1 IN-	Functionally the same as pin 13 except inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 13.
15	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
16	IF1 BP-	Same as pin 15.	See pin 13.
17	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 IN	Balanced IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
19	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
20	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	
21	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 18.
22	IF2 BP-	Same as pin 21.	See pin 18.
23	MUTE	This pin is used to mute the data output (DATA OUT). MUTE>2.0V turns the DATA OUT signal on. MUTE<1.0V turns the DATA OUT signal off. The MUTE signal should be logic low in the Sleep Mode.	
24	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.5V and increases with increasing signal strength.	
25	FM OUT	Linear output from the FM demodulator. This pin is used in analog applications when signal fidelity is important. This output is inverted for low side injection of the LO and normal for high side injection.	
26	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater. When using a RF2905 transmitter and receiver back to back, a data inversion will occur, when the LO is low side injected. A high side injection will add an inversion of the Rx data.	

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Pin	Function	Description	Interface Schematic
27	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
28	IF2 OUT	Balanced IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 27 through a 5pF capacitor and an FM discriminator circuit.	
29	VCC6	This pin is used is supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
30	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 31 although a small imbalance can be used to tune in the proper frequency range.	
31	RESNTR-	See RESNTR+ description.	See pin 30.
32	VCC2	This pin is used is supply DC bias to the VCO, prescaler, and PLL. An RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
33	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	
34	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to V_{CC} is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 30.
35	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic high (DIV CTRL>2.0V) selects the 64/65 divisor. A logic low (DIV CTRL<1.0V) selects the 128/129 divisor.	
36	MOD CTRL	This pin is used to select the prescaler modulus. A logic high (MOD CTRL>2.0V) selects 64 or 128 for the prescalar divisor. A logic low (MOD CTRL<1.0V) selects 65 or 129 for the prescaler divisor. Due to design timing constraints, the prescaler in the divide by 65 or 129 modes has a limited frequency range for accurate operation. These two modes are not recommended for use from 400MHz to 460MHz.	
37	OSC E2	Oscillator emitter. See pin 1 description.	See pin 38.
38	OSC B2	Oscillator base. The application schematic shows a typical Colpitts oscillator circuit. This pin may be driven by an external source. If so, it should be AC coupled using a capacitor. The level should be about 500mV$_{PP}$	

Pin	Function	Description	Interface Schematic
39	OSC E1	Oscillator emitter. See pin 1 description.	See pin 40.
40	OSC B1	Oscillator base. The application schematic shows a typical Colpitts oscillator circuit. This pin may be driven by an external source. If so, it should be AC coupled using a capacitor. The level should be about 500mV$_{PP}$	
41	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
42	VREF P	Bypass pin for the prescaler reference voltage. A 33nF capacitor to ground is needed to suppress reference spurs in the device. This value may be different for different PCB arrangements.	
43	LOCK DET	This pin provides an analog output indicating the lock status of the PLL. The amplitude of this signal is typically 200mV$_{PP}$ around a DC level of V_{CC}-0.1V.	
44	VCC1	This pin is used to supply DC bias to the receiver RF electronics. An RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
45	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
46	VCC3	This pin is used to supply DC bias to the transmitter PA. An RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
47	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp is also reduced with output power. This pin MUST be low when the transmitter is disabled.	
48	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	

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RF2925 Theory of Operation and Application Information

The RF2925 is a part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433/868MHz ISM bands or 915MHz US ISM band.This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products.

In its basic form, the RF2925 can implement a two-way half duplex FSK transceiver with the addition of some crystals, filters, and passive components. There are two reference crystals that allow for the transmit carrier and the receiver LO to be independently generated with a common PLL and VCO. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters but has a -3dB bandwidth of 25MHz and can still be used (with lower gain) at higher frequency with the other type of filters. The PA output and LNA input are available on separate pins and are designed to be connected together through a DC blocking capacitor. In the Transmit mode, the PA will have a 50Ω impedance and the LNA will be a high impedance. In Receive mode, the LNA will have a 50Ω interface and the PA will have a high impedance. This eliminates the need for a TX/RX switch and allows a single RF filter to be used in transmit and receive modes. Separate access to the PA and LNA allow the RF2925 to interface with external components such as higher power PA's, lower NF LNA's, upconverters, and downconverters for a variety of implementations.

FM/FSK SYSTEMS

The MOD IN pin drives an internal varactor for modulating the VCO. This pin can be driven with a voltage level needed to generate the desired deviation. This voltage can be carried on a DC bias to select the desired slope (deviation/volt) for FM systems. Or, a resistor divider network referenced to Vcc or ground can divide down logic level signals to the appropriate level for a desired deviation in FSK systems.

On the receiver demod, two outputs are available, an analog FM output and a digital FSK output. The FM output is a buffered signal coming off of the quadrature demodulator. The digital output is generated by a data slicer that is DC coupled differentially to the demodulator. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesired 2xIF product. This balanced data slicer has a speed advantage over a conventional adaptive data slicer where a large capacitor is used to provide DC reference for bit decision. Since the balanced data slicer does not have to charge a large capacitor, the RF2925 exhibits a very fast response time. For best operation of the on-chip data slicer, FM deviation needs to exceed the carrier frequency error anticipated between the receiver and transmitter with margin.

The data slicer itself is a transconductance amp and the DATA OUT pin is capable of driving rail to rail output only into a very high impedance and small capacitance. The amount of capacitance will determine the bandwidth of the DATA OUT. At a 3pF load, the bandwidth is in excess of 500kHz. The rail to rail output of the data slicer is also limited by the frequency deviation and bandwidth of the IF filters. With the 180kHz bandwidth filters on the eval boards, the rail to rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation vs. data rate (mod index) is important in evaluating the applicability of the RF2925 for a given data rate.

While this type of data slicer is best for wideband deviation, it can also work for narrowband if care is taken to minimize frequency differences. By loading down the DATA OUT pin, the output will be limited to a small data signal on a DC carrier. With this signal, an external data slicer can be used to achieve higher data rates or improve performance in narrow deviations. Alternatively, an AFC loop can be added to correct for frequency errors with a few external components.

For FM or FSK modulation, an internal varactor is used to directly modulate the VCO with the baseband data. The primary consideration when directly modulating the VCO is the data rate verses PLL loop bandwidth. The PLL will track out the modulation to the extent of its loop bandwidth which distorts the modulating data. Therefore, the lower frequency components of the modulating data should be 5 to 10 times the loop bandwidth to minimize the distortion. The lower frequency components are generated by long strings of 1's or 0's in the data stream. By limiting the number of consecutive, same bits, the lower frequency component can be set. In addition, the data stream should be balanced to minimize distortion. Using a coding pattern such as Manchester is highly recommended to optimize system performance.

The PLL loop bandwidth is important in several other system parameters. For example, switching from transmit to receive requires the VCO to retune to another frequency. The switching speed is proportional to the loop bandwidth, the higher the loop bandwidth, the

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faster the switching times. Phase noise of the VCO is another factor. Phase noise outside of the loop bandwidth is due to the noise of the VCO itself rather than the crystal reference. A design trade-off must be made here in selecting a PLL loop bandwidth with acceptable phase noise and switching characteristics and minimal distortion of the modulation data.

AM/ASK SYSTEMS

The transmitter of the RF2925 has an output power level adjustment (LVL ADJ) that can be used to provide approximately 18dB of power control for amplitude modulation. The RSSI output of the receiver section can be used to recover the modulation. The RSSI output is from a current source and needs to have a resistor to convert to a voltage. A 51kΩ resistive load will produce an RSSI voltage of 0.7V to 2.5V, typically. A parallel capacitor is suggested to limit the bandwidth and filter noise. For ASK applications, the 18dB range of the LVL ADJ does not produce enough voltage swing in the RSSI for reliable communication. The On-Off keying (OOK) is suggested to provide reliable communications. To achieve this, both the LVL ADJ and TX ENABL need to be controlled together (please note that LVL ADJ cannot be left high when TX ENABL is low). This will provide a on/off ratio of >50dB. One unfortunate consequence of modulating this way is VCO pulling by the power amp. This results in a spurious output outside the desired transmit band as the PLL momentarily loses lock and reacquires. This can be avoided by pulse shaping the TX data to slow the change in the VCO load to a pace that the PLL can track with its given loop bandwidth. The loop bandwidth can also be increased to allow it to track faster changes due to load pulling.

For the ASK/OOK receiver demodulator, an external data slicer is required. The RSSI output is used to provide both the filtered data and a very low pass filtered (relative to the data rate) DC reference to a data slicer. Because the very low pass filter has a slow time constant, a longer preamble may be required to allow for the DC reference to get to a stable state. Here, as in the case of the FSK transmitter, the data pattern also affects the DC reference and the reliability of the received data. Again, a coding scheme such as Manchester such should be used to improve data integrity.

APPLICATION AND LAYOUT CONSIDERATIONS

Both the RX IN and TX OUT have a DC bias on them. Therefore, DC blocking caps are required. If the RF filter has DC blocking characteristics like a ceramic dielectric filter, then only 1 DC blocking capacitor would be needed to separate the DC of RX IN and TX OUT. These are RF signals and care should be taken to route these signals keeping them physically short. Because of the 50Ω/high impedance nature of these two signals, they may be connected together into a signal 50Ω device such as a filter. An external LNA or PA can be used, if desired, but an external RX/TX switch may be required.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO either radiated or coupled by traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2925 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible. Figure 1 is a recommended layout pattern for the VCO components. When using loop bandwidths lower than the 5kHz shown on the eval board, better filtering of the Vcc at the resonators (and lower Vcc noise as well) will help reduce phase noise of the VCO. A series resistor of 100Ω to 200Ω and a 1μF or larger capacitor can be used.

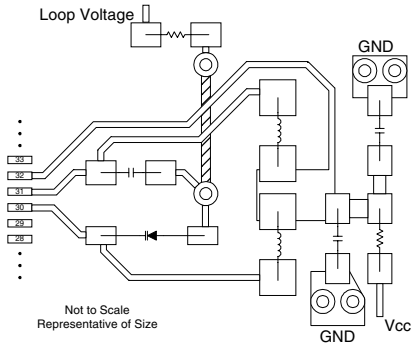


Figure 1. Recommended VCO Layout

For the interface between the LNA/mixer, the coupling capacitor should be as close to the RF2925 pins as possible with the bias inductor being further away. Once again, the value of the inductor can be changed to compensate to trace inductance. The output impedance of the LNA is in the order of several kΩ which makes matching to 50Ω very hard. If image filtering is desired, a high impedance filter is recommended.

The quad tank of the discriminator can be implemented with ceramic discriminators available from a couple of sources. This design works well for wideband applications and where the temperature range is limited. The temperature coefficient of a ceramic discriminator can be in the order of +/- 50ppm per degree C. An automatic frequency control loop can be implemented using the DC level of the FM OUT for feedback to an external varactor on the reference crystal. An alternative to the ceramic discriminator is a LC tank. Figure 2 shows a schematic implementation of a LC tank.

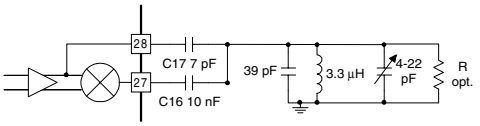


Figure 2. LC Type Discriminator Circuit

The DEMOD IN pin has a DC bias on it and must be DC blocked. This can be done either at the pin or at the ground side of the LC tank (this must also be done if a parallel resistor is used with a ceramic discriminator). The decision whether to used a LC or a ceramic discriminator should be based upon the frequency deviation in the system, discriminator Q needed, and frequency and temperature tolerances. Tuning of the LC tank is required to overcome the component tolerances in the tank.

Predicting and Minimizing PLL Lock Time

The RF2925 implements a conventional PLL on chip, with a VCO followed by a prescalar dividing the output frequency down to be compared with a signal from the reference oscillator. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF2925 is:

$$\text{Lock time} = D/fc + 35000 * C * dV$$

Where D is a factor to account for the loop damping. For loops with low phase margin (30° to 40°), use D=2 whereas for loops with better phase margin (50° to 60°), use D=1. fc is the loop cut frequency. C is the sum of all shunt capacitors in the loop filter. dV is the required step voltage change to produce the desired frequency change during the transient.

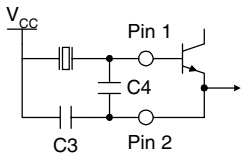
To lock faster, we need to minimize C.

1. To this end, use the divide by 128 rather than the 64, and a correspondingly lower frequency reference crystal to achieve the desired output frequency.
2. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.
3. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

Evaluation Board Crystal Oscillator

Which Topology?
The RF2925 on-board reference oscillator is configured as common collector, internally biased, with the Base and Emitter accessible. This can conveniently be used to implement a Colpitts oscillator with the addition of two external capacitors and a crystal. This allows the used of relatively cheap and readily available crystals, has a minimum parts count and doesn't require the use of inductors.

Colpitts Topology
The basic topology of the Colpitts oscillator used is below:

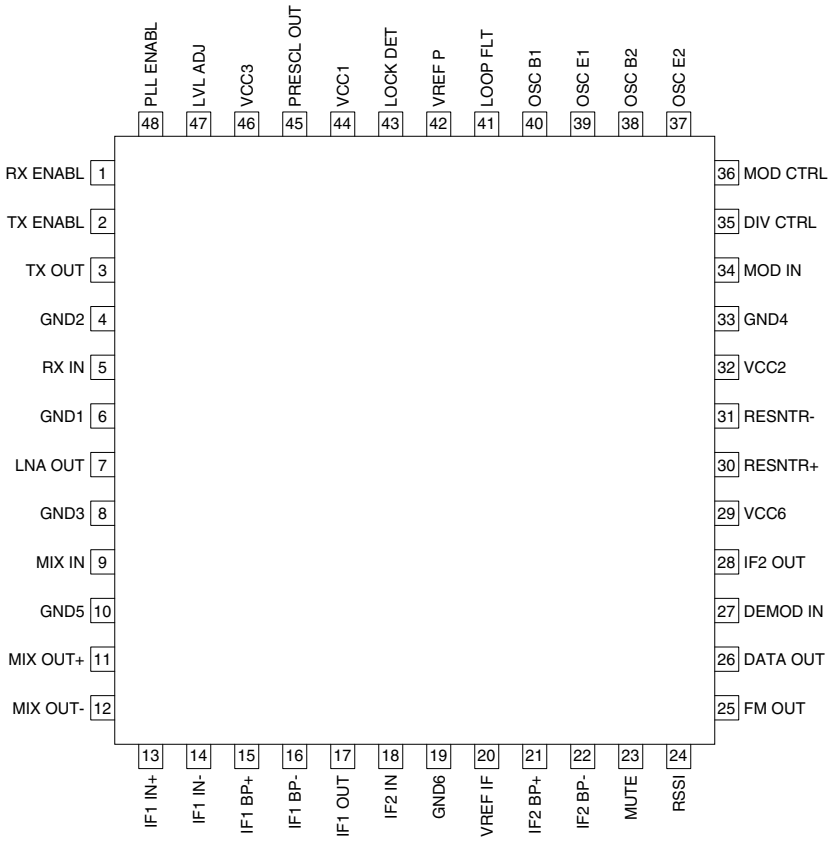


The transmitter is acting as an emitter-follower. The voltage gain is set by capacitors C3 and C4 which are acting as a tapped capacitive impedance transformer.

The maximum loop gain is achieved when C4 has twice the capacitance of C3. C3 in series with C4 determines the load capacitance across the crystal. For a parallel resonant, fundamental mode crystal, the crystal manufacturer will design the crystal for a specific load capacitance where the crystal will meet it's specifications of frequency accuracy, temperature stability, ESR and so forth. Any deviation from the nominal capacitance will pull the oscillation frequency, allowing the frequency to be tuned by placing an adjustable reactance in series with the crystal.

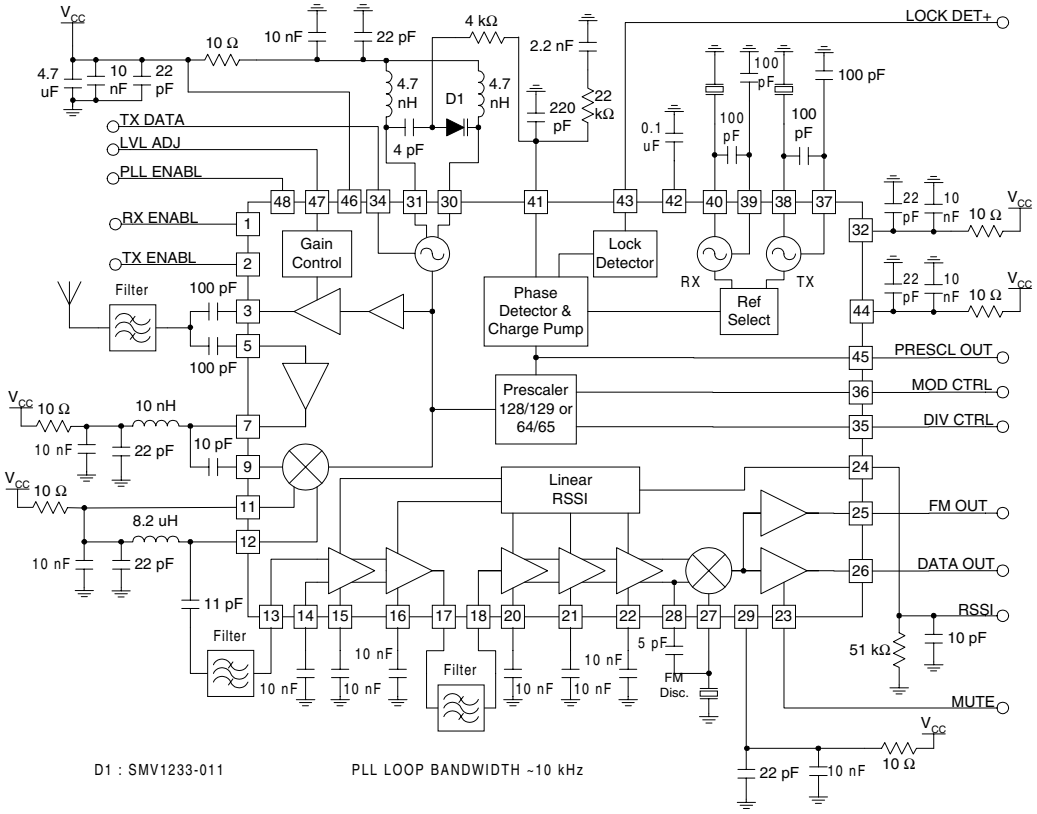
Selection of a Crystal
The most obvious parameter to define is frequency, followed by frequency accuracy under nominal conditions and stability versus temperature. Another key parameter is the resonant mode of the crystal, either series or parallel. Series resonant mode is generally used when the crystal is being operated at an overtone of it's resonant frequency, whereas parallel resonant mode is generally used with fundamental mode operation. Parallel resonant, fundamental mode is preferred as there is a multitude of this type of crystal available to cover the full range of operating frequencies of the RF2925, and it facilitates a simple oscillator topology. In this case "parallel resonant mode" needs to be specified along with nominal load capacitance and series resistance. An optional parameter to specify is pulling sensitivity, in PPM/pF, which defines how sensitive the crystal is to variation in load capacitance. Drive level should also be listed. When comparing crystals from difference vendors, series resistance, frequency accuracy and temperature stability are all good indicators, but there are many other factors to trade off, including cost and packaging.

Pin Out


PLL ENABL 48
LVL ADJ 47
VCC3 46
PRESCL OUT 45
VCC1 44
LOCK DET 43
VREF P 42
LOOP FLT 41
OSC B1 40
OSC E1 39
OSC B2 38
OSC E2 37
RX ENABL 1
TX ENABL 2
TX OUT 3
GND2 4
RX IN 5
GND1 6
LNA OUT 7
GND3 8
MIX IN 9
GND5 10
MIX OUT+ 11
MIX OUT- 12
36 MOD CTRL
35 DIV CTRL
34 MOD IN
33 GND4
32 VCC2
31 RESNTR-
30 RESNTR+
29 VCC6
28 IF2 OUT
27 DEMOD IN
26 DATA OUT
25 FM OUT
13 IF1 IN+
14 IF1 IN-
15 IF1 BP+
16 IF1 BP-
17 IF1 OUT
18 IF2 IN
19 GND6
20 VREF IF
21 IF2 BP+
22 IF2 BP-
23 MUTE
24 RSSI

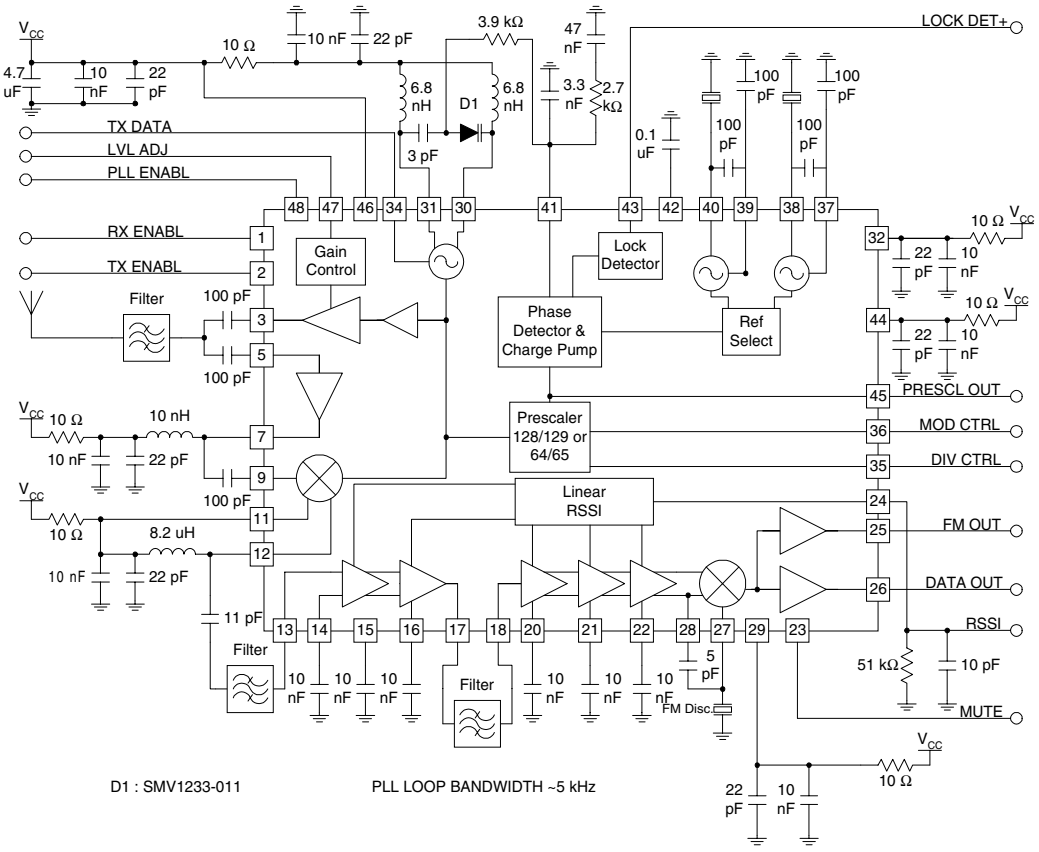
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915 MHz Application Schematic



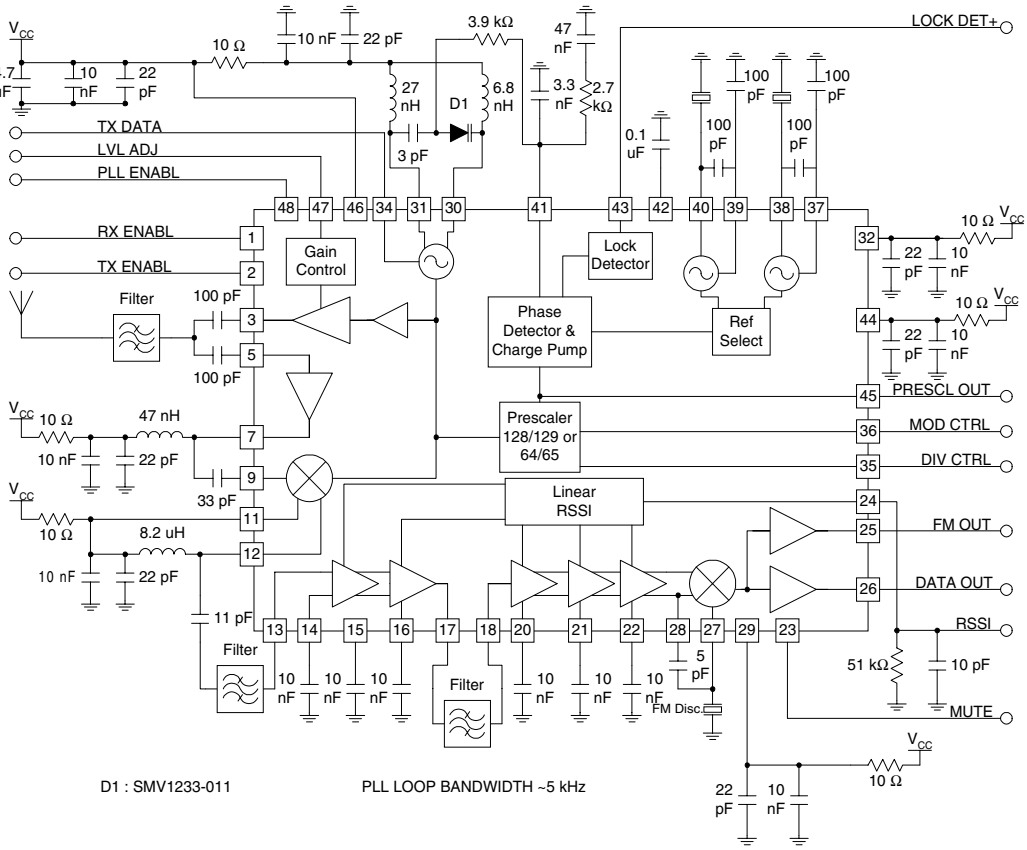
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868 MHz Application Schematic



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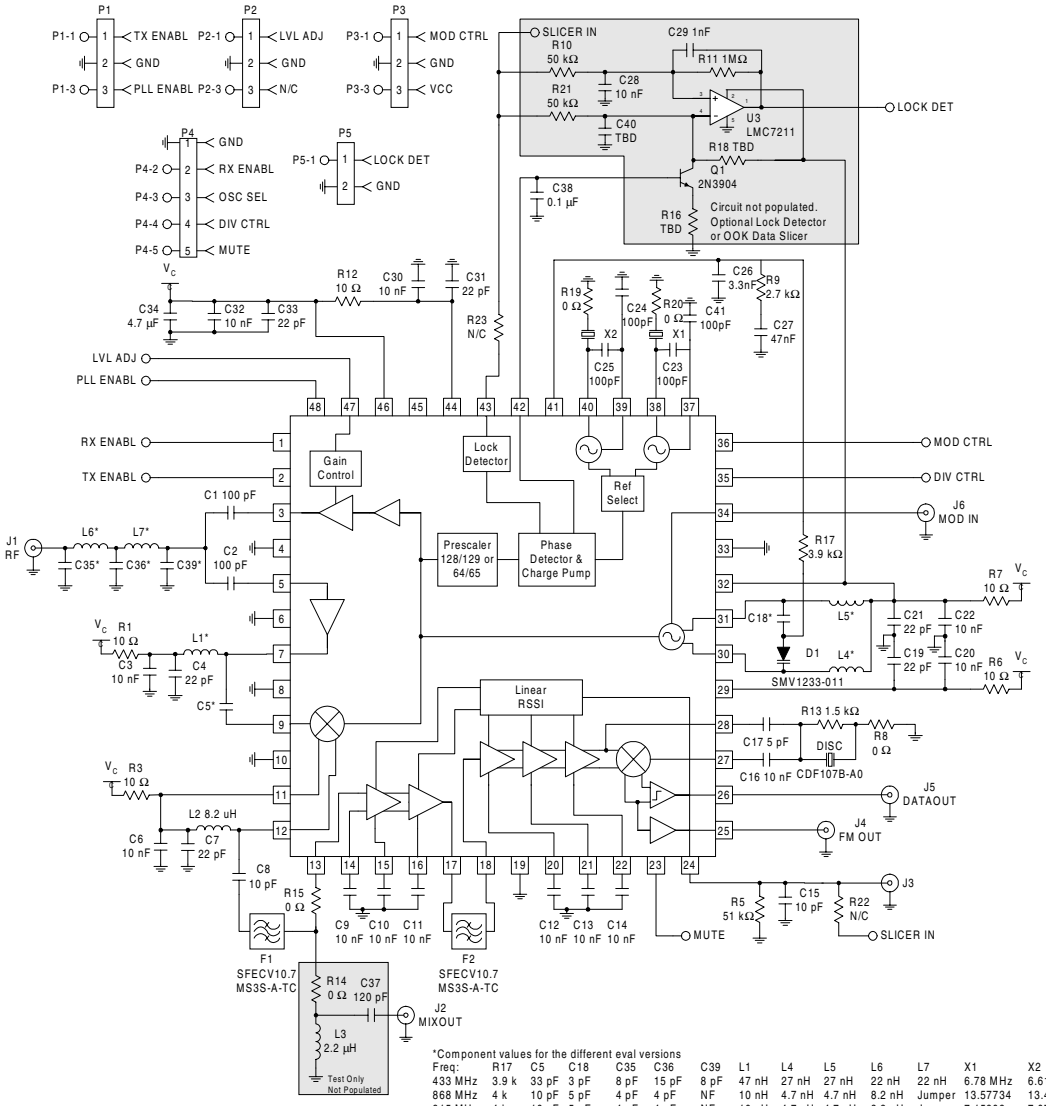
433 MHz Application Schematic



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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



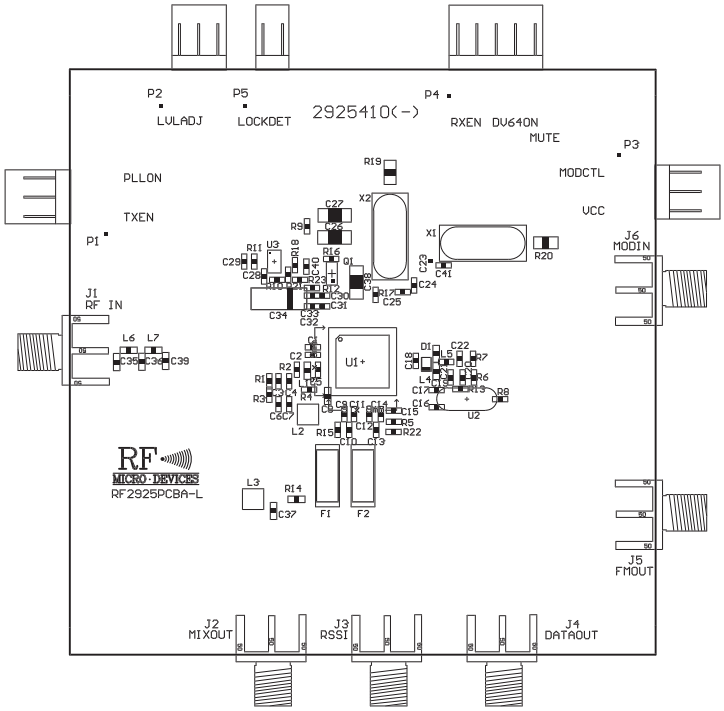
*Component values for the different eval versions

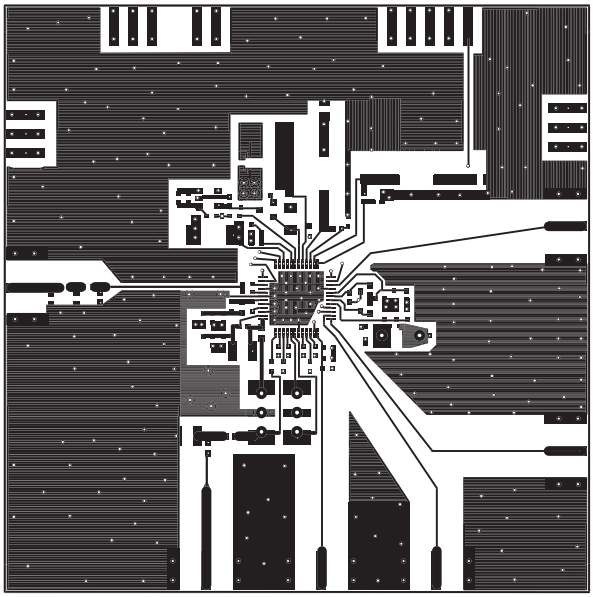
Freq:	R17	C5	C18	C35	C36	C39	L1	L4	L5	L6	L7	X1	X2
433 MHz	3.9 k	33 pF	3 pF	8 pF	15 pF	8 pF	47 nH	27 nH	27 nH	22 nH	22 nH	6.78 MHz	6.612 MHz
868 MHz	4 k	10 pF	5 pF	4 pF	4 pF	NF	10 nH	4.7 nH	4.7 nH	8.2 nH	Jumper	13.57734	13.410156
915 MHz	4 k	10 pF	5 pF	4 pF	4 pF	NF	10 nH	4.7 nH	4.7 nH	8.2 nH	Jumper	7.15909	7.07549

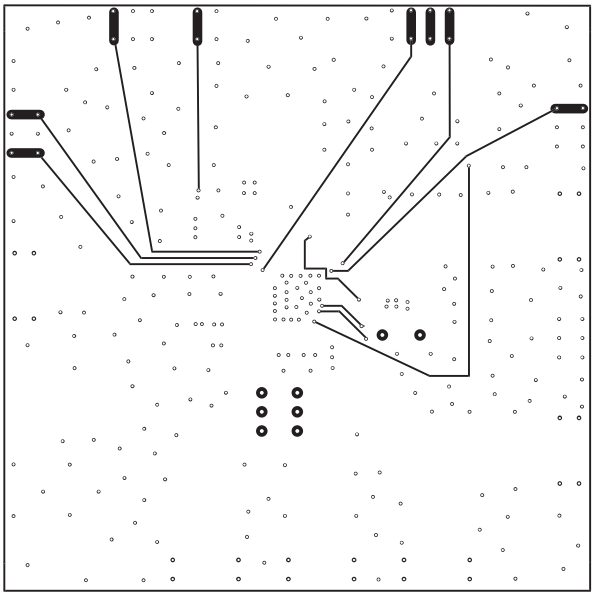
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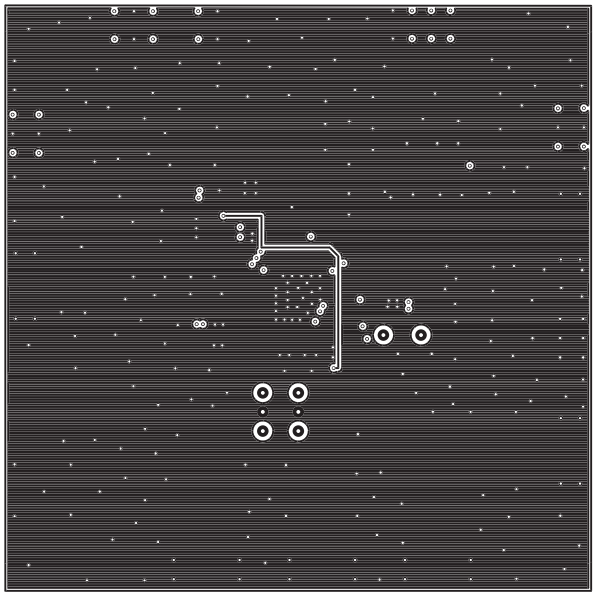
Evaluation Board Layout
Board Size 3.05” x 3.05”

Board Thickness 0.040”, Board Material FR-4, Multi-Layer

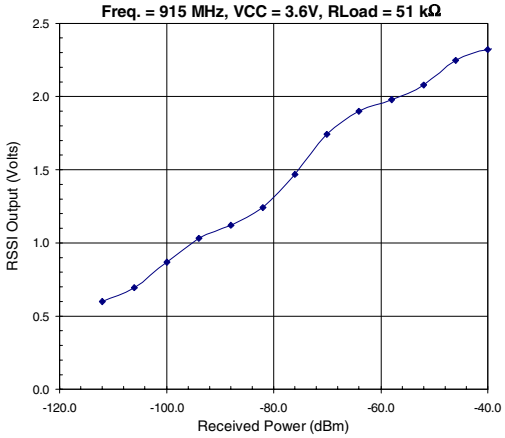




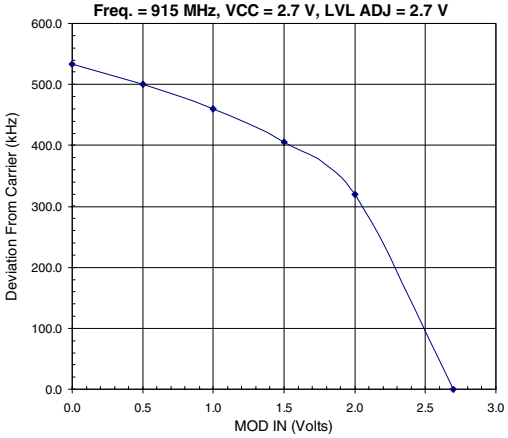




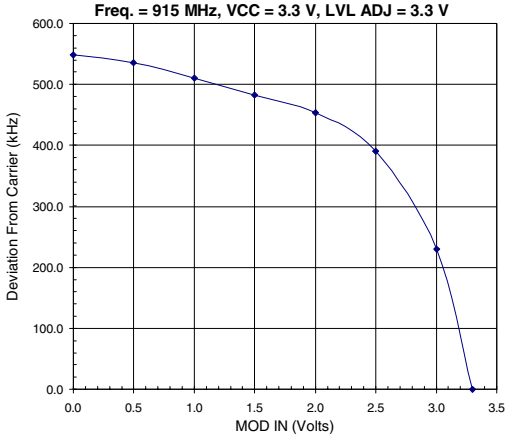
RSSI
Freq. = 915 MHz, VCC = 3.6V, RLoad = 51 kΩ



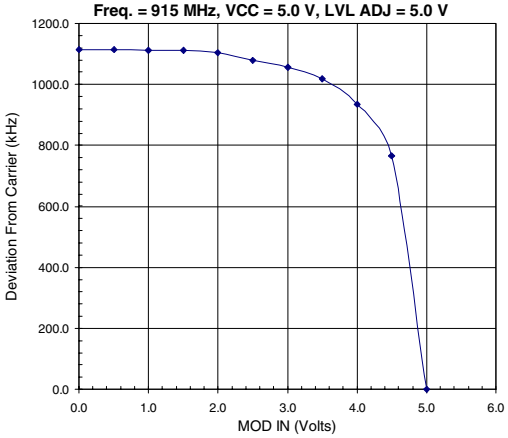
Modulation Deviation
Freq. = 915 MHz, VCC = 2.7 V, LVL ADJ = 2.7 V



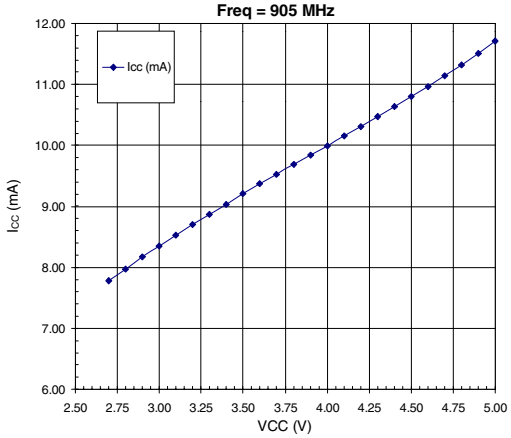
Modulation Deviation
Freq. = 915 MHz, VCC = 3.3 V, LVL ADJ = 3.3 V



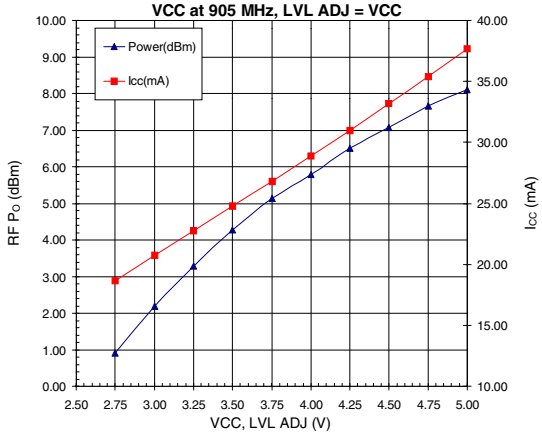
Modulation Deviation
Freq. = 915 MHz, VCC = 5.0 V, LVL ADJ = 5.0 V



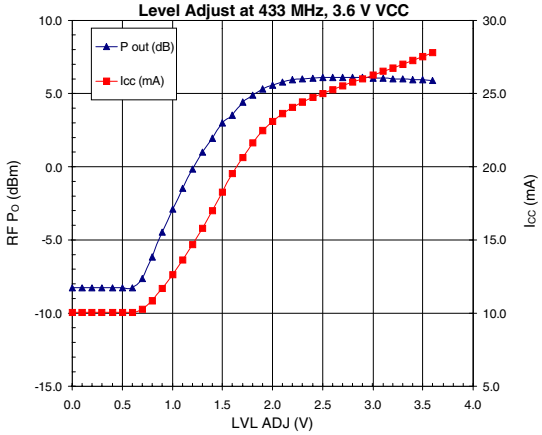
RX Mode Current versus VCC
Freq = 905 MHz



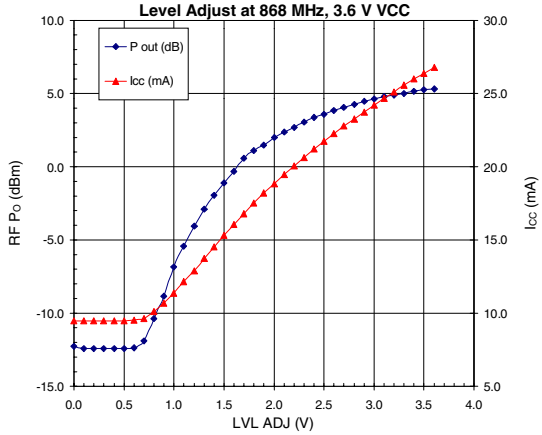
TX Power Output and I_{CC} versus
VCC at 905 MHz, LVL ADJ = VCC



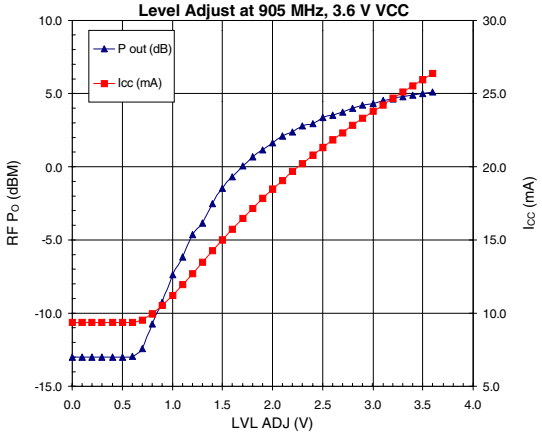
TX Power Output and I_{CC} versus
Level Adjust at 433 MHz, 3.6 V VCC



TX Power Output and I_{CC} versus
Level Adjust at 868 MHz, 3.6 V VCC



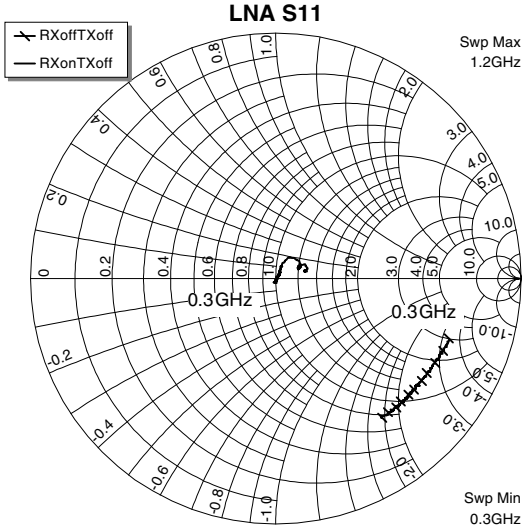
TX Power Output and I_{CC} versus
Level Adjust at 905 MHz, 3.6 V VCC



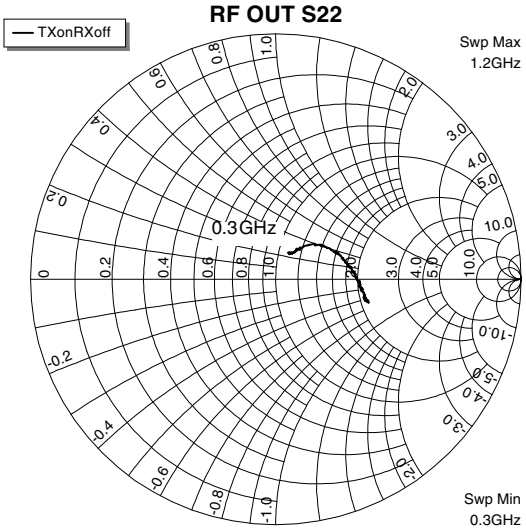
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LNA S11



RF OUT S22



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RF MICRO·DEVICES

Preliminary

RF2926

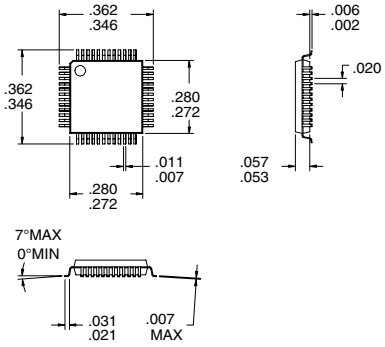
UHF DUAL CONVERSION TRANSCEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

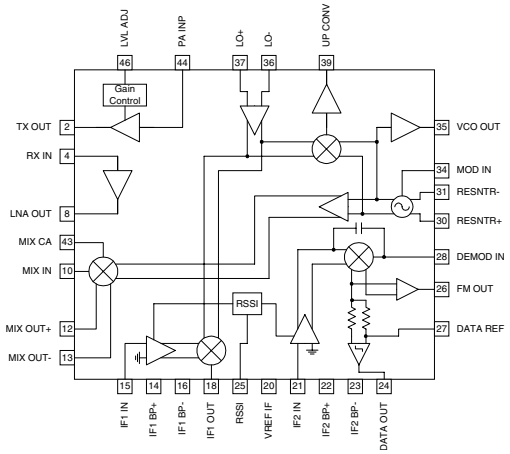
The RF2926 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 48-lead plastic TQFP packaging and is designed to provide a dual conversion, half-duplex transceiver. The chip is intended for linear (AM, FM) or digital (ASK, FSK, OOK) applications in the North American 915MHz and European 433/868MHz ISM bands. The integrated VCO has a buffered output to feed the RF signal back to the PLL IC to form the frequency synthesizer. Separate RX ENABL, TX ENABL, and PLL ENABL lines allow for half duplex operation as well as turning on the VCO to give the synthesizer time to settle and complete power down-mode.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Monolithic Integrated Transceiver
- 2.7V to 5.0V Supply Voltage
- Narrow Band and Wide Band FM/FSK
- 300MHz to 1000MHz Frequency Range
- 130MHz Bandwidth in First IF
- 5mW Output Power at 433MHz

Ordering Information

RF2926	UHF Dual Conversion Transceiver
RF2926 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

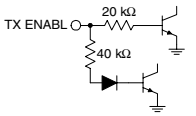
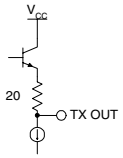
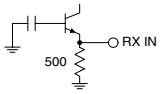
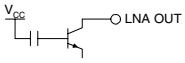
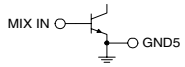
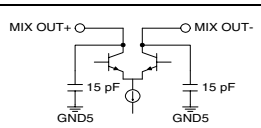
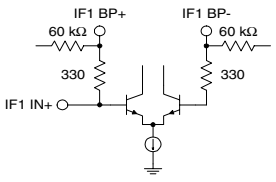
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=433MHz
RF Frequency Range		300 to 1000		MHz	
VCO					
VCO Frequency Range		300 to 1000		MHz	
VCO OUT Level		-18		dBm	50Ω load impedance
VCO OUT Impedance		50		Ω	
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level		+2		dBm	Freq=433MHz
Power Control Range	20			dB	
Power Control Sensitivity		TBD		dB/V	See plot
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage
Antenna Port Impedance		50		Ω	TX ENABL="1"
Antenna Port Impedance		TBD		Ω	TX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics			-50	dBm	Measured on eval board with RF filters in system.
Spurious		TBD		dBc	
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
RX Sensitivity		-99		dBm	IF BW=400kHz, Freq=915MHz, S/N=8dB
RSSI DC Output Range		0.7 to 2.2		V	R_{LOAD}=51kΩ
RSSI Sensitivity		25		mV/dB	See plot
RSSI Dynamic Range	70	80		dB	
LNA and Mixer					
Cascaded Gain		18		dB	Freq=915MHz; RX current 12mA
Cascaded Noise Figure		7		dB	Freq=915MHz; RX current 12mA
Cascaded Input IP_3		-18.5		dBm	Freq=915MHz; RX current 12mA
LO Leakage			-70	dBm	
First IF Section					
IF 3dB Bandwidth		130		MHz	
Voltage Gain		34		dB	IF=110.6MHz, Z_L=330MΩ
Noise Figure		13		dB	
Input IP_3		TBD		mV_{PP}	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	

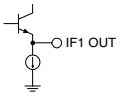
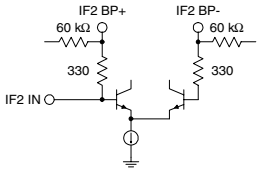
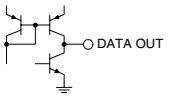
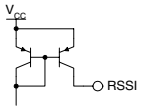
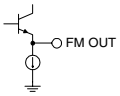
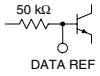
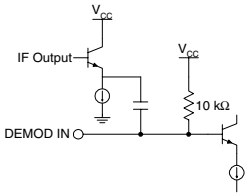
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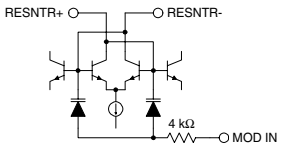
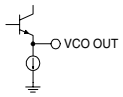
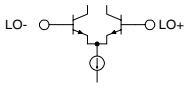
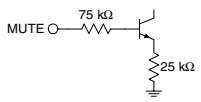
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Second IF Section					
IF Frequency Range	0.1	10.7	22	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT pin
Demod Input Impedance		10		kΩ	
FM Output Impedance		500		Ω	
Data Output Impedance		>1		MΩ	
FM Output Bandwidth		1.6		MHz	
Data Output Bandwidth	1.4			MHz	
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ‖ 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	Z_{LOAD}>10kΩ
FM Output AC Level		200		mV_{PP}	Z_{LOAD}>10kΩ
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		37.3		mA	TX Mode, LVL ADJ=3.6V
		10.9		mA	TX Mode, LVL ADJ=0V
		10 to 18		mA	RX Mode; Current is adjustable
			1	μA	Power Down Mode
		3.8		mA	PLL Only Mode

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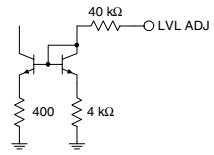
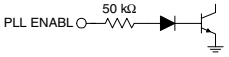
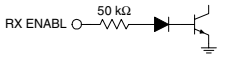
Pin	Function	Description	Interface Schematic
1	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
2	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance (see output impedance plot in Figure TBD) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
3	GND2	Ground connection for the 40 dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance (see input impedance plot in Figure TBD) when the receiver is enabled. RX IN is a high impedance when the receiver is disabled.	
5	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
6	LNA GND	Ground connection for the LNA.	
7	LNA GND	Ground connection for the LNA.	
8	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
9	GND3	Same as pin 4.	
10	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
11	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
12	MIX OUT+	Complementary (with respect to pin 13) IF output from the RF mixer. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
13	MIX OUT-	IF output from the RF mixer. For a balanced mixer output, pull-up inductors from pin 12 and 13 to V_{CC} and a capacitor between the pins should be used. The sum of the total pull-up inductance should be used to resonate the capacitor between pins 12 and 13.	See pin 12.
14	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 16.
15	IF1 IN	IF input to the 40dB limiting amplifier strip. A DC blocking capacitor is required on this input. The value of this capacitor should be small enough as to not attenuate the IF frequency when terminated into the 330Ω input impedance.	

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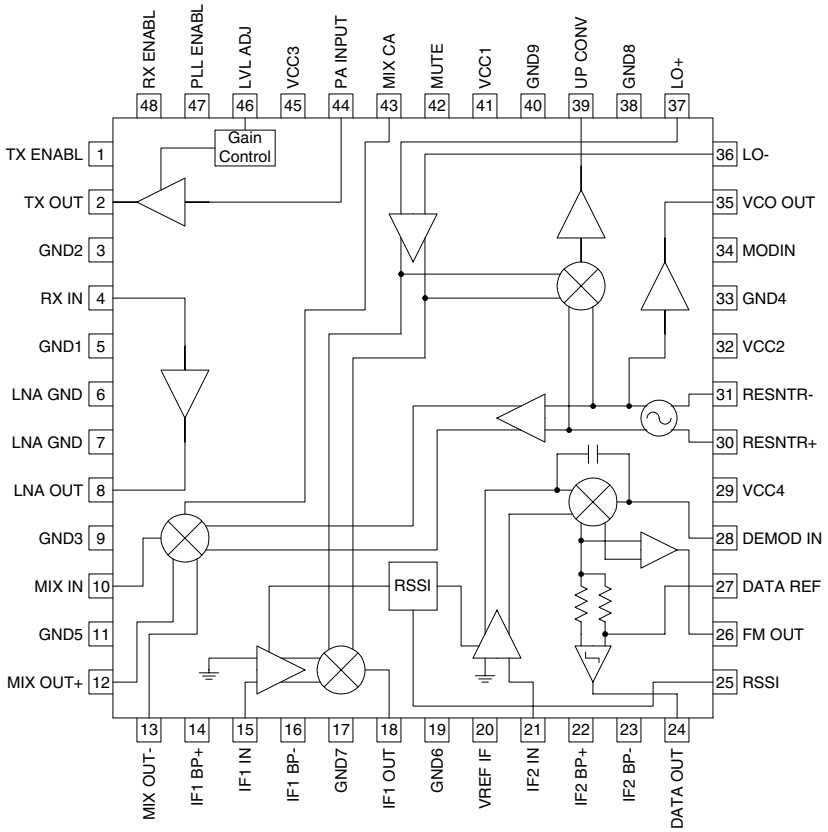
Pin	Function	Description	Interface Schematic
16	IF1 BP-	See pin 14.	See pin 15.
17	GND7	Ground connection for 40dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
18	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330 Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
19	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
20	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	
21	IF2 IN	IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330 Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
22	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 20.
23	IF2 BP-	See pin 21.	See pin 20.
24	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater.	
25	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.5V and increases with increasing signal strength.	
26	FM OUT	Linear output from the FM demodulator. This pin is used in analog applications when signal fidelity is important.	
27	DATA REF	This pin is used for setting the adaptive Data Slicer DC reference level. A capacitor from this pin to ground can be used to set the reference level at the average DC level of the data bit stream.The DC level determines the bit decision threshold.	
28	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
29	VCC4	This pin is used is supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	

Pin	Function	Description	Interface Schematic
30	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 31 although a small imbalance can be used to tune in the proper frequency range.	
31	RESNTR-	See RESNTR+ description.	See pin 30.
32	VCC2	This pin is used is supply DC bias to the VCO and buffer amps. A 10nF capacitor is recommended for 10.7MHz IF applications.	
33	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	
34	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 30.
35	VCO OUT	This pin is used is supply a buffered VCO output to go to the PLL chip. This pin has a DC bias and needs to be AC coupled.	
36	LO-	Balanced input for the first LO. This signal is presented to both the receiver second downconverter and transmit upconvertor.	
37	LO+	Complementary input of LO-	See pin 36.
38	GND8	Ground for LO amp and transmit upconvertor. Keep traces physically short and immediately to the ground plane for best performance.	
39	UP CONV	The output of the transmit signal upconvertor. This signal should be filtered to remove the undesired sideband and spurs before being applied to the PA input, pin 45.	
40	GND9	Same as pin 38.	See pin 38.
41	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
42	MUTE	This pin is used to mute the data output (DATA OUT). MUTE>2.0V turns the DATA OUT signal on. MUTE<1.0V turns the DATA OUT signal off. The MUTE signal should be logic low in the Sleep Mode.	
43	MIX CA	Mixer Current Adjust. This pin is used to adjust the current in the receiver. A resistor connected to ground controls the bias current in the mixer. The resistor should vary between 1kΩ to open circuit to vary the current from 18mA to 10.6mA	
44	PA INP	Input of the transmit power amplifier.	
45	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	

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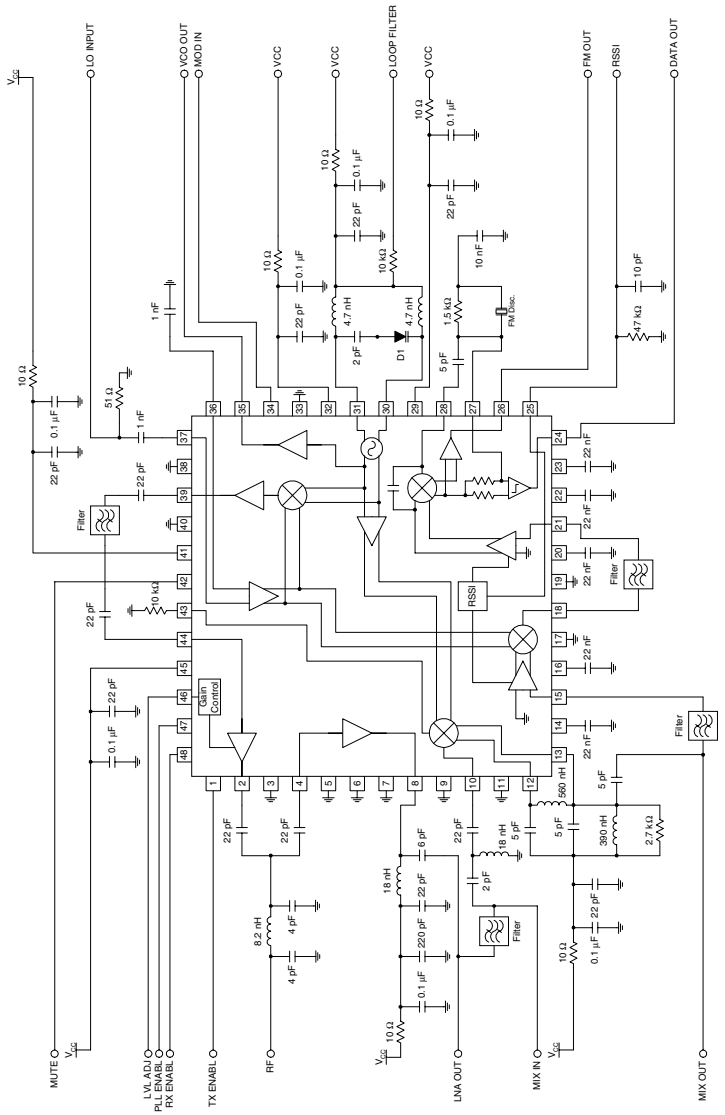
Pin	Function	Description	Interface Schematic
46	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp is also reduced with output power. This pin MUST be low when the transmitter is disabled.	
47	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
48	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	

Pin Out



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Application Schematic
915MHz



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MICRO·DEVICES

Preliminary

RF2938

2.4GHZ SPREAD SPECTRUM TRANSCEIVER

Typical Applications

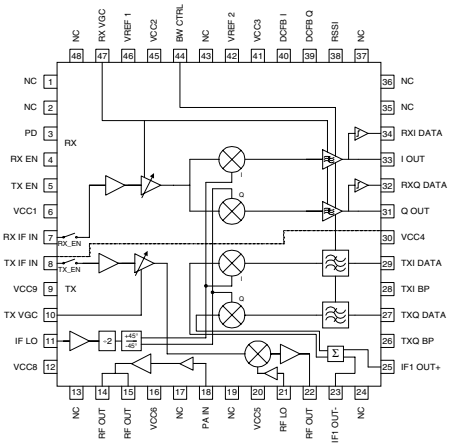
- Wireless LANs
- Wireless Local Loop
- Secure Communication Links
- Inventory Tracking
- Wireless Security
- Digital Cordless Telephones

Product Description

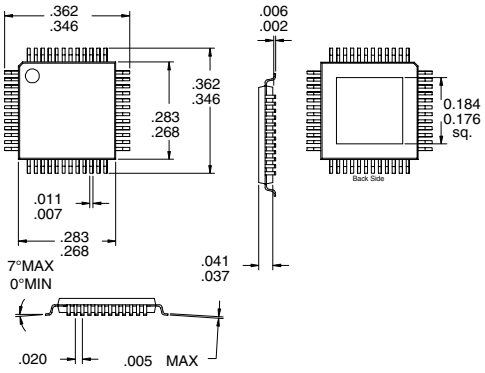
The RF2938 is a monolithic integrated circuit specifically designed for direct-sequence spread-spectrum systems operating in the 2.4GHz ISM band. The part includes a direct conversion from IF receiver, quadrature demodulator, I/Q baseband amplifiers with gain control and RSSI, on-chip programmable baseband filters, dual data comparators. For the transmit side, a QPSK modulator and upconverter are provided. The design reuses the IF SAW filter for transmit and receive reducing the number of SAW filters required. Two cell or regulated three cell (3.6V maximum) battery applications are supported by the part. The part is also designed to be part of a 2.4GHz chip set consisting of the RF2444 LNA/Mixer and one of the many RFMD high efficiency GaAs HBT PA's and a dual frequency synthesizer.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: TQFP-48 EPP

Features

- 45MHz to 500MHz IF Quad Demod
- On-Chip Variable Baseband Filters
- Quadrature Modulator and Upconverter
- 2.7V to 3.6V Operation
- Part of 2.4GHz Radio Chipset
- 2.4GHz PA Driver

Ordering Information

RF2938	2.4GHz Spread Spectrum Transceiver
RF2938 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

11 TRANSCEIVERS

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.3V, Freq=280MHz, R_{BW}=10kΩ
RX Frequency Range	45		500	MHz	
Cascaded Voltage Gain		20 to 93		dB	Dependent upon RX VGC
Cascaded Noise Figure		5		dB	At maximum gain.
Cascaded Input IP_3		-110		dBm	V_{GC} <1.2V
Cascaded Input IP_3		-55		dBm	V_{GC}>2.0V
RSSI Dynamic Range		60		dB	At V_{GC}=1.4V
RSSI Output Voltage Compliance		1.1 to 2.3		V	Maximum RSSI is 2.5V or V_{CC}-0.3, whichever is less. V_{GC}=1.4V
IF LO Leakage		-68		dBm	f=280MHz, LO Power=-10dBm
Quadrature Phase Offset		6		°	I leads Q.
Quadrature Phase Variation		±2	±4	°	With expected LO amplitude and harmonic content.
Quadrature Amplitude Offset		+0.25		dB	Q>I
Quadrature Amplitude Variation		±0.25		dB	
IF AMP and Quad Demod					
Gain Control Range		43		dB	VGC <1.2V max gain, VGC>2.0V=min gain
Noise Figure		5		dB	Single Sideband
IF Input Impedance		230-j400		Ω	Single ended. 280MHz
Input IP_3		-68		dBm	V_{GC}<1.2V
		-8		dBm	V_{GC}>2.0V
RX Baseband Amplifiers					
THD		3		%	At maximum gain setting
		3		%	At minimum gain setting
Gain Control Range		30		dB	V_{GC}<1.2V=max gain, V_{GC}>2.0V=min gain
VGA Output Voltage		500		mV_{PP}	R_L≥5kΩ, C_L≤5pF
VGA DC Output Voltage		1.7		V	
RX Baseband Filters					
Baseband Filter 3dB Bandwidth	1		35	MHz	5th order Bessel LPF. Set by BW CTRL
Passband Ripple			0.1	dB	
Baseband Filter 3dB Frequency Accuracy		±10	±30	%	
Group Delay		15		ns	At 35MHz, increasing as bandwidth decreases.
Group Delay		400		ns	At 2MHz.
Baseband Filter Ultimate Rejection		>80		dB	
Output Impedance		20		Ω	Designed to drive≥5kΩ, ≤5pF load.

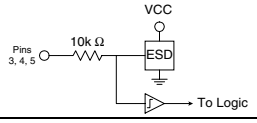
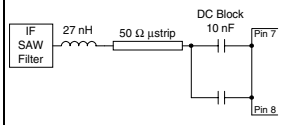
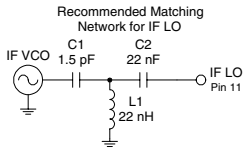
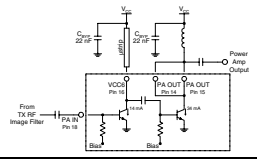
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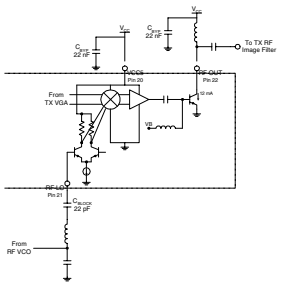
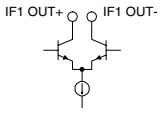
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Data Amplifiers					
Bandwidth	40			MHz	
Gain (Limiting mode)		60		dB	Open Loop.
Rise and Fall Time		2	5	ns	5pF load.
Logic High Output	V_{CC}-0.3V	V_{CC}		V	Source Current 1mA
Logic Low Output			0.3	V	Sink Current 1mA.
Hysteresis		30		mV	
Transmit Modulator and LPF					
Filter Gain		0		dB	Any setting
Baseband Filter 3dB Bandwidth	1		35	MHz	5th order Bessel LPF, Set by BW CTRL
Passband Ripple			0.1	dB	
Group Delay		15		ns	At 35MHz, increasing as bandwidth decreases.
Group Delay		400		ns	At 2MHz.
Ultimate Rejection		>80		dB	
Input Impedance	3			kΩ	Single ended
Input AC Voltage			200	mV_{p-p}	Linear, Single ended.
IF Frequency Range	45		500	MHz	
Output Impedance		2		kΩ	Open Collector when TX on, hi-Z when off
I/Q Phase Balance		0	4		
I/Q Gain Balance		0.5±0.25		dB	
Conversion Voltage Gain		1.1		V/V	With Current Combination into 50Ω single-ended load
Output P1dB		-6		dBm	With Current Combination into 50Ω single-ended load
Carrier Output		30		dBm	Without external offset adjustments. 280MHz
Harmonic Outputs		-30		dBc	
Transmit VGA and Upconverter					
VGA Gain Range		17		dB	
VGA Input Voltage Range		1.0 to 2.0		V	Positive Slope
VGA Gain Sensitivity		17		dB/V	
VGA Input Impedance		230-j400		Ω	
RF Mixer Output Impedance		50		Ω	With matching elements.
VGA/Mixer Conversion Gain		+10 to +27		dB	With 50Ω match on the output.
VGA/Mixer Output Power		-9		dBm	1dB compression - Single Side Band, TX GC=1.0V
VGA/Mixer Output Power		-4		dBm	1dB compression - Single Side Band, TX GC=2.0V

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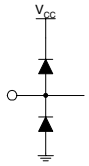
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmit Power Amp					
Linear Output Power		6		dBm	
Gain		23		dB	
Output P1dB		12		dBm	
Output Impedance		50		Ω	
Input IP3		0		dBm	
Input Impedance		50		Ω	
Power Down Control					
Logical Controls “ON”	V_{CC}-0.3V		V_{CC}+0.3V	V	Voltage supplied to the input, not to exceed 3.6V
Logical Controls “OFF”	-0.3	0	0.3	V	Voltage supplied to the input.
Control Input Impedance		>1		MΩ	
RX to TX and TX to RX Time		TBD		ns	
IF LO Input					The IF LO is divided by 2 and split into quadrature signals to drive the frequency mixers.
Input Impedance		1050-j1200		Ω	f=560MHz
Input Power Range	-15	-10	0	dBm	peak
Input Frequency	90		1000	MHz	(2x IF Frequency)
RF LO Input					
Input Impedance		33-j110		Ω	f=2.16GHz untuned.
Input Power Range	-15		0	dBm	
Input Frequency	2000		2400	MHz	
Power Supply					
Voltage	2.7	3.3	3.6	V	
Total Current Consumption					V_{CC}=3.3V, Baseband BW 1MHz to 40MHz
Sleep Mode Current		1		µA	PD=1, RX EN=1, TX EN=1
PA Driver Current		48		mA	
RX Current BW (MHz)					
0-11		65		mA	
12-20		70		mA	
20-30		110		mA	
TX Current BW (MHz)					Excluding PA Driver
0-11		95		mA	
12-20		105		mA	
20-30		115		mA	

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Pin	Function	Description	Interface Schematic
1	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
2	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
3	PD	This pin is used to power up or down the transmit and receive baseband sections. A logic high powers up the quad demod mixers, TX and RX GmC LPF's, baseband VGA amps, data amps, and IF LO buffer amp/ phase splitter. A logic low powers down the entire IC for sleep mode. Also, see State Decode Table.	
4	RX EN	Enable pin for the receiver 15dB gain IF amp and the RX VGA amp. Powers up all receiver functions when PD is high, turns off the receiver IF circuits when low. Also, see State Decode Table.	See pin 3.
5	TX EN	This pin is used to enable the transmit upconverter, buffer amps, 15db IF amp, quad mod mixers, TX LO buffer, TX VGA, and PA driver. TX EN is active low, when TX EN <1V, the transmit circuit is active if PD is high. A logic high (TX EN >2V) disables the transmit IF/RF circuitry and quad mod. Also, see State Decode Table.	See pin 3.
6	VCC1	Power supply for RX VGA amplifier, IC logic and RX references.	
7	RX IF IN	IF input for receiver section. Must have DC blocking cap. The capacitor value should be appropriate for the IF frequency. External matching to 50Ω recommended. For half duplex operation, connect RX IF IN and TX IF IN signals together after the DC blocking caps, then run a transmission line from the output of the IF SAW.	See pin 8.
8	TX IF IN	Input for the TX IF signal after SAW filter. External DC blocking cap required. External matching to 50Ω recommended. For half duplex operation, connect RX IF IN and TX IF IN signals together after the DC blocking caps, then run a transmission line from the output of the IF SAW.	
9	VCC9	Power supply for the TX 15dB gain amp and TX VGA.	
10	TX VGC	Gain control setting for the transmit VGA. Positive slope.	
11	IF LO	IF LO input. Must have DC blocking cap. The capacitor value should be appropriate for the IF frequency. LO frequency=2xIF. Quad mod/demod phase accuracy requires low harmonic content from IF LO, so it is recommended to use an n=3 LPF between the IF VCO and IF LO.	
12	VCC8	Power supply for IF LO buffer and quadrature phase network.	
13	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
14	RF OUT	This is the output transistor of the power amp stage. It is an open collector output. The output match is formed by an inductor to V_{CC}, which supplies DC and a series cap.	
15	RF OUT	This is the output transistor of the power amp stage. It is an open collector output. The output match is formed by an inductor to V_{CC}, which supplies DC and a series cap.	See pin 14.
16	VCC6	Power supply for the PA driver amp. This inductance to ground via decoupling, along with an internal series capacitor, forms the interstage match.	See pin 14.
17	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	

Pin	Function	Description	Interface Schematic
18	PA IN	Input to the power amplifier stage. This is a 50Ω input. Requires DC blocking/tuning cap.	See pin 14.
19	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
20	VCC5	Supply for the RF LO buffer, RF upconverter and amplifier.	
21	RF LO	Single ended LO input for the transmit upconverter. External matching to 50Ω and a DC block are required.	See pin 20.
22	RF OUT	Upconverted Transmit signal. This 50Ω output is intended to drive an RF filter to suppress the undesired sideband, harmonics, and other out-of-band mixer products.	See pin 20.
23	IF1 OUT-	The inverting open collector output of the quadrature modulator. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun with IF1 OUT+, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, just IF1 OUT+ can be used to drive a SAW single-ended with an RF choke (high Z at IF) from V_{CC} to IF1 OUT-.	
24	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
25	IF1 OUT+	The non-inverting open collector output of the quadrature modulator. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun with IF1 OUT-, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, just IF1 OUT+ can be used to drive a SAW single-ended with an RF choke (high Z at IF) from V_{CC} to IF1 OUT+.	See pin 23.
26	TXQ BP	This is the quadrature phase modulator bypass pin. A 10nF capacitor to ground is recommended.	
27	TXQ DATA	Q input to the baseband 5 pole Bessel LPF for the transmit modulator.	
28	TXI BP	This is the in-phase modulator bypass pin. A 10nF capacitor to ground is recommended.	
29	TXI DATA	I input to the baseband 5 pole Bessel LPF for the transmit modulator.	
30	VCC4	Power supply for quadrature modulator.	
31	Q OUT	Baseband analog signal output for quadrature channel. 500mV$_{P-P}$ linear output.	
32	RXQ DATA	Logic-level data output for the quadrature channel. This is a digital output signal obtained from the output of a Schmitt trigger. 0.3V to VCC3 - 0.3V swing minimum.	
33	I OUT	Baseband analog signal output for in-phase channel. 500mV$_{P-P}$ linear output.	
34	RXI DATA	Logic-level data output for the in-phase channel. This is a digital output signal obtained from the output of a Schmitt trigger. 0.3V to VCC3 - 0.3V swing minimum.	
35	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
36	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	

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Pin	Function	Description	Interface Schematic
37	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
38	RSSI	Received signal strength indicator. Connect 8.2pF to ground. Output impedance is 40kΩ in parallel with 2pF.	
39	DCFB Q	DC feedback capacitor for quadrature channel. Requires decoupling capacitor to ground. (22nF recommended)	
40	DCFB I	DC feedback capacitor for in-phase channel. Requires capacitor to ground. (22nF recommended)	
41	VCC3	Supply for the I and Q data amps.This pin should be bypassed with a 10nF capacitor connected as direct as possible to GND3. Ground this pin if data amps are not used.	
42	VREF 2	Gain control reference voltage. No current should be drawn from this pin (<50μA). 2.0V nominal.	
43	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
44	BW CTRL	This pin requires a resistor to ground to set the baseband LPF bandwidth of the receiver and transmit GmC filter amps.	
45	VCC2	Supply for the I and Q baseband and GmC filters. This pin should be bypassed with a 10nF capacitor.	
46	VREF 1	This is a bypass pin for the bias circuits of the GmC filter amps and for I/Q inputs. No current should be drawn from this pin (<10μA). 1.7V nominal.	
47	RX VGC	Receiver IF and baseband amp gain control voltage. Negative slope.	
48	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
Pkg Base		Ground for all circuitry in the device. A very low inductance from the base to the PCB groundplane is essential for good performance. Use an array of vias immediately underneath the device.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 3-6, 9, 10, 12, 26-34, 38-42, 44-47.	

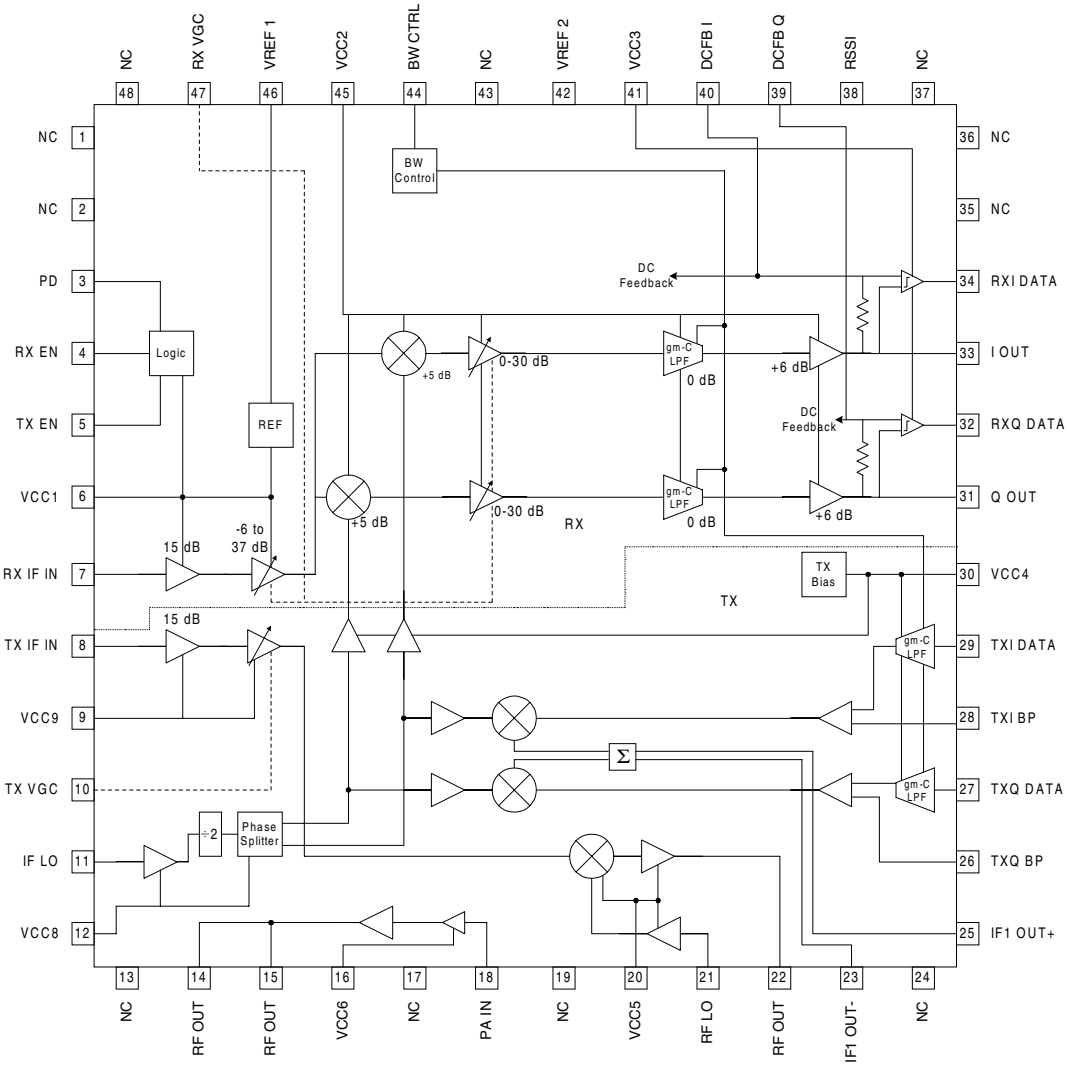
State Decode Table	Input Pins			Internally Decoded Signals		
	PD	RX EN	TX EN	BB EN	RXIF EN	TXRF EN
Sleep Mode	0	x	x	0	0	0
Baseband Only	1	0	1	1	0	0
Receive Mode	1	1	1	1	1	0
Transmit Mode	1	0	0	1	0	1
Full Duplex	1	1	0	1	1	1

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NOTES	
BB_EN Enables:	
	TX_LPF's and buffers
	Quad Demodulator mixers
	Baseband VGA and gm-C LPF's
	Data Amplifiers
	IF LO buffer/phase splitters
RXIF_EN Enables:	
	Front-end IF amplifier (RX)
	RX IF VGA amplifiers
TXRF_EN Enables:	
	Front-end IF amplifier (TX)
	TX VGA
	RF upconverter and buffer
	PA driver
	RF LO buffer
	Quad Modulator mixers

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Detailed Functional Block Diagram



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RF2938 Theory of Operation

Receiver

RX IF AGC/MIXER

The front end of the IF AGC starts with a single-ended input and a constant gain amp of 15dB. This first amp stage sets the noise figure and input impedance of the IF section, and its output is taken differentially. The rest of the signal path is differential until the final baseband output, which is converted back to single-ended. Following the front end amp are multiple stages of variable gain differential amplifiers, giving the IF signal path a gain range of 9dB to 52dB. The noise figure (in max gain mode) of the IF amplifiers is 5dB, which should not degrade the system noise figure.

The IF to BB mixers are double-balanced, differential in, differential out, mixers with 5dB conversion gain. The LO for each of these mixers is shifted 90° so that the I and Q signals are separated in the mixers.

RX Baseband Amps, Filters, Data Slicers, and DC Feedback

At baseband frequency, there are multiple AGC amplifiers offering a gain range of 0dB to 30dB. Following these amplifiers are fully integrated gm-C low pass filters to further filter out-of-band signals and spurs that get through the SAW filter, anti-alias the signal prior to the A/D converter, and to band-limit the signal and noise to achieve optimal signal-to-noise ratio. The 3dB cut-off frequency of these low pass filters is programmable with a single external resistor, and continuously variable from 1MHz to 35MHz. A five-pole Bessel type filter response was chosen because it is optimal for data systems due to its flat delay response and clean step response. Butterworth and Chebychev type filters ring when given a step input making them less ideal for data systems.

The filter outputs, with +6dBm gain, drive the linear $500mV_{PP}$ signal off-chip, but also connect internally to a data slicer which squares up the signal to CMOS levels, and drives this “data” signal off-chip. This data slicer is a high speed CMOS comparator with 30mV of hysteresis and self-aligned input DC offset. This data slicer can be independently disabled if only the linear outputs are desired.

DC feedback is built into the baseband amplifier section to correct for input offsets. Large DC offsets can arise when a mixer LO leaks to the mixer input and then mixes with itself. DC offsets can also result from random transistor mismatches. A large external capacitor is needed for the DC feedback to set the high pass cutoff, and this capacitor is reused to set the DC input level for the self-aligned data slicer.

The receive signal path also has an RSSI output which is the sum of both the I and Q channels. The RSSI has about 60dBm of dynamic range and the RSSI characteristic is optimized to give best linearity and dynamic range at a VGC setting of 1.4V. It is recommended that the system sets VGC to 1.4V to take an RSSI reading to make channel activity and signal level decisions, then adjusts VGC to obtain optimum dynamic range from the I_{OUT} and Q_{OUT} outputs.

LO Input Buffers

RF LO Buffer

The RF LO input has a limiting amplifier before the mixer on both the RF2444 (RX) and RF2938 (TX). This limiting amplifier design and layout is identical on both ICs, which will make the input impedance the same as well. Having this amplifier between the VCO and mixer minimizes any reverse effect the mixer has on the VCO, expands the range of acceptable LO input levels, and holds the LO input impedance constant when switching between RX and TX. The LO input power range is -18dBm to +5dBm, which should make it easy to interface to any VCO and frequency synthesizer.

IF LO Buffer

The IF LO input has a limiting amplifier before the phase splitting network to amplify the signal and help isolate the VCO from the IC. Also, the LO input signal must be twice the desired intermediate frequency. This simplifies the quadrature network and help reduce the LO leakage onto the RX_IF input pin (since the LO input is now at a different frequency than the IF). The amplitude of this input needs to be between -15dBm and 0dBm. Excessive IF LO harmonic content affects phase balance of the modulator and demodulator so it is recommended that a simple n=3 low pass filter is included between VCO and IF LO input.

Transmitter

TX LPF and Mixers

The transmit section starts with a pair of 5-pole Bessel filters identical to the filters in the receive section and with the same 3dB frequency. These filters pre-shape and band-limit the digital or analog input signals prior to the first upconversion to IF. These filters have a high input impedance and expect an input signal of $200mV_{PP}$ typical. Following these low pass filters are the I/Q quadrature upconverter mixers. Each of these mixers is half the size and half the current of the RF to

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IF downconverter on the RF2444. Recall that this upconverted signal may drive the same SAW filter (in half duplex mode) as the RF2444 and therefore share the same load. Having the sum of the two BB to IF mixers equal in size and DC current to the RF to IF mixer, will minimize the time required to switch between RX and TX, and will facilitate the best impedance match to the filter.

TX VGA

The AGC after the SAW filter starts with a switch and a constant gain amplifier of 15dB, which is identical to the circuitry on the receive IF AGC. This was, done, as on the RX signal path, so that the input impedance will remain constant for different TX gain control voltages. Following this 15dB gain amplifier is a single stage of gain control offering 15dB gain range. The main purpose of adding this variable gain is to give the system the flexibility to use different SAW filters and image filters with different insertion loss values. This gain could also be adjusted real time, if desired.

TX Upconverter

The IF to RF upconverter is a double-balanced differential mixer with a differential to single-ended converter on the output to supply 0dBm peak linear power to the image filter. The upconverted SSB signal should have -6dBm power at this point, and the image will have the same power, but due to the correlated nature of the signal and image, the output must support 0dBm of linear power to maintain linearly.

+6dBm PA Driver

The SSB output of the upconverter is -6dBm of linear power. The image filter should have at most 4dB of insertion loss while removing the image, LO, 2LO and any other spurs. The filter output should supply the PA driver input -10dBm of power.

The PA driver is a two-stage class A amplifier with 10dB gain per stage and capable of delivering 6dBm of linear power to a 50Ω load, and has a 1dB compression point of 12dBm. For lower power applications, this PA driver can be used to drive a 50Ω antenna directly.

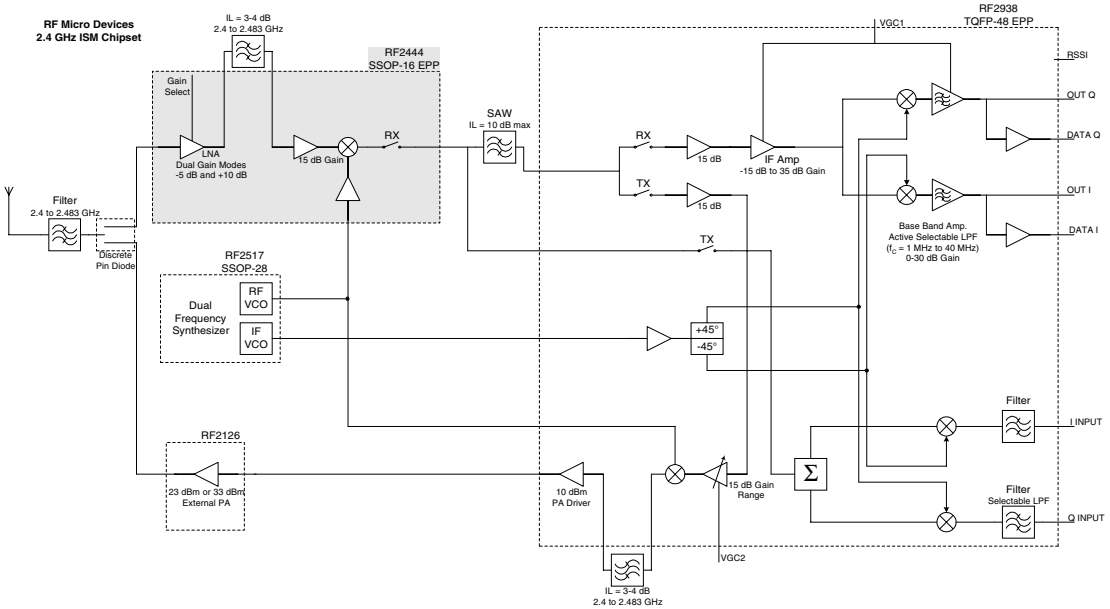
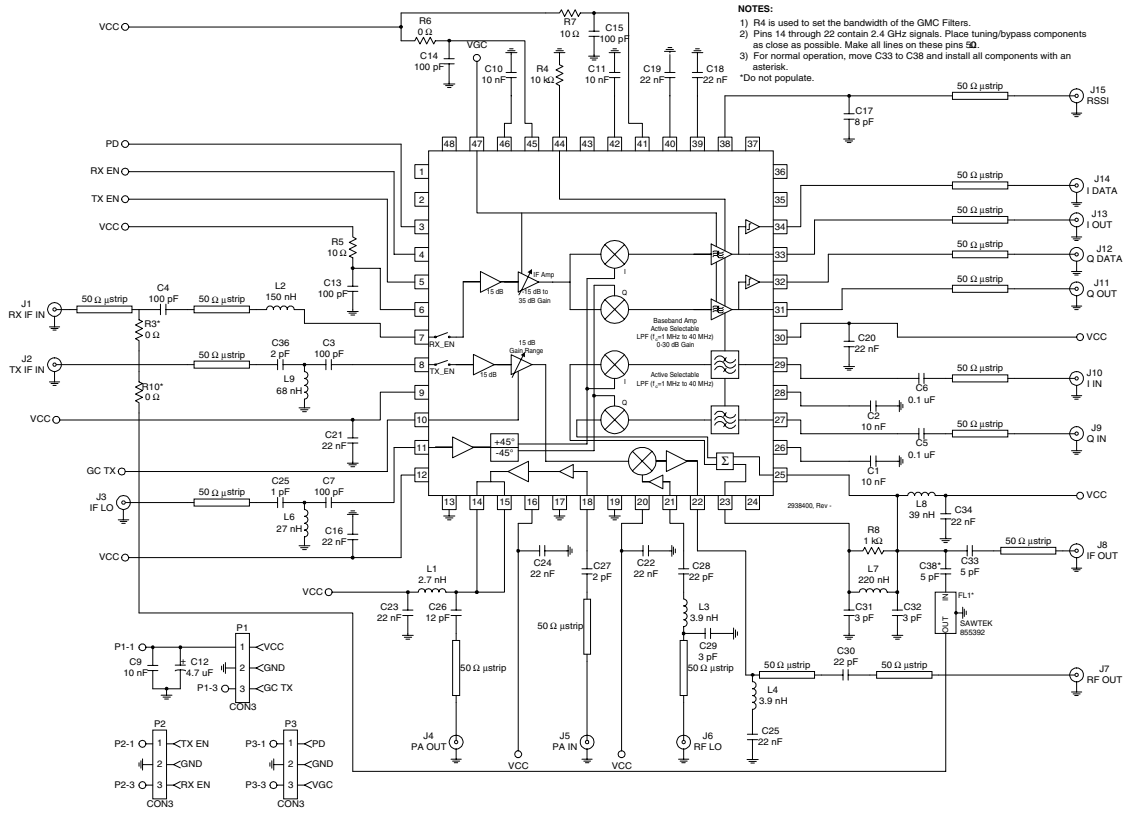


Figure 1. Entire Chipset Functional Block Diagram

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Evaluation Board Schematic

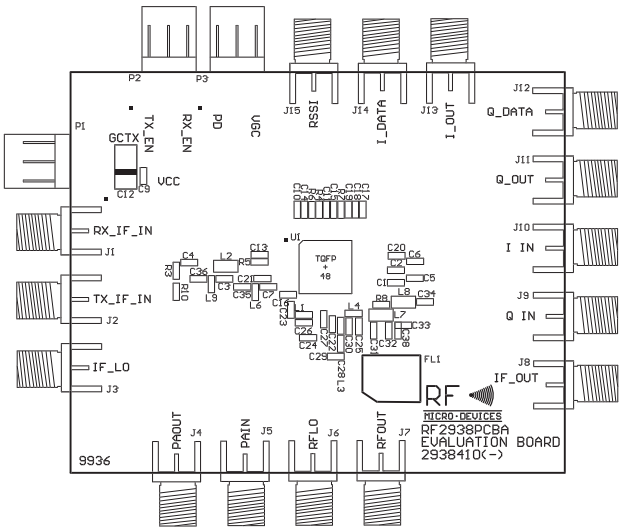
(Download Bill of Materials from www.rfmd.com.)

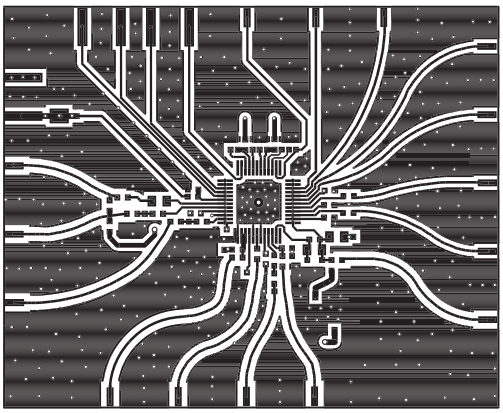


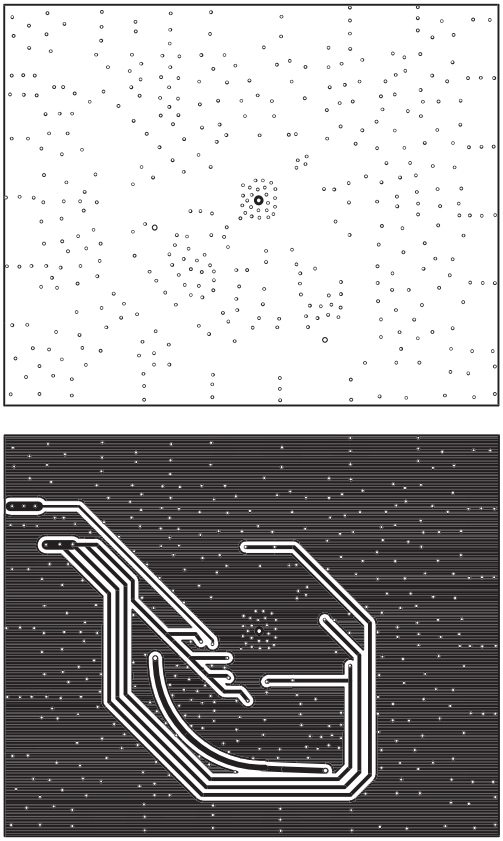
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Evaluation Board Layout
Board Size 2.580” x 2.086”

Thickness: Top to Gnd Laminate, 0.008”; Gnd to Bottom Laminate, 0.023”; Board Material FR-4; Multi-Layer

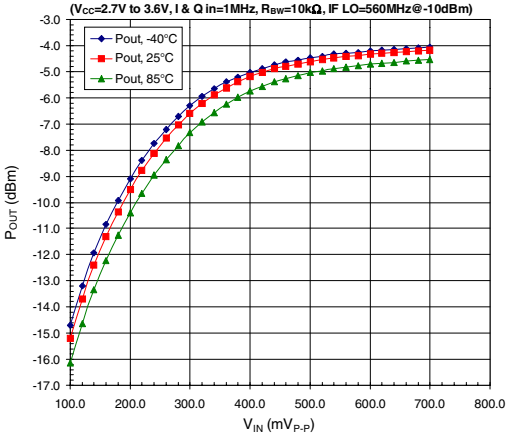






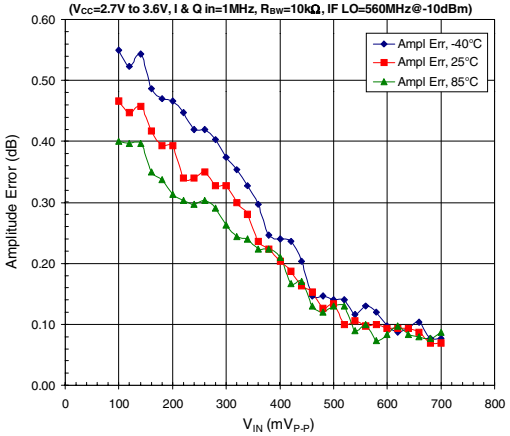
V_{IN} versus P_{OUT}

(V_{CC}=2.7V to 3.6V, I & Q in=1MHz, R_{BW}=10kΩ, IF LO=560MHz@-10dBm)



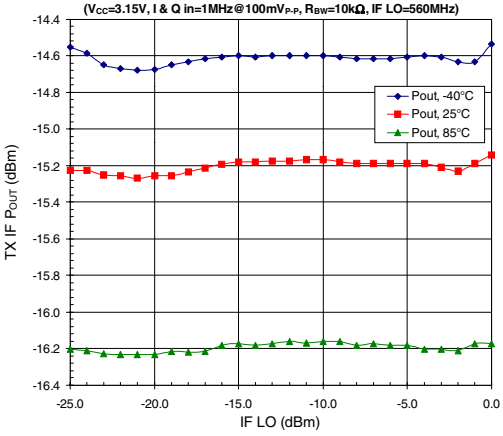
V_{IN} versus Amplitude Error

(V_{CC}=2.7V to 3.6V, I & Q in=1MHz, R_{BW}=10kΩ, IF LO=560MHz@-10dBm)



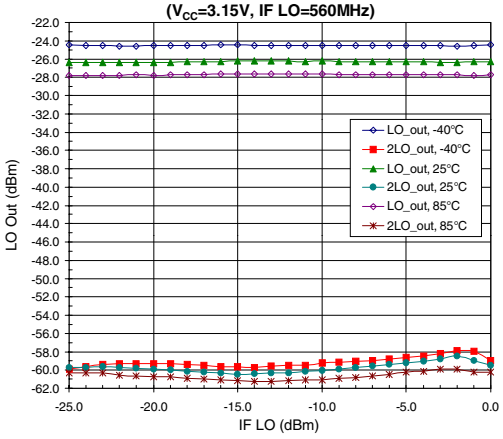
TX IF P_{OUT} versus IF LO

(V_{CC}=3.15V, I & Q in=1MHz@100mVP-P, R_{BW}=10kΩ, IF LO=560MHz)



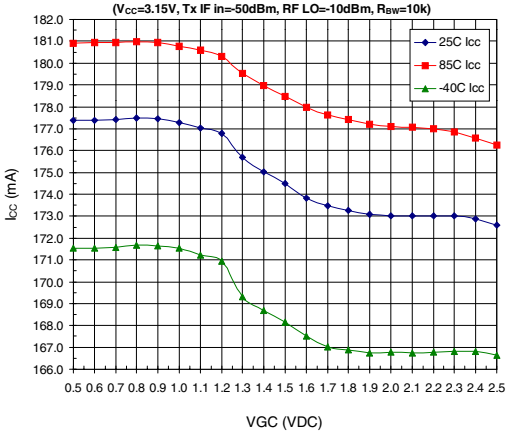
LO & 2LO Out versus IF LO

(V_{CC}=3.15V, IF LO=560MHz)



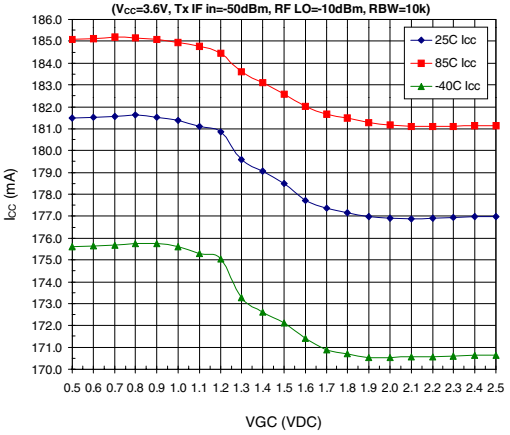
Total I_{CC} versus VGC

(V_{CC}=3.15V, Tx IF in=-50dBm, RF LO=-10dBm, R_{BW}=10k)



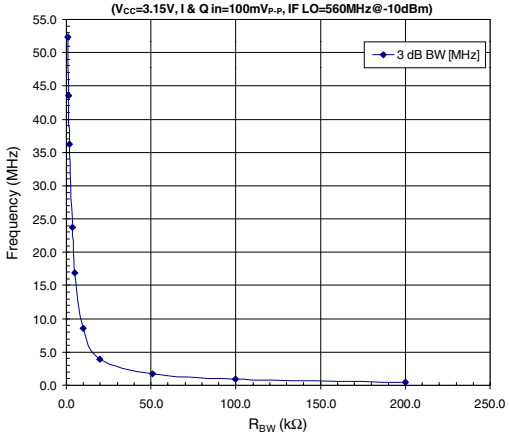
Total I_{CC} versus VGC

(V_{CC}=3.6V, Tx IF in=-50dBm, RF LO=-10dBm, RBW=10k)



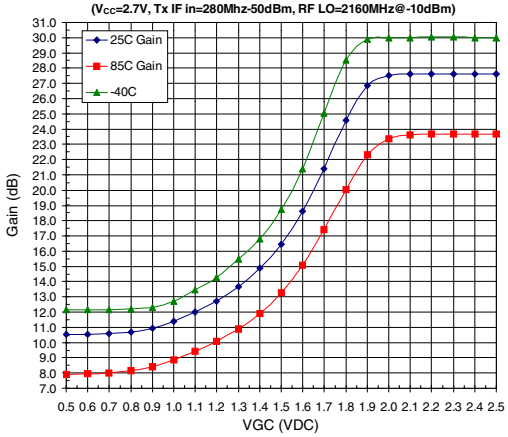
R_{BW} versus 3dB BW Point

(V_{CC}=3.15V, I & Q in=100mV_{P-P}, IF LO=560MHz@-10dBm)



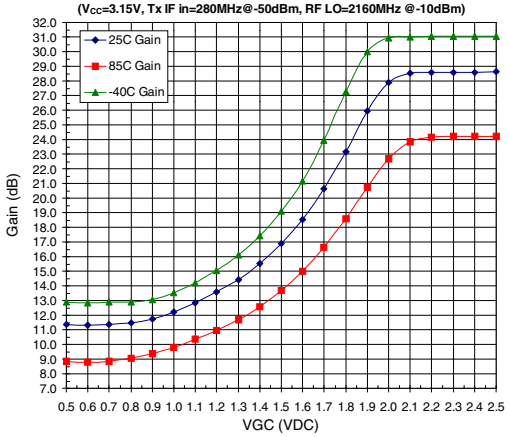
RF Conversion Gain versus VGC

(V_{CC}=2.7V, Tx IF in=280Mhz-50dBm, RF LO=2160MHz@-10dBm)



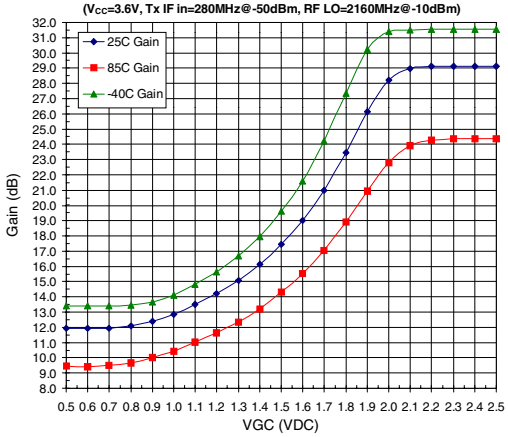
RF Conversion Gain versus VGC

(V_{CC}=3.15V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz @-10dBm)



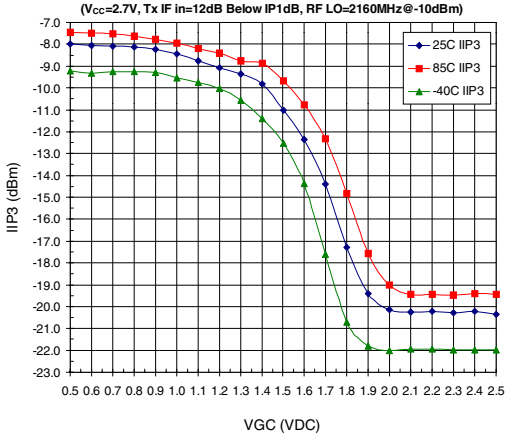
RF Conversion Gain versus VGC

(V_{CC}=3.6V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz@-10dBm)



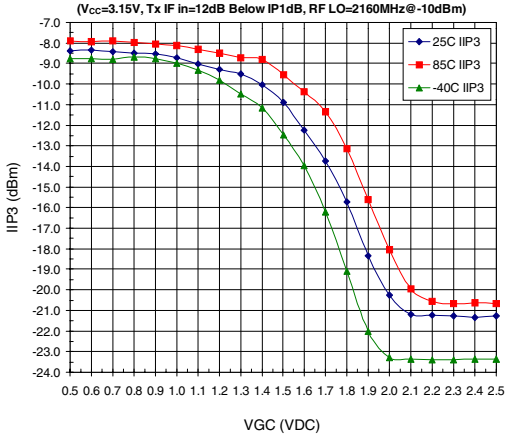
IF-RF IIP3 versus VGC

(V_{CC}=2.7V, Tx IF in=12dB Below IP1dB, RF LO=2160MHz@-10dBm)



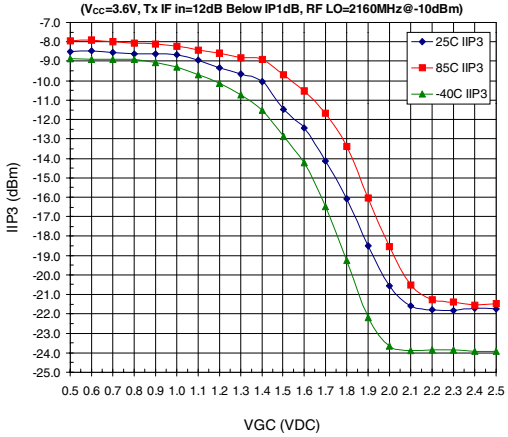
IF-RF IIP3 versus VGC

(V_{CC}=3.15V, Tx IF in=12dB Below IP1dB, RF LO=2160MHz@-10dBm)

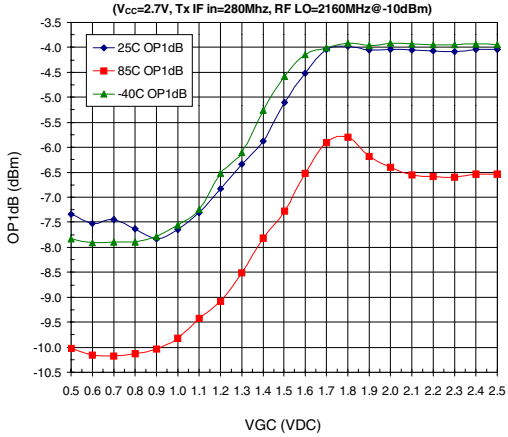


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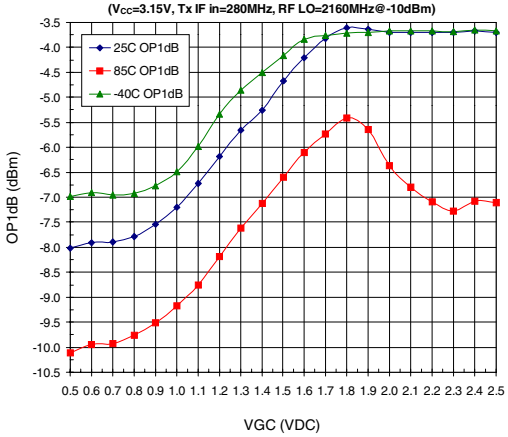
IF-RF IIP3 versus VGC
(V_{CC}=3.6V, Tx IF in=12dB Below IP1dB, RF LO=2160MHz@-10dBm)



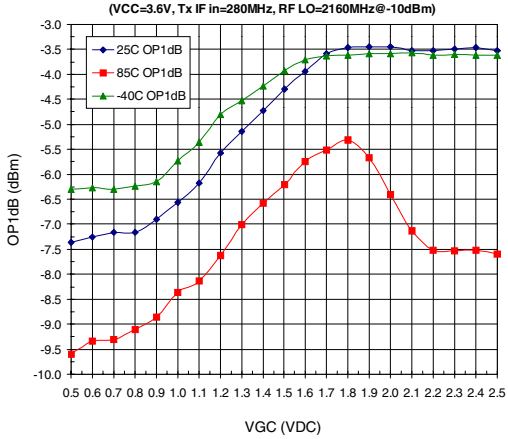
IF-RF OP1dB versus VGC
(V_{CC}=2.7V, Tx IF in=280Mhz, RF LO=2160MHz@-10dBm)



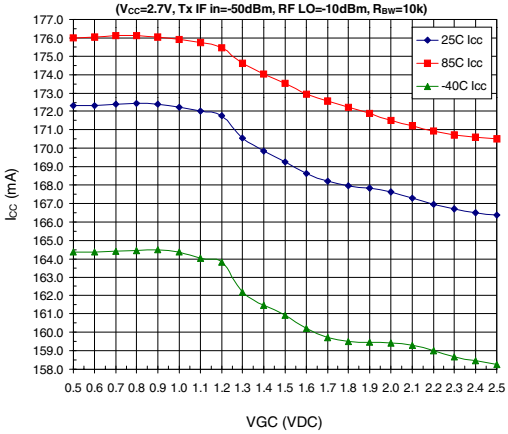
IF-RF OP1dB versus VGC
(V_{CC}=3.15V, Tx IF in=280MHz, RF LO=2160MHz@-10dBm)



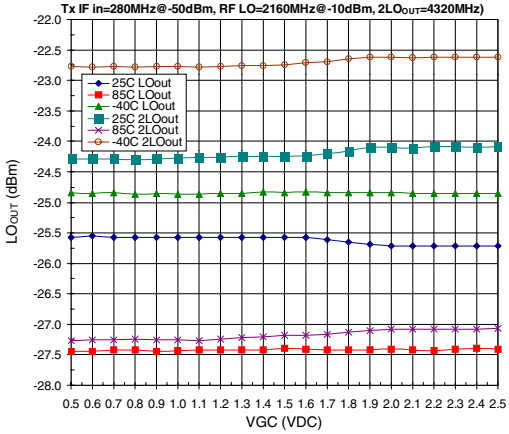
IF-RF OP1dB versus VGC
(VCC=3.6V, Tx IF in=280MHz, RF LO=2160MHz@-10dBm)



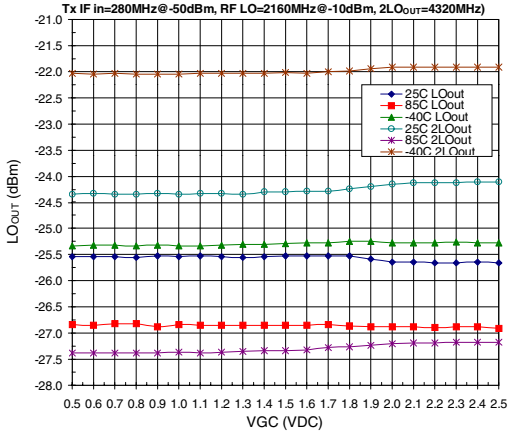
Total I_{CC} versus VGC
(V_{CC}=2.7V, Tx IF in=-50dBm, RF LO=10dBm, R_{BW}=10k)



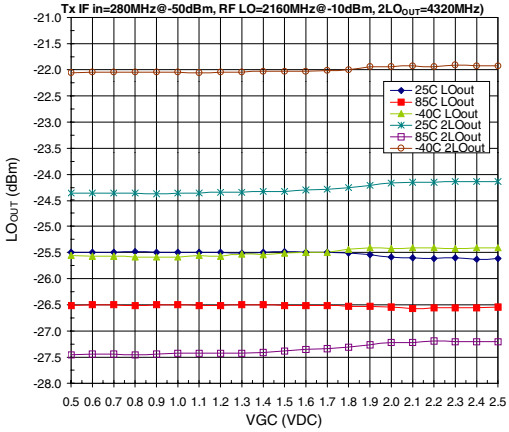
RF LO_{OUT} & RF $2LO_{OUT}$ versus VGC (V_{CC}=2.7V,
Tx IF in=280MHz@-50dBm, RF LO=2160MHz@-10dBm, $2LO_{OUT}$=4320MHz)



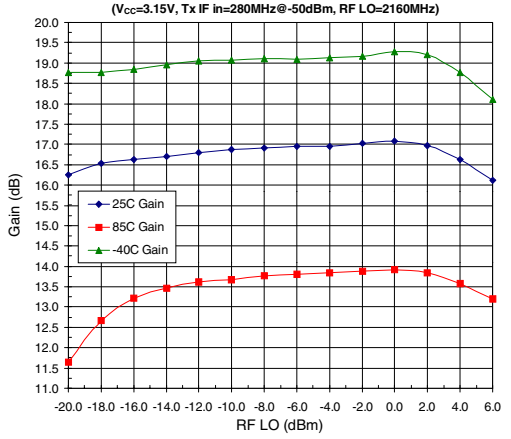
RF LO_{OUT} & RF $2LO_{OUT}$ versus VGC (V_{CC}=3.15V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz@-10dBm, $2LO_{OUT}$=4320MHz)



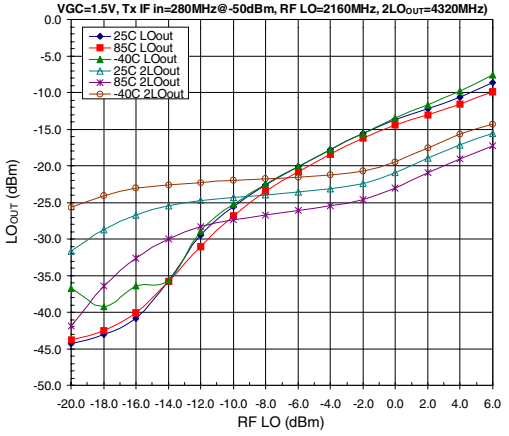
RF LO_{OUT} & RF $2LO_{OUT}$ versus VGC (V_{CC}=3.6V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz@-10dBm, $2LO_{OUT}$=4320MHz)



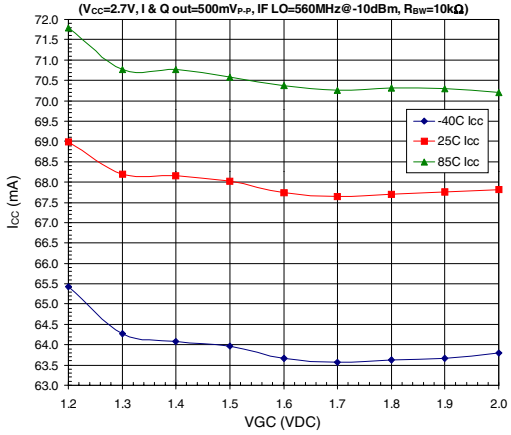
RF Conversion Gain versus RF LO Level (V_{CC}=3.15V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz)



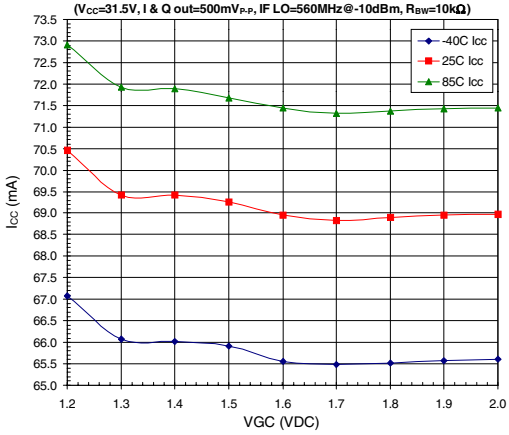
RF LO_{OUT} & RF $2LO_{OUT}$ versus RF LO Level (V_{CC}=3.15V, VGC=1.5V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz, $2LO_{OUT}$=4320MHz)



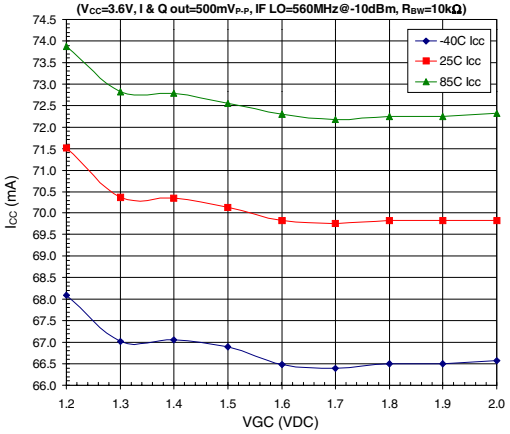
RX I_{CC} versus VGC (V_{CC}=2.7V, I & Q out=500mV_{P-P}, IF LO=560MHz@-10dBm, R_{BW}=10kΩ)



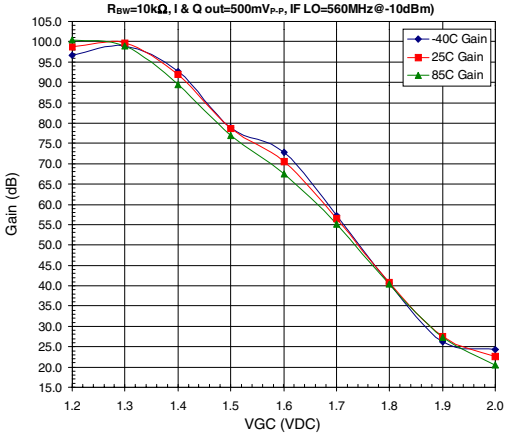
RX I_{CC} versus VGC (V_{CC}=31.5V, I & Q out=500mV_{P-P}, IF LO=560MHz@-10dBm, R_{BW}=10kΩ)



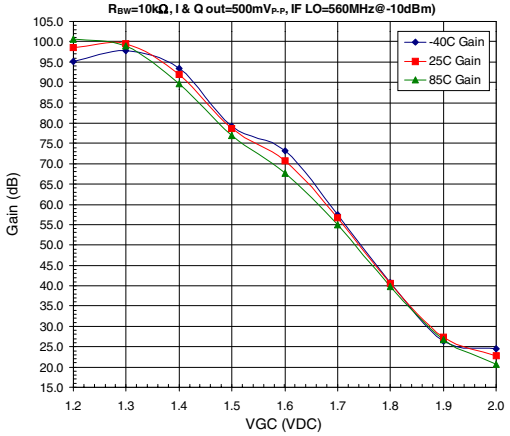
RX I_{CC} versus VGC
(V_{CC}=3.6V, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm, R_{BW}=10kΩ)



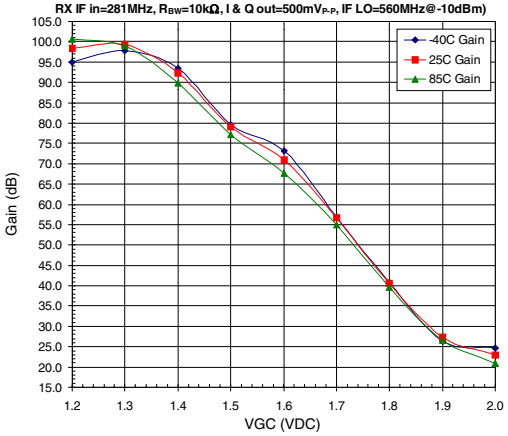
RX Gain versus VGC (V_{CC}=2.7V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



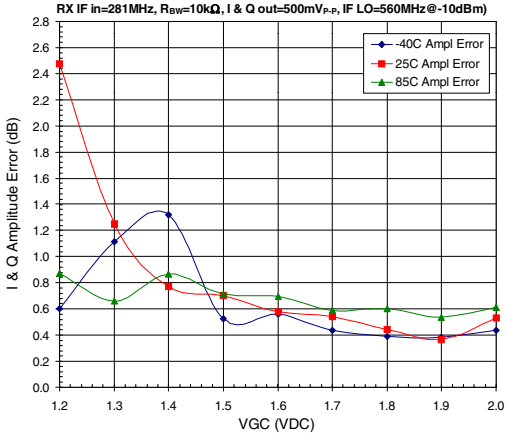
RX Gain versus VGC (V_{CC}=3.15V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



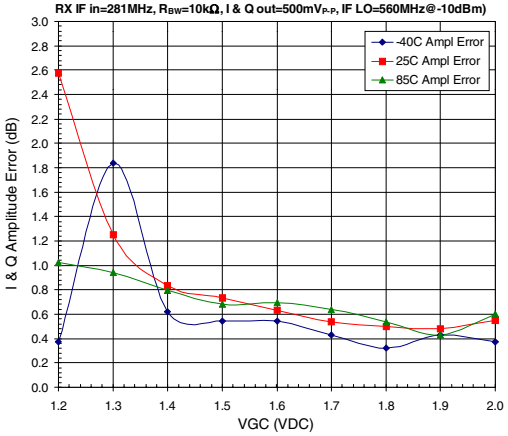
RX Gain versus VGC (V_{CC}=3.6V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



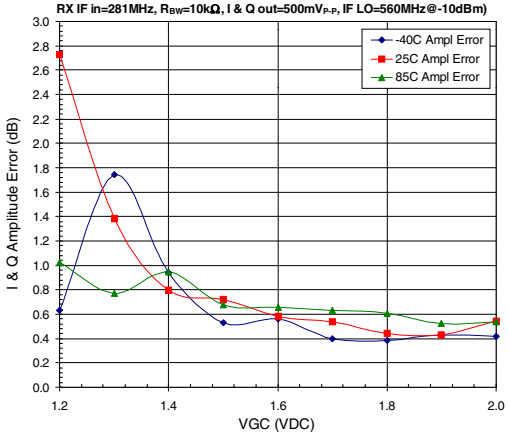
I & Q Amplitude Balance versus VGC (V_{CC}=2.7V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



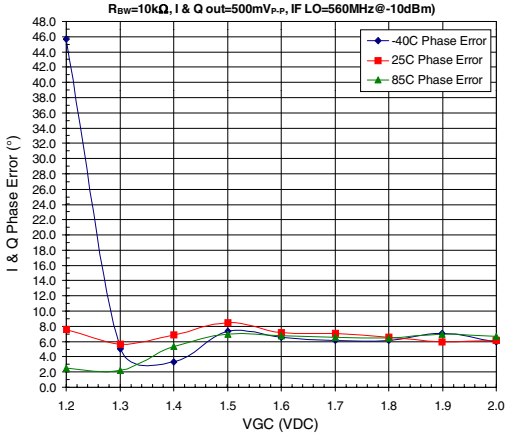
I & Q Amplitude Balance (V_{CC}=3.15V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



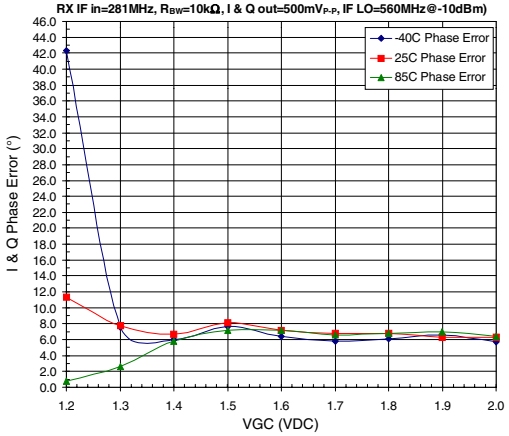
I & Q Amplitude Balance (V_{CC}=3.6V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



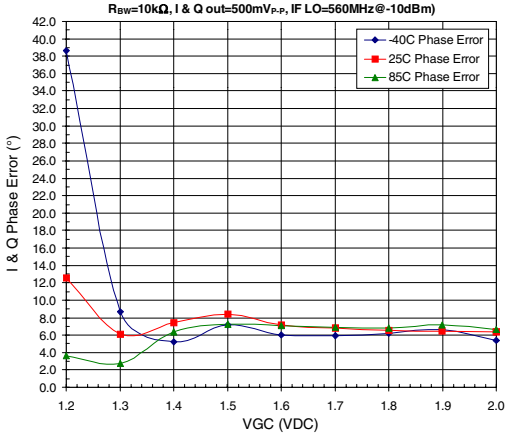
I & Q Phase Error versus VGC (V_{CC}=2.7V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



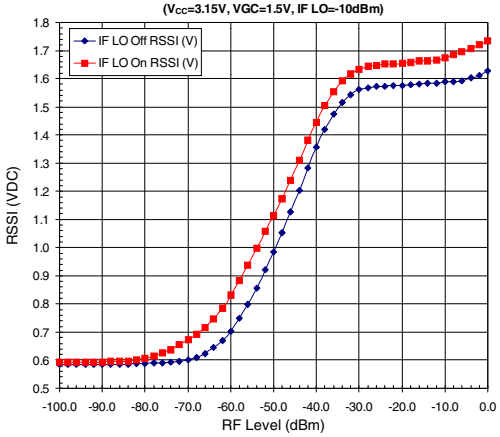
I & Q Phase Error versus VGC (V_{CC}=3.15V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



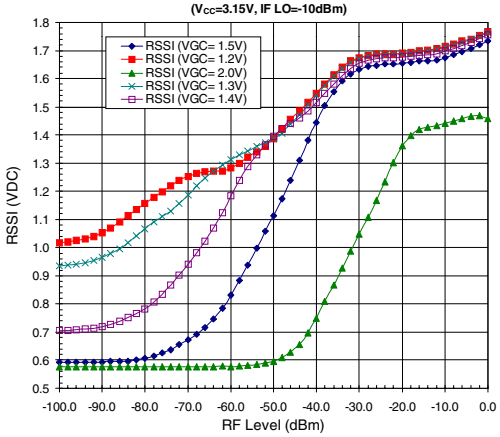
I & Q Phase Error versus VGC (V_{CC}=3.6V, RX IF in=281MHz, R_{BW}=10kΩ, I & Q out=500mV$_{P-P}$, IF LO=560MHz@-10dBm)



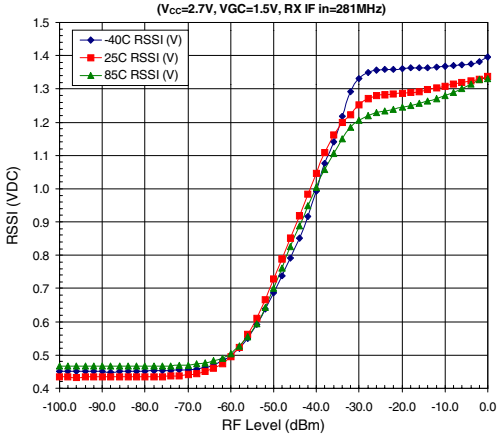
RSSI (V_{CC}=3.15V, VGC=1.5V, IF LO=-10dBm)



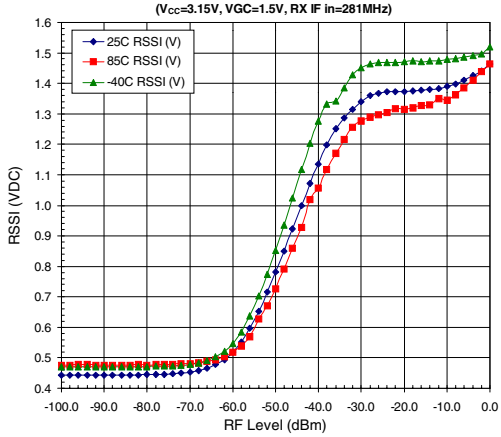
RSSI versus VGC (V_{CC}=3.15V, IF LO=-10dBm)



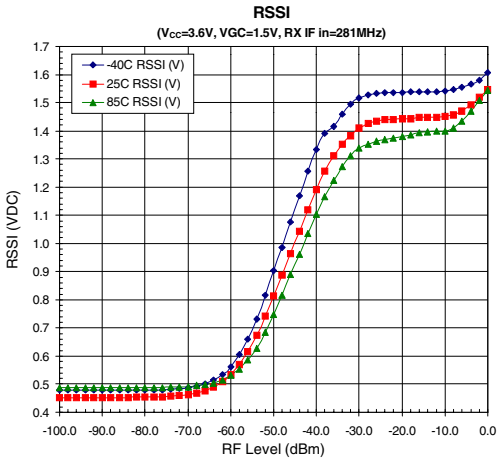
RSSI
(V_{CC}=2.7V, VGC=1.5V, RX IF in=281MHz)



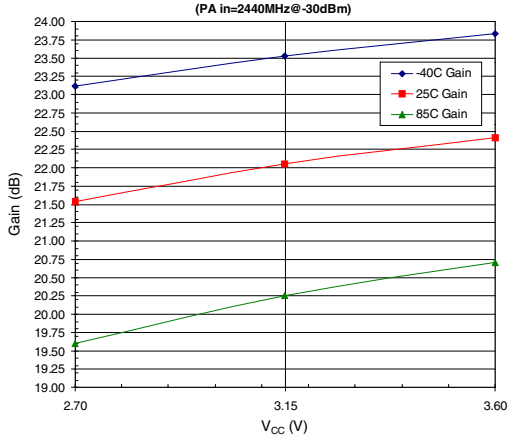
RSSI
(V_{CC}=3.15V, VGC=1.5V, RX IF in=281MHz)



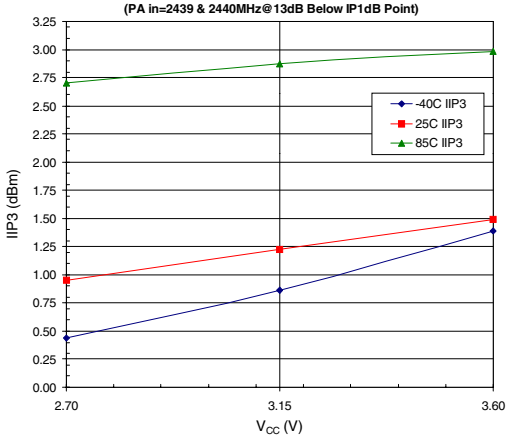
RSSI
(V_{CC}=3.6V, VGC=1.5V, RX IF in=281MHz)



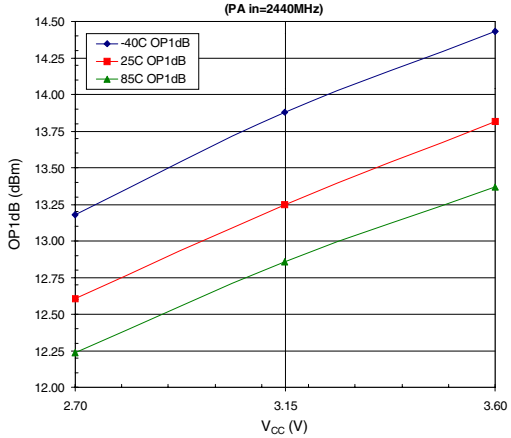
PA Gain versus V_{CC}
(PA in=2440MHz@-30dBm)



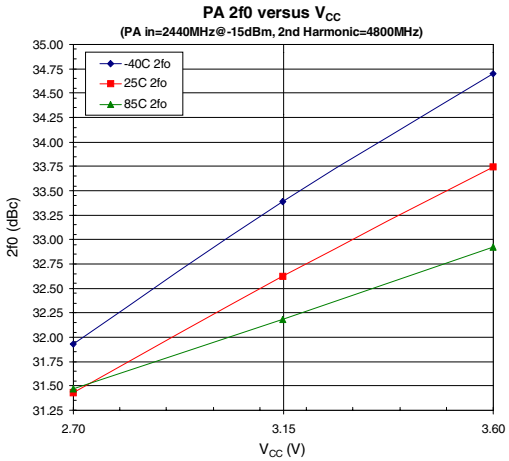
PA IIP3 versus V_{CC}
(PA in=2439 & 2440MHz@13dB Below IP1dB Point)



PA OP1dB versus V_{CC}
(PA in=2440MHz)



11
TRANSCEIVERS


PA 2f0 versus V_{CC}
(PA in=2440MHz@-15dBm, 2nd Harmonic=4800MHz)
-40C 2fo
25C 2fo
85C 2fo
2f0 (dBc)
35.00
34.75
34.50
34.25
34.00
33.75
33.50
33.25
33.00
32.75
32.50
32.25
32.00
31.75
31.50
31.25
2.70
3.15
3.60
V_{CC} (V)

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MICRO·DEVICES

RF2945

433/868/915MHZ FSK/ASK/OOK TRANSCEIVER

Typical Applications

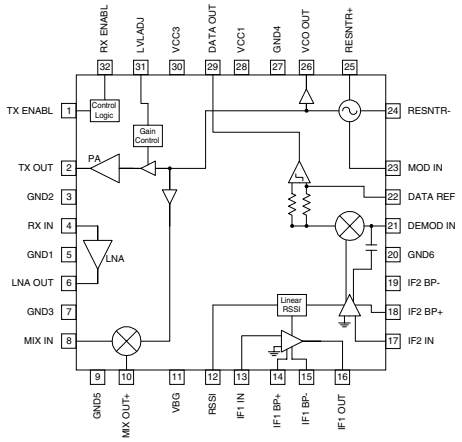
- Wireless Meter Reading
- Keyless Entry Systems
- 433, 868 and 915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

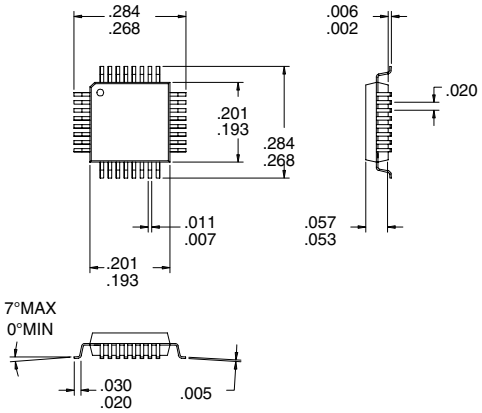
The RF2945 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 32-lead plastic TQFP packaging and is designed to be used with a PLL IC to provide a fully functional FM transceiver. The chip is intended for digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433/868MHz ISM bands. The integrated VCO has a buffered output to feed the RF signal back to the PLL IC to form the frequency synthesizer. Internal decoding of the RX ENABL and TX ENABL lines allow for half duplex operation as well as turning on the VCO to give the synthesizer time to settle and complete power downmode. The DATA REF line allows the use of an external capacitor to control the DC level at the adaptive Data Slicer input for setting the bit decision threshold.

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: LQFP-32

Features

- Fully Monolithic Integrated Transceiver
- 2.4V to 5.0V Supply Voltage
- Narrow Band and Wide Band FSK
- 300MHz to 1000MHz Frequency Range
- 10dB Cascaded Noise Figure
- 10mW Output Power With Power Control

Ordering Information

RF2945	433/868/915MHz FSK/ASK/OOK Transceiver
RF2945 PCBA-L	Fully Assembled Evaluation Board (433MHZ)
RF2945 PCBA-H	Fully Assembled Evaluation Board (915MHz)

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11 TRANSCEIVERS

RF2945

Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

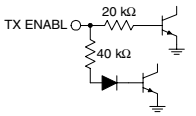
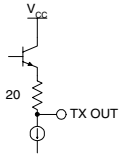
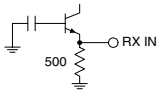
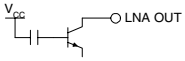
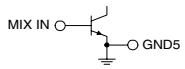
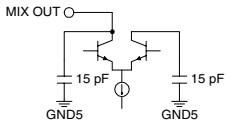
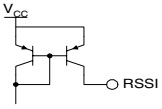
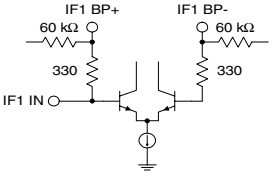
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
VCO OUT Impedance		50		Ω	
VCO OUT Level		-20		dBm	Freq=915MHz
VCO/PLL Phase Noise		-72		dBc/Hz	10kHz offset, 5kHz loop BW
		-98		dBc/Hz	100kHz offset, 5kHz loop BW
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+8.5		dBm	Freq=433MHz
	1	+3	5	dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage. Dependent on external circuitry.
Antenna Port Impedance		50		Ω	TX ENABL="1", RX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-38		dBc	Freq=915MHz, with eval board filter
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity	-91.5	-96		dBm	IF BW=400kHz, Freq=915MHz, S/N=8dB
LO Leakage		-55		dBm	Freq=915MHz
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		22.5		mV/dB	
RSSI Dynamic Range	70	80		dB	

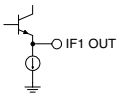
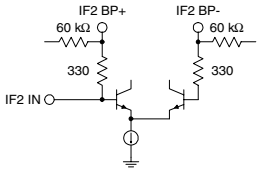
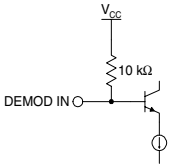
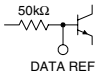
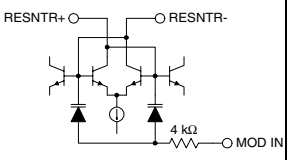
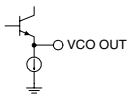
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LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1", TX ENABL="0"
Antenna Port VSWR			1.5:1		RX Mode
Output Impedance		Open Collector		Ω	433MHz and 915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		10		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT pin
Demod Input Impedance		10		kΩ	
Data Output Bandwidth	1.4			MHz	3dB Bandwidth, Z_{LOAD}=1MΩ ‖ 3pF
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ ‖ 3pF. Output voltage is proportional with the instantaneous frequency deviation.
Power Down Control					
Logical Controls "ON"	2.0			V	Voltage supplied to the input
Logical Controls "OFF"			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Turn On Time			1	ms	Turn on/off times are dependent upon
Turn Off Time			1	ms	PLL loop parameters
RX to TX and TX to RX Time			100	µs	
Power Supply					
Voltage		3.6		V	Specifications
	2.7		5.0	V	Operating limits Temperature range -40°C to +85°C
	2.4			V	Operating limits Temperature range +10°C to +40°C
Current Consumption	17	22	27.4	mA	TX ENABL, LVLADJ=3.6V, RX ENABL=0V
	4.8	6.1	7.2	mA	TX ENABL=3.6V, LVLADJ, RX ENABL=0V
	4.4	6.1	6.8	mA	TX ENABL=0V, RX ENABL=3.6V
			1	µA	TX ENABL, LVLADJ, RX ENABL=0V
		3.6		mA	PLL Only Mode, TX ENABL, RX ENABL=3.6V, LVLADJ=0V

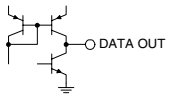
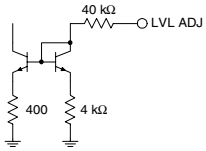
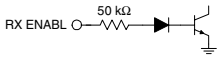
RF2945

Pin	Function	Description	Interface Schematic
1	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
2	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance (see output impedance plot) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
3	GND2	Ground connection for the 40 dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance (see input impedance plot) when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
5	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
6	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
7	GND3	Same as pin 3.	
8	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
9	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
10	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
11	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	.
12	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.3V and increases with increasing signal strength.	
13	IF1 IN	IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	

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Pin	Function	Description	Interface Schematic
14	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
15	IF1 BP-	Same as pin 14.	See pin 13.
16	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330 Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 IN	IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330 Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 17.
19	IF2 BP-	Same as pin 18.	See pin 17.
20	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
21	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
22	DATA REF	This pin is used for setting the adaptive Data Slicer DC reference level. A capacitor from this pin to ground can be used to set the reference level at the average DC level of the data bit stream.The DC level determines the bit decision threshold.	
23	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 24.
24	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 25 although a small imbalance can be used to tune in the proper frequency range.	
25	RESNTR-	See RESNTR+ description.	See pin 24.
26	VCO OUT	This pin is used is supply a buffered VCO output to go to the PLL chip. This pin has a DC bias and needs to be AC coupled.	
27	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

RF2945

Pin	Function	Description	Interface Schematic
28	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68 pF capacitor is recommended for 433MHz applications.	
29	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater.	
30	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
31	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. NOTE: This pin MUST be low when the transmitter is disabled.	
32	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	

Operation Mode	TX ENABL	RX ENABL	Function
Sleep Mode	Low	Low	Entire chip is powered down. Total current consumption is <1µA. *
Transmit Mode	High	Low	Transmitter, VCO are on.
Receive Mode	Low	High	Receiver, VCO are on. *
PLL Lock	High	High	VCO is on. This mode allows time for a synthesizer loop to lock without spending current on the transmitter or receiver.

* LVL ADJ pin must be low to disable transmitter.

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RF2945 Theory of Operation and Application Information

The RF2945 is part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433MHz to 868MHz ISM band, and 915MHz U.S. ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products.

In its basic form, the RF2945 can be implemented as a two-way half-duplex FSK transceiver with the addition of some crystals, filters, and passive components. The RF2945 is designed to interface with common PLL IC's to form a multi-channel radio. The receiver IF section is optimized to interface with low-cost 10.7MHz ceramic filters and has a 3dB bandwidth of 25MHz and can still be used (with lower gain) at higher frequencies with other types of filters. The PA output and LNA input are available on separate pins and are designed to be connected together through a DC blocking capacitor. In the transmit mode, the PA will have a 50Ω impedance and the LNA will have a high impedance. In the receive mode, the LNA will have a 50Ω impedance and the PA will have a high impedance. This eliminates the need for a TX/RX switch, and allows for a single RF filter to be used in transmit and receive modes. Separate access to the PA and LNA allows the RF2945 to interface with external components such as a high power PA, lower NF LNA, upconverters, and downconverters, for a variety of implementations.

FM/FSK SYSTEMS

The MOD IN pin drives an internal varactor for modulating the VCO. This pin can be driven with a voltage level needed to generate the desired deviation. This voltage can be carried on a DC bias to select desired slope (deviation/volt) for FM systems. Or, a resistor divider network referenced to VCC or ground can divide down logic level signals to the appropriate level for a desired deviation in FSK systems.

On the receiver demod, the DATA OUT pin is the output of an internal data slicer providing logic level outputs. The digital output is generated by a data slicer that compares the demodulator with a DC reference voltage recovered from the demodulator. The reference voltage is obtained by a filter capacitor on pin 22. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesirable 2xIF product. This type data slicer has the ability to track out minor frequency errors in the system, but requires a longer period of time for the preamble for optimum results. For best operation of the on-chip data slicer, FM deviation needs to be larger than $40kHz_{P-P}$

The data slicer itself is a transconductance amplifier, and the DATA OUT pin is capable of driving rail-to-rail output only into a very high impedance and a small capacitance. The amount of capacitance will determine the bandwidth of DATA OUT. In a 3pF load, the bandwidth is in excess of 500kHz. The rail-to-rail output of the data slicer is also limited by the frequency deviation and bandwidth of IF filters. With the 400kHz bandwidth filters on the evaluation boards, the rail-to-rail output is limited to less than 320kHz. Choosing the right IF bandwidth and deviation versus data rate (mod index) is important in evaluating the applicability of the RF2945 for a given data rate.

The primary consideration when directly modulating the VCO is the data rate versus PLL bandwidth. The PLL will track out the modulation to the extent of its bandwidth, which distorts the modulating data. Therefore, the lower frequency components of the modulating data should be five to 10 times the loop bandwidth to minimize the distortion. The lower frequency components are generated by long strings of 1's and 0's in data stream. By limiting the number of consecutive, same bits, lower frequency components can be set. In addition, the data stream should be balanced to minimize distortion. Using a coding pattern such as Manchester is highly recommended to optimize system performance.

The PLL loop bandwidth is important in several system parameters. For example, switching from transmit to receive requires the VCO to retune to another frequency. The switching speed is proportional to the loop bandwidth: the higher the loop bandwidth, the faster the switching times. Phase noise of the VCO is another factor. Phase noise outside the bandwidth is because of the VCO itself, rather than a crystal reference. The design trade-offs must be made here in selecting a PLL loop bandwidth with acceptable phase noise and switching characteristics, as well as minimal distortion of the modulation data.

ASK/OOK SYSTEMS

The transmitter of the RF2945 has an output power level adjust (LVL ADJ) that can be used to provide approximately 18dB of power control for amplitude modulation. The RSSI output of the receiver section can be used to recover the modulation. The RSSI output is from a current source, and needs to have a

resistor to convert to a voltage. A 51kΩ resistor load typically produces an output of 0.7V to 2.5V. A parallel capacitor is suggested to the band limit of the signal. For ASK applications, the 18dB range of the LVL ADJ does not produce enough voltage swing in the RSSI for reliable communications. The on/off keying (OOK) is suggested to provide reliable communications. To achieve this, the LVL ADJ and TX ENABL need to be controlled together (please note that LVL ADJ cannot be left high when TX ENABL is low). This will provide an on/off ratio of greater than 50dB. One of the unfortunate consequences of modulating in this manner is VCO pulling by the PA. This results in a spurious output outside the desired transmit band, as the PLL momentarily loses lock and reacquires. This may be avoided by pulse-shaping TX data to slow the change in the VCO load to a pace which the PLL can track with its given loop bandwidth. The loop bandwidth may also be increased to allow it to track faster changes brought about by load pulling.

For the ASK/OOK receiver demodulator, an external data slicer is required. The RSSI output is used to provide both the filter data and a very low pass filter (relative to the data rate) DC reference to the data slicer. Because the very low pass filter has a slow time constant, a longer preamble may be required to allow for the DC reference to acquire a stable state. Here, as in the case of the FSK transmitter, the data pattern also affects the DC reference and the reliability of the receive data. Again, a coding scheme such as Manchester should be used to improve data integrity.

APPLICATION AND LAYOUT CONSIDERATIONS

Both the RX IN and the TX OUT have a DC bias on them. Therefore, a DC blocking cap is required. If the RF filter has DC blocking characteristics (such as a ceramic dielectric filter), then only one DC blocking cap would be needed to separate the DC of the RX and TX. These are RF signals and care should be taken to run the signal keeping them physically short. Because of the 50Ω/high impedance nature of these two signals, they may be connected together into a single 50Ω device (such as a filter). An external LNA or PA may be used, if desired, but an external RX/TX switch may be required.

The VCO is a very sensitive block in the system. RF signals feeding back into the VCO (either radiated or coupled by traces) may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonator and varactor are very important. The capacitor and varactor should be close to the RF2945 pins, and the trace length should be as short as possible. The inductors may be placed further away, and reducing the value of the inductors can compensate any trace inductance. Printed inductors may also be used with careful design. For best results, physical layout should be as symmetrical as possible. Figure 1 is a recommended layout pattern for the VCO components. When using the loop bandwidth lower than 5kHz shown on the evaluation board, better filtering of the VCC at the resonators (and lower VCC noise, as well) will help reduce phase noise of the VCO. A series resistor of 100Ω to 200Ω, and a 1μF or larger capacitor may be used.

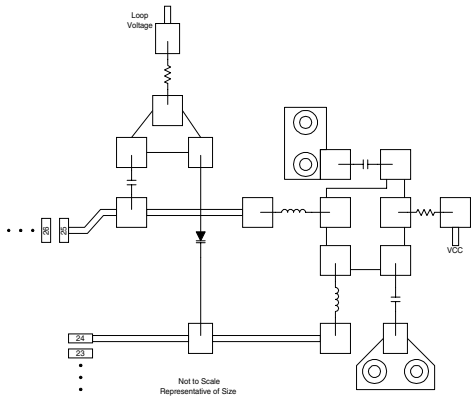


Figure 1. Recommended VCO Layout

For the interface between the LNA/mixer, the coupling capacitor should be as close to the RF2945 pins as possible, with the bias inductors further away. Once again, the value of the inductor may be changed to compensate for trace inductance. The output impedance of the LNA is in the order of several kΩ, which makes matching to 50Ω very difficult. If image filtering is desired, a high impedance filter is recommended.

The quad tank of the discriminator may be implemented with ceramic discriminator available from a couple of sources. This design works well for wideband applications where temperature range is limited. The temperature coefficient of ceramic discriminators may be in the order of +50ppm/°C. The alternative to the ceramic discriminator is the LC tank, which provides a broadband discriminator more useful for high data rates.

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PLL Synthesizer

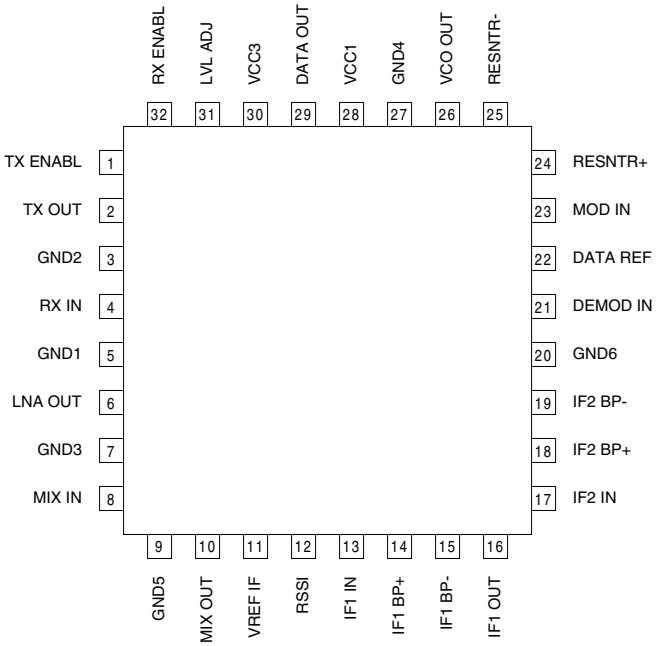
The RF2945 evaluation board uses an LMX2316 PLL IC from National Semiconductor. This PLL IC may be programmed from the software available from National Semiconductor (codeloader at www.national.com/appinfo/wireless/). An external reference oscillator is required for the PLL IC allowing for the evaluation of different reference frequencies or step sizes. The National Semiconductor software also has a calculator for determining the R and C component values for a given loop bandwidth.

The RF2945 is controlled by RX ENABL and TX ENABL which are decoded to put the RF2945 into one of four states. It may be put into a PLL-only mode with TX ENABL and RX ENABL both high. This condition is used to provide time for the synthesizer to turn on an obtained lock before turning on the receiver or transmitter. Note that LVL ADJ needs to be held low for PLL-only mode. Sometimes, it is desirable to ramp up the power amplifier to minimize load pulling on the VCO. To do this with the RF2945, first put the RF2945 into PLL mode by putting TX ENABL and RX ENABL high. Then, ramp up LVL ADJ to turn on the transmitter and PA. The rate at which LVL ADJ is allowed to ramp up is dependent on the PLL loop bandwidth. VCC pushing also affects the VCO frequency. A good low pass filter on VCC will minimize the VCC pushing effects.

For applications requiring fast switching speeds or turn-on times, and low data rate loop filter bandwidths, the LMX2316 may be configured to drive the loop filter in a fast switching mode. Please refer to literature on the LMX2316 for more information.

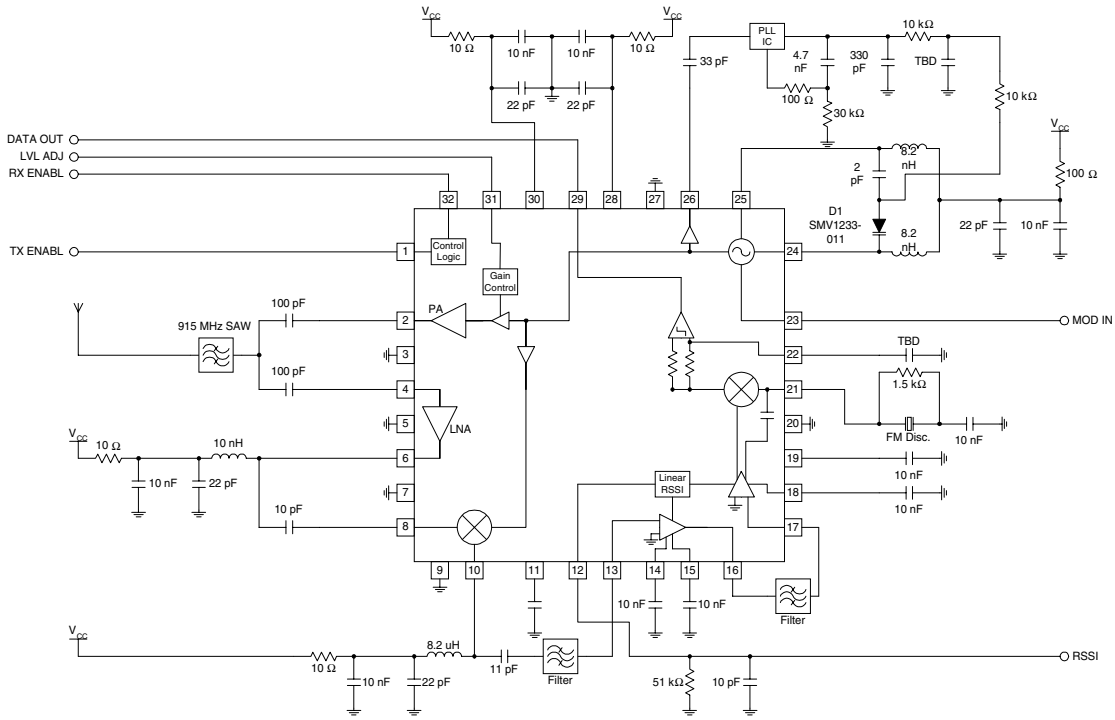
RF2945

Pin Out

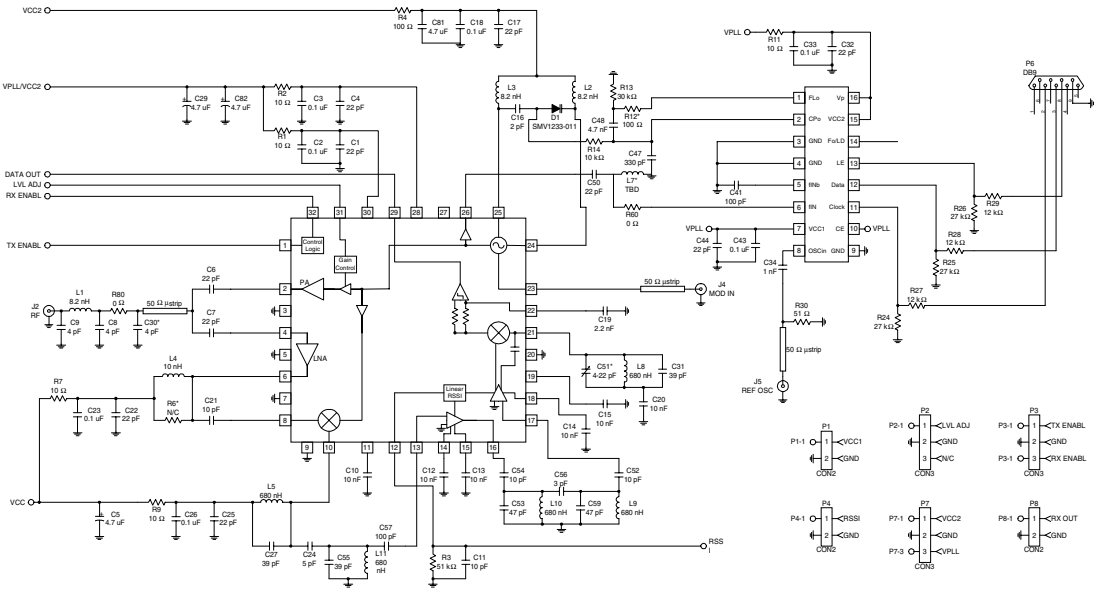


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Application Schematic - 915 MHz

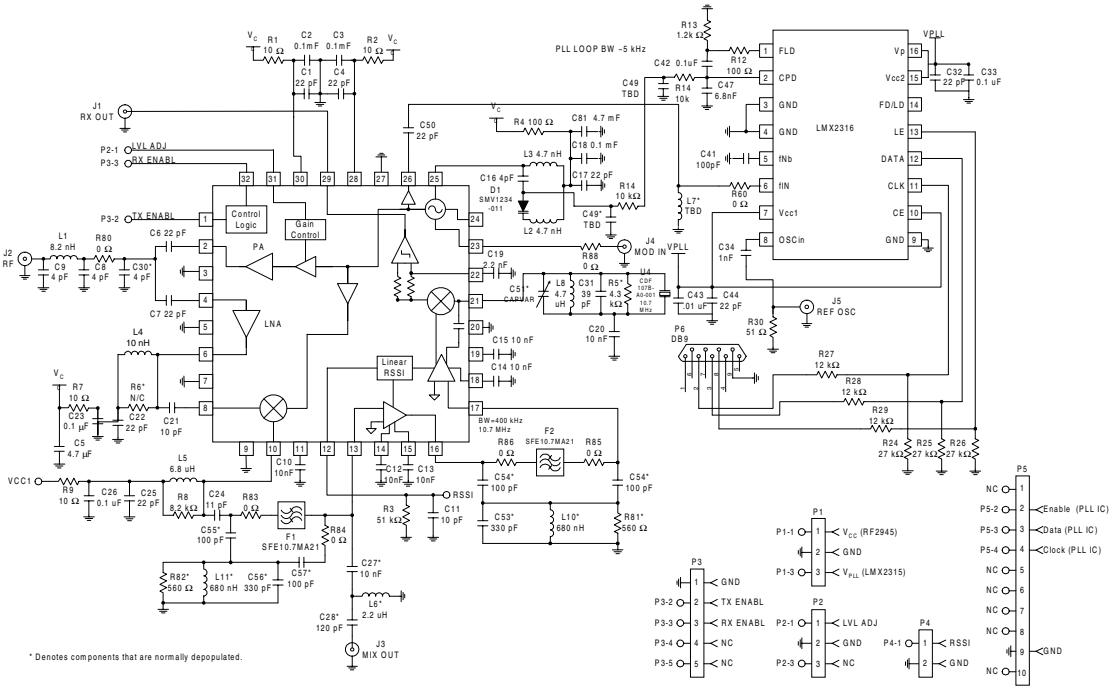


Application Schematic - 915 MHz IF=25MHz, BW=2MHz



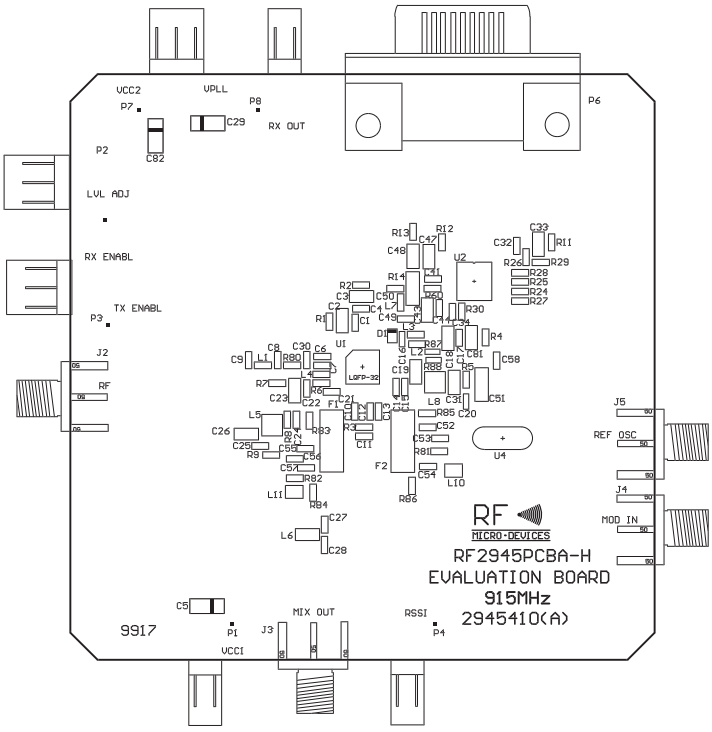
Evaluation Board Schematic

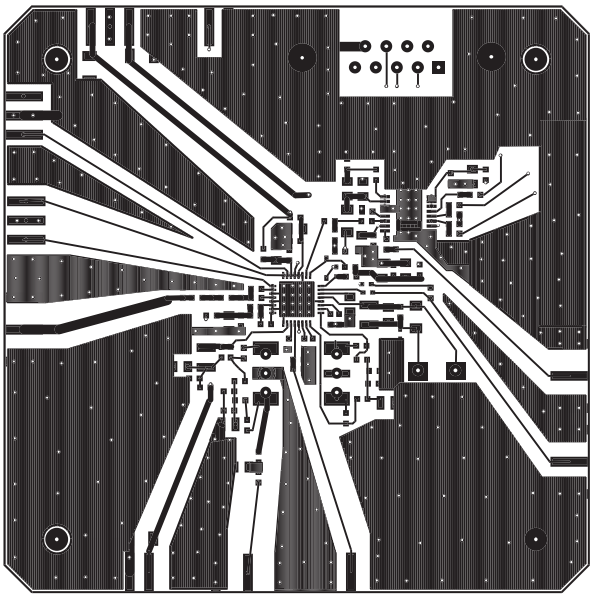
(Download Bill of Materials from www.rfmd.com.)

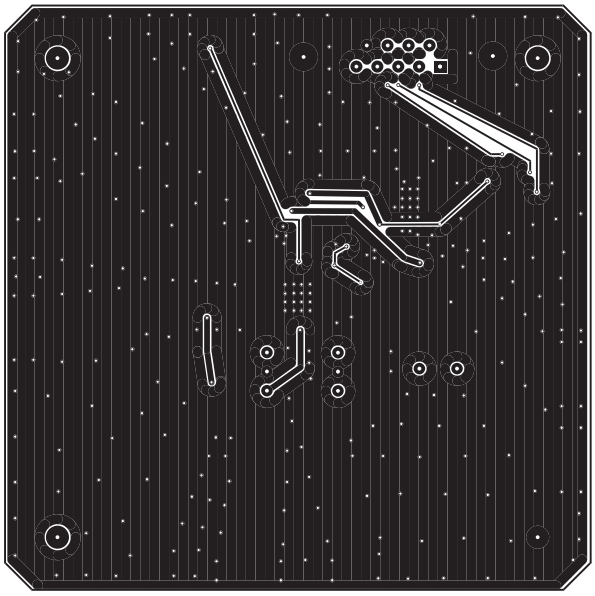


Evaluation Board Layout
Board Size 3.050” x 3.050”

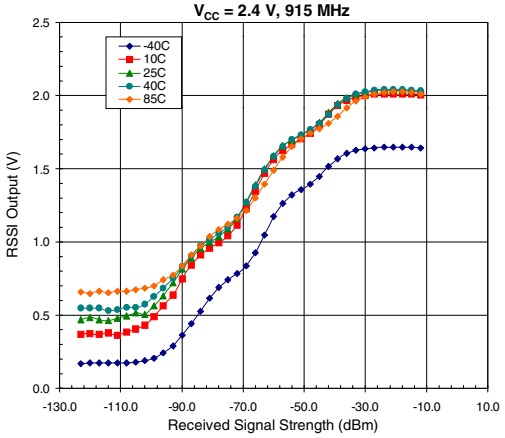
Board Thickness 0.031”, Board Material FR-4



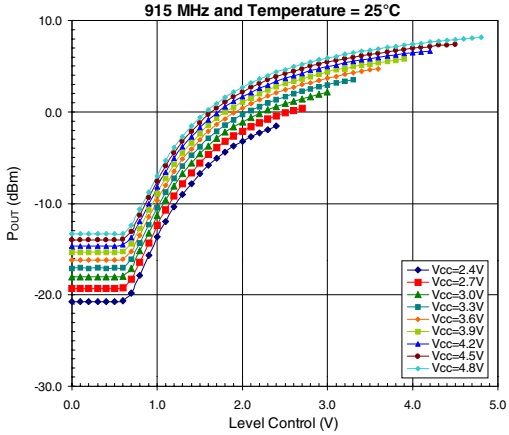




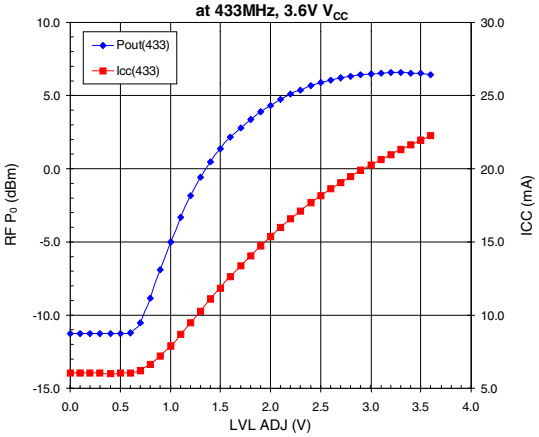
RSSI Output versus Temperature
V_{CC} = 2.4 V, 915 MHz



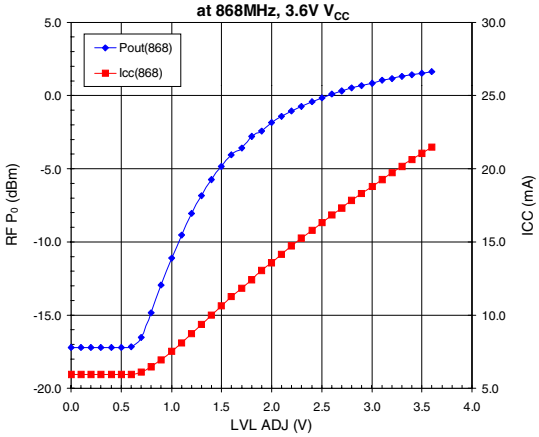
P_{OUT} versus Level Control and V_{CC}
915 MHz and Temperature = 25°C



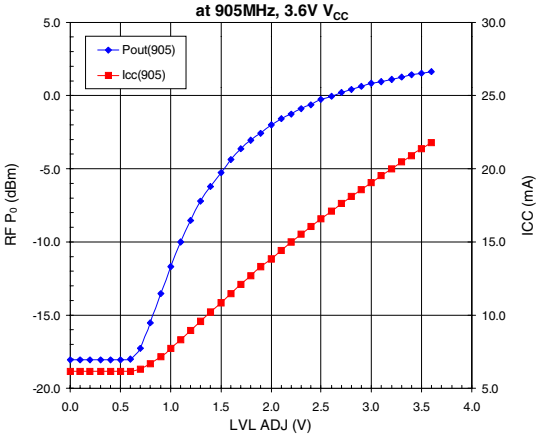
TX Power Output and ICC versus Level Adjust
at 433MHz, 3.6V V_{CC}



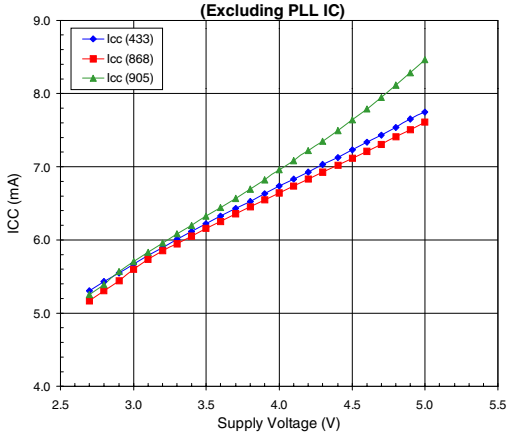
TX Power Output and ICC versus Level Adjust
at 868MHz, 3.6V V_{CC}



TX Power Output and ICC versus Level Adjust
at 905MHz, 3.6V V_{CC}



Receive Current versus V_{CC}
(Excluding PLL IC)



RF9901

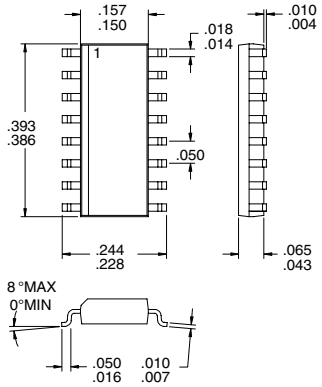
FSK TRANSMITTER

Typical Applications

- Handheld POS Terminals
- General Purpose 868 and 915MHz ISM Band Applications
- Digital Communication Systems
- Commercial and Consumer Products

Product Description

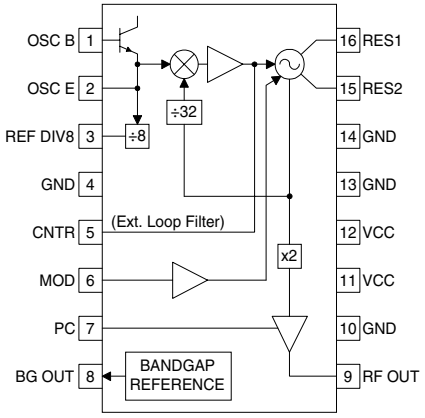
The RF9901 is a monolithic integrated circuit intended for use as a low-cost FSK transmitter. The unit is provided in 16-lead plastic packaging, and is designed to mate directly with the RF9902 FSK receiver. The two-chip set provides all functions necessary to implement a binary FSK transceiver for such applications as 868/915MHz ISM-band handheld terminals for POS, meter-reading, bar-code reading; as well as other digital applications such as SMR. The self-contained VCO and divide-by-32 circuitry simplify the system requirements, and the on-chip bandgap reference provides temperature stability and minimizes process variations. The part operates from a 3V to 5V supply, with no negative voltage required.



Package Style: SOP-16

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V to 5V Supply
- Direct Binary FSK Modulation
- On-Chip Divider for PLL
- Output Power up to +4dBm
- On-Chip VCO
- 400MHz to 930MHz Operation

11

TRANSCEIVERS

Ordering Information

RF9901	FSK Transmitter
RF9901 PCBA	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF9901

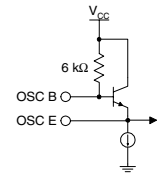
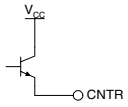
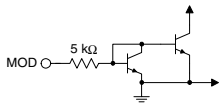
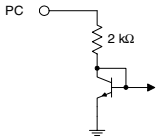
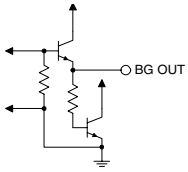
Absolute Maximum Ratings

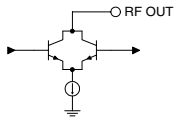
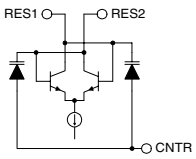
Parameter	Rating	Unit
Supply Voltage V_{CC}	-0.5 to +7.5	V_{DC}
Input Modulation Level	V_{CC}	V
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.0V, V_{PC}=+3.5V, Freq=915MHz
Reference Frequency		F_C/64		Hz	Set by external crystal
PLL Lock Time			10	ms	
Modulation Type		Binary FSK			
Modulation Frequency		10 to 500		kHz	
Modulation Input Level	0		V_{CC}	V	
VCO Sensitivity		25		MHz/V	
Phase Detector Sensitivity		0.4		µA/°	
RF Output					
RF Output Frequency Range		400 to 930		MHz	
Output Power		0	+4	dBm	
Output Power in Off Mode			-10	dBm	
Output Impedance		2		kΩ	Open Collector Output
Harmonic Output			-30	dBc	
Other Spurious Components			-30	dBc	
Power Supply					
Voltage		3.0 to 5.0		V	
Current		30		mA	

Pin	Function	Description	Interface Schematic
1	OSC B	Oscillator base. The application schematic shows a typical Colpitts oscillator circuit. This pin may be driven by an external source. If so, it should be AC coupled using a capacitor. The level should be about 500mV$_{PP}$	
2	OSC E	Oscillator emitter. See pin 1 description.	See pin 1.
3	REF DIV8	Reference Oscillator Divide By Eight output. This output can be used as a reference frequency for other circuitry. Leave this pin unconnected if this signal is not used.	
4	GND	Ground. This pin should be connected to the ground plane as close to the package as possible. A recommended method is to put a via through to the backside ground plane either in the pad or connected to the pad to which the pin is soldered.	
5	CNTR	Loop filter. A series RC network to ground is needed to stabilize the loop. The smaller the capacitance, the higher the loop bandwidth will be. The lockup time specified is for a capacitor value of 50nF or less. The lockup time may be varied by changing these values. Note that loop lockup time is also a function of the VCO resonator setting. Fastest lock time results when the VCO resonator is set to resonate at just above F_O with the control voltage forced to V_{CC} / 2. The loop is a classical type 2 loop, consisting of a "lead" resistor and a capacitor, and the associated calculations can be used.	
6	MOD	Digital modulation input. The upper frequency limit of this input is 500kHz. The lower frequency limit is set by the loop filter. If the duty cycle of the input is 50%, then the frequency deviation at the output will be symmetric about the carrier frequency. Duty cycles of other than 50% will result in an asymmetric frequency deviation where the carrier frequency will not be centered between the two output frequencies. The amplitude of the modulation input sets the amount of frequency deviation. A larger amplitude results in a larger deviation. The modulation input is designed to be driven by a logic level (0V and V_{CC}). With no external resistor, the maximum modulation is > 500kHz. A series resistor is used to reduce the modulation (frequency deviation) to the desired amount. Note that the modulation is applied to an internal varactor in the VCO circuit causing the PLL to attempt to "correct" the deviation. It is therefore necessary to make the loop time constant sufficiently long (slow) so that this "correction" does not take place.	
7	PC	Power control input. When at 0V, the output amplifier is disabled. At positive voltages above 1V, the output power is turned on. The higher the voltage, the higher the power. If the full power supply voltage is to be connected to this pin, a series resistor of 1.5kΩ should be placed in series with the pin. Note that the sensitivity of this voltage was deliberately set so that maximum power could be obtained with a very low voltage.	
8	BG OUT	Bandgap reference voltage output. The output voltage is 1.1V. The maximum current drain is about 1mA. If a long lead is used to connect this pin, a series resistor should be used to prevent the lead from causing oscillation.	

9	**RF OUT**	Power amplifier output. There must be a DC connection to V_{CC}, typically through an RF choke. The recommended circuit is shown in the application schematic. It uses inductors to feed DC to the PA collector. The output frequency is the crystal frequency multiplied by 64. If the output is properly matched into 50Ω, then greater than +4dBm output power can be achieved. Output power is also dependent upon the operating frequency.	
10	**GND**	Ground. See pin 4 description.	
11	**VCC**	Power supply voltage input. This pin is used to supply the operating voltage. This pin should be bypassed to ground as close to the package as possible.	
12	**VCC**	Power supply voltage input. See pin 11 description.	
13	**GND**	Ground. See pin 4 description.	
14	**GND**	Ground. See pin 4 description.	
15	**RES2**	VCO resonator. There must be a DC path to V_{CC} on these pins. Chip inductors are recommended. The values of the inductors connected to pins 15 and 16 must also change depending on the required F_O. As the inductor values increase, the output frequency will decrease. At 915MHz, 18nH is recommended. At 450MHz, 56nH is recommended. The maximum DC voltage at the resonator pins is 4.5V. Therefore, a series resistor will improve the locking of the PLL depending upon the supply voltage. The resistor should be placed between V_{CC} and the choke inductor L3. A recommended resistor value at 5.0V is 500Ω. At 6.0V, the resistor value will increase to approximately 1kΩ.	
16	**RES1**	VCO resonator. See pin 15 description.	See pin 15.

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RF9901 Evaluation Board Crystal Oscillator

Background

The RF9901 is an FSK transmitter that can be used to transmit FSK data using an RF carrier frequency in the range of 400MHz to 930MHz. This device is intended for and ideally suited to both European and United States ISM band applications.

The RF9901 evaluation board (RFMD Part Number RF9901PCBA) utilizes a Colpitts oscillator to generate the reference frequency for the PLL phase detector. The PLL consists of an integrated voltage controlled oscillator (VCO), a divide by 32 prescaler, and a reference frequency oscillator amplifier. The output carrier frequency is then the reference frequency multiplied by 64.

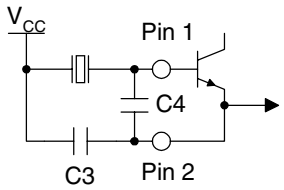
Which Topology?

The Colpitts oscillator is only one of many types of oscillators that could have been used and was chosen primarily for its low parts count. Other oscillators have various trade-offs for the designer which may result in choosing another oscillator type.

This article does not delve into oscillator design, but is simply to provide assistance in understanding why the particular crystal was chosen and what the general topology of the oscillator used on the evaluation board is. There are many references available to aid the designer who wishes to better understand the Colpitts oscillator and oscillator design in general.

Colpitts Topology

The basic topology of the Colpitts oscillator used is below:



The transistor is acting as an emitter-follower. The voltage gain is set by capacitors C3 and C4 which are acting as a tapped capacitive impedance transformer. The output power and frequency of the crystal oscillator can be optimized by adjusting C3 and C4. The frequency can be tuned by placing an adjustable inductor in series with the crystal.

What Type of Crystal?

After determining which type of oscillator was going to be used, a crystal needed to be chosen. The Colpitts crystal oscillator can use either a parallel or series resonant crystal. Examples of oscillators using each type of crystal would be fundamental mode and third overtone, respectively.

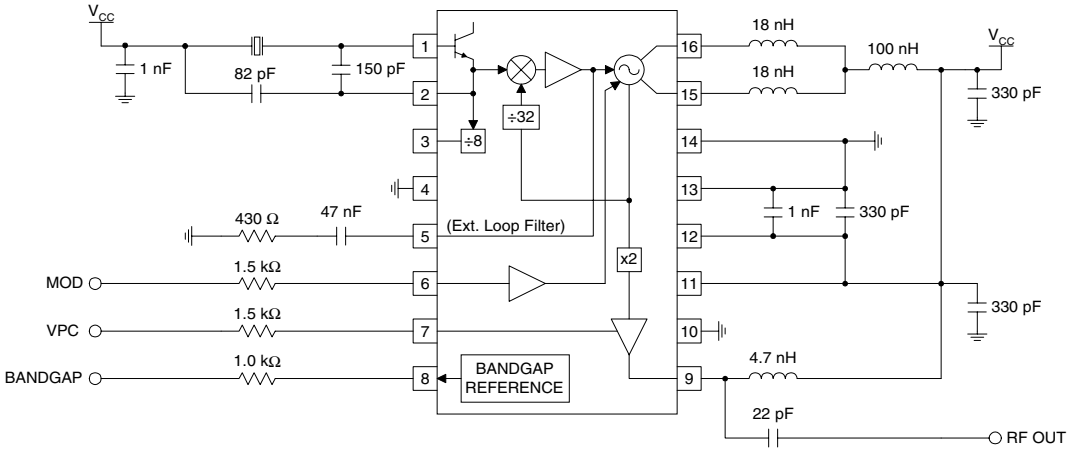
For our application, since we are using a fundamental mode common-emitter Colpitts oscillator, a parallel resonant crystal was chosen. For the RF9901 we wanted an RF output frequency of 916MHz, so we chose a crystal whose frequency is 14.31818MHz, resulting in an RF output frequency of 64x14.31818MHz=916.36MHz.

Which Crystal?

Specifically, a crystal manufactured by Epson America, Inc. which is available from Digi-Key, is used. It is a cylinder-type quartz crystal, type CA-301. The Epson part number is CA-301 14.31818M-C. This crystal has the following properties:

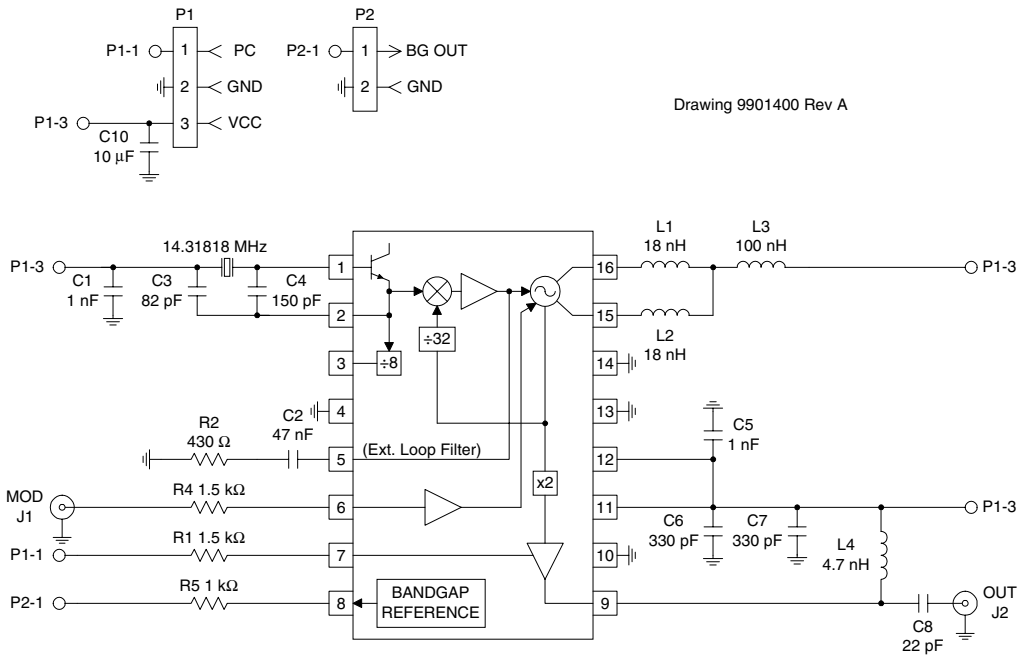
Specification	Value
Operating Temperature	-20°C to +70°C
Maximum Drive Level	2mW Max
Recommended Level	10mW to 100mW
Frequency Tolerance	±30ppm
Load Capacitance	18pF
Series Resistance	50Ω Max

Application Schematic



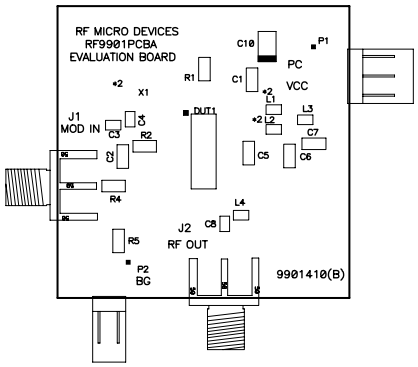
Evaluation Board Schematic

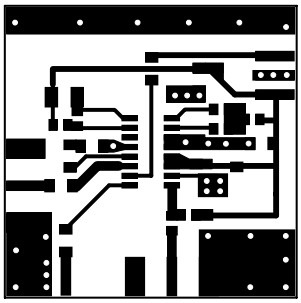
(Download Bill of Materials from www.rfmd.com.)



Component values for 916 MHz output frequency (F0). The output frequency is related to the crystal frequency (Fref) by F0 = Fref x 64. L1 and L2 must also change depending on the required F0.

Evaluation Board Layout





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RF9902

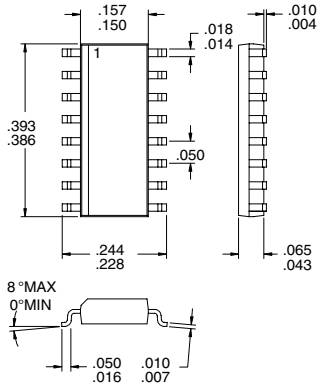
FSK RECEIVER

Typical Applications

- Handheld POS Terminals
- General Purpose 868 and 915MHz ISM Band Applications
- Digital Communication Systems
- Commercial and Consumer Systems

Product Description

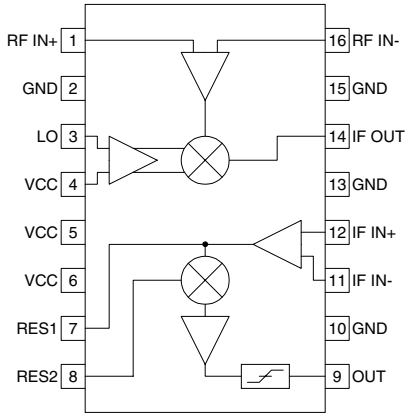
The RF9902 is a monolithic integrated circuit intended for use as a low-cost FSK receiver. The unit is provided in 16-lead plastic SOIC packaging, and is designed to operate with the RF9901 FSK transmitter. The two-chip set provides all functions necessary to implement a binary FSK transceiver for such applications as 868/915MHz ISM-band handheld terminals for POS, meter-reading, bar-code reading; as well as other digital applications such as SMR. The part contains the input amplifier, mixer, IF limiting amplifier, phase detector, and an output Schmitt trigger to generate the FSK digital signal. The part operates from a 3V to 5V supply with no negative voltage required.



Package Style: SOP-16

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V to 5V Supply
- Fully Integrated FSK Receiver
- Direct Binary FSK Demodulation
- CMOS / TTL Output Levels
- 400MHz to 930MHz Operation
- RF9901 Compatible

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TRANSCEIVERS

Ordering Information

RF9902	FSK Receiver
RF9902 PCBA	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

RF9902

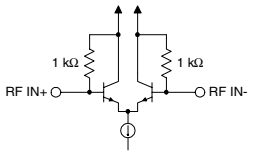
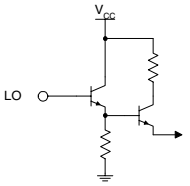
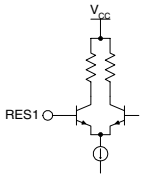
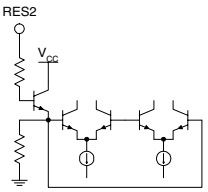
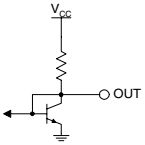
Absolute Maximum Ratings

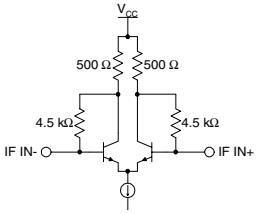
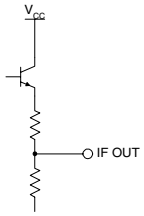
Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +7.0	V_{DC}
Input RF Power	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

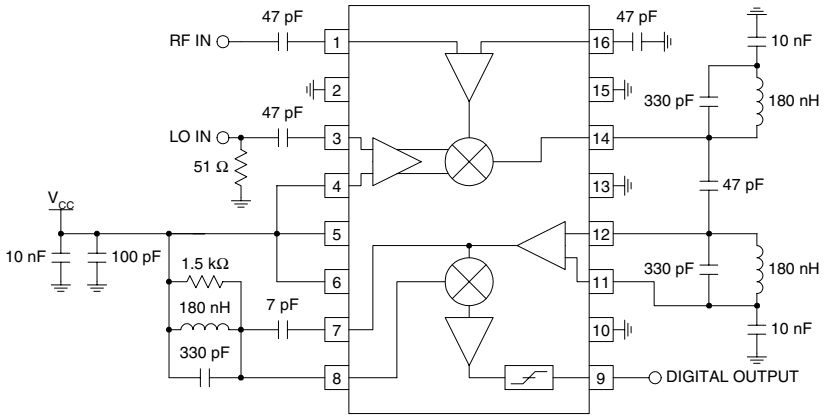
RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=+4.0V_{DC}
RF Frequency		400 to 930		MHz	
IF Frequency		3 to 30		MHz	Lower IF frequencies may be used. However, the IF amplifier is AC coupled and the IF gain rolls off significantly at low frequencies.
LO Frequency		270 to 960		MHz	
RF Gain		16		dB	
Overall Gain		108		dB	
Input IP3		-10		dBm	
Noise Figure		8			For maximum sensitivity applications, an external low noise amplifier with a gain of at least 10dB should be used. A noise image filter should be placed between the low noise amplifier and the RF9902's RF input.
Digital "0" Output Level			0.2	V	
Digital "1" Output Level	V_{CC}-0.2			V	
Polarity		"1"			$F_{IN}>F_{REF}$
Output Source/Sink Current	1			mA	
Mixer Output Resistance		500		Ω	
IF Input Resistance		500		Ω	
Power Supply					
Voltage		3.0 to 5.0		V	
Current		25		mA	

Pin	Function	Description	Interface Schematic
1	RF IN+	RF input. This port is internally biased but requires a DC blocking capacitor. The functionality of this pin and pin 16 may be interchanged.	
2	GND	Ground. This pin should be tied to the backside ground plane as close to the package as possible.	
3	LO	Local Oscillator input. This pin requires a DC blocking capacitor. The LO signal level should be between -6dBm and -3dBm for optimum performance.	
4	VCC	V_{CC}. This pin should be bypassed to ground as close to the package as possible using a chip capacitor.	
5	VCC	V_{CC}. This pin should be bypassed to ground as close to the package as possible using a chip capacitor.	
6	VCC	V_{CC}. This pin should be bypassed to ground as close to the package as possible using a chip capacitor.	
7	RES1	Provides the sampled IF signal phase shifted for the quadrature tank circuit connected to pin 8 using a capacitor. The value of the capacitor is typically 7pF for a 20MHz IF and will vary based upon the IF used.	
8	RES2	Quadrature tank circuit. The external resonator should be tied between this pin and V_{CC}. (V_{CC} is needed to DC bias the pin to the power voltage). The object of the tank circuit is to obtain a 90° phase shift between the ports of the demodulator at the center IF frequency. When at 90° the modulation comparator is near its threshold. It is the relative phase shift versus frequency which determines the modulation state of the signal. Ideally, the Q of the tank circuit should be such that the 3dB bandwidth is approximately equal to the modulated frequency shift of the carrier. Wider bandwidths are possible provided that the peak-to-peak phase shift is at least 45°.	
9	OUT	Digital output which indicates the modulation state of the carrier input. It is a logic signal, which when low, is equal to 0V plus a small offset (100mV). When high it indicates positive modulation and the voltage goes to within ~100mV of V_{CC}. The output circuit is a Schmitt Trigger to prevent "chatter" during transitions.	
10	GND	Ground. This pin should be tied to the backside ground plane as close to the package as possible.	

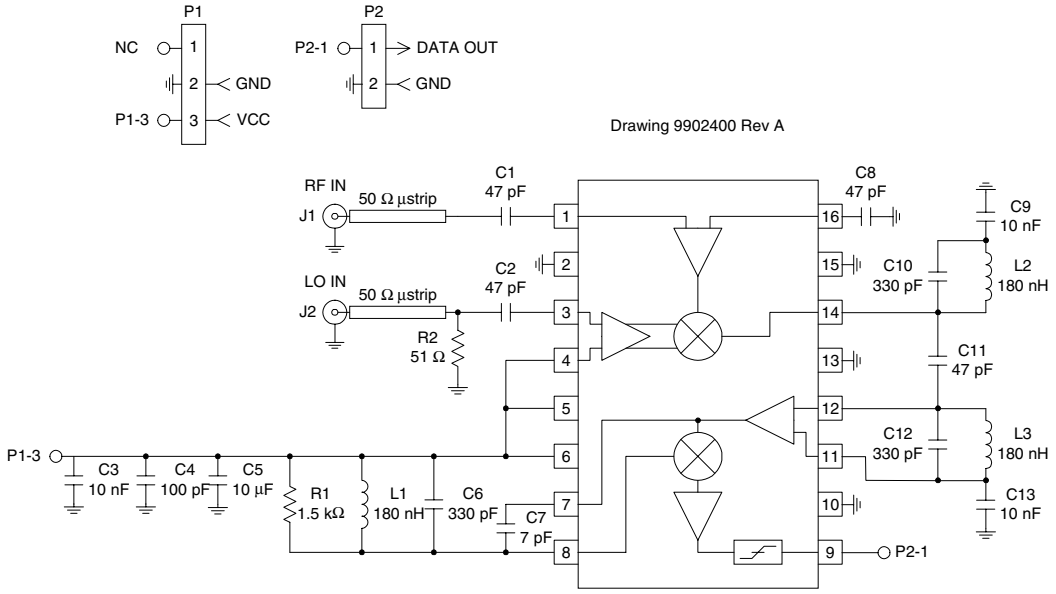
11	**IF IN-**	Complementary IF input from the IF filter. The input impedance is about 500Ω (each input). There may be a low impedance DC and high impedance AC path from pin 12 to this pin; or this pin and pin 12 may be a DC open. The DC from the mixer output must be blocked. This pin should be bypassed to ground near the package with a chip capacitor whose reactance is low at the IF frequency.	
12	**IF IN+**	IF input from the IF filter. The input impedance is about 500Ω (each input). There may be a low impedance DC and high impedance AC path from this pin to pin 11; or pin 11 and this pin may be a DC open. The DC from the mixer output must be blocked. Pin 11 should be bypassed to ground near the package with a chip capacitor whose reactance is low at the IF frequency.	See pin 11.
13	**GND**	Ground. This pin should be tied to the backside ground plane as close to the package as possible.	
14	**IF OUT**	Mixer output. This pin cannot be resistively (DC) loaded. A coupling capacitor or filter which has a high DC resistance should be connected to this pin. The circuitry around pin 12 and this pin is dependent on the filter type used. If a ceramic filter is used (open circuit DC path), this pin is tied to the input of the filter and the output is connected to pin 12. Pin 11 is then bypassed to ground with a chip capacitor near the package. The IF response is peaked at about 20MHz. The gain is sufficiently high, however, that an IF of 3MHz to 30MHz may be used with good results.	
15	**GND**	Ground. This pin should be tied to the backside ground plane as close to the package as possible.	
16	**RF IN-**	Out-of-phase RF input. This pin should be AC grounded as close to the package as possible using a chip capacitor. The functionality of this pin and pin 1 may be interchanged.	See pin 1.

Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

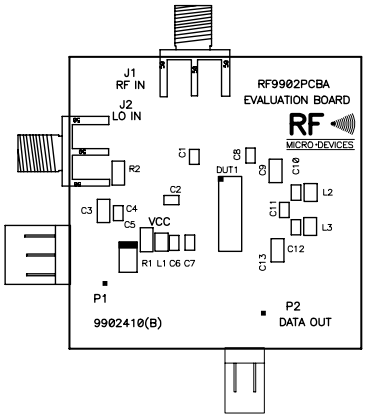


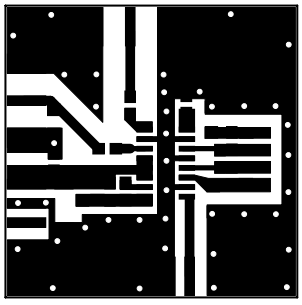
Note: Component Values for 20 MHz IF Frequency.

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TRANSCEIVERS

Evaluation Board Layout





12 VCOs

Part	Description	Frequency (MHz)	Vcc (Volts)	Icc (mA)	Output Power (dBm)	Package	Page
RF2504	VCO/High-Isolation Buffer Amplifier	700 to 1500	2.2 to 5.0	5.5	-6	SOP-8	12-1
RF2506	VHF/UHF VCO/High-Isolation Buffer Amplifier	10 to 1000	2.7 to 3.6	9	-3	SOP-8	12-9

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RF MICRO·DEVICES

Preliminary

RF2504

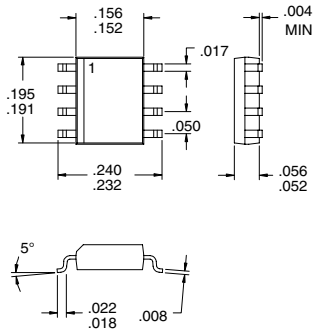
VCO/HIGH-ISOLATION BUFFER AMPLIFIER

Typical Applications

- 2-Way Paging
- ISM Band Systems
- Wireless Local Loop Systems
- GPS Receivers
- Cellular Systems
- Low Voltage Applications

Product Description

The RF2504 is an integrated oscillator and buffer amplifier chain designed to achieve extremely low sensitivity to fluctuations in load impedance and power supply noise, thereby greatly reducing load pulling and pushing. The IC offers great flexibility, yet is easy to use. This product was designed for use in applications with low supply voltages. It has a power-down feature and is designed to operate from 700MHz to 1500MHz with the help of an external resonator. Frequency control is achieved with an external varactor diode. The IC's ease of use, reduced load pulling, small size, and low cost make it an ideal LO (Local Oscillator) for almost any wireless application.



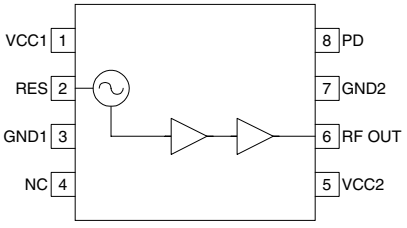
Package Style: SOP-8

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Features

- High-Isolation / Reduced Load Pulling
- Low Current Consumption
- -6dBm Output Power
- Digitally Controlled Power Down Mode
- 700MHz to 1500MHz Operating Range
- Single 2.2V to 5V Supply



Functional Block Diagram

Ordering Information

RF2504	VCO/High-Isolation Buffer Amplifier
RF2504 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

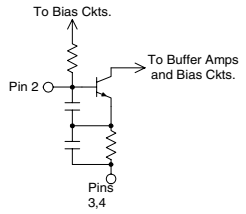
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.8	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5.8	V_{DC}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
Operating Frequency		700 to 1500		MHz	
915MHz Operation					T=25°C, V_{CC}=2.7V, Z_{LOAD}=50Ω, V_{PD}=2.7V
Output Power		-6		dBm	
2nd Harmonic		-8		dBc	
3rd Harmonic		-19		dBc	
Load Pulling		200		kHz	Into 1.67VSWR Load
V_{CC} Pushing		4.7		MHz/V	
Phase Noise		-104		dBc	100kHz Offset. Better phase noise is achievable at the expense of output power.
		-83		dBc	10kHz Offset
Power Supply					
Operating Voltage		2.2 to 5.0		V_{DC}	At 2.2V and -40°C, output power will be reduced to typically -11dBm.
Supply Current		5.5		mA	

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Pin	Function	Description	Interface Schematic
1	VCC1	Power supply connection for the VCO. This pin should be well bypassed close to the package with a capacitor suitable for the frequency of operation as well as a capacitor to minimize low frequency noise from the voltage supply. The ground side of the capacitors should connect immediately to ground plane.	
2	RES	Connection point for the resonator circuit. The resonator is an inductive element. Changing the effective inductance, either physically or with a varactor tuned circuit, will change the frequency of operation. Note that all parasitics on the circuit board will contribute to the effective inductance and will influence the frequency of operation. These effects become more pronounced at higher operating frequencies. This pin has DC bias present. A DC blocking capacitor, suitable for the frequency of operation, should be used if the external circuitry has DC present or presents a DC path to ground. See Application Example Schematic and Theory of Operation section of this data sheet for design details.	
3	GND1	Ground connection for the VCO. Keep traces physically short and connect immediately to ground plane for best performance. In order to minimize load pulling, it is recommended that pin 3 have a different return path to ground than pin 7 (i.e., separate vias to a common ground plane).	See Pin 2
4	NC	Not connected.	
5	VCC2	Power supply connection for the buffer amplifiers. This pin should be well bypassed close to the package with a capacitor suitable for the frequency of operation. The ground side of the capacitor should connect immediately to ground plane.	
6	RF OUT	RF output pin. This is an open-collector output and must be biased externally. A shunt bias/matching inductor to V_{CC} and a series blocking/matching capacitor are recommended. See Application Example Schematic.	
7	GND3	Ground connection for the buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance. In order to minimize load pulling, it is recommended that pin 3 have a different return path to ground than pin 7 (i.e., separate vias to a common ground plane).	
8	PD	Power Down pin for the VCO and buffer amplifiers. A logic “low” (0.0 to 0.7V) turns the entire device off and supply current drops to less than 1µA. A logic “high” (≥3.0V) turns the device on. Note that the voltage on this pin should never exceed 5.5V_{DC}.	

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Application Notes

The RF2504 has two functional parts: an oscillator and buffer amplifier. The functional blocks have separate ground and VCC pins to increase the isolation and reduce load pulling, one of the key design objectives. An external resonator is used to add design flexibility, and the loaded Q of this resonator will affect the performance of the resulting oscillator.

To create an oscillation, negative resistance is generated at pin 2 with a circuit similar to a Colpitts oscillator. The input impedance at pin 2, measured with a vector network analyzer, is shown here in the data sheet. In general, the impedance looks like a negative resistance in series with a capacitor. The negative resistance decays as the frequency increases. An oscillator is created when an inductive element is placed on pin 2 that is the conjugate of the capacitive reactance. A greater inductive element will create a lower frequency of oscillation.

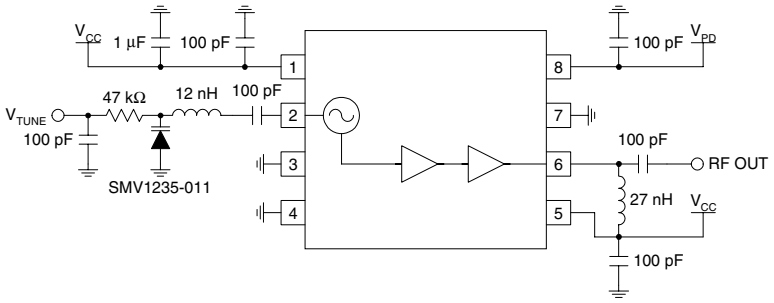
The S11 looking into pin 2 is also shown here in the data sheet. It has return gain from 500 MHz to 2200 MHz at room temperature. The specified frequency range of 750 MHz to 1500 MHz defines the region where the output power is relatively flat. At lower and higher frequencies, the power will tend to roll off from the nominal value. The specified frequency range is conservatively set to ensure oscillation and maintain performance, but the RF2504 can be used over a broader frequency range with degraded performance.

The overall Q of the external resonator will affect performance. Lower Q means lower power, higher phase noise, and more load pulling. If the Q is too low, the circuit will not oscillate. The IC is designed to oscillate into a resonator with Q>10. The performance is measured with a microstrip resonator or high quality inductor, which usually has a Q>50. These measurements define the best performance that can be expected from the ICs. Lower Q resonators, particularly those including a lossy varactor, might have degraded performance.

The specified output power is measured into a 50Ω load. The IC has a high output impedance, and if desired, output matching can be used to obtain more power by transforming 50Ω into a higher impedance. On the RF2504, this could be accomplished by simply changing the values of the external output inductor and capacitor.

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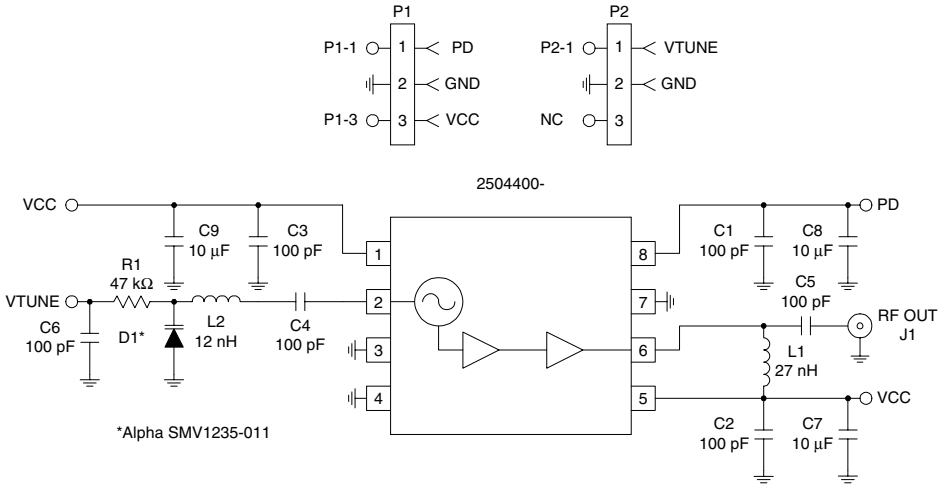
Application Schematic
915 MHz Operation



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Evaluation Board Schematic
915MHz Operation

(Download Bill of Materials from www.rfmd.com.)

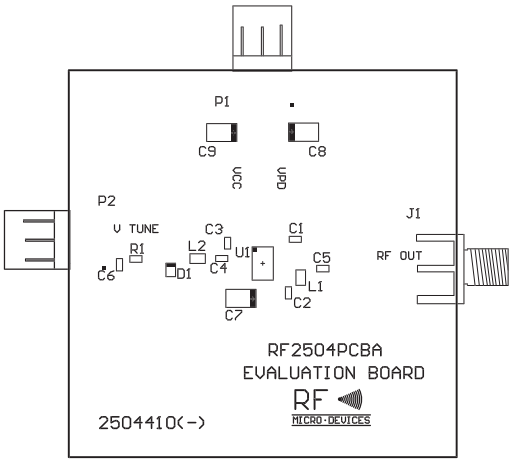


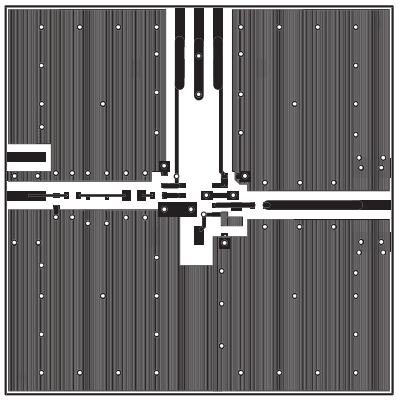
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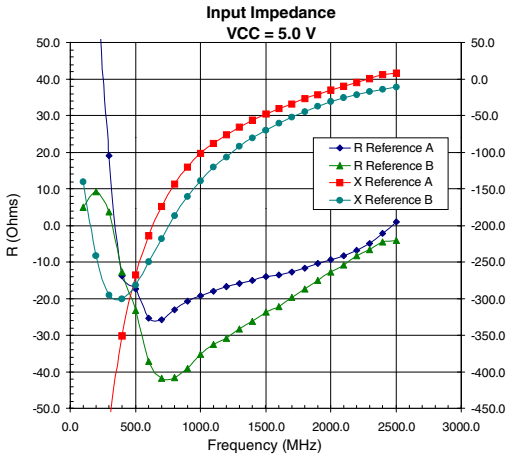
VCOs

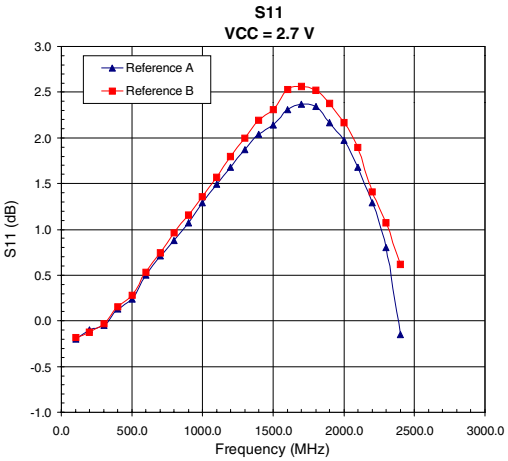
Db00.bk Page 7 Thursday, January 6, 2000 6:50 PM

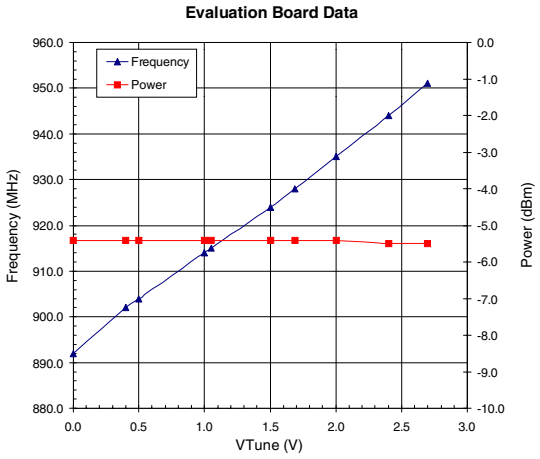
Evaluation Board Layout
915MHz Operation
Board Size 2.0” x 2.0”

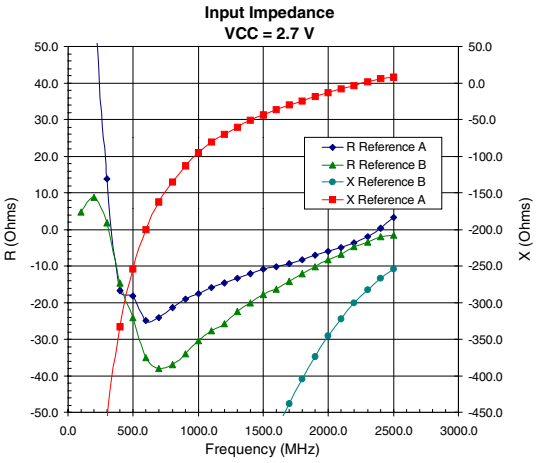


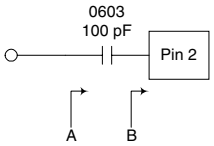












Reference positions for input impedance measurements of RF2504

12 VCOs

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MICRO·DEVICES

Preliminary

RF2506

VHF/UHF VCO/HIGH-ISOLATION BUFFER AMPLIFIER

Typical Applications

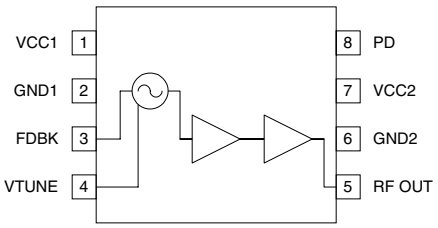
- Low Voltage
- Wireless LANs
- IF LO for 2.45GHz ISM Band Systems
- Wireless Local Loop
- Digital Cordless Phones

Product Description

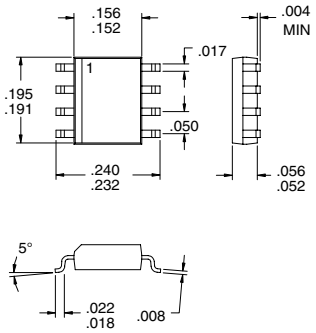
The RF2506 is an integrated oscillator and buffer amplifier chain designed to achieve low sensitivity to fluctuations in load impedance and power supply noise, while maintaining superior phase noise performance. The IC offers great flexibility, yet is easy to use. This product was designed for use in applications with low supply voltages. It has a power-down feature and is designed to operate from 10MHz to 1000MHz with the help of an external resonator. Frequency control is achieved with an external varactor diode. The IC's ease of use, reduced load pulling, small size, and low cost make it an ideal LO (Local Oscillator) for wireless applications in the VHF/UHF range. The RF2506 was designed to operate with the 2.4GHz chipset; specifically with the IF portion of the RF2518 PLL/synthesizer.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-8

Features

- High-Isolation/Reduced Load Pulling
- Low Current Consumption
- -7dBm Output Power
- Digitally Controlled Power Down Mode
- 10MHz to 1GHz Operating Range
- Single 2.7V to 3.6V Supply

Ordering Information

RF2506	VHF/UHF VCO/High-Isolation Buffer Amplifier
RF2506 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

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VCOs

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Absolute Maximum Ratings

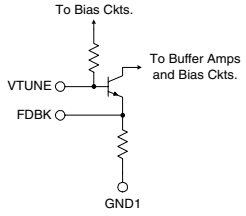
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.8	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +5.8	V_{DC}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

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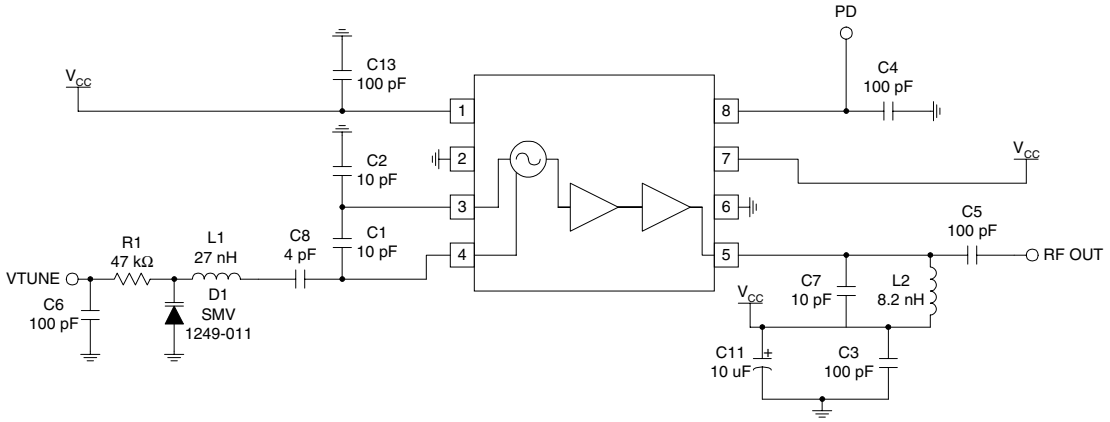
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
Operating Frequency		10 to 1000		MHz	
560MHz Operation					T=25°C, V_{CC}=2.7V, Z_{LOAD}=50Ω, V_{PD}=2.7V, O/P terminated into LC. Characterized @ 560MHz as per eval board. Data will change depending on frequency of operation and resonant tank network.
Output Power		-3		dBm	
2nd Harmonic		-27		dBc	
3rd Harmonic		-35		dBc	
Load Pulling		50		kHz_{P-P}	Into 1.75 VSWR Load
V_{CC} Pushing		190		kHz/V	Supply sweep from 2.7V to 3.2V
Phase Noise		-110		dBc	100kHz Offset. Better phase noise is achievable by increasing the loaded Q of the resonator circuit.
		-90		dBc	10kHz Offset
560MHz Operation					T=25°C, V_{CC}=2.7V, Z_{LOAD}=50Ω, V_{PD}=2.7V, O/P terminated in 50Ω. Characterized @ 560MHz as per eval board. Data will change depending on frequency of operation and resonant tank network.
Output Power		-7		dBm	
2nd Harmonic		-11.5		dBc	
3rd Harmonic		-15.5		dBc	
Load Pulling		35		kHz_{P-P}	Into 1.75 VSWR Load
V_{CC} Pushing		160		kHz/V	Supply sweep from 2.7V to 3.2V
Phase Noise		-107		dBc	100kHz Offset. Better phase noise is achievable by increasing the loaded Q of the resonator circuit.
		-88		dBc	10kHz Offset
Power Supply					
Operating Voltage		2.7 to 3.6		V_{DC}	At 2.2V and -40°C, output power will be reduced to typically -11dBm.
Supply Current		9		mA	

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Pin	Function	Description	Interface Schematic
1	VCC1	Power supply connection for the VCO. This pin should be well bypassed close to the package with a capacitor suitable for the frequency of operation as well as a capacitor to minimize low frequency noise from the voltage supply. The ground side of the capacitors should connect immediately to ground plane.	
2	GND1	Ground connection for the VCO. Keep traces physically short and connect immediately to ground plane for best performance. In order to minimize load pulling, it is recommended that pin 2 has a different return path to ground than pin 6 (i.e., separate vias to a common ground plane).	See pin 2.
3	FDBK	Feedback output to resonant circuit. A Colpitts oscillator is formed by placing a capacitor from this pin to pin 4 and from this pin to ground. A DC blocking capacitor, suitable for the frequency of operation, should be used if the external circuitry has DC present or presents a DC path to ground. See the application schematic of this data sheet for design details.	See pin 4.
4	VTUNE	Tank circuit input. A resonant circuit is placed from this pin to ground. The capacitive side is tapped to the FDBK point and the inductive side includes a varactor for voltage tuning to provide the VCO function. A DC blocking capacitor, suitable for the frequency of operation, should be used if the external circuitry has DC present or presents a DC path to ground. See the application schematic of this data sheet for design details.	
5	RF OUT	RF output pin. This is an open-collector output and must be biased externally. A shunt bias/matching inductor to V_{CC} and a series blocking/matching capacitor are recommended. See Application Example Schematic.	
6	GND2	Ground connection for the buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance. In order to minimize load pulling, it is recommended that pin 2 has a different return path to ground than pin 6 (i.e., separate vias to a common ground plane).	
7	VCC2	Power supply connection for the buffer amplifiers. This pin should be well bypassed close to the package with a capacitor suitable for the frequency of operation. The ground side of the capacitor should connect immediately to ground plane.	
8	PD	Power Down pin for the VCO and buffer amplifiers. A logic “low” (0.0 to 0.7V) turns the entire device off and supply current drops to less than 1μA. A logic “high” (≥3.0V) turns the device on. Note that the voltage on this pin should never exceed 5.5V_{DC}.	

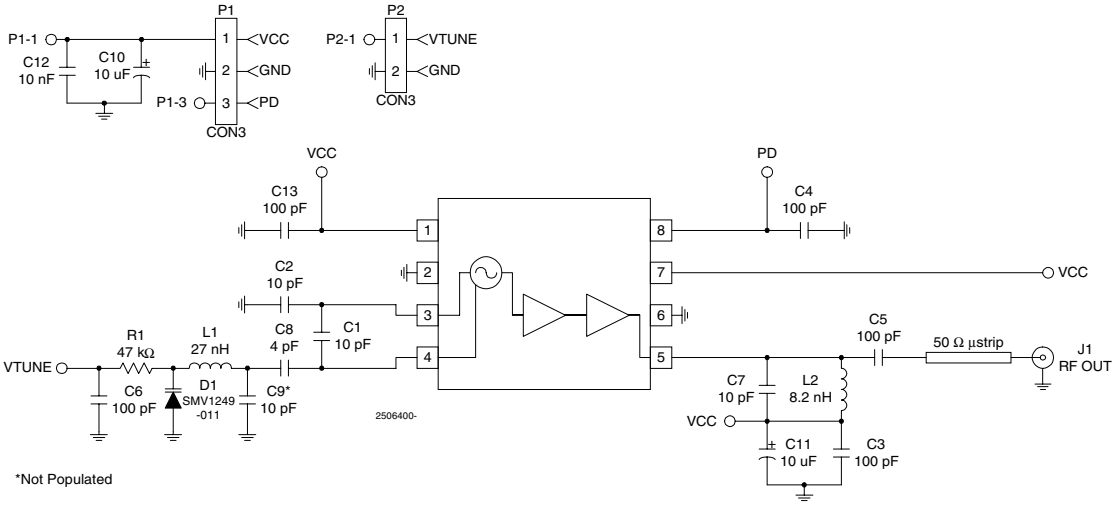
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Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



*Not Populated

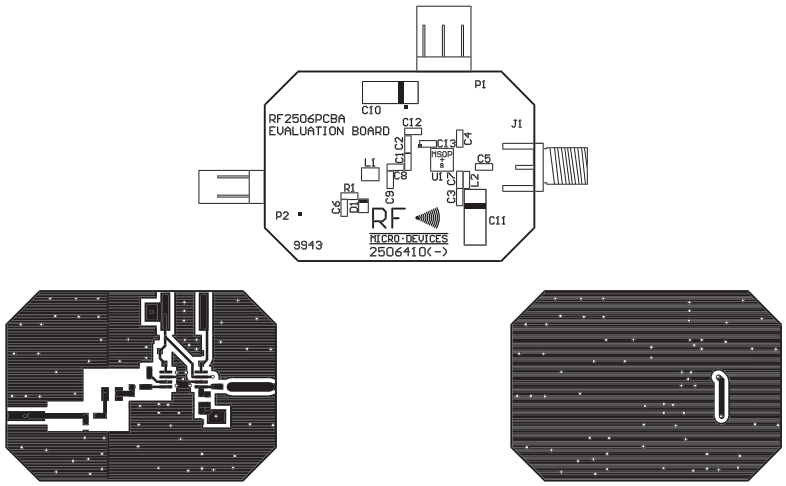
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VCOs

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Evaluation Board Layout 900MHz
Board Size 1.404" x 0.986"

Board Thickness 0.031”, Board Material FR-4



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13 Technical Notes and Articles

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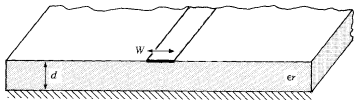
For 50Ω System

dBm	mW	dBmV	mV_{RMS}	mV_P	mV_{PP}
-50	0.000	-3.0	0.7	1.0	2.0
-45	0.000	2.0	1.3	1.8	3.6
-40	0.000	7.0	2.2	3.2	6.3
-35	0.000	12.0	4.0	5.6	11.2
-30	0.001	17.0	7.1	10.0	20.0
-25	0.003	22.0	12.6	17.8	35.6
-20	0.010	27.0	22.4	31.6	63.2
-15	0.032	32.0	39.8	56.2	112.5
-10	0.100	37.0	70.7	100.0	200.0
-5	0.316	42.0	125.7	177.8	355.7
0	1.000	47.0	223.6	316.2	632.5
1	1.259	48.0	250.9	354.8	709.6
2	1.585	49.0	281.5	398.1	796.2
3	1.995	50.0	315.9	446.7	893.4
4	2.512	51.0	354.4	501.2	1002.4
5	3.162	52.0	397.6	562.3	1124.7
6	3.981	53.0	446.2	631.0	1261.9
7	5.012	54.0	500.6	707.9	1415.9
8	6.310	55.0	561.7	794.3	1588.7
9	7.943	56.0	630.2	891.3	1782.5
10	10.000	57.0	707.1	1000.0	2000.0
11	12.589	58.0	793.4	1122.0	2244.0
12	15.849	59.0	890.2	1258.9	2517.9
13	19.953	60.0	998.8	1412.5	2825.1
14	25.119	61.0	1120.7	1584.9	3169.8
15	31.623	62.0	1257.4	1778.3	3556.6
16	39.811	63.0	1410.9	1995.3	3990.5
17	50.119	64.0	1583.0	2238.7	4477.4
18	63.096	65.0	1776.2	2511.9	5023.8
19	79.433	66.0	1992.9	2818.4	5636.8
20	100.000	67.0	2236.1	3162.3	6324.6
21	125.893	68.0	2508.9	3548.1	7096.3
22	158.489	69.0	2815.0	3981.1	7962.1
23	199.526	70.0	3158.5	4466.8	8933.7
24	251.189	71.0	3543.9	5011.9	10023.7
25	316.228	72.0	3976.4	5623.4	11246.8
26	398.107	73.0	4461.5	6309.6	12619.1
27	501.187	74.0	5005.9	7079.5	14158.9
28	630.957	75.0	5616.7	7943.3	15886.6
29	794.328	76.0	6302.1	8912.5	17825.0
30	1000.000	77.0	7071.1	10000.0	20000.0

For 75Ω System

dBm	mW	dBmV	mV_{RMS}	mV_{P}	mV_{PP}
-50	0.000	-1.2	0.9	1.2	2.4
-45	0.000	3.8	1.5	2.2	4.4
-40	0.000	8.8	2.7	3.9	7.7
-35	0.000	13.8	4.9	6.9	13.8
-30	0.001	18.8	8.7	12.2	24.5
-25	0.003	23.8	15.4	21.8	43.6
-20	0.010	28.8	27.4	38.7	77.5
-15	0.032	33.8	48.7	68.9	137.7
-10	0.100	38.8	86.6	122.5	244.9
-5	0.316	43.8	154.0	217.8	435.6
0	1.000	48.8	273.9	387.3	774.6
1	1.259	49.8	307.3	434.6	869.1
2	1.585	50.8	344.8	487.6	975.2
3	1.995	51.8	386.8	547.1	1094.1
4	2.512	52.8	434.0	613.8	1227.7
5	3.162	53.8	487.0	688.7	1377.4
6	3.981	54.8	546.4	772.8	1545.5
7	5.012	55.8	613.1	867.1	1734.1
8	6.310	56.8	687.9	972.8	1945.7
9	7.943	57.8	771.8	1091.6	2183.1
10	10.000	58.8	866.0	1224.7	2449.5
11	12.589	59.8	971.7	1374.2	2748.4
12	15.849	60.8	1090.3	1541.9	3083.7
13	19.953	61.8	1223.3	1730.0	3460.0
14	25.119	62.8	1372.6	1941.1	3882.2
15	31.623	63.8	1540.0	2177.9	4355.9
16	39.811	64.8	1727.9	2443.7	4887.4
17	50.119	65.8	1938.8	2741.9	5483.7
18	63.096	66.8	2175.4	3076.4	6152.8
19	79.433	67.8	2440.8	3451.8	6903.6
20	100.000	68.8	2738.6	3873.0	7746.0
21	125.893	69.8	3072.8	4345.6	8691.1
22	158.489	70.8	3447.7	4875.8	9751.6
23	199.526	71.8	3868.4	5470.7	10941.5
24	251.189	72.8	4340.4	6138.3	12276.5
25	316.228	73.8	4870.0	6887.2	13774.5
26	398.107	74.8	5464.3	7727.6	15455.2
27	501.187	75.8	6131.0	8670.5	17341.1
28	630.957	76.8	6879.1	9728.5	19457.0
29	794.328	77.8	7718.5	10915.6	21831.1
30	1000.000	78.8	8660.3	12247.4	24494.9

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$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + 12\,d\,/\,W}}$$

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_e}} \cdot \ln\left(\dfrac{8d}{W} + \dfrac{W}{4d}\right) & \text{for } \dfrac{W}{d} \le 1 \\ \dfrac{120\,\pi}{\sqrt{\varepsilon_e} \cdot \left(\dfrac{W}{d} + 1.393 + 0.667 \cdot \ln\left(\dfrac{W}{d} + 1.444\right)\right)} & \text{for } \dfrac{W}{d} \ge 1 \end{cases}$$

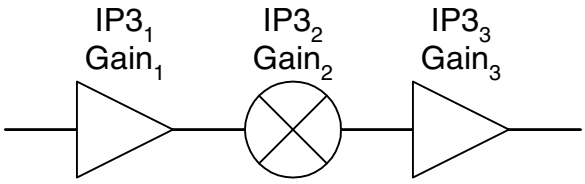
For further details on those formulas please refer to:
I.J. Bahl and D.K. Trivedi, "A Designer's Guide to Microstrip Line", Microwaves, May 1977, pp. 174-182

Dielectric Constant	Width/Height (W/d)	Effective Dielectric Constant	Characteristic Impedance
4.8	0.5	3.28	92.1
4.8	0.8	3.38	75.8
4.8	1	3.43	68.1
4.8	1.2	3.47	62.4
4.8	1.3	3.49	59.9
4.8	1.4	3.51	57.6
4.8	1.5	3.53	55.5
4.8	1.6	3.55	53.6
4.8	1.7	3.57	51.7
4.8	1.8	3.59	50.0
4.8	1.9	3.60	48.5
4.8	2	3.62	47.0
4.8	2.2	3.65	44.3
4.8	2.5	3.69	40.8
4.8	3	3.75	36.1
4.8	4	3.85	29.5
4	0.5	2.80	99.7
4	0.8	2.88	82.2
4	1	2.92	73.9
4	1.2	2.95	67.7
4	1.3	2.97	65.0
4	1.4	2.98	62.5
4	1.5	3.00	60.2
4	1.6	3.01	58.1
4	1.7	3.03	56.2
4	1.8	3.04	54.3
4	1.9	3.05	52.6
4	2	3.07	51.0
4	2.2	3.09	48.1
4	2.5	3.12	44.4
4	3	3.17	39.3
4	4	3.25	32.1
2.55	0.5	1.93	120.1
2.55	0.8	1.97	99.3
2.55	1	1.99	89.4
2.55	1.2	2.01	82.1
2.55	1.3	2.02	78.8
2.55	1.4	2.03	75.9
2.55	1.5	2.03	73.2
2.55	1.6	2.04	70.6
2.55	1.7	2.05	68.3
2.55	1.8	2.05	66.1
2.55	1.9	2.06	64.1
2.55	2	2.07	62.2
2.55	2.2	2.08	58.7
2.55	2.5	2.10	54.1
2.55	3	2.12	48.0
2.55	4	2.16	39.3

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Return Loss (dB)	$\lvert\Gamma_O\rvert$	VSWR	Insertion Loss (dB)	Power Transmitted (%)	Power Reflected (%)
-1.0	0.891	17.391	-6.87	20.57%	79.43%
-1.5	0.841	11.610	-5.35	29.21%	70.79%
-2.0	0.794	8.724	-4.33	36.90%	63.10%
-2.5	0.750	6.997	-3.59	43.77%	56.23%
-3.0	0.708	5.848	-3.02	49.88%	50.12%
-3.5	0.668	5.030	-2.57	55.33%	44.67%
-4.0	0.631	4.419	-2.20	60.19%	39.81%
-4.5	0.596	3.946	-1.90	64.52%	35.48%
-5.0	0.562	3.570	-1.65	68.38%	31.62%
-6.0	0.501	3.010	-1.26	74.88%	25.12%
-7.0	0.447	2.615	-0.97	80.05%	19.95%
-8.0	0.398	2.323	-0.75	84.15%	15.85%
-9.0	0.355	2.100	-0.58	87.41%	12.59%
-10.0	0.316	1.925	-0.46	90.00%	10.00%
-15.0	0.178	1.433	-0.14	96.84%	3.16%
-20.0	0.100	1.222	-0.04	99.00%	1.00%
-25.0	0.056	1.119	-0.01	99.68%	0.32%
-30.0	0.032	1.065	0.00	99.90%	0.10%
-35.5	0.017	1.034	0.00	99.97%	0.03%
-40.0	0.010	1.020	0.00	99.99%	0.01%

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The cascaded IP3 for the above is calculated using the equation

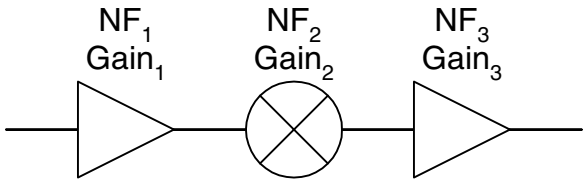
$$IP_{TOT} = \frac{1}{\frac{1}{IP3_1} + \frac{Gain_1}{IP3_2} + \frac{Gain_1 \cdot Gain_2}{IP3_3} + \ldots}$$

Use the linear terms for IP3 and Gain in the above equations, not the decibel form, ie.:

$$Gain_n = 10^{\frac{Gain_n(dB)}{10}}$$

$$IP3_n = 10^{\frac{IP3_n(dB)}{10}}$$

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The cascaded noise figure for the above is calculated using the equation

$$NF_{TOT} = NF_1 + \frac{NF_2 - 1}{Gain_1} + \frac{NF_3 - 1}{Gain_2 \cdot Gain_1} + \frac{NF_4 - 1}{Gain_3 \cdot Gain_2 \cdot Gain_1} + \ldots$$

Use the linear terms for Noise Figure and Gain in the above equations, not the decibel form, ie.:

$$Gain_n = 10^{\frac{Gain_n(dB)}{10}}$$

$$NF_n = 10^{\frac{NF_n(dB)}{10}}$$

Some examples:

NF_1 [dB]	$Gain_1$ [dB]	NF_2 [dB]	$Gain_2$ [dB]	NF_3 [dB]	NF_{TOT} [dB]
3	10	5	10	5	3.49
3	10	5	5	5	3.58
3	10	5	10	10	3.62
3	10	5	5	10	3.97
3	5	5	10	5	4.39
3	5	5	5	5	4.62
3	10	10	10	5	4.65
3	5	5	10	10	4.72
3	10	10	5	5	4.72
3	10	10	10	10	4.75
3	10	10	5	10	5.02
3	5	5	5	10	5.54
3	5	10	10	5	6.91
3	5	10	5	5	7.04
3	5	10	10	10	7.10
3	5	10	5	10	7.59
5	10	10	5	5	6.16

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Optimization of Quadrature Modulator Performance

Introduction

Quadrature modulators are common building blocks in a communications link. By their nature they are capable of sending virtually any modulation scheme. They can send both analog, such as AM and FM, and digital modulation schemes, such as BPSK, QAM, and QPSK.

A common set of specifications for quadrature modulators is the carrier suppression and sideband suppression. The question often arises as to how they correlate with amplitude and phase error for the same device. This article presents a derivation showing the relationship between these four parameters.

Because the overall performance of the system can be affected by the modulator, its performance is important. Therefore, the need to optimize the carrier suppression and the sideband suppression of a quadrature modulator often arises. For those who may not be experienced with quadrature modulators, this can be a confusing task. This article will make this optimization easier to understand and perform.

Discussion

The first question that arises is why optimization is required at all. The primary reason is that there are imbalances in the Gilbert cell mixers and phase error introduced by the phase-shifting network. These imperfections are caused by slight differences in devices on the same die. There are also imbalances and offsets between the in-phase and quadrature signal paths as a result of process variations. These errors are not present in an ideal device, however they cannot be eliminated in practice.

The second question then would be how to compensate the device to optimize the performance. To understand how compensation can be achieved, it is helpful to understand how sideband suppression, carrier suppression, amplitude error and phase error are related.

The block diagram of a typical quadrature modulator is shown in Figure 1.

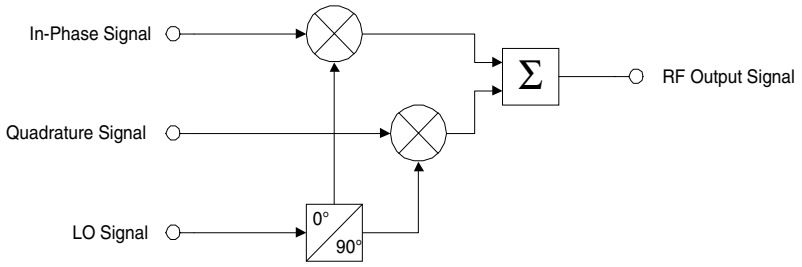


Figure 1. Quadrature Modulator Functional Block Diagram

The circuit multiplies the in-phase signal by the local oscillator and the quadrature signal by a 90° shifted version of the local oscillator. These signals are then summed to form the RF output signal.

Derivation

To begin the derivation, the input signals are defined as follows:

$$I(t) = G\cos(\omega t + \phi) + D$$

$$Q(t) = \cos(\omega t + 90°)$$

Note that this implies that the error injected into the system is due to the in-phase signal. The amplitude G represents the ratio of the amplitudes of the input signals. The phase offset, ϕ, represents the phase error. This is typically a small value representing how far from quadrature the signals are. The DC offset, D, represents the DC offset between the two signals. Ideally there is no offset, but in practice, there is an offset introduced by imbalances in the modulator circuitry. The quadrature signal is, by definition, 90° out of phase with the in-phase signal.

With the signals defined, it is a matter of performing the mathematical analysis that parallels the modulators' functionality. The RF output is given by

$$RF(t) = G\cos(\omega t + \phi)\cos(\omega_c t) + D\cos(\omega_c t) - \sin(\omega_c t)\cos(\omega t + 90°)$$

As can be seen, the carrier can only be present at the output if there is a DC offset between the input signals. Now, rearrange the terms to get the upper sideband and lower sideband terms using the trigonometric identities[1]

$$\sin(\alpha)\cos(\beta) = \frac{1}{2}\sin(\alpha - \beta) + \frac{1}{2}\sin(\alpha + \beta)$$

$$\cos(\alpha)\cos(\beta) = \frac{1}{2}\cos(\alpha - \beta) + \frac{1}{2}\cos(\alpha + \beta)$$

$$USB(t) = \frac{1}{2}G\cos(\omega_c t + \omega t + \phi) - \frac{1}{2}\sin(\omega_c t + \omega t + 90°)$$

$$LSB(t) = \frac{1}{2}G\cos(-\omega_c t + \omega t + \phi) - \frac{1}{2}\sin(\omega_c t - \omega t - 90°)$$

These can be rewritten to obtain

$$USB(t) = \frac{1}{2}G\cos(\omega_c t + \omega t + \phi) - \frac{1}{2}\cos(\omega_c t + \omega t)$$

$$LSB(t) = \frac{1}{2}G\cos(\omega t - \omega_c t + \phi) + \frac{1}{2}\cos(\omega_c t - \omega t)$$

Applying the trigonometric identity[1]

$$\cos(\alpha + \beta) = \cos(\alpha)\cos(\beta) - \sin(\alpha)\sin(\beta)$$

with

$$\alpha = \omega_c t + \omega t$$

$$\beta = \phi$$

the final form of the equations is reached

$$USB(t) = \frac{1}{2}G\cos(\omega_c t + \omega t)\cos(\phi) - \frac{1}{2}G\sin(\omega_c t + \omega t)\sin(\phi) - \frac{1}{2}\cos(\omega_c t + \omega t)$$

$$LSB(t) = \frac{1}{2}G\cos(\omega t - \omega_c t)\cos(\phi) - \frac{1}{2}G\sin(\omega t - \omega_c t)\sin(\phi) + \frac{1}{2}\cos(\omega_c t - \omega t)$$

We want these equations in this form is to allow them to be easily converted to envelope-phase form[2] since the sideband suppression is the ratio of the magnitude (envelope) of the upper sideband to the magnitude of the lower sideband. In general, a signal can be represented as the sum of the real and imaginary terms

$$x(t) = x_R(t)\cos(\omega t) - x_I(t)\sin(\omega t)$$

This expression can be rewritten in envelope-phase form as follows

$$x(t) = r(t)\cos[\omega t + \phi(t)]$$

where

$$r(t) = \sqrt{x_R{}^2(t) - x_I{}^2(t)}$$

$$\phi(t) = \operatorname{atan}\left[\frac{x_I(t)}{x_R(t)}\right]$$

The upper sideband and lower sideband envelopes are

$$USB_{env} = \sqrt{\left(\frac{1}{2}G\cos\phi - \frac{1}{2}\right)^2 + \left(-\frac{1}{2}G\sin\phi\right)^2}$$

$$LSB_{env} = \sqrt{\left(\frac{1}{2}G\cos\phi + \frac{1}{2}\right)^2 + \left(-\frac{1}{2}G\sin\phi\right)^2}$$

After expanding these terms we obtain

$$USB_{env} = \sqrt{\frac{1}{4}G^2 - \frac{1}{2}G\cos\phi + \frac{1}{4}}$$

$$LSB_{env} = \sqrt{\frac{1}{4}G^2 + \frac{1}{2}G\cos\phi + \frac{1}{4}}$$

The ratio for sideband suppression is then given by

$$\frac{USB_{env}}{LSB_{env}} = \sqrt{\frac{\frac{1}{4}G^2 - \frac{1}{2}G\cos\phi + \frac{1}{4}}{\frac{1}{4}G^2 + \frac{1}{2}G\cos\phi + \frac{1}{4}}} = \sqrt{\frac{G^2 - 2G\cos\phi + 1}{G^2 + 2G\cos\phi + 1}}$$

Therefore, the lower sideband suppression in dBc (decibels relative to the upper sideband) is given by

$$Suppression(dBc) = 20\log\sqrt{\frac{G^2 - 2G\cos\phi + 1}{G^2 + 2G\cos\phi + 1}} = 10\log\left[\frac{G^2 - 2G\cos\phi + 1}{G^2 + 2G\cos\phi + 1}\right]$$

This expression can be plotted as a set of suppression contours,[3] with amplitude error and phase error as the axes. To facilitate this, the equation was solved for phase error, ϕ, in terms of amplitude error, G, and sideband suppression, SBS.

$$\phi = \operatorname{acos}\left[\frac{1 - 10^{\frac{SBS}{10}} - G^2 10^{\frac{SBS}{10}} + G^2}{2G10^{\frac{SBS}{10}} + 2G}\right]$$

This equation was used in conjunction with the sideband suppression equation to generate data using a spreadsheet program. This data was plotted and the result is contained in Figure 2.

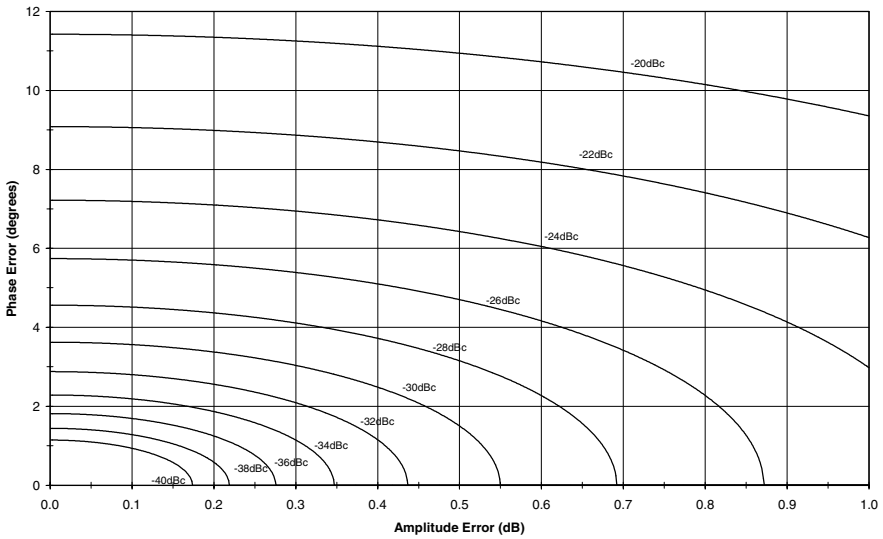


Figure 2. Sideband Suppression vs. Amplitude Error and Phase Error

Since it is often easiest to balance the amplitude error, it is convenient to plot phase error versus sideband suppression assuming the amplitude error has been balanced. Figure 3 is such a plot.

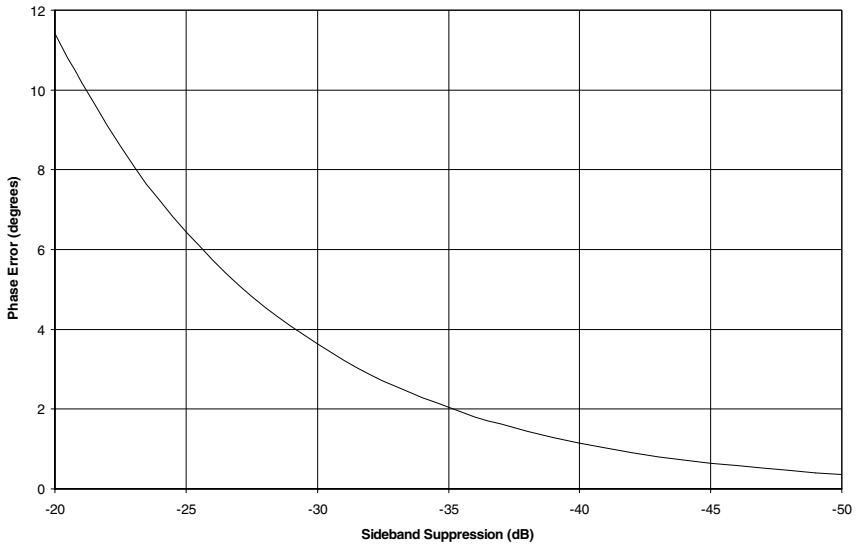


Figure 3. Sideband Suppression vs. Phase Error with no Amplitude Error

Optimization Example

The RF2422, an HBT 2.5GHz direct quadrature modulator, and its fully assembled evaluation board were chosen to demonstrate one way of optimizing performance. The board allows quick testing of the device, requiring two DC connections, a local oscillator input, two baseband inputs (In-Phase and Quadrature), and the RF output. All but the DC inputs are standard SMA style connectors. Refer to the schematic in Figure 4.

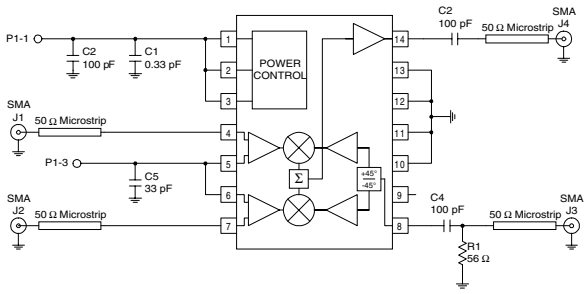


Figure 4. RF2422 Evaluation Board Schematic

Carrier suppression is a function of the DC offset between the in-phase signal and the quadrature signal in the device. This offset can be compensated by altering the DC offset of the input signals. Therefore, to improve the carrier suppres-

sion, start by adjusting the DC component of the in-phase signal (which should nominally be equal to V_{REF}), watching the output on the spectrum analyzer. As it is adjusted, there will be a point where the carrier level is minimized. Next, do the same with the DC component of the quadrature signal. Again, there will be a point where the carrier level is minimized. At this point, the carrier suppression has been optimized. The change to each DC level should be no more than about 20mV.

The carrier suppression can also be adjusted by adjusting V_{REF} This is a course adjustment since V_{REF} is connected to both I_{REF} and Q_{REF} and the degrees of freedom have been reduced. The above procedure could then be used to fine tune the adjustment. Either way, the same results should be obtained.

Sideband suppression is a function of both the amplitude error and the phase error of the device. These errors can be compensated by adjusting the input signals. Therefore, to optimize the sideband suppression, begin by adjusting the amplitude of the in-phase signal. There will be a point when the sideband level is at a minimum. Next, do the same for the quadrature signal. Again, there will be a point when the sideband level is minimized. To optimize further, adjust the phase of the quadrature signal. Again, there will be a point where the sideband level is minimized. At this point, the sideband suppression is optimized. The change in the amplitude should be no more than about 10mV and the change in phase should be no more than about 4°. Table 1 provides a list of the test equipment used.

Signal	Equipment
Local Oscillator	Rohde&Schwarz SMT-03 Signal Generator
V_{CC} and V_{REF}	Hewlett-Packard E3620A Dual Output Power Supply
I and Q Signals	Hewlett-Packard 8904A 4-Channel Multifunction Synthesizer
RF Output	Hewlett-Packard 8593E Spectrum Analyzer

Conclusions

This note has presented the derivation of the relationship that exists between the four primary specifications for a quadrature modulator: carrier suppression, sideband suppression, phase error, and amplitude error. Equations were presented that allow for translation between sideband suppression and phase and amplitude error. These equations were used to generate a plot that allows the designer of a system to quickly see how these specifications interact. It can be seen that good sideband suppression is the combination of both little phase error and little amplitude error.

It is often desirable to optimize the carrier suppression and the sideband suppression of quadrature modulators. This article presented a simple and straight-forward method of performing this optimization. This method is suitable for other similar devices and has been used to increase their performance.

An example of the outlined optimization method was used to improve the performance of an RF2422. For an RF2422 evaluation board, a carrier suppression of 44.1dB and a sideband suppression of 54.5dB were achieved. This is roughly a 15dB to 20dB improvement over an uncompensated board. Comparable improvements have been attained with other quadrature modulators.

References

1. M. Spiegel, Mathematical Handbook of Formulas and Tables, McGraw-Hill Book Company, 1968.
2. R. E. Ziemer, Introduction to Digital Communication, Macmillan Publishing Company, 1992.
3. W. Djen, Application Note AN1892, Philips Semiconductors, December 1994.

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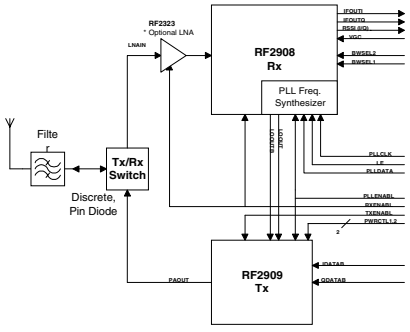
RF290X Digital Cordless Telephone Evaluation Kit

Product Description

The RF290X is an RF printed circuit board assembly (PCBA) intended to serve as a reference design for an RF module targeted for digital cordless telephone application. The RF290X PCBA includes the RF2908 Receiver/Synthesizer IC and the RF2909 Modulator/Transmitter IC that provide a two-chip monolithic radio solution of spread spectrum systems operating in the North American 902MHz to 928MHz ISM band under FCC Part 15.247. The chip-set is optimized for Time Division Duplex (TDD) applications. A block diagram of the radio is shown in Figure 1. The evaluation kit includes software and a cable for programming the PLL frequency synthesizer through the parallel port of a PC. RF shields for the PCBA are also included in the kit. Key features associated with the RF290X are as follows.

- RF290X Key Features
- 2-Chip Time-Division-Duplex (TDD) Transceiver Solution
- Compatible with Direct Sequence and Frequency Hop Spread Spectrum (DSSS/FHSS) Systems operating under FCC Part 15.247
- 2.7V to 3.6V Supply Voltage Range (2 Cell or 3 Cell Compatible)
- 50mW (@Antenna) Transmit Power
- Digital or Analog Tx Power Control
  - 3 Digitally Programmable Tx Levels (0dBm, 10dBm, 17dBm)
  - Analog Tx Level Control (1mW to 50mW)
  - QPSK/BPSK Linear Modulator
- Direct Conversion Receiver Architecture
- No Image Filter Required
- Quadrature RF Demodulator
- 1-Bit Stepped RF Gain Control for Adaptive IIP3
- 5-Pole On-chip Bessel Filter
- Dual (I&Q) Linear AGC or Limiting IF Output
- 86-Channel RF PLL Frequency Synthesizer
- On-Chip VCO (includes On-Chip Varactor)
- Serially Programmable
- Standard 3-Wire Interface

Figure 1: RF290X Evaluation PCB Block Diagram



Initial Configuration

The RF290X PCBA can be configured to support a variety of applications and includes both selectable settings that can be configured through an SMT switch (SW1), and I/O components that can be changed with a soldering iron. The configuration of the PCBA can be optimized by the user to best address a given system requirement. Prior to applying power to the PCBA, it is recommended that the user become familiar with the configuration options that are described in the following sections.

Receiver Configuration

The following receiver settings are selectable by the user through the SW1 SMT switch:

4. Receiver Enable (RXENABL)
5. Receiver Baseband Bandwidth (0.96MHz, 1.92MHz, 3.84MHz, 9.6MHz)
6. RF2908 Front End Gain (IP3 Select)

The receiver electronics can be enabled by sliding SW1-6 to the right (toward the number 6) or by applying a logic high to P5-1.

Receiver Filter Configuration

Filtering in the receiver is accomplished in three filters:

1. Coaxial Resonator RF Filter (F1)
2. Dual 3-Pole Lumped Element LC Filters
3. On-Chip Selectable 5-Pole Bessel Filters

The coaxial resonator filter is recommended for rejection of large signal, out-of-band interferors. Other RF filters (SAW, LC, etc.) can be applied successfully with the chip-set. The selection of the RF filter will depend largely on the cost/performance goals of the end product. The coaxial resonator filter that is included on the RF2908X PCBA has a nominal -3dB bandwidth of 902MHz to 928MHz and an insertion loss of 2dB.

The receiver baseband bandwidth is established by the combination of dual lumped element LC-filters and dual 5-pole Bessel filters that are selectable on the RF2908. The combination of the LC filters and the on-chip filters establish the adjacent channel rejection of the receiver. For optimum performance in DSSS applications, the baseband cut-off frequency should be set to 0.7 to 0.8 times the chipping rate. The lumped element LC filters are populated at the factory with component values that provide a 0.96MHz 3-pole Bessel filter. Other filter bandwidths are possible and can be designed using the graphs provided in Figures 2 (Bessel filter values), 3a and 3b (Butterworth filter values). The PCBA components L6-9, C32, C33, C42, and C43 component values can be adjusted in accordance with Figures 2, 3a and 3b to provide the desired filter response and bandwidth. The dual, on-chip 5-pole Bessel filter bandwidths are selected by SW3 (BWSEL2) and SW4 (BWSEL1). Table 1 provides the control interface for selection of these bandwidths.

Figure 2: Bessel Filter Component Values (L in uH; C in pF; Freq. in Hz)

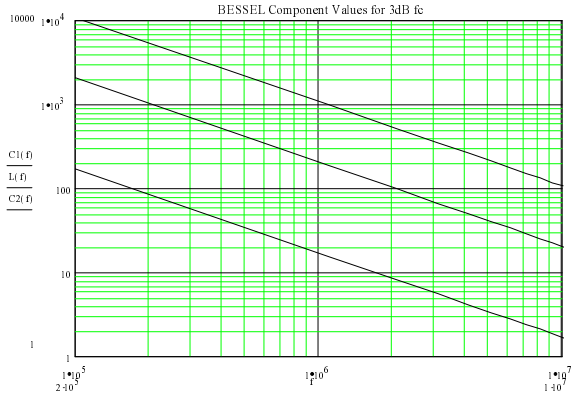


Figure 3a: Butterworth Filter Component Values (L in uH; C in pF; Freq. in Hz)

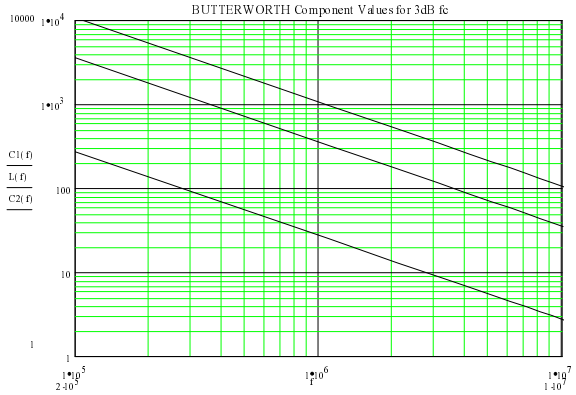


Figure 3b: External LC-Filter Circuit Architecture (For RF2908, Rs=125ohms-MOUTI/Q; R1=1kohm-INI/Q)

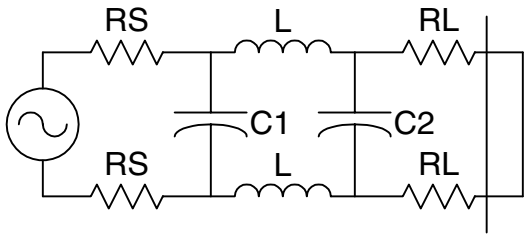


Table1: On-Chip BW Control Logic

BWSEL1	BWSEL2	IF-3dB Bandwidth
Low	Low	960kHz
Low	High	1.92MHz
High	Low	3.84MHz
High	High	9.6MHz

Receiver Front End Configuration

The RF290X includes the RF2323 silicon low noise amplifier. By including the RF2323, the receiver system noise figure is improved by 4dB (5dB versus 9dB) over an implementation without the RF2323. The decision to use the RF2323 will depend largely on the cost/performance objectives of the product.

The RF2908 includes a 16dB switched attenuator that can be used to dynamically reduce the RF gain and increase the input IP3 of the RF2908. An example application for this switched attenuator might be in a digital cordless telephone application where the attenuator would be switched on to mitigate receiver desensitization from out-of-band large signal interference when the handset is within 100 feet of the base. Outside of the 100 foot radius, the attenuator would be switched off to maximize the range of the phone. The switched attenuator is enabled by SW1-7 on the PCBA.

Receiver IF Output Configuration

The following settings are hardwired on the PCB, but can be changed by moving or removing a component on the PCBA.

1. The I and Q channel IF linear outputs are connected as IF outputs (SMA connections J2 and J3). This configuration is intended for system applications that require a linear IF and utilize AGC. If the dual data comparators are not used, $V_{CC}3$ (Pin 20) should be disconnected (left open) to minimize noise degradation in the IF from the comparators.
2. For system applications that utilize IF limiting, and require a logic level baseband output, the dual data comparators can be used as 1-Bit A/D converters. The data comparators can be connected to the IF outputs by removing R12 and R10 and installing 0ohm resistors for R11 and R13.

Transmitter Configuration

The following transmitter settings are selectable by the user through the SW1 SMT switch.

1. Transmitter Enable (TXENABL)
2. Digital Tx Output Level (1mW, 10mW, 50mW P_{OUT})
3. Linear Tx Output Level Control (APC)

The transmitter electronics can be enabled by sliding SW1-5 to the right (toward the number 5) or by applying a logic high input voltage to P5-3.

Digital/Analog Transmit Output Power

The nominal peak output power from the part can be controlled digitally using the PWRCTRL1 (SW1-2) and PWRCTRL2 (SW1-1), or by using an analog input voltage at P1-3 (APC) for a continuously variable output level. In either case, the DC current consumption of the part will be optimized for selected output power.

Operating Mode	PWRCTRL1 (SW1-2)	PWRCTRL2 (SW1-1)	APC (P1-3)
Digital Low Power (1mW)	Low	Low	Low
Digital Med. Power (10mW)	High	Low	Low
Digital High Power (50mW)	Low	High	Low

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Analog Power (1mW to 80mW)	Low	Low	0.5-V_{CC} (Max. APC input is 3.6V)

Best DC-RF efficiency at maximum output power is obtained when operating the RF2909 using APC control. For maximum output power, an APC input voltage of 2.8V provides the same RF output power as the Digital High Power state. With APC=2.8V, DC current consumption is approximately 40mA lower than the Digital High Power state.

The output power obtained will vary linearly with the modulation input voltage level applied to IDATAB (J4) and QDATAB (J5). Maximum output power (at a given level setting) will be achieved for an IDATAB and QDATAB input voltage level of 500mVp.

QPSK/BPSK Modulator

The RF2909 QPSK linear modulator is equally adept at BPSK and other PSK modulation techniques. To use the device as a BPSK modulator, the IDATAB (J4) and QDATAB (J5) should be wired (shorted) together. Data can then be input to the composite pin (J4/J5) to BPSK modulate the carrier.

Initial Power-Up of the RF290X Evaluation PCBA

The RF290X is designed to operate from a 3.3VDC+/-0.3VDC supply voltage. Three independent supply voltage connections must be made for proper operation of the PCBA. Although not required, it is a good practice to initialize these voltages simultaneously from a common power supply. It is also recommended that these voltage connections be made to the PCBA using twisted pair wiring.

V_{CC} Name	PCB Connection	Supply Voltage	Function
VBATT	P1-1	3.3V+/-0.3V	Supply voltage for the transmitter
PLLVCC	P5-1	3.3V+/-0.3V	Supply voltage for the PLL Frequency synthesizer and VCO
IFVCC	P4-1	3.3V+/-0.3V	Supply voltage for the receiver

The expected DC current consumption levels in the various operating modes are as shown in the table below.

RF290X Specifications

RF290X Cordless Telephone RF Module				
		Specification		
Parameter	**Min**	**Typical**	**Max**	**Units**
General Characteristics				
RF Frequency Range		902 to 928		MHz
Baseband Frequency Range		DC - 9.6		MHz
- Externally Programmable				
Receiver RF Characteristics				
Operating RF Frequency Band		902 to 928		MHz
Tangential Sensitivity (with RF2323)		-105		dBm
- IFBW=0.96MHz				
Tangential Sensitivity (without RF2323)		-101		dBm

- IFBW=0.96MHz				
Noise Figure (with RF2323)		5		dB
Noise Figure (without RF2323)		9		dB
Input Third-Order Intercept Point				
- Minimum Gain (without RF2323)		-10		dBm
- Maximum Gain (without RF2323)		7.5		dBm
LO Leakage @ RFIN		-67		dBm
I/Q Phase Imbalance		+/-2		Deg
Baseband Lowpass Filter Cut-off		0.96		MHz
Baseband Highpass Filter Cut-off		0.1		MHz
Baseband Bandwidth Range		0.96 to 9.6		MHz
Transmitter RF Characteristics				
Output Power				
- Digital Low Power Mode		0.7		dBm
- Digital Med. Power Mode		9.5		dBm
- Digital High Power Mode		17.5		dBm
- Analog High Power Mode (V_{APC}=2.8V)		17.25		dBm
Harmonic Output			-25	dBm
Modulator LO Suppression (High Power)		-20		dBc
PLL Frequency Synthesizer				
RF Channels (902 to 928MHz)		85		
Step Size		300		kHz
VCO Tuning Range		120		MHz
Phase Noise				
@10kHz Offset/PLL BW=5kHz		-66		dBc
@100kHz Offset/PLL BW=5kHz		-96		dBc
Reference Frequency		9.6		MHz
Settling Time		1.5		msec
DC Power				
Supply Voltage Range (V_{CC})	3	3.3	3.6	V
I_{CC} - Receive (without RF2323)		55		mA
I_{CC} - Receive (with RF2323)		62		mA
I_{CC} - Transmit Digital Low Power Mode		78		mA
I_{CC} - Transmit Digital Med. Power Mode		89		mA
I_{CC} - Transmit Digital High Power Mode		236		mA

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I_{CC} - Transmit Analog High Power Mode				
- V_{APC}=2.8V		196		mA
Supply Current (I_{CC}) - Sleep Mode		0.05		mA

Programming the PLL Frequency Synthesizer

The PLL Frequency synthesizer is programmed by connecting the parallel port of a PC to the 9-pin PCB connector with the cable provided. Prior to programming the PLL, PLLENABL should be connected logic high. This can be accomplished by sliding SW1-8 to the right (towards the 8) or by connecting P5-3 to V_{CC}.

The software used to program the PLL can be copied from the supplied diskette to the PC hard drive. The file RF2908.exe should then be executed from a DOS-shell. The program will prompt the user to enter the appropriate channel (swallow counter divisor). The table below provides a cross-reference for the specific data entry into the program to establish the desired operating frequency.

PLL Software Data Entry for Specific RF Operating Frequencies

Data	f,MHz	Data	f,MHz	Data	f,MHz	Data	f,MHz
0	902.4	22	909	44	915.6	66	922.2
1	902.7	23	909.3	45	915.9	67	922.5
2	903	24	909.6	46	916.2	68	922.8
3	903.3	25	909.9	47	916.5	69	923.1
4	903.6	26	910.2	48	916.8	70	923.4
5	903.9	27	910.5	49	917.1	71	923.7
6	904.2	28	910.8	50	917.4	72	924
7	904.5	29	911.1	51	917.7	73	924.3
8	904.8	30	911.4	52	918	74	924.6
9	905.1	31	911.7	53	918.3	75	924.9
10	905.4	32	912	54	918.6	76	925.2
11	905.7	33	912.3	55	918.9	77	925.5
12	906	34	912.6	56	919.2	78	925.8
13	906.3	35	912.9	57	919.5	79	926.1
14	906.6	36	913.2	58	919.8	80	926.4
15	906.9	37	913.5	59	920.1	81	926.7
16	907.2	38	913.8	60	920.4	82	927
17	907.5	39	914.1	61	920.7	83	927.3
18	907.8	40	914.4	62	921	84	927.6
19	908.1	41	914.7	63	921.3	85	927.9
20	908.4	42	915	64	921.6		
21	908.7	43	915.3	65	921.9		

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Advantages of HBT

Approximately four years ago, RF Micro Devices began an investigation of process technologies for use in wireless communications products. Our studies indicated that the best approach is to match the technology to the application thus providing the customer with the optimum price/performance solution. Our investigation revealed that Gallium Arsenide Heterojunction Bipolar Transistor technology is the optimum technology for many wireless components; in particular the power amplifier function. In general HBT components have the following characteristics which are essential to wireless communication components:

1. High linearity
2. Very wide frequency response F max higher than 50GHz
3. High voltage breakdown (greater than 20 volts)
4. High gain per stage resulting in high efficiency designs
5. Very low parasitics resulting in high Q capacitors and inductors
6. No negative power supply required
7. Low phase noise
8. Thermally rugged

From these advantages it appeared that HBT was the optimum technology for all wireless components. However there were some perceived disadvantages, namely:

1. Perception of low reliability
2. High cost
3. Poor manufacturing uniformity resulting in unreliable deliveries and additional costs

Fortunately for the wireless market, RF Micro Devices and TRW have been able to significantly reduce or eliminate the above mentioned disadvantages. TRW, through their use of Molecular Beam Epitaxy and their vast working knowledge of HBTs (in excess of eight years), has produced devices which are extremely reliable. These HBT devices have Mean Time Between Failures of 1100 years at an operating temperature of 125 degrees Celsius. Additionally, RF Micro Devices has performed numerous life tests on several different types of components produced using HBT.

Our life tests have indicated devices which are extremely rugged thermally. In addition, TRW has performed a space qualification on an HBT MMIC; therefore, the HBT process is now space qualified.

No matter how superior the technology, if its cost is prohibitive for the application (typically consumer products), a good match does not exist. RF Micro Devices has taken the lead in reducing the die size of various wireless components through proprietary techniques. By reducing the die area, the cost per component has been reduced to the point where HBTs are effectively competing with GaAs MESFET and high performance Silicon Bipolar devices. As an example,

RF Micro Devices offers HBT components which, in OEM quantities, sell below one dollar.

TRW has perfected a manufacturing process flow which has enabled uniformity of production. This uniformity of production is indicated by consistent betas from lot to lot and by extremely high wafer yields. HBT is the optimum process technology for many wireless applications because it meets the requirement of the best price and performance of any commercially available process.

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Growth of Personal Communication Services (PCS)

Cellular growth within the United States has experienced phenomenal expansion rates during the past ten years. As this growth occurred, service providers were constantly looking for future competitive threats from a new undefined source known as PCS. Five years ago the communication industry's vision for PCS was a simple system which utilized micro cells placed in high traffic areas such as hotels, airports, etc. This system would not allow the ability to roam or receive calls. The handsets would operate much as a portable cordless telephone with no air time charges and a fixed monthly rate. These handsets were simple technically and the increased capacity needed through higher air time usage could occur primarily through frequency reuse because the micro cells would only have enough power for relatively small areas such as a few city blocks or perhaps only a single building.

Enter 1995 and all old concepts have been discarded with the Federal Communications Commission's plan for a spectrum auction. Although the auction was delayed, eventually the process was started and the spectrum cost buyers billions of dollars. In addition to the spectrum cost, new communication technologies were adapted for PCS such as CDMA and GSM (DCS 1900) and performance enhancements were made from components using state-of-the-art Gallium Arsenide MESFET and Gallium Arsenide HBT's. These systems were designed and tested and these technical factors plus the cost of the spectrum are providing the fuel for explosive growth for the PCS market.

Instead of being competitive to current cellular systems, these new PCS handsets and PCS systems will be transparent to the end customer and provide communication which include all services that are currently provided plus greatly reduce the factors which currently limit cellular growth. These factors primarily include poor quality, lost calls due to hard hand-off between cells, poor voice quality, and most importantly the high cost of air time.

The new PCS system will provide high quality communications and many experts believe will eventually allow for the elimination of air time charges in the home roaming areas. These developments will place PCS in direct competition with wired telephones. When this occurs, the PCS market will experience growth with the potential to exceed any previous consumer electronic device. Without doubt, PCS will exceed the growth rates of portable consumer electronic devices of all types.

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HBT Technology Adds Power to CDMA Chip Set

These four chips provide all of the front-end functions that are needed for CDMA handsets.

Introduction

Efficient bandwidth utilization and low operating power characterize code-division-multiple-access (CDMA) transmissions, capturing the interest of several major telephone carriers in the technology. In support of future CDMA and dual-mode (analog/CDMA) handset designs, the engineers at RF Micro Devices (Greensboro, NC), in cooperation with CDMA-developer Qualcomm, Inc.(San Diego, CA) and device foundry TRW (Redondo Beach, CA), have created an RF chip set with the performance levels required by CDMA system designers.

The chip set is based on the low-power GaAs heterojunction-bipolar-transistor (HBT) device technology from TRW. The CDMA chips perform all the RF front-end functions in a handset (Fig. 1), including frequency translation, RF and intermediate-frequency (IF) amplification, and automatic gain control (AGC).

The chip set consists of the RF9906 low-noise amplifier (LNA)/mixer, the RF9908 upconverter integrated circuits (ICs), and the RF9907 and RF9909 AGC amplifier ICs. These ICs can be used in a handset design prior to second-stage frequency conversion.

The RF9906 integrates a low-noise preamplifier, double-balanced mixer, two switched variable-gain IF amplifiers, and a switched local-oscillator (LO) output buffer amplifier (Fig. 2). The IC is housed in a QSOP-24 surface-mount package and is designed to provide high dynamic range from a single +3.6 V_{DC} supply without additional external matching networks or bias circuitry.

The RF9906 is optimized for 850 to 900 MHz assuming 2.5 to 3.0 dB external image filter loss, although the wideband circuits provide similar performance from 500 to 1500 MHz. The 1 dB IF bandwidth is 110 MHz to either output port.

The overall gain of the RF9906 is 26 dB to the differential (IF1) port or 16 dB to the single-ended (IF2) port at the nominal gain setting. The gain can be tuned by (4.5 dB by adjusting a control voltage between 0.5 and 2.5 V. The IF output impedance is 1kΩ for IF1 and 750Ω for IF2 ports. The overall noise figure is 2.8 dB and the input third-order intercept point is -8 dBm at the nominal gain setting. The RF and LO input-port VSWRs are less than 1.50:1, while the LO output-port VSWR is less than 2.00:1. The LO-to-RF isolation is more than 50 dB in addition to image filter rejection.

The RF9906's LNA employs a combination of series and shunt feedback around a common-emitter amplifier to achieve excellent port impedance match without reactive elements. The gain is 16 dB, with more than 22 dB reverse isolation at 880 MHz (Fig. 3). The noise figure is less than 1.5 dB at frequencies below 1.2 GHz (Fig. 4). The input third-order intercept point is -3 dBm. The DC current drain is 7 mA.

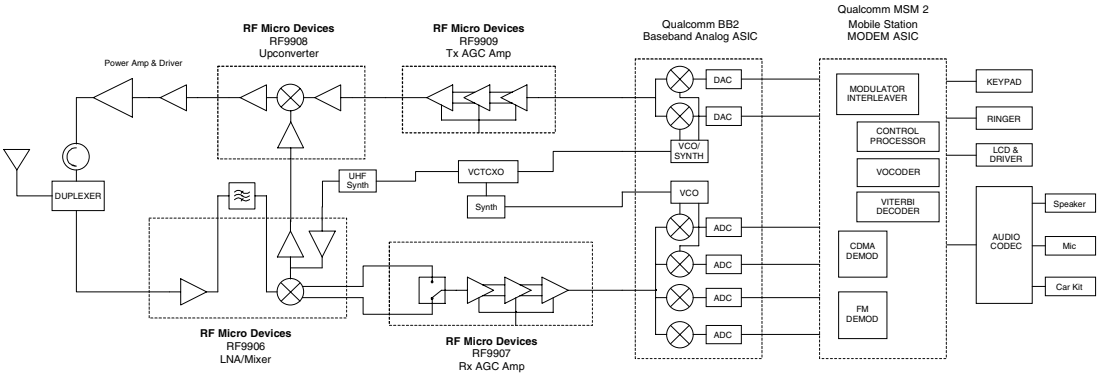


Figure 1: The CDMA chips provide the basic front-end functions required by a handset design.

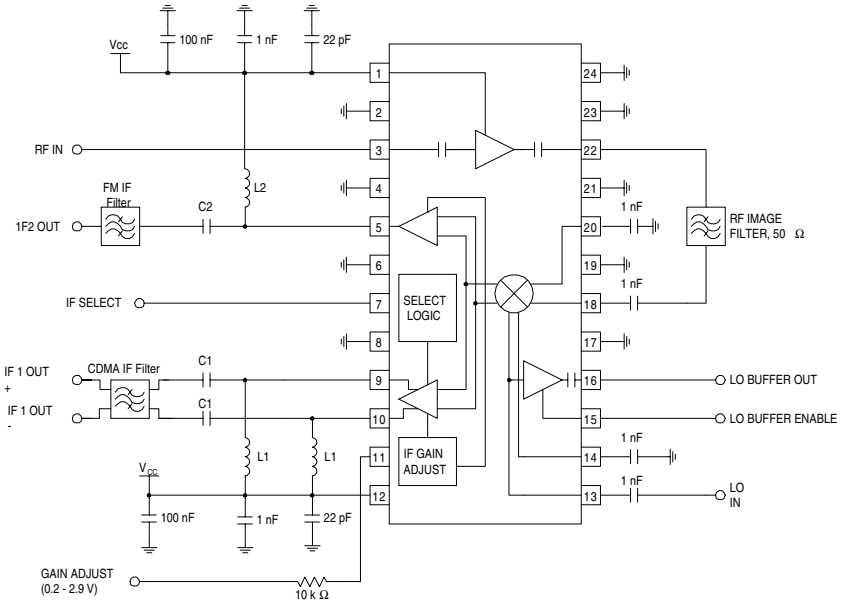


Figure 2: The RF9906 integrates an LNA, mixer, two switched variable-gain IF amplifiers, and a switched local-oscillator (LO) output buffer.

The RF9906's double-balanced mixer is a series-connected differential RF amplifier with a cross-coupled active LO switch (Gilbert cell). Series feedback sets the third-order intercept point. The mixer draws 9 mA and features measured double-sideband noise figure of 9 dB and an input third-order intercept point of +6 dBm. The 50 Ω device can achieve an input third-order intercept point of +10 dBm at +4.8 V_{DC} with no increase in noise figure. The mixer's gain is reduced by only 0.4 dB when the LO power is reduced to -9 dBm.

Two variable-gain IF amplifiers follow the mixer, selected by logic-level signals. The gain-control circuit uses a phase-cancellation technique. The mixer noise figure and input third-order intercept point are affected by less than 1 dB by the IF output selection at the nominal gain setting. The mixer's gain at the IF1 port is 13.5 ± 4.5 dB while gain at the IF2 port is 3.5 ± 4.5 dB. Current drains for the IF1 and IF2 selections, including bias and logic circuits, are 14 and 6 mA, respectively.

The switched LO output buffer provides 0-dB gain into a 50 Ω load over the LO input-power range of -6 to -3 dBm. The isolation to the LO port is 20 dB. The on/off output ratio is also 20 dB. The buffer, with an AC-coupled output port, is switched on with greater than 3.1 V on pin 15. DC current drain is dependent upon the LO drive, being 2.7 mA with -6-dBm LO power and 4.3 mA with 0 dBm LO power.

The RF9908 upconverter IC is housed in an eight-pin SOIC package. It contains a Gilbert-cell mixer with differential IF inputs and differential LO ports (for single-ended LO operation, one port is connected to an AC ground). The mixer is followed by a Class B push-pull output buffer amplifier. The IC operates at +3.6 VDC with 0 dB conversion gain and +13 dBm output third-order intercept point. The gain and intercept-point performances are not affected by changing the LO level.

The mixer is made of a differential pair amplifier and a four-quadrant multiplier. The lower differential part of the mixer pair is the IF amplifier, which has emitter-degeneration resistors to reduce the IF gain. By keeping the IF level small and well below the LO level, mixer linearity improves. The upper portion of the mixer incorporates switching transistors. Large LO signals (ideally square waves) are applied to the bases of the two cross-coupled transistors to alternately turn the

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paired transistors on and off with minimal distortion.

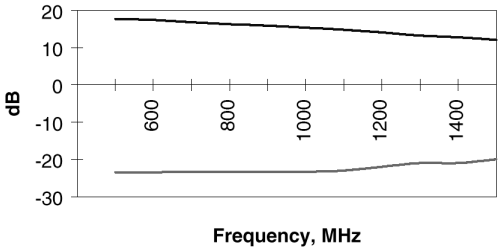


Figure 3. The LNA in the RF9906 provides gain of better than 12dB at 1.1 GHz, with more than 22 dB isolation at that same frequency.

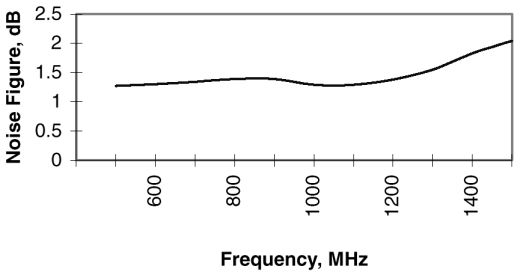


Figure 4. The LNA in the RF9906 has better than 1.5 dB noise figure to about 1200 MHz.

Because of the balanced nature of the mixer, the unit has excellent port-to-port isolation and low LO feedthrough at the output port. The spurious content within a 20 MHz bandwidth of the desired output range is typically better than -70 dBc and better than -50 dBc in a 60 MHz bandwidth. The LO leakage to the RF output port is -30 dBm, with at least 30 dB IF-to-RF-port isolation. In the output stage, the current for each transistor flows for approximately one-half of the input cycle, with each transistor providing a different half of the output waveform, resulting in considerable current conservation compared to Class A (always on) designs.

The RF9908 operates with LO drive levels of -6 to 0 dBm, with better than 1.50:1 VSWR and no external matching. The self-contained IC works to 2 GHz. The only external components needed are supply bypass capacitors and DC blocking capacitors on the IF and LO ports.

To complement the two frequency-translation ICs, the RF9909 and RF9907 AGC amplifiers provide gain-control functions for the CDMA transmitter and receiver sections, respectively. The AGC circuits are critical in maintaining consistent power levels with changing distances between handsets and base stations in a cellular network. Similar to the frequency converter ICs, the AGC ICs both operate from a single +3.6 VDC supply with low power consumption.

In a dual-mode system, the transmit AGC amplifier will typically handle a constant-level narrowband input signal. This AGC amplifier must provide linear amplification when needed or attenuation when signal levels are too high (close to the base station). To do this, the RF9909 offers an 84 dB gain range stretching from -45 to +39 dB. The gain control characteristic is monotonic and linear over the 84 dB range.

At the maximum gain setting of 39 dB, the output third-order intercept point is +16 dBm referenced to 1000 Ω. The noise figure is better than 20 dB for gain settings of 0 to 39 dB. The IC typically draws only 20 mA power-supply current from a single +3.6 VDC supply and handles signals from DC to 200 MHz.

The RF9907 receiver AGC amplifier must handle a wide range of input-signal levels, but must do so with consistently-low noise figure. The RF9907 features a 90 dB gain range (-45 to +45 dB), with analog gain control tuned by means of a DC voltage. The monotonic gain-control characteristic is extremely linear over the 90 dB gain range. Under maximum gain conditions, the RF9907's noise figure remains under 6 dB in either analog (FM) or digital (CDMA) modes. Under minimum gain conditions, the input third-order intercept point is better than -5 dBm (referenced to a 500 Ω load). The RF9907 typically draws only 13 mA from a single +3.6 VDC supply and features a 3 dB frequency range of 10 to 175 MHz.

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RFIC Components for Cordless Phones

Introduction

The commercial market for RF Integrated Circuits (RFICs) is expanding rapidly. Many commercial applications are appearing which need small, efficient components which provide higher levels of integration. Some examples include Point-of-Sale (POS) Terminals, cordless and cellular telephones, wireless meter reading equipment, wireless security systems, and many others. This increased integration level provides very low component counts on the PC board, and reduces the burden placed on the system manufacturer, ultimately allowing much lower system cost. This progression is analogous to that seen with digital circuits and micro-processors, whereby increasing levels of technology was placed upon the IC, and taken off the circuit board.

One application which requires high-volume, low-cost RFICs is the digital cordless telephone. Several 900 MHz phones have appeared on the market recently, requiring a low-cost RF section. Some of these RF sections are all discrete, others use a number of individual ICs, while still others use highly integrated ICs. Also, some of the entries utilize channel frequency hopping, others use direct-sequence spread-spectrum (DS-SS), and others use a combination of DS-SS and frequency hopping. A highly integrated RF chipset for a 915 MHz spread-spectrum cordless phone has been developed and will be described. The specific chipset as described here was developed under contract, and as such it is not generally available for sale. It does, however, demonstrate capability and the functionality presented here is available through RFMD standard components.

RF Chipset Requirements

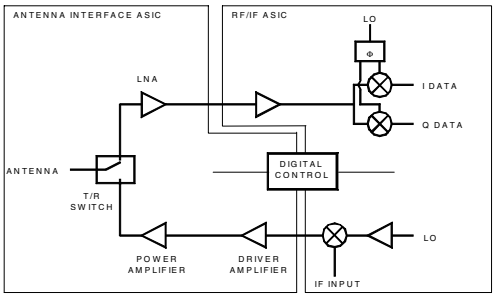


Figure 1. Block diagram of the RF section

The RF section such as that shown in Fig. 1 performs the following functions:

- Modulates the baseband spread-spectrum encoded data signals directly onto an RF carrier at 915 MHz,
- Amplifies the modulated signal with a power amplifier to 100 mW for transmission,
- Provides for switching between transmit and receive paths, using a T/R switch with digital control,
- Receives the incoming signal and amplifies with a low-noise amplifier,
- Demodulates the signal directly to baseband In-phase and Quadrature-phase components.

The chipset consists of two chips; an Antenna Interface ASIC and a RF/IF ASIC, as shown in Fig. 2 and 3. RF Micro Devices, Inc. utilized **Optimum Technology Matching**™, choosing high-performance GaAs MESFET technology for the Antenna Interface ASIC, and low-cost Silicon bipolar technology for the RF/IF ASIC. This partitioning of technologies allows the optimum price/ performance trade-off.

Antenna Interface ASIC

The Antenna Interface ASIC is a GaAs MESFET circuit, including a T/R switch, high-gain power amplifier, and a low-noise amplifier. The chip, supplied in a plastic SOIC-16 package, operates from a single 5V power supply. The overall specifications for the circuit require gain of 23 dB in transmit mode with 100 mW transmitted power, and 13 dB gain with less than 3 dB noise figure in receive mode. The T/R switch is controlled by digital translators, so a standard CMOS or TTL level input can be applied to control transmit or receive. Power down features are incorporated on all circuits and are tied to the T/R control.

The power amplifier is a self-biased, 3-stage GaAs MESFET design, with a total gate width on the final stage of 1.2mm. The final stage is biased slightly Class-AB, and consists of depletion-mode FETs with pinch-off voltage of ~-0.9V. Total current consumption in transmit mode is ~60 mA. Enhancement-mode FETs are used for part of the driver amplifiers as well as in the power down circuitry. The EFETs allow the amplifier to be shut off completely when not in use, using only the positive voltages available from the translators. The entire amplifier operates from a single 5V

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supply, with no need for an external negative voltage.

The LNA is a 12 dB gain block with ~2 dB noise figure. The input and output are matched to 50Ω; the output interfaces directly to the RF IN port on the RF/IF ASIC.

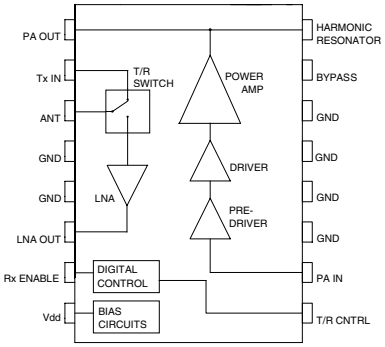


Figure 2. Antenna Interface ASIC.

RF/IF ASIC

The RF/IF ASIC is a Silicon bipolar circuit, and includes a bi-phase modulator for transmit, and a quadrature demodulator for receive. The LO input power is -10 dBm, which is amplified by the LO buffers to 0 dBm, and is distributed to both the up- and down-converter. Direct bi-phase modulation and direct quadrature demodulation is used, so a single external synthesizer is all that is required for the transceiver function. The 90° phase shifter for the quadrature demodulator is included on-chip to simplify the interface requirements.

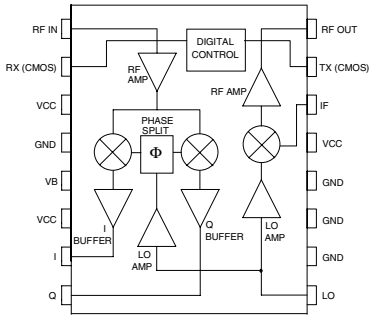


Figure 3. RF/IF ASIC.

The bi-phase modulator accepts inputs from 0 to >3 MHz with up to $0.5V_{p-p}$. Carrier suppression is >25 dBc for the maximum input level. Maximum output from the chip is -10 to -15 dBm. This provides an easily achievable level from the bipolar process, placing the majority of the gain and power output onto the GaAs circuit, where gain/stage and power are much higher.

The quadrature demodulator operates directly at 915 MHz. Input signals can range from 900-930 MHz, and the I/Q output bandwidth is 0 to 3 MHz minimum. Amplitude and phase balance specs are <1 dB and ±5°, respectively. I/Q output level can be as high as $1.4V_{p-p}$ at 1dB gain compression.

This chip also operates from a single 5V power supply and is supplied in an SOIC-16 package.

Summary

A highly integrated 2 chip set has been designed for cordless phones operating in the 915 MHz ISM-band using direct-sequence spread-spectrum modulation. This chipset allows the phone to be produced with much lower manufacturing costs and greater reliability than do the discrete components.

This paper was originally presented during the 1994 Wireless Symposium, Santa Clara, California.

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Wireless Antenna Interface

The demand for consumer wireless products poses design challenges with respect to cost, performance, packaging and semiconductor technology. The author provides practical guidelines, illustrating them with an antenna interface integrated circuit.

The growing market for wireless communication products has spawned a large demand for carrier-frequency integrated RX/TX circuit functions. Many of the communications products using these RFICs require low power consumption, small size and single-polarity power supply operation. In addition, some applications require low intermodulation distortion. All applications require low cost.

With the appropriate selection of semiconductor device and package technologies, it is now practical to meet these design and cost goals by using integrated circuits. In this article a radio frequency integrated circuit (RFIC) is described which combines the power amplifier, LNA and T/R switch functions for a cordless telephone application. It is an antenna interface ASIC (for application specific integrated circuit).

This antenna interface ASIC was developed using a conventional GaAs MESFET technology which had been developed specifically for commercial RFIC applications. This application requires lower power and less linearity than typical cellular applications, thus FET technology is practical for single-polarity supply operation. Plastic surface-mount packaging technology is used for lowest production cost.

Design Trade-offs

Developing RFIC chipsets for the growing wireless communications market involves more cost aggressive engineering trade-offs than have customarily been encountered for other MMIC applications. These include:

1. Package type and pin count: For low cost productions at frequencies below 3 GHz, narrowbody SOIC (small outline integrated circuit) packaging is the preferred style. The PLCC (Plastic Leadless Chip Carrier) is much less desirable due to the package thickness dimension, which is 3 times that of an SOIC. The largest available pin count for narrowbody SOIC is 16, and this includes pins allocated for low inductance RF grounding. Higher pin count widebody SOIC packages are available, but for economically-sized dice, say 50 mils square, the wirebond lead lengths required to wire the die in the larger package result in excessive parasitics, especially lead inductances. For IFIC products, which need only handle frequencies of 100 MHz or less, the widebody SOIC packages are practical.

PLCC packages have similar die-size versus package size trade-offs to be considered. In addition, PLCC packaging costs are generally higher than for SOIC packages. SSOP packages, which use 25 mil lead pitch, rather than the 50 mil pitch used by SOIC and PLCC, are being used with more frequency. The finer lead pitch allows a smaller footprint for a given pin count, and the body is vertically thinner than the 50 mil package styles. However, leadframe parasitics are higher and thermal conductivity is lower with the SSOP package than with the 50 mil pitch packages.

Depending upon the number of input/output (I/O) ports required in the RF function, along with the number of RF ground pins required for acceptable circuit performance, there may not be many pins left for off-chip connections. At some point, MCM (Multi-Chip Module) techniques may enable some passive circuit elements to be included within the same package as the active die, but this is not generally cost-effective now.

Some specific circuit functions, such as power amplifiers, require extremely low inductance ground connections and thermal conduction paths which may not be practical to achieve using plastic packaging. Such functions require considerably more attention in the area of package design than do lower signal level circuit functions, but the cost constraints are still present.

Examples of low-cost customized packages for power amplifiers include fused leadframe SOICs, embedded heat spreaders, and single-layer ceramic chip carriers. Fused leadframes are usually effective up to the point at which the magnitude of the inductive voltage developed across the RF ground path becomes comparable to the input signal magnitude. For a 900 MHz power amplifier with a Class AB output stage, the fused leadframe is practical up to approximately one watt of output power. A plastic package using an embedded heat spreader, which also serves as an extremely low inductance ground path, is an effective solution for higher power and higher frequency applications. Single-layer ceramic packages with ground vias to the backside are another cost-effective packaging solution for higher

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power or higher frequency products. Both alumina and aluminum nitride chip carrier technologies are becoming more affordable. The general rule to be observed in developing custom packages for wireless applications is: "The more the package physically resembles an existing SMD (Surface Mount Device) package, the more likely it is to be a commercial success."

2. Semiconductor technology used: Passive elements with acceptable performance may be fabricated on GaAs substrates, but require substantial amounts of die area. For example, a 600 micron gate MESFET uses approximately 18,000 square microns of die area. A 20 pf MIM capacitor, which is the size required for low-VSWR DC blocking at the 50 ohm level at 900 MHz, uses 69,000 square microns. Depending upon the circuit topology, several such DC blocks may be necessary. It is easy to see how die size can grow rapidly with the number of passive elements. At 900 MHz, it is usually a good trade-off to put DC blocks and RF bypasses off-chip, whenever possible.

With high performance silicon processes, passive elements are also practical in the 800 MHz to 3 GHz range. The high-performance silicon processes tend to approach that of GaAs in cost, however, so the same caution about area applies. On the other hand, with moderate-performance, lower-cost silicon processes, the substrate parasitics associated with passive elements can be substantial. In this case, circuit performance, rather than die cost, influences how many monolithic passive elements are included within the die.

3. Cost versus performance trade-off for passive elements: This particular trade-off must be made throughout an RFIC design cycle, whenever a passive element is used in the circuit topology. As noted, there is a significant cost penalty incurred, in the form of die area required, whenever a monolithic passive element is used in a design. This cost penalty must be weighed against the circuit performance degradation penalty which will occur if the passive element is placed off-chip. In the 900 MHz band and below, this trade-off usually favors off-chip passives. Above 3 GHz, full monolithic solutions usually are favored. The 1.9 GHz PCS and 2.5 GHz ISM bands are in an intermediate gray area from a design trade-off standpoint.

4. How many power supply voltages?: The answer is usually "one," and this complicates some circuit designs, particularly power amplifiers, if GaAs MESFET is the desired technology. With some performance trade-offs, single voltage supply circuits are realizable. The value of the supply voltage is also an important consideration in the selection of the design approach used. It not only influences the semiconductor technology choice, but the circuit topology choices, as well.

5. Powerdown or standby operation: Portable wireless applications, and some fixed applications, require a powerdown feature whereby the entire circuit function, or parts of it, have the DC bias turned off to conserve the battery charge when the circuit is not in use. Powerdown is usually straightforward to implement with most circuit functions. With power amplifiers, particularly if GaAs MESFET technology is used with a single power supply, the powerdown function presents some particular design challenges. This factor may influence the choice of semiconductor technology used in the RFIC design.

6. What circuit functions are to be included?: Depending upon how the overall circuit requirements are partitioned, certain semiconductor technologies are favored. Beyond the obvious partitioning of frequency range, i.e., RF versus IF, some circuit functions may also dictate which technology is most appropriate for the application. For example, GaAs MESFET, or perhaps silicon MOSFET technology provides the most compact RF switch functions. If the circuit partitioning includes T/R or antenna diversity switches, then FET technology of some form is probably the most desirable choice.

7. Impedance matching techniques: As noted, monolithic passive elements may increase the die size significantly. If the impedance matching topologies commonly used with hybrid or discrete circuits are applied to a monolithic circuit, the die cost may escalate unacceptably. Significant die area conservation may be achieved by using passive feedback or active circuitry to implement the impedance matching. Lossy RC feedback methods may be practical for many wireless applications which may tolerate the resulting degradation in output power and noise figure. Cordless telephones, wireless LANs and wireless security systems are examples of applications for which RC feedback circuits may be applied for impedance matching.

8. The tolerance for parts count: Assuming he could procure the parts at a reasonable price, most radio manufacturers would prefer a one-chip solution, to be used with a minimum number of off-chip components, perhaps one or two RF bypass capacitors on the power supply line. This may not be practical at an acceptable cost, and a cooperative design effort is most appropriate between supplier and user.

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Antenna Interface Design

RF Micro Devices recently undertook the development of a custom RF chipset for a cordless telephone, to be operated in the 902-928 MHz ISM band, using digital modulation. Single power supply operation and a powerdown feature were ancillary requirements. Since the final product is intended for a low cost consumer application, total product cost was of paramount importance. A moderate-performance silicon bipolar technology for the RX downconverter and TX upconverter functions, and a GaAs MESFET technology for the antenna interface ASIC were considered to be optimum. The antenna interface ASIC, which is the subject of this paper, consists of a low noise amplifier (LNA), a 100 mW power amplifier (PA), and a transmit/receive (T/R) switch. Narrowbody SOIC-16 packaging was selected for use in both RFIC products.

A block diagram of the antenna interface ASIC is shown in Fig.1. The LNA develops 24 dB of gain in two stages and the three-stage power amplifier has a large-signal gain of 32 dB. The supply voltage used is +5.0 volts.

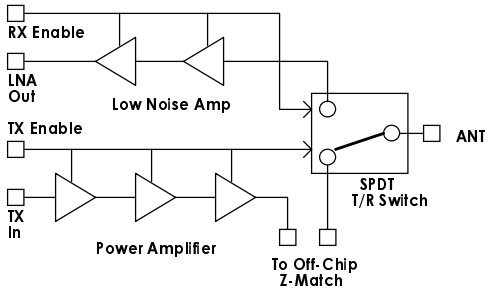


Figure 1. Antenna Interface ASIC Block Diagram.

In selecting a GaAs MESFET vendor for the antenna interface ASIC, several of the customer's requirements had to be taken into consideration. Since the RFIC design required powerdown capability from a single positive supply voltage, the process to be used needed an enhancement-mode FET (EFET) device. In addition, a low-cost process was required. The process selected uses planar MESFET structures with a 0.6 micron gate length and two-level front metal. Multiple depletion-mode (DFET) MESFET implants and one EFET implant are available. Also important, the process does not use either air bridges or via holes, resulting in better yield, and accordingly, lower cost.

The same basic circuit topology is used in both LNA stages and in the predriver and driver stages of the PA. As shown in Fig. 2, this gain block consists of a common-source EFET with resistive feedback and a DFET source-follower on the output. The EFET derives its gate bias from the feedback network, so in order to achieve powerdown, another EFET is used as a DC switch in series with the V_{DD} line for the gain block. The feedback provides the input impedance match to the gain block, and the source-follower matches the EFET drain to the load. The source-follower makes the gain block relatively insensitive to load impedance, so it is possible to use 7.5 pf interstage blocking capacitors, thereby saving considerable chip area over what a 20 pf DC block would require. The LNA output DC block and the PA input DC block are both off-chip, to save more die area.

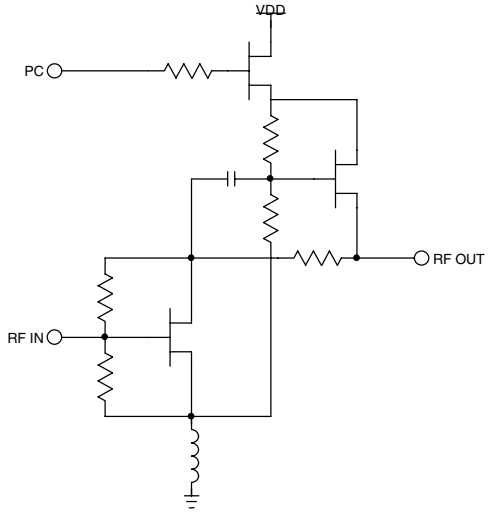


Figure 2. LNA/PA Driver Gain Block.

The PA final stage, shown in Fig. 3, consists of a common-source DFET using self-biasing. The powerdown feature is achieved using an EFET DC switch in the source circuit of the DFET. The EFET gate is connected to the TX-enable control line. The channel "on" resistance of the EFET is absorbed into the self-bias resistance network of the DFET. Because the current density capability of the EFET is lower than that of the DFET, the EFET switch uses over twice the gate width of the DFET in order to handle the current required in the final stage. The final stage also contains an RC feedback network to improve out-of-band stability. The output matching network is entirely off-chip in order to both save die area and minimize dissipative losses in the matching elements. The RF bypassing for the source self-bias resistor is off-chip.

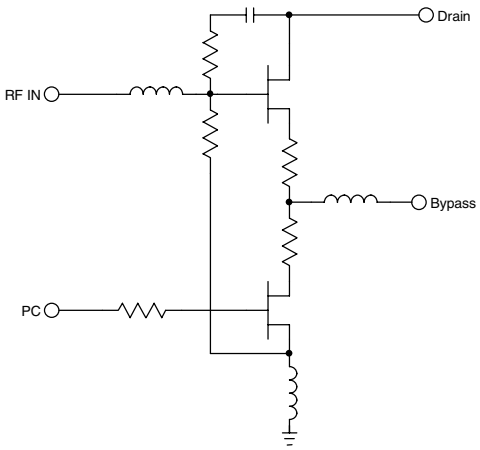


Figure 3. PA Final Stage

The T/R switch consists of a pair of series DFETs, one in the TX leg, and one in the RX leg. Because the isolation specifications for the T/R switch are not particularly stringent, shunt DFETs were not required in the circuit. This saved die area and eliminated the requirement for another set of low-inductance ground pins on the package. The switch FET gates are tied to the TX-enable and RX-enable control lines, respectively. The requirement for a negative bias source for the switch is eliminated by biasing the switch FET sources and drains at VDD potential. This does require the use of DC blocks on the RF lines, however. The TX and antenna (ANT) line DC blocks are off-chip, and the RX line DC block is a monolithic 20 pf metal film-insulator-metal film (MIM) capacitor.

The entire antenna interface ASIC design fits on a die which is approximately 60 mils square. Every pin on the package is allocated, either to RF signal, control signal, or DC/RF ground. Although it would have been desirable to have all the RF signal and ground nodes assigned to the shortest package pins, the die layout does not permit such an arrangement. All grounds are on short pins, but several RF signal lines had to use corner pins, which have higher parasitic values than the short pins. Wherever possible, the extra lead and wirebond inductances have been absorbed into the RF circuitry associated with that lead.

Measured Performance

Modeled and measured performance of the PA circuit is shown in Figs. 4-9. Fig. 4 shows the measured IRL and large-signal gain of the PA portion of the RFIC from 715 MHz to 1.115 GHz. The input power is -13 dBm, single tone, and the bias voltage is 5.0 volts. The modeled IRL is shown in Fig. 5 under the same operating conditions, and does agree reasonably well with the measured IRL data, except the slope is backwards. The discrepancy is probably due to parasitics on the test board which were not properly modeled initially. Fig. 6 shows the modeled output power for the PA. This agrees fairly well with the measured large-signal gain from Fig. 4.

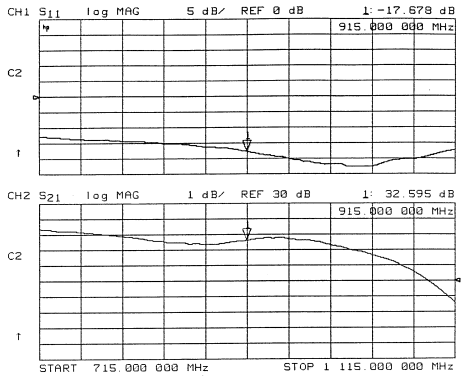


Figure 4. Measured IRL and Large Signal Gain.

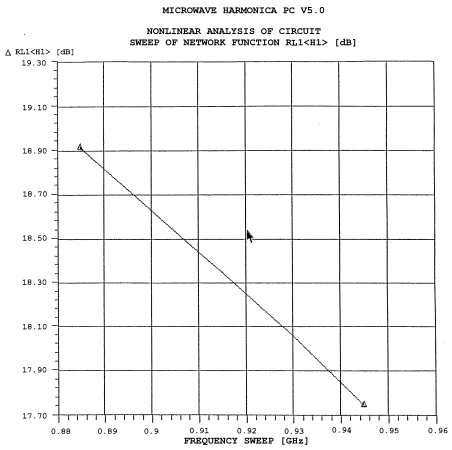


Figure 5. Simulated PA IRL.

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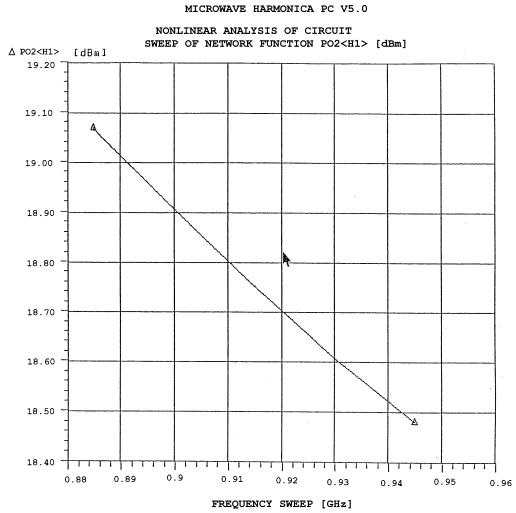


Figure 6. Simulated PA Output.

The modeled third-order intermodulation distortion is shown in Fig. 7. The two-tone input power for this simulation is -16 dBm. The resulting two-tone output power from this simulation is ±17 dBm, and the IMD is approximately -19 dBc. Fig. 8 shows the measured two-tone output spectrum resulting from a two-tone drive level of -19 dBm, and the resulting IMD is -20.6 dBc. A direct comparison of simulated-to-measured two-tone output power versus drive power is shown in Fig. 9, and simulated-to-measured IMD is shown in Fig. 10. The simulated performance, particularly in the case of IMD, becomes overly optimistic at high drive levels. This is most likely due to the inability of the TOM MESFET model to model the device behavior accurately under these conditions.

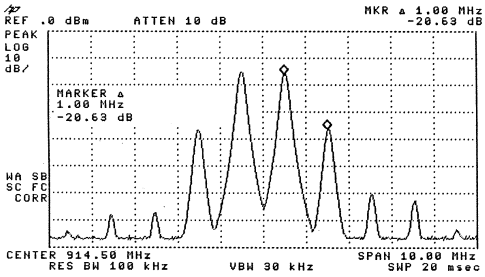


Figure 8. Measured IM_3, Pin=-19dBm Two Tone Avg.

The specification for the PA is -25 dBc IM3. This circuit falls short in this regard. The operating condition which results in acceptable IM3 performance, shown in Fig. 11, is a two-tone input power of -21 dBm.

The performance shortfall in the PA is caused by the driver stage having lower drain bias current than had been modeled. This situation was caused by the fact

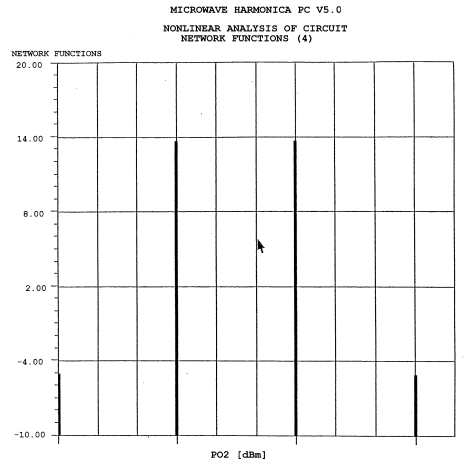


Figure 7. Simulated IM3, Pin=-16dBm Two Tone Avg.

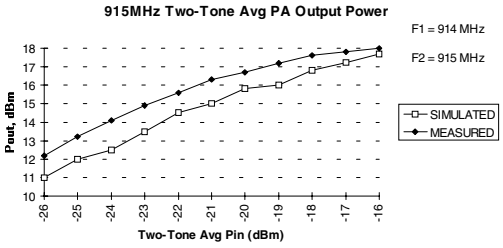


Figure 9. Simulated vs Measured Output Power.

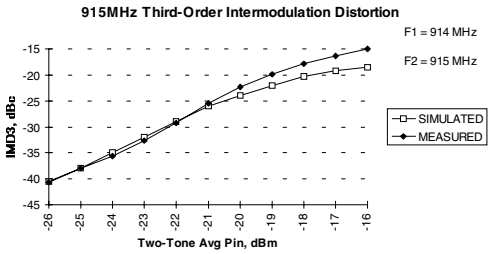


Figure 10. Two Tone Avg. Pin, dBm.

that some of the EFET model parameters used in the initial design were incorrect.

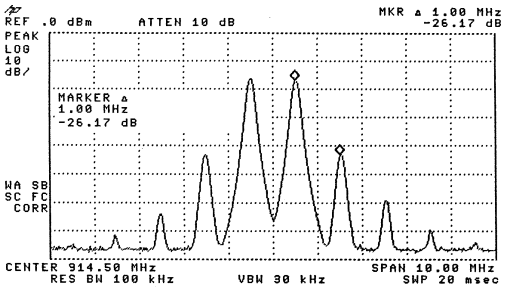


Figure 11. Measured IM3, Pin=-21 dBm Two Tone Avg.

Although the data is not shown here, the LNA has a NF of approximately 3.0 dB at the LNA input, and the T/R switch "on" loss is 0.8 dB. The T/R switch isolation, from the TX port to the RX port, with the switch set to the TX-ANT position and ANT terminated, is approximately 18 dB at +20 dBm input power at the TX port.

Acknowledgments

The author wishes to acknowledge the contributions of Clarence Oliver, who performed layout and assembly of the test circuit boards, and Jill Howard, who coordinated the prototype packaging effort and helped with the device performance measurements.

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A Direct Quadrature Modulator for 0.9GHz to 2.5GHz Wireless Systems

Introduction

As wireless system designs have moved from carrier frequencies at approximately 900 MHz to wider bandwidth applications like Personal Communication System (PCS) phones at 1.8 GHz and wireless local area networks at 2.4 GHz, designers have been forced to implement discrete RF designs because of the absence of RF integrated circuits (RFICs) at these higher frequencies. System designs at these higher frequencies have a great need for highly integrated RFICs for quadrature modulators, power amplifiers, and low noise amplifiers/mixers.

Foreseeing the wireless expansion to higher data rates and higher carrier frequencies, RF Micro Devices initiated a product development schedule for RFICs for use in these applications. The first of these high-frequency products is the RF2422 direct quadrature modulator. This low-cost, high performance quadrature modulator (see Figure 1) operates from carrier frequencies of 0.9 to 2.5 GHz and integrates a 90° carrier phase shift network, limiting amplifiers, two doubly-balanced mixers, a summing amplifier, and an output stage that drives 50 ohms. The unit features operation from a single 5 volt power supply, a built-in standby power supply switch, and is packaged in a 16-lead small outline integrated circuit (SOIC).

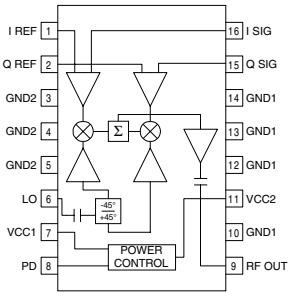


Figure 1. RF2422 Functional Block Diagram

The RF2422 is implemented using TRW's advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process. There are many features of this high performance process that make it ideal for the RF2422. First, the process features transistors with f_T of approximately 25 GHz. This high f_T allows the IC designer to use fewer devices and less current to attain gain at high frequencies. The process also provides thin-film resistors and high-Q metal-insulator-metal (MIM) capacitors. Thin film resistors possess excellent matching which is important in a quadrature modulator design where the I and Q circuitry must be identical. MIM capacitors allow the IC designer to implement DC blocking and filtering on chip instead of requiring the system designer to provide these externally. Another extremely important aspect of GaAs HBT is the semi-insulating substrate. The semi-insulating substrate results in negligible metal-to-substrate parasitics which means less high frequency crosstalk and leakage, and superior grounding.

Operation and Performance

The function of a quadrature modulator (also known as a vector or I/Q modulator) is to modulate a high-frequency carrier with lower frequency data. The beauty of a quadrature modulator is that it can be used to create all forms of analog and digital modulation. Amplitude, phase, and frequency modulation can all be implemented with a quadrature modulator. In order to evaluate the performance of a quadrature modulator, it is necessary to choose a specific modulation that is easy to generate and that allows the user to judge the important characteristics of the modulator. In general, RFIC manufacturers and users have settled on sinusoidal single sideband suppressed carrier (SSB or SSBSC) modulation.

SSB modulation allows the user to evaluate several important characteristics of a quadrature modulator: output power, carrier suppression, image suppression (phase and amplitude error), and harmonic distortion. To implement SSB modulation is a relatively simple task. The user connects a sinusoidal carrier to the local oscillator (LO) input of the modulator at the frequency of transmission. The I and Q ports are each driven with sinusoids of equal frequency and amplitude that are in phase quadrature with each other. The frequency used should reflect the data rate that will be used in the system. The output of the modulator is viewed with a spectrum analyzer centered at the carrier frequency. This method of evaluating modulator performance is inexpensive and fast for manufacturers and simple for end users to utilize.

A typical SSB output spectrum is shown in Figure 2. Proceeding from right to left, the frequency spikes represent the upper sideband, the carrier, the lower side-

band, and harmonic distortion. The upper sideband is, of course, the desired output and the other responses are all unwanted. The power level of the upper sideband, measured using a spectrum analyzer, is defined as the SSB output power. Raising and lowering the amplitudes of the I and Q signals will raise and lower the output power. The LO level should be kept constant and not used to change output power. Figure 3 shows a graph of I/Q amplitude versus output power with an LO level of -5 dBm at 2 Ghz.

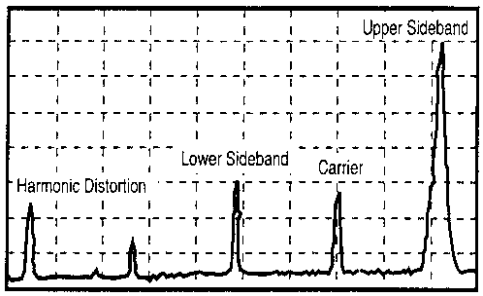


Figure 2. Typical SSB Output Spectrum.

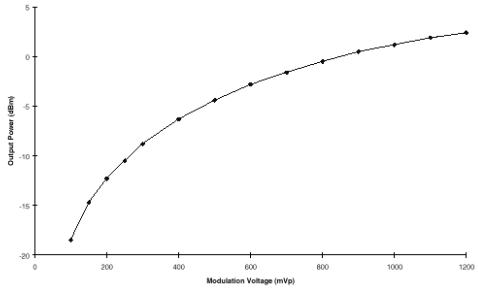


Figure 3. Modulation vs. Output Power (SSB); LO=2 GHz, -5 dBm.

The frequency spike immediately left of the upper sideband is the carrier. The difference in power between the upper sideband and the carrier (in dB) is the carrier suppression. Carrier suppression is determined by the DC voltage matching between the ISIG, IREF, QSIG, and QREF pins, and by the amount of LO leakage to the output. The DC voltages at the I and Q input pins control the DC currents in the I and Q mixers. In order for the carrier to be suppressed, these currents must be identical. If the user provides DC voltages at the four I and Q input pins that are identical, then the RF2422 exhibits excellent carrier suppression. This is due to the superior matching of thin-film resistors in TRW's process. As mentioned before, suppression is also affected by LO leakage through the package and PC board. The higher the carrier frequency, the worse this problem becomes. Even with leakage, carrier suppression can be optimized by adjusting DC voltages at the I and Q inputs relative to each other. Generally, adjustments of just a few millivolts will allow the user to null the carrier. It is important to note that carrier suppression is a relative measurement in that it is dependent on SSB output power. As I and Q modulation levels are decreased, the SSB output power will decrease, but the carrier will not, thus yielding less carrier suppression. It follows that users must be sure of what modulation levels are being used whenever reading a manufacturer's carrier suppression data. Figure 4 illustrates that carrier suppression in the RF2422 is typically below -30 dBc across the operating frequency range, without any adjustment. Note: The I and Q ports were each driven with 500 mV_{pk}.

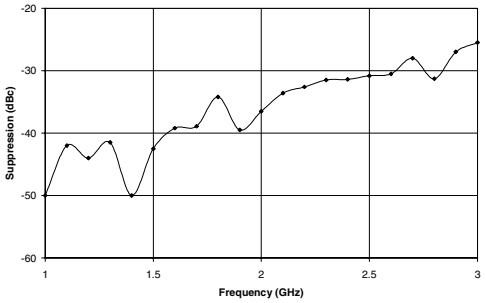


Figure 4. Carrier Suppression vs. Frequency.

The next frequency spike is the lower sideband. The difference in power between the upper sideband and the lower sideband (in dB) is the image suppression. Image suppression is an indicator of phase and amplitude error. The more the phase and amplitude error, the worse the image suppression. These errors are caused by such things as package parasitics, nonlinear transistor operation, and layout asymmetry. Although these problems are addressed in design, they can never be completely eradicated. Amplitude and phase errors are largely frequency dependent, but they can also depend in a lesser extent on LO power level and power supply voltage. It is very important to evaluate the modulator under system operating conditions. Image suppression can be adjusted externally by changing the phases and amplitudes of I and Q relative to each other. Phase error in the RF2422 is very minimal. As shown in Figure 5a, phase error is typically within a few degrees at any given frequency. Amplitude error (Figure 5b) is only a few tenths of a dB at the frequency extremes. These small phase and amplitude errors combine to yield image suppression numbers that typically range in the mid 30s, as shown in Figure

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5c.

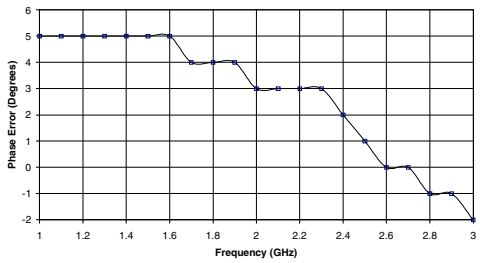


Figure 5a. Phase Error vs. Frequency.

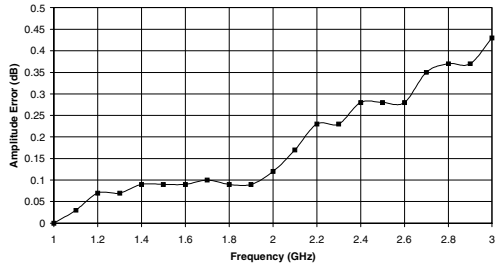


Figure 5b. Amplitude Error vs. Frequency.

The two frequency spikes furthest to the left are harmonic distortion. Although there are other spurious products that can be viewed if the spectrum is spanned at higher frequencies, these specific products are the closest to the carrier with the most power, and therefore the most difficult to filter. In addition, manufacturers usually only specify the suppression of the distortion spike furthest to the left since it is stronger than the one that is closer in. As the amplitudes of the I and Q signals are increased, the power of this harmonic will increase, much like an IM_3 product. Like the carrier and the lower sideband, system designers prefer harmonic distortion to be kept to a minimum to prevent saturation of the power amplifier or any components in the receiver.

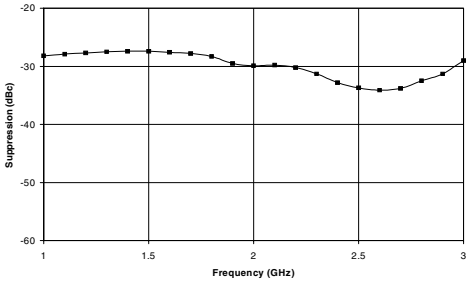


Figure 5c. Sideband Suppression vs. Frequency.

Description of Design

The LO connection to the RF2422 is a single-ended, 50 ohm termination so that no transformer or balun is needed. The port is DC blocked internally so that no external blocking capacitor is needed. Having entered the part, the LO signal immediately travels through an R-C network that acts as a phase splitter. The R-C network consists of a high-pass and a low-pass filter which each shift the LO signal 45 degrees, but in opposite directions. The result is that the LO signal is split into two signals of equal frequency but 90 degrees out of phase. The output of one filter will propagate to the I mixer while the output of the other filter will go to the Q mixer. The R-C network is designed around a 2 GHz center frequency so that when the LO signal is below 2 GHz, the high-pass filter attenuates the amplitude of its signal; likewise for the low-pass filter when the LO is above 2 GHz. In order to equalize the two filter outputs, limiters must be used after the R-C networks.

Each of the two limiter stages consists of a high-gain differential amplifier. The limiters' function is to amplify the two quadrature signals to the point where the waveforms are clipping. The clipping effectively equalizes the two signals since both limiters are designed identically and will clip at the same time. Obviously, if the LO signal is low enough in power or far enough in frequency from 2 GHz, the limiters will not be able to equalize the two signals, causing a transmission amplitude error. The recommended LO power level for the RF2422 is -5 dBm.

The quadrature LO signals proceed to the I and Q mixers where they are each coupled to the top four transistors in a Gilbert cell. Because the signals are high amplitude square waves, the top transistors act like high speed switches. The bottom differential pair of each of the mixers (Gilbert cells) act as the inputs for the lower frequency modulating signals. In the I mixer, these input pins are referred to as ISIG and I REF; in the Q mixer as QSIG and QREF. There is no DC blocking on any of these inputs; each input effectively looks into the base of a transistor. This translates to a very high impedance looking into each input (approximately 30 K ohms), and therefore these ports will draw very little DC current (40 (A) unless the part is operated in saturation mode. Saturation occurs when the voltage at these inputs approaches 4 V_{DC}. When the voltages at these pins approach 1.5 V_{DC}, the transistor current sources associated with each of the Gilbert cells begin to saturate, causing nonlinear operation. From this information it is clear that for linear operation the I and Q pins should be driven with signal levels between 1.5 to 4 V_{DC}. The recommended offset voltage is from 2.5

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to 3 V_{DC}. In order to boost the input compression point of the mixers, emitter degeneration is used in the bottom differential pair of each mixer.

The output currents of the two mixers are summed at the collectors across two load resistors. The summed outputs are then amplified by a differential amplifier which acts as a driver to the output stage. Emitter degeneration is once again used for maximum linearity.

The output stage is required to convert the differential output from the driver to a single-ended signal. In order to keep current consumption to a minimum, a push-pull configuration is used. The output impedance is designed to look like 50 ohms across the frequency operating range.

External Components

The RF2422 is extremely easy to insert into a wireless system. Only three external components are required to make the RF2422 fully operational. All three components are bypass capacitors. Two capacitors are needed to bypass the VCC1 and VCC2 pins and the third capacitor is used to bypass IREF and QREF if the baseboard-to-I/Q connections are single-ended (IREF and QREF would be tied together in this case). If IREF and QREF are being used in a differential connection, then no bypass capacitor would be needed for those pins. As with all RF board designs, bypass capacitors should be placed as close as possible to the part.

The LO port has a 50 ohm input impedance and is generally coupled to a synthesizer with 50 ohm microstrip. Although an input level of -5 dBm is suggested for the LO input, this number is not critical for operation. In fact, the part will continue to operate at levels less than -10 dBm, but with less conversion gain and degraded amplitude accuracy. Therefore, the match between the LO port and the synthesizer may or may not be important, depending on system requirements. The output impedance of the RF2422 is 50 ohms and is usually coupled to a power amplifier of driver with 50 ohm microstrip. There is an internal DC block so that no external series capacitor is needed. Generally the match between the output and the following amplifier is quite important, so as to achieve maximum power transfer. If the input impedance of the following power amplifier is a 50 ohm termination, then no extra matching components are needed between the two unless DC blocking is required for the amplifier.

The PD pin is used to power down the part when operation is not needed. For example, in time division duplex (TDD) systems where the transmitter and receiver are operated in alternating time slots, the RF2422 could be powered down when the receiver is in use to minimize current consumption and thus extend battery life on handheld units. The PD pin can be directly driven with a CMOS driver where +5 V_{DC} powers up the part and ground powers it down.

The modulation input pins of ISIG, IREF, QSIG, and QREF can be driven with any modulating waveforms. ISIG and IREF are differential inputs to the I mixer on the RF2422 as QSIG and QREF are differential inputs to the Q mixer. For carrier suppression, the DC voltages at all four pins must be equal.

Applications

Wireless local area networks using direct-sequence spread-spectrum modulation can successfully use the RF2422, as illustrated in the simplified system block diagram in the front of this catalog. In the transmitter, I and Q baseband data are first modulated by a pseudo-random bit code that is much higher in frequency than the I/Q data. Once this frequency spreading has taken place, the resulting signals are fed into the I and Q inputs of the RF2422. The RF2422 enables the spread signals to perform what is typically GMSK or QPSK modulation directly onto a 2.45 GHz carrier. This approach eliminates much of the filtering and LO requirements necessary for multiple upconversion schemes. Other applications include PCS and DCS1800 digital systems operating at 1.8 to 2 GHz, and satellite communications systems operating in L-band.

Conclusion

The RF2422 direct quadrature modulator fills an important gap in 2 GHz wireless systems. Direct modulation up to 2.5 GHz is now possible with a proven chip that can greatly simplify a wireless transmitter. The RF2422 packs numerous discrete functions into one small SOIC package so that system designers can reduce size, cost, and valuable engineering time.

This article was originally presented in **RF Design**; August 1994.

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LNA/Mixer ICs Ease Wireless Receiver Design

Integrated front-end components provide sensitivity and IMD control while operating under low-voltage/current conditions.

New digital communications systems integrate high-capacity wireless transceivers in packages as small as a PCMCIA card. Such transceivers rely on multifunction RF integrated circuits (ICs) to meet such rigid size requirements. Part 3 of this design series examines the role of RF ICs for high-performance wireless receiver front ends, particularly in hand-held systems.

Although the signal processing in many modern receivers occurs in the digital realm, analog circuits are still needed to amplify weak incoming signals from the antenna to a voltage which can be conveniently digitized. Direct conversion is the simplest receiver architecture. However, this approach places all filtering and detection processes at the signal frequency. Attractive from a cost and complexity standpoint, and adequate for less-demanding applications at lower frequencies, this technique does not provide adequate interference rejection in crowded bands. The method also fails to reject the noise close to the carrier characteristic of UHF and microwave oscillators used as receiver local oscillators (LOs).

Typically, communications receivers are constructed using a superheterodyne architecture (Fig. 1). The signal frequency is converted to a lower intermediate frequency (IF) in one or more steps for efficient amplification, filtering, and detection. Architectures using a single IF are often a good compromise when considering cost, size, and performance requirements.

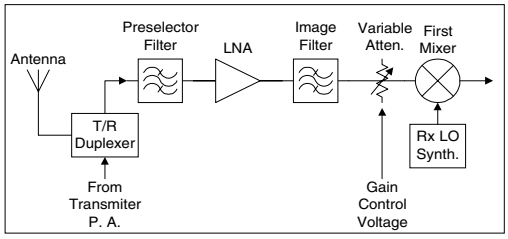


Figure 1: This Superheterodyne structure is typical among wireless communication receivers.

The receiver is isolated from the transmitter and connected to the antenna through a duplexer. The duplexer may consist of band-splitting filters when the transmitter and receiver are sufficiently separated in frequency, such as in 900MHz cellular telephone systems. Alternately, the transmit/receive (T/R) duplexer may be a single-pole, double-throw (SPDT) switch when transmit and receive signals overlap or are too close in frequency to effectively filter, as may be the case in the 902 to 928MHz band.

The typical superheterodyne receiver front-end circuitry consists of a band-limiting preselector filter (which may be part of the T/R duplexer), a low-noise amplifier (LNA), a mixer, and an LO. The gain ahead of the mixer may be controlled either by a variable-gain LNA or a voltage-controlled attenuator.

Successful receiver design optimizes the combination of sensitivity, interference rejection, overload protection, current consumption, size, and cost. In addition, battery-operated equipment must run at 3V or less. Therefore, a number of design issues must be considered.

First of all, the LO and IF bands must be selected. Two frequency bands at the LO±IF are converted to IF. The LO must be offset above or below the desired frequency by the IF. In addition to the desired frequency, an image frequency offset by twice the IF in the direction of the LO is also converted to the IF band.

A serious interference potential exists if the image response is not eliminated. Since the noise at the image frequency is also converted to the IF, the noise figure may be increased by 3dB. The image signal may be filtered at any place ahead of the mixer. Placing the image filter just ahead of the mixer can lower the loss ahead of the LNA, reducing the overall system noise figure.

An alternate image-rejection technique is based on phase-cancellation techniques similar to single-sideband (SSB) generation. However, the rejection potential of the phase-cancellation method is difficult to realize because this technique relies on exact phase and amplitude tracking of two signal paths over temperature and time. For this reason, filters achieve much higher rejection in practice. Phase cancellation remains an interesting potential approach since it is

more appropriate for monolithic implementation on an IC at low microwave frequencies than monolithic high-Q filters.

The general IF choice is driven by IF and RF filter technology. The IF is chosen to be high enough so that the RF filters can reject the image frequency, but not so high as to unnecessarily increase the cost of the IF circuitry. The IF bandwidth and group delay must be matched to the characteristics of the received signal. Common communications receiver IFs are in the 10- to-100MHz range. The exact IF is based on the frequency of potential interference sources and the LO synthesizer characteristics, among other considerations. Placement of the LO above or below the IF is based on the occupation of the resulting image bands and on LO synthesizer capabilities.

Receiver noise figure (NF) determines the receiver sensitivity in the absence of interference. The overall receiver NF will be the sum of duplexer loss, preselector loss, LNA NF, and mixer/IF amplifier noise according to:

$$F = F_{dup} + [(F_{pre} - 1)/G_{dup}] + [(F_{lna} - 1)/G_{dup}G_{pre}] + [(F_{mix} - 1)/G_{dup}G_{pre}G_{lna}] + \ldots \quad (1)$$

While man-made noise and interference at 1 GHz may be equal to kTB or less in suburban or rural environments, noise in urban environments may be as much as 17dB more than kTB and thus dominate the receiver system noise. In view of the other contributions to overall receiver noise level, LNA NF of 1.5 to 2.5 dB is adequate for most applications.

Potentially more important to receiver performance in the real-world operating environment is third-order intermodulation distortion (IMD). Odd-order IMD (of which third-order IMD is the largest) falls into the frequency band occupied by the desired signal and therefore cannot be eliminated by filtering techniques. Intermodulation products involving strong signals from nearby transmitters on adjacent and alternate channels can thereby mask a distant desired signal, even though the IF filter has adequate adjacent-channel rejection.

Intermodulation performance is usually specified in terms of the third-order intercept point (IP_3). This is the theoretical output power at which the extrapolated low-level third-order intermodulation products equal the two desired output signals. The value of IP_3 can be used to calculate the third-order intermodulation products given the level of two equal-amplitude signals according to:

$$IM_3 = 3P_{signal} - 2IP_3 \quad (2)$$

where:

P_{signal}= the power level of each test signal (in dB)

and

IP_3 = the third-order intercept point (in dB)

IP_3 can be referenced to the input or the output by simply translating the value according to the linear gain.

The receiver mixer is particularly vulnerable to IMD due to the higher signal levels following the LNA. The problem is often alleviated by reducing the signal level to the mixer under strong signal conditions by means of a variable-gain LNA or variable attenuator between the LNA and mixer. Usually, two switched-gain or attenuation states are sufficient to obtain good intermodulation performance. The bulk of receiver signal-level control ahead of the detection process is relegated to the IF amplifier.

Better LNA and mixer intermodulation performance usually comes at the price of higher current drain — the bane of battery-powered equipment. Thus, noise, intermodulation, and current drain cannot be simultaneously optimized. As a compromise, overall LNA/mixer gain is typically set at 20 to 25dB, just high enough to remove IF amplifier noise from the overall receiver NF. Gain is typically distributed between the LNA and mixer according to the intermodulation and noise capabilities of the two blocks. The intermodulation performance is then maximized at the current drain, which can be tolerated by the system.

The impedance between component interfaces must be controlled to achieve optimum performance. The LNA NF, for example, is directly affected by the source impedance. Filter characteristics will also be affected by the terminating impedances at the input and output ports.

A clever choice of interface impedance can minimize receiver front-end current drain. High load impedance requires less current from a monolithic output buffer to produce a given voltage. Although filters at UHF and microwave frequencies are designed for use at 50Ω, IF filters are available at terminating impedances as high as several thousand ohms.

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The only method of matching high-impedance on-chip circuitry to a low impedance filter monolithically at IF is with an active buffer, which may consume more than half the total LNA/mixer current. Alternately, low-impedance filters can be matched to a high-impedance output port using external reactive components. Also, higher-impedance IF filters can be used.

Voltage as well as current-swing limits must be considered when setting the IF impedance level. The maximum peak-to-peak output voltage swing (V_{output}) is about V_{output} - 1 for resistive IF loads. Reactive matching networks can be used with open-drain output circuits to produce as much as 2Voutput - 1 peak-to-peak output swing. The optimum IF impedance (for minimum current drain) is a function of power-supply voltage and output IP_3 requirements. In other words, the same design considerations used to maximize efficiency in a power amplifier apply to low-signal-level circuits in the receiver as well.

As an example, assume no external-matching components are allowed, but a 50Ω output drove capability is required from the output buffer. The output IP_3 (OIP_3) level is assumed to be 10dB more than the maximum linear output power. The maximum linear output power is calculated from the maximum output current-voltage (I-V) swing by:

$$P_{out}(max) \cong (V^+ - 1)^2/4R_L \quad (3)$$

and

$$OIP_3\ (dBm) \cong 40 +$$

$$10 \log_{10} (R_L \times I_Q^2/2) \quad (4)$$

where:

R_L = the load impedance, and

I_Q = the current consumption.

To produce a +12dBm OIP_3 level, the output buffer must consume 8mA. However, if the IF output load impedance can be raised to 500Ω, the buffer current needs to be 2.5mA for the same OIP_3 level. The voltage-swing limit in Eq. 3 restricts the 50Ω output power levels to +13 and +19dBm, respectively, at power supplies of +3 and +5V_{DC}.

As another example, consider a case where reactive components can be used to transform the impedance. For a given power-supply voltage and desired current drain, there will be an optimum load resistance for the maximum output power and OIP_3.

$$R_L \cong (V^+ - 1)/I_Q \quad (5)$$

and

$$OIP_3\ (dBm) \cong 40 +$$

$$10 \log_{10} [(V^+ - 1)(I_Q/2)] \quad (6)$$

For example, 50Ω transformed to 500 Ω at an open-drain IF output provides +16dBm OIP_3 with only 4mA current drain.

Finally, receiver current drain is minimized over time by simply placing the circuit in an idle mode when the receiver is not needed. Typical idle-mode current drain is between 10 and 100μA. The idle mode is activated by a CMOS logic line from the system controller.

Receiver design can be simplified by combining front-end components, such as the LNA and mixer, into a single plastic SO-14 or SO-16 package. The LNA/mixer combination usually excludes the LO in order to meet the widest set of applications.

An example of such an LNA/mixer architecture (Fig. 2) contains all necessary receiver front-end functions except the LO and passive filtering. The IC (model RF2401) contains a high-dynamic-range LNA, a 1-bit digital attenuator to reduce mixer input level in the presence of strong signals, a second RF amplifier bundled with a double-balanced mixer, and an IF output buffer. The output of the LNA is available externally to permit optional insertion of a bandpass filter between the LNA and mixer.

The LNA/mixer IC achieves 21 dB total gain and 3dB noise figure in a 50Ω system. It draws 30mA from a +5V_{DC} supply with -7dBm input IP_3 level. The IC incorporates a logic-controlled switch for 10μA idle-mode operation. No external-matching circuitry is required.

A similar circuit (Fig. 3) draws 15mA from a power supply as low as +3V_{DC} with similar intermodulation and noise performance, as well as 18dB gain in a 50Ω system (model RF2418). The IC's output buffer can be connected in a high-impedance configuration to reduce current drain to only 6.5mA. With a 500Ω IF load, the total gain increases to 24dB in this mode.

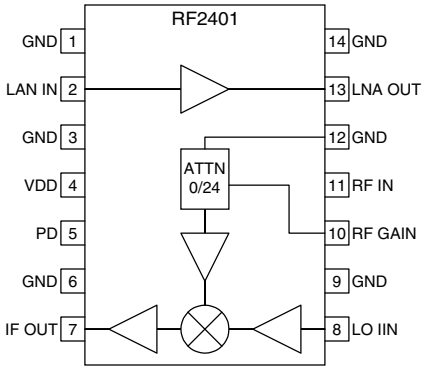


Figure 2: This LNA/Mixer IC includes idle-mode power switching and a digital attenuator to reduce mixer-generated image signals.

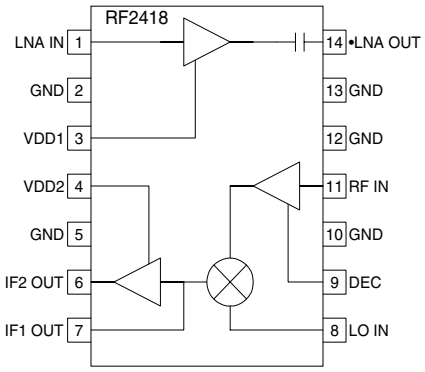


Figure 3: This LNA/Mixer IC includes idle-mode power switching and a digital attenuator to reduce mixer-generated image signals.

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Low-Cost Integrated Solution for Analog Cellular RF Blocks

Abstract

As the United States analog cellular market continues to enjoy expanding markets in most cities, the need for improved cost performance of analog hand-held units continues to increase. Even though the implementation of digital cellular systems is just around the corner, the analog market is expected to remain significant for years to come. As analog hand-held designs have matured over the years, the design focus has shifted from technology development toward size and cost reductions. A seemingly good solution for the size and cost requirements is to replace discrete or module based RF blocks with surface mount integrated circuits (RFICs), providing that the analog cellular performance requirements (IS-19B) can be satisfied with the IC's particular technology. Until recently, IC solutions were possible that satisfied either the size and performance or the size and cost requirements, but not all three. This paper presents an IC solution to the analog cellular receive LNA/Mixer and transmit Power Amplifier blocks that satisfies the performance and size requirements at a favorable cost, competitive with discrete solutions. System considerations, such as filter requirements, gain levels, noise performance, intermodulation performance, and power control are discussed.

Introduction

The technical specifications for US analog cellular phones are found in Electronic Industries Association Interim Standard 19-B (IS-19B). This paper discusses some of the key RF specifications in that document, but the scope is not intended to be limited to this one system. The issues presented here are directly applicable to other similar analog systems, such as TACS, NMT, and CT1. The concepts and frequencies of operation have much in common between these systems, and the devices summarized in this paper have application to all of them. The receiver LNA (Low Noise Amplifier)/Mixers described here are also relevant to other 900MHz applications, including digital ones. A generalized, representative block diagram for a US analog cellular phone is shown in Figure 1. In response to present day market pressures to minimize cost and size, a logical level of integration for some of the RF blocks is indicated by the dashed lines in the block diagram.

RF Block Descriptions

The duplexer is effectively two ganged filters that accomplish the frequency duplexing (hence the filter's name) of the input Rx frequency band (869-894MHz) with the output Tx frequency band (824-849MHz). This allows both bands to share a common antenna. The filter response of the Tx-Ant path serves to limit the amount of Rx-band noise generated in the transmitter that reaches the Rx LNA input. It also attenuates the harmonics of the Tx frequency that reach the antenna and get radiated. The Ant-Rx path filter response protects the Rx LNA from potentially harmful levels of Tx power and attenuates the receiver's response to the first IF image.

The LNA's main function is to provide enough gain to overcome the noise figure of subsequent stages, while adding as little of its own noise to the signal as possible. In effect, the Rx LNA sets the receiver's noise figure, and hence its sensitivity level (minimum usable input signal level). In contrast, the LNA's gain tends to work against the over-all linearity of the receiver because the net IP3i (input third order intercept point) will be reduced from the mixer's IP3i by the combined gain of the LNA and filters appearing before the mixer. In other words, the higher the gain of the LNA, the lower the receiver's net IP3i, or linearity, will be. This assumes that the LNA's IP3i is sufficiently high, compared to the mixer's IP3i minus the net gain before it.

In most super-heterodyne receivers, an image filter is inserted between the LNA and the first mixer. This serves two similar functions. It provides attenuation, in addition to that provided by the duplexer, of the first IF image. It also prevents the LNA's output image-band noise from being converted down and degrading the IF signal to noise ratio (S/N).

The primary function of the mixer is to convert the input Rx frequency down to a fixed IF frequency. Which particular channel is converted to the IF is determined by the frequency of the LO source. Since the mixer's IP3i typically sets the receiver's over-all IP3i, the mixer design tends to focus on maximizing IP3i and the associated noise figure is accepted, with the intention of overcoming it with the LNA's gain and low noise figure. The critical balance in the LNA/Mixer design in most multi-channel receivers boils down to trading off the LNA's gain against the mixer's noise figure (balancing overall sensitivity with over-all linearity).

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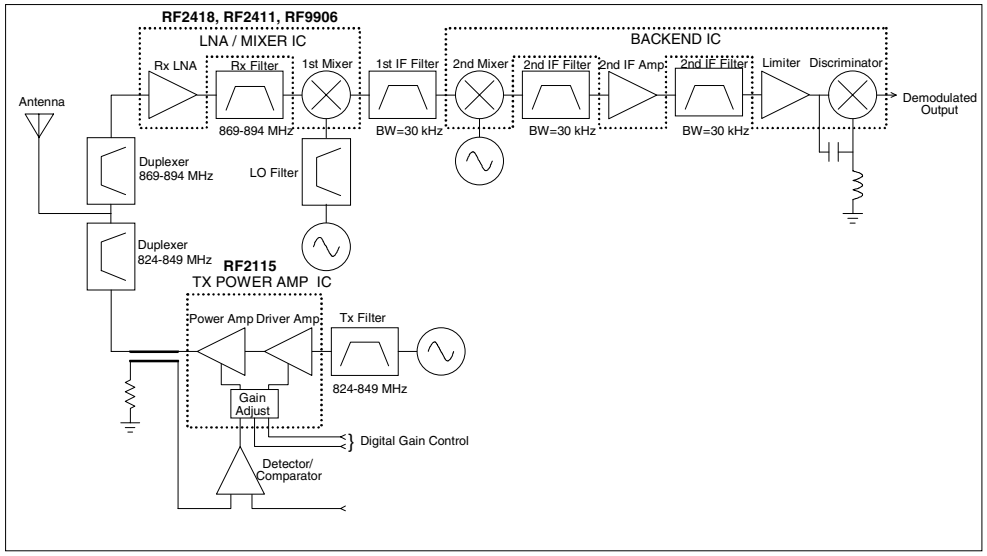


Figure 1. Typical Analog Cellular Radio RF Block Diagram

Many receiver designs also incorporate a filter between the Mixer's LO port and the LO source. The purpose of this filter is to prevent the noise at one IF frequency below the Rx from being mixed with the Rx down to the IF.

The IF filter that follows the mixer selects the channel that is to be passed on to the receiver back-end. In addition to initial channel selectivity, this filter prevents off-channel signals from reaching the back-end, where intermodulation distortion would be severe, due to the large levels of gain present. Because the interfering channels do not reach the back-end, the mixer primarily determines the overall IP3i. An additional function of the filter is that it attenuates the 2nd IF image response.

After the IF filter, the back-end of the receiver typically consists of a mixer that converts the IF down to a 2nd IF, limiting amplifiers, highly selective filters, and an FM discriminator. Single ICs that integrate these blocks (not including the filters) are readily available from several manufacturers. The reason for converting to a 2nd IF (commonly 455kHz) is that tight filtering and high levels of gain (>100dB) can be accomplished more economically. The demodulated output of the discriminator is passed on to base-band signal processing where voice, supervisory tones, signaling tones, and wide-band data are separated and processed independently.

The Tx Power Amp's (PA's) main function is to supply specified levels of output power at the antenna port. The power amp must be capable of adjusting its output power over a range of at least 20dB. A key concern for the power amp is that it supply the maximum specified output power as efficiently as possible, since the PA's efficiency is the major factor in determining a handheld unit's battery life. The PA must also not add so much Rx-band noise that the level that reaches the LNA input degrades receive sensitivity. The PA's noise performance determines the minimum Rx-band attenuation that will be required of the duplexer. Similarly, the harmonic output of the PA and the power detecting circuitry will determine the amount of harmonic attenuation required of the duplexer. The gain designed into a PA must also be carefully considered. There must be enough gain to ensure that the output remains saturated in order to maintain efficiency, but too much gain will degrade the relative attenuation of spurious signals. In many cases there are in-band spurs that cannot be eliminated completely by frequency plan selection and/or shielding. The amount of spur enhancement in the PA, therefore, must be minimized, and this usually correlates to keeping the gain low. Another key consideration for the PA is that it will see a wide range of impedance change from the antenna, as well as a highly reflective impedance outside of the

duplexer's pass band. The PA must be able to maintain its performance over a wide range of load VSWR's.

The primary function of the Tx filter preceding the PA is to reduce the amount of Rx-band noise generated in the Tx frequency source. In some cases, by using a high quality (low noise) source, this filter may be eliminated. An additional feature of this filter is that it attenuates Tx harmonics from the source before they reach the PA input.

The coupler between the PA output and duplexer is used to obtain an output power sample that is detected for output power level verification and control.

Specific Analog Cellular Requirements

In describing the receiver performance requirements, it is best to discuss RF Sensitivity first, because this measured level becomes the reference for measuring other receiver criteria. RF Sensitivity is the power level, in dBm, of a carrier FM modulated with a 1kHz test tone that, when demodulated by the receiver under test, produces a 1kHz audio signal with a 12dB SINAD ratio (Signal-plus-Noise-plus-Distorton to noise-plus-distortion). 12dB SINAD is a common reference and is generally regarded as the minimum allowable audio quality. RF Sensitivity is then the minimum usable carrier level that can be received by the subscriber unit. IS-19B specifies this level as -116dBm, maximum.

Since SINAD is primarily dominated by the S/N of the demodulated audio, assuming that the demodulator and audio circuits have moderate to low distortion, the key issue for achieving adequate sensitivity is to maintain a good S/N throughout the entire receive path. This is synonymous with keeping a low overall noise figure for the entire receiver. In order to keep the overall noise figure acceptably low, certain RF blocks must be carefully designed for low individual noise figures. By referring to the equation for cascaded noise figure (in this equation, NF and G are linear, not dB, expressions),

$$NF_T = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{NF_n - 1}{G_1 G_2 G_3 \ldots G_n},$$

we see that the total cascaded noise figure for a given system will be dominated by the noise figure of the first stage or two if the first stages have enough gain, since the noise figure of each stage is divided by the gain that appears before it. Note that in the simple case of two cascaded blocks,

$$NF_T = NF_1 + \frac{NF_2 - 1}{G_1},$$

the noise contribution of the second stage is reduced by the gain of the first stage. From this equation we can see that it is desirable to keep the LNA's gain fairly high, and that the NF of the LNA must be minimized. It is also obvious that every dB of insertion loss before the LNA degrades the NF by approximately 1dB. For this reason, the insertion loss of the duplexer must be minimized.

Given that the specified level for sensitivity is -116dBm, that the thermal noise power available in a 30 kHz band-width is

$$kTB = -174 + 10\log(30{,}000) = -129.2(dBm),$$

and that a Carrier-to-Noise (C/N) of approximately 2 dB at the input of a typical FM demodulator correlates to 12dB SINAD, the theoretical lowest obtainable sensitivity can be determined as follows**:**

$$-129.2 + 2 = -127.2dBm$$

The maximum allowable noise figure for the receiver to satisfy sensitivity can be found by comparing this limit to the specification:

$$-116 - (-127.2) = 11.2dB$$

This indicates that a receiver with an over-all NF of 11.2 dB should barely be sufficient to meet the -116 dBm sensitivity requirement. For every dB of sensitivity margin desired, the receiver's net noise figure must be reduced one dB from 11.2dB. The spread sheet shown in Figure 2 calculates, among other things, the total noise figure of a cascaded set of RF blocks, based on the cascaded noise figure equation. The numbers used in this analysis are based on filters and a back-end IC that are commercially available. This spread sheet illustrates how that, given a desired sensitivity of-119 dBm, the gain and noise figure of the LNA and noise figure of the mixer can be set in order to achieve a desired sensitivity.

In order to discuss other receiver specifications, it is first necessary to describe the specified measurement method. In these tests, the RF input is varied until

CALCULATED DATA		ENTERED DATA									
	TOTAL SYSTEM	DUPL.	LNA	RX BPF	MIXER	IF BPF	BK. END 2ND MIXER	BK. END 2ND IF BPF	BK. END IF AMP	BK. END 2ND IF BPF	BK. END LIM.
NF (dB)	8.2	3.3	1.8	2.5	9.5	2.0	6.2	6.0	10.0	6.0	20.0
Gain (dB)	114.0	-3.3	11.0	-2.5	3.8	-2.0	17.0	-6.0	44.0	-6.0	58.0
IP3i (dBm)	-7.0	100.0	-5.0	100.0	0.0	25.0	-9.0	100.0	-30.0	100.0	-40.0
Selecitvity	N/A	0.0	0.0	0.0	0.0	20.0	0.0	30.0	0.0	30.0	0.0
Sens. (dBm)	-119.0										
IM (dB)	73.7		BW (kHz)		30.0	C/N Ratio		2.0	C/I Ratio		6.0

Figure 2. Receiver Performance Spread Sheet Analysis

12dB SINAD is measured at the output. This sensitivity level is recorded and the input generator's level is increased by 3dB. Depending on the test being performed, an interfering signal or signals are introduced. The interfering signals' input levels are increased until the measured SINAD falls back to 12dB. The difference between the interferers and the sensitivity (not the sensitivity plus 3 dB) is what is specified.

In the case of Adjacent and Alternate Channel Desensitization, the specifications are 16 and 60dB respectively. These specifications dictate the minimum amount of net attenuation required by the IF filters at (one and two channel spacings away from the input channel. The design tradeoff here is that increasing the selectivity of the 1st and/or 2nd IF filters will improve this measurement, but may have a negative effect on the filters' size, cost, and group delay ripple. Increasing the group delay ripple will increase the demodulated audio's distortion and increase the wide band data Bit Error Rate (BER). For these reasons, it is best not to try for too much margin on the Adj./Alt. specifications.

The IS-19B specification for Intermodulation Spurious Response Desensitization performance (termed here "IM") is 65dB. IM is the measured difference between the sensitivity level and the level of two interfering sources placed at 60 and 120kHz above or below the tuned channel. These two interfering sources will produce third order responses due to non linearities in the receiver. One of these responses will land at the same frequency as the tuned frequency, i.e. co-channel interference. Figure 3, demonstrates that IM is related to the receiver's IP3i by the following equation:

$$IP3i = S + \frac{C}{2} + \frac{3IM}{2} - \frac{3}{2} \qquad (dB).$$

C is the Carrier to Interferer ratio (C/I), in dB, which has the effect of causing the increased input's SINAD to fall back to 12dB. This ratio is typically 6dB for FM discriminators. S is the measured sensitivity level.

If we wanted to build a receiver with 70dB IM and -119 dBm sensitivity, the receiver's net IP3i would then need to be -12.5dBm. A significant point results from considering this equation. If we rearrange the equation to express IM in terms of IP3i and sensitivity,

$$IM = +\frac{2IP3i}{3} - \frac{2S}{3} - \frac{C}{3} + 1 \qquad (dBm),$$

we see that for a fixed IP3i, the IM improves 2/3dB for every 1dB of improvement in sensitivity. In other words, for IS-19B applications, noise figure and IP3i are interrelated, and better sensitivity will improve IM without having to increase the IP3i.

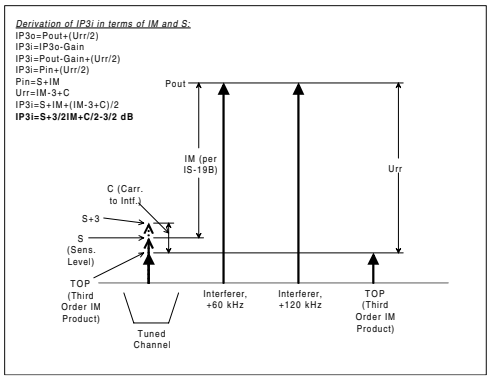


Figure 3. Receiver Output Spectrum

Given that we now have a relationship established between IM and IP3i, we can use the cascaded IP3i equation (in this equation, IP3i and G are linear, not dB

expressions),

$$\frac{1}{IP3_{iT}} = \frac{1}{IP3_{i1}} + \frac{G_1}{IP3_{i2}} + \frac{G_1G_2}{IP3_{i3}} + \frac{G_1G_2G_3}{IP3_{i4}} + \ldots + \frac{G_1G_2G_3\ldots G_n}{IP3_{in}},$$

to analyze the effects of individual blocks' IP3is on the receiver's IM. Referring back to the spread sheet of Figure 2, we see how the mixer's IP3i and the LNA's gain and noise figure can be traded off and what the expected net IM will be. The mixer and LNA parameters were varied to yield a total sensitivity of -119 dBm and an IM of at least 73dB.

Another key consideration for the filter selections throughout the receiver is insuring that the receiver does not respond to frequencies outside of its designed input range (869-894MHz). One of the bands that will most likely have a response is the first image, situated in the band two IF frequencies above the Rx band, assuming the LO is injected at one IF above the Rx-band (high side injection). The response tendency exists here because signals in this band that reach the mixer will also convert down directly to the IF. The combined filtering from the duplexer and Rx filter (or image filter) must attenuate this band enough that signals introduced at 60dB or more above the measured sensitivity will not cause the SINAD to fall below 12dB when the receiver is being supplied with an on-channel modulated carrier. Another likely response will occur at what is called a "half-IF spur". This occurs at an input frequency that is one half of the IF frequency above the tuned input channel. The response here is due to 2nd order distortion in the receiver, primarily in the mixer. The mechanism is the 2nd harmonic of the spur frequency mixing with the 2nd harmonic of the LO, and the difference-product lands at the IF. This tends to come into play only when the IF frequency is low and the receiver is tuned to the lower channels. Otherwise, the spur is attenuated by the duplexer and/or the image filter so much that the second order distortion of the mixer does not come into play. Another very likely spur frequency will occur two 2nd IF spacings away from the tuned channel. Both this frequency and the tuned channel will mix down in the 2nd mixer to the second IF frequency. The only filter that can provide any useful attenuation of this relatively close spur is the 1st IF filter. Given that a C/I of ~6dB will cause the discriminator's output SINAD to fall back to 12dB, and the specification, relative to the sensitivity level, is 60dB, then the IF filter should have

$$60 - 3 + 6 = 63(dB),$$

minimum, of attenuation at the second IF image.

Another consideration for the filter selection in the receiver is the conducted spurious specification of -47dBm, maximum. From the receiver, the most likely candidate for leakage out the antenna connector is the LO. The actual amount of LO power conducted out of the antenna port will be determined by the LO drive level, the LO-to-RF leakage in the mixer, the reverse isolation of the LNA, and the net attenuation of the LO band in the image filter and duplexer. This specification has little bearing on most designs, however, because the small amounts of attenuation required of the filters in the LO band tend to fall out naturally by satisfying the image requirements.

Transmitter specifications require the power radiated by the antenna to be controllable over a 20dB range for hand-held (Class III) units. This range is selectable in 4 dB steps from +28dBm to +8dBm. The individual power levels (PL2=+28 through PL7=+8dBm) are selectable by the cellular system in order to balance system power requirements. These requirements dictate that some sort of power level control circuit be incorporated into the transmit RF power amp. In addition, detector circuitry is normally incorporated after the PA to sample the output power as part of a closed loop control circuit. The key requirement here is that the power amp must be able to vary its output according to an input analog and/or digital control signal. In addition, it must have at least a 20dB control range for hand-held operation.

The PA must also be as efficient as possible, while meeting the other RF requirements, at PL2 (maximum output). This requirement is not specified by IS-19B. However, it is highly desirable, from the user's point of view, for the current drain under transmit conditions be minimized. This maximizes "talk time", a key consumer consideration.

Another key requirement of the PA is that it maintain stability under a very wide range of load conditions. In-band, the PA may see large impedance changes due to the antenna's proximity to various objects (i.e. users, metal structures, etc...). Out of band, the PA is guaranteed to see severe mismatches, due to the duplexer's out-of-band impedance. The PA will also be required to source a fixed amount of output power, regardless of

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the load variations, since the power control loop will detect primarily forward power.

Regarding harmonics and spurious Tx frequencies, the maximum relative levels allowed to be conducted to the antenna are related to the output level by the following equation:

$$dBc(\min) = 43 + 10\log(Pout, inwatts).$$

At maximum output (PL2), the output power is 28dBm, or -2dBw. Therefore, the minimum attenuation of any spurious or harmonic signal out of the duplexer is

$$43 + (-2) = 41(dBc).$$

The difficulty of meeting this requirement is that most FM power amps employ saturating output devices. Saturating amplifiers tend to degrade the input carrier to spurious attenuation due to the fact that the amplifier limits the gain of the carrier due to the output limiting on the larger signal, but the spur's gain is not reduced nearly as much, depending on what the small-signal gain is. Note that this phenomenon is most significant for frequency plans where the spurious signals fall within the Tx band, and the duplexer's selectivity will not help reduce the spurious level. This consideration, along with the power level available from the Tx source, will determine what the gain of the PA is designed for.

Another difficulty with saturating power amps, is that their outputs clip. The obvious by-product of a clipping stage is an output spectrum with appreciable harmonic content. In addition, the diode based detectors used in most power control circuit designs are quite capable of generating harmonically rich spectra. Achieving harmonic suppression at the antenna will be largely the burden of the duplexer.

Another implied requirement of the PA is that it not degrade Rx sensitivity by raising the Rx-band noise floor such that the noise power into the Rx port of the duplexer is higher than kTB. In order to keep the transmitter's noise from affecting the receiver, the noise must be at least a few dB below kTB. Since the Tx source will provide kTB, at minimum, to begin with, the duplexer must filter out at least all of the noise amplified and added by the PA. If the transmitter design includes a Tx filter between the PA and Tx source, then the noise contributions come solely from the PA. This filter is not used in designs where the Tx source has good noise performance and the duplexer provides sufficient attenuation in the Rx-band.

Requirements Satisfied

Three LNA/Mixer ICs have been designed to meet the requirements of IS-19B. Table 1 summarizes their key performance parameters

Device	LNA Gain	LNA NF	LNA IP3i	Mxr Gain	Mxr NF	Mxr IP3i	Idd/ Vdd
RF2418	11.0	1.8	-5	3.8	10.5	0	7 / 5.0
RF2411	13.5	1.9	-5	7.2	10.0	5	14 / 4.0
RF9906	16.5	1.5	-6	4.0	9.0	6	20 / 3.6

Table 1. LNA/Mixer Performance

The RF2411 was fabricated in a GaAs MESFET process. It has two output options, one high impedance output suitable for matching to high impedance IF filters, and one ~50 ohm buffered output for devices requiring a low impedance source. The RF2411 is fabricated in a GaAs HBT (Heterojunction Bipolar Transistor) process, and has balanced outputs. The RF9906 is also fabricated in a GaAs HBT process, and features selectable IF amplifiers after the mixer, one balanced output and one single-ended. It's IP3i has also been improved over the other two parts. All three parts operate off of single-ended supplies (no negative supply is required).

The spread sheet calculations shown in Figure 4 illustrate IS-19B receiver specification compliance of systems based on all three LNA/Mixer ICs. Here again, the calculations are based on a commercially available back-end IC and filters.

An HBT power amplifier design has been developed, the RF2115, to satisfy IS-19B receiver requirements. Since this PA uses HBT technology, it operates with 50% efficiency on a single supply. No negative supply is required, as is the case with most MESFET PAs. Table 2 summarizes the major parameters.

Psat, (dBm) Vcc= 5.0	Psat, (dBm) Vcc= 5.8	Psat, (dBm) Vcc= 6.5	Small Sig. Gain (dB)	Eff. (%)
29.3	30.4	31.5	32	50

Table 2. RF2115 Performance

The RF2115 has two types of power control capability. Vcc1 can be used to provide analog power control. Two bits of digital gain control, which vary the output in 10dB steps over a 30dB range, are also provided. The analog gain adjustment can be used in conjunction

CALCULATED DATA		ENTERED DATA										
RF2418	TOTAL SYSTEM	DUPL.	LNA	RX BPF	MIXER	IF BPF	BK. END 2ND MIXER	BK. END 2ND IF BPF	BK. END IF AMP	BK. END 2ND IF BPF	BK. END LIM.
NF (dB)	**8.3**	3.3	**1.8**	2.5	**10.5**	2.0	6.2	6.0	10.0	6.0	20.0
Gain (dB)	**118.7**	-3.3	**11.0**	-2.5	**8.5**	-2.0	17.0	-6.0	44.0	-6.0	58.0
IP3i (dBm)	**-7.3**	100.0	**-5.0**	100.0	**0.0**	25.0	-9.0	100.0	-30.0	100.0	-40.0
Selecitvity	**N/A**	0.0	0.0	0.0	0.0	20.0	0.0	30.0	0.0	30.0	0.0
Sens. (dBm)	**-118.9**										
IM (dB)	**73.4**		BW (kHz)		30.0	C/N Ratio		2.0	C/I Ratio		6.0

CALCULATED DATA		ENTERED DATA										
RF2411	TOTAL SYSTEM	DUPL.	LNA	RX BPF	MIXER	IF BPF	BK. END 2ND MIXER	BK. END 2ND IF BPF	BK. END IF AMP	BK. END 2ND IF BPF	BK. END LIM.
NF (dB)	**7.1**	3.3	**1.9**	2.5	**10.0**	2.0	6.2	6.0	10.0	6.0	20.0
Gain (dB)	**119.9**	-3.3	**13.5**	-2.5	**7.2**	-2.0	17.0	-6.0	44.0	-6.0	58.0
IP3i (dBm)	**-6.2**	100.0	**-5.0**	100.0	**5.0**	25.0	-9.0	100.0	-30.0	100.0	-40.0
Selecitvity	**N/A**	0.0	0.0	0.0	0.0	20.0	0.0	30.0	0.0	30.0	0.0
Sens. (dBm)	**-120.1**										
IM (dB)	**75.0**		BW (kHz)		30.0	C/N Ratio		2.0	C/I Ratio		6.0

CALCULATED DATA		ENTERED DATA										
RF9906	TOTAL SYSTEM	DUPL.	LNA	RX BPF	MIXER	IF BPF	BK. END 2ND MIXER	BK. END 2ND IF BPF	BK. END IF AMP	BK. END 2ND IF BPF	BK. END LIM.
NF (dB)	**5.9**	3.3	**1.5**	2.5	**9.0**	2.0	6.2	6.0	10.0	6.0	20.0
Gain (dB)	**119.7**	-3.3	**16.5**	-2.5	**4.0**	-2.0	17.0	-6.0	44.0	-6.0	58.0
IP3i (dBm)	**-7.5**	100.0	**-6.0**	100.0	**6.0**	25.0	-9.0	100.0	-30.0	100.0	-40.0
Selecitvity	**N/A**	0.0	0.0	0.0	0.0	20.0	0.0	30.0	0.0	30.0	0.0
Sens. (dBm)	**-121.3**										
IM (dB)	**74.9**		BW (kHz)		30.0	C/N Ratio		2.0	C/I Ratio		6.0

Figure 4. Receiver Performance Calculations Based on Three LNA/Mixer ICs

with the digital steps in order to achieve both high resolution and a large range (>30dB) while maintaining a relatively constant level of compression over the full control range. In addition, the power control loop delay is maintained relatively constant over the full range.

Conclusion

The RF requirements of IS-19B and how they drive individual block requirements were described. In addition, three LNA/Mixer ICs and one power amp that satisfy IS-19B requirements were presented. These devices are available from RF Micro Devices, Greensboro, NC. In addition to these devices, similar designs for digital systems are also available.

This paper was originally presented during the RF Expo West, San Diego, January 1995.

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ICs Simplify the Design of Digital Communications Links

Integrated solutions perform a host of RF functions in a wide range of emerging digital communications systems.

Digital communications systems are slowly replacing their analog counterparts. The potential is significant for applications which blend low-cost digital-signal-processing (DSP) functions with new RF integrated circuits (ICs) aimed at wireless designs. This first of four articles will examine the requirements for ICs in these emerging digital communications systems, starting with modulators.

Digital RF links (Fig. 1) require more sophisticated RF circuitry than their analog predecessors to produce and decode more complex modulation schemes. Transmitters must be extremely linear and accurate in frequency and power level, while receivers must be linear with accurate demodulation processes.

In a digital RF link, data may be purely digital or partly digital and partly analog (such as digital cellular telephones). Numerous emerging applications, such as wireless local-area networks (WLANs) and security systems, also make use of spread-spectrum frequency allocations at 900 and 2400 MHz.

In a typical digital RF link, RF inputs and outputs are quadrature baseband signals suitable for conversion to and from digital data bits. A transmit/receive (T/R) switch is necessary for time multiplexing, while an antenna diversity switch is sometimes used to eliminate nulls caused by multipath effects. (Fig. 2)

Generally, processor-generated data words are multiplexed with digitized analog data and then serialized, forming a long serial-data bit stream which is sent asynchronously over the RF link. As in RS-232 links, the data will often be duplexed; that is, sent and received in bursts for bi-directional operation. Two multiple-access schemes for RF digital transmissions are the time-sharing time-division-multiple-access (TDMA) and code-dependent code-division-multiple-access (CDMA) formats. In each format, especially the latter, sophisticated RF ICs are required for system implementation.

An IC which facilitates the modulation of an RF carrier by digital data is the quadrature modulator. It transforms digital data for transmission to modulated RF signals. Sophisticated systems include a pair of digital-to-analog converters (DACs) and anti-alias filters between the processor and the quadrature modulator. The resulting RF signal needs only to be amplified and fed to an antenna.

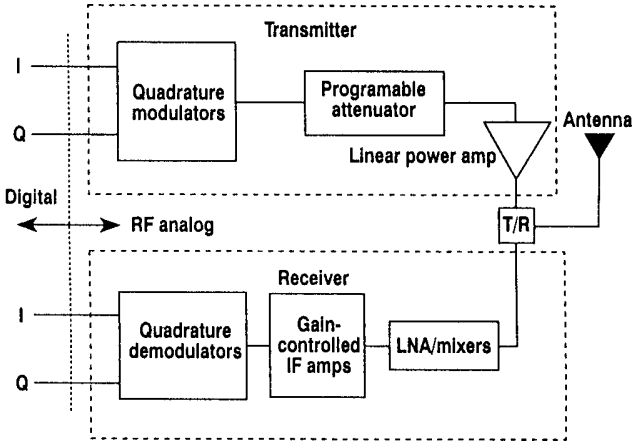


Figure 1. Quadrature modulators play key roles in the transmitter and receiver sections of wireless communication systems.

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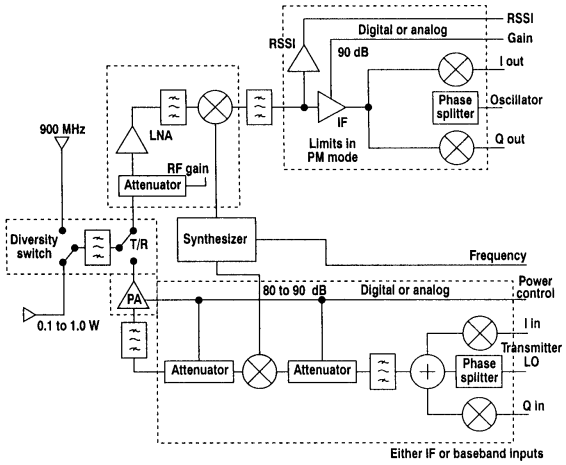


Figure 2. In a typical RF data system, a high-speed switch selects between receiver and transmitter sections.

Some systems may generate data with an application-specific integrated circuit (ASIC) and feed the digital data directly to the quadrature modulator. Spread-spectrum data transmitters are often implemented by convolving the data with the pseudo-random spreading sequence and applying digital signals directly to a quadrature modulator.

In frequency-shift keying (FSK), a modulated frequency (¦m) is added to a carrier frequency (¦c) to represent a binary 1 or subtracted from the carrier for a binary 0. The carrier frequency is set by a crystal oscillator with a phase-locked loop (PLL) or a direct digital synthesizer (DDS). The processor typically controls the transmit and receive frequencies to minimize interference and maximize data reception. A simple FSK scheme involves application of the modulating signal to the PLL.

Time-multiplexed FSK requires that the signal be ramped up and down in order to avoid spectral splatter from the instantaneous change of digital states. Similarly, the pan-European GSM system employs Gaussian-minimum-shift-keying (GMSK) modulation to conserve frequency spectrum. In this approach, a Gaussian filter smooths the modulation signal; the system operates with partial responses with minimized bandwidth requirements and greatly-attenuated out-of-band sidelobes. The Gaussian filters are implemented digitally. The quadrature components of the modulating signal are digitally derived, converted to analog signals with DACs, and applied to a quadrature modulator.

Unlike FSK, quadrature phase-shift keying (QPSK) permits the transmitted symbol to contain more than one bit of information, increasing the amount of data per frequency channel. QPSK is most-commonly generated by quadrature modulators. The quadrature modulator allows control of the phase and amplitude of the RF carrier. Frequency modulation (FM), phase modulation (PM), and/or amplitude modulation (AM) can be achieved by orthogonal modulation of the fixed carrier while generating low spurious products.

The RF signal generated by the quadrature modulator can be expressed as:

$$x(t) = a(t) \cos [2pf(t) + (f)] \quad (1)$$

where:

f = the signal frequency,

a = the signal amplitude,

x = the signal displacement, and

f = the phase modulation or shift.

This equation can be rewritten as:

$$x(t) = I(t) \cos [2pf(t)] - Q(t) \sin [2pf(t)] \quad (2)$$

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where:

I(t) = the in-phase modulation component, and

Q(t) = the quadrature modulation component.

Both signals are inputs to the modulator. The output of the two multiplication processes are simply summed to obtain the desired result.

To generate arbitrarily-modulated signals, the I and Q baseband input signals must have precise time values. The signals are usually derived through digital means to optimize programmability, achieve exact transfer functions, and maintain small size and low price. For GMSK, for example, simple look-up tables can be used to find the sine and cosine of the angle information from a digital Gaussian filter.

In the modulator, double-balanced mixers translate the input information to a modulated carrier. In these mixers, the carrier must also be available in phase quadrature (90 deg.) to suppress the ambiguous frequencies created in the multiplication process. As a result, the modulator also contains a phase shifter to derive quadrature signals from the local oscillator (LO). The mixers multiply the LO, and modulation signals and their outputs are added. When the I and Q inputs are in phase quadrature, the output is that of a single-sideband modulator.

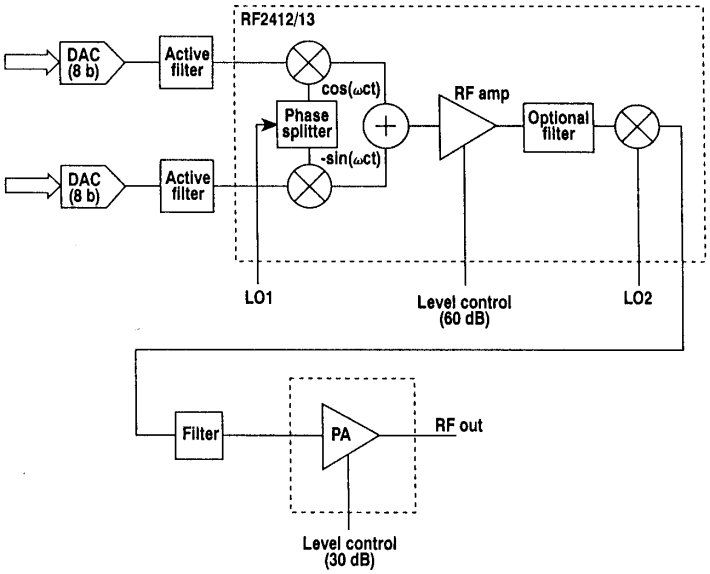


Figure 3. Level control can be implemented at both the IF and RF output stages in an IF modulation system for CDMA applications

When the I and Q baseband input signals are not accurate, frequencies other than the desired offsets are generated, such as unsuppressed sidebands. A 40-dB sideband suppression level implies 1-deg. phase accuracy and 1-percent amplitude matching between the I and Q signals. Residue of the carrier signal results from DC offsets on the I and/or Q input signals to the modulator. If the I and Q signals are balanced, the carrier will disappear.

Intermodulation (IM) products can be created by nonlinearity during the multiplication process. The IM level usually increases with the amplitude of the modulating signals as the modulators are driven closer to saturation.

In some architectures, a transmit intermediate frequency (IF) is used rather than directly modulating the RF carrier. In such cases, a highly-integrated circuit may be needed, where a quadrature modulator is linked on chip to a frequency upconverter (Fig. 3).

In CDMA applications, the output signal must be controlled over a 60-to-90-dB range. With a modular/con-

verter IC, some of this level control can be achieved at the IF stage, with the remainder executed at the power-amplifier stage.

Modulators fabricated with IC processes cost less than hybrid approaches and can be housed in tiny SOIC packages. Improved performance results from the inherent component matching and propagation-path equalization from the IC process. (The model RF2402 quadrature modulator IC provides phase and amplitude accuracies of 2 deg. and 1 dB from 800 to 1000 MHz, for example, with 0-dB output power and simple interface to DACs.)

Fabrication processes for IC quadrature modulators include silicon-bipolar, GaAs MESFET, and heterojunction-bipolar-transistor (HBT) technologies. Silicon-bipolar technology offers the lowest operating frequencies of the three, working well through VHF with limited output levels at higher frequencies. (Silicon-bipolar models RF2802 and RF2803, for example, provide output signals to 200 and 900 MHz, respectively.) The technology has high internal parasitic coupling between on-chip components, necessitating the design of balanced structures (such as baluns) to maintain carrier suppression and phase balance. The interface to external circuitry must contain some form of internal or external balun.

GaAs MESFET modulators provide higher output levels at higher frequencies than silicon units, with more functionality. Because GaAs substrates offer much better isolation, single-ended 50-W input and output ports can be used for simpler user interfaces (eliminating baluns for example). GaAs units feature better performance than silicon units at higher frequencies, such as UHF. As an example, the RF2402 GaAs modulator delivers good phase accuracy to 900 MHz with a single-ended output level of 0 dBm into a 50-W load. For more power, the RF2423 GaAs modulator produces as much as +20 dBm at the same frequency and includes a gain-control function. GaAs MESFET IC technology is the optimum choice for most 900-MHz applications, considering its breadth of functionality and minimal external circuitry.

HBT quadrature modulators offer improved performance above 2 GHz and smaller size compared to GaAs MESFET devices. (Model RF2422 uses this technology to match the performance of the RF2402 modulator from 1500 to 2500 MHz.) Unfortunately, the technology is still more expensive than silicon-bipolar or GaAs MESFET technologies so HBT technology should be reserved for those applications above 2 GHz that require the best performance and highly-integrated functionality.

Future articles in this series will feature ICs for other sections of digital RF links. The next installment will examine programmable attenuators and plastic-packaged linear power amplifiers based on HBT technology.

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A Linear, High Efficiency, HBT, CDMA Power Amplifier

Abstract
RF Micro Devices introduces a new linear power amplifier for CDMA applications based on their HBT (Heterojunction Bipolar Transistor) technology. This power amplifier operates from a single 4.8V power sup-ply without the need for a negative voltage. The amplifier will provide up to 29dBm average output power under CDMA modulation, with >50% efficiency! Saturated output power for analog operation is 31.5dBm at over 57% efficiency. On-board power down is included, and provides less than 10mA current consumption in the OFF state. The part is packaged in an industry standard 16-lead SOIC with a fused center lead. Pricing is competitive at less than $7 in volume.

Introduction
As CDMA (Code Division Multiple Access) systems begin to see implementation in the US and other countries, many manufacturers are rolling out their CDMA cellular handsets. The final power amplifier for these handsets is critical to the competitive positioning of the product. This power amplifier must:

- operate at full power with the CDMA waveform without generating adjacent channel interference,
- operate in analog AMPS or ETACS mode while in systems which do not support CDMA,
- have very high efficiency to maximize talk time,
- maintain efficiency and linearity at lower power levels.

Traditionally, CDMA power amplifiers have been based on hybrid modules, which are large and expensive. In contrast, the RF2108 is an integrated power amplifier, providing the full performance from a single 16-lead SOIC plastic package. This package may be assembled using standard surface-mount techniques, and enables the designer to maintain a very small footprint for the RF output interface.

Using HBT semiconductor technology from RF Micro Devices, the RF2108 allows full high-efficiency, linear performance from a single positive 4.8V power supply. The part operates from 4.0V to 4.8V, to accommodate battery voltage degradation. Power down is accomplished with 0V on a single control pin, consuming less than 10mA in stand-by mode. During full power operation, the power-added efficiency (or total efficiency) can be as high as 53% while simultaneously meeting CDMA Adjacent and Alternate Channel Interference requirements. When driven with a CW signal (as in FM-modulated AMPS mode), the output power at 4.8V increases to 31.5dBm at 57% efficiency. Depending upon the implementation of the power control ALC loop, an on-board control may be used for AMPS mode to provide >30dB of power control with a fixed input level. More commonly, the input level may be varied as is done in CDMA mode.

Key Advantages of HBT Power Amplifier Technology
The HBT Power Amplifier drives several key features of the phone operation and design. Some are advantages to the end customer, such as talk time and overall phone size. Others are related to the ease of design and manufacturing the phone, such as single voltage supply, on-board power-down, device linearity, and on-board power control. These advantages are discussed below:

- Talk time. The current consumption of the transmitter is nearly always dominated by the power amplifier. For battery operated applications, the power-added (or total) efficiency is extremely important. Linear applications such as CDMA have typically required Class-A biased power amplifiers, which have low efficiencies of approximately 25-35%. The RF2108 provides very high efficiency of >50% while meeting CDMA ACPR requirements. Also important for CDMA systems is the quiescent bias current. Since, in the CDMA system the average power levels are kept low, the current consumption at average +10dBm output is an important figure of merit. Since the RF2108 is biased deep into Class AB, the current consumption at +10dBm output is 40mA. This extends the lifetime of the battery under nominal operating conditions in the phone. Also, in analog mode, the RF2108 provides, without a matching circuit change, up to 31.5dBm with 57% efficiency.
- Small Package Size. CDMA cellular phones are entering a consumer market which is relatively mature. The consumer demands small handsets, which drives the PCB area available for the RF components. Most existing CDMA linear power amplifiers use hybrid modules, which are difficult to implement in the required area; thus, the SOIC packaged, integrated amplifier approach is extremely beneficial. The RF2108 replaces a mod-

ule implementation with a single 16-lead SOIC.

- No Negative Voltage. HBT is a unique technology, allowing performance better than GaAs MESFETs, yet allowing biasing similar to Silicon Bipolar from a single positive voltage. This eliminates one of the primary disadvantages with GaAs MESFETs – the requirement for a negative voltage. For a system de-signer to implement negative voltage with sufficient current to drive a power MESFET gate, some kind of switching regulator or "charge pump" must be used. This can be expensive and cumbersome. If the charge pump is implemented on-chip, excessive low-frequency noise, additional current, and additional external components minimize the benefit.
  HBT provides an elegant solution to the high-efficiency linear power amplifier. With no need for additional components, the part provides an overall smaller, more efficient, and lower cost solution.
- No supply-side switch. The RF2108 HBT Power Amplifier provides a single pin for power down. This function powers down the part with 0V on the control pin, and provides full power with 3.6V on the control. In power-down mode, less than 10mA of total current is consumed, allowing very long standby times for the phone.
  To utilize a GaAs MESFET power amplifier, the system designer generally must insert a switch into the bias supply line to the part for shutdown. This switch must be capable of supporting very high currents, and tends to be very expensive as a result. A MOSFET switch will cost on the order of $0.50 to $0.75, which is a substantial portion of the overall power amplifier cost. The loss through the switch also reduces the voltage available on the drain of the MESFET PA, thus requiring more current to achieve the same output power.
- Gain Control. Using the same pin as is used for power down, the gain can be controlled over 30dB with a 2.0V to 3.6V control range. Since linearity is not maintained during this power control, this function is useful in AMPS mode only; for CDMA mode the input power to the PA will be varied. If this function is not required, the pin may be tied strictly to a power down control.
- Low Noise-Power Output. A key parameter related to the power amplifier in AMPS mode is the noise power output in a 30kHz bandwidth. This defines the required rejection in the receive band (869MHz to 894MHz) for the duplexer, since for a full-duplex system the transmitter will tend to "self-jam" the receiver. The noise transmitted by the power amplifier is related to it's noise figure and gain in the receive band. The RF2108 operates with better than -90dBm/30kHz in the receive band.

HBT Technology

The RF2108 is one of a family of power amplifiers from RF Micro Devices based upon HBT technology for both linear and constant-envelope applications. This technology, provided by TRW and being commercialized by RFMD, is a proven technology originally developed for military and space applications. Based upon a Gallium Arsenide/Aluminum Gallium Arsenide (GaAs/AlGaAs) heterostructure, the power and efficiency performance is the highest of any commercially available integrated solution. Being a bipolar structure, the part can operate from a single positive voltage supply without adding components – extremely important in a battery operated system such as a cellular phone.

The critical geometries in a HBT transistor are vertical structures, not lateral. The emitter, base, and collector are stacked vertically by semiconductor layer growth, using MBE (Molecular Beam Epitaxy). This is a very accurate and repeatable growth process. Since each layer is placed over the entire wafer at once, no photolithography is required for this process; thus, mask alignment and optical resolution is not an issue. Also, this means wafers can be prepared and stock-piled, eliminating this step from the critical path of product manufacturing.

Once the layers are completed, then the lithography begins. Since all the critical geometries are already defined, the minimum feature size is currently 2μm. This is much more manufacturable than the 0.5μm to 1.0μm gate geometries typically required by GaAs MESFETs.

The TRW HBT process is the most reliable commercially available HBT process in the world. As a military subcontractor, TRW has qualified the process for many of their military programs. Additionally, as a space equipment manufacturer, the HBT process has been qualified for Class S space applications. This level of ruggedness is absolutely needed for spacecraft, since it is somewhat difficult to repair a failed component in space, but is also demanded by the commercial marketplace today. RF Micro Devices and TRW have both been diligently testing the HBT process and products to determine the ruggedness and failure rates. The MTBF is found to be $4x10^7$ hours at 125°C junction temperature, and $5x10^5$ hours at 185°C. Over 1.35 million device hours have been tested on packaged power amplifiers under full RF stress conditions at 250°C

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junction temperature without a failure to-date. Additional information is available on the reliability of HBTs, and may be obtained with the application information package on the RF2108.

RF2108 Theory of Operation and Application Information

The block diagram for the RF2108 is shown in Figure 1. The part is a two-stage device with 28dB linear gain. The drive required for full-power CDMA operation is approximately 0dBm. To fully saturate the output, approximately +4dBm CW is required. Bias control is provided through a single pin interface, and the final stage ground is achieved through the large pins on both sides of the package. First stage ground is brought out through a separate ground pin for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane. The output is brought out through the 4 output pins, with two pins providing bias and harmonic termination, and the other 2 pins feeding the RF output.

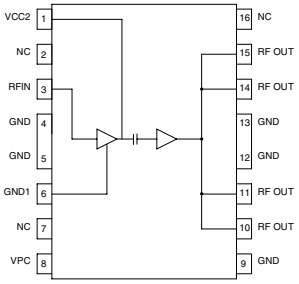


Figure 1. Block Diagram and pinout for RF2108

The amplifier operates in Class AB bias mode. The final stage is “deep AB”, meaning the quiescent current is extremely low, around 40mA. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at 27dBm average output power, draws about 240mA. The bias level changes according to the drive level without distorting the RF signal through a proprietary biasing technique (patent pending). The optimum load for the output stage is approximately 10Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, leads, and microstrip, and a shunt capacitor external to the part. With this match, a 50Ω terminal impedance is achieved. The input is matched to 50Ω with just a blocking capacitor needed.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive pull-up with high value resistors on this pin to Vpc. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

$V_{CC}2$ provides supply voltage to the first stage, as well as provides some control over the operating band. Essentially, the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be by-passed individually before being combined with Vcc for the output stage to prevent feedback and oscillations.

The RFout pins provide the output power. Bias for the final stage is fed to pins 14 and 15, which also provides the second-harmonic trap. Pins 10 and 11 provide the output line, which is matched as shown in the application schematic for optimum operation at either minimum battery voltage or nominal voltage.

The part will operate over a 4.0V to 4.8V range. If the full power is desired at minimum voltage, then the load can be optimized at that point. At that point, the specified efficiency, linearity and power should be attainable. As the voltage is increased, however, the output power will increase. Thus, in a phone design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This will occur at a less-than-optimum efficiency, since the load is optimized for 4.0V. This is true of any power amplifier, however, the important point to note is that the RF2108 can be set up to provide the specified power at 4.0V if desired.

The HBT breakdown voltage is >20V, so nominally at 4.8V there should be no issue with overvoltage. Under extreme conditions, however, which can occur in a cellular handset environment, the supply voltage could be as high as 8.5V. These conditions may correspond to operation in a battery charger, especially with the battery removed, which “unloads” the supply circuit. To add to this worst-case scenario, the RF drive may be at full power during transmit, and the output VSWR could be extremely high, corresponding to a broken or removed antenna. Under all of the above conditions, the peak RF voltages could well exceed 2X the supply voltage, forcing the device into breakdown. The RF2108 includes overvoltage protection diodes at the output, which begin clipping the waveform peaks at approximately 13V. This protects the device’s output from breaking down under these worst-case conditions, and provides a rugged, robust component for the system designer.

High current conditions are also potentially dangerous to any RF device. High currents lead to high channel

temperatures and may force early failures. The RF2108 includes a proprietary bias circuit (patent pending) to temperature compensate the RF transistors, thus limiting the current through the bias network and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations, and the part is remarkably consistent over the full -30°C to +85°C commercial temperature range.

RF2108 Performance

The RF2108 performance is summarized below. A full data sheet is available from RF Micro Devices.

The single-tone power and efficiency vs input power, along with the two-tone IMD products vs output power are shown in figures 2 and 3.

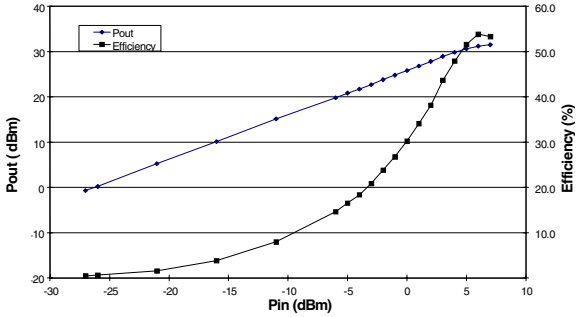


Figure 2. Power output and efficiency vs. input power

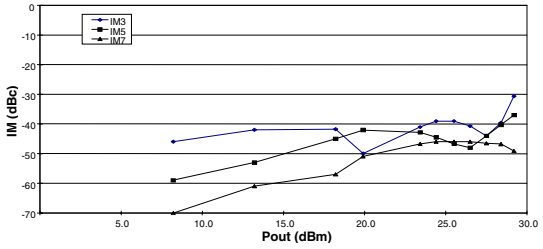


Figure 3. Two-tone IMD vs. output power

Since the CDMA utilizes QPSK signaling, the adjacent channel power (ACP) measurement test for linearity. Figure 4, 5 and 6 show plots with the ACP of the RF2108 at various power levels.

A common problem associated with high-efficiency cellular power amplifiers is stability, especially into a duplexer. Since duplexers can be designed with various out-of-band characteristics, a robust cellular power amplifier must operate without oscillation into ceramic, helical, and SAW duplexers. The RF2108 has been

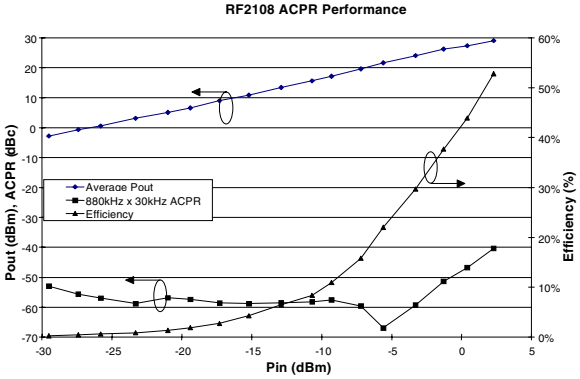


Figure 6. ACPR and efficiency vs. input power

tested into various types of duplexers, without oscillating.

Parameter	Typical Performance	Conditions
Frequency Range	800 to 900MHz	Externally tuned for individual bands
Maximum Linear Output Power	29dBm	While meeting ACP requirements
ACP @ 885kHz Offset	-40dBc	Relative to 1.23MHz center band
ACP @ 1.98MHz Offset	-60dBc	Relative to 1.23MHz center band
Maximum CW Output Power	31.5dBm	With specified load at 4.8V
Total CW Efficiency	57%	At Max Output
Power Gain	28dB	
Noise Power Output	-90dBm/30kHz	In Receive Band, any power setting
Quiescent Current	40mA	
"OFF" Current	10µA, max	V_{PC}<0.2V
Voltage Range	4.0 to 4.8V	
V_{PC} "ON"	3.6V	
Stability	Unconditional	
Temperature Range	-30 to +85°C	Operating

Conclusion

The RF2108 HBT CDMA Cellular Dual-Mode Power Amplifier has been introduced by RF Micro Devices. This amplifier provides the best overall performance of any CDMA PA on the commercial market. Operating from a single positive supply, linear efficiencies of 50% and power levels of 29dBm are achievable from a single 16-lead SOIC surface mount package from 4.0V to 4.8V. In AMPS mode, the part provides 31.5dBm power with 57% efficiency. Power down and power control are integrated on-chip without additional components required. The new power amplifier can be used to simplify cellular phone design and improve operation, as well as significantly reducing overall cost. The price of the RF2108 in volume is less than $7.

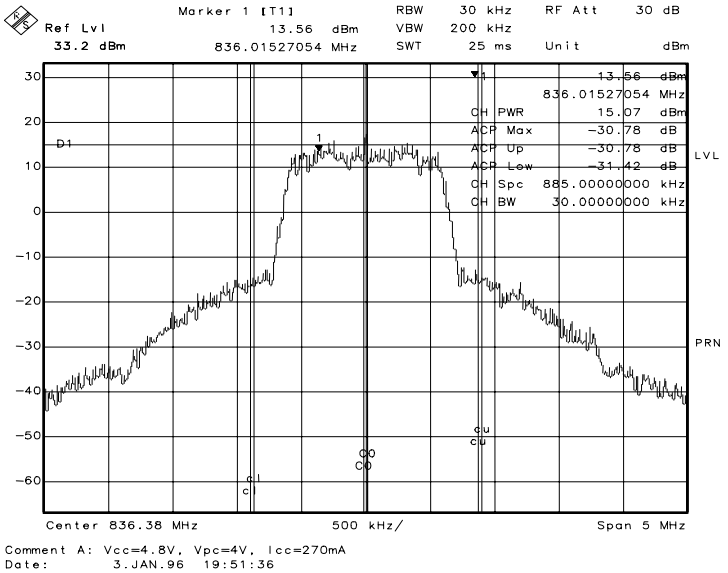


Figure 4. ACP at +27dBm output power and 44% efficiency

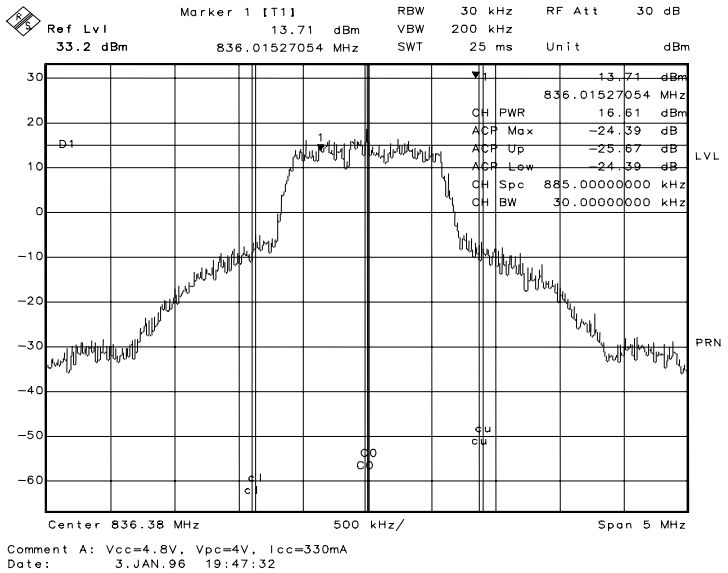


Figure 5. ACP at +29dBm output power and 53% efficiency

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New High Power, High Efficiency HBT GSM Power Amplifier

Abstract
RF Micro Devices introduces a new power amplifier for GSM applications based on revolutionary HBT (Heterojunction Bipolar Transistor) technology. This power amplifier operates from a single 4.8V or 6V power supply without the need for a negative voltage. The power output at 4.8V is 35 dBm, and at 6V the PA provides 36 dBm! The overall efficiency is as high as 62%. On-board power control is included, as is power down. The part is packaged in an industry standard 16-lead SOIC with 4 fused, wide leads.

Introduction

With the maturation of digital cellular systems in Europe, Japan, and North America, next generation handsets must offer advantages to the consumer. These generally take the form of lower cost, smaller size, and longer battery life.

One component which has traditionally been either expensive, large, power-hungry, or any combination of these has been the RF power amplifier. This critical component governs much of the battery life, size, ease of implementation, and manufacturability of the phone. For 5-cell applications between 5.3V and 6.0V, this function can now be performed using HBT (Heterojunction Bipolar Transistor) technology from RF Micro Devices. The new RF2123 GSM power amplifier provides all of these advantages to the handset designer, amplifying a +6 dBm input signal to over +35 dBm output, at up to 60% efficiency. Moreover, no negative voltage is required, either internal or externally generated. Additionally, an on-board analog gain control provides greater than 60 dB of power control from 1V to 4V control voltage. When the control is reduced to <0.5V, the part is shut off, drawing less than 1mA.

Key Advantages of HBT Power Amplifier Technology

The HBT Power Amplifier drives several key features of the phone operation and design. Some are advantages to the end customer, such as talk time and overall phone size. Others are related to the ease of design and manufacturing the phone, such as single voltage supply, on-board power-down, and on-board power control. These advantages are discussed below:

- Talk time. The current consumption of the transmitter is dominated by the power amplifier. For battery operated applications, the power-added (or total) efficiency is extremely important. Sixty percent total efficiency for a two-stage, 30dB gain GSM power amplifier IC is ideal for maximizing talk time – a key performance advantage at the competitive system level.
- Small Package Size. As cellular phone sizes shrink, the available real estate for RF components shrinks as well. Traditional power amplifier designs become difficult to implement in the required area; thus the SOIC packaged, integrated amplifier approach is extremely beneficial. The RF2123 takes the place of a large discrete implementation, or a MESFET IC implementation with additional components such as a negative voltage generator and a supply-side switch. The unique “Quad BatWing” package pioneered by RF Micro Devices allows superior heat-sinking and electrical grounding. This allows over 4-W of output power to be transmitted in GSM mode with no special heat slug or non-standard packaging.
- No Negative Voltage. HBT is a unique technology, allowing performance better than GaAs MESFETs, yet allowing biasing similar to Silicon Bipolar from a single positive voltage. This eliminates one of the primary disadvantages with GaAs MESFETs – the requirement for a negative voltage. For a system de-signer to implement negative voltage with sufficient current to drive a MESFET gate, some kind of switching regulator or “charge pump” must be used. This can be expensive and cumbersome. If the charge pump is implemented on-chip, excessive low-frequency noise, additional leakage current, and additional external components minimize the benefit.
- HBT provides an elegant solution to the high-efficiency power amplifier. With no need for additional components, the part provides an overall smaller, more efficient, and lower cost solution.
- No supply-side switch. The RF2123 HBT Power Amplifier provides a single pin for power down. This function powers down the part with less than 0.5V on the control pin, and provides full power with 4V on the control. In power-down mode, less than 1mA of total current is consumed, allowing very long stand-by times for the phone.
- To utilize a GaAs MESFET power amplifier, the system designer must insert a switch into the bias sup-

ply line to the part for shutdown. The gate cannot be used to switch the MESFET on and off due to the high gate-source capacitance. On-board charge pumps must consume milliamps of current during power-down. This supply-side switch must be capable of supporting very high currents, and tends to be very ex-pensive as a result. A MOSFET switch will cost on the order of $0.50 to $0.75, which is a substantial portion of the overall power amplifier cost. The loss through the switch also reduces the voltage available on the drain of the MESFET PA, thus requiring more current to achieve the same output power.

- Gain Control. Using the same pin as is used for power down, the gain is controlled over 60dB with a 1V to 4V control range. A typical power control characteristic is shown in Fig. 1.
- High Reliability. At RF Micro Devices, we have logged over 1.5 million device hours under RF stress accelerated lifetest since 1993. Junction temperatures of 250°C are used to accelerate the test. In addition, TRW has been running accelerated DC lifetest, which correlate with RF stress results. The reliability is much improved over the initial HBT technologies available 8-10 years ago. Today, over 40 million hours MTBF at 125°C junction temperatures is achieved.

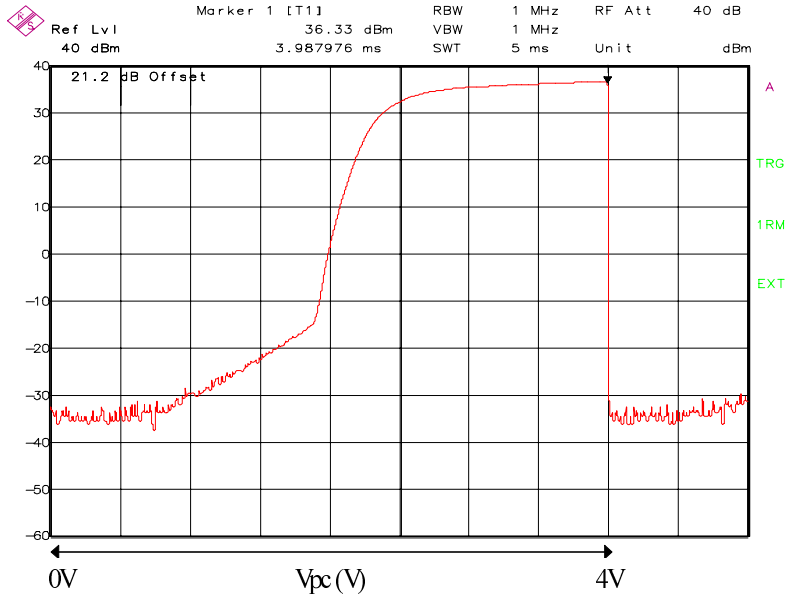


Figure 1. Output power vs. Vpc from 0 to 4V. Note that the power control range is >60dB with the maximum output power at 36.3dBm.

HBT Technology

The RF2123 is one of a family of power amplifiers from RF Micro Devices based upon HBT technology for both linear and constant-envelope applications. This technology, provided by TRW, is a proven technology originally developed for military and space applications. Based upon a Gallium Arsenide/Aluminum Gallium Arsenide (GaAs/AlGaAs) heterostructure, the power and efficiency performance is the highest of any commercially available integrated solution. Being a bipolar structure, the part can operate from a single positive voltage supply without adding components – extremely important in a battery operated system such as a cellular phone.

The critical geometries in an HBT transistor are vertical structures, not lateral. The emitter, base, and collector are stacked vertically by semiconductor layer growth, using MBE (Molecular Beam Epitaxy). This is a very accurate and repeatable growth process. Since each layer is placed over the entire wafer at once, no photolithography is required for this process; thus, mask

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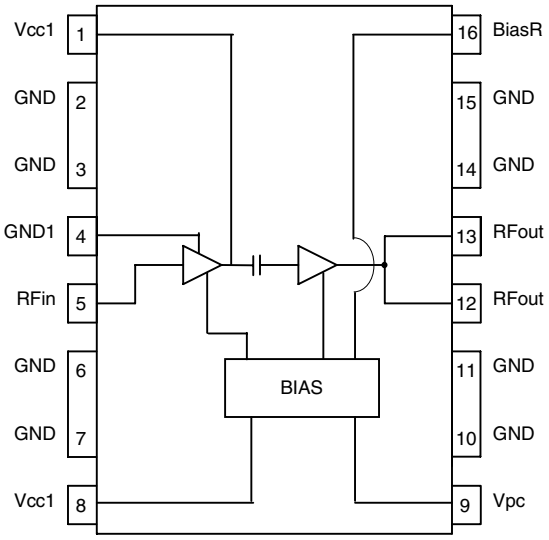


Figure 2. Block Diagram and Pinout for RF2123.

alignment and optical resolution is not an issue. Also, this means wafers can be prepared and stock-piled, eliminating this step from the critical path of product manufacturing.

Once the layers are completed, then the lithography begins. Since all the critical geometries are already defined, the minimum feature size is currently 2mm. This is much more manufacturable than the 0.5-1.0mm gate geometries typically required by GaAs MESFETs.

We feel the TRW HBT process is the most reliable commercially available HBT process in the world. As a military subcontractor, TRW has qualified the process for many of their military programs. Additionally, as a space equipment manufacturer, the HBT process has been qualified for Class S space applications. This level of ruggedness is absolutely needed for spacecraft, since it is somewhat difficult to repair a failed component in space, but is also demanded by the commercial marketplace today. RF Micro Devices and TRW have both been diligently testing the HBT process and products to determine the ruggedness and failure rates. The MTBF is currently defined to be 4x107 hours at a junction temperature of 125°C. Additional information is available on the reliability of HBTs, and may be obtained with the application information package on the RF2123.

In order to meet the continuing demand for GaAs HBT, RF Micro Devices has licensed the proprietary TRW HBT process for commercial wireless applications and is building a high-volume wafer fab in Greensboro, NC to provide the industry with these power amplifiers and other high-performance ICs. This wafer fab will be the largest GaAs HBT wafer fab in the world, and will continue to enforce our dominant position as the leading supplier of GaAs HBT circuits.

RF2123 Theory of Operation and Application Information

The block diagram for the RF2123 is shown in Figure 2. The part is a two-stage device with 30 dB gain at full power. The drive level required to fully saturate the output is +6 dBm. Bias control is provided through a single pin interface, and the final stage ground is achieved through the large pins on both sides of the package. First stage ground is brought out through a separate ground pin for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane. The output is brought out through the 2 output pins, and combined off-chip to form the output line.

The amplifier operates in Class AB bias mode. The final stage is “deep AB”, meaning the quiescent current is extremely low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 1A. The optimum load for the output stage is ~3.5W. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, leads, and microstrip, and two shunt capacitors external to the part. With this match, a 50W terminal impedance is

achieved. The input is matched to 50W with just a blocking capacitor needed. The input is DC coupled; thus, a blocking cap must be inserted in series.

Vcc1 provides supply voltage to the first stage, as well as provides some control over the operating band. Essentially, the bias is fed to this pin through a short transmission line. A tuning capacitor external to Pin 1 sets the frequency of the gain peak. A resistor in parallel with the bias choke for the first stage helps to stabilize and dequeue the circuit.

The RFout pins provide the output power. Pins 12 and 13 should be combined externally. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the 1-1.5A of current required.

The HBT breakdown voltage is >20V, so nominally at 6V there should be no issue with overvoltage. Under extreme conditions, however, which can occur in a cellular handset environment, the supply voltage could be as high as 8.5 to 9.5V. These conditions may correspond to operation in a battery charger, especially with the battery removed, which “unloads” the supply circuit. To add to this worst-case scenario, the RF drive may be at full power during transmit, and the output VSWR could be extremely high, corresponding to a broken or removed antenna. Under all of the above conditions, the peak RF voltages could well exceed 2X the supply voltage, forcing the device into breakdown. The RF2123 includes overvoltage protection diodes at the output, which begin clipping the waveform peaks at ~15V. This protects the device’s output from breaking down under these worst-case conditions, and provides a rugged, robust component for the system designer.

High current conditions are also potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2123 includes reference diodes in the bias circuit to temperature compensate the RF transistors, thus limiting the current through the bias network and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations, and the part is remarkably consistent over the full -30 to +85°C commercial temperature range.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in the following table were taken with a 12.5% duty cycle and a 600ms pulse.

RF2123 Performance

The RF2123 performance is summarized in Table 1 below. A full data sheet is available from RF Micro Devices.

Parameter	Typical Performance	Conditions
Frequency Range	890-915 MHz	
Maximum CW Output Power	4-W	With specified load at 6V
Total CW Efficiency	55%	at Max Output
Gain at Max Power	30 dB	
Gain Control Range	45 dB, min	
Vpc Current	1 mA, max	
“OFF” Current	10 uA, max	Vpc < 0.2V
Voltage Range	5.3 to 6V	
Stability	Spurious <-60dBm	Output VSWR < 8:1
Temperature Range	-30 to +85 C	Operating

Table 1. RF2123 Performance Summary

Conclusion

The RF2123 HBT GSM Cellular Power Amplifier has been introduced by RF Micro Devices. This amplifier provides the best overall performance of any integrated PA on the commercial market. Operating from a single positive supply, efficiencies of 55% and power levels of 4-W are achievable from a single 16-lead SOIC surface mount package at 6V. Power down and power control are integrated on-chip without additional components required. The new power amplifier can be used to simplify cellular phone design and improve operation, as well as significantly reducing overall cost.

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New High Efficiency HBT Analog Cellular Power Amplifier

Abstract
RF Micro Devices introduces a new power amplifier for Analog Cellular applications based on revolutionary HBT (Heterojunction Bipolar Transistor) technology. This power amplifier operates from a single 4.8V power supply without the need for a negative voltage. The power output from 824MHz to 849MHz is 1.2W with 420mA current – a total efficiency of 60%! On-board gain control is included, as is power down. The part is packaged in an industry standard 16-lead SOIC with a fused center lead. Pricing is competitive at less than $5 in volume.

Introduction

With the introduction of digital cellular systems in North America and Europe, analog phone manufacturers are becoming more competitive. Differentiating factors such as talk time, stand-by time, size, and especially cost are driving new analog phone development. In this type of environment, the components used in these phones must offer unprecedented performance/cost advantages. One component which has traditionally been either expensive, large, power-hungry, or any combination of these has been the RF power amplifier. This critical component governs much of the battery life, size, ease of implementation, and manufacturability of the phone. For 4-cell applications operating between 4.0V and 4.8V this function can now be performed using HBT (Heterojunction Bipolar Transistor) technology from RF Micro Devices. The RF2131 AMPS/ETACS Power Amplifier can amplify a +6dBm input signal to +30.8dBm output, drawing only 420mA from a single positive supply. Additionally, an on-board analog gain control provides greater than 30dB of power control from 2V to 3.6V control voltage. When the control is reduced to 0V, the part is shut off, drawing less than 10mA.

Key Advantages of HBT Power Amplifier Technology

The RF2131 drives several key features of the phone operation and design. Some are advantages to the end customer, such as talk time and overall phone size. Others are related to the ease of design and manufacturing the phone, such as single voltage supply, on-board power-down, and on-board power control. These advantages are discussed below:

- Talk time. The current consumption of the transmitter is dominated by the power amplifier. For battery operated applications, the power-added (or total) efficiency is extremely important. Sixty percent total efficiency for a two-stage, 25dB gain AMPS/ETACS power amplifier IC is ideal for maximizing talk time – a key performance advantage at the competitive system level.
- Small Package Size. As cellular phone sizes shrink, the available real estate for RF components shrinks as well. Traditional power amplifier designs become difficult to implement in the required area; thus the SOIC packaged, integrated amplifier approach is extremely beneficial. The RF2131 takes the place of a large discrete implementation, or a MESFET IC implementation with additional components such as a negative voltage generator and a supply-side switch.
- No Negative Voltage. HBT is a unique technology, allowing performance better than GaAs MESFETs, yet allowing biasing similar to Silicon Bipolar from a single positive voltage. This eliminates one of the primary disadvantages with GaAs MESFETs – the requirement for a negative voltage. For a system de-signer to implement negative voltage with sufficient current to drive a MESFET gate, some kind of switching regulator or “charge pump” must be used. This can be expensive and cumbersome. If the charge pump is implemented on-chip, excessive low-frequency noise, additional current, and additional external components minimize the benefit. HBT provides an elegant solution to the high-efficiency power amplifier. With no need for additional components, the part provides an overall smaller, more efficient, and lower cost solution.
- No supply-side switch. HBT Power Amplifiers from RFMD provide a single pin for power down. This function powers down the part with 0V on the control pin, and provides full power with ~3.6V on the control while drawing less than 1mA from a controller. In power-down mode, less than 1mA of total current is consumed, allowing very long stand-by times for the phone. To utilize a GaAs MESFET power amplifier, the system designer must insert a switch into the bias supply line to the part for shutdown. The gate cannot be used to switch the MESFET on and off due to the high gate-source capacitance. This switch must be capable of supporting very high currents, and tends to be very expensive as a result. A MOSFET switch will cost

on the order of $0.50 to $0.75, which is a substantial portion of the overall power amplifier cost. The loss through the switch also reduces the voltage available on the drain of the MESFET PA, thus requiring more current to achieve the same output power.

- Gain Control. Using the same pin as is used for power down, the gain is controlled over 30dB with a 2V to 3.6V control range. This pin offers less than 1mA current consumption, even under full drive. With very deep Class AB bias on the final stage, the current decreases rapidly with lower power, making the RF2131 very efficient even at reduced powers.
- Low Noise-Power Output. A key parameter related to the power amplifier is the noise power output in a 30kHz bandwidth. This defines the required rejection in the receive band (869MHz to 894MHz) for the duplexer, since for a full-duplex system like AMPS the transmitter will tend to "self-jam" the receiver. The noise transmitted by the power amplifier is related to it's noise figure and gain in the receive band. The RF2131 operates with better than -90dBm/30kHz in the receive band as shown in Figure 1.

HBT Technology

The RF2131 is one of a family of power amplifiers from RF Micro Devices based upon HBT technology for both linear and constant-envelope applications. This technology, provided by TRW, is a proven technology originally developed for military and space applications. Based upon a Gallium Arsenide/Aluminum Gallium Arsenide (GaAs/AlGaAs) heterostructure, the power and efficiency performance is the highest of any commercially available integrated solution. Being a bipolar structure, the part can operate from a single positive voltage supply without adding components – extremely important in a battery operated system such as a cellular phone.

The critical geometries in an HBT transistor are vertical structures, not lateral. The emitter, base, and collector are stacked vertically by semiconductor layer growth, using MBE (Molecular Beam Epitaxy). This is a very accurate and repeatable growth process. Since each layer is placed over the entire wafer at once, no photolithography is required for this process; thus, mask alignment and optical resolution is not an issue. Also, this means wafers can be prepared and stockpiled, eliminating this step from the critical path of product manufacturing.

Once the layers are completed, then the lithography begins. Since all the critical geometries are already defined, the minimum feature size is currently 2mm. This is much more manufacturable than the 0.5mm to 1.0mm gate geometries typically required by GaAs MESFETs.

We feel the TRW HBT process is the most reliable commercially available HBT process in the world. As a military subcontractor, TRW has qualified the process for many of their military programs. Additionally, as a

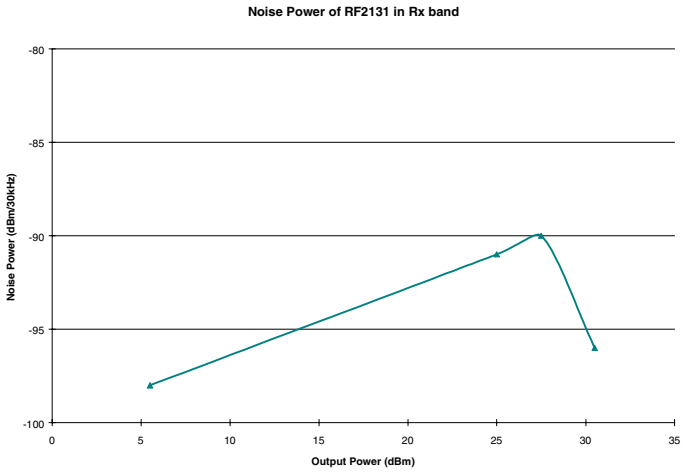


Figure 1. Noise Power of RF2131 in Rx Band

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space equipment manufacturer, the HBT process has been qualified for Class S space applications. This level of ruggedness is absolutely needed for spacecraft, since it is somewhat difficult to repair a failed component in space, but is also demanded by the commercial marketplace today. RF Micro Devices and TRW have both been diligently testing the HBT process and products to determine the ruggedness and failure rates. The MTBF is currently defined to be 107 hours at a junction temperature of 125°C. Additional information is available on the reliability of HBTs, and may be obtained with the application information package on the RF2131.

RF2131 Theory of Operation and Application Information

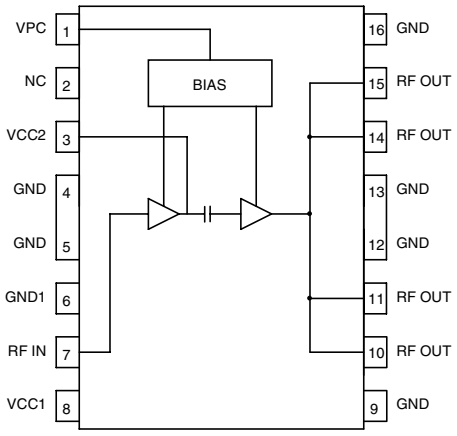


Figure 2. Block Diagram and Pinout for RF2131.

The block diagram for the RF2131 is shown in Figure 2. The part is a two-stage device with 25dB gain at full power. Therefore, for +31dBm output power, the drive required to fully saturate the output is +6dBm. Bias control is provided through a single pin interface, and the final stage ground is achieved through the large pins on both sides of the package. First stage ground is brought out through a separate ground pin for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane. The output is brought out through the 4 output pins, and combined off-chip to form the output line.

The amplifier operates in Class AB bias mode. The final stage is "deep AB", meaning the quiescent current is extremely low, around 40mA. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 360mA.

The optimum load for the output stage is ~10Ω. This is the load at the output collector, and is created by the series inductance formed by the output bond wires, leads, and microstrip, and a shunt capacitor external to the part. With this match, a 50Ω terminal impedance is achieved. The input is matched to 50Ω with just a blocking capacitor needed. For AMPS, the match is slightly different than for ETACS; however, in any case the optimum load for 1.2W is the same at the device.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on the input pin to V_{PC} and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

V_{CC2} provides supply voltage to the first stage, as well as provides some control over the operating band. Essentially, the bias is fed to this pin through a short transmission line. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. For ETACS, the capacitor placement is slightly different than for AMPS. This supply should be bypassed individually before being combined with V_{CC} for the output stage to prevent feedback and oscillations.

The RFout pins provide the output power. Pins 10 and 11 should be combined externally with Pins 14 and 15 with a symmetric combiner. Care should be taken to ensure that the output paths are symmetric up to the point of combining. This prevents "odd-mode" cancellation from occurring wherein one side tries to get out-of-phase with the other, which affects efficiency and stability. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the 400mA of current required.

The part will operate over a 4.0V to 4.8V range. If the full power is desired at minimum voltage, then the load can be optimized at that point. At that point, the specified efficiency and power is attainable. As the voltage is increased, however, the output power will increase. Thus, in a phone design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This will occur at a less-than-optimum efficiency, since the load is optimized for 4.0V. This is true of any power amplifier, however, the important point to note is that the RF2131 can be set up to provide the specified power at 4.0V if desired.

The HBT breakdown voltage is >20V, so nominally at 4.8V there should be no issue with overvoltage. Under

extreme conditions, however, which can occur in a cellular handset environment, the supply voltage could be as high as 8.5V to 9.5V. These conditions may correspond to operation in a battery charger, especially with the battery removed, which "unloads" the supply circuit. To add to this worst-case scenario, the RF drive may be at full power during transmit, and the output VSWR could be extremely high, corresponding to a broken or removed antenna. Under all of the above conditions, the peak RF voltages could well exceed 2X the supply voltage, forcing the device into breakdown. The RF2131 includes overvoltage protection diodes at the output, which begin clipping the waveform peaks at ~15V. This protects the device's output from breaking down under these worst-case conditions, and provides a rugged, robust component for the system designer.

High current conditions are also potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2131 includes reference diodes in the bias circuit to temperature compensate the RF transistors, thus limiting the current through the bias network and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations, and the part is remarkably consistent over the full -30°C to +85°C commercial temperature range.

RF2131 Performance

The RF2131 performance is summarized in Table 1 below. A full data sheet is available from RF Micro Devices.

A common problem associated with high-efficiency cellular power amplifiers is stability, especially into a duplexer. Since duplexers can be designed with different out-of-band characteristics, a robust cellular power amplifier must operate without oscillation into inductive-coupled as well as capacitive-coupled filters. The RF2131 has been tested into various types of duplexers without oscillating.

The minimum output power is achieved with the power control set between 0V up to ~2V, then the power increases approximately linearly as V_{PC} increases from 2V to 3.6V. The characteristic has been designed to function with a low sensitivity of output power to control voltage. If the sensitivity of the gain control is too high, the ALC loop in the phone may oscillate.

Conclusion

The RF2131 HBT Analog Cellular Power Amplifier has been introduced by RF Micro Devices. This amplifier provides the best overall performance of any integrated PA on the commercial market. Operating from a single positive supply, efficiencies of 60% and power levels of 1.2W are achievable from a single 16-lead SOIC surface mount package from 4.0V to 4.8V. Power down and power control are integrated on-chip without additional components required. The new power amplifier can be used to simplify cellular phone design and improve operation, as well as significantly reducing overall cost. The price of the RF2131 in volume is less than $5.

Parameter	Typical Performance	Conditions
Frequency Range	800-950 MHz	Externally tuned for individual bands
Maximum CW Output Power	1.25-W	With specified load at 4.8V
Total CW Efficiency	60%	At Max Output
Gain at Max Power	25 dB	
Noise Power Output	-90 dBm/30kHz, max	in Receive Band, any power setting
Gain Control Range	30 dB, min	
Vpc Current	1 mA, max	
"OFF" Current	10 uA, max	Vpc < 0.2V
Voltage Range	4.0 to 4.8V	
Stability	Unconditional	
Temperature Range	-30 to +85?C	Operating

Table 1: RF2131 Typical Performance

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High Efficiency HBT Low Voltage Programmable Gain Power Amp

Abstract
RF Micro Devices introduces a new power amplifier with digital gain control for low voltage applications. The power amplifier operates up to 1GHz and delivers 0.5W at 3.6V with an efficiency near 60%. The digital gain control provides 4 gain settings in 8dB steps. This device uses HBT (Heterojunction Bipolar Transistor) technology and a low cost plastic package. This power amplifier is suited for low cost applications, such as the final output stage for a 900MHz ISM band handset or as a driver for 400MHz mobile phones. The device operates from a single 3.6V power supply without the need for a negative voltage. The power output from 900MHz to 930MHz is 0.45W with 220mA of current – a total efficiency of 57%! In addition to the on-board gain control, the device draws less than 10µA of supply current when in the power down mode without the need for a supply side switch. The part is packaged in an industry standard 16-lead SOIC with a fused center lead. Pricing is competitive at less than $3 in volume.

Introduction
Cordless phone manufacturers are under intense pressure to reduce the cost of their handsets, while improving performance. Phone designs that operate with a low voltage and offer a high degree of integration will succeed in this market. Spread spectrum handsets operating in the Industrial-Scientific Medical (ISM) band offer a clear advantage over their VHF predecessors. The users of spread spectrum handsets are less likely to experience line interference compared with the 45MHz handsets. Electronic noise from appliances, computers and other electronic devices, along with typically poor range is characteristic of the old 45MHz cordless phones. If adequate power is delivered to the antenna, these problems do not exist in the 900MHz spread spectrum phones. As much as 1-W of transmitted power is allowed by the Federal Communications Commission in this band. However, battery life and talk time are reduced as the output power is increased. Cordless phone manufacturers have generally kept their output power levels around 250-mW in order to get the best tradeoff of talk time versus handset range. Cordless phones also implement a gain control function to maximize talk time.

Ideally suited for this 900MHz application is the RF2155, the newest member of a family of HBT high efficiency power amplifiers offered by RF Micro Devices. This integrated PA is also well suited for lower frequency applications, such as a driver amplifier for 400MHz mobile phones. The RF2155 offers digital gain control, high-efficiency, 0.45W output power, operation from a single 3 V supply, and low cost. This Low Voltage Programmable Gain PA amplifies a 0 dBm input signal to 26.5dBm of output power, drawing less than 220mA of current from a single 3.6 V supply. The IC implements a 2-bit digital gain control that gives 4 gain settings in approximately 8dB increments. When the power down pin is reduced to 0V, the PA draws less than 10mA of supply current, without the need for a costly supply side switch. The RF2155 is packaged in a standard 16-lead SOIC with fused center leads. In addition to the high-efficiency, the HBT technology doesn't require a negative supply that is typically needed for a MESFET PA. This integrated power amplifier greatly reduces the component count, overall size, performance variations that are typical of discrete power amplifiers, and most importantly, it reduces the overall cost.

Another application for this IC is as a driver for 400MHz mobile phones.

RFMD Harnesses HBT Technology
The RF2155 is one of a family of power amplifiers from RF Micro Devices based upon HBT technology for both linear and constant-envelope applications. Specifically, the RF2155 is similar to the RF2115 1.0W Programmable gain PA which is currently shipped in high volumes for 6V cellular phone applications. The HBT technology, provided by TRW, is a proven technology originally developed for military and space applications. Based upon a Gallium Arsenide/Aluminum Gallium Arsenide (GaAs/AlGaAs) heterostructures, HBT offers power and efficiency performance that is the highest of any commercially available integrated solution. By coupling this technology with proven power amplifier designs, low cost packaging, and cost-effective test, RF Micro Devices offers this performance at prices that can't be matched in the industry.

HBTs, being bipolar devices, have many advantages. They operate from a single positive voltage supply without adding components – extremely important in a small battery operated system such as a cordless phone. Also, the critical geometries in an HBT transistor are vertical structures, not lateral. The emitter, base, and collector are stacked vertically by semiconductor layer growth, using MBE (Molecular Beam Epit-

axy). This is a very accurate and repeatable growth process. Since each layer is placed over the entire wafer at once, no photolithography is required for this process; thus, mask alignment and optical resolution is not an issue. Also, this means wafers can be prepared and stock-piled, eliminating this step from the critical path of product manufacturing.

Photolithography only begins after the layer growth is completed. Since all the critical geometries are already defined, the minimum feature size is 2µm. This is much more manufacturable than the 0.25µm to 1.0µm gate geometries typically required by GaAs MESFETs.

We feel the TRW HBT process is the most reliable commercially available HBT process in the world. As a military subcontractor, TRW has qualified the process for many of their military programs. Additionally, as a space equipment manufacturer, the HBT press has been qualified for Class S space applications. RF Micro Devices and TRW have both thoroughly tested the HBT process and products to determine the ruggedness and failure rates. Based on these measured failure rates, Figure 1 shows the predicted MTBF for the RF2155 as a function of ambient temperature. At an ambient temperature of 85°C, the MTBF is greater than 10^7 hours. This data assumes a maximum junction temperature of 135°C under the full output power condition.

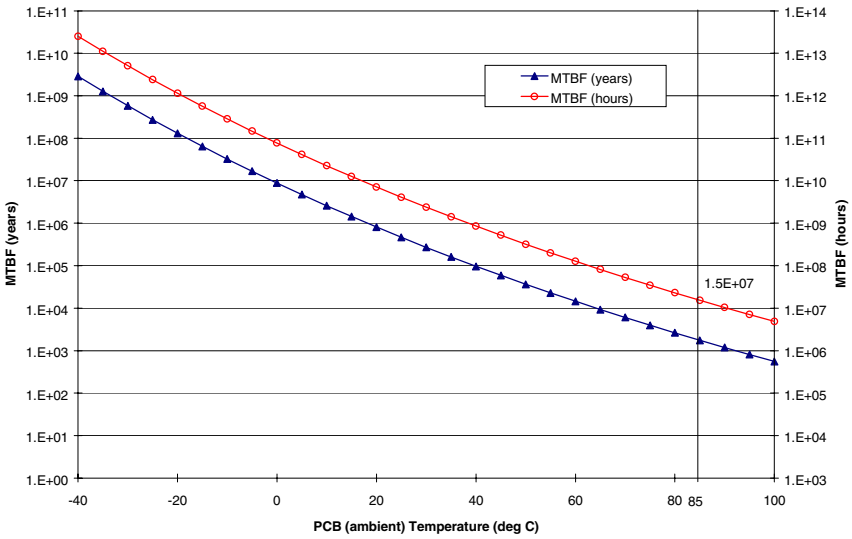


Figure 1. RF2155 MTFB as a Function of Temperature

RF2155 Theory of Operation and Application Information

The block diagram for the RF2155 is shown in Figure 2. The IC is a two-stage programmable gain power amplifier with over 30 dB of small-signal gain that operates between 3V and 5.5V. With an input drive level of 0dBm, the PA delivers up to 27dBm with an efficiency near 60% for a 3.6V supply. A power down feature is implemented with a single pin interface (pin 8), when this pin is grounded, the PA draws less than 10µA. When the voltage on the power down pin (VPD) is increased to a nominal value of 3.0V, the PA is turned on. This pin draws about 3mA of current when set to 3V. Pin 3 is connected to the battery voltage and is used to supply base current to the RF transistors.

The output stage ground is achieved through the large pins on both sides of the SOIC. Ground for the first stage is returned through a separate ground pin (pin 6) to isolate it from the output ground. These pins should be connected directly with vias to the PCB ground plane. The output is brought to two pins: pin 11, which is used for the output signal and pin 14, which is used to feed in the final stage bias.

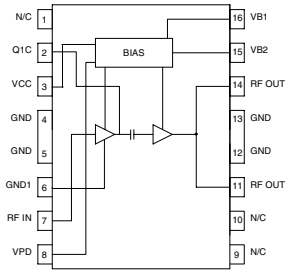


Figure 2. Block Diagram and Pinout for RF2155

The amplifier operates in Class AB mode. When both gain control bits (pins 15 and 16) are logic high (full gain), the IC draws about 70mA of quiescent current. When an RF signal is applied to the input, the output stage self-biases, and draws about 190mA of DC current. Digital control bits, VB1 and VB2 switch degeneration resistors into the common-emitter amplifier, thus reducing the gain of the power amplifier. In addition, when the high order bit, VB1, is set to logic low, the quiescent bias current of the entire PA reduces to about 15mA. This ensures that the current consumption in the lowest gain settings is minimized. For instance, with both gain bits set low, the PA delivers about +3dBm of power and consumes less than 25mA of DC current.The gain control bits operate with a minimum logic high level of 2.5V and a maximum low level of 0.8V. The current draw of the control bits are less than 300µA each for a 2.8V level. A truth table showing out-put power versus bit settings for the 4 available gain settings is shown below:

VB1	VB2	Pout (dBm) (Pin = 0dBm)
1	1	+26.5
1	0	+18.5 ± 3
0	1	+10.5 ± 4
0	0	+1.5 ± 4

Pin 2 is the supply voltage for the first stage. The inductance between this pin and the bypass capacitor sets the frequency of the small-signal gain peak. A short microstrip line between the pin and bypass capacitor conveniently realizes this inductance. Moving this capacitor away from the device shifts the gain peak to a lower frequency.

The input is DC coupled and requires a blocking capacitor. A series inductor can be added to the input to improve the VSWR. Under all 4 gain settings, the input VSWR is better than 2.5:1 with an 8.2nH series inductor on the input.

The RF2155 is designed to operate at a nominal voltage of 3.6V, however the PA will operate with degraded power down to 3.0V. The high HBT breakdown voltages ensure damage free operation up to a maximum supply voltage of 5.5V.

RF2155 Performance

The RF2155 performance is summarized in the following table.A full data sheet is available from RF Micro Devices.

Parameter	Typical Performance	Conditions
Frequency Range	430-950 MHz	Externally tuned for individual bands
Output Power Levels and Supply Currents:		With a 9 ohm load impedance.
Bit1=2.7V; Bit2=2.7V	26.8 dBm / 225 mA	
Bit1=2.7V; Bit2=0V	21.2 dBm / 123 mA	
Bit1=0V; Bit2=2.7V	14.2 dBm / 58 mA	
Bit1=0V; Bit2=0V	4.7 dBm / 23 mA	
Output Power Variation over Temperature; -20 C to +85 C	+/- 0.2 dB	Bit1=2.7V; Bit2=2.7V
Total CW Efficiency	57 %	at Max Output Level
Gain at Max Power	26.5 dB	Bit1=2.7V; Bit2=2.7V
Vpc Current	4 mA, max	
"OFF" Current	10µA, max	Vpc < 0.2V
Voltage Range	3.0 to 5.5V	
Stability	Unconditional	
Temperature Range	-30 to +85°C	Operating

The performance of the RF2155 has been characterized at the 900MHz ISM band on a low-cost, 30mil FR-4 printed circuit board. The application schematic and layout drawing for the PA are included in Figures 3 and 4, respectively. Notice the output match is achieved with a microstrip transmission line and a single shunt capacitor. Bias to the output stage is fed through a microstrip transmission line, this line is less than ¼ wavelength and thus also provides part of the output impedance match and harmonic termination. To reduce PCB area, the microstrip transmission line from pin 11 to the matching capacitor C10 can be realized by a shorter and narrower line. For instance, the inductance of this line is approximately 4 nH and can be realized with a 20mil wide by 310mil long transmission line or by a lumped inductor. The width of the output transmission line between the PA and capacitor C10 was chosen for this evaluation board to give a 50Ω impedance, making it simple to tune the output match. This width preserves the 50Ω load impedance up to the point where the output capacitor is placed on the transmission line. By using lumped inductors on the output pins, the area for the entire PA and external components is less than 0.4 square inches. Notice that the two capacitors, C9 and C14, are 1μF tantalum bypass capacitors and can be reduced to a single capacitor in a typical phone application.

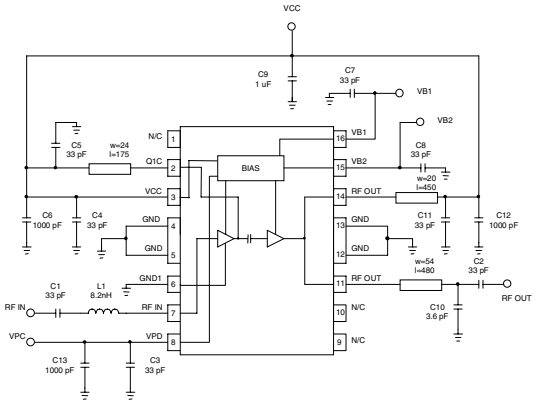


Figure 3. RF2155 Application Schematic; Board Material: FR-4, h=30 mils

Measurement Results

Measured data from the evaluation board described above is presented next. Figure 5 shows the output power and total supply current as input power is varied for the RF2155 operating at 3.6V.

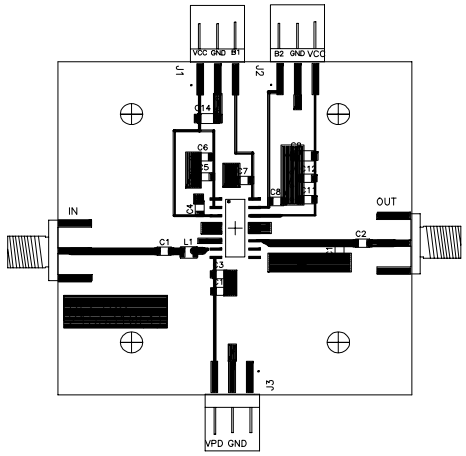


Figure 4. RF2155 Printed Circuit Board; Board Material: FR-4, h=30 mils.

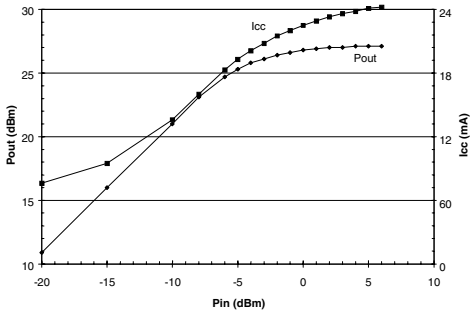


Figure 5. Pout and Icc versus Pin

This data is with the programmable gain bits set to full gain and the power down voltage at 3.0V. Here the saturated power is about 0.5W with an efficiency of 58% for an input level of 0dBm. The 1dB output compression point for the PA is about 25.5dBm. The output power reaches 1.0W when the supply voltage is increased to 5.5 V as shown in Figure 6Notice that the total efficiency of the PA is greater than 56% over the entire supply range of 3.0V to 5.5V. The efficiency peaks above 58% at the typical voltage for a 2-cell nickel cadmium or nickel metal hydride battery.

An important feature of this power amplifier is the programmable gain. Programmable gain provides increased talk time, since it allows the power delivered to the antenna to be reduced when the handset is close to the base station. The digital control implemented in the RF2155 simply requires 2 digital control

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bits to provide the 4 gain settings. The output power for the RF2155 under the 4 gain settings across the 900MHz ISM band is shown in Figure 7.The variation in output power across the ISM band is about 0.1dB in the full gain setting. In the lowest gain setting the output power variation across this band is about 1.5dB.

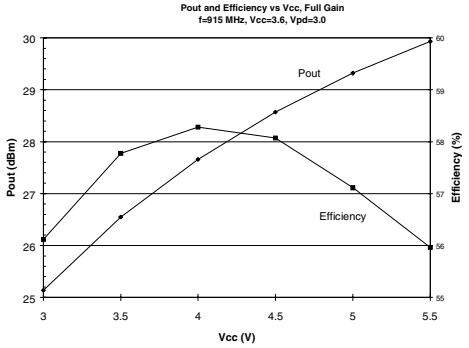


Figure 6. Pout and Efficiency versus Vcc

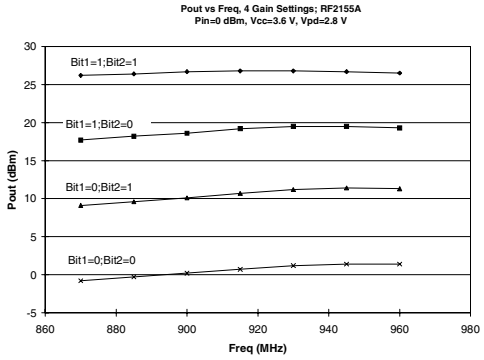


Figure 7: RF2155 Output power in the ISM 900 band, 4 gain settings

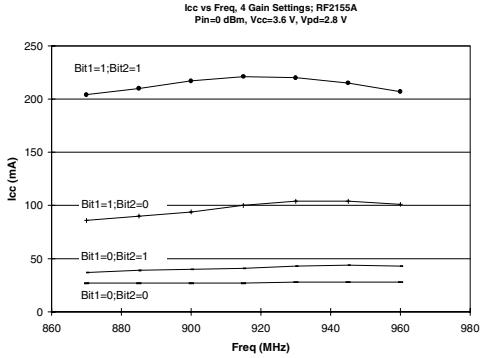


Figure 8: Total current of the RF2155 in the ISM 900 band for the 4 gain settings

Class AB bias not only gives a better efficiency at a saturated output level, but it also enhances the efficiency at lower output levels. To further improve efficiency at the lower gain settings, the high-order bit, VB1, is used to reduce the quiescent bias current below 20 mA when the bit is set low. Current for the 4 gain settings is shown in Figure 8 There is about a 10 fold reduction in supply current across the gain control range. With +5 dBm output power, the PA draws less than 25 mA.

Conclusion

The RF2155 HBT Programmable Gain Power Amplifier is introduced by RF Micro Devices. With a 0 dBm input level, this IC amplifier delivers up to 0.5W and has an efficiency near 60% while operating from a single supply from 3.0 to 5.5V. Additionally, the PA offers a convenient 2-bit digital gain control function, giving 4 levels of power control, in 8dB steps. This IC draws less than 25mA when in the lowest gain setting, thus significantly increasing talk time. The RF2155 has applications in any analog communications systems that require a high-efficiency, low-voltage, and low-cost PA. Specifically this IC was designed for 900MHz cordless phones and 400MHz industrial radios, where the digital gain control PA will increase battery life, simplify the transmitter design, reduce overall component count, and reduce cost. Using discrete matching components, the size required for this PA is less than 0.4 square inches. The price of the RF2155 in volume is less than $3.

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High Linearity HBT Amplifiers for CATV Systems

Abstract
Monolithic Amplifiers using GaAs HBT technology have been developed. HBT based amplifiers offer extremely flat frequency response with high dynamic range and use less DC power than Silicon or GaAs MESFET based circuits. These inexpensive amplifiers are packaged in a standard SOIC plastic packages and feature very flat frequency response to beyond 1GHz with OIP_3 numbers in excess of +40dBm. They are capable of amplifying multicarrier CATV signals with very high fidelity.

Introduction
The need for high linearity amplifiers arises from stress placed on communications channels by the addition of more data and the requirement to handle digitally modulated signals with high fidelity. As the amount of data increases and the necessity to reduce spurious interference increases, the channel linearity must be improved over current implementations. A particularly difficult problem is obtaining the linearity and bandwidth needed for the amplification of multicarrier signals such as those found in the TV distribution industry. Cable TV, for example, is expanding rapidly in terms of both the number of channels and additional subscribers. Hence, more bandwidth and power output capacity (without degrading linearity) are necessary. These systems are also incorporating more technology into their systems including two-way channels for voice and data, and digital video modulation. As this additional capacity is added, the bandwidth and signal handling capability of the various links in the distribution chain must be improved. In addition to the need for more capacity, the linearity of the channel must further improve because digital modulation schemes are less tolerant of IM distortion products than the analog systems currently in use. The infrastructure needed to accommodate these technology innovations must be in place throughout the distribution chain before it can become available to the consumer. Hence, there is considerable pressure to improve channel linearity, bandwidth, and power handling capability in the many links of the various distribution channels.

RF Micro Devices is developing a line of high linearity, wide bandwidth products to address these requirements. The first in the series is the RF2312 amplifier which has been released as a standard product by RFMD. Other higher power units are the RF2317 (a higher power version of the RF2312) and the RF2316, which is a balanced device having improved second order distortion over the unbalanced designs. The latter two devices will be in full production in January, 1997.

The RF2312 and RF2317 are essentially a low cost, traditional Darlington “Gain Block” circuits with the exception that performance far outstrips previously available units. The gain is essentially flat over the bandwidth from 1MHz to well over 1GHz and has an IP3 of over +40dBm. The secret to the performance of the unit (as in all the units mentioned) is in the use of GaAs Heterojunction technology in the fabrication of the device. The unit will replace more expensive and less reliable discrete amplifiers and permit much better distortion levels for a given amount of DC power consumption.

Characteristics of Multicarrier Channels
A multicarrier channel consists of many independent RF carriers each with its own frequency and modulation. It is important that each of these signals remain “uncontaminated” by all of the other signals in the channel. For simplicity, consider that if n CW carriers are present, have the same amplitude, and are coherent with each other, the resulting frequency spectrum is a “picket fence” as shown in figure 1. The time waveform resembles an impulse function as shown in figure 2. (Note that because the frequency spectrum does not start at zero and because some phase distortion is introduced by filters and amplifiers in the chain, the time function is generally not, strictly speaking, an impulse.) The amplitude of the voltage peak is $20\log(n)$dB above the amplitude peak of a single tone. This occurs when all of the signals have a peak amplitude occurring at the same point in time. If, however, each carrier is independent and has a random phase with respect the other carriers, the time waveform is similar to that shown in figure 3 while the frequency spectrum remains the same as in figure 1. In some newer systems, this spectrum can extend from a few MHz to about 1GHz. The result is a noise like signal which has the same average power as in the coherent case, but has much smaller peak excursions. This is an important fact, since the amplifier has to be designed to handle peak excursions in a linear fashion and designing the part for voltage excursions of $20\log(n)$ dB above the single tone amplitude would be very difficult and be an “overkill”.

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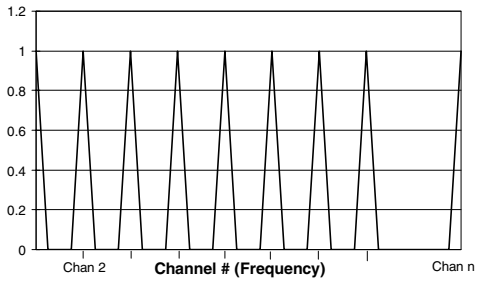


Figure 1. CATV Spectrum

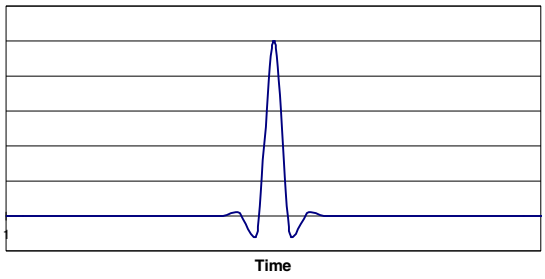


Figure 2. Time waveform of signal with zero phase

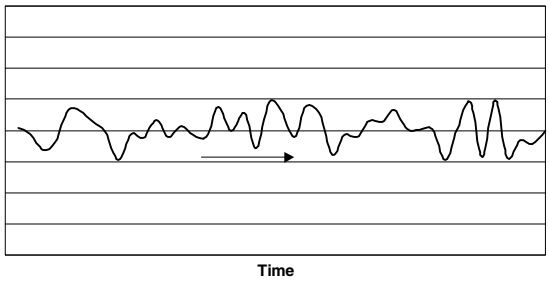


Figure 3. Time waveform with random carrier phases

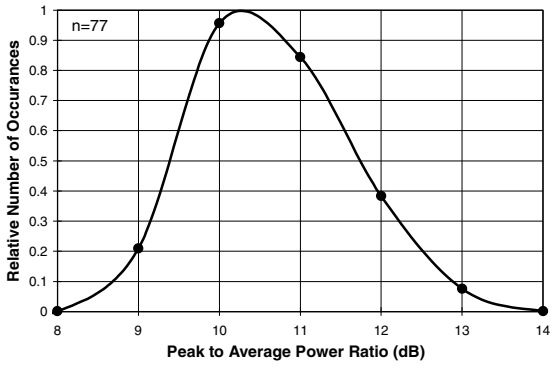


Figure 4. Peak to average power ratio for CATV signal

Because the signal is noise like, the peak excursions of the voltage waveform are a statistical function and therefore the maximum level is indeterminate except to say that it is smaller than A*20 log(*n*), where A is the amplitude of each carrier and *n* is the number of signals. In fact, successive measurements may yield different answers. Because of the nature and quantity of the signals present, however, it is possible to estimate the maximum likely excursion of the waveforms. Many measurements have shown that as the number of signals increase, the actual peak excursion is always reduced markedly from the theoretical maximum given above. The curve of figure 4 shows the probability of measuring a number of peak to average power ratios with a typical CATV composite signal. Note that, in general, 14dB is the practical (but not theoretical) maximum ratio of peak to average power in the composite signal. Therefore, the design of an amplifier which is to handle such a signal must have a linear signal handling ability which is 14dB above the average power and 14+10*Log(*n*)dB power handling ability over the power in a single channel.

As an example, consider a 110 channel system where each carrier is at a level of 50dBmV (0.316V_{RMS}).

Channel Power=$(0.316)^2/75$=1.33mW=+1.24dBm.

Composite Average Power=110*1.33mW=146mW =+21.6dBm

Peak Power if each carrier phase is 0° =+43.8dBm

Expected Nominal Peak Power=10.5+21.6 =+32.1dBm

Maximum Peak Power = 14 + 21.6 = 35.6dBm (3.6W)

Maximum Output Voltage Peak = 16.4V (or 32.8V_{PP})

Therefore, an amplifier designed to handle this signal should have the ability to produce +35.6dBm in a linear fashion - i.e. be able to swing 32.8V_{PP} without clipping.

Causes of Distortion

Four different sources of distortion in an amplifier are listed below. These issues must be addressed either in the design of the amplifier or in the choice of technology used to implement the circuit.

- **Voltage compliance**: As noted above, an amplifier which has to handle 110 signals must be capable of an output peak to peak voltage swing of about 31dB higher than the peak to peak voltage of each carrier signal and 40dB higher than the RMS voltage of

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each carrier signal. So, if the output is set to +35dBmV (the RMS voltage of a single signal is 35dB above 1mV=56.2mV$_{RMS}$), the output swing must be at least 66dBmV which is a 5.64V$_{PP}$ voltage swing (+/- 2.82V). If the amplifier clips during this voltage swing, severe distortion results. In practical circuits, there is an emitter degeneration resistor which raises emitter voltage causing early saturation. It is also necessary to guard band the saturation of the output device since approaching V$_{SAT}$ will cause distortion as well. So the DC V$_{CE}$ (or V$_{DS}$ for FETs) used for the design must be at least 6.5V for this application (or about 3.8V if the collector feed is a choke instead of a resistor). In general, high transistor breakdown voltages are needed for these applications in order to prevent voltage compliance distortion.

- **Drive Current**: Although the exponential I-V characteristic of bipolar devices is thought to make the device nonlinear, experimental results and analysis prove otherwise. The use of emitter degeneration, feedback and ample DC collector current permit the designed to obtain arbitrarily good linearity of G$_M$ (Transconductance). It is necessary to bias the device at a high enough current level to achieve suitably linear operation. In general, devices used in this application have more current drive than would theoretically be necessary to drive the load at the required power level. This excess current is used to provide superior linearity over amplifiers designed for single carrier applications.
- **Distortion due to non linearity of base-collector capacitance**: Because devices used for multicarrier systems are, of necessity, fairly large devices (because of power density), the base-collector capacitance may be larger than other amplifiers of the same power level. Ideally, the transistor's capacitance is constant, and therefore may cause roll off in frequency response, but not contribute distortion. Real world devices, however, exhibit a non linear capacitance vs. voltage curve which contributes significantly to distortion in the output signal, particularly when the voltage swing is quite large.
- **Non linear R$_{out}$ of the transistor**: Non linear loading of the output by the amplifying device itself also causes considerable distortion in the output waveform. Ideally, R$_{out}$ is high and constant. If it is not, the loading of the output changes with signal voltage level, in effect modulating the output signal and causing distortion.

Advantages of HBT

The subject amplifiers are fabricated with a GaAs HBT technology. It is a proven technology which uses a GaAs/AlGaAs heterostructure for producing bipolar devices which have very high f_T, very high Early Voltage, high BV$_{CEO}$ and a capacitance vs. Voltage curve that is nearly flat. This HBT process is the most reliable commercially available HBT process in the world and has been qualified for class S space applications. The level of ruggedness is absolutely needed for space applications, but it is also demanded by commercial applications such as TV distribution systems and cellular base stations which have to be extremely rugged and reliable.

RF Micro Devices has supplied high volumes of Power Amplifiers utilizing this process with excellent results. The HBT process and products built with this process have been tested to determine that failure rates are at least 10^7 hours at 125 degrees C.

The main reason that this technology was selected for this product was that it provides superior linearity and bandwidth compared to other technology choices. The desired performance requires amplifying devices which have a very high transition frequency (f_T). The minimum f_T is about 15GHz and 20GHz or more is desirable in order to obtain a really flat response with good return loss through 1GHz. Silicon devices could not be used for this application because, as the f_T of Silicon Bipolar monolithic transistors increases, a heavy price is paid in terms of breakdown voltage. The best Si BJT devices (for ICs) which have an f_T in excess of 15GHz, have a breakdown voltage of 12V (BV$_{CBO}$) and higher f_T devices result in even less BV$_{CBO}$. So, there is a limit to the voltage swing on the output which is too low for any multicarrier applications. GaAs devices (both HBT and MESFET) can have Breakdown voltages which are much higher (18V for MESFET and over 22V for the HBT) even though they have transition frequencies well over 20GHz.

For the HBT, whose f_T is over 25GHz, the DC collector voltage can be as high as 10V and the resultant voltage swing is then 20V$_{PP}$. With a push pull arrangement, the voltage swing doubles to 40V$_{PP}$ which covers most CATV distribution requirements. This makes the HBT the best candidate to provide the best voltage compliance for a wideband amplifier. The second very real advantage of the HBT is the fact that base - collector capacitance is small and much more constant than either the Si BJT or the MESFET. Figure 5 shows the capacitance variation vs. voltage for a Si

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BJT and an HBT. Note that the HBT capacitance is nearly constant with collector voltage. This has a significant effect on linearity as will be shown later.

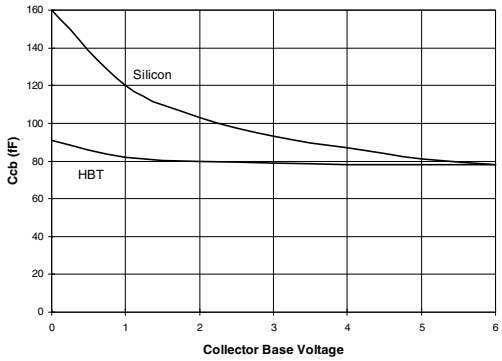


Figure 5. Ccb for HBT and Silicon Bipolar

RF Micro Devices has approached the marketplace for RF products using a philosophy of Optimum Technology Matching (OTM) which uses the best technology at our disposal (GaAs MESFET, Silicon Bipolar, CMOS, and GaAs HBT) to address the needs of the market. In other words, we don't restrict the selection of the technology utilized, a priori, but instead, seek that which will yield the most effective solution for our customers. In this case, the overriding concern is to maximize the linearity of the amplifier with minimum power consumption, and of course, do so at a reasonable price. Over the years, our experience is that the most linear amplifiers we can build are invariably GaAs HBT devices. In order to illustrate the performance differences and show why we selected HBT for ultra linear amplifier products, three different parts have been simulated for comparison - two HBT parts, a Si BJT part, and a GaAs MESFET part. The modeling used to simulate these devices is very accurate and has been tested in practice for many types of circuit. One of the HBT parts is the RF2312, and the other is the RF2317. We have laboratory confirmation of the accuracy of the simulation since each of these parts have been tested

Figure 6 shows distortion in the RF2312 and RF2317 which use HBT devices. The test tones are those used for DIN4500B testing which is a standard test used for European TV systems. The large tone is at a frequency of 736MHz. The smaller tones are each 6dB below the large tone, and the frequency offsets are 18 and 24MHz, respectively. Normally, the DIN rating is the highest level for the large signal which produces distortion products which are -60dBc. As seen in figure 6, the RF2312 distortion is -53dBc for the +60.5dBmV level used for the test. In order to obtain -60dBc, the level of the large signal must be decreased to about 57dBmV. Since we are only interested in comparative data, the signal is left at +60.5dBmV for the comparisons even though all but the RF2317 will not have good enough performance at the +60.5dBmV level. The RF2317 obviously has the capability to produce significantly more than +60.5dBmV per channel since its IM products are down about 65dB. In fact, it should meet DIN requirements up to a level of +63dBmV.

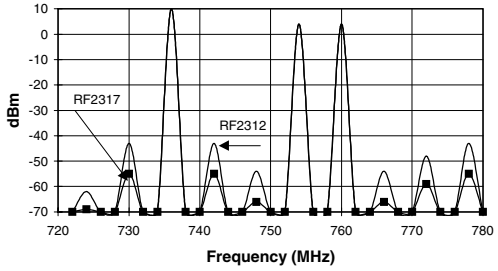


Figure 6. IM distortion with Three-Tone Input

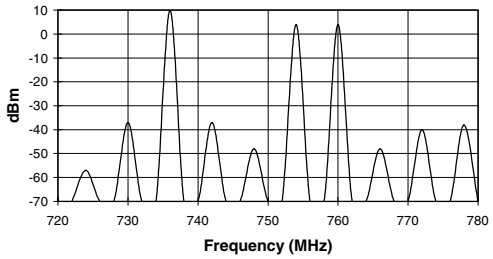


Figure 7. IM Distortion with Three-Tone Input, Silicon device

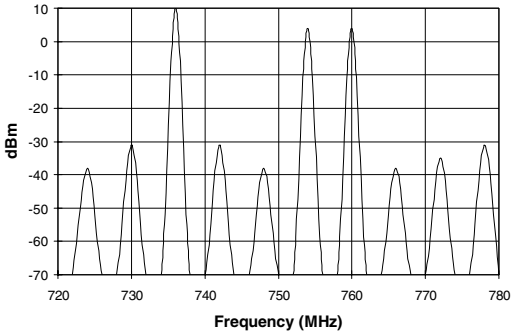


Figure 8. IM Distortion with Three-Tone Input, GaAs MESFET device

The spectrum of figure 7 is the output of the same circuit as the HBT parts except that Silicon Bipolar tran-

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sistors are used. The transistors are actually hypothetical transistors, in that they have identical properties as the HBT circuit except for the base - collector capacitance which is set to have Capacitance vs. Voltage variations like the Silicon transistor shown in figure 5. The bias conditions, both current and voltage are identical to those used for the RF2312 simulation. This Silicon circuit is a very optimistic case since no Silicon BJT IC process exists which has the combination of Early Voltage, f_T, and BVCEO which is associated with the HBT device. But, if one could find a Silicon process with these attributes the result would be as shown. Note that the distortion products increase by approximately 6dB, because, and only because, the base - collector capacitance varies with voltage. The degradation in performance shows clearly the advantages of the HBT over any process which has a significant variation in Capacitance vs. Voltage.

Figure 8 shows the same circuit using GaAs MESFET devices for the active elements of the design. Again, the bias conditions are identical. In addition, the sizing (Gate width) and pinch off voltage for these FETs were optimized for best performance. This circuit is not hypothetical in the sense used above, because it is possible to physically realize the circuit. The linearity of this circuit suffers because of varying capacitance like the Silicon device, and also because of the strongly non linear output conductance of MESFETs. In addition, because of the lower GM for the MESFET, no source degeneration is possible. In fact, it proved impossible to obtain the same gain as is possible with the HBT and Si BJT implementations, so the input signals had to be increased to get the same output power. The results are clearly very inferior to both the Si Bipolar design and the HBT. So, while it is possible to obtain MESFET devices which have sufficient breakdown and f_T, they are not a good choice for high linearity amplifiers because gain is lower and distortion is higher.

Chip Design

The RF2312 and RF2317 are a simple Darlington "Cascadable Gain Block" circuit design as shown in figure 9. This is a broadband feedback amplifier which has its inputs and outputs matched to 75Ohms by virtue of the feedback resistor. Gain is determined by the feedback resistor (RFB) and the emitter resistor (RE2). These resistors along with resistor RB also set the DC bias conditions on the part. The output is connected to the power supply through an inductor (to provide an RF open circuit) and a series resistor which sets the current through the device. The value of the resistor is determined by calculating the necessary voltage drop at the desired current level. The voltage drop is the difference between the power supply voltage and the device voltage as given in figure 10. For example, if the power supply voltage is to be 10V and the device current is desired to be 100mA, consulting figure 10, we see that the device voltage is 5.4V and the drop across the external resistor must be 10-5.4=4.6V. The current is 100mA, so R=4.6/.1 = 46Ohms. In this manner, the desired bias conditions may be set up for any power supply voltage from about 7V to 12V. Voltages outside of that range are not recommended.

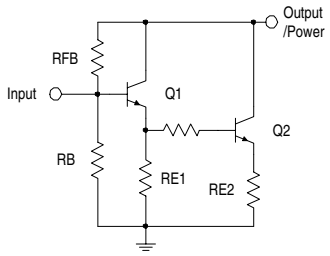


Figure 9. Darlington gain block

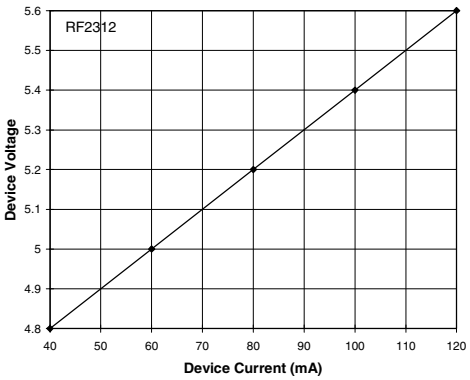


Figure 10. Device voltage vs. device current

The inductor value is set such that the reactance at the lowest frequency of operation is at least 200 Ohms. The input and output coupling capacitors are set such that their reactance at the lowest frequency of operation is less than 10Ohms.

Chip Performance

A summary of the measured performance of the RF2312 and RF2317 is shown in table 1. Note that the table reflects measurements done in a 50Ohm system. This is because we were equipped for only 50 Ohm measurements for some of the parameters. So for consistency, all of the performance measures are listed as 50 Ohm measurements. To perform all of the measure-

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ments with laboratory test equipment, a 50 to 75Ohm transformer must be connected to both the input and output ports. Unfortunately, the transformers have some loss and don't do a good job over the full bandwidth of the part - hence the 50Ohm measurements. Because the imaginary parts of Z_{IN} and Z_{OUT} are very low, the VSWR is pretty good in both 50Ohm and 75Ohm systems, so 50Ohm measurements were performed for the table.

Typical Performance	RF2312	RF2317 (expected)
Gain	15.5dB	14.5dB
Gain Flatness	±0.3dB	±0.5dB
Bandwidth (3dB)	2.5GHz	1.8GHz
Noise Figure	3.8dB	5dB
P_{MAX} @ 500MHz	+21dBm	+26dBm
OIP_3 @ 500MHz	+38dBm	+44dBm
OIP_2	+57dBm	+63dBm
Input VSWR	1.4:1	1.2:1
Output VSWR	1.6:1	1.3:1
I_{CC}	100mA	200mA
V_D	5.4V	8.0V

Table 1. Chip performance

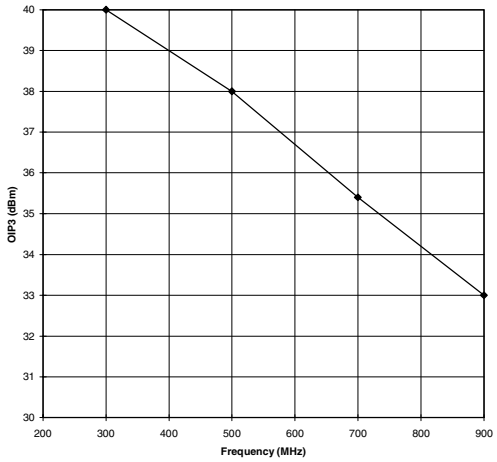


Figure 11. OIP3 vs. frequency

A concern with any wideband amplifier of this sort is its stability - particularly when driving filters and severely unmatched loads. The HBT parts have been tested under a variety of conditions using various bandpass and lowpass filters without evidence of any oscillations. The parts has also been driven and loaded simultaneously with 10:1 tuners and showed no unstable properties.

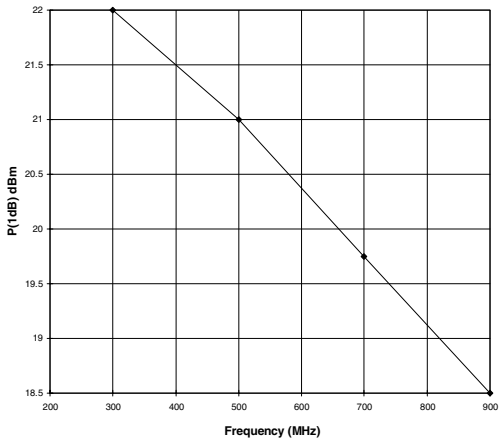


Figure 12. P_{1dB} vs. frequency

Figures 11 and 12 show the Output Third Order Intercept Point (OIP3) and Power Output at the 1 dB gain compression point (P_{1dB}) of the RF2312 vs. Frequency. Note that power handling ability does decrease as frequency increases. This is inherent in the Darlington configuration. It is the result of Beta decreasing in the second transistor (Q2) which forces the emitter follower stage (Q1) to provide more current at higher frequencies. A lower f_T, as may be found in a Si device, aggravates that situation - i.e. the higher the f_T of the devices, the better. Distortion resulting from this effect can be decreased by increasing the collector current of the first stage (lower the value of RE1). This, of course, increases overall power consumption. The current level set in the RF2312 is set to achieve the performance goals for the part, and yield good multicarrier performance up to 1 GHz.

Figure 15 shows the frequency response of the RF2312 mounted on a PCB with approximately 3 inch microstrip traces. Note that while the amplifier has a very flat frequency response, parasitic elements associated with the construction of the circuit board roll the response off slightly at the higher frequencies. Generally, this roll off is of the order of a few tenths of a dB if care is taken in the layout of the PCB. One frequently overlooked aspect of the layout is the ground traces. To obtain a flat frequency response, a ground plane should be placed directly under the amplifier and the ground pins soldered directly to it. If the opposite side of the PCB is used for ground plane, multiple vias should be placed beneath each ground pin. Input and output traces should be 50 or 75Ohm microstrip and

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high quality, high frequency coupling capacitors and inductors should be used.

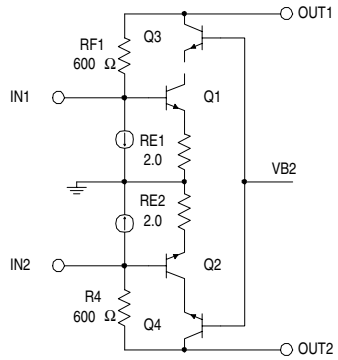


Figure 13. Cascode push-pull amplifier

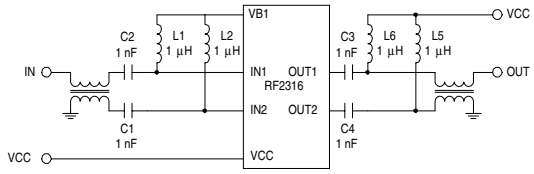


Figure 14. External connections for the RF2316

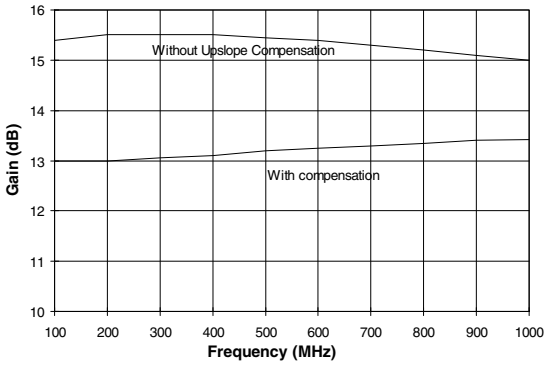


Figure 15. Gain vs. frequency

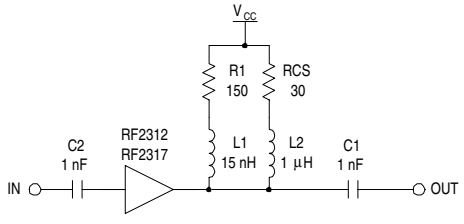


Figure 16. Circuit for high frequency up-slope compensation

In some applications, however, even a few tenths of a dB can be a problem. In that case, the circuit of figure 16 can be used to provide a positive “upslope” to the frequency response. Essentially, a series L-R is added to the output circuit in parallel with the VCC feed L-R network. This loads the output at the lower frequencies hence reducing the gain. As frequency goes up, however, the loading is reduced because the reactance of the inductor goes up with frequency. This circuit may be used with any Darlington amplifier which has adequate bandwidth, including the RF2317 and the RF2316. The output return loss is also improved with the addition of this circuit.

Push Pull Configuration

Figure 13 shows a partial schematic of a Push Pull Cascode circuit using HBT devices. This architecture is typically used for high power distribution amplifiers which produce high output voltages. It has an inherent advantage over singe ended designs in that the output voltage swing can be double that of the single ended design (providing 4 times the power) and, importantly, the even order distortion products are reduced from a single ended design. That is, for a given collector current and voltage, the balanced design produces the same odd order results (same IP3), but even order distortion is reduced typically 10 dB (better IP2) - depending on the balance achieved. The disadvantage of this circuit configuration is that it requires transformers or baluns in order to convert the single ended input and output signals to differential balanced signals at the ports of the active device. These passive devices have power loss which must be made up by the amplifier. The frequency response is also adversely affected.

The RF2316 is a balanced amplifier. It uses external baluns which are easy to wind and have a minimal impact on frequency response and power. The connections external to the chip are shown in figure 14. The unit will produce an output of +44 dBmV per channel with acceptable distortion products.

Conclusion

The HBT amplifiers offer the best frequency response and the highest linearity (for a given DC power consumption) of any commercially available integrated circuit. They offer the small size and the inherent reliability and repeatability of a monolithic design. OIP3 numbers up to +48 dBm have been achieved and the frequency response is extremely flat across a full Gigahertz of bandwidth for all the mentioned parts. They operate from a single power supply, which can range from 7 to 12V. Pricing is less than $4.00 for the RF2312 and RF2317.

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European Applications for RF2403 Cordless Telephone Front End RFIC

A front end RFIC for cordless telephone applications has been developed for use in the 902MHz to 928MHz ISM (Industrial-Scientific-Medical) band in the United States under Part 15 of the FCC Rules. Potential applications for this RFIC in this frequency band include cordless telephones, wireless LANs, wireless security systems and point-of-sale (POS) terminals.

This RFIC, the RF2403, consists of a single-stage LNA, a two-stage PA with 21dBm of output power and a transmit/receive switch. The RFIC is built using a commercial GaAs MESFET process, and is packaged in a SOP-16 narrowbody surface-mount package. The circuit operates with a +5.0V supply, and has separate enable lines which control the bias to the transmit and receive functions. All bias and control signals operate with voltages which lie between ground potential and V_{DD}. With both enable lines at logic low, the circuit is in a "powerdown" mode in which it draws approximately 1.0mA of leakage current from the V_{DD} supply. Some external passive components are required, primarily for DC blocking and RF bypassing functions. The PA output impedance matching circuitry, consisting of a pi-network, is realized using external passive components in order to both conserve die area and to reduce parasitic losses. This same RFIC has been evaluated for use in 433MHz European applications, and has been found to have very good RF performance there.

Although no changes have been made to the RFIC itself, several changes to the application circuit are necessary for operation at 433MHz. Table 1 shows the component values for both versions of the RF2403 application circuit. The two application schematics are shown, for 433MHz operation and for 915MHz operation, in Figures 1 and 2, respectively. The resulting RF performance for these circuits is shown in Table 2. The I/O port return losses are somewhat degraded at 433MHz, primarily due to the excess reactance of the on-chip DC blocking capacitors in the RFIC. The RF2403 does have comparable gain, output power and linearity at 433MHz with respect to its performance at 915MHz.

RF Specification	Measured Performance (All Typical) @V_{DD}=5.0V	
	433MHz Circuit	915MHz Circuit
LNA Gain[1]	17dB	16dB
LNA NF[1]	2.4dB	2.7dB
LNA P_{1dB}[1]	+6.0dBm	+6.0dBm
RX IRL, ANT port[1]	6.0dB	9.0dB
LNA ORL	15dB	13dB
PA Small Signal Gain[1]	28dB	28dB
PA P_{1dB}[1]	19.0dBm	21.0dBm
PA IRL	11dB	17dB
PA ORL, ANT port[1]	11.5dB	10.5dB
PA Two-tone P_{OUT}[1,2] @ -25dBc IMD3	17.5dBm	16.7dBm

Table 2. RF2403 measured performance, using the two application schematics

Note 1: Performance is measured through the monolithic T/R switch
Note 2: f_1=432.5MHz, f_2=433.5MHz, or, f_1=914.5MHz, f_2=915.5MHz

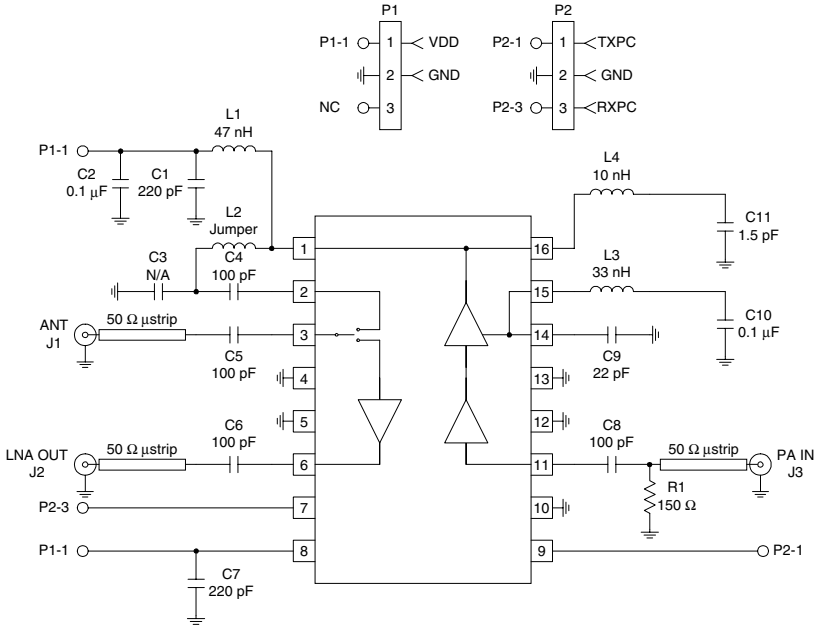


Figure 1. RF2403 Application Circuit for 433 MHz European Applications

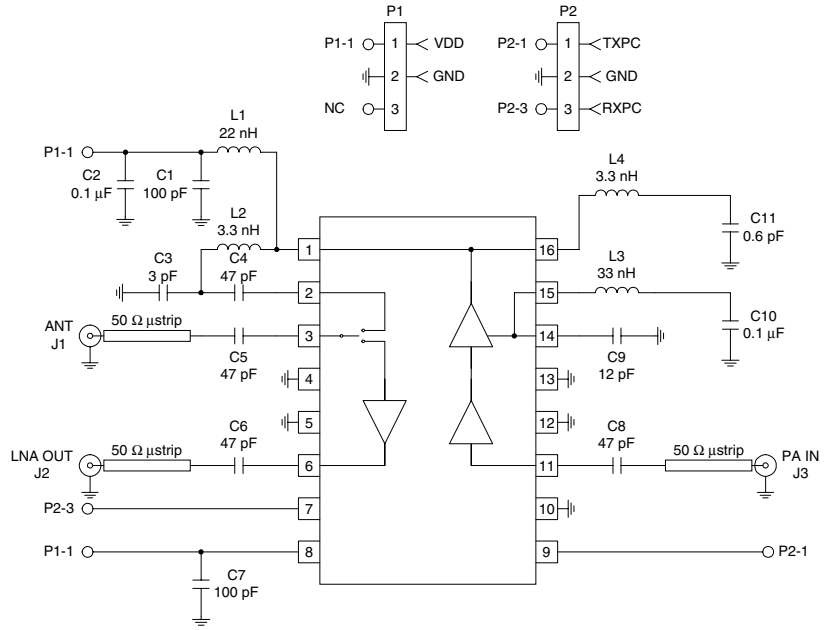


Figure 2. RF2403 Application Circuit for 915 MHz ISM Applications

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Component Designation	Value (0805 size, unless noted otherwise)	
	433MHz Circuit	915MHz Circuit
C1	220pF	100pF
C2	0.1µF	0.1µF
C3	Omit	3.0pF
C4	100pF	47pF
C5	100pF	47pF
C6	100pF	47pF
C7	220pF	100pF
C8	100pF	47pF
C9	22pF	12pF
C10	0.1µF	0.1µF
C11	1.5pF ATC 100A	0.6pF ATC 100A
L1	47nH	22nH
L2	Replace with metal strip jumper	3.3nH
L3	33nH	33nH
L4	10nH	3.3nH
R1	150Ω 1206, added shunt to ground on DC-isolated side of C8	Omit

Table 1. Application circuit component values

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Combination Oscillator/Buffer Amplifier ICs Simplify LO Design

Abstract
Two new combination oscillator/buffer amplifier ICs are introduced by RF Micro Devices to make the task of designing an LO for wireless applications simpler. The RF2501 and RF2502 are combination oscillator/buffer amplifier ICs with a power down feature that operate anywhere from 750MHz to 1500MHz with the help of an external resonator. The RF2501 offers low current consumption and low output power, while the RF2502 offers higher output power. These ICs are flexible, yet easy to use, and can reduce the load pulling, overall size, and cost of an LO for wireless applications.

Introduction
Local oscillators are very important components of wireless systems, yet the task of designing and building an LO can be very challenging, particularly to those who have not previously designed one. Two new ICs, the RF2501 and RF2502 from RF Micro Devices, are combination oscillator/buffer amplifier ICs that simplify the task of building an LO. They cover the frequency range of 750 MHz to 1500 MHz, which is just right for many wireless applications, including the 902MHz to 928MHz ISM band.

The RF2501 and RF2502 are made to be flexible and easy to use by utilizing an external resonator to set the frequency of oscillation. Both ICs incorporate several integrated buffer amplifiers to minimize load pulling and flatten the output power response. They operate off of a single 5 V supply and have a power down feature that is great for applications that have to conserve battery power.

The RF2501 is a low current, low power integrated oscillator/buffer amplifier. It typically draws approximately 2.6mA and sources -14dBm into a 50Ω load at room temperature and VCC of 5V.

The RF2502 is a higher current, higher power integrated oscillator/buffer amplifier. It typically draws approximately 4.5mA and sources -6dBm into a 50Ω load at room temperature and VCC of 5V.

The ICs are made with silicon BJT technology, which produces good phase noise for an integrated oscillator. Operating at 1500MHz and room temperature, phase noise at 100kHz offset has been measured at -96dBc and at 10kHz offset has been measured at -76dBc for both ICs when used with a microstrip resonator on FR4 board. At lower frequencies, the phase noise will improve, 6dB lower phase noise has been measured at 750MHz.

The RF2501 and RF2502 are offered in a standard SOIC-8 package. When used in a design, they can reduce the overall size and cost of the LO, which are important considerations for wireless applications.

Functional Description
A functional block diagram of the RF2501 is shown in Fig. 1. It includes an oscillator, four buffer amplifiers

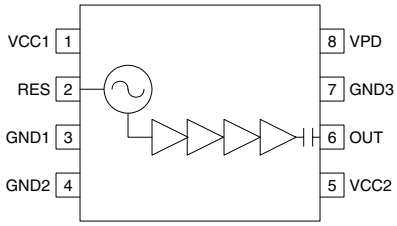


Figure 1. RF2501 Functional Block Diagram

and power down circuitry. Pins 1-4 supply the oscillator, and pins 5-7 supply the buffer amplifiers. Pin 8 is the power down pin, Vpd, that controls the bias to both.

A high voltage on Vpd turns on the IC, and a low voltage on Vpd turns off the IC. When Vpd is 0V, the supply current is less than 1µA. Vpd should be less than 0.7V to fully turn off the IC. To fully turn on the IC, Vpd should be 3.0V or higher, but should not exceed the maximum rating of 5.5V.

The external resonator input is pin 2 and requires a dc blocking capacitor. The resonator is an inductive element. Changing the effective inductance either physically or with a varactor tuned circuit, will change the frequency of oscillation. It should be noted that all parasitics on the circuit board will contribute to the effective inductance and will influence the oscillation frequency. These effects become more pronounced at higher frequencies.

The output of the RF2501 has an internal choke and dc blocking capacitor. This feature reduces the overall size and parts count of the resulting LO.

A functional block diagram of the RF2502 is shown in Fig. 2. The oscillator portion of the IC is the same as

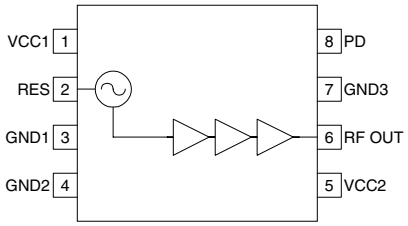


Figure 2. RF2502 Functional Block Diagram

the RF2501. The differences are in the buffer amplifiers. There are three buffer amplifiers instead of four, to increase the available output voltage swing, and the required supply current is greater. The output is open collector, which requires an external choke and blocking capacitor. The result is more available power into a 50Ω load.

Theory of Operation

Each IC has two functional parts: an oscillator and buffer amplifier. The functional blocks have separate ground and VCC pins to increase the isolation and reduce load pulling, one of the key design objectives. An external resonator is utilized to add design flexibility, and the loaded Q of this resonator will impact the performance of the resulting oscillator.

To create an oscillation, negative resistance is generated at pin 2 with a circuit similar to a Colpitts oscillator. Figure 3 shows the input impedance at pin 2 measured with a vector network analyzer, it looks like a negative resistance in series with a capacitor. The negative resistance decays as the frequency increases. An oscillator is created when an inductive element is placed on pin 2 that is the conjugate of the capacitive reactance. A greater inductive element will create a lower frequency of oscillation.

Figure 4 shows the S11 looking into pin 2. It has return gain from 500MHz to 2200MHz at room temperature. The specified frequency range of 750MHz to 1500MHz defines the region where the output power is relatively flat. At lower and higher frequencies, the power will tend to roll off from the nominal value. The specified frequency range is conservatively set to ensure oscillation and maintain performance, but the RF2501 and RF2502 can be used over a broader frequency range with degraded performance.

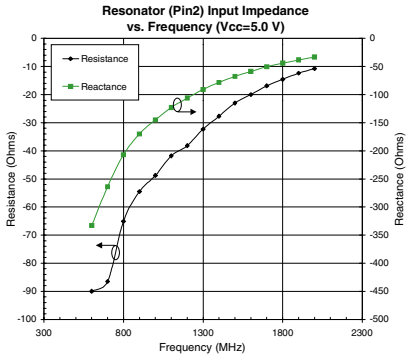


Figure 3. RF2501/2 Input Impedance

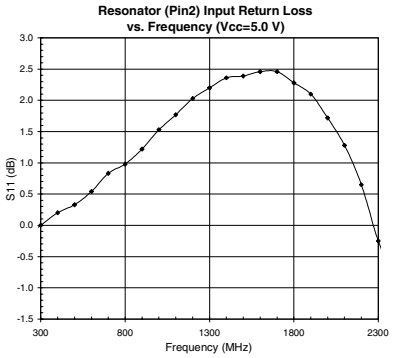


Figure 4. RF2501/2 Input S11 versus Frequency

The overall Q of the external resonator will impact performance. Lower Q means lower power, higher phase noise, and more load pulling. If the Q is too low, the circuit will not oscillate. The ICs are designed to oscillate into a resonator with Q>10. The performance is measured with a microstrip resonator or high quality inductor, which usually have a Q>50. These measurements define the best performance that can be expected from the ICs, a later section describes typical performance and specifications. Lower Q resonators, particularly those including a lossy varactor, might have degraded performance.

The specified output power is measured into a 50Ω load. Both ICs have a high output impedance, and if desired, output matching can be used to obtain more power by transforming 50Ω into a higher impedance. On the RF2502, this could be accomplished by simply

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changing the values of the external output inductor and capacitor.

Applications

In order to demonstrate the use of the RF2501 and RF2502, several application circuits are built and tested. The ICs are used to build VCOs at the 902MHz to 928MHz ISM band, and the RF2502 is used to build a VCO near 1500MHz.

The schematic of a VCO built with the RF2501 is shown in Fig. 5. The resonator is a 15nH coil and varactor connected to pin 2. The zero bias capacitance of the varactor is 15pF, and it is biased through a low cost resistor. Besides the external resonator, the only other external parts required are by-pass capacitors.

The tuning curve and output power for this circuit are shown in Fig. 6. The typical measured performance for this circuit at room temperature into a 50Ω load and VCC of 5V are -12dBm output power, 2.9mA supply current, harmonics less than -12dBc, VCC pushing of 1.7MHz/V, less than 76 kHz of load pulling into a 1.67 VSWR load, and phase noise of -102dBc at 100kHz offset, -89dBc at 25kHz offset, and -81dBc at 10kHz offset.

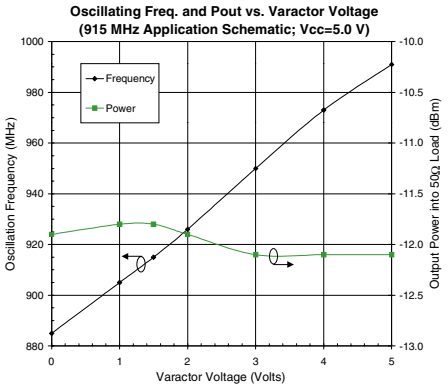


Figure 6. RF2501 915MHz ISM Band Tuning Curve and Output Power

A similar schematic for a VCO operating in the 902MHz to 928MHz ISM band using the RF2502 is shown in Fig. 7. The resonator is the same, and it has an additional 27nH external output choke and output blocking capacitor. The tuning curve and output power for this circuit are shown in Fig. 8. The typical measured performance for this circuit at room temperature into a 50Ω load and VCC of 5V are -5.0dBm output power, 4.8mA supply current, harmonics less than -9.5dBc, VCC pushing of 1.55MHz/V, less than 140kHz of load pulling into a 1.67 VSWR load, and phase noise of -101dBc at 100kHz offset, -88dBc at 25kHz offset, and -80dBc at 10kHz offset.

A last application circuit using the RF2502 in a VCO that operates from 1331MHz to 1607MHz is shown in Fig. 9. The resonator coil is smaller, the varactor zero bias capacitance is 10pF, and the external output choke is 18nH. The external output choke is selected from the manufacturers data to have a self-resonant frequency above the frequency of operation.

The tuning curve and output power for this VCO are shown in Fig. 10. The typical measured performance for this circuit at room temperature into a 50Ω load and VCC of 5V are -5.6dBm output power, 4.2mA supply current, harmonics less than -13 dBc, VCC pushing of 1.8MHz/V, less than 535kHz of load pulling into a 1.67 VSWR load, and phase noise of -96dBc at 100kHz offset, -83dBc at 25kHz offset, and -75dBc at 10kHz offset. The load pulling is measured at 1500MHz.

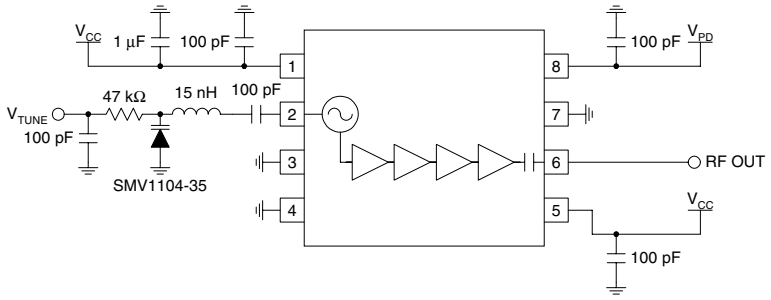


Figure 5. RF2501 915MHz Application Schematic

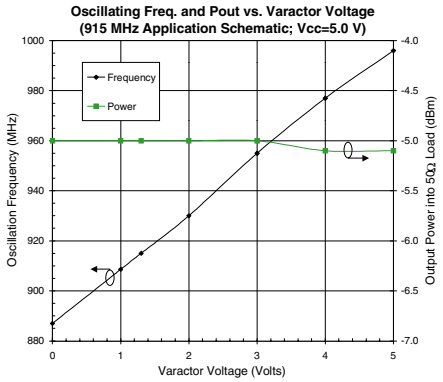


Figure 8. RF2502 915MHz ISM Band Tuning Curve and Output Power

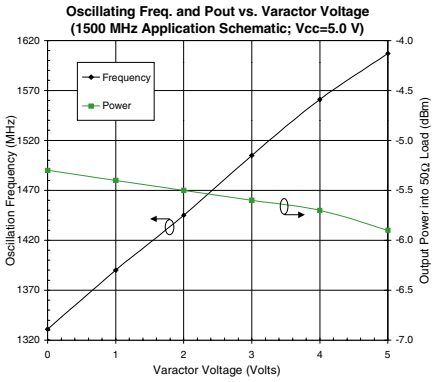


Figure 10. RF2502 1500MHz ISM Band Tuning Curve and Output Power

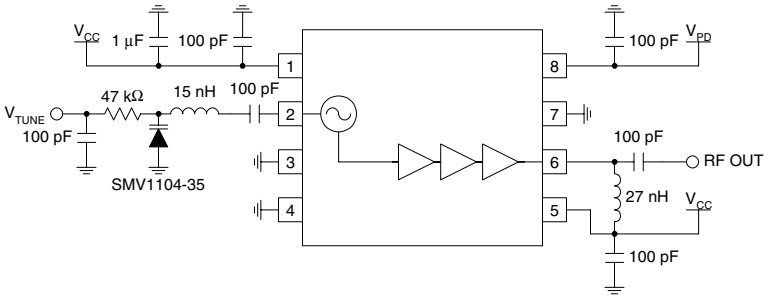


Figure 7. RF2502 915MHz Application Schematic

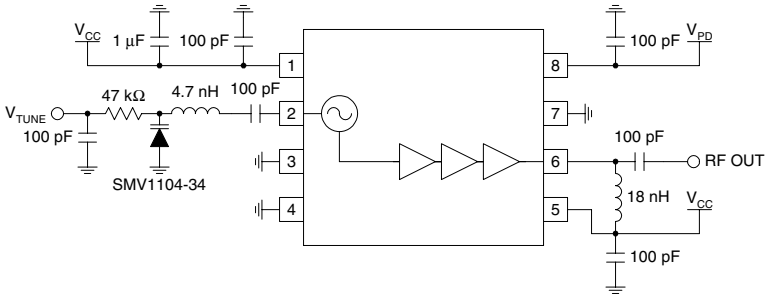


Figure 9. RF2502 1500MHz Application Schematic

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Parameter	Measured Performance			Units
IC	RF2501	RF2502	RF2502	
Frequency	885 to 991	887 to 996	1331 to 1607	MHz
Tuning Voltage	0 to 5	0 to 5	0 to 5	V
Supply Current	2.9	4.8	4.2	mA
P_{OUT}	-12	-5	-5.6	dBm
2nd Harmonic	-15	-9.5	-13	dBc
3rd Harmonic	-12	-18	-23	dBc
V_{CC} Pushing	1.7	1.6	1.8	MHz/V
Load Pulling[A]	76	140	535	kHz
Phase Noise:				
100kHz Offset	-102	-101	-96	dBc
25kHz Offset	-89	-88	-83	dBc
10kHz Offset	-81	-80	-75	dBc
Schematic	Figure 5	Figure 7	Figure 9	
[A]Load Pulling is measured into a 1.67 VSWR load.				

Table 1. Typical measured performance of application circuits at room temperature

Parameter	RF2501	RF2502	Units
VCC	5	5	V
Frequency	750-1500	750-1500	MHz
ICC (on)	2.6	4.8	mA
ICC (off)	<1	<1	mA
VPD (on)	5	5	V
VPD (off)	0	0	V
IPD (on)	<100	<100	nA
IPD (off)	<0.1	<0.1	nA
Output Power	-14	-6	dBm
Load Pulling[A]:			
750 MHz	<100	<200	kHz
1500 MHz	< 1	<1	MHz
VCC Pushing	<3	<3	MHz/V
Phase Noise[B]:			
100 kHz Offset	-96	-96	dBc
10 kHz Offset	-76	-76	dBc
Temperature	-40 to 85	-40 to 85	°C
[A]Load Pulling is measured into a 1.67 VSWR			
[B]Phase noise is measured at 1500MHz at room temperature with a low loss microstrip resonator. Phase noise generally improves by 6dB/ octave as the frequency is lowered.			

Table 2. Summary of specifications and typical performance into a 50Ω load at room temperature using a microstrip resonator

A summary of the measured performance at room temperature for these three application circuits is shown in Table 1. The values quoted are typical across the band, there will be some variation with frequency and component variation.

Specifications

The specifications and typical performance of the RF2501 and RF2502 are summarized in Table 2. The parameters are typical values at room temperature for a microstrip resonator or a similar high Q inductor. The specific performance of a circuit using the RF2501 or RF2502 will vary depending on the Q of the resonator and frequency. In particular, low Q resonators will result in degraded performance.

There are some general trends in performance with the frequency of operation. It can be expected that the load

pulling will be greater at higher frequencies than at lower frequencies due to the greater effects of parasitic package coupling. Phase noise is greater at higher frequencies due to device physics, and can generally be estimated using the factor of 6dB/octave. Phase noise in Table 2 is typical performance at 1500MHz, and an oscillator built at 750MHz will generally have 6dB better phase noise.

Summary and Conclusions

Two new oscillator/buffer amplifier ICs are introduced by RF Micro Devices. The RF2501 and a higher power version, the RF2502, are flexible building blocks that can be used to build an LO from 750MHz to 1500MHz. They offer a power down feature, low current consumption, reduced load pulling, and can be used to reduce the size and cost of building an LO.

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Quadrature Modulator/Demodulator IC Covers Baseband to 250MHz

Introduction

Most modern wired and wireless communication systems require sophisticated frequency conversion to and from baseband. Quadrature, or I/Q, modulation is frequently used by system designers to up-convert data to an intermediate frequency (IF) of anywhere from 1MHz up to several hundred MHz. Simultaneously, the receiver must down-convert the information contained at the IF and output the data in its original I/Q format. RF Micro Devices has developed an advanced integrated circuit (IC) that can perform both of these important functions. The RF2703 Quadrature Modulator/Demodulator is a monolithic IC that operates from a single 2.7V to 6V power supply. This low cost, high performance IC packs an LO limiting stage, a digital divider, and two double-balanced mixers within a small SO-14 plastic package (see Figure 1).

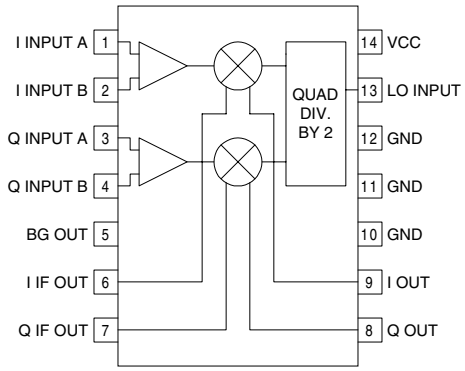


Figure 1. The functional block diagram.

Demodulator

The RF2703 can be configured easily within a receiver to perform as a quadrature demodulator, as illustrated in Figure 2. The RF2703 outputs I and Q signals with typically 2° or better phase error and 0.1dB or better amplitude imbalance. The baseband (I/Q) outputs of the device can handle data rates from DC to 50MHz and can drive greater than 1Vp-p into a high impedance analog-to-digital converter (ADC) or operational amplifier. DC offset between the I and Q outputs is typically smaller than 10mV.

Operation of the RF2703 is simple and easy to understand. When used as a demodulator in a receiver, the system IF carrier is fed from an IF amplifier or filter into the I INPUT and Q INPUT ports of the RF2703 (pins 1 through 4 in Figure 1). These input pins are tied together in demodulation mode so that the IF signal is fed into the Gilbert cell mixers (see Figure 3) in parallel. The input impedance of each of the four input pins is 1200Ω, but when these pins are driven in a single-ended configuration the total impedance is half that, or 600Ω (refer to Figure 2). The IC can also be driven differentially where pins 1 and 2 are complementary and pins 3 and 4 are complementary.

The IF signal drives the lower differential pair of each of the two Gilbert cell mixers. The upper transistors, or switching transistors, are driven by the local oscillator (LO) signal. The LO signal is provided by an external VCO or other frequency synthesizer and is connected to the RF2703 at the LO pin. Since the LO circuitry is driven by voltage and there is no concern for noise figure or maximum power transfer, there is generally no need to match this port. A shunt 50Ω resistor can be placed externally to the port to interface with test equipment, but otherwise power is not a concern. If a VCO or other LO source cannot supply enough voltage, a reactive match (voltage transformation) can be implemented. The LO signal frequency must be twice the frequency of the IF signal, because the digital divider (flip-flop) which splits the LO signal into two quadrature waveforms also divides the frequency of the LO signal by two. The highest frequency of recommended operation is 250MHz for the IF signal, which translates to 500MHz for the LO input. The IC will operate above this frequency range but phase accuracy and amplitude balance may degrade.

From the system designer's point of view, using twice the LO frequency is beneficial in that LO leakage into other components of the system does not appear as co-channel interference. In a typical receiver, the received signal may be very weak (≅ -110dBm) at the antenna. As the signal passes through an LNA/mixer stage it is down-converted to IF. Assuming the LNA/mixer stage has 20dB of gain, the IF signal is now at -90dBm. Any kind of jammer at the IF frequency (co-channel interference) greater than around -100dBm will wreak havoc once the IF signal reaches the IF amplifier. The jammer will be amplified and reduce dynamic range, effectively increasing bit error rate. An IF VCO commonly outputs levels around -5dBm. Since

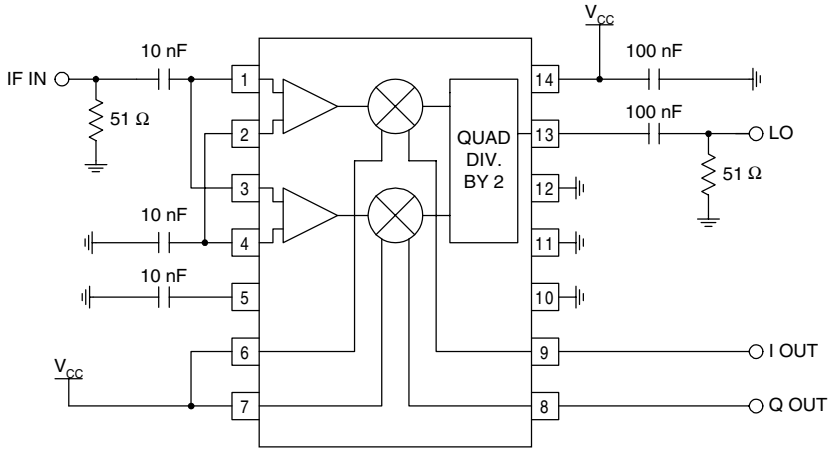


Figure 2. The demodulator configuration.

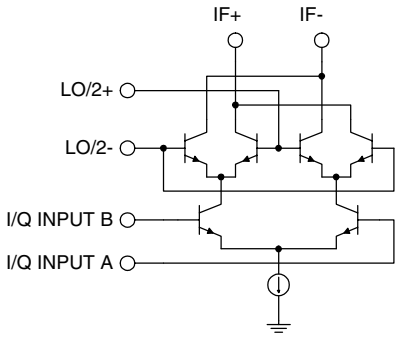


Figure 3. The Gilbert cell Mixer equivalent circuit.

it is virtually impossible to get 95dB of isolation inside a portable device, such as a cordless or cellular phone, the VCO output will leak into the IF signal path and act as co-channel interference. With a 2X frequency LO source, this problem is eliminated because any leakage into the IF path will be bandpass filtered, a huge advantage. In some systems, CDMA cellular for example, the transmission chain uses gain control to precisely regulate the output level of the radio frequency (RF) carrier. The gain control is generally done at IF by an automatic gain control (AGC) amplifier before the data is up-converted to RF. Under conditions where the AGC amplifier is attenuating, the output of the amplifier can be down around -90dBm. As in the receive case, the VCO output can leak into the IF path at the AGC amplifier output or into the upconverter input. This co-channel interference will not be filtered and will pass out the antenna as a jammer. Once again, a 2X frequency LO source will not cause this problem as its leakage will be filtered out before it ever reaches the antenna.

As the 2X frequency LO signal enters the RF2703, the LO signal immediately passes through several limiting amplifier stages to ensure that it will have a large enough signal swing to drive the flip-flop circuitry. This feature allows the system designer to have great flexibility with LO signal level. The IC will accurately perform the dividing function over all but the highest frequencies with as little as 60 mVp-p drive level at the LO input. Since performance of the LO circuitry is frequency-dependent, especially at the higher end of the frequency range, phase and amplitude accuracy can be optimized by increasing the LO signal level from 60 mVp-p until sideband suppression is maximized.

The LO signal continues straight from the limiting stages to the flip-flop. The LO actually acts as the clock signal for the flip-flop, which divides the clock frequency by two and outputs two signals which are 90° out of phase. One of these signals drives the switching transistors of the I Gilbert cell and one of them drives the switching transistors of the Q Gilbert cell. The Gilbert cells mix the IF and LO/2 signals together to extract the baseband data; 20dB of conversion gain is also provided in the mixers to boost a weak IF signal. The baseband data proceeds through output buffers and exits the part at pins 8 and 9 (IOUT and QOUT). The output ports have a 50Ω AC output impedance but are designed to drive high impedance loads (>10kΩ). Each output also contains an internal 2 kΩ resistor that sinks current for the output emitter follower transistor. Since the outputs are DC coupled, using lower imped-

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ance output loads will cause more current to be drawn from the IC. The RF2703 can drive down to a 50Ω DC coupled load, but the output voltage swing will decrease by more than 6dB. Typically an ADC, op-amp, or digital filter will follow the RF2703, all of which have high input impedances.

Having described the circuitry involved in demodulation, it is helpful to understand how a demodulator works mathematically. The following example is a simple but effective way to communicate the theory of operation of a quadrature demodulator. In the example, single sideband (SSB) modulation will be used, where the data signals are two sinusoids, i(t) and q(t), that are in quadrature. When the IF carrier with data reaches the demodulator, it can be expressed as follows:

$$V(t) = A \cos[(\omega_{IF} + \omega_m)t] \quad (1)$$

where:

A = signal amplitude,

ω_{IF} = the IF carrier frequency, and

ω_m = the data frequency.

As shown in Figure 4, an LO signal at the IF frequency is split into an in-phase signal and a quadrature signal. These two signals are then multiplied with V(t):

$$Vi(t) = A \cos[(\omega_{IF} + \omega_m)t] \cos(\omega_{IF}t) \quad (2)$$

and

$$Vq(t) = A \cos[(\omega_{IF} + \omega_m)t] \sin(\omega_{IF}t) \quad (3)$$

where:

Vi(t) = the in-phase product and

Vq(t) = the quadrature product.

Using trigonometric identities:

$$Vi(t) = A/2 \cos(\omega_m t) + A/2 \cos[(2\omega_{IF} + \omega_m)t] \quad (4)$$

and

$$Vq(t) = A/2 \sin(\omega_m t) + A/2 \sin[(2\omega_{IF} + \omega_m)t]. \quad (5)$$

After low-pass filtering at baseband:

$$Vi(t) = A/2 \cos(\omega_m t) = A/2\ i(t) \quad (6)$$

and

$$Vq(t) = A/2 \sin(\omega_m t) = A/2\ q(t). \quad (7)$$

Thus the demodulator has retrieved the data. The above math can be worked in reverse to illustrate SSB modulation.

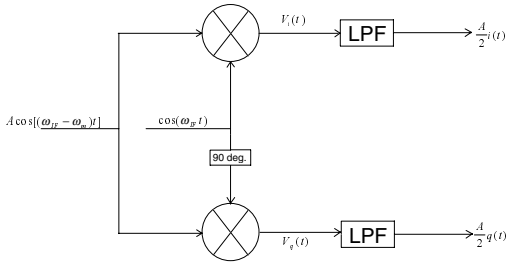


Figure 4. Quadrature Demodulation Operation.

Modulator

The RF2703 can be configured as a quadrature modulator for use in a transmit chain, as in Figure 5. Generally, quadrature modulators are described by their single sideband (SSB) output spectrum. Typical carrier suppression for the RF2703 is 25dBc, although this number can be increased by adjusting the DC voltages at the I and Q baseband inputs (pins 1 through 4) to obtain a null in the carrier. Suppression of the unwanted sideband is typically 35dBc or better, which corresponds to less than 2° phase error and less than 0.1dB amplitude imbalance. The RF2703 is capable of driving several hundred millivolts peak-to-peak into a 1200Ω load (see Figure 6) while providing up to 15dB of conversion gain (see Figure 7).

Operation of the RF2703 in modulation mode is similar to that in demodulation mode, except in reverse. In this case, baseband data is fed into the I INPUT and Q INPUT ports (pins 1 through 4). Figure 5 shows how to connect the baseband single-endedly, but the data can still be connected differentially just as in demodulation mode. The data drives the lower differential pair of each of the Gilbert cell mixers; the I data drives one mixer and the Q data drives the other.

The LO signal is applied to the IC as described earlier with the frequency at twice what the desired IF output frequency is. The same levels and frequency range used in demodulation mode apply in modulation mode. The LO signal proceeds through the limiting stages and through the flip-flop to drive the switching transistors of each of the Gilbert cell mixers. The outputs of the two mixers are summed together by tying pins 6

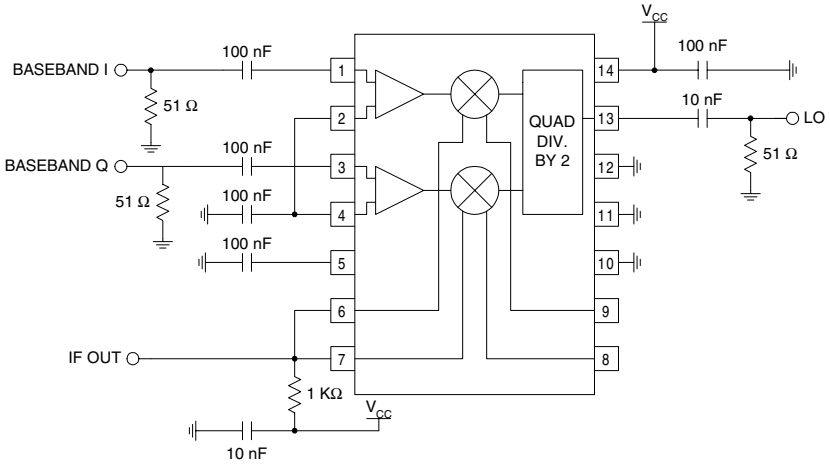


Figure 5. The modulator configuration.

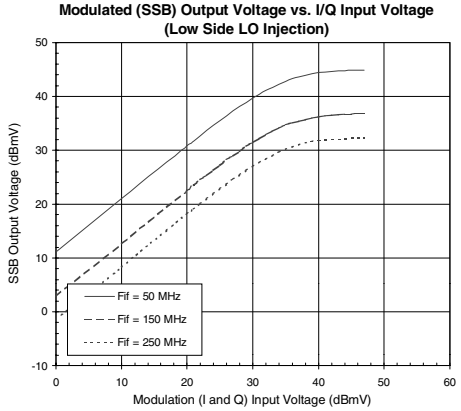


Figure 6. IF Output vs. I/Q Modulation Level

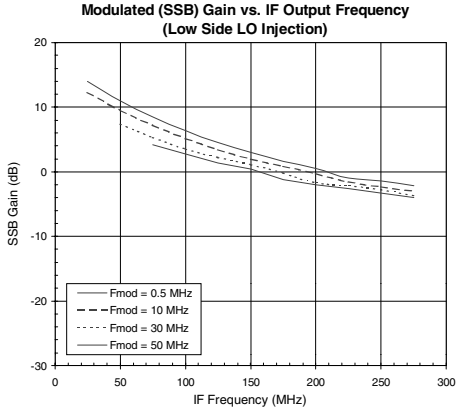


Figure 7. SSB Modulator Gain vs. IF Frequency

and 7 together external to the part.

Pins 6 and 7 are direct connections to the collectors of the switching transistors of the Gilbert cells. For this reason, the power supply (Vcc) must be connected to these pins in both operation modes. During modulation, Vcc is provided through a load resistor or through an inductor. In modulation mode the load resistor not only provides DC biasing, it also determines the conversion gain of the Gilbert cells. Since connecting through a resistor will cause a voltage drop which can saturate the Gilbert cell switching transistors, it is recommended to use no more than 1200Ω. If a choke or matching inductor is used in parallel with the resistor, then this value can be increased somewhat. It may be necessary in a system to match the output to a lower impedance, and this can be achieved by a simple L-C network tuned for the frequency desired.

Conclusion

The RF2703 provides two critical building blocks in RF system design. This low-cost, high-performance IC fills the need for extremely accurate modulation and demodulation for any number of wired and wireless communication systems. With outstanding performance, low cost, and small size, the RF2703 is helping to simplify many RF system designers' work.

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An FSK Transmit and Receive Chip Set

The RF9901 and RF9902 are low cost monolithic integrated circuits which can be used separately or together as a two-chip set that provides all the functions necessary to implement a binary FSK transceiver for such applications as 915MHz ISM-band handheld terminals for POS meter reading, bar-coding reading, as well as other digital applications such as SMR.

The parts are provided in 16-lead plastic SOIC packaging, operate from a 3V to 5V supply with no negative voltage required and cover the 400MHz to 950MHz frequency range. They are implemented using a low cost silicon bipolar process which features NPN transistors with an f_t of 5GHz, PNP transistors with an f_t of 1GHz, thin film resistors, Schottky diodes and capacitors.

THE RF9901 TRANSMITTER

The RF9901 operates as an FSK transmitter with all the functions required to form a fully integrated PLL system. A functional block diagram of the device is shown in Figure 1 and a typical application circuit for operation at 916MHz is shown in Figure 2. The PLL section consists of an integrated phase-frequency detector, VCO, divide-by-32 prescaler and reference frequency oscillator amplifier. The VCO runs at one half of the output frequency, f_o, since a doubler circuit is used after the VCO to provide the output signal.

Bandgap Reference

The bandgap reference voltage is used internally for biasing to achieve constant performance over varying temperature and power supply voltages. On-chip circuitry provides a bandgap voltage of 1.15V. The bandgap is brought out through a pin and can be used as an external reference for circuitry that has less than 1mA current draw and can provide a constant load. A series resistor should be used to prevent any oscillations in the case of a long lead being connected to this pin.

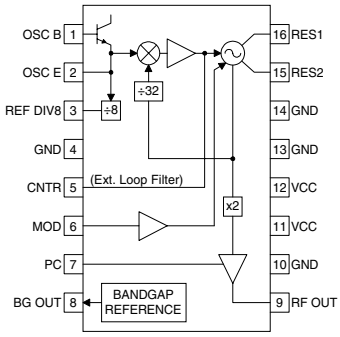


Figure 1. RF9901 Functional Block Diagram

Crystal Reference Oscillator

The crystal reference oscillator is a common emitter Colpitts design which uses a parallel resonant crystal operating in the fundamental mode. The crystal is calibrated with a 50pF load. The values of the external

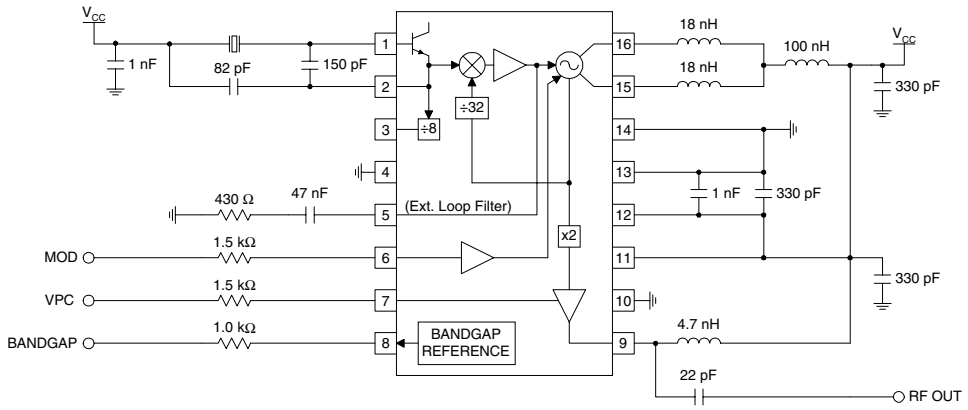


Figure 2. RF9901 916MHz Application Schematic

feedback capacitors can be adjusted for optimal performance at different frequencies. The crystal can be replaced by an external source. The signal should be AC coupled using a capacitor and the level should be about 500mV_{p-p}.

VCO and Output Amplifier

The VCO design is based on a balanced configuration which utilizes cross-coupling between the bases and collectors of a transistor pair. The tank resonator circuits are formed by a pair of external inductors and on-chip varactor diodes which are driven by the phase/frequency detector to form part of the PLL.

A balanced configuration was used instead of a single ended design since it can provide differential drive to the prescaler section and has better rejection of unwanted modulation signals although it does require two tuning elements instead of one. The VCO resonators must have a DC path to VCC on these pins. The value of the inductors required for an f_o=916MHz is 18nH with the values required for other frequencies being approximated by the following empirically derived formula

$$L = \frac{12.6 \cdot 10^6}{f^2}$$

where L is the inductor value in nH and f is the frequency in MHz.

The transmitter uses a VCO/doubler approach for f_o although a fundamental VCO was the first consideration for the original design. The trade-off between the two approaches were that the doubler design has a higher output level, better noise characteristics and greater temperature stability than the fundamental design while the main advantage in the fundamental design is that the f_o/2 harmonic level is much lower. The f_o/2 level in the doubler design is only 25dB below the fundamental.

Typical harmonic levels for an fo = 916MHz at 0dBm into a 50Ω load with V_{CC}=4V and the power control voltage on pin 7, V_{PC}=2.5V, are as follows:

Harmonic	Level Below Fundamental (dBc)
2fo	20
3fo	min 30
fo/2	25
Reference Frequency	min 55

The typical current draw at V_{CC}=4V, V_{PC}=2.5V is 26mA. The power control pin when set to 0V disables the output amplifier and the device draws about 20mA so it does not function as a complete power down control. At positive voltages above 1V the output amplifier turns on. The higher the voltage, the higher the power although a series resistor of 1.5kΩ should be placed on pin 7 if V_{PC} is taken directly from V_{CC}.

The amplifier output must have a DC connection to V_{CC} through an RF choke. The RF choke can be part of the matching network. An extra one or two components at the most can be added to the output network to reduce the f_o/2 level since the network is a high pass structure.

PLL Parameters and Frequency Modulation

The fixed divide by 32 prescaler is implemented using a master/slave flip-flop divider architecture while the phase/frequency detector essentially uses D type flip-flops and charge pumps to provide the control signal to the VCO.

The application circuit, Figure 2, indicates a series RC to ground on pin 5 for the loop filter. The values will give a lock time of less than 3ms, smaller capacitor values will increase the loop bandwidth and decrease the lock time. The lock time is also a function of the VCO resonator setting since the fastest lock time results when the VCO resonator is set to resonate at just above f_o with the loop control voltage set at V_{CC}/2. The VCO sensitivity is about 25MHz/V and the phase detector sensitivity is about 0.4μA/degree.

The modulation input is designed to be driven by a logic level, 0V or V_{CC}. The maximum modulation frequency is 500kHz and a series resistor can be used to reduce the frequency deviation. The modulation is applied to an internal varactor in the VCO, therefore the PLL will correct the frequency offsets caused by the modulation unless the loop bandwidth is narrow enough.

THE RF9902 RECEIVER

This part contains the input amplifier, mixer, IF limiting amplifier, phase detector, and an output Schmitt trigger to generate the FSK digital signal as shown in Figure 3. There are two sections to the chip; one section performs the downconversion from the RF to IF frequency while the second amplifies and demodulates the IF signal. A typical application circuit for use at an

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IF=20MHz is shown in Figure 4.

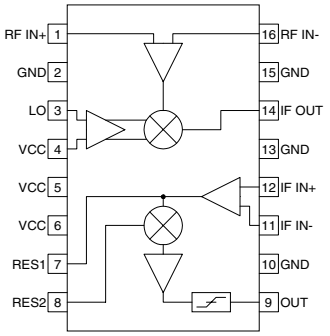


Figure 3. RF9902 Functional Block Diagram

RF Amplifier and Mixer

A differential RF amplifier and Gilbert cell mixer form the basis of the downconversion section. The RF input requires a DC blocking capacitor and can be brought in on pin 1 or pin 16. The unused pin should be AC grounded at the package. This front-end section has typically 18dB of gain and a noise figure of around 7dB. The 1dB input compression point is -22dBm and the input IP3 is -10dBm. The RF input VSWR is less than 1.5:1 across the operating frequency. The IF output impedance is 500Ω and the pin has to be loaded with a coupling capacitor or a filter with a high DC resistance.

IF Section

This section has an IF amplifier, limiting amplifier, FM demodulation circuitry, and a Schmitt trigger. The IF signal from the mixer is filtered externally and amplified to provide the required drive level to the limiter. The differential IF amplifiers have about 90dB of gain. The function of the limiter is to remove amplitude variations from the IF frequency since the FM detection circuitry will attempt to demodulate any amplitude variations in addition to the required frequency variations. This would decrease sensitivity and increase the distortion in data signal output.

The IF input impedance is 500Ω and pin 11 is the complementary input. Pin 11 should be bypassed to ground with a capacitor as close to the package as possible. There should be no DC path between the mixer output and IF input.

FM Demodulation

The FM demodulation is accomplished by a quadrature detector consisting of an analog multiplier and an external quadrature tank circuit. The multiplier can be easily implemented on chip and discrete components can be used for the quadrature tank.

The limiter signal is split into two and applied differentially to the lower transistors in the multiplier and also to the upper transistors via the external phase shift capacitor as shown in Figure 4. The two signals are at the same frequency but have a 90° phase difference at the carrier frequency and the multiplier acts as the phase detector.

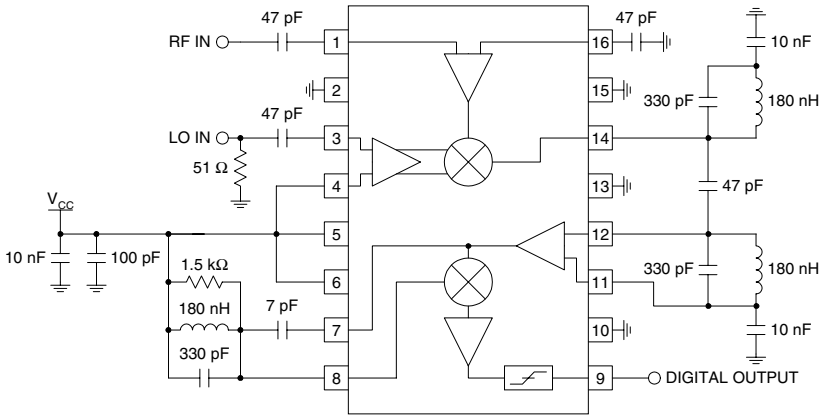


Figure 4. RF9902 Application Schematic

The external quadrature tank circuit should have a connection to V_{CC} for internal biasing purposes. The tank circuit provides the 90° phase shift at the carrier frequency and a linear phase shift on either side of the carrier. It is the relative phase shift versus frequency which determines the modulation state of the signal. The Q of the tank circuit should be such that the 3dB bandwidth is approximately equal to the modulated frequency shift of the carrier. Wider bandwidths are possible provided that the peak-to-peak phase shift is at least 45°. High Q components should be used since the shunt resistor can always be adjusted to lower the Q.

The digital output indicates the modulation state of the carrier input. It is a logic signal which when low is equal to 0V and when high is equal to V_{CC} indicating positive modulation. The Schmitt trigger helps in restoring the shape of the demodulated digital output.

The RF9902 draws 25mA at a V_{CC}=4V and has an RF sensitivity of at least -80dBm for an IF=30MHz. Higher IF frequencies may lead to a degradation in sensitivity. An external LNA, or gain block such as the RF2304, with at least 10dB of gain and an image noise filter between the LNA and RF9902 input should be used for maximum sensitivity applications.

Circuit Board Layout for the RF9901 and RF9902

The ground pins should be connected directly to the PCB ground plane as close to the package as possible. The V_{CC} pins should be bypassed to ground directly at the package and any decoupling capacitors on the board should have a direct return to ground.

The RF9902 receiver requires some extra care in the board layout to achieve sensitivity and maximize stability. The VCC must be bypassed with quality RF capacitors and the circuitry around the IF output and inputs must be bypassed close to the package. The PCB board must have a good double sided ground plane which runs directly under the part on both sides. This isolates one side of the part from the other. Although the functionality of pins 1 and 16 can be interchanged, it is recommended that pin 1 is used for the input signal. This will minimize any potential coupling between the RF and IF sections.

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Low-Cost HBT Upconverters for CDMA Transmitter ICs

To support the increasing demand for Code Division Multiple Access (CDMA), the latest digital communication technology in cellular industry, RF Micro Devices (RFMD) developed CDMA chip sets for both receiver and transmit chain. The CDMA chip sets were designed and manufactured on an advanced GaAs Heterojuction Bipolar Transistor (HBT) process from TRW. The HBT process offers several advantages over other processes such as high Ft, low noise transistors, and process consistency. The CDMA program is two-fold: The first chip set, which was designed for cellular band, consist of a Receive and a transmit IF AGC Amps(RF9907 and RF9909), a Receive LNA/ Mixer(RF9906), and a Transmit Upconverter(RF9908); the second chip set, designed for PCS band, consist of a Receive LNA/Mixer (RF9936) and a Transmit Upconverter(RF9938). This paper describes the two Transmit Upconverters for this CDMA program.

Design architecture is the same for both cellular and PCS designs. The PCS upconverter, RF9938, is a modified RF9908 with performance optimized for the PCS band. Both ICs operate at 3.6V_{DC} with 0dB conversion gain.

With -10dBm input at the IC, typical Adjacent Channel Power Rejection (ACPR) for the RF9908 is -37dB for the 880KHz offset and -58dB for the 1.98MHz offset. The typical ACPR for the RF9938 is -43dB. The nominal power supply current for the RF9908 is 18mA and 25mA for the RF9938. The overall performance is affected by less than +/-1dB over temperature, frequency, and the LO drive level. Both ICs are pin compatible and are packaged in a standard 8-lead plastic SOIC package.

Figure 1 is a simplified circuit topology of the mixer. As shown in the figure, the mixer is a Gilbert Cell based multiplier with an IF amplifier at the bottom and the LO switching transistors at the top. Double balanced mixers such as this offers the best port to port isolation and low LO feed-through at the output. Minimum port to port isolation is 30dB for both upconverters and the minimum spurious signal in a 60MHz bandwidth is 50dBc.

Input ports for the IF and LO are configured for differential operation. However, the LO can be driven single ended if one of the input port is AC grounded. Input impedance for the IF amplifier is 265Ω, set by the inter-

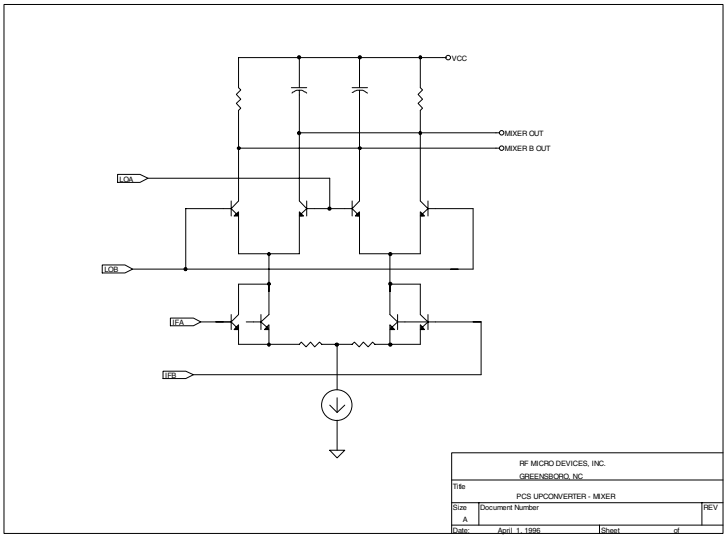


Figure 1. Simplified Circuit Topology

nal resistors. The LO input impedance is 50Ω. The IF amplifier portion of the mixer has a set of signal degeneration resistors on the transistor emitters. These resistors are designed to increase the mixer linearity by reducing the gain in the IF amplifier and keeping the signal level well below LO signals. Unfortunately, the same resistors also increase the overall noise figure. The resistor values were carefully calculated for optimal linearity and the noise figure. There are several design techniques used to improve the overall noise figure. First, the transistors in the IF amplifiers are doubled and paralleled. The paralleled transistors reduce r_b and r_e the transistors and reduces the overall noise figure. Second, a couple of capacitors are place on the collector of the mixer output transistors. These shunt capacitors act as low pass filters and reduce high frequency mixed spurious signals. Again, the values of these capacitors were carefully calculated to meet the conversion gain and linearity requirements. Third, a good bypass capacitor on the current mirror further reduces the overall noise figure.

The LO portion of the mixer contains a two sets of cross-coupled transistors to alternately turn the paired transistors on and off. Typically, an LO buffer amplifier (e.g. a limiting amplifier) is required to provide a sufficient voltage swing (ideally square waves) to drive the mixer. However, to conserve the overall current and to make the IC small, the LO buffer amplifier is omitted. The mixer is designed for an LO drive level of -6dBm or greater for best mixer performance.

The final stage of the ICs is a low noise RF amplifier. The RF amplifier takes the high impedance differential output of the mixer and converts it to a 50Ω single ended RF output. The RF amplifier is a push-pull class B amplifier where the current for each transistor flow for approximately one half of the input cycle and provides a different half of the overall signal. Since the current is only flowing one half of the time for each transistor, the required linearity can be met with about half of the current than classic “A” type amplifier.

One of the biggest advantages of CDMA technology compared to FDMA or TDMA is the capacity expansion. Unlike FDMA, where available spectrum is divided into 30kHz wide channels, or TDMA, time sharing of multiple users in 30kHz, in CDMA, multiple users share the same spectrum simultaneously. The limitation is not depended on the number of physical channels but on the channel condition. As the number of users increase, interference and the probability of higher data error rate will increase also. For this reason, the linearity requirements in CDMA is very demanding and important. The ACPR is a method of testing the IC linearity. It is a relative measurement of the energy in a 1.23MHz bandwidth CDMA waveform to the energy in the adjacent channels with a given offset (+/-880kHz, and +/-1.98MHz for Cellular systems and 1.25MHz for PCS systems). The following graphs show the typical ACPR performance of RF9908 and RF9938. Figure 2 is the RF9908 ACPR with +/-885kHz offset. Figure 3 is the RF9908 ACPR with +/-1.98MHz offset. Figure 4 is the RF9938 ACPR with +/-1.25MHz offset.

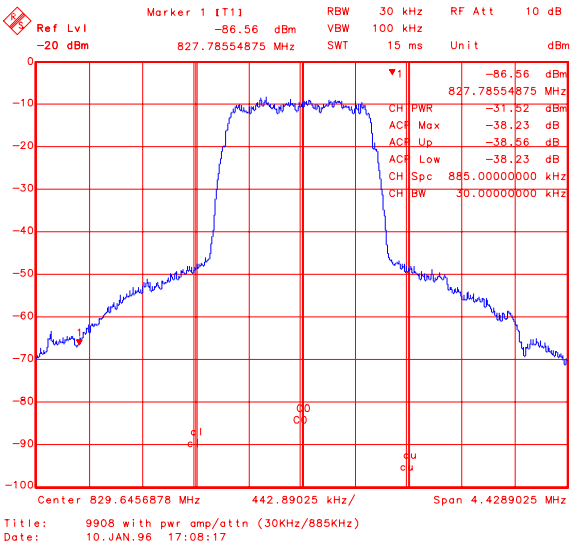


Figure 2. RF9908 ACPR at ±885 kHz Offset

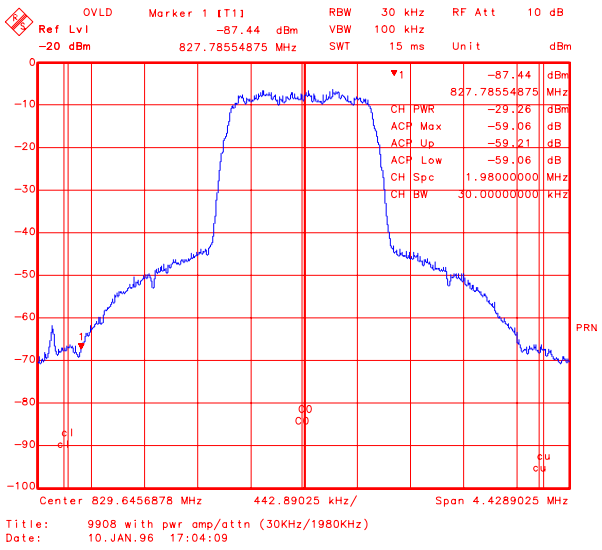


Figure 3. RF9908 ACPR at ±1.98 MHz Offset

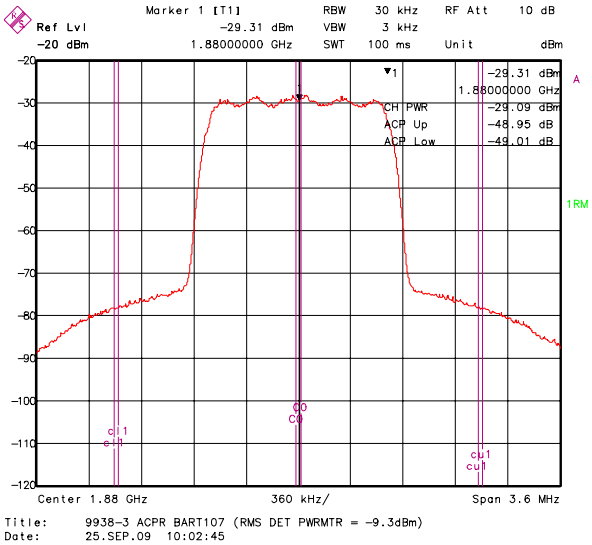


Figure 4. RF9938 ACPR at ±1.25 MHz Offset

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High Dynamic Range GaAs HBT LNA/Mixers for PCS Systems

Abstract
A family of fully monolithic GaAs Heterojunction Bipolar Transistor (HBT) LNA/Mixer products have been developed to address spread-spectrum Personal Communication System (PCS) applications in the North American 1930MHz to 1990MHz frequency band. Three products have been developed to provide low-cost solutions for high-performance RF products. The RF9936 family of products include monolithic LNAs that provide a typical gain of 13.5dB and an associated 50Ω noise figure of 1.4dB. Cascaded LNA/Mixer (including a 3.5dB loss image filter) gain is 26dB to 28dB, single-side band noise figure is typically 2.5dB, and input third-order intercept point (IIP3) ranges from -11dBm to -14dBm (product dependent). All three products are available in low-cost plastic packages to support commercial/ consumer wireless applications.

PCS Spread Spectrum Systems

Unlike the 900MHz U.S. cellular frequency band, devices designed for 1900MHz Personal Communication Systems (PCS) will predominantly utilize some form of spread-spectrum multiple access method. Code Division Multiple Access (CDMA) and Time Division Multiple Access (TDMA) are two such competing spread spectrum technologies approved for use in the 1900MHz PCS frequency band. Both access methods offer advantages over analog Frequency Division Multiple Access (FDMA) systems. The performance advantages of these next generation spread spectrum systems include increased channel capacity (more users per MHz), reduced susceptibility to multipath fading, intrinsic communication link security due to digital coding, and extended operating time in battery operated products. While many of the performance advantages of these spread-spectrum techniques are realized through digital modulation and digital signal processing techniques, high performance RF components must be applied in these systems to realize the theoretical benefits in real world applications. Increased system channel capacity is one spread spectrum performance advantage that can be limited by the performance of the receiver's RF front-end. Maximizing the dynamic range of the spread-spectrum receiver at 1900MHz requires selection of a robust technology for active devices that simultaneously achieve low noise and high levels of linearity. In portable wireless products, it is particularly important to achieve low noise, highly linear active device performance at DC bias levels that can be supported in battery powered products.

Receiver Dynamic Range Issues

Optimizing the dynamic range of any receiver requires careful management of the intercept point and noise figure of the various components used in the receiver design. In most applications, the LNA/Mixer generally limits the useful dynamic range of the receiver. The spurious-free dynamic range (SFDR) is a useful quantity for receiver designers because it provides a figure-of-merit indicative of the receiver's ability to receive signals near or at the minimum detectable level in the presence of interference (usually from adjacent channels). The SFDR of a receiver is defined as the difference in dB between the receiver noise floor (usually the noise power in the detection bandwidth) and the level of two equal signals that produce an intermodulation product equal to the noise power in the detection bandwidth. The SFDR can be related mathematically to the n-order input intercept point, thermal noise in the detection bandwidth, and receiver noise figure. The two-tone third order intercept point relation is used most often because third order distortion products are generally most likely to fall inside the receiver detection bandwidth. It can be derived that the SFDR of a receiver is related to the two-tone third order input intercept point (IIP_3) by the following equation:

$$SFDR = 2/3[IIP_3 + 174 - NF - 10\log(BW)] \text{ dB}$$

IIP_3 = Two-tone third order intercept point referred to the receiver input

NF = Receiver Noise Figure

BW = Detection BW

Since the receiver detection bandwidth (BW) is primarily dictated by issues unrelated to LNA/Mixer performance (usually modulation type and frequency tolerances), LNA/Mixers that simultaneously minimize noise figure and maximize intercept point optimize the useful dynamic range of receivers.

Receiver Linearity Issues

A block diagram of the RF portion of a typical CDMA spread spectrum handset is shown in Figure 1. CDMA handsets operate full duplex. Therefore, a duplexer is used to avoid receiver interference from the transmitter.

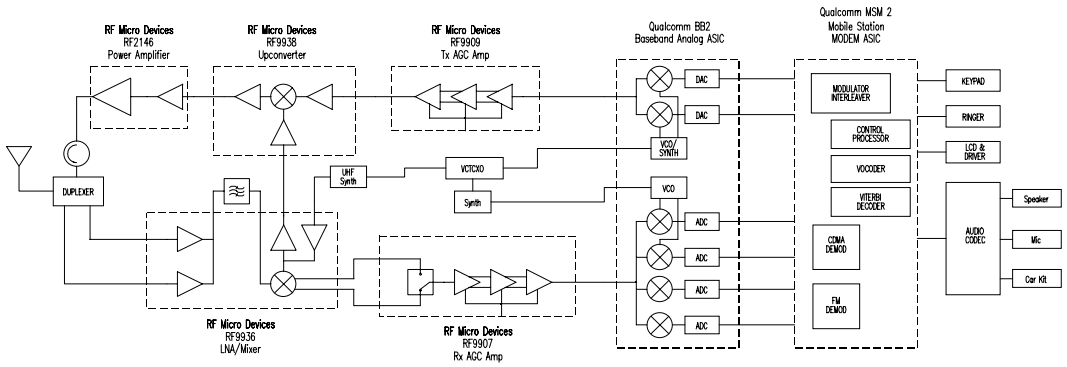


Figure 1. Typical CDMA Handset block diagram

Since the duplexer can not completely filter the transmitted signal, the receiver's LNA may see relatively high out-of-band power levels at its input from the transmitter. Depending on the rejection of the duplexer and the distance of the user from the base station, the power level that leaks into the receiver input can be many dB higher than the received input signal. This operating condition drives the linearity (IP3) requirements of the LNA. If the LNA is not sufficiently linear, the potential exists for receiver desense and/or cross modulation distortion from the transmitter on the received signal. A full-band image filter follows the LNA in the receiver cascade. Since many dB more of additional attenuation of the transmit band signal is provided by the image filter, the linearity requirements of the mixer are driven primarily by adjacent channel interference considerations rather than transmit band interference.

In spread spectrum systems, the total power at the receiver input is spread over the entire channel bandwidth. Although the average channel power transmitted per user per hertz is lower than narrowband systems, the total channel power in either system is equivalent. Since more users are intended to occupy adjacent channels, the potential for adjacent channel interference may actually be higher in spread spectrum receivers as compared to narrowband systems. Figure 2 presents this classical adjacent channel interference scenario for a 1.25MHz CDMA channel allocation. The third-order intermodulation distortion product of two adjacent channels (1960, 1958.75MHz) falls directly in the channel bandwidth of the third channel (1962.5MHz). Since the RF front-end passes the entire receive band, the total adjacent power from all users must be used to determine the linearity requirements of the RF front-end. If the RF front-end is not sufficiently linear, the systems channel capacity will be degraded. The potential for third-order intermodulation distortion can be reduced in the IF electronics if the adjacent channel is rejected sufficiently by the channelizing filter that follows the RF mixer.

Receiver Noise Figure Issues

PCS spread spectrum receiver noise figure considerations are no different than those of any other receiver. Lower RF front-end noise figure in the handset allows the receiver to operate reliably at increased distances from the base station. The RF front-end must also have sufficient gain to establish the overall noise figure of the receiver. As was mentioned in the previous section, channelizing filters are often used at the RF mixer output. Due to the relatively high IF, SAW filters are the technology of choice in CDMA hand-sets. While SAW filters do an excellent job establishing the receiver's operating channel, high out-of-band rejection performance requirements often produce multi-resonator designs that have insertion loss that exceed 10dB. This places additional pressure on the gain and noise figure that must be achieved in the RF front-end.

Active RF Component Technology Selection

At RF Micro Devices, we utilize Optimum Technology Matching™ to select the appropriate IC technology to satisfy the technical requirements of our products at the lowest cost. Optimum Technology Matching™ means that we consider all IC technologies at our disposal (GaAs HBT, GaAs MESFET, Silicon Bipolar) on an application-by-application basis. For our PCS LNA/Mixer products, the technology selected for these products is GaAs HBT. GaAs HBT was selected over GaAs MESFET and Silicon Bipolar in these products primarily for the due to the superior spurious-free dynamic

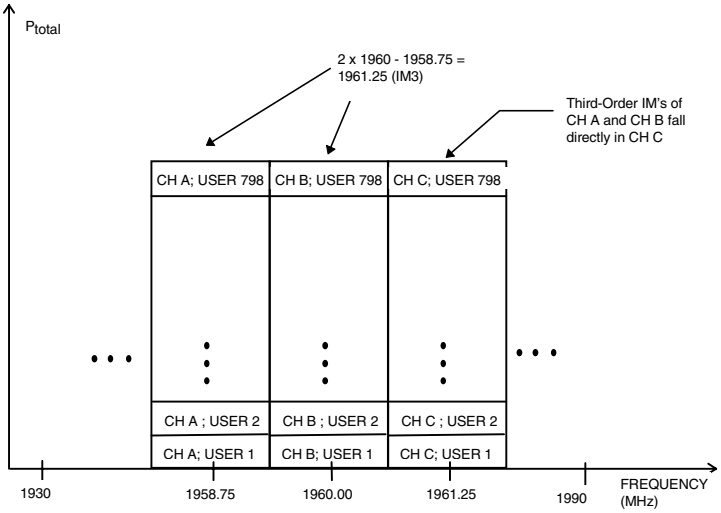


Figure 2. Third-order intermodulation distortion products can produce interference in LNA/Mixers that lack adequate linearity.

range that can be achieved in LNA/Mixers operating at the 1900MHz PCS frequency band under the same DC bias conditions. In comparison, GaAs MESFET's are more non-linear than GaAs HBT's due primarily to the inherently non-linear output conductance of the MESFET. Source degeneration in the MESFET can be used to linearize these devices, but due to the lower transconductance of the MESFET, both the gain and noise figure suffer in these high performance applications. On the other hand, silicon bipolar devices have similar transconductance characteristics to GaAs HBT's, but exhibit additional distortion characteristics primarily due to non-linear base collector capacitance [1]. Another major difference between the GaAs Heterojunction bipolar and the Silicon homojunction bipolar is that the base of the HBT can be much more heavily doped than the emitter. The effect of the additional base doping is a reduction in the base sheet resistance by as much as two orders of magnitude [2]. Since the base resistance is a major contributor to bipolar device noise, the result is an inherently lower noise device.

PCS LNA/Mixer Products

Over the past two years, a family of PCS LNA/Mixer products have been developed to support development of PCS CDMA handsets by Qualcomm, Inc. of San Diego, CA. Part pinout block diagrams for the RF9936, RF9976, and RF9986 are shown in Figure 3.

The RF9936 was the first PCS LNA/Mixer developed at RFMD. The RF9936 includes two selectable LNAs that share a common output, an variable gain low noise amplifier, an active balanced mixer, a LO isolation buffer, and a switchable LO buffer. The RF9936 was architected with two LNAs to interface to two half-band duplexers. The LNAs provide 13.5dB of gain with an associated 50Ω noise figure of 1.4dB typically without source tuning. Due primarily to the linearity of the GaAs HBT device, the LNA/Mixers achieve an OIP3 of +16dBm and consume a modest 5mA @ 3.6V. The spectrum for a two-tone third-order intercept point characterization of the LNA is as shown in Figure 4.

Another feature provided by the RF9936 is a low noise variable RF gain amplifier. Using an analog control input voltage, the power gain of the part can be adjusted more than 10dB. This is accomplished by a monolithic PIN diode network (positioned prior to the active mixer) in conjunction with IP3 optimized DC current steering. The measured two-tone, third-order input intercept point (IIP3) of the part as a function of cascade power gain is shown in Figure 5A. As can be seen in the figure, the cascaded IP3 referred to the input of the part (IIP3) can be increased with a corresponding reduction in gain. Also plotted in Figure 5B is the cascaded noise figure as a function of gain control. Both the measured IIP3 and noise figure shown in Figure 5A & 5B include the effect of an interstage

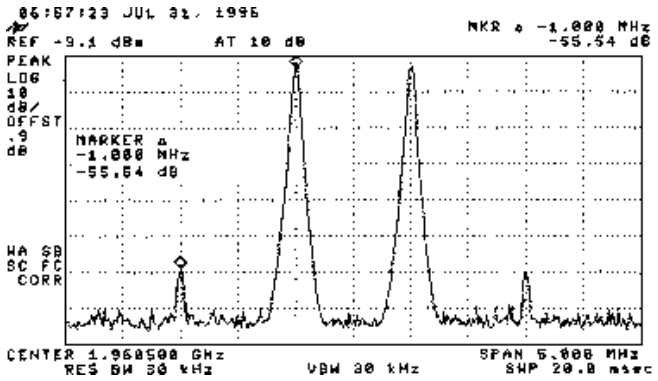


Figure 4. The LNA's Measured OIP_3

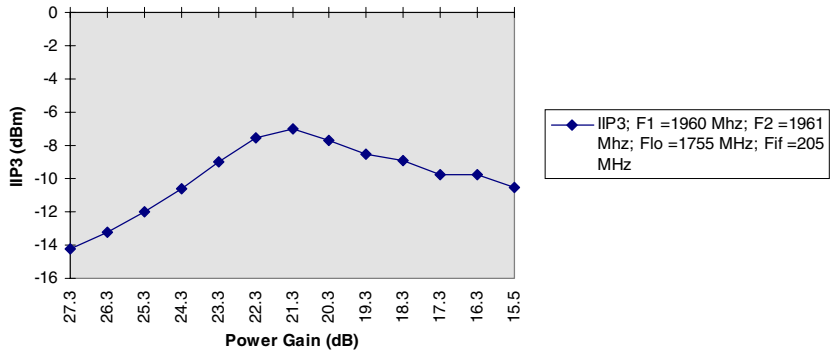


Figure 5a. Measured IIP_3 versus Power Gain for the RF9936

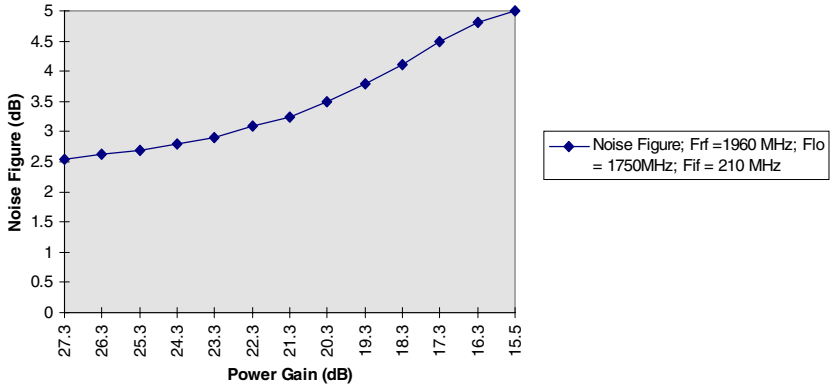
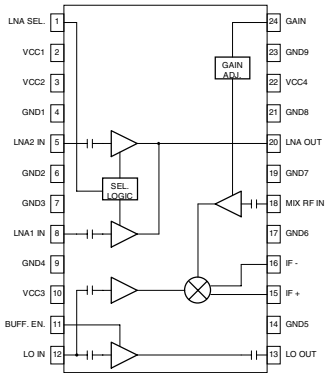


Figure 5b. Measured Noise Figure versus Power Gain for the RF9936

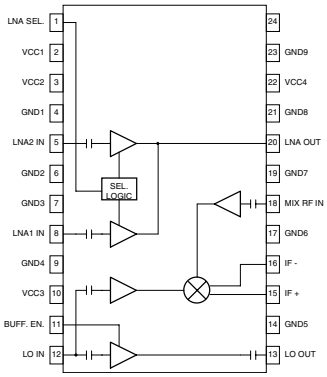
SAW image filter that passes the 1930MHz to 1990MHz PCS receive band. In order to minimize the number of external components, on-chip DC blocking capacitors are included on all RF I/Ohs except for the LNA output. The RF9936 provides a balanced IF output impedance of 1KΩ to interface to a balanced SAW or high impedance filter. IF chokes are required at the output of the part to supply bias to the mixer. Two monolithic LO buffer amplifiers are provided on the RF9936 as well. One buffer is used to provide additional isolation between the LO port of the mixer and the RF input port. The second buffer is switchable and is used to buffer the LO into the transmitter's upconverter, or the PLL prescaler.

The RF9976 differs from the RF9936 in that the OIP3 of the part is 2dB higher and is typically +15dBm. The RF/IF conversion gain is also 1dB higher than the RF9936. No gain control is provided in the RF9976. Other AC performance parameters and functionality are equivalent to the RF9936. The additional 2dB of OIP3 comes with an additional 8mA of DC current consumption. A complete performance summary for the RF9976 is provided in Table 1.

RF9936



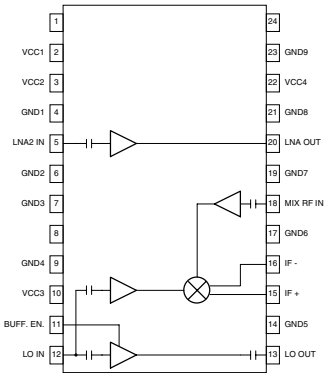
RF9976



-No Gain Control

IP3I: ~1 dB Higher than RF9936

RF9986



-No Gain Control

-Single LNA

IP3I: ~3 dB Higher than RF9936

Figure 3. The RF9936, RF9976, and RF9986 PCS LNA/Mixers provide feature and performance options in low-cost, pin-for-pin compatible packages.

Parameter	**RF9936**	**RF9976**	**RF9986**
LNA Gain	13.5 dB	13.5 dB	13.5 dB
LNA Noise Figure	1.4 dB	1.4 dB	1.4 dB
LNA IIP3	+5.5 dBm	+5.5 dBm	+5.5 dBm
LNA/Mixer Gain*	27 dB	28 dB	26 dB
LNA/Mixer Noise Figure*	2.5 dB	2.5 dB	2.5 dB
LNA/Mixer IIP3*	-14 dBm	- 13 dBm	-11 dBm
Gain Control Range	12 dB	N/A	N/A
DC Power	42 mA @ 3.6V	50 mA @ 3.6 V	50 mA @ 3.6V
Package	QSOP-24	QSOP-24	QSOP-24

* Cascaded Gain/NF/ IP3 performance parameters include a 3.5 dB insertion loss image filter between the LNA and mixer.

Table 1. The RF9936, RF9976, RF9986 provide three design options for PCS LNA/Mixers

The third LNA/Mixer in the trilogy is the RF9986. The RF 9986 is a single LNA/Mixer without gain control. The gain of the RF9986 is 1dB lower than the RF9936 with an equivalent cascaded noise figure. The OIP3 is equivalent to the RF9976's +15dBm. The RF9986 provides the highest IIP3 of the three parts. The typical IIP3 for the RF9986 is -11dBm. Like the RF9976, no gain control is provided in this part. A complete performance summary of the RF9986 is provide in Table 1.

Conclusion

For 1900Mhz PCS applications, three unique HBT LNA/Mixer products have been developed that achieve wide dynamic range for high performance commercial applications. These products were developed for CDMA handsets, but offer designer's using other multiple access techniques the opportunity to achieve peak performance in their wireless products. The RF9936, RF9976, and RF9986 are supplied low cost, QSOP-24 plastic packages in production quantities.

References

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2. J.A. Higgins, "GaAs Heterojunction Bipolar Transistors: A Second Generation Microwave Power Amplifier Transistor", Microwave Journal, May 1991, pp. 176-194.

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A Highly Integrated Receiver IC for Spread Spectrum Applications

Introduction

An integrated receiver has been developed which includes most of the circuitry needed for reception of a digitally modulated signal. The device is manufactured using a low-cost high-performance Silicon Bipolar process, and contains a RF front-end, IF amplifier with gain control and Received Signal Strength Indicator (RSSI), and a quadrature demodulator. The circuit can be used for 915MHz ISM band systems, or as a dual IF section in higher frequency and super-heterodyne systems. Since the intended applications are usually under size and cost pressure, the device is packaged in a small low-cost plastic SSOP-24 package.

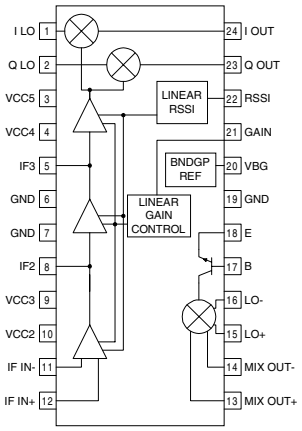


Figure 2. RF2903 Functional Block Diagram

Direct Sequence Spread Spectrum (DSSS) generally uses Phase Shift Keying (PSK) to modulate the carrier. The two most common forms are Quadrature PSK QPSK and biphase PSK (BPSK). BPSK modulates one bit at a time on the carrier, by setting the carrier phase to either 0 or to 180 degrees. QPSK modulates two bits at a time, one bit on the In-phase (I) channel, and the other bit on the Quadrature (Q) channel. This results in phase modulation in 90 degrees increments. Though the modulator for BPSK is simpler than for QPSK, the receiver needs to have a quadrature demodulator in both cases to resolve frequency offset and channel distortion between the transmitter and receiver. Amplifiers in those systems need to be linear to handle interfering signals without deteriorating the system performance (measured by the Bit Error Rate).

Because of the flexibility chosen in the chip architecture the device can also be used as a FM or ASK receiver.

Architecture

A block diagram for a basic Spread Spectrum receiver is shown in Figure 3. The RF2903 contains the RF front-end with RF Amplifier and Downconverter, three IF amplifier stages with linear gain control and RSSI, and a quadrature demodulator. Each of those functions will be described in more detail below. Components that are not included on-chip are the filters, the Local Oscillators, and the Base Band processing. The Gain Control is set by the Base Band Processor to such a level that the system is operating linearly, and no jamming by interferers can occur. The RSSI output of the RF2903 can be used as a "signal present" indicator, or as a coarse input for the gain control loop. In case there is no in-band interference expected the gain control may be fixed at the maximum level.

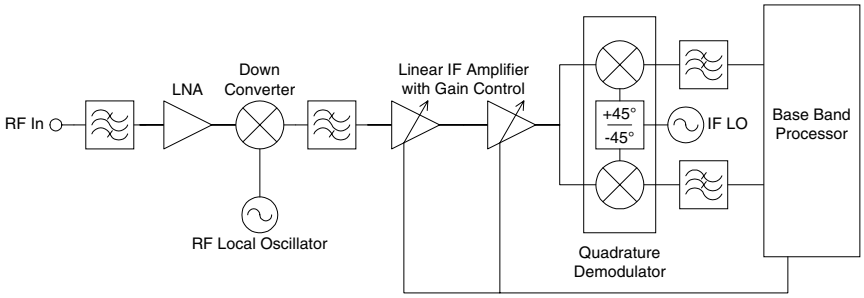


Figure 3. Typical Direct Sequence Spread Spectrum Receiver Architecture

Front End With RF Amplifier And Downconverter

The RF Amplifier and mixer are implemented as a differential amplifier with the RF signal modulating the current source in the common leg, see Figure 4. The current source also serves as the LNA. One of the differential inputs is normally terminated or connected to V_{CC} when a single ended input signal is used. The current through the current source is set by the base voltage that is externally provided (usually using the internal bandgap reference) and the value of the emitter resistor. The typical current in the current source is 5mA.

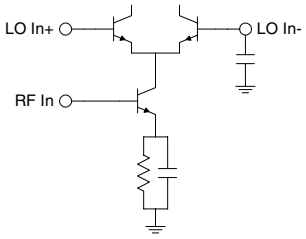


Figure 4. The Front End Circuit

RF2903 Pre-Amp/Mixer Power Gain vs. Frequency (Load=1k)

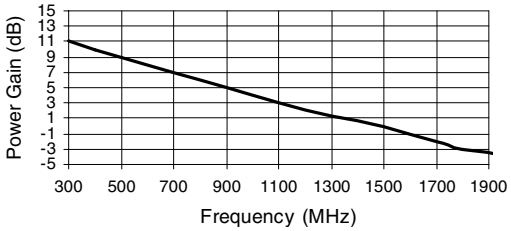


Figure 5. Front-End Gain

To obtain maximum flexibility in the system design the front-end can be configured in different ways. In case the RF input is directly at the RF2903 the LNA/Mixer should be configured for maximum gain and lowest noise figure. This is achieved by a common emitter configuration as shown in Figure 7. To increase system sensitivity one may choose to use an external LNA, and improve the overall noise figure. In this case, it is more important to obtain a high IP_3 in the LNA/Mixer. The common base configuration of Figure 6 achieves this, with the IP_3 being about 10dB higher than in the common emitter configuration but with higher noise figure and lower gain.

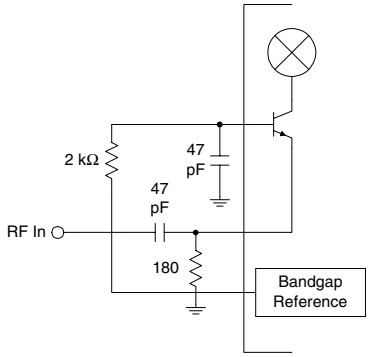


Figure 6. LNA in Common Base Configuration

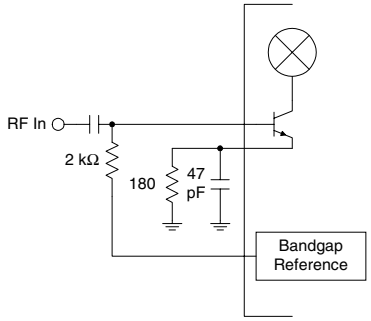


Figure 7. LNA in Common Emitter Configuration

IF Amplifier With Linear Gain Control And RSSI

The IF section consists of three identical gain stages, each with gain control and a Received Signal Strength Indicator (RSSI) detector. One of the goals in the IF section design was a linear gain control (measured in dB/V). This was achieved by putting gain control in all stages, being controlled by a segmentation amplifier. When the RF2903 is used in a linear system, for example a Direct Sequence Spread Spectrum receiver, the gain control will be used to keep the signal levels throughout the system such that no clipping occurs, even when a strong in-band interfering signal is present. When this device is used in a system where no linearity is required, for example a FM or Frequency Hopping receiver, the gain can be set to the maximum value at all times. The RSSI is than an indicator for the received signal strength.

To avoid amplification of DC offsets throughout the device, the output each of each stage is normalized at

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VCC through an external inductor to VCC. With this approach the external LC resonator also serves as a bandwidth limiting filter, to avoid that the amplifier gets saturated by wide band noise in the high gain region.

Amplifier Stages

Each of the IF stages is made up of two differential pairs put in parallel, see Figure 8. One differential pair has high gain, while the other has low gain because of the emitter resistors. The gain control of each stage is achieved by gradually turning on one pair, while the other pair is gradually turned off. The actual gain of each stage is depending on the Q factor of the external resonator. A lower Q results in a lower equivalent parallel resistor, and hence in lower gain. The output of each stage is internally connected to the input of the next stage, and one pin is used for the power supply and bandwidth limiting for each stage.

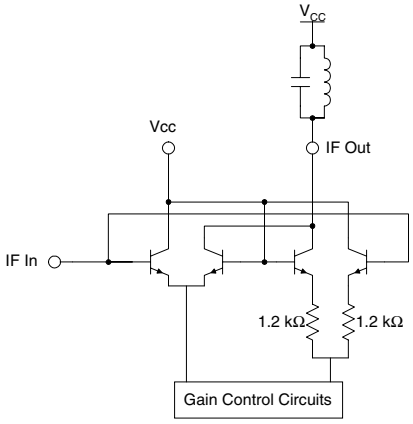


Figure 8. A single IF Amplifier Stage

The first and last stage have slightly different interconnections. The first stage has a balanced input, hence the complementary input is not connected to VCC as shown, but has a separate pin instead. The output stage has a balanced output, which goes through a buffer amplifier to the mixers.

The maximum gain in each amplifier stage is about 23dB, with an additional 25dB in the buffer amplifier and demodulator.

Gain Control

The gain control is achieved by turning on one pair, while turning off the other pair of the IF amplifier stage described above. Because the outputs of the pairs are open collectors, hence current sources, current adding occurs at the output. This means that the gain control can be done by putting more current into one pair while reducing the current in the other pair. Another differential amplifier as shown in Figure 9 is used for controlling the current into each differential pair. There are three of those amplifiers, one for each stage. The VBG' voltage determines at which control voltage that stage comes into action. In this way sequencing of the gain stages is achieved to optimize the dynamic range of the IF section. When the voltage is slowly increased, the first stage is turned on first, then the second stage, and as last the third stage. Because there are no capacitors besides parasitics in the circuit, the response time is very fast. The gain can be changed over the full range within 100ns, while no ringing or overshoot occurs.

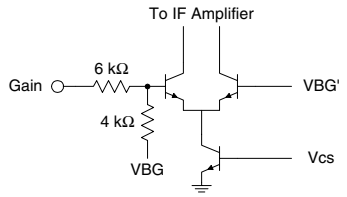


Figure 9. The Gain Control Circuits

VCS is derived from the bandgap voltage to set the current into each amplifier. The bandgap reference is used to obtain maximum temperature stability and minimize the effects of manufacturing process variations.

RSSI

The RSSI signal is obtained by rectifying the signal at the output of each stage, then summing those signals. Because the signal level is measured at the output of each stage, the RSSI vs. input power response changes when the gain control voltage is changed. This needs to be taken into account when designing a feedback loop that uses the RSSI signal to set the gain control voltage to maintain a constant output signal. The RSSI output is an open-collector PNP transistor, and an external resistor of 3kΩ is recommended. A capacitor to suppress IF signal should also be connected to the RSSI output and determines the actual response bandwidth, which potentially can be as high as the IF frequency itself.

Quadrature Demodulator

The quadrature demodulator consists of two Gilbert Cell mixers which are both driven differentially by the IF amplifier output, see Figure 11. The LO signals to the mixers need to be provided externally and should be 90 degrees out of phase. A phase splitter for this purpose is shown in Figure 12. This circuit achieves an accurate 90 degrees phase difference over a wide fre-

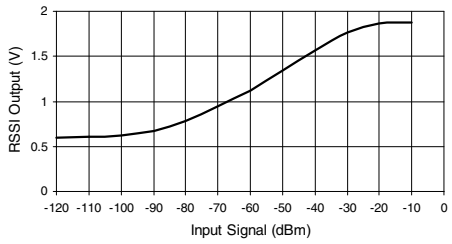


Figure 10. RSSI Characteristic at Maximum Gain

quency range, but introduces also an amplitude difference. This is no problem, however, because the LO inputs drive the mixers into saturation, taking out any amplitude difference between the I and Q LO signals. The only requirement is that the RC networks are matched to obtain an accurate phase shifting. The LO inputs are connected directly to the base of the input transistor, hence an external pull-up resistor is needed. The complementary LO inputs of the Gilbert Cells are internally connected to V_{CC}, hence the external DC voltage should be very close to V_{CC}. A 470Ω resistor to V_{CC} is small enough to achieve this, because the current into the inputs is very low.

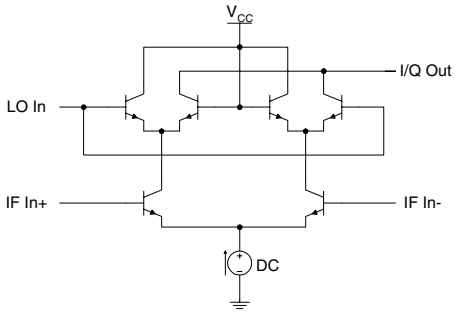


Figure 11. A Simplified Gilbert Cell Mixer

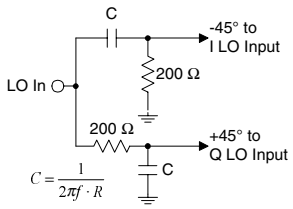


Figure 12. The Phase Splitter Circuit

The outputs of the Gilbert Cell mixers are buffered by an emitter follower such that the device can drive low impedance base band filters directly.

An on-chip bandgap reference is used for biasing all circuits. By doing this the performance of the chip is not sensitive for temperature and power supply voltage variations, and very consistent performance is achieved over the 2.7V to 5.5V range. The bandgap voltage is made available externally through a pin, and can be used for biasing the front-end as shown in Figure 6 and Figure 7, or for any other circuit in the system. The bandgap voltage is 1.63V and capable of driving up to 1mA.

Using The Device

Because of the high flexibility in the use of the device, many different circuits can be built using this chip. We will describe the three main configurations: the standard quadrature demodulator, an FM demodulator, and a configuration where the demodulator is bypassed.

Basic Application Schematic

The schematic for using the RF2903 with a quadrature demodulator is shown in Figure 15. The resonators are tuned for 50MHz, but may be scaled for any frequency up to 200MHz. Note that the biasing of the first amplifier stage is done through a resistor rather than through a resonator. A resistor can be used here because the bias is only for the base of the input transistor, it is not feeding the collector of an output. Hence the current is only a fraction of a milli-amp, and the voltage drop across the resistor is insignificant. The advantage of using an resistor instead of a resonator is to avoid inductive coupling between the stages, which could result in instability at higher gain settings.

Also worth mentioning is the choice of the mixer output and IF input pin. A single ended filter is used, thus the balanced mixer output and balanced IF section input can not be used. Only one output and one input is used, while the other is terminated. Pin 14 is used as the mixer output, and pin 11 as the IF input. It is also possible to use pin 13 and pin 12, but because the leads of those two pins run parallel inside the package a strong coupling exists between those pins. Since a filter is inserted between the mixer output and the IF input, it is crucial not to degrade the isolation. Measured isolation between pin 12 and 13 is 40dB, and between pin 11 and 14 better than 60dB. When high isolation is required it is recommended to use pin 11 and 14, rather than pin 12 and 13. The overall gain of this circuit is shown in Figure 14. The sensitivity in Figure 13 is measured with a signal bandwidth of 1MHz, based on a 0dB signal-to-noise ratio. This means that

if an actual system would have a signal bandwidth of 100kHz, the sensitivity would be 10dB better, while if a detection margin of 20dB is needed, the sensitivity would be 20dB less.

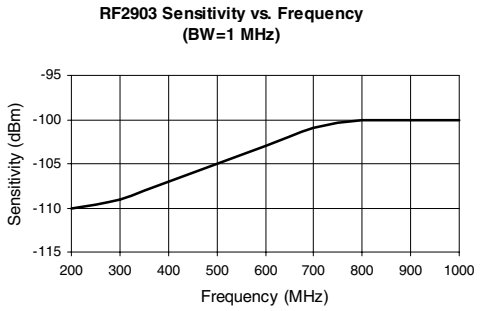


Figure 13. Receiver Sensitivity vs. Frequency

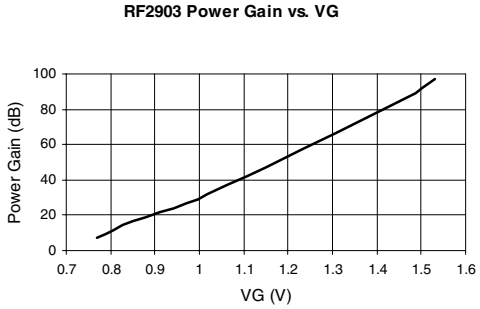


Figure 14. Overall Gain vs. Gain Control Voltage

FM Demodulation Circuit

The RF2903 can also be used as an FM or FSK receiver. The schematic for this configuration is mostly the same as shown before in Figure 15, but with a few changes in the configuration of the demodulator, see Figure 15.

The gain control can be set to maximum since no linearity in the IF section is needed. The I mixer is configured as straight-through by applying a DC signal to its LO input. This means that the IF signal from the IF section is multiplied by a DC signal (hence amplified), and the IF signal is available at the mixer output, see Figure 11. The IF signal is then phase shifted through an FM discriminator and applied to the Q mixer. Here the phase shifted IF signal is mixed with the IF signal, giving a DC output signal which is proportional to the phase difference between the two. Since the phase shifting in the quadrature tank is proportional with the frequency offset from the tank's center frequency, the demodulated output signal is a function of the instantaneous IF frequency.

Direct-Through Configuration

When no demodulation is needed at all, the mixers can be configured as regular amplifiers by applying a DC voltage to the LO inputs. When the DC voltage at the LO input in Figure 11 is less than V_{CC}, only one half of the differential pairs will be active and hence the IF signal is amplified and available at the I/Q output. The implementation of this circuit is shown in Figure 17.

When used in this configuration all the gain is accomplished at the IF frequency. Especially when the maximum possible gain of over 90dB is needed, attention needs to be paid to the layout and shielding of the circuit to avoid oscillations.

Board Layout

When designing a board layout for this device, some of

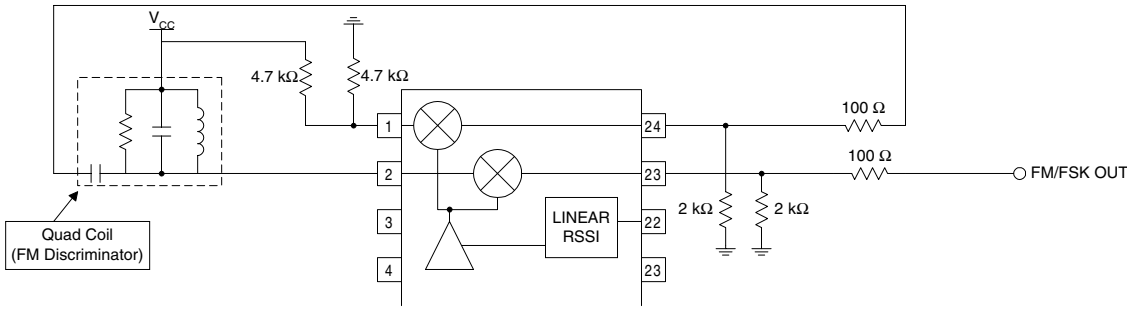


Figure 16. Detector Circuit for a FM or FSK Receiver

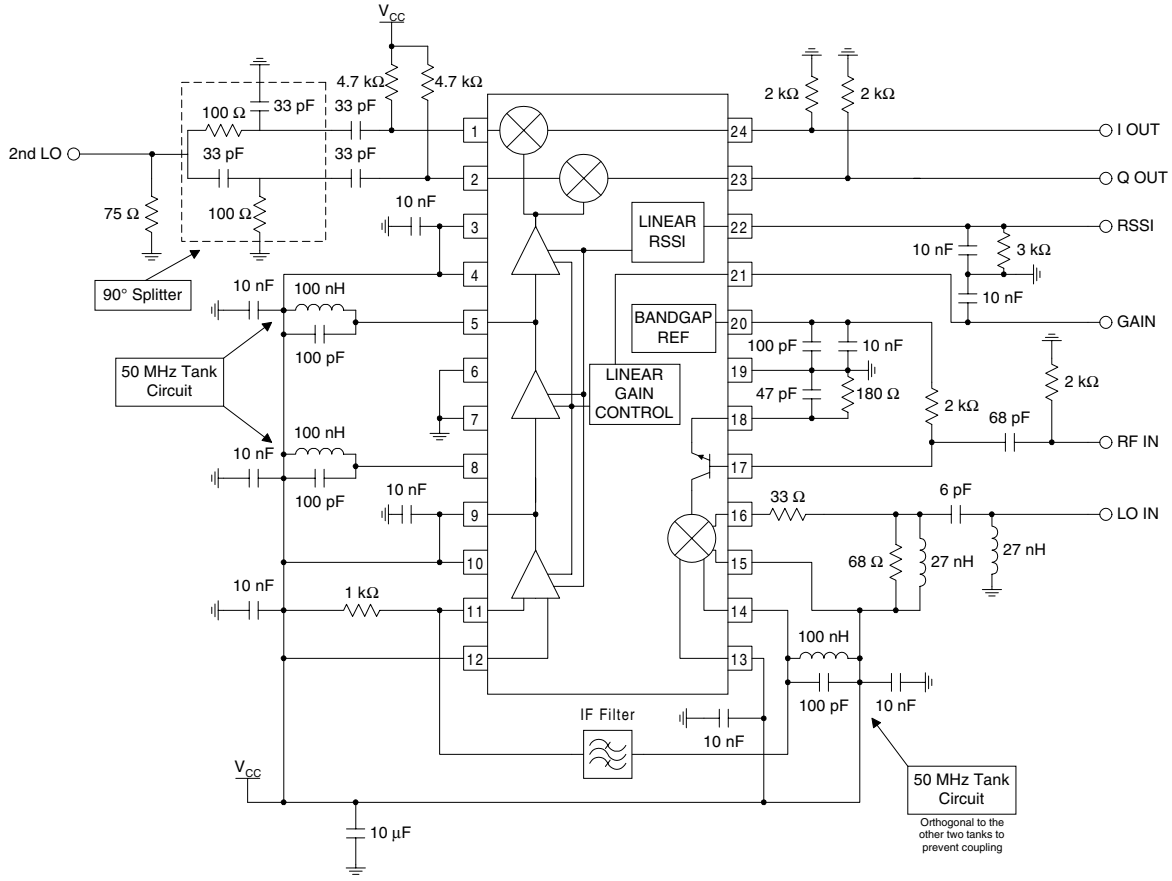


Figure 15. Basic Application Schematic for Quadrature Demodulation

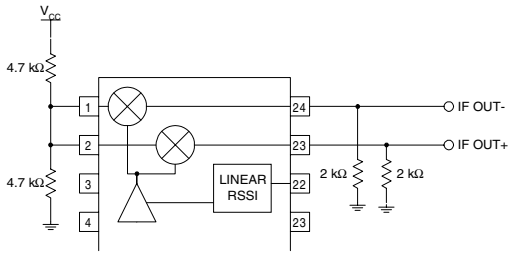


Figure 17. Used With IF Direct Through

the external circuits need special attention. To obtain maximum stability it is important that there is minimal feedback from the (interstage) outputs to the input. To achieve this the resonator tank circuits need to be orthogonal to minimize inductive coupling. Also, the spacing between the tanks should be as large as layout restrictions permit. The decoupling on the power supply pins should be done with a capacitor that has a series resonance frequency close to the IF frequency, and the capacitors should be mounted as close to the pins as physically possible.

When isolation between the mixer output and IF input is critical for e.g. image and spurious suppression, a slot in the ground plane of the PCB helps to minimize coupling due to ground currents. The slot should be at least 1mm wide and run lengthwise under the RF2903 such that the ground currents in the mixer circuit and the IF input pins are isolated. A proposed layout for the circuit is shown in Figure 18

Frequency Tuning

The device can be used over an IF frequency range of less than 100kHz to 200MHz. The low end of the fre-

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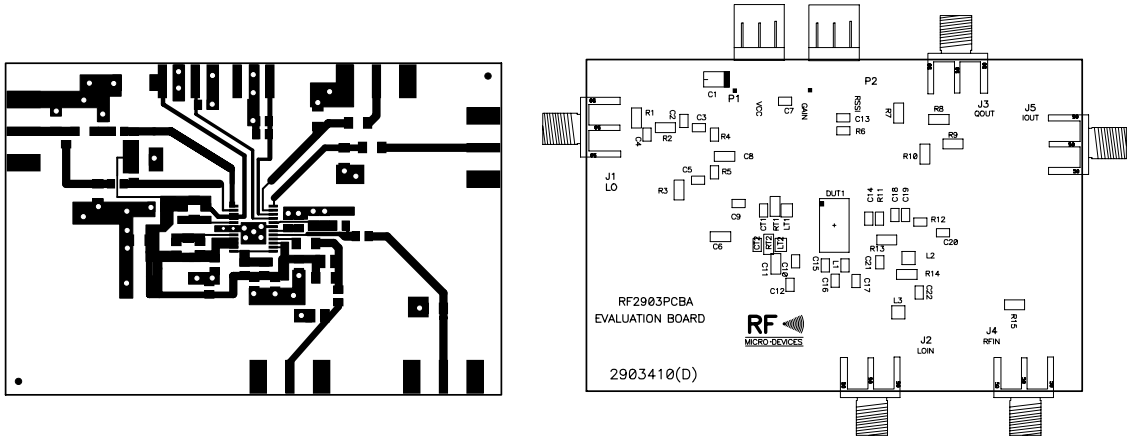


Figure 18. Layout of the Test Board

quency range is limited by the practicability of inductors for the tank circuits, while the high frequency limit is set by gain roll-off and increasing coupling on the board resulting in instability. Even though the device can operate over a wide frequency range, it is intended for narrow bandwidth operation. The bandwidth is limited by the tank circuits, and a wider bandwidth can be obtained with lower Q resonators, at the expense of maximum gain. The wider bandwidth also results in more noise power, which eventually will saturate the amplifier at higher gains, thus limiting the usable bandwidth depending on signal-to-noise ratio requirements. On the other hand, the bandwidth of the resonators should not be too narrow to avoid reduced gain caused by different frequency responses in the stages due to component tolerances. Too narrow band resonators will also result in very high gain, causing instability. This can addressed by damping the resonators by adding a parallel resistor to the tank circuits.

Conclusion

A highly integrated, very low cost receiver chip for DSSS and FM has been demonstrated. The device operates over a wide frequency range, and from a low battery voltage. The part is designed to be used in many different systems, and the flexibility in configurations makes the part suitable for several radio designs and architectures.

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Heterojunction Bipolar Transistor - Reliable, High Quality Solutions at a Very Low Cost

Heterojunction Bipolar Transistor (HBT) technology is an optimum solution for the demanding needs of today's commercial communication standards. Typical characteristics of HBT devices are high linearity and efficiencies, low phase noise, thermal ruggedness, and low cost. HBTs have a breakdown voltage greater than 20V which eliminates possible problems with overvoltage, making them ideal for battery operated applications. Their bipolar structure allows these devices to operate from a single positive supply. This lets the designer eliminate additional components, such as switching regulators, required by a dual supply operation typical of MESFET components. HBT devices are currently used in space applications as well as high volume commercial communications products in both the transmit and receive chains.

Yet even with such high acceptance, there are still some lingering perceived disadvantages associated with HBT. There are misperceptions that HBT devices have poor reliability, questionable performance repeatability in volume, and high device cost since the technology was initially intended for military use. To dispel these misperceptions the evolution of HBT must be understood.

During the early 1980s the US government approached manufacturers to develop a new technology for its military and space programs. GaAs/AlGaAs HBT technology was born. The initial crop of wafers appeared promising, demonstrating high gain. These devices were subjected to forward biased, accelerated life tests at high temperatures. The result of the bias/temperature stress on some devices was premature failure.

The failed devices experienced rapid DC current gain (β) degradation and increased turn on voltages (V_{BE}). Analysis revealed the failures were caused by a diffusion of positively charged interstitial beryllium, the p-type dopant, from the base into the base-emitter graded region where it could incorporate onto AlGaAs lattice sites. The β degradation was attributed to the creation of a potential spike in the conduction band at the emitter-base junction reducing electron injection. The increased V_{BE} was caused by an increase of the space charge region recombination and reverse hole injection as the beryllium approached the emitter. The findings were widely reported through a variety of articles published on the topic. HBT was labeled an unreliable technology with questionable repeatability. However, HBT research did not end here.

In the late 1980s TRW began to study methods of improving HBT reliability. Optimizing the structure and the wafer growth process became a primary focus. Several studies were conducted to understand methods for beryllium doping as well as ways to limit diffusion. TRW found that interstitial beryllium migration could be minimized through a combination of an increased As/Ga flux ratio and a reduction in the substrate temperature during growth of the wafer layers. The higher flux ratio reduces Be+ formation in a controlled method, lowering concentration and improving device stability. It was also determined that Molecular Beam Epitaxy (MBE) was the most ideal growth process. The MBE process is so precise that the wafer is grown one molecular layer at a time. The emitter, base, and collector layers are placed over the entire wafer evenly and at once. As a result no fine geometry photolithography is required to define the active region; requirements on mask alignment and optical resolution are greatly reduced. Utilizing this data, a new generation of high reliability, low cost HBT devices was born.

These new HBT devices are grown on a 3-inch semi-insulating substrate by using MBE. Silicon is used for the n-type dopant and beryllium for the p-type dopant. The devices are fabricated using a self-aligning ohmic metal process where a double photoresist liftoff technique aligns the base ohmic contact to within 0.15µm of the emitter mesa edge. The emitter and base mesa are formed by wet etch and boron implantation provides device isolation. An As/Ga flux ratio of 3:1 is utilized with a substrate temperature at approximately 570°C. The resulting profile is optimized for reliability.

This generation of HBT devices was subjected to accelerated life tests at high temperatures ranging from 220°C to 260°C. The failure criteria was established as 1dB degradation in gain from pre-lifetest levels. The devices grown using the TRW-defined method did not experience the failures of previous generations of HBT devices. A Mean Time to Failure (MTF) was calculated by Arrhenius's equation $MTF = Ce^{-Ea/kT}$, where C is a constant, Ea is the activation energy, k is Boltzmann's constant, and T is temperature in Kelvin. MTF was determined to be 4.6×10^7 hours at a junction temperature of 125°C, the equivalent of approximately

4,566 years. The devices proved that the method TRW developed for growing HBT wafers using MBE techniques yielded reliable and repeatable devices.

This same process produced the world's first space-qualified class "S" HBT components which are currently flying in space. It is a powerful testament to the reliability of these devices, as once an application is launched into space its components must function for decades in the harshest of environments. The same production line which fabricates the class "S' devices is utilized to fabricate commercial HBT devices.

Realizing the reliability issues an emerging HBT technology faced during its infancy 10 years ago had been solved, RF Micro Devices successfully transitioned HBT technology to the commercial marketplace. RF Micro Devices has used HBT technology to design components such as low noise amplifiers/mixers, quadrature modulators, demodulators, gain blocks, and power amplifiers with efficiencies up to 65%. For the past 4 years, these devices have logged over 1.5 million device hours under RF stress accelerated lifetests at junction temperatures of 250°C. In conjunction, TRW has been running accelerated DC lifetests which correlate with the RF stress test results. Today over 40 million hours MTF at 125°C junction temperature have been achieved.

HBT devices are currently used in hundreds of different applications ranging from cellular phones to wireless security systems to cable television system components. The list of applications grows every day as the benefits of this technology are discovered and utilized by the electronics industry. Since its introduction as a solution for the needs of wireless systems, GaAs/AlGaAs HBT technology has had a significant impact on communication systems designs. Through a powerful combination of high gain and efficiency that is best of any commercial solution currently available, HBT devices provide designers reliable, high quality solutions at a very low cost.

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The RF2411 General Purpose UHF Downconverter IC

Introduction

Communication receivers are constructed using a superheterodyne architecture. The received signal frequency is converted to a lower “intermediate” frequency (IF) in one or more steps for efficient amplification, filtering, and detection. The first downconverter circuit is often the primary determinant of overall receiver performance. This circuit typically consists of a band-limiting preselector filter (which may actually be the receive path of a duplexer), a low-noise amplifier (LNA), an image filter, a mixer, and a local oscillator.

The RF2411 is a monolithic integrated circuit UHF receiver downconverter which implements all of the RF functions of the required circuitry except passive filters and local oscillator in a 14-lead small outline plastic package. The block diagram of the device is included in Figure 1. It is suitable for general application in the

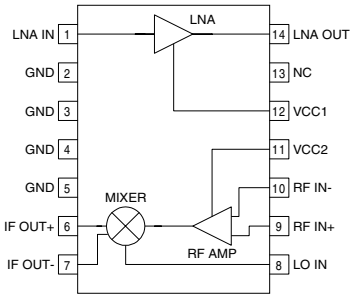


Figure 1: RF2411 Functional Block Diagram

500MHz to 1900MHz frequency range, at power supply voltages from 3V to 6V. Its high level of performance with a minimum of external components is a direct result of the advanced heterojunction bipolar transistor (HBT) IC process used. Broadband impedance matching at the RF ports and flexible IF interface simplify application to many receiver systems.

LNA Description

The LNA achieves broadband impedance match to 50Ω and low noise figure through internal feedback circuitry, not by use of external components. Input return loss is greater than 20dB and output return loss is greater than 10dB over the entire 1MHz to 1500MHz range. LNA gain slopes from 17dB at 1MHz to 11dB at 1500MHz, as plotted in Figure 2. LNA reverse isolation

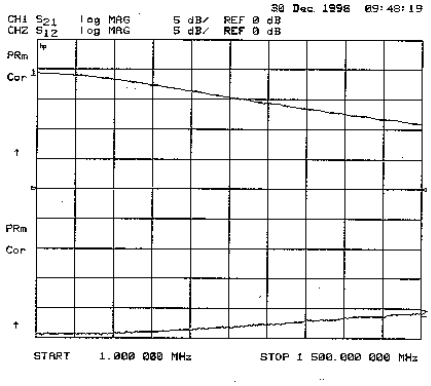


Figure 2: LNA Gain and Reverse Isolation vs. Frequency

is high over a the full frequency range, decreasing from 24dB at 1MHz to 21dB at 1500MHz. Noise figure is low and almost flat, increasing from 1.7dB at 500MHz to 2.4dB at 1500MHz, as plotted in Figure 3.

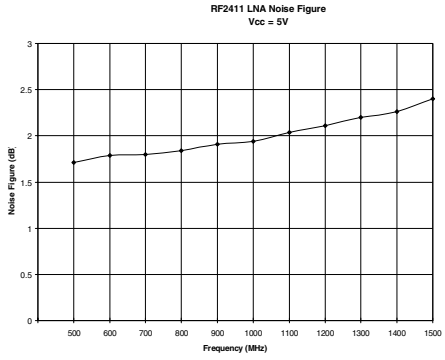


Figure 3: Noise Figure vs. Frequency

There is a dependence of LNA noise figure, gain, and IIP3 on power supply voltage at 880MHz. Gain can be seen to decrease from 14.6dB to 11.8dB as V_{CC} is reduced from 5V to 2.5V. IIP3 decreases from -1.75dBm to -11.6dBm, and noise figure decreases slightly from 1.88dB to 1.7dB over the same supply voltage range.

The excellent broadband impedance match insures optimum duplexer and image filter performance. In addition, the wideband gain, noise and isolation characteristics guarantee simple application to many UHF receiver systems.

Mixer Description

The RF2411 mixer is a double-balanced "Gilbert" type with differential IF output taken as open collectors for flexible IF interface. The RF input is typically matched to 50Ω system impedance using a single external series inductor, in this case 27nH, to cancel capacitive reactance. The LO input is internally matched over the full frequency range. LO input return loss increases from 11dB at 1MHz to 22dB at 1500MHz.

The doubly-balanced mixer delivers greater than 30dB LO input to mixer RF input isolation. LO input to IF output isolation is typically greater than 30dB over the 1MHz to 1500MHz range for differential IF interface. Mixer RF to IF isolation is typically greater than 25dB over the 400MHz to 1500MHz range.

Mixer conversion gain is dependent upon details of the IF interface. Power gain is directly dependent upon interface impedance. A 1000Ω interface impedance will result in 3dB more conversion gain than a 500Ω interface impedance, for example. Also, a differential interface will result in 6dB more gain than a single-ended interface at the same impedance level.

A differential interface can be through a balun transformer or directly to a differential SAW IF filter. Alternately, one collector may be tied directly to V_{CC} and output taken single-ended from the remaining output. In either case, maximum performance in typical application is obtained connecting the mixer collector(s) to V_{CC} through inductors resonant with the IF circuit capacitance, including circuit board trace and filter capacitance, so that the interface is entirely resistive at the IF frequency. The output capacitance of the mixer itself is less than 1pF per collector.

Figure 4 shows the dependence of mixer noise figure, gain, and IIP3 on power supply voltage at 880MHz RF and 965MHz LO (85MHz 1000Ω differential IF interface). Gain can be seen to decrease from 12.8dB to

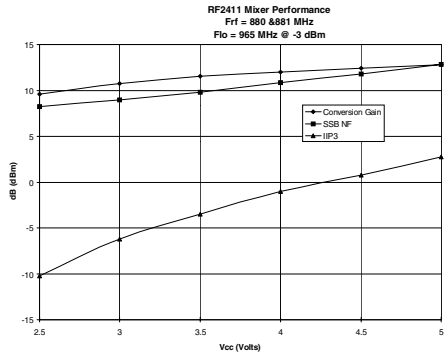


Figure 4: Mixer Gain, Noise Figure, and IIP3 vs. Supply Voltage

9.6dB as V_{CC} is reduced from 5V to 2.5V. IIP3 decreases from +2.8dBm to -10.3dBm, and SSB noise figure decreases from 12.85dB to 8.22dB over the same voltage range. This characteristic indicates best noise figure but poorer IIP3 and gain (and thus higher noise contribution from following components) at lower power supply voltage compared with V_{CC}=5V.

Figure 5 shows the dependence of mixer gain, noise figure, and IIP3 on LO input power (V_{CC}=5.0V, F_{RF}=880MHz and 881MHz, F_{LO}=965MHz, F_{IF}=85MHz, 1000Ω differential interface). Conversion

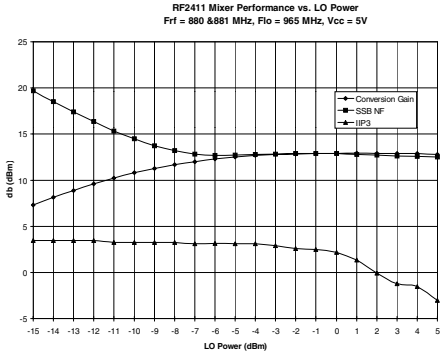


Figure 5: Mixer Gain, Noise Figure, and IIP3 vs. LO Power

gain and noise figure are only weakly dependent upon LO drive between -6dBm and +5dBm. IIP3 is maximum (+3.5dBm) at lowest LO drive, decreasing to 2.9dBm at -3dBm and more sharply to -3dBm at +5dBm LO drive. This characteristic indicates optimum

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mixer performance at LO drive levels between -7dBm and -4dBm.

Application Example

A typical application is diagrammed in Figure 6. Similar

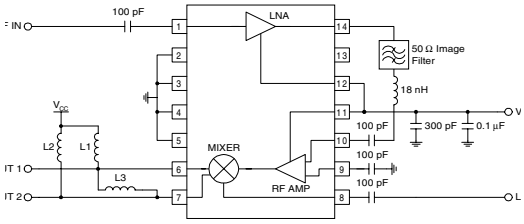


Figure 6: Schematic for Typical Application

to many cellular phone receiver applications, a monolithic image filter and interface to a differential IF filter are utilized. The IC RF ports are not blocked to DC by internal capacitors since the typical monolithic duplexer and image filters do not present a DC path. The only external components necessary in such an application are the series inductor at the mixer RF port, a broadband AC bypass at the IC V_{CC} pins, and the IF interface components. The IF interface components can be simply two chip inductors to power supply as shown, connecting to a differential input SAW IF filter such as the Sawtek 854596. The inductor value is chosen to resonate with filter and circuit board stray capacitance at the IF frequency. The mixer interface impedance is set by the filter input impedance in this example circuit, 1000Ω (differential) for the Sawtek filter. Alternately, impedance transformation may be included in the interface circuit to a higher impedance to increase conversion gain or to a lower impedance to increase mixer 1dB compression point. In all cases ground connections must be low inductance paths directly to a good RF ground plane.

Figure 7 shows the dependence of overall cascaded noise figure, gain, IIP3, and DC current drain on power supply voltage for such a configuration at 880MHz RF and 965MHz LO (85MHz 1000Ω differential IF interface). The image filter loss is 3dB at 880MHz. Gain

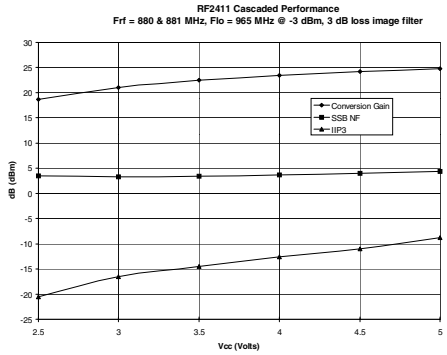


Figure 7: Cascaded Noise Figure, Gain, and IIP3, and Current Drain vs. Supply Voltage

can be seen to decrease from 24.8dB to 18.7dB as V_{CC} is reduced from 5V to 2.5V. IIP3 decreases from -8.8dBm to -20.5dBm largely due to the mixer. Noise figure decreases from 4.4dB at 5V to a minimum of 3.3dB at 3V.

LO leakage to the LNA input is less than -43dBm with 0dBm LO input power. This value is less than the sum of LNA and mixer reverse isolation, indicating degradation by a leakage mechanism external to the IC.

Conclusion

The RF2411 integrates the LNA and mixer of a high-performance UHF receiver downconverter in a 14 lead small outline plastic package. Its broadband characteristics extend the useful frequency range from 500MHz to 1900MHz frequency range. The flexible IF interface accommodates single-ended and differential filters from < 400kHz to > 200MHz. It is especially useful in portable equipment, requiring the bare minimum of external components to minimize total circuit size and cost.

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Integrated, Single-Step, 10dB Attenuator for Power Control Applications

Introduction

Wireless communication is continuing to expand into all areas of the business, government, and consumer sectors. New markets are opening around the world for products that will meet specialized requirements. To build such products, designers rely on having access to ever more sophisticated and integrated devices.

Basic Types of Integrated Attenuators and their Advantages

One particular type of device that has not seen a great deal of development is the surface mount, integrated attenuator. They are useful in reducing the power level of RF signals by a specific amount. There are two general classes - step and variable. Step attenuators allow one or more discrete levels of attenuation and are set by one or more control inputs. The variable class allows a specific value of attenuation to be selected from an overall range via an analog control voltage. They are more flexible than step attenuators as they allow any amount of attenuation to be set but the cost is greater circuit complexity. In both types, when no attenuation is selected, the attenuation is just the insertion loss of the device. The simplest type, and the focus of this article, is the single-step attenuator which needs only one control input.

Integrated attenuators offer several advantages over solutions using other types of devices. They are small, consume very little power, and can handle reasonable input power levels. Their small size makes them very attractive when trying to preserve or reduce printed circuit board space. Being designed with field effect transistor (FET) technology, they can function while drawing very low levels of current. Other approaches to providing the same function would include the use of discrete semiconductors, PIN diodes, or resistive networks in combination with active, discrete switches or relays. Each of these alternatives has drawbacks in cost, size, or performance when compared with the integrated solution.

Attenuator Design

An integrated attenuator is internally composed of a resistive attenuator network, in either a 'pi' or 'T' configuration, and active switches for signal routing. Figure 1 shows an equivalent circuit for a 'pi' attenuator along with the standard equations for first-order calculation of the resistor values. One example of this kind of component is the RF2421 from RF Micro Devices. It is a monolithic, GaAs MESFET, switched attenuator in an SOP-8 style package. It has a digitally controlled, single-step, typical attenuation of 10dB. The supply voltage range is 2.7V to 6V DC and no negative supply voltages are required. The current consumption is less than 1uA with no attenuation and is typically less than 500uA in the attenuation mode.

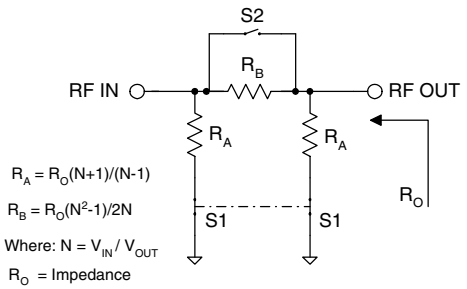


Figure 1. Single-Step Attenuator Equivalent Circuit

The input and output of the device have a low voltage standing wave ratio (VSWR) 50Ω match (Fig. 2) and the RF output can drive up to +16dBm. It has 1dB typical insertion loss over the specified 500 to 3,000MHz operating frequency range and good flatness in any 50MHz band (Fig. 3). The resistors are nickel chromium and provide excellent temperature stability. The RF ports are reversible, i.e., the input signal can be applied to either port. The attenuation control pin has an internal pull-down resistor which causes the attenuator to be turned off when it is not connected.

Typical Applications

Typical uses for this type of part include local oscillator, IF and RF level control throughout communications, measurement, and control circuits. Due to its flat, wideband response, it has little effect on phase and group delay and thus introduces minimal distortion. One radio designer required a way to reduce the output of the receive mixer in a CDMA base station prior to the IF amplifier. He found the RF2421 to be an ideal solu-

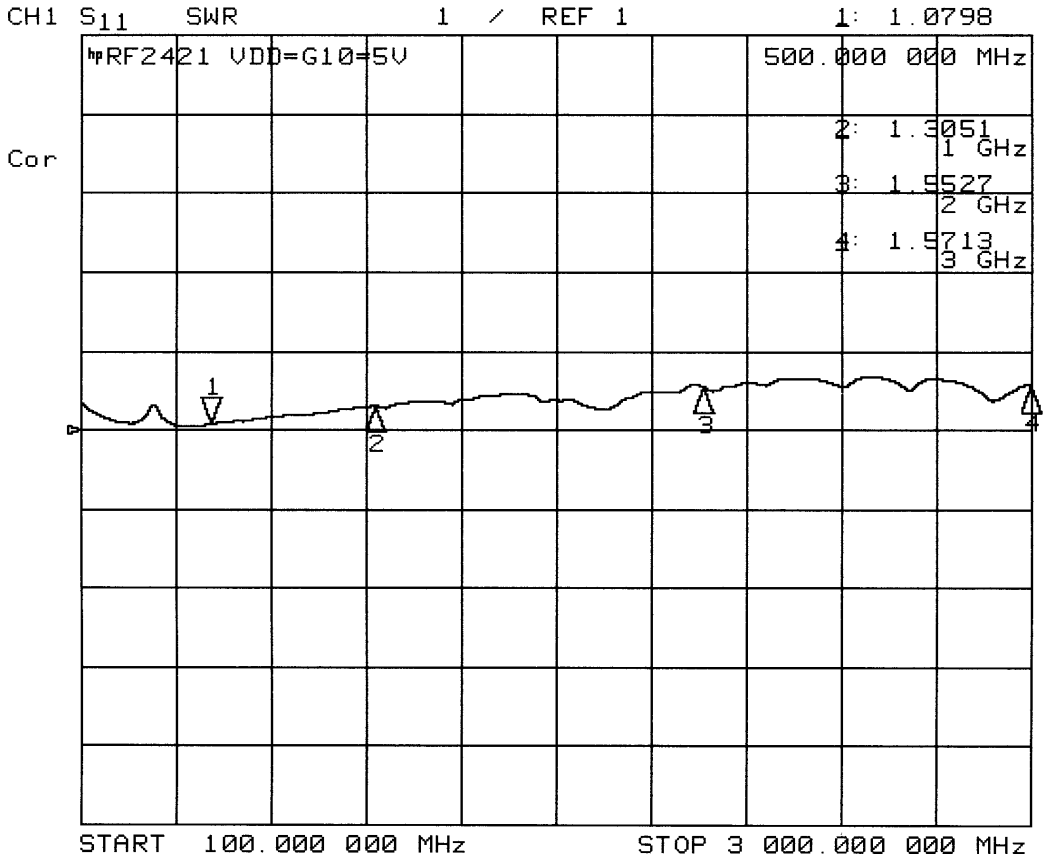


Fig. 2. RF2421 VSWR over Frequency

tion. Also, to provide one step of transmit level control with little degradation of the noise figure (NF), it could be used in a CDMA handset transmit chain between the upconverter and the bandpass filter (Fig. 4). Since the device is purely passive, it produces no additive noise and the NF is, essentially, the insertion loss. Even in the attenuation mode, the effect on noise figure would be minimal since the attenuator's noise figure would be the third term in the cascade NF equation.

In PCS systems, the base stations may be fed from multiple picocells that are physically separated from it by up to a hundred feet or more of coaxial cable. The signal levels coming into the base station will vary depending on the cable length and individual transponder power. It is desirable to keep the signals at a uniform level at the base station, and to do so, it may be necessary to attenuate the stronger signals. Again, a step attenuator can be easily dropped in to perform this function.

The upper end of a receiver's dynamic range is determined by the largest signal it can handle without being overdriven and producing unacceptable levels of distortion caused by nonlinearity. Switching in an attenuator before a low noise amplifier (LNA) in the presence of strong, in-band signals allows reception by preventing them from overdriving the receiver front end. This effectively shifts the dynamic range upward by the amount of the attenuation. For this application, it is important that the third-order intercept point (IP3) performance of the attenuator in the off-attenuation mode is better than that of the LNA so it does not worsen the receiver's linearity.

As a gain control element at the input of an amplification stage, the step attenuator would offer the added

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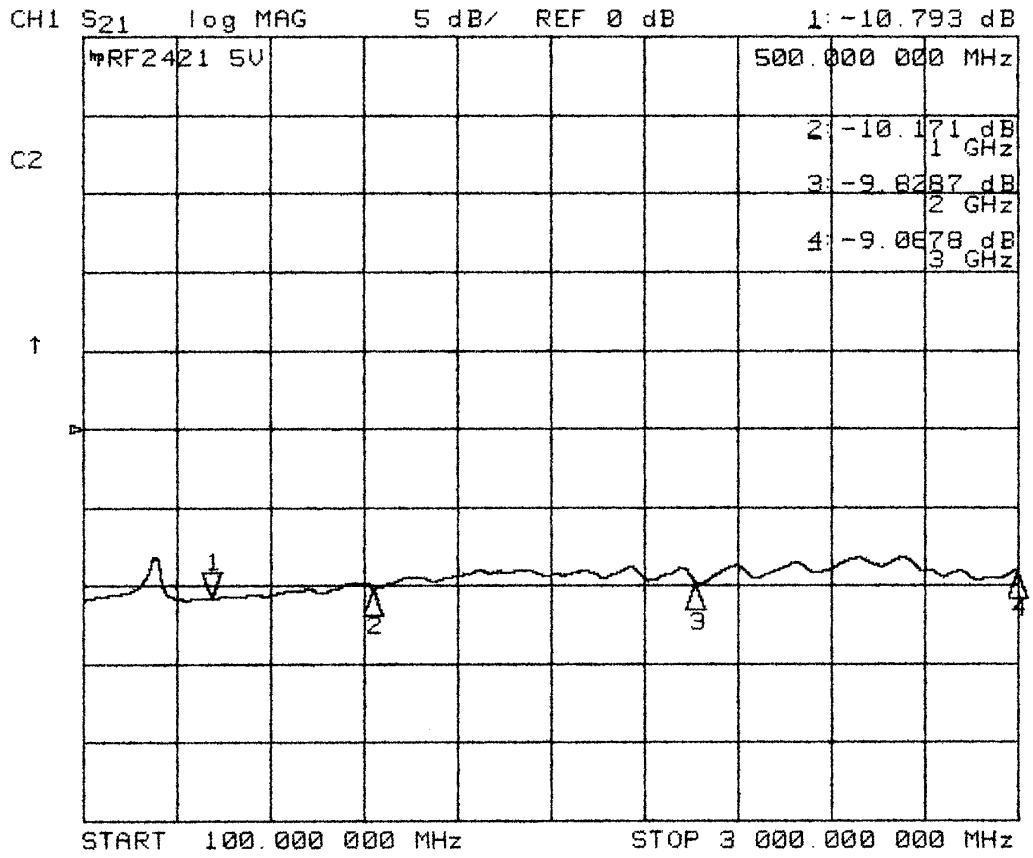


Figure 3. RF2421 Frequency Response

benefit of reducing the VSWR by reducing the return loss. In many cases, only one or two dB of additional isolation is needed to improve amplifier instability or to help isolate a poorly matched load from a source. When the attenuator is active, it is actually a pad since it has the same input and output characteristic impedance. It presents itself to the signal as a lossy transmission line having zero path length and, therefore, no delay. A 10dB pad would decrease a 2:1 VSWR to about 1.07:1.

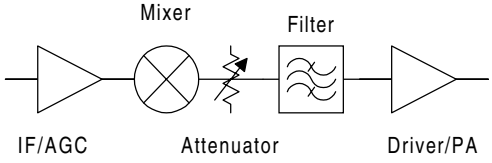


Figure 4. CDMA Handset Transmit Application

Conclusion

The RF2421 Single Step 10dB Integrated Attenuator is an extremely versatile component allowing radio designers to improve system performance by appropriately setting RF signal levels through their systems.

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Silicon Transceiver Family for Low-Power Wireless Communications

Abstract
A family of low-power RF transceivers has been developed for wireless data communications devices operating in the European 433MHz to 869MHz ISM bands or the U.S. 902MHz to 928MHz ISM band. All three IC's have been implemented in a 15GHz silicon bipolar process technology that allows low-power FSK/ASK transceiver operation in commercial wireless products. Typical applications include wireless security systems, wireless meter reading equipment, or virtually any wireless data link application operating up to 1Mb/s. All three devices include an inherent transmit/receive switch, a complete receiver/demodulator, a low-power voltage-controlled oscillator (VCO), and a complete modulator/transmitter. Additionally, the RF2905/2925 include an on-chip PLL frequency synthesizer that can be used to support up to 4-channel operation. For applications requiring more channels, the RF2915 is designed to interface directly to commercially available programmable PLL frequency synthesizers. The RF2905 provides for two-channel transceiver operation, while the RF2925 is optimized for single channel operation in systems using Time Division Duplexing (TDD). The typical DC power consumption of these devices is less than 1uA@3.0V in the sleep mode, 8.2mA@3.0V in the receive mode, and 23mA@3.0V in the transmit mode. At 3.0V operation, the receiver achieves a typical cascaded noise figure of 10dB and the transmitter produces +4dBm (@915MHz) typically into a 50Ω load. The chip also provides for modulation flexibility and can be configured as an FSK/FM, or ASK/AM data transceiver. The RF2905/2925 are packaged in a low-cost 48-pin LQFP package. The RF2915 is packaged in a 32-pin LQFP package.

This paper also discusses operation of the device as an unlicensed FSK transceiver in the U.S. 902MHz to 928MHz ISM band with regulatory compliance to FCC Part 15.249. In addition, a variety of application considerations are provided to assist system designers in implementing the device as a one-way transmitter/receiver, or as a full two-way RF transceiver using FSK or OOK AM data modulation.

Product Applications and Technology Selection

Until recently, low-cost wireless data or voice products for a wide range of consumer and industrial applications have predominately utilized lower VHF frequency bands for unlicensed operation of low-power RF devices. Operation in these frequency bands, such as the U.S. 49.82MHz to 49.90MHz band, has been an obvious choice for designers in these cost sensitive applications due to the abundant supply of low-cost highly integrated components. The success and wide market acceptance of wireless products, such as 49MHz analog cordless telephones, have resulted in the demand for next generation wireless products that achieve higher performance levels at lower cost. Furthermore, the crowded conditions that exist in the traditional VHF frequency bands and the need for additional bandwidth to support advanced products using digital modulation techniques have motivated product designers to develop products that operate in spectrum allocated at UHF, such as the U.S. 902MHz to 928MHz ISM band. To reduce product development cycles in these next generation products three new monolithic RF transceiver products (RF2905/2915/2925) have been introduced by RF Micro Devices that provide product designers with "Antenna-to-Bits and Back" solutions for their wireless applications. Target wireless applications for the RF2905 transceiver family include utility meter reading, security systems, bar code scanners, cordless telephones, and RFID tags just to name a few.

All three transceiver products were designed to achieve high performance levels while minimizing DC power consumption. Integral to the design process was the use of Optimum Technology Matching™ to select the appropriate IC technology to meet the product objective. Optimum Technology Matching™ means that we consider all RFIC technologies at our disposal for new designs to develop the lowest cost solution that meets the technical requirements of a given application. In the case of the RF2905 transceiver family, the primary applications for these devices are in battery powered applications, such as those found in wireless utility meter reading applications where the primary battery may be expected to last for 10 years or more. In the case of the RF2905 transceiver family, a 15GHz silicon bipolar process technology was deemed as an Optimum Technology Match for this application. The silicon bipolar process we selected provides a minimum geometry device that exhibits a 15GHz F_T under 3V and 0.5mA DC operation. Of the GaAs and silicon IC processes we considered, this process allows us to provide a monolithic, low-power, UHF transceiver IC that sells for less than $4.00 in volume.

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Product Descriptions

The RF2905/2915/2925 are quite similar products. All support wireless applications with data rates less than 1MB/s using FSK or ASK digital modulation. The RF2905/2925 also support linear modulation, allowing their application in systems employing analog FM or AM. All three products, as shown in Figures 1a & 1b, utilize the same single conversion, superheterodyne receiver architecture.

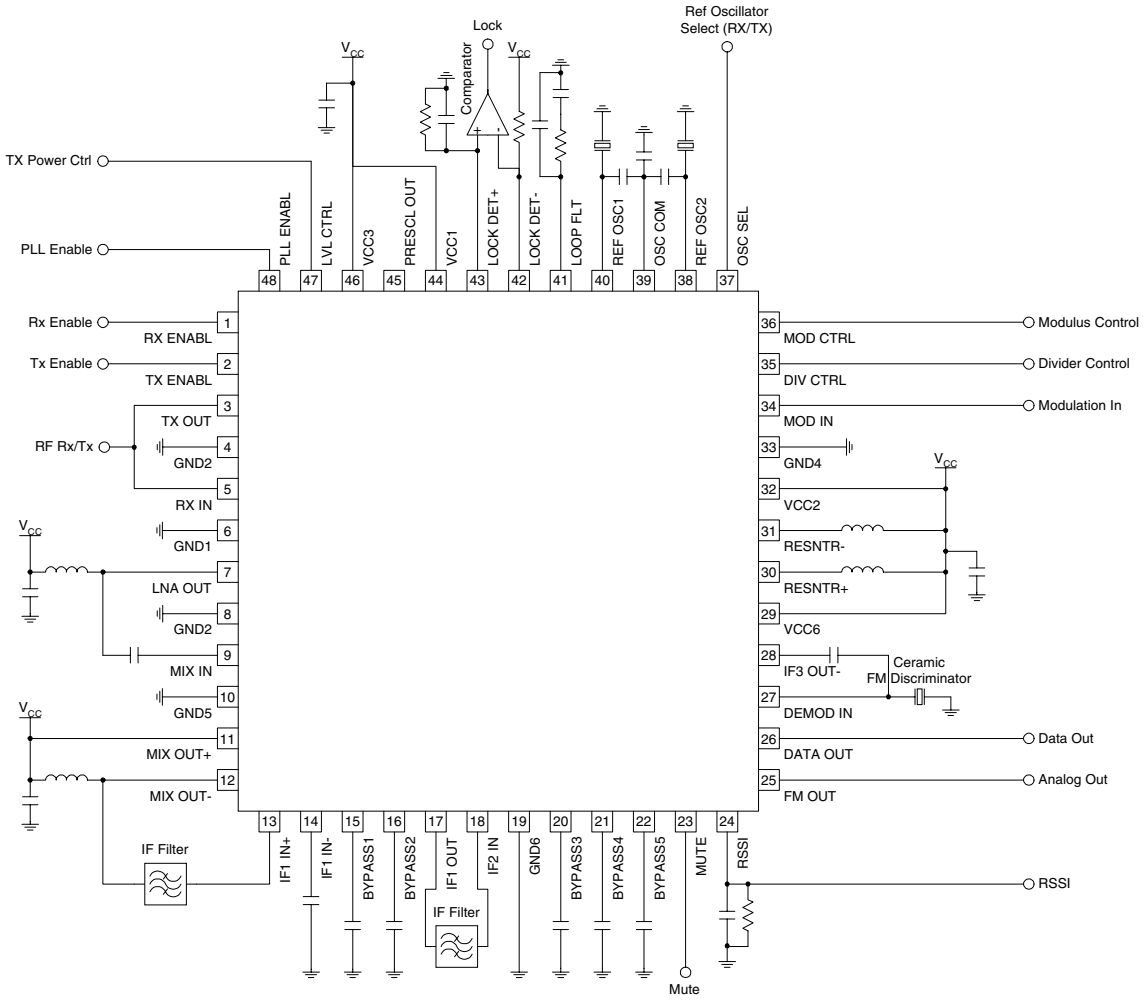


Figure 1a. RF2905/2925 Functional Block Diagram

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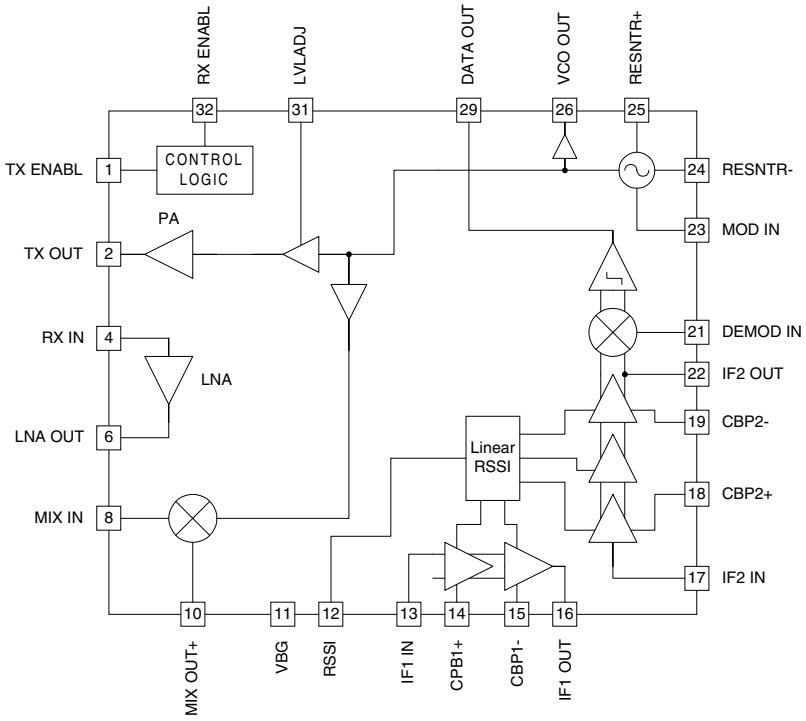


Figure 1b. RF2915 Functional Block Diagram

Frequency Range-All	**300-1000MHz**
Receiver Sensitivity-All	**-97 dBm for 10E-4 BER (FSK)**
Tx Power (433/915)-All	**+10/+4 dBm @ 3.0V**
Modulator FM Deviation-All	**500kHz p-p Typical**
Rx/Tx Turn-Around Time -RF2905/ 2915/2925	**6 mSec/Ext. PLL/150usec Typ.**
DC Power Consumption-Receive- RF2905/2915/2925	**8.2/5.5/8.2 mA @ 3.0 V**
DC Power Consumption-Transmit- RF2905/2915/2925	**23/20/23 mA @ 3.0 V**

Table 1. Performance Summary for the RF2905 Transceiver Family

Table 1 also provides a performance summary for key parameters associated with each device. Receiver interfaces are designed to be directly compatible with low-cost 10.7MHz ceramic filters. On the transmit side, carrier modulation is imparted by either direct modulation of the VCO using the on-chip modulation varactors in FM/FSK applications, or through modulation of the carrier amplitude using a linear output power control pin in AM/ASK applications. The devices also include an inherent 50Ω T/R switch that greatly simplifies their antenna interface. The receiver input and transmitter outputs can be connected directly together (with DC

block) and provide a 50Ω interface without external matching components in the transmit and receive operating modes. The RF2905/2925 provide an on-chip PLL to lock the VCO to one of the reference crystal oscillators. The RF2915 is designed to interface the on-chip VCO to an external PLL frequency synthesizer. Selection of the transceiver appropriate for a given application begins with consideration of the number of RF channels required by the system. Tables 2a & 2b provide a selection guide for the transceivers based on the number of channels required in transceiver or simplex (Rx or Tx only) applications.

Product Part #	# of RF Channels in European 433MHz ISM band	# of RF Channels in European 869MHz ISM band**	# of RF Channels in U.S. 915MHz ISM band
RF2925	1	1	1
RF2905	1	1	2
RF2915	10	10	171

Table 2a. RF Channels* Supported in Two-Way Transceiver Operation

Product Part #	# of RF Channels in European 433MHz ISM band	# of RF Channels in European 869MHz ISM band**	# of RF Channels in U.S. 915MHz ISM band
RF2925	1	1	1
RF2905	2	2	4
RF2915	10	10	171

Table 2b. RF Channels Supported in One-Way Simplex Operation

** 150kHz Channel Bandwidth*

*** Operation in bandwidth allocated for wideband use in non-specific applications within the 868-870MHz Frequency band*

While only single-channel transceiver operation is supported in the 433MHz to 869MHz European ISM bands using the RF2905/2925, the RF2915 provides ten (10) 150kHz channels in 433MHz European ISM band when used in conjunction with an external PLL frequency synthesizer. As shown in Table 2b, the RF2905 can be used to provide a four-channel receiver or transmitter in the U.S. 915MHz ISM band for simplex applications. Four channel operation is accomplished with the RF2905 by independent control of the two reference oscillators (OSCSLT) and the prescaler modulus control input (MODCTL). Using the RF2905, a two-channel receiver or transmitter in the 433MHz to 869MHz bands is also supported without the need for an external PLL. For applications requiring more channels, the RF2915 should be used to interface to an external PLL frequency synthesizer. The RF2915 includes all the functionality of the RF2905 minus the on-chip PLL.

By design, all three transceivers are intended to operate half-duplex. Therefore, an additional consideration in selection of the transceiver product is the Rx/Tx turn-around time. The RF2905 provides independent control (ON/OFF) of the on-chip crystal reference oscillators to provide multiple channels, but minimum Tx/Rx (or Rx/Tx) turn-around times are typically on the order of milliseconds due to the start-up time required by the crystal reference oscillators. In general, applications requiring turn-around times less than 1msec, such as those found in systems using TDD, should utilize the RF2915 or RF2925. Using the RF2925, both on-chip reference oscillators remain on in both transmit and receive modes and the device is capable of providing turn-around times less than 150µsec. The RF2915 relies on an external reference oscillator circuit, thus the device is applicable to both TDD and FDMA system applications.

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Application Example - 915MHz, 28.8Kb/s FSK Data Transceiver Using the RF2905

The RF2905/2915/2925 are available on evaluation PCB's that provide users with a convenient way to try out the transceiver in their wireless application. As an example, the RF2905 evaluation PCB can be used out-of-the-box to provide a 28.8Kb/s two-way data link in the U.S. 902MHz to 928MHz ISM band. Application considerations related to range of the transceiver, PLL bandwidth, and regulatory compliance required for device operating under FCC Part 15.249 are discussed in the paragraphs that follow. Similar issues apply to operation of the devices in the European ISM bands. A detailed schematic of the application circuit discussed is provided in Figure 2.

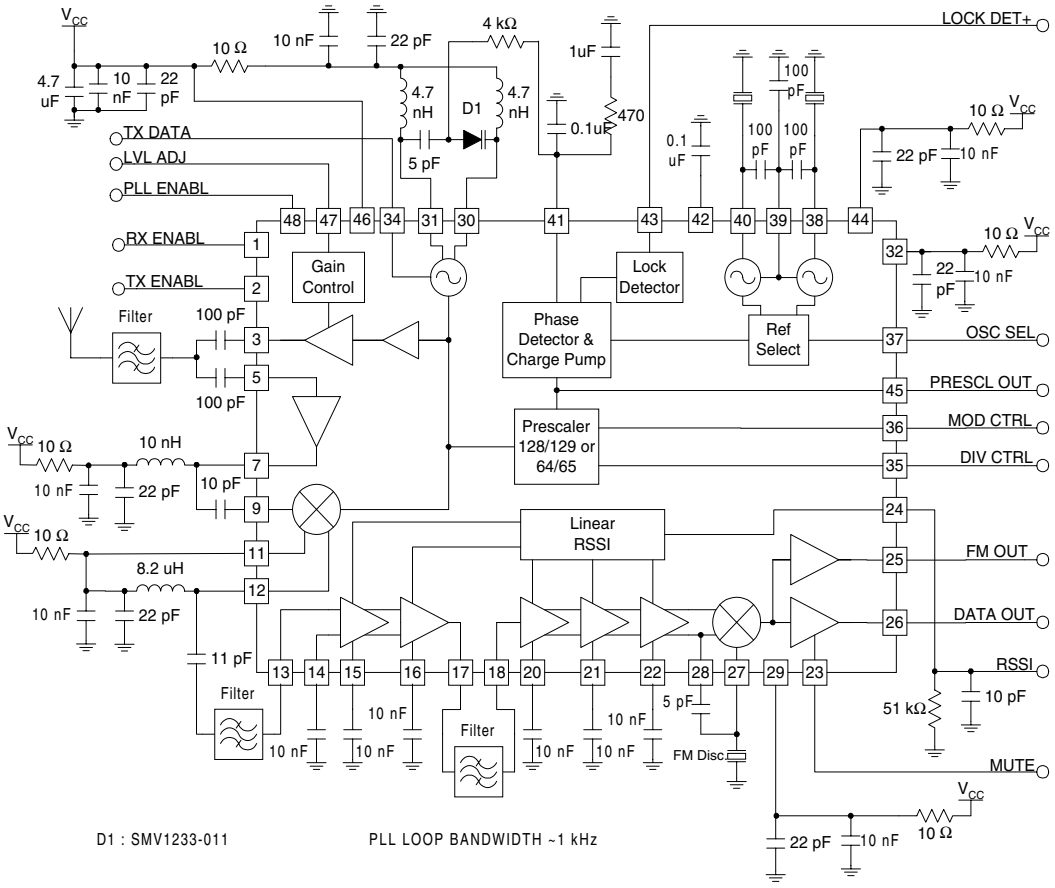


Figure 2. Application Circuit for 915MHz 9.6KB/s FSK Transceiver

Transceiver Operation

The RF2905 has four basic operating modes: sleep; lock; receive; and, transmit. The sleep mode allows the transceivers to be turned completely off to reduce the device current consumption to much less than 1µA. When the IC is in the lock mode, the VCO, prescaler, and LO buffer circuitry is enabled to allow the PLL to achieve lock prior to enabling the receiver or transmitter functions. This avoids the possibility of an inadvertent spurious emission during the interval when the PLL is locking. In operation, the receiver and transmitter functions are enabled once the PLL has achieved lock.

28.8Kb/s FSK Receiver Application Considerations

In order to minimize susceptibility to receiver desensitization in the low power single-conversion receiver, RF-IF conversion gain should be limited to that required to set the receiver noise figure. The RF2905 typically provides 16dB of RF-IF voltage gain in the LNA/mixer, achieving a 10dB cascaded noise figure. Additional rejection of interference within the 902MHz to 928MHz band is provided by dual 10.7MHz ceramic IF filters that were selected to establish a 150kHz channel. The 150kHz channel bandwidth is much wider than the 28.8Kb/s data bandwidth and sacrifices some receiver sensitivity in this application. The additional bandwidth allows for center frequency errors in the transmitter and receiver associated with low-cost crystals. The 10.7MHz IF was selected because of the availability of low-cost ceramic filters in a variety of bandwidths up to 280kHz. The user is free to select other IF's and/or filters that are compatible with the 25MHz, -3dB bandwidth provided by the 100dB limiting IF. A balanced multiplier is provided as an FSK demodulator. An external 10.7MHz ceramic discriminator provides the quadrature phase component for the multiplier. Other quadrature networks, such as a discrete LC tank can also be used with the chip.

The IF also provides over 80dB of received signal strength indication (RSSI). The RSSI works with the IF amplifiers to provide a DC output voltage proportional to the strength of the RF input signal. A graph of the RSSI response is shown in Figure 3.

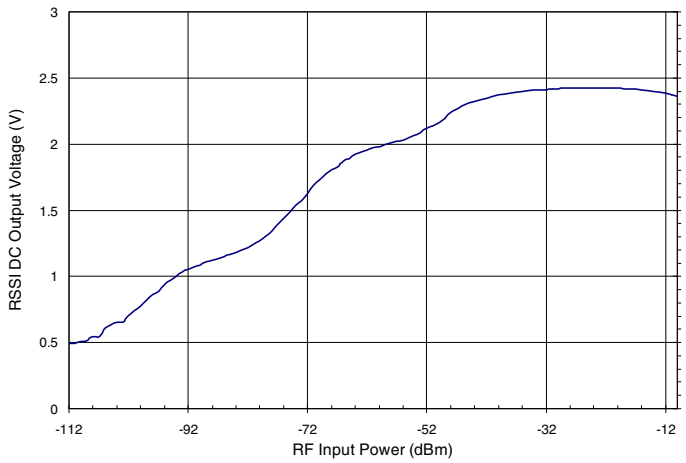
The graph shows a typical range of 0.5V to 2.5V over RF input power range of 80dB. The RSSI output could also be used as the demodulator in a simple AM on-off keyed (OOK) system. An external data slicer would be necessary to convert the analog RSSI output to a logic level in this type of system.

The output of the FSK demodulator is DC coupled internally to the data slicer. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesired 2xIF product. The data slicer is a one bit analog-to-digital converter that uses the balanced output from the demodulator to make a bit decision and provide a rail-to-rail output. This balanced data slicer has a speed advantage over a conventional adaptive data slicer where a large capacitor is used to provide DC reference for the bit decision. Since the balanced data slicer does not have to charge a large capacitor, the RF2905 requires a much shorter preamble and exhibits a response time that is nearly instantaneous when compared to an adaptive RC data slicer. For best operation of the balanced on-chip data slicer, FM deviation needs to exceed the center frequency error anticipated between the transmitter and receiver. In general, the FM deviation should be set as wide as possible to avoid duty cycle distortion in the data output when the received signal is not centered on the FM discriminator.

FSK Tx Modulator/PLL Considerations

On-chip varactors are used to impart FSK/FM modulation directly to the VCO. This direct modulation eliminates the need for frequency upconversion and greatly simplifies the filtering requirements required to comply with FCC Part 15.249. In order to directly modulate the

Figure 3. RSSI Output Voltage vs. RF Input Power



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VCO, the PLL bandwidth should also be set much lower than the data bandwidth to avoid distortion of the transmitted FSK signal. As a competing consideration, the PLL bandwidth (in conjunction with the start-up time of the crystal reference oscillators) also effects the Rx/Tx turn-around time (Rx/Tx switching time) of the transceiver. Therefore, a trade-off exists in selecting the appropriate PLL bandwidth that allows the VCO to be directly modulated at the data rate while achieving the desired Rx/Tx turn-around time.

As the primary consideration, the modulation rate needs to be much higher than the PLL bandwidth to prevent the PLL from tracking out the modulation. In application, long strings of "1's" or "0's" can also be tracked out by the PLL and can produce bit errors. Therefore, the lowest frequency data input to the modulator should always be greater than the PLL bandwidth. For these reasons, Manchester encoding is recommended when using the FSK modulator. When Manchester encoding is used, two symbols are required to transmit a single bit of information. Using Manchester encoding, a binary one is represented by a positive half-bit period pulse followed by a negative half-bit period pulse. A binary zero is represented by a negative half-bit period pulse followed by a positive half-bit period pulse. Since a Manchester encoded data stream has zero DC value on a bit-by-bit basis, long strings of "1's" or "0's" will not be distorted by the PLL. The PLL bandwidth is set externally to the device using a passive second-order loop filter that uses two capacitors and a resistor in a shunt configuration (see Figure 4). Experimentally, we have determined that the PLL bandwidth should be a least five to ten times lower than the minimum data rate input to the modulator. In our 28.8Kb/s example, the 1kHz PLL bandwidth maintains data symbol integrity and provides a 6msec Rx/Tx turn-around time. The peak frequency deviation provided by the modulator varies with the amplitude of the modulation input. Figure 5 provides a graph of the FM deviation characteristics of the open loop VCO as a function of the modulation input (MODIN). Once a PLL bandwidth consistent with the data rate has been established, the PLL lock time can be predicted using second-order PLL loop equations. Figure 6 provides a plot of the RF2905 PLL lock time as a function of the PLL loop bandwidth. To determine the Rx/Tx turn-around time of the transceiver, the start-up time of the crystal reference oscillator should be added to the PLL lock times in Figure 6. The start-up time of the crystal reference oscillators can also be influenced by the choice of external circuitry and the PLL configuration.

The Rx/Tx turn-around time includes both the start-up time of the crystal oscillator and the PLL lock time. For all practical purposes, the start-up time of the crystal oscillator sets a lower bound on the Rx/Tx turn-around time that can be achieved in operation. In other words, if the PLL takes zero seconds to lock, the Rx/Tx turn-around time is the time it takes the crystal reference oscillator to start. The RF2905 includes a dual-modulus/dual-divide prescaler that provides 64/65 and 128/129 divisors. Thus, for operation in the 915MHz ISM band, either 7MHz or 14MHz crystals can be used in the reference oscillator circuitry. Since the start-up time of an oscillator is inversely proportional to the bandwidth of the crystal, a 14MHz crystal oscillator will start twice as fast as a 7MHz crystal oscillator (assuming a constant crystal "Q"). Therefore, by using a 14MHz crystal and the 64/65 prescaler, the start-up time of the crystal oscillator can be cut in half over that achieved by the 7MHz crystal oscillator circuit. Experimentally,

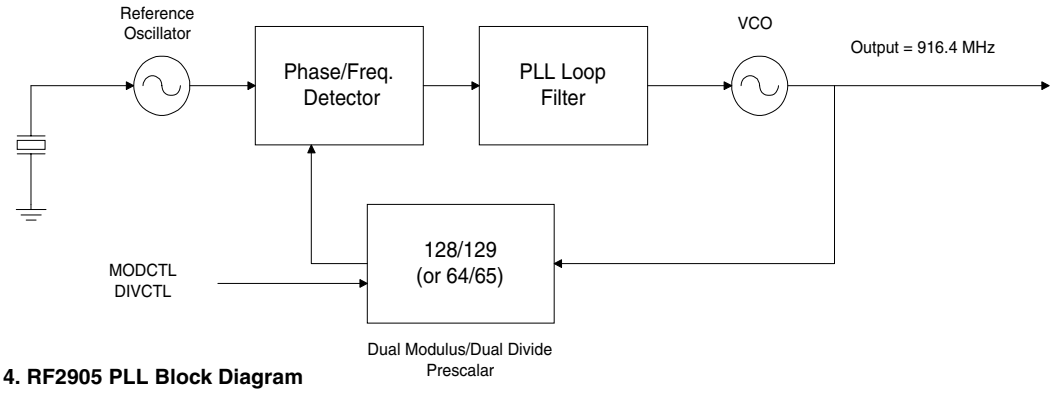


Figure 4. RF2905 PLL Block Diagram

Figure 5. Deviation from Carrier vs. Modulation Input Voltage (Vcc=3V, LVL ADJ=3V)

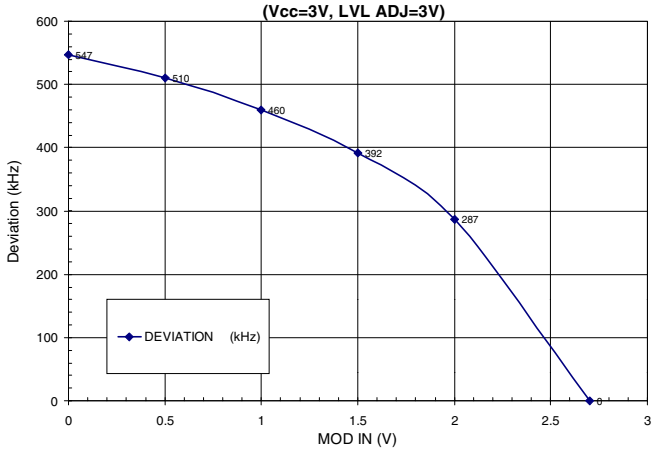
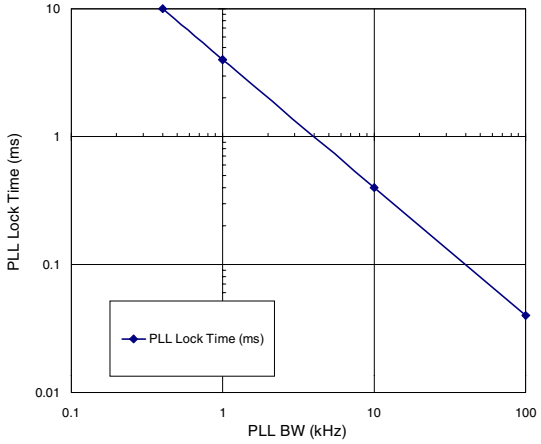


Figure 6. PLL Lock Time vs. PLL BW



oscillator start-up times of 1msec have been recorded using 14MHz crystals. To achieve an Rx/Tx turn-around time of 1msec would require the PLL bandwidth to be greater than 10kHz and the use of 14MHz reference crystal oscillators. As mentioned previously, if a turn-around time less than 1msec is required, then the RF2925 should be considered for the application.

Transceiver Range Considerations

A sample receiver sensitivity calculation for a system using the RF2905/2915/2925 is shown below. In Equation 1 below, the noise figure applied is the measured SSB noise figure of the device. The IF detection bandwidth (BW) of 150kHz established by the 10.7MHz ceramic filters provided on the evaluation PCB, and the required IF predetection signal-to-noise ratio is chosen to be 12dB to provide a BER of 10^{-4} for FSK demodulation. Since no RF image filter is provided on the evaluation PCB, a 3dB degradation due to the image noise is also taken into account.

Equation 1.

Sensitivity = -174dBm+Image Noise+NF+ 10log BW**+SNR(dBm)

Sensitivity = -174dBm+3dB+10dB+ 10log(150K)dB+12dB (dBm)

Sensitivity = -97.2dBm

**BW= Noise equivalent predetection bandwidth

Transmit power is restricted for unlicensed devices operating under FCC Part 15.249 to a field strength of 50mV/meter at a distance of three (3) meters. Assuming a unity gain isotropic antenna, this corresponds to a transmitter output power level of 0.75mW or -1.25dBm. The RF2905/2915/2925 provide a healthy +4dBm max. at 3.0V to provide additional margin for applications that utilize more lossy antennas. As shown in Figure 7, DC current consumption of the device is also reduced at lower output power settings.

With respect to path loss equations for estimation of indoor transceiver range, a convenient point of reference is the one-over-r-squared free space path loss equation (Equation 2).

$$\mathrm{Pr} = PtGtGr\ (\lambda / 4\pi)^2 (1 / d^2) \qquad \text{Eq. 2}$$

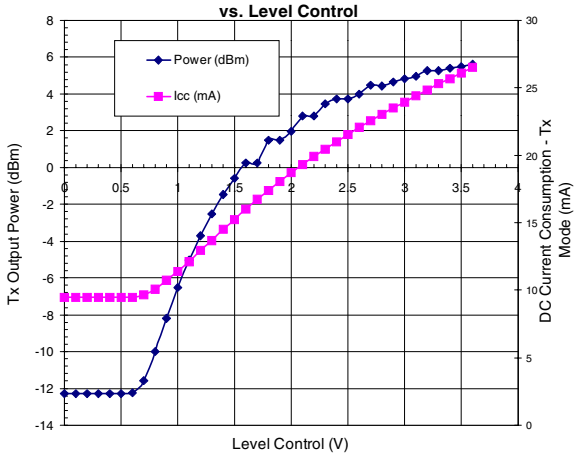
For indoor RF propagation, experience has shown one should expect higher path loss than that predicted by the free path loss equation. Published models for estimation of path loss in buildings modify the exponent of the distance term in Equation 2 (2 for free space) to three or more and often include a fixed offset term. Actual RF propagation in buildings will be depend on a wide variety of factors, but for estimation purposes one might assume the distance exponent is in the range of 3 to 4 in many scenarios. Solving Equation 2 (assuming unity gain antennas and a distance exponent of three or four) results in a range prediction of 450feet and 132feet in the 902MHz to 928MHz frequency band, respectively. The free-space path loss equation predicts a range of nearly one mile. Obviously, the range of the device will depend on the environment in which the device is operated and on a variety of considerations that are beyond the scope of this example.

915 MHz Transceiver Test Results

In order to further validate the transceiver design, field testing of a two-way 916MHz radio link using the RF2905 hardware was undertaken to characterize the range of the device in a commercial office building. For obvious reasons, the RFMD Corporate Headquarters building was selected for performance of the in-building range testing. The RFMD Corporate Headquarters, as shown in Figure 8, is an "L" shaped building that is constructed using interior/exterior steel stud walls and a brick exterior. Interior to the building, along the center-line, are steel-frame office cubicles containing steel office furniture. Based on the building construction, one would expect an RF signal might be challenged in attempting to propagate throughout the building.

To accomplish the testing, an RF2905 transmitter was set-up in the far corner of the Engineering Lab (see Figure 8) and operated at an output power level of 0.75mW into 50Ω. The 916.4MHz carrier was modulated at 28.8Kb/s with an occupied signal bandwidth of 110kHz. The transmitted output was observed on a

Figure 7. TX Output Power and DC Power Consumption vs. Level Control



spectrum analyzer and is shown in Figure 9a (close in) and Figure 9b (broadband). In order to achieve compliance to FCC Part 15.249, the spurious emissions from the device must fall below the levels shown in Figure 10. As shown in Figure 9a, the highest spurious emissions from the device outside the ISM band are offset from the carrier by twice the reference frequency. The level of this reference spur is -58.7dBm. This compares to the out-of-band limit of -49.3dBm for FCC compliance in this frequency range. FCC Part 15.249 also limits harmonics of the transmitted output to 500microvolts/meter, or -41.25dBm. As shown in Figure 9b, the second and third harmonics of the transmitter output are also well below this level.

The receiver was operated from a 3.6V lithium battery located at various locations throughout the building. One-quarter wavelength monopole antennas were used on both the transmitter and receiver. A digital voltmeter was used to measure the RSSI output voltage from the receiver. The measured DC RSSI output was then compared against measured RSSI output versus RF input power (ref. Figure 3) to determine the signal strength at the point of measurement. Since the RSSI detector is a broadband power detector, the data output was monitored throughout the field test to ensure the signal being detected was the one that was transmitted. A typical output from the receiver data slicer for the 28.8Kb/s Manchester encoded data signal used in the test is shown in Figure 11. Figure 11 also displays a sample of the transmitted random data. Using a low-side LO on the receive side results in data inversion from the transmitter to the receiver. The measured signal power at various points throughout the building are as shown in Figure 8. A signal level consistent with a bit error rate of less than 10^{-4} was maintained throughout the building, except in the furthest corner. In this location, the data signal was still quite discernible, but had fallen below the target signal quality. As a point of comparison, the measured data was plotted against the path loss equation for distance exponents of 2, 3 and 4 in Figure 12. Although the data applicability is limited, it is clear that the path loss exceeds a 40log(R) prediction at the extremes of the building.

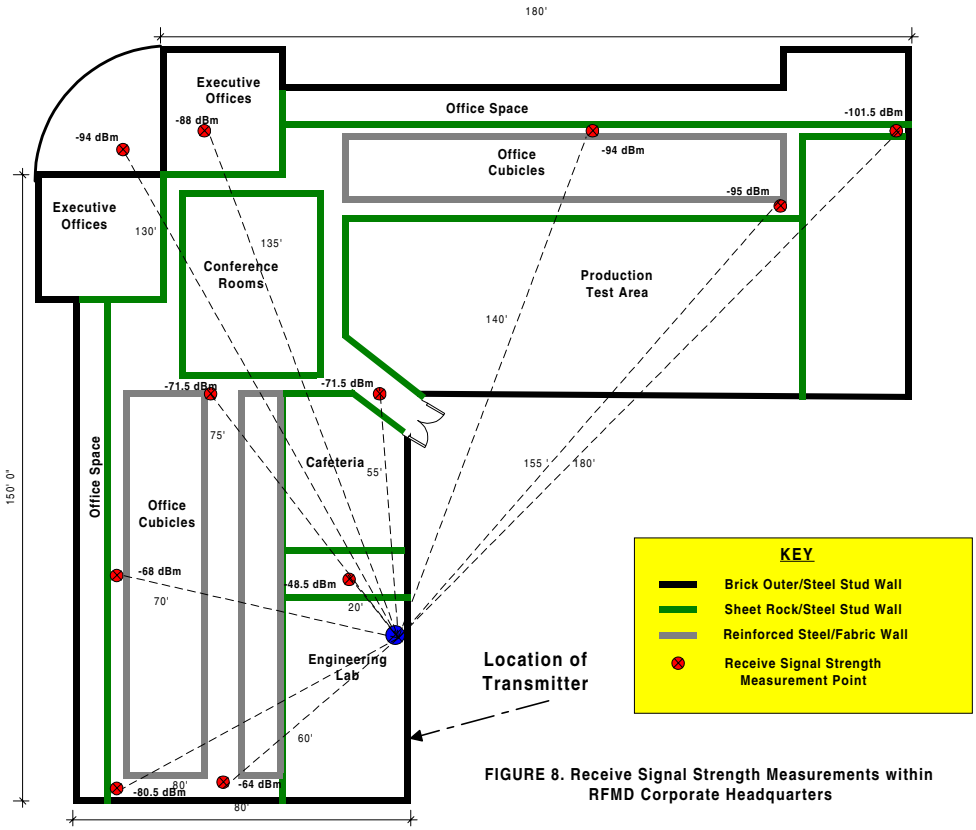
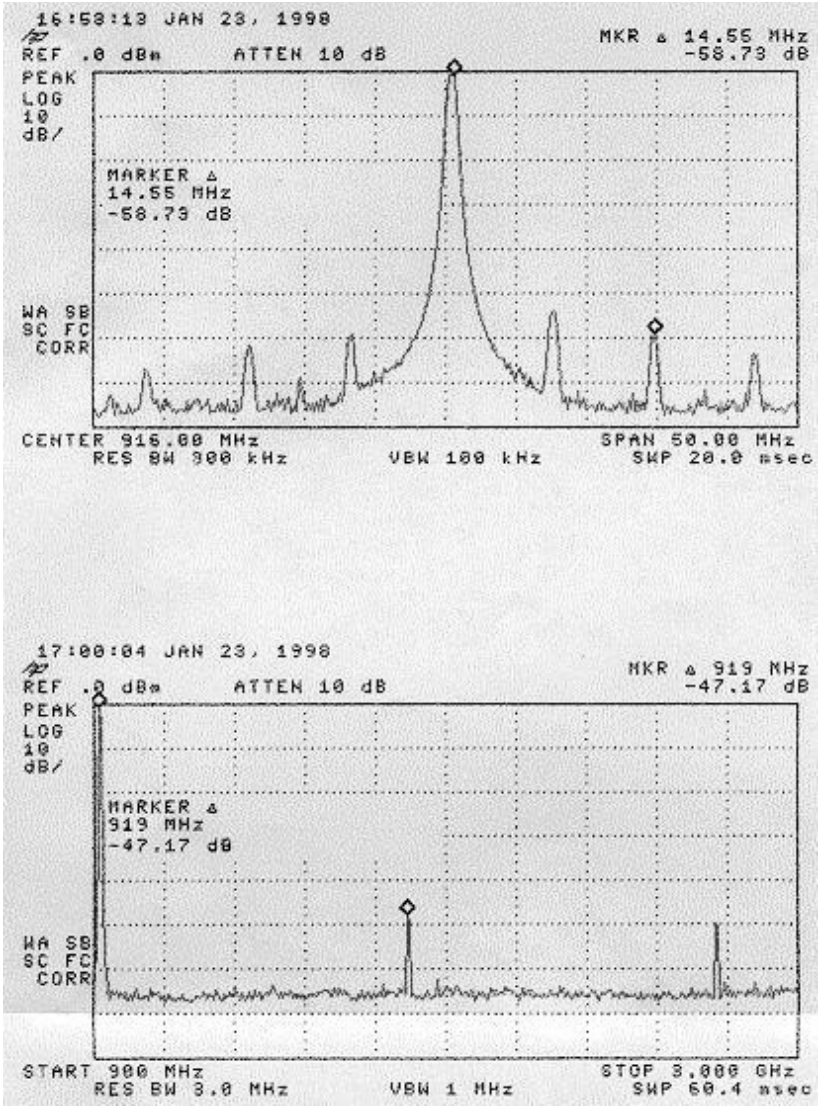


FIGURE 8. Receive Signal Strength Measurements within RFMD Corporate Headquarters

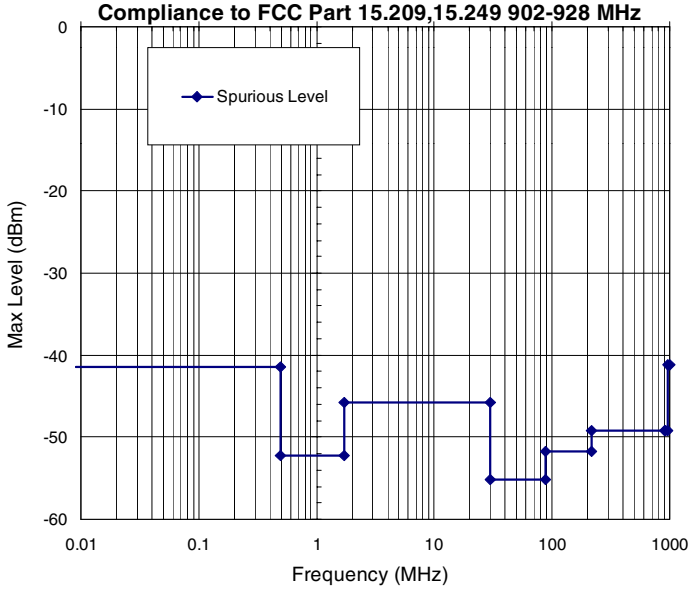


Figures 9a & 9b. Observed Transmitter Output Waveforms

Conclusion

A family of transceiver IC's have been developed that offer robust transceiver performance in wireless radio applications in the European and U.S. ISM bands. The IC's can be configured for FM/FSK or AM/ASK data modulation. Product differentiation with regard to the number of RF channels and the Rx/Tx turn-around time are provided in the RF2905 family to support a wide range of battery-powered applications. The viability of using the device as a wireless data transceiver has also been demonstrated in a large commercial office building. The IC's are manufactured on 8-inch silicon wafer ICs, and are currently available in volume for under $4.00.

Figure 10. Maximum Spurious Emission Levels for Compliance to FCC Part 15.209,15.249 902-928 MHz



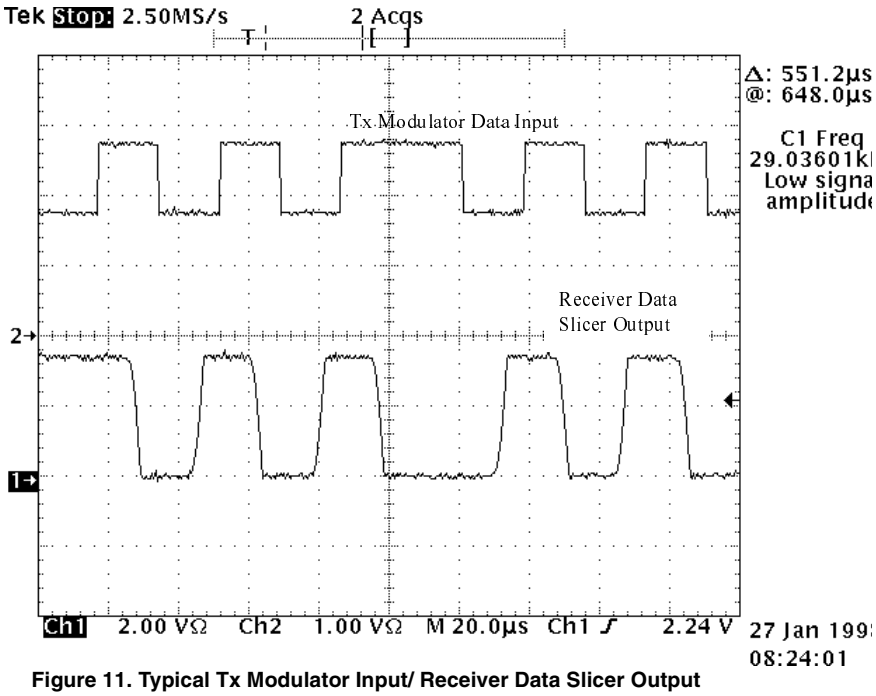
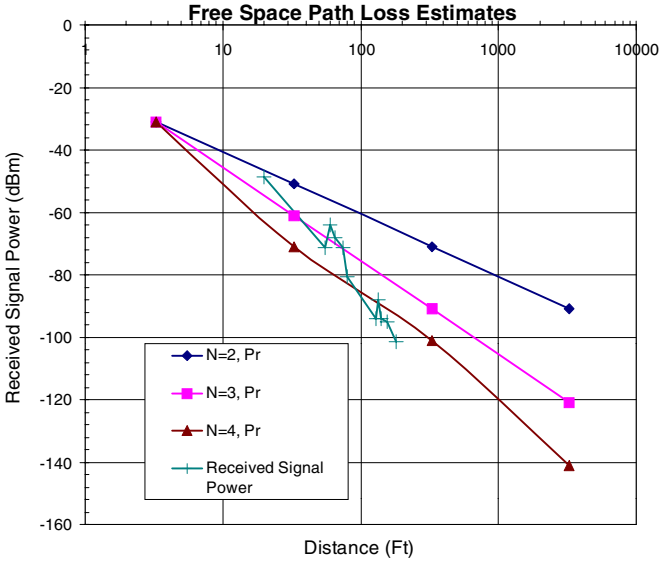


Figure 11. Typical Tx Modulator Input/ Receiver Data Slicer Output

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Figure 12. Measured Rx Signal Power As Compared to Free Space Path Loss Estimates



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Highly Integrated ASICs for CDMA Cellular/PCS Phones

Introduction

The first generation of Cellular and Personal Communication Services (PCS) phones that are based on Code Division Multiple Access (CDMA) relied on limited integration of RF and IF functions (see Figure 1). Integrated Circuits (IC's) were designed to handle automatic gain control (AGC) amplification, upconversion, and power amplification in the transmit chain. In the receive chain, IC's were developed to handle low noise amplification and downconversion, and receive

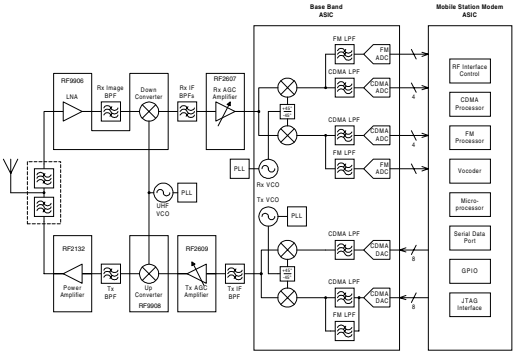


Figure 1. 1st Generation CDMA Cellular Phone Architecture

AGC amplification. Baseband ASIC's were developed separately and included modulation, demodulation, analog/digital conversion, and all other digital processing circuitry. The next generation of phones followed very rapidly with new ideas for integration and chip partitioning (see Figure 2). Phone designers chose to remove quadrature modulation and demodulation functions from the baseband ASIC's and place them in the analog RF/IF chips to alleviate mixed-signal isolation issues and allow for lower power CMOS designs. In order to lower chip count and save valuable phone board real estate, phone designers moved to integrate the transmit AGC amplifier with the transmit upconverter. To accommodate this new CDMA architecture which pushes toward higher levels of integration, RF Micro Devices developed three new integrated circuits. The RF9957 CDMA/FM Receive AGC/Demodulator, the RF2667 CDMA/FM Receive AGC/Demodulator and the RF9958 CDMA/FM Transmit Modulator/AGC/ Upconverter are all monolithic IC's that are fabricated in an advanced bipolar Silicon process. All three of these low-cost IC's operate at a 3V power supply and are provided in small QSOP plastic packages.

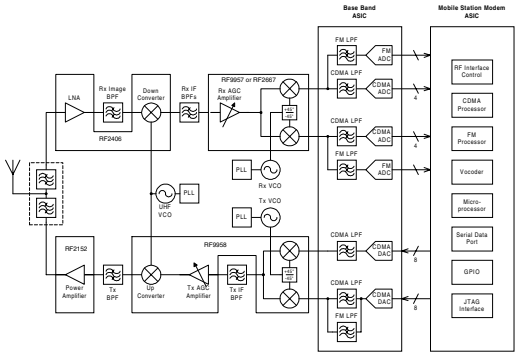


Figure 2. 2nd Generation CDMA Cellular Phone Architecture

Transmit IC

The RF9958 integrates three functions into a single QSOP-28 package: quadrature modulation, variable gain amplification, and upconversion (see Figure 3). In a transmit system the RF9958 receives baseband information from a mixed-signal or digital ASIC in the form of in-phase/quadri-phase (I/Q) data. The RF9958 provides differential input ports that are driven with the I/Q waveforms riding on a DC reference of 0.6VDC. Single-ended operation can also be accommodated if the I/Q data is driven into the ISIG and QSIG pins with the IREF and QREF pins capacitively coupled to ground (see Figure 4). In both cases, the 0.6VDC reference is applied to all four pins.

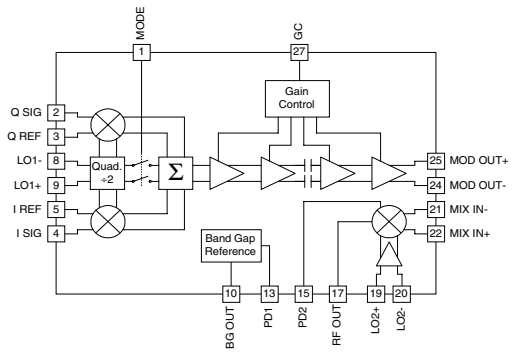


Figure 3. RF9958 Functional Block Diagram

The local oscillator (LO) signal onto which the I/Q data is modulated can also be provided to the part differentially or single-endedly. In general, differential drive is always recommended for ideal operation because it provides symmetrical swings on-chip that give better phase accuracy, but single-ended drive will work adequately. In order to split the incoming LO signal into two signals that are in phase quadrature, the RF9958 utilizes a divide-by-two flip-flop circuit. Consequently, the LO signal provided to the part must be twice the desired carrier frequency. It is common, in an RF transceiver, to use a voltage-controlled oscillator (VCO) that operates at twice the carrier frequency so that VCO leakage into other components of the system does not appear as co-channel interference. The flip-flop circuitry can operate up to 360MHz, which translates to a carrier of 180MHz. If a higher carrier frequency is desired, the flip-flop circuitry can be adapted to operate at higher speeds with minimal effort. Under normal operation the outputs of the flip-flop circuitry are mixed with the I/Q data and sent on to the AGC amplifier. The RF9958 features an option to pass the flip-flop outputs directly to the AGC amplifier and bypass the I/Q mixers. This option is useful for dual-mode (CDMA/FM) phone designers that prefer to do frequency modulation (FM) by modulating a VCO, where the output of the VCO is connected to the LO input of the RF9958. In this instance the modulation and VCO frequencies are operated at twice the desired frequency. Pin 1 (MODE) on the part is the mode select switch that chooses either CDMA or FM mode operation. Logic "high" selects CDMA mode while logic "low" selects FM mode.

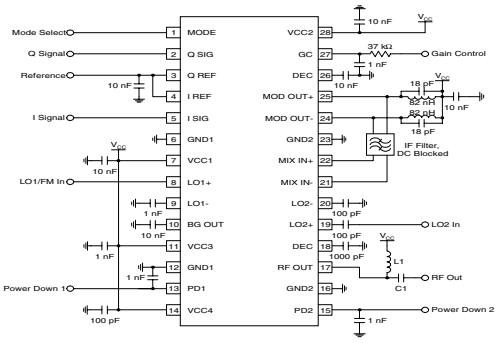


Figure 4. RF9958 Application Schematic

In the IS-98 CDMA cellular system, the cellular base station sends control signals to the mobile phone directing the transmit AGC amplifier to increment or decrement its gain in 1dB steps. As the mobile strays further from the base station, the transmit AGC amplifier is directed to increase its gain and hence, its output power, while the reverse occurs as the mobile approaches the base station. The transmit AGC amplifier in the RF9958 has an 88dB gain range and is controlled by an external DC voltage that is typically generated by a digital ASIC chip on the phone board. With a nominal 300mVp-p I/Q input signal, the AGC amplifier will output over a range of -91dBm to -3dBm into a 200Ω differential load. In FM mode, the AGC amplifier can drive +2.5dBm into the same load. The gain is controlled by varying a DC voltage on Pin 27 (GC). With a 37kΩ series resistor (refer to Figure 4), the specified voltage range is from 0.5VDC to 2.5VDC. Over the majority of the DC control voltage range, the gain adjusts with good linearity; the AGC amplifier also exhibits excellent temperature tracking (see Figure 5). Typically the output of the AGC amplifier is connected to an IF bandpass filter which in turn is connected to an upconverter.

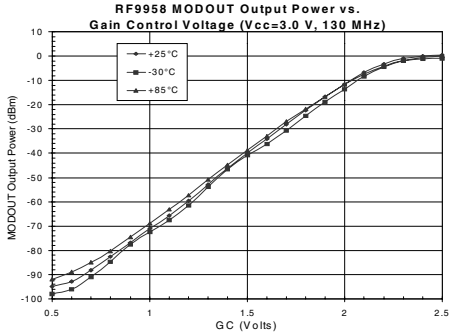


Figure 5. Plot of RF9958 AGC Output Power vs. Gain Control Voltage

The upconverter on the RF9958 is specifically designed around IS-98 specifications but its excellent performance allows it to be used in a variety of applications. It has a typical power gain of 0.5dB (source impedance = 200Ω, load impedance = 50Ω), an output IP3 of +14dBm, and a noise figure of 15dB. It also features a double-balanced mixer that provides LO and IF rejection at the RF output. The IF port is differential with a 200Ω balanced input impedance. The LO port is symmetrical and can be driven differentially or single-endedly. Since most 900MHz VCO's have single-ended outputs, the input impedance of the upconverter LO port is designed to be 40Ω single-ended into either Pin 19 (LO2+) or Pin 20 (LO2-). At the RF output of the upconverter, an impedance transformer is required to present a 50Ω output impedance. This can be accom-

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plished with just two components: a shunt inductor and a series capacitor (refer to Pin 17 in Figure 4). The shunt inductor actually serves two purposes. It acts as a choke to provide DC voltage to the upconverter and it performs an impedance transformation. The series capacitor completes the transformation to 50Ω. This L-C combination can be adjusted to conform to a system's particular frequency range.

In some cases, the quadrature modulator and AGC amplifier are needed, but an external upconverter is preferred. To accommodate an external upconverter for special applications, the RF9958 features a "power down" capability for its internal upconverter. To enable the internal upconverter, the user shorts Pin 10 (BG OUT) and Pin 15 (PD2). Pin 15 is the upconverter "power down" pin and Pin 10 provides a DC reference voltage needed to bias the active circuitry in the upconverter. To "power down" the internal converter, Pin 15 (PD2) is grounded, which results in a 20mA power supply current savings.

Receive ICs

The RF9957 performs all necessary receive IF signal amplification and then demodulates down to I/Q baseband data (see Figure 6). In a typical cellular phone receiver, a low-noise amplifier (LNA)/mixer IC amplifies and then downconverts the RF input signal from the antenna to an IF frequency (refer back to Figure 2). The IF signal then typically passes through a surface acoustic wave (SAW) bandpass filter. The RF9957 takes the signal at this point and outputs baseband I/Q data into an external mixed-signal IC.

The IF inputs of the RF9957 are designed to accommodate either differential or single-ended signals, depending on the SAW filter characteristics. In dual-mode applications where there are two different IF bandwidths, two distinct IF filters are used and thus two IF input ports are required on the RF9957. To date, most system designers have used a differential SAW filter for the CDMA path and a single-ended filter for the FM path, so the application schematic reflects these common choices (see Figure 7). The CDMA input port (Pins 4 and 5) and the FM input port (Pins 8 and 9) are selectable with Pin 14 (IN SEL). A logic "high" selects the CDMA input while a logic "low" selects FM.

The CDMA input port has a 2.4kΩ differential input impedance. An external resistor can be placed across Pins 4 and 5 to lower the input impedance of the port. The FM input port has a 1.2kΩ single-ended input impedance. The AGC amplifier consists of 4 variable gain stages where the last three are common to both the CDMA and FM signal path. So when selecting

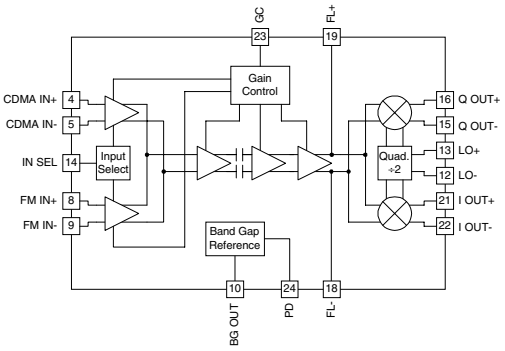


Figure 6. RF9957 Functional Block Diagram

between the two modes, the user is actually choosing which input amplifier stage is being activated.

The AGC amplifier has a typical gain range of 105dB. The typical cascade power gain of the AGC amplifier and demodulator is from -55dB to +50dB (see Figure 8). Since the power gain spec is referenced to a 500Ω source and a 5000Ω load, the cascade voltage gain is from -45dB to +60dB. The cascade noise figure and IP3 performance of the RF9957 are aimed at easy integration into an IS-98 CDMA cellular phone (see Figures 9 and 10). At the output of the amplifier, two pins are provided to allow for bandpass filtering. A parallel tank circuit will provide filtering at the receive IF frequency as well as provide a necessary DC pull-up to the power supply for the AGC output stage. (refer to Pins 18 and 19 in Figure 7).

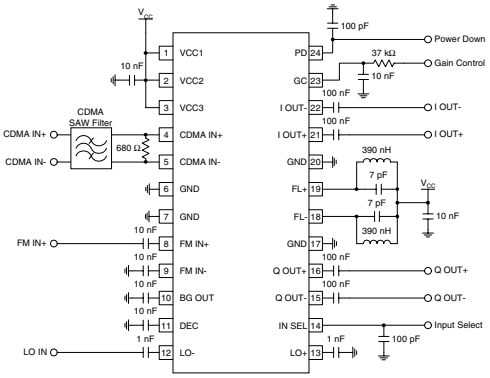


Figure 7. RF9957 Application Schematic.

The output of the AGC amplifier connects internally to the input of the demodulator. The IF signal will enter the demodulator and mix with an LO signal. The output

of the mixer will then be I/Q baseband data. The LO input port (Pins 12 and 13) can be driven differentially or single-endedly, but a differential drive will give better phase performance. The input impedance is 400Ω single-ended and 800Ω balanced. The LO circuitry in the RF9957 is very similar to the circuitry in the RF9958 in that it uses a divide-by-two flip-flop architecture to achieve phase quadrature. This implies that the LO frequency must be twice the IF frequency in order to properly demodulate down to baseband. The flip-flop circuitry limits the maximum allowable IF frequency, and in this design the flip-flop circuitry can handle up to about 500MHz (which translates to an IF of 250MHz).

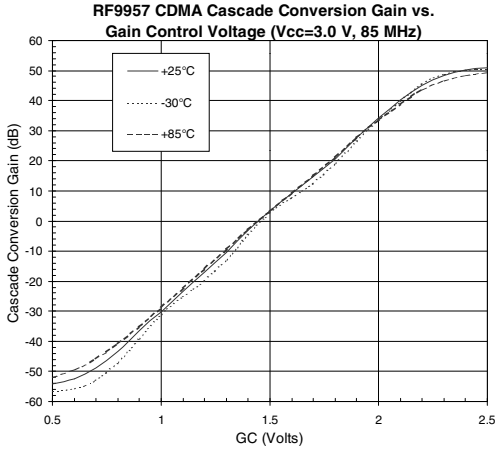


Figure 8. Plot of RF9957 Conversion Power Gain vs. Gain Control Voltage

The output of the demodulator is separated into two ports: I (Pins 21 and 22) and Q (Pins 15 and 16). Both outputs are differential and have 2kΩ balanced output impedances. The power gain specifications for the IC were written for a 5kΩ load on each of the I and Q output ports. If additional voltage gain is desired, then the load impedance should be increased. In order to save power supply current, the RF9957 incorporates a "power down" feature for the Q mixer. When the IN SEL pin is logic "low" (FM mode), the Q mixer shuts down and only the I mixer continues to operate. In CDMA mode, both mixers are in operation. Typically, the I and Q output ports will drive a mixed-signal IC which contains A/D converters and digital low-pass filters.

In order to allow greater flexibility, RF Micro Devices also offers the RF2667, which is a slight variation of the RF9957. In the RF2667, the Q mixer "power down" feature has been eliminated, so that when FM mode is

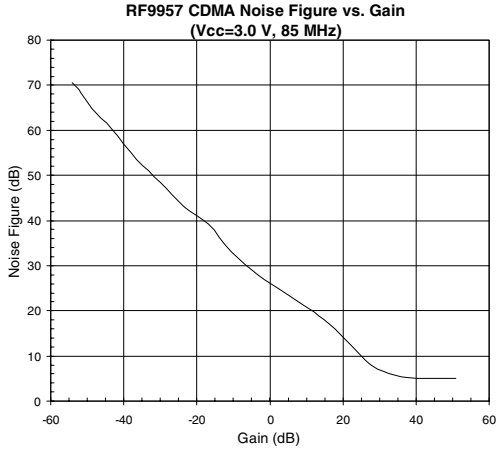


Figure 9. Plot of RF9957 Noise Figure vs. Power Gain

selected, both mixers continue to operate. This design

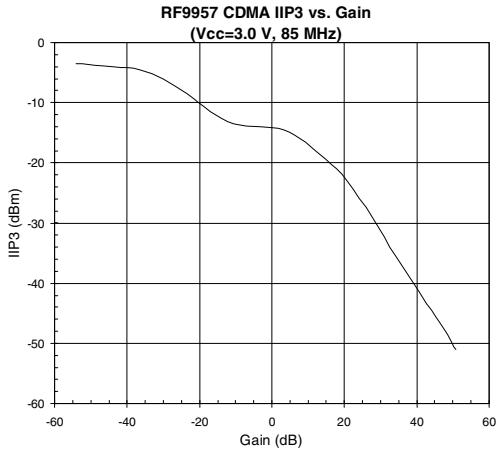


Figure 10. Plot of RF9957 Input IP3 vs. Power Gain

change was made to accommodate system architectures that require both I and Q channels to decode FM data. A second difference is in the I and Q maximum output voltage swing. The RF2667 allows up to 2.4V_{PP} balanced typical output swing before 1dB compression, whereas the RF9957 allows 500mV_{PP} This change was to allow the RF2667 to mate with A/D converters that require higher input voltage levels. Another performance variation is frequency range; the RF2667 will operate up to an IF frequency of at least 300MHz.

Conclusion

Three highly integrated IC's have been created to simplify CDMA cellular transceiver design. The RF9958 packs quadrature modulation, transmit AGC amplification, and upconversion into a single QSOP-28 plastic package. The RF9957 and RF2667 each feature receive AGC amplification and quadrature demodulation in a single QSOP-24 plastic package. All of these IC's are shipping in production volumes and are available today.

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Transmit and Receive AGC Amplifiers for CDMA Cellular/PCS Phones

Introduction

Cellular and Personal Communication Services (PCS) phones that are based on Code Division Multiple Access (CDMA) need careful regulation of signal levels on both the forward and reverse channels. In the reverse channel (mobile phone to base station) a transmit automatic gain control (AGC) amplifier must carefully adjust the output power of the mobile so that it does not dominate the input spectrum at the base station.

Each mobile's signal should arrive at the base station at the same power level; this helps ensure that capacity is maximized. In the forward channel (base station to mobile) a receive AGC amplifier adjusts to accommodate widely varying signal levels coming in from the base station. At a CDMA mobile phone antenna numerous signals sent from the cell base station are layered on a single frequency band and within this group of signals lays the desired data.

All of these signals (desired and undesired) pass through a low noise amplifier front end and then through a downconverting mixer. Immediately following the mixer the waveforms pass through a CDMA intermediate frequency (IF) bandpass filter. All of the aforementioned signals are in-band and are not filtered. Because of this condition the receive AGC amplifier cannot simply limit. The strongest signal would be limited and compress all other signals that were received, so if the desired data was not the strongest, it would be lost. It becomes clear that the receive AGC amplifier must provide linear amplification and attenuation to prevent limiting of undesired signals. RF Micro Devices has developed two integrated circuits (ICs) that perform both of these important functions. The RF2607 CDMA/FM Receive AGC Amplifier and the RF2609 CDMA/FM Transmit AGC Amplifier are both monolithic ICs that are fabricated in an advanced bipolar Silicon process. Both of these low cost, high performance ICs pack variable gain differential amplifier stages, gain control operational amplifiers, and temperature compensation circuitry within small QSOP16 plastic packages.

Transmit AGC

The RF2609 features a 90dB gain range from -48dB power gain to +42dB power gain and is powered from a single 3.6V supply. In a cellular system, the cellular base station sends control signals to the mobile phone directing the RF2609 to increment or decrement its gain in 1dB steps. As the mobile strays further from the base station, the RF2609 is directed to increase its gain and hence, its output power, while the reverse occurs as the mobile approaches the base station. The gain of the IC is controlled by a single DC voltage externally supplied by a digital-to-analog (D/A) converter which is swept from 0VDC to 3VDC. Figure 1 illustrates the gain response of the RF2609 as the gain control voltage is swept.

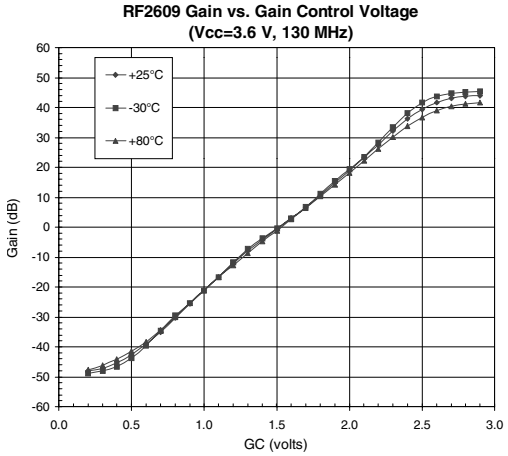


Figure 1. Gain response of the RF2609 as the gain control voltage is swept

CDMA system specifications dictate that as the gain is swept over its entire range, the transmit AGC amplifier must maintain a minimum input third order intercept point (IIP3). Another way to state this requirement is that the adjacent channel power rejection of the amplifier must remain constant regardless of the output level. This specification ensures that IS-95 transmitted spectrum requirements are met under the entire gain range of the AGC amplifier. To clarify how this affects the design, in a CDMA phone the input signal provided to the RF2609 will remain constant even while the gain is increased or decreased. Thus, the output signal will vary proportionally with the gain of the IC. Under these conditions, the third order (IM3) products must remain constant and not rise as the gain moves upward. The RF2609 uses a proprietary variable gain amplifier scheme that achieves excellent IM3 performance (see

Figure 2) while keeping down the noise figure of the device (see Figure 3). Although the noise requirements for the transmit AGC amplifier are not as stringent as that of the receive AGC amplifier, the challenging IIP3 requirements for the RF2609 make the noise figure more difficult to achieve. The final design, however, was able to meet both IS-95 specifications under nominal and worst-case conditions.

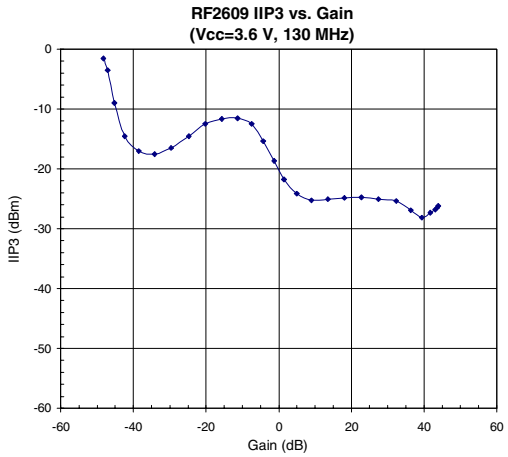


Figure 2. The RF2609 IIP3 vs. Gain

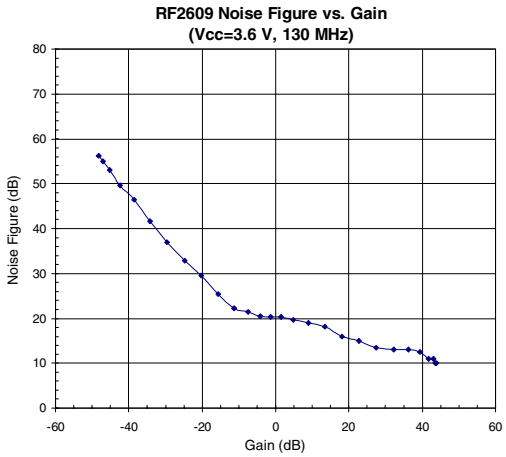


Figure 3. The RF2609 Noise Figure vs. Gain

Understanding how to incorporate the RF2609 into a transmit chain is straightforward (see Figure 4). Pins 1 and 2 are the input port for the IC.

Source Impedance

The differential impedance of the input port is 1000Ω, so for maximum power transfer, the system designer need only provide a source impedance of 1000Ω. Typically, an intermediate frequency (IF) filter will precede the RF2609 and provide a 1000Ω source impedance. If a 1000Ω filter cannot be used, a simple L-C network can be designed to perform an impedance transformation. Since there is DC present on pins 1 and 2, the source should be AC coupled through capacitors as shown in Figure 4.

Once the IF signal is fed into the IC, it travels through four variable gain amplifier stages. Each of these amplifiers is controlled by gain control circuitry, which primarily consist of operational amplifiers. External to the part, a DC gain control voltage is fed from a D/A converter and enters the IC through pin 16. In order to achieve the correct gain curve, the DC gain control voltage must pass through a 3.3kΩ resistor. A capacitor is placed from pin 16 to ground in order to lowpass filter the signal from the D/A converter. The earlier mentioned gain control voltage range of 0VDC to 3VDC is referenced to the GAIN label on Figure 4, not at pin 16.

The output port of the RF2609 consists of pins 9 and 10. The output of the IC is open collector, which means that it looks like a high impedance. Open collector also means that the output pins must be supplied DC voltage externally for the internal output circuitry to operate.

The output is left high impedance for greater flexibility and greater precision. A system designer can choose whatever output impedance they desire and use 1% resistors to guarantee good matching. The IC was designed to drive 500Ω (1000Ω output impedance in parallel with 1000Ω load) but other impedance levels can be used if the change in power gain is taken into account. Referring back to Figure 4, a 1000Ω resistor is placed across pins 9 and 10 to set the differential output impedance of the IC.

Inductors (L1) connect the power supply to the output pins. The inductors can be used with series capacitors (C2) to form an impedance transformation network if the IF filter does not look like 1000Ω.

If the filter impedance is 1000Ω, then the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the signal frequency. In this case, C2 merely acts as a DC blocking capacitor.

Receive AGC

The RF2607 features a 96dB gain range from -48dB power gain to +48dB power gain and is powered from a single 3.6V supply. As the transmit AGC amplifier is instructed to adjust its gain, the receive AGC amplifier will track, so that they work in parallel. As the mobile strays further from the base station, the RF2607 is directed to increase its gain while the reverse occurs as the mobile approaches the base station. The gain of the IC, like the RF2609, is controlled by a single DC voltage externally supplied by a digital-to-analog (D/A) converter which is swept from 0 to 3VDC. Figure 5 illustrates the gain response of the RF2607 as the gain control voltage is swept.

With this IC, the more demanding specification to meet is noise figure. In a CDMA receiver, this component follows the downconverting mixer and must retain good noise performance at the high end of the gain range. At the same time the IIP3 must increase steadily as the gain drops from the high end of the gain range. Using a variable gain amplifier scheme similar to that used in the RF2609, both requirements are achievable. At 45 dB gain the RF2607 typically produces a noise figure of 4.5dB and an IIP3 of -41dBm. Figures 6 and 7 illustrate nominal performance of the IC over the entire gain range.

Incorporating the RF2607 into a system is very simple.

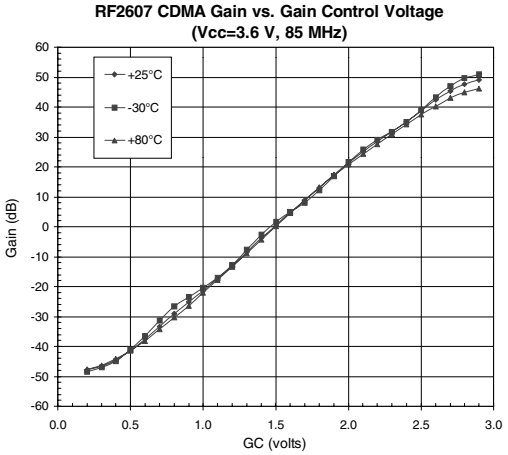
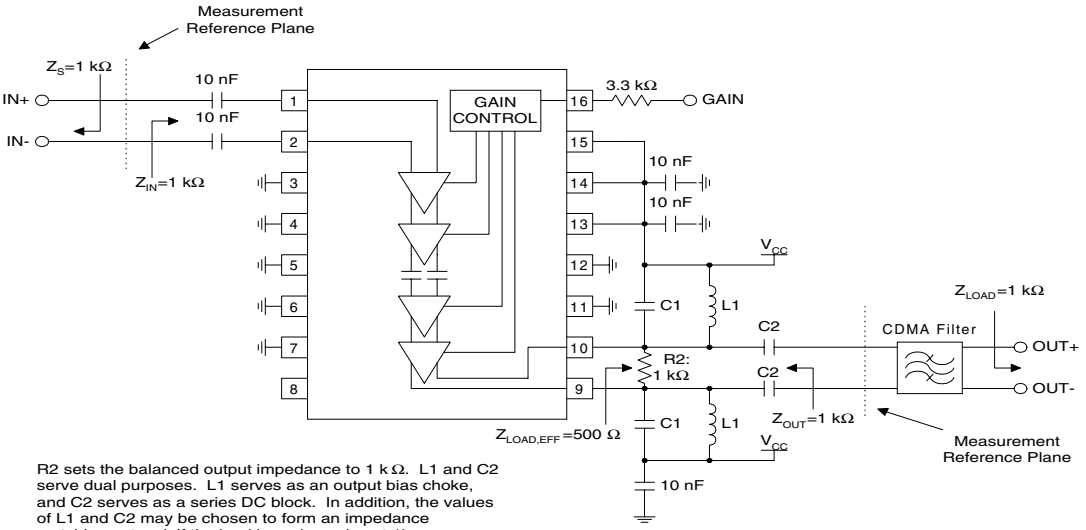


Figure 5. RF2607 CDMA Gain vs. Gain Control Voltage

The RF2607 has two input ports, one for CDMA operation and one for FM operation. This feature allows the IC to be used in dual mode phones that operate in both Advanced Mobile Phone Service (AMPS) systems and IS-95 North American Digital Cellular (NADC) systems. In dual mode systems, two signal paths are required at IF in order to filter properly. The CDMA path requires a filter with a 1.26MHz bandwidth while the



R2 sets the balanced output impedance to 1 kΩ. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the load impedance is not 1kΩ. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 1 kΩ.

Figure 4. RF2609 Application Circuit

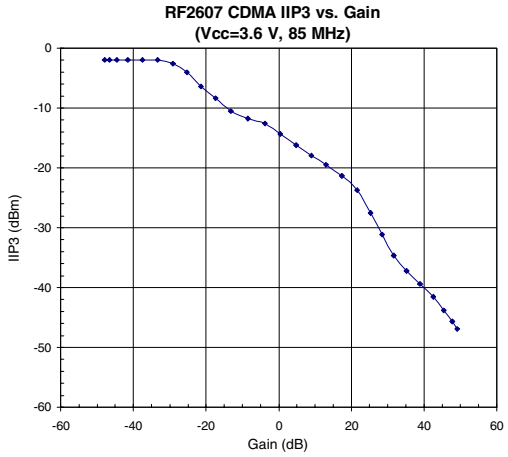


Figure 6. RF2607 CDMA IIP3 vs. Gain

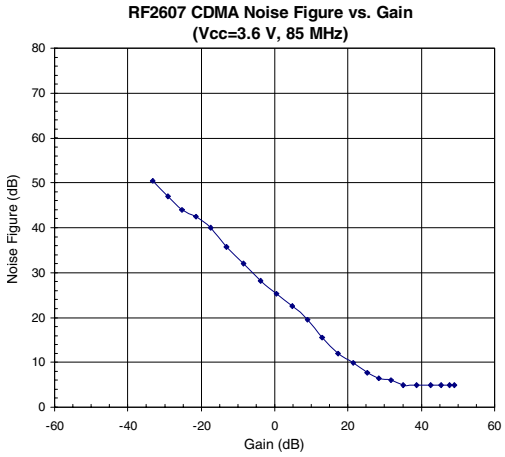


Figure 7. RF2607 CDMA Noise Figure vs. Gain

FM path requires a filter with a 30 kHz bandwidth. The RF2607 accommodates both paths by providing two separate inputs that can be switched. Even though there are two inputs, there is virtually no difference in RF2607 performance between the two modes. The SELECT pin (pin 7) is a digital switch which determines in which mode the IC will be. Logical high corresponds with CDMA mode while logical low corresponds with FM mode.

In CDMA mode, pins 1 and 2 are the balanced input port and the differential input impedance is 1000Ω. To guarantee a good match to a 500Ω IF filter (see Figure 8), a 1000Ω 1% resistor (R1) is placed across the input port. The IC can operate with a higher or lower impedance filter by merely adjusting the external 1% resistor. The noise figure, gain, and IIP3 specifications, however, are all based upon the configuration in Figure 8. Once the IF signal is fed into the IC, it travels through four variable gain amplifier stages. Like the RF2609 each of these variable gain amplifiers is controlled by operational amplifiers. External to the part, a DC gain control voltage is fed from a D/A converter and enters the IC through pin 16. In order to achieve the correct gain curve, the DC gain control voltage must pass through a 4.7 kΩ resistor, which, together with a capacitor to ground, forms a lowpass filter to clean up the signal from the D/A converter. Like the RF2609 the gain control voltage range of 0 to 3 VDC is referenced to the GAIN label on Figure 8, not at pin 16.

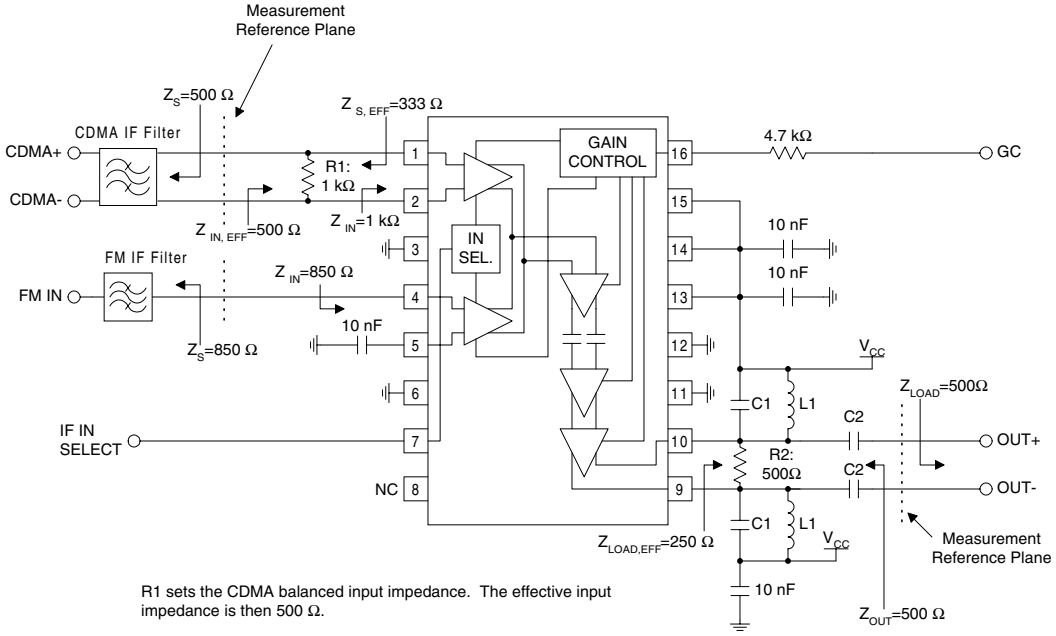
In FM mode, pins 4 and 5 are the balanced input port and the differential input impedance is 1000Ω. In FM mode, however, most system designers prefer to couple into the part single-endedly. In this case pin 4 or pin 5 can be used as the input port with the other pin AC coupled to ground. The single-ended input impedance is then 850Ω.

The output port of the RF2607 consists of pins 9 and 10 and is open collector. Since the output is open collector, the power supply must be fed through inductors. As with the RF2609, the output impedance and load can be varied. Typically, a 500Ω resistor is placed across pins 9 and 10 to set the differential output impedance of the IC. Referring to Figure 8, inductors (L1) connect the power supply to the output pins. The inductors can be used with series capacitors (C2) to form an impedance transformation network if the IF filter does not look like 500Ω. If the filter impedance is 500Ω, then the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the signal frequency. In this case, C2 merely acts as a DC blocking capacitor.

Alternative Architecture

An alternative CDMA phone architecture integrates additional components with both AGC amplifiers. In the transmit chain, a quadrature modulator is added in front of the AGC amplifier so that the system designer interfaces with a baseband input port. In this case, I and Q data drives the IC at baseband frequencies and is upconverted to IF where the AGC amplifier takes over. The RF9958 CDMA Transmit IC includes both the modulator and AGC amplifier as well as an RF upconverter. The upconverter can be powered down if the

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R1 sets the CDMA balanced input impedance. The effective input impedance is then 500 Ω.

R2 sets the balanced output impedance to 500 Ω. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network of the load impedance is not 500 Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the load impedance is 500 Ω.

Figure 8. RF2607 Application Circuit

system designer only wishes to use the modulator/ AGC section. In the receive chain, a demodulator is added to the receive AGC amplifier. In this case, the output of the part is I/Q data at baseband frequencies.

The RF9957 CDMA Receive IC includes both of these functions. Both the RF9957 and RF9958 operate from a single 3V power supply.

Summary

The RF2607 and the RF2609 are two critical components of the RF section of a CDMA phone (see Figure 9). Both of these IC's were designed to meet all of IS-95's worst-case requirements and are available in high volume at low cost. Please call RF Micro Devices' Marketing Department for additional information and details on these two products, or any others, at 910-664-1233. Also, please check our web page at www.rfmd.com.

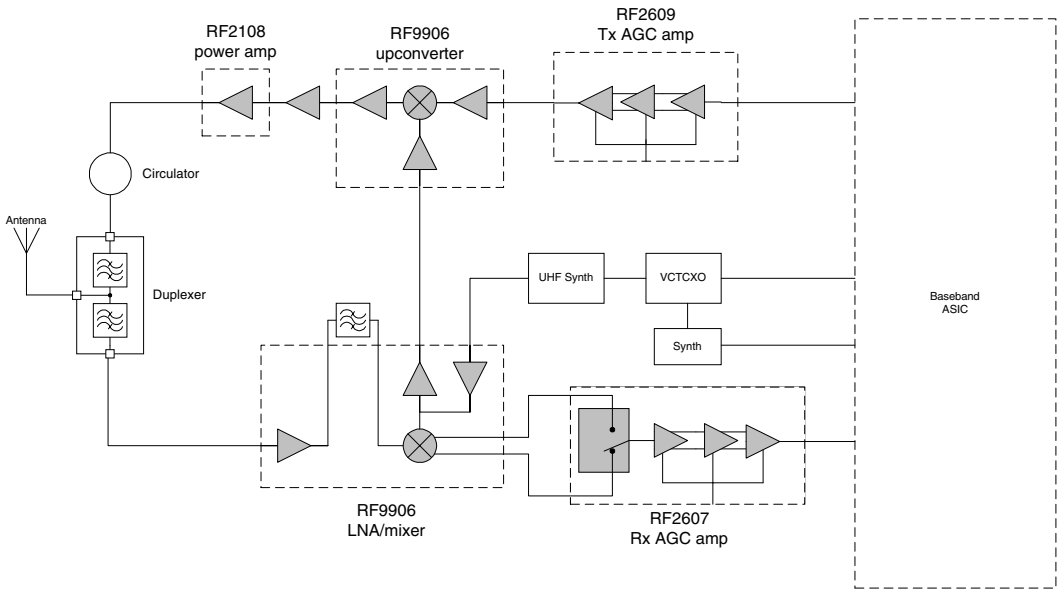


Figure 9. CDMA System Simplified Block Diagram

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Frequency Synthesis Using the RF2510

Introduction

Narrow band receivers utilizing crystal referenced phase locked loops (PLL) allow for cost effective transmitters, receivers, and transceivers to be constructed with receiver sensitivities in the -97dBm range for frequency shift keying (FSK) with bit error rates (BER) of 10^{-4} (-94dBm for amplitude shift keying (ASK)). This is possible because of the availability of low cost crystals, which provide the required frequency accuracy to use narrow band IF filters. These 10.7MHz ceramic filters come in bandwidths of 110kHz to 360kHz and are available (in volume) for less than 40 cents each. SAW solutions are accompanied by frequency tolerances and drift on the order of 200kHz as compared to 50kHz for a crystal available (in volume) for less than 50 cents. In applications such as the European 868MHz to 870MHz ISM band, the majority of the allocated bandwidth must be used to accommodate the SAW center frequency drift (Subband A 600kHz, Subband B 500kHz), leaving little room for modulation sidebands. Noise bandwidth for the SAW approaches is typically 800kHz. Sensitivities of the SAW solutions are in the -80dBm range due to the increased noise bandwidth as well as receiver noise figure. The PLL approach offers approximately 7dB of sensitivity improvement due to decreased noise bandwidth and 7dB due to receiver noise figure.

The RF2510 is a Frequency Synthesizer Integrated Circuit designed for use in ISM Band Transmitter Products, including the European 433.05MHz to 434.79MHz and 868MHz to 870MHz Bands, as well as the United States 902MHz to 928MHz Band. In general, the RF2510 can be used over the 300MHz to 1000MHz range. The RF2510 integrates PLL components such as a voltage controlled oscillator (VCO), prescaler, crystal oscillator (RefOsc), phase detector, charge pump, and power down circuitry. A modulation pin is also provided for FM or FSK applications using on-chip diodes. The RF2510 is available in 16 pin plastic surface mount packaging (SSOP-16). With a 9mA typical current draw at 3Volts and 10.5mA at 3.6Volts, the RF2510 is well suited for battery powered applications.

This article discusses the design and measurement of a frequency synthesizer to be used in ISM band applications. The formulas used for calculation of key parameters are presented and measurement results are shown. Particular emphasis is given to the tradeoffs between loop bandwidth and phase noise, two key parameters of any frequency synthesizer design. All measurements were performed with a spectrum analyzer, and the data presented is typical of a standard product evaluation board routinely assembled for customer sampling.

Design Features

Figure 1 shows a functional block diagram for the RF2510. The crystal oscillator topology is a modified Colpitts type which requires two external capacitors as well as the crystal to be connected to Pins 1 and 2 as shown. In addition, an external reference oscillator can be injected at Pin 1 when one is already available, eliminating the need for the Colpitts circuitry discussed above.

Pin 4 is the output of the transmitter. An output attenuator can be used to decrease sensitivity to output VSWR and a harmonic filter is used to meet the ISM band specifications.

The power down pin (Pin 7) is used to disable the onboard voltage reference. It is active low so that a DC voltage less than 1Volt powers down the RF2510. Current consumption in power down mode is less than 1microamp.

The division ratio N of the prescaler is controlled by the logic levels at Pins 9 and 10. Depending on the combination shown in Figure 1, divisors of 64, 65, 128, or 129 can be achieved.

Pins 11 through 13 are associated with the VCO. MODIN (Pin 12) is connected to the smaller tuning diodes used to FM or FSK the VCO. An external varactor circuit is connected between Pins 11 and 13 for locking the VCO to the required center frequency as well as flexibility in tuning range and/or sensitivity. The VCO inductors are connected to Pins 11 and 13 and they serve to set the center frequency as well as provide bias current to the oscillator.

The outputs of the on-chip charge pumps are connected to the loop filter pin (Pin 14). A common loop filter for low cost synthesizers is a one port three element passive filter, however higher performance two port passive or active filter topologies could also be used. The voltage on the loop filter pin tunes the varac-

tor of the VCO.

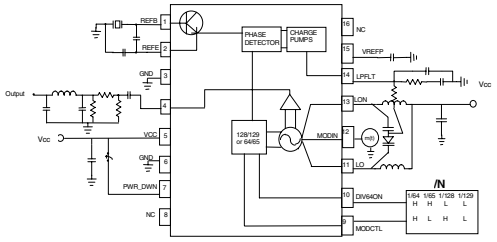
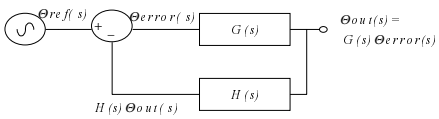


Figure 1. RF2510 Functional Block Diagram

Charge Pump PLL Design

Figure 2 shows a block diagram of a generalized PLL showing the feedforward function G(s) and feedback function H(s). The transfer functions of the PLL can be expressed in terms of these functions as shown.



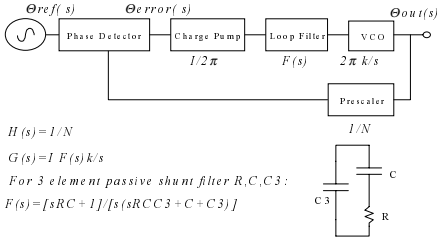
$$\Theta out(s) = G(s)\,\Theta error(s)$$
$$G(s)[\Theta ref(s) - H(s)\,\Theta out(s)]$$
$$G(s)\Theta ref(s) - G(s)H(s)\,\Theta out(s)$$

$Acl = \Theta out(s)/\Theta ref(s) = G(s)/[1 + G(s)H(s)]$ Closed loop gain

$Aol = G(s)H(s)$ Open loop gain

Figure 2. General PLL Transfer Functions

Figure 3 shows the design of a third order type 2 charge pump based PLL. The loop filter for this design is a one port, three element passive filter. All the design equations needed for the loop design are shown in Figure 3. Phase margins of 45 degrees to 60 degrees are typically used to guarantee loop stability.



$H(s) = 1/N$

$G(s) = I\,F(s)\,k/s$

For 3 element passive shunt filter R,C,C3:

$F(s) = [sRC + 1]/[s(sRCC3 + C + C3)]$

$$Aol = G(s)H(s) = I\,F(s)\,Kv/Ns$$
$$\frac{I\,Kv(sRC + 1)}{Ns^2(sRCC3 + C + C3)}$$

Type 2 since two poles at origin. Will lock to step change in phase or frequency. Constant phase error for ramping frequency shift(acceleration)

$Acl = G(s)/[1 + G(s)H(s)] =$ Third Order C.E. in denominator

ϕm = phase margin, deg
fo = loop BW, Hz
wo = loop BW, rad/sec
k = VCO tuning sensitivity, Hz/V
I = Charge pump current, Amps
N = Prescaler Divisor

$$t1 = \frac{\tan(\phi m) + \sec(\phi m)}{wo} \qquad K = \frac{kI}{N}$$

$$t2 = \frac{1}{wo^2 t1} \qquad Co = \frac{K}{wo\sqrt{\frac{1 + wo^2 t1}{1 + wo^2 t2}}}$$

$$C3 = t2\frac{Co}{t1} \qquad C = Co - C3 \qquad R = \frac{t1}{C}$$

$$tlock = 4/fo$$

Figure 3. Charge Pump PLL Design Equations

Figures 4 and 5 show the open loop gain and phase for a sample PLL. As can be seen, the loop BW is 5kHz and the phase margin is 60 degrees. The loop BW is defined as the frequency where the open loop transfer function reaches unity gain and the phase margin is the difference between the phase at unity gain and 180 degrees.

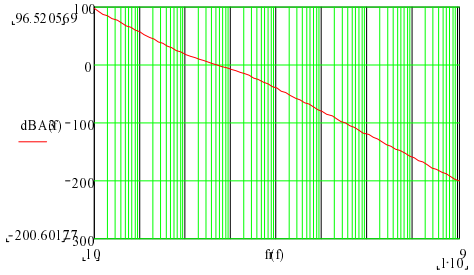


Figure 4. Open Loop Gain

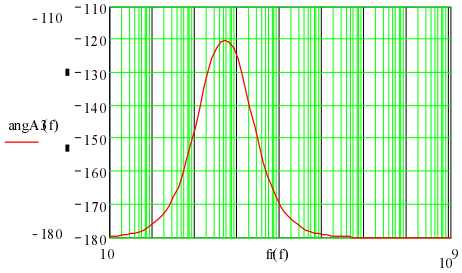


Figure 5. Open Loop Phase

Noise Analysis

Oscillator phase noise is usually characterized with Leeson's model (as shown in Equation 1). The oscillator active device has a 1/f phase noise corner frequency. This is approximately 5kHz for Silicon NPN and 5MHz for GaAs MESFET at 900MHz. When placed in a feedback loop to form an oscillator this 1/f phase noise is scaled by the circuit group delay $\tau=2Q_L/\omega_0$ into frequency noise. Since phase is the integral of frequency, the resulting frequency noise spectral density is divided by the offset frequency to convert or integrate to phase noise. The term in Equation 1 is squared because L(f) is a noise power ratio. The noise floor of the oscillator is determined by the amplifier compressed gain, noise figure, output power, and thermal noise (kT). When the 1/f model terms drop below the noise floor, Equation 1 is approximately equal to the noise floor.

$$L(f) = 10\log\left[\left(1+\left(\frac{f_o}{2f(Ql)}\right)^2\right)\left(1+\frac{f_c}{f}\right)10^{(G+NF+kT+Po)/10}\right]$$

f_o = oscillator center frequency, Hz
f = offset frequency, Hz
Ql = loaded resonator Q
f_c = active device 1/f corner frequency, Hz
G = compressed Gain of active device, dB
NF = noise figure of active device, dB
kT = -174 dBm Thermal noise
Po = oscillator output power, dBm

Equation 1. Leeson's Formula for Phase Noise

Figure 6 shows phase noise calculated for a reference oscillator at 7.15MHz and a VCO at 915.2MHz. The floors of the two oscillators are approximately the same, while the very large Q of the crystal oscillator results in much lower 1/f noise.

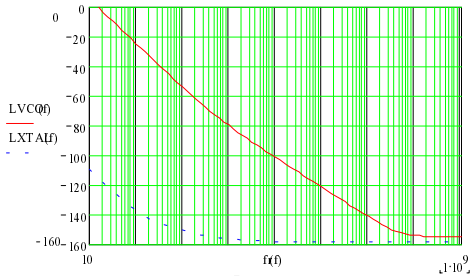


Figure 6. Oscillator Phase Noise

Figure 7 shows several PLL noise transfer functions of interest to estimate PLL phase noise. The reference oscillator and divider noise will be multiplied by the closed loop PLL transfer function. Inside the loop bandwidth, this is equivalent to adding 20logN to the phase noise of both the reference oscillator and the divider.

Outside the loop bandwidth, contributions by the reference oscillator and divider to the phase noise characteristic are attenuated due to the lowpass characteristic of the closed loop transfer function. The VCO noise is multiplied by a highpass function which is inversely proportional to the open loop gain. It is unity for offsets much greater than the loop bandwidth and rolls for offsets less than the loop bandwidth.

The third noise transfer function is that due to noise on the VCO tune line coming from the phase detector. This noise voltage will modulate the VCO and impact the overall phase noise. Since it is injected at a point between previously defined transfer functions, it can be scaled by the phase detector gain Kpd and then multiplied by the closed loop gain to get its contribution to

the output. This equation is shown in Figure 7 and Figure 8 shows the noise characteristic of the VCO, the Reference Oscillator + 20logN, the Divider noise +20logN, and a noise voltage on the tune line multiplied by the phase detector noise gain. Note that this noise voltage could arise from a number of sources, including varactors in the VCO, loop filter components, or from the phase detector/charge pump circuitry.

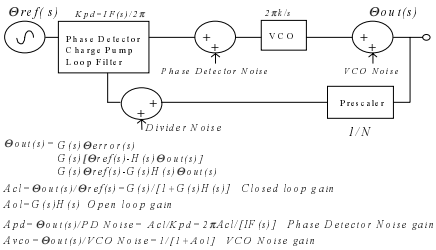


Figure 7. PLL Noise Transfer Functions

For an optimal phase noise design, loop bandwidth is normally chosen as the intersection of the VCO curve and the multiplied reference or divider curve, whichever occurs at the lower frequency. In the case of Figure 8, this would be approximately 20kHz. In other instances lock time may be of prime concern and bandwidth is set to approximately 4 divided by the locktime. Also, when direct modulation of the VCO is required, the loop BW must be set lower than the modulation frequency in order to keep the PLL from canceling the modulation. Manchester encoding can be used to keep long strings of 1's or 0's from being cancelled by the PLL, due to their low apparent frequency despite the higher data rate.

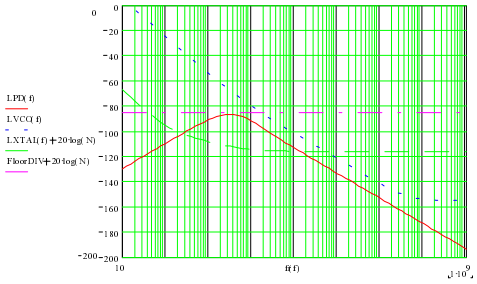


Figure 8. PLL Phase Noise Contributors for BW=5kHz

Figure 9 shows the results of multiplying the noise sources by their respective transfer functions and Figure 10a shows the composite noise curve generated by the RMS sum of the four noise curves. Note the peaking in the noise characteristic due to the loop bandwidth being set below the crossover frequency shown in Figure 8. Figure 10b shows the result if the loop BW is set to 100kHz. In this case, the result is a pedestal in the noise response caused by the divider noise.

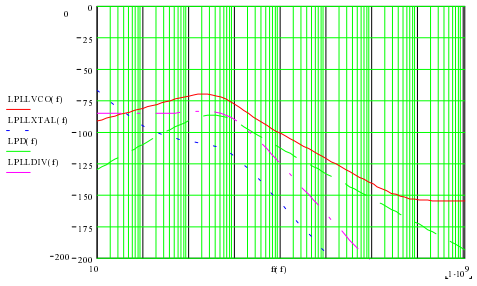


Figure 9. PLL Noise Contributors for BS=5kHz (modified by PLL)

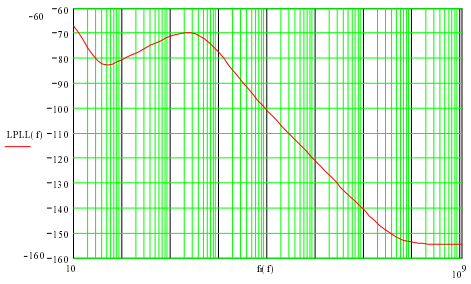


Figure 10a. Overall PLL Phase Noise (BW=5kHz)

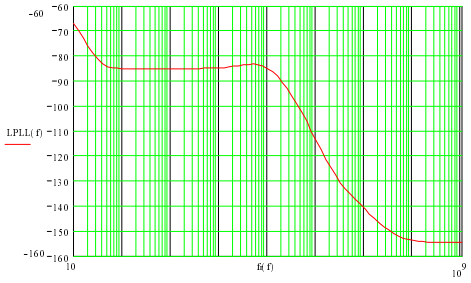


Figure 10b. Overall PLL Phase Noise (BW=100kHz)

Figure 11 shows measured PLL phase noise for bandwidths of 5kHz and 100kHz. Figure 11a indicates a phase noise at 10kHz offsets of -49-31=-80 dBc/Hz, taking into account the 1kHz resolution BW. Figure 11b indicates a phase noise of approximately -65-35=-100 dBc/Hz at 100kHz offsets. Figure 11c shows the phase noise for 100kHz BW, which has the same noise pedestal shown in Figure 10b. Figure 12 shows measured phase noise data at 10kHz and 100kHz as loop BW is varied. From this plot the optimum loop BW for phase noise can be seen to be in the 10 to 20kHz range. Due to modulation at 9600 baud, the RF2510 evaluation boards are typically configured for 5kHz loop BW.

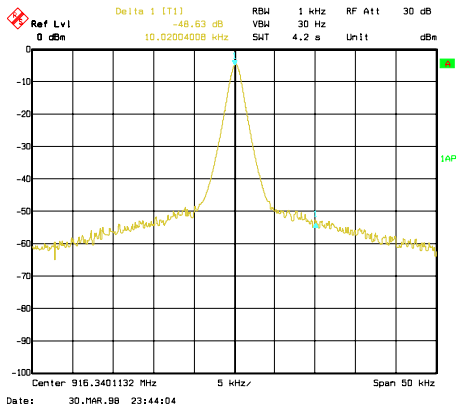


Figure 11a. Measured Phase Noise (BW=5kHz)

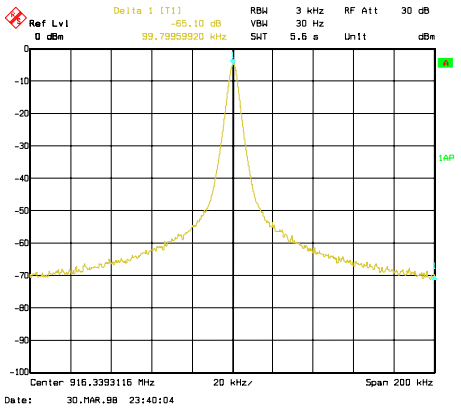


Figure 11b. Measured Phase Noise (BW=5kHz)

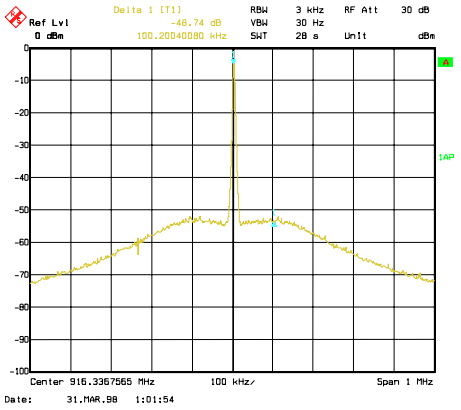


Figure 11c. Measured Phase Noise (BW=100kHz)

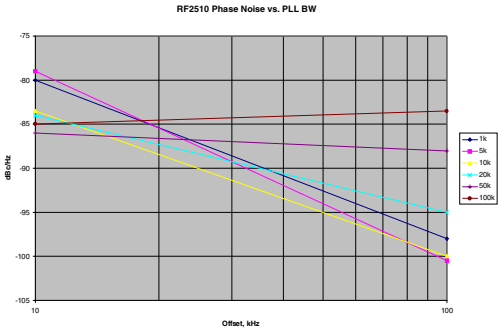
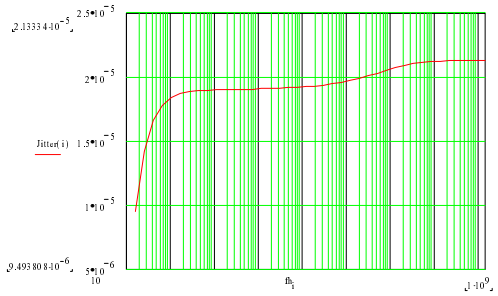


Figure 12. Measured Phase Noise as a Function of Loop BW

Once the phase noise characteristic is obtained, information such as Jitter, RMS Phase Deviation, and RMS Frequency Deviation or Residual FM can be determined. Jitter is obtained by integrating the phase noise over a specified bandwidth. Figure 13 shows results of this integration for different bandwidths using 10Hz as the lower limit. For upper limits of 100Hz and above, the Jitter is approximately $2x10^{-5}rad^2$. RMS Phase Deviation is the square root of the Jitter. Figure 14 shows the RMS Phase Deviation in degrees. For upper limits of 100Hz and above, the RMS Phase Deviation is approximately .25degrees. RMS Frequency Deviation or Residual FM is obtained by multiplying the phase noise by a frequency term and then integrating over a specified bandwidth. Figure 15 shows the RMS Frequency Deviation or Residual FM which is approximately 1Hz for an upper limit of integration of 3MHz. In practice, this upper limit is determined by filters which limit the noise bandwidth. Figure 16 shows the equations for calculating the above parameters from phase noise plots and Table1 shows some data sheet parameters for the RF2510.



.Figure 13. Jitter in rad^2 for BW=10Hz-fhHz

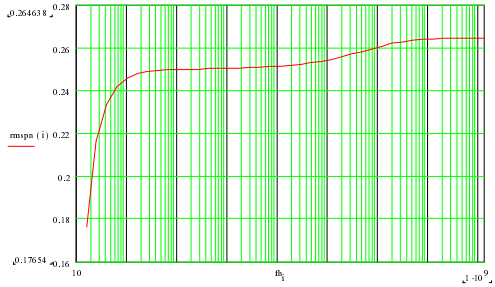


Figure 14. RMS Phase Deviation in deg for BW= 10Hz-fhHz

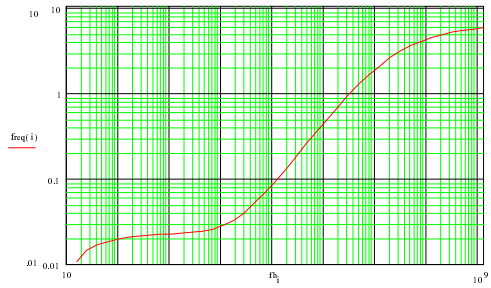


Figure 15. RMS Frequency Deviation or Residual FM in Hz for BW= 10Hz-fhHz

$$Jitter := \int_{fl}^{fh} 2 \cdot L(f)\, df \quad rad^2$$

$$RMSPhase := \sqrt{Jitter} \cdot \frac{180}{\pi} \quad deg$$

$$RMSFrequency := \sqrt{\int_{fl}^{fh} 2 \cdot L(f) \cdot f^2\, df} \quad Hz$$

Figure 16. Parameters Calculated from L(f)

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Table 1. RF2510 Data Sheet Parameters

Parameter:		Specification		Units
	Min	Typ	Max	
General Characteristics				
Frequency Range	300	433, 868, 915	1000	MHz
Modulation Options		FM/FSK		
Transmitter RF Characteristics				
Output Power (50 ohm load)		-5.5		dBm
Modulation Rate			2	MHz
Max. FM Deviation	200			kHz
PLL/Prescaler Characteristics				
Prescaler Divide Ratio		64/65/128/129		
PLL Lock Time		4/Loop BW		ms
PLL Phase Noise (100kHz offset, 5kHz Loop BW)		-98		dBc/Hz
Crystal Startup		2	4	ms
Max. Crystal Rs		50		Ω
Charge Pump Output Current		+/-40		uA
Harmonics (with three element lowpass filter on board)		-50	-41.25	dBm
Spurious		-62	-49.2	dBm
VCO Gain, K_{VCO} (dependent upon external components)		70		MHz/V
Power Supply				
Operating Voltage	2.4	3.6	5.0	V
Tx Mode Current Consumption (3.6V)	7.5	10.5	13.5	mA
Sleep Mode Current Consumption			1	uA
Temperature Range	-40		+85	°C
Package		16 pin QSOP, plastic		

Note 1: The PLL Lock time is externally programmable through appropriate selection of an external resistor and capacitor (see application circuit)

Conclusion

The RF2510 is a Frequency Synthesizer Integrated Circuit designed for ISM Band transmitter applications. Its features have been discussed, and trade-offs between PLL parameters and phase noise have been presented. The RF2510 integrates PLL components such as a VCO, prescaler, RefOsc, phase detector, charge pump, and power down circuitry. The IC is available in industry standard SSOP-16 packaging and can be used to construct low cost transmitters.

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4. Leeson, D.B. “A Simple Model of Feedback Oscillator Noise Spectrum”, Proceedings of the IEEE, Vol. 54, Feb. 1966, pp. 329-330.
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A 3V HBT Power Amplifier for CDMA/AMPS Handsets

Abstract
A high power, high efficiency, low cost power amplifier has been developed utilizing commercial gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) technology. The RF2152 is suitable for 3V applications, especially CDMA/AMPS handsets. Operating in the IS95 bandwidth with a supply voltage of 3.4V, the amplifier can provide 28dBm of output power (meeting IS95 linearity requirements), with 30dB of gain and a power added efficiency (PAE) of 38 percent.

Introduction

The RF2152 is the latest addition to a family of power amplifiers introduced by RF Micro Devices (RFMD) utilizing GaAs HBT technology. This commercially proven technology has several advantages over other technologies, such as MESFET or PHEMT. Since HBT's are bipolar, no negative bias is required, nor is it necessary to include a charge pump to generate this voltage, which adds die count and cost to the product. The HBT can be completely powered down using a control voltage, eliminating the need for a drain supply switch used in MESFET designs. RFMD's HBT process also utilized backside vias, resulting in low ground inductance when used in conjunction with a slug type package. The amplifier is packaged in a 16-pin EDSSOP package, and has been developed with low cost 0402 size components for minimizing application circuit size.

The performance summary of the RF2152 power amplifier is shown below.

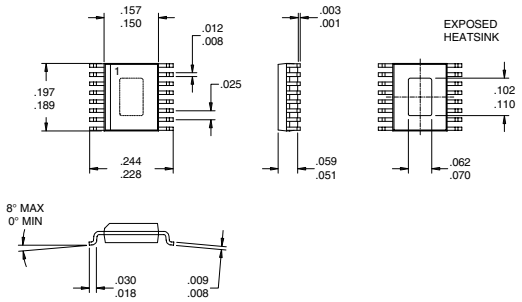
Frequency	824MHz to 849MHz
V_{CC}	3.0V to 5.0V
Output Power	31dBm AMPS 28dBm CDMA
Gain	30dB
Linearity	-44dBc @ 885kHz -56dBc @ 1980kHz
PAE	55% AMPS 38% CDMA

The RF2152 can also be tuned for JDMCA/TACS (877MHz to 924MHz) with similar performance.

Package Description

The RF2152 power amplifier is packaged in an EDSSOP-16 package with backside ground. The dimensions for this package are shown in Figure 1.

Figure 1: PSSOP-16 Package Outline



Advantages of Using an MMIC Power Amplifier

There are currently two options available for the power amplifier in a CDMA handset. The first is a module that usually consists of a single package containing the power amplifier die, and several components used for matching and bias decoupling. The other option is to use a packaged power amplifier MMIC, and design a matching network externally on the phone PCB. RFMD is currently developing products for both of these options, with the RF2152 being a packaged MMIC amplifier requiring external components.

The advantage of the packaged amplifier becomes obvious when choosing the operating voltage for the handset. In discussions with various vendors, it was found that approximately 50 percent of handset designs for the 3V CDMA market will use a regulated V_{CC}. In this case, there will be a single output impedance that will result in optimum performance from the power amplifier. Modules are typically designed to operate across the entire possible region of operation, typically 3.0V to 4.3V, for a lithium ion battery-powered design. This requires a compromise in load line design, since the module cannot be opened and retuned for the various applications. Of course, for the other 50 percent of the handset designs, this load line (designed for a wide range of V_{CC}'s) can also be implemented on the PCB for MMIC power amplifiers.

The following discussion shows the variation in load lines for two supply voltage conditions. The calculation of the correct load line can be approximated by the equation:

RL={(V_{CC}-VSAT)^2}/(2*PSAT)
(Assuming a real load line)

Where
VCC=the supply voltage for the handset.
VSAT=the saturation voltage for the transistor (for this example, 0.4V will be used).
PSAT=the saturated output power of the amplifier, typically 3dB above linear output power for a CDMA power amplifier.

For a 3.0V handset application, with 28dBm output power at the power amplifier:
RL=2.7ohms

However, for a 4.3V handset application, with 28dBm output power at the power amplifier:
RL=6.04ohms

In the case of a handset design using an unregulated supply voltage, a load line must be designed that will allow the part to meet CDMA specifications under all these conditions. So it is obvious a compromise must be made. In the case of a handset design using a regulated V_{CC} design, however, an optimum load line can be used *if the tuning is accessible to the handset designer*. Using an MMIC power amplifier makes this optimization possible.

High Volume Low Cost Commercial HBT Technology

The RF2152 utilizes the TRW/RFMD high volume low cost commercial HBT process. This is a mature process developed by TRW in the late 1980's. Since the early 1990's, TRW and RFMD have worked together to optimize this process for low cost commercial applications. A unique feature of this process is the utilization of molecular beam epitaxy (MBE), which is an accurate and repeatable method for growing the various transistor layers. Previously viewed as an expensive research process, MBE is now being used in low cost commercial processing. This has been accomplished through the development of multi-wafer MBE reactors at TRW. This results in better uniformity and reduced process variation when compared with older MOCVD-type processes.

A major milestone in the success of this process was reached with the recent announcement of the completion of the world's largest HBT fab located at RFMD's headquarters in Greensboro, North Carolina. With the implementation of cross-linked manufacturing, RFMD and TRW will now provide customers with two geographically separated manufacturing locations for high volume production using the same process. The only difference is the transition to four-inch wafers at the RFMD fab. This results in a 70 percent increase in parts per processed wafer.

Manufacturing Advantages of Using HBT Technology

As mentioned earlier, the TRW/RFMD HBT process takes advantage of high volume MBE-based transistor growth. In an HBT transistor, the critical geometries are vertical, and are controlled during this MBE process. This is very different from MESFET technologies, where critical geometries are based on photolithographic processing steps that are dependent on mask alignment and optical resolutions.

Additionally, the turn-on voltage (VBE) of an HBT is controlled by the bandgap of the structure, and is not a function of processing. With MESFET's, the turn-on voltage (VT) is greatly affected by processing, especially surface effects such as traps. This results in large variations in bias current, which are commonly corrected using expensive post processing adjustments such as laser trimming resistors.

the HBT process also allows wafers to be completed and stockpiled, thus eliminating several steps from the critical path of production development.

Finally, the minimum geometries in the HBT process are 2μm, typically two to four times the gate geometries found in MESFET's. This also increases the manufacturability of this process.

Design Advantages of Using HBT Technology

There are many advantages to using HBT technology in power amplifiers, rather than the older MESFET and HEMT-based approaches. One of the biggest is simplicity for the customer's designs. HBT's, unlike MESFET's, do not require any negative voltages for operation, so a charge pump is not required either in the IC package (where it will use current) or in the handset (where it will add cost).

Another advantage is power control. All power amplifiers require some means of power-down control to reduce battery current consumption when not in use. In MESFET-based designs, the conventional means for power-down control is to use an external "drain side switch" to disconnect the battery voltage, and shutting down the charge pump supplying gate bias. This "brute force" approach is required because the alternative would be to design a charge pump to provide additional negative voltage to fully deplete the MESFET, which would consume too much current.

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There are two negative results with using a drain side switch. First, the cost of an added component. Second, the voltage drop across the switch, which must be considered when comparing PAE results with HBT power amplifiers.

For example, assuming two amplifiers (one MESFET and one HBT), both operating at 3.0V, 28dBm out, 40 percent PAE, and the drain side switch has a voltage drop of 0.15V. This would require that 3.15V be supplied to the MESFET amplifier to have 3.0V at the drain. This would result in a drop of two PAE percentage points.

Looking at this another way, the affect of a drain side switch on talk time is even more apparent. Assuming the battery was allowed to run down to 3.0V before shutting the phone off, and both PA running at 40 percent efficiency, the following currents are derived:

PA without drain switch (i.e., HBT PA)
28dBm out=0.63W
40 percent PAE

I_{CC}=0.63W/(3.0V*0.4)

I_{CC}=525mA

However, in a PAE with a drain switch, the voltage at the drain will be 2.85V. Assuming the load line was reoptimized to provide 40 percent PAE, the current required will be:

I_{DD}=0.63W/(2.85V*0.4)

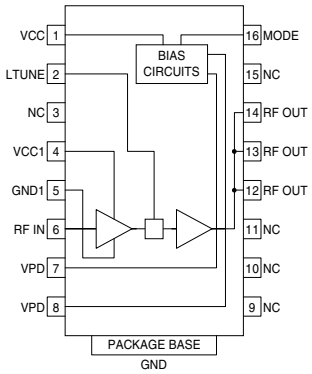
I_{DD}=552mA

The result is a five percent increase in current consumption in a FET-based amplifier at low battery voltage.

Theory of Operation and Applications

A functional block diagram of the RF2152 is shown in Figure 2.

Figure 2: Block Diagram of RF2152



As shown above, the RF2152 is a two-stage power amplifier with internal bias circuits. Interstage tuning is accomplished partially off-chip to account for board ground inductance from various manufacturing technologies. Power down and low power modes are controllable via external pins.

The first stage ground is brought out through a separate pin for isolation from the output stage. The output stage is grounded through the package slug.

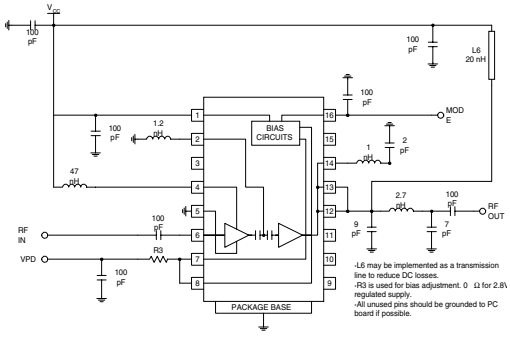
The following is a description of the various I/O's.

Pin	Function
1	Supplies VCC to the bias circuits
2	Interstage tuning control
3	No Connect
4	Supplies VCC to the first stage
5	Ground for the first stage
6	RF input
7	Bias fine control
8	Power down control
9	No Connect
10	No Connect
11	No Connect
12	RF Out
13	RF Out
14	Harmonic Trap
15	No Connect
16	VMODE (output bias adjustment

Application Circuit

The application schematics for the most common applications (IS95 CDMA) are shown in Figure 3.

Figure 3: RF2152 Applications Circuit



It should be noted that many of the capacitors shown for bias decoupling have been found necessary to reduce test equipment noise on a test bench, but unnecessary in an actual handset with a battery.

The evaluation board layout, containing the power amplifier and matching components, may be found in the RF2152 data sheet.

Performance over Wide Supply Voltage Variations

To demonstrate the possible utilization of the RF2152, typical parts were tuned for use across a wide supply voltage range of 3.0V to 5.0V. This would demonstrate the typical requirements of a handset using very low cost NiCad batteries with a typical charger voltage of 5.0V. Figures 4 through 18 show the amplifier performance overall bias and temperature conditions, *without retuning the part*.

Figure 4: CDMA Mode: Adjacent Channel Linearity

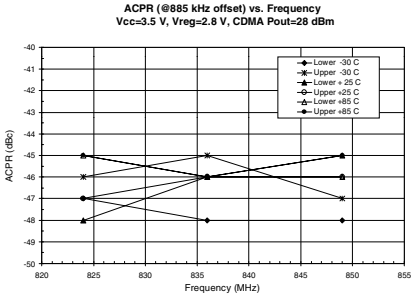


Figure 5: Alternate Channel Linearity

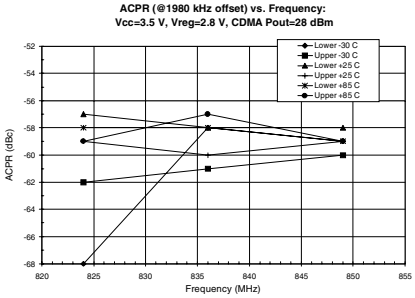


Figure 6: Gain vs. Frequency

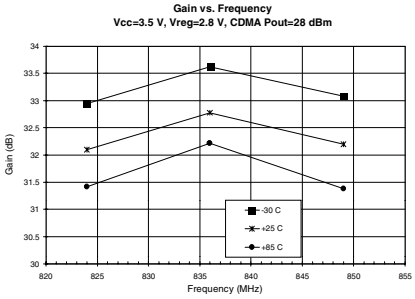


Figure 7: PAE vs. Frequency

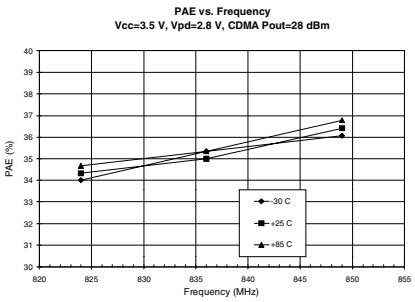


Figure 8: Adjacent Channel Linearity (3.0V)

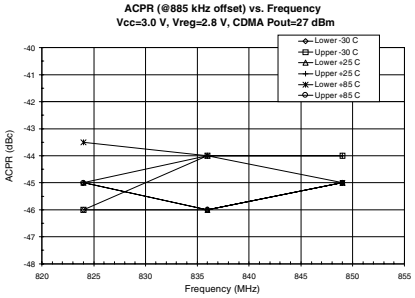


Figure 9: Alternate Channel Linearity (3.0V)

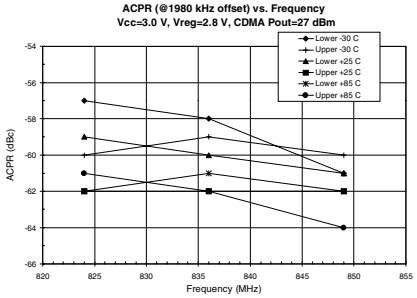


Figure 10: Gain vs. Frequency (3.0V)

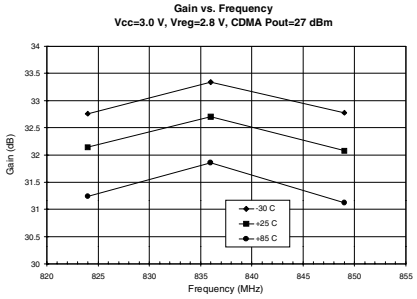


Figure 11: PAE vs. Frequency (3.0V)

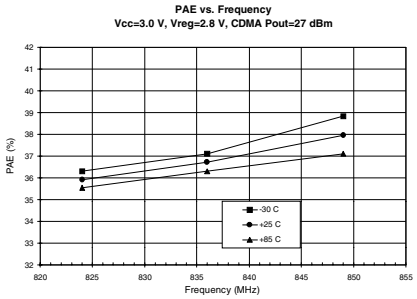


Figure 12: Adjacent Channel Linearity (5.0V)

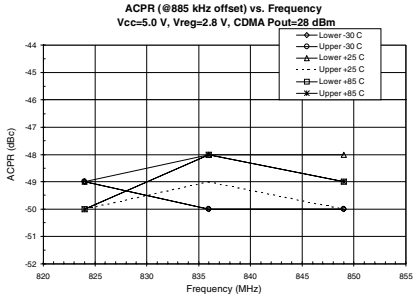


Figure 13: Alternate Channel Linearity (5.0V)

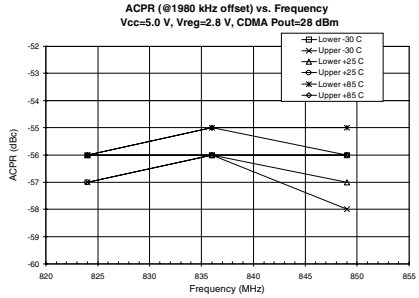


Figure 14: PAE vs. Frequency (5.0V)

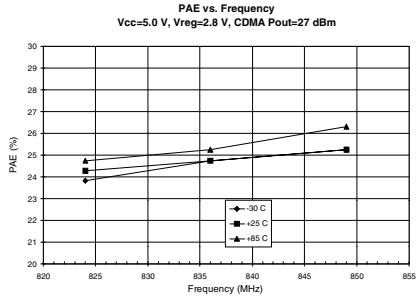


Figure 15: Gain vs. Frequency (5.0V)

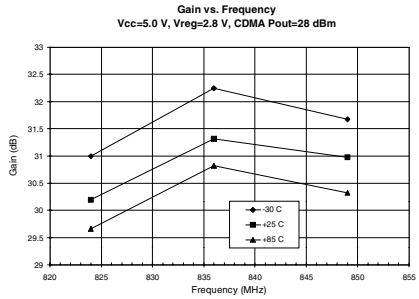


Figure 16: AMPS Mode Performance (3.0V)

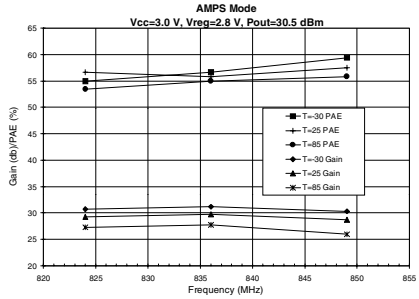


Figure 17: AMPS Mode Performance (3.5V)

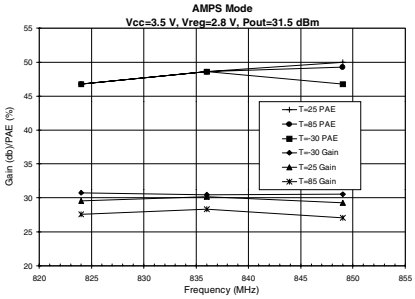
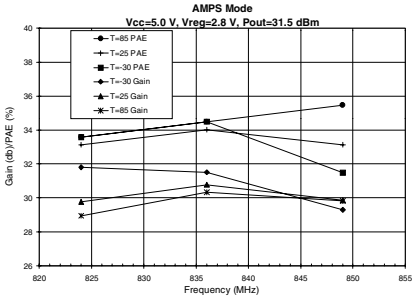


Figure 18: AMPS Mode Performance (5.0V)



Performance with Regulated Supply Voltage

The data below shows the performance of an RF2152 power amplifier tuned for optimal performance at 3.5V.

FREQ	PIN	ICC	ACP1	ACP2	EFF
824	-3.5	469	44/44	58/59	38%
836	-4.4	460	44/44	58/59	39%
849	-4.6	444	44/44	58/59	40%

Low Power Mode

While CDMA power amplifier performance is typically specified at 27dBm to 28dBm output power, the actual average operating output power of a CDMA handset is typically 10dBm to 15dBm. With this in mind, the RF2152 utilizes two external bias control pins to lower the quiescent current approximately 50 percent in low power (less than 15dBm) mode.

Pin 16 (VMODE) directly controls the output bias. Pulling this line TTL low will reduce the bias in the output stage by about 50 percent. Pin 7 is a fine adjustment for both stages. Depending on the output power required in the handset design, this line can be used for further bias reduction in low power mode.

Conclusion

The RF2152 HBT is an integrated power amplifier on the market for IS95 CDMA and dual CDMA/AMPS applications. The amplifier offers the handset designer the opportunity to optimize an amplifier for their particular application with excellent performance. The amplifier is optimized for CDMA performance, with excellent efficiency and low power mode aimed at improving talktime in 3V handsets.

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A Transceiver IC for Cordless Telephones

Introduction

The RF9904 transceiver is a monolithic integrated circuit that was primarily developed for the expanding 900MHz digital cordless telephone market. Manufacturers require a more integrated approach to their design in order to lower manufacturing costs and increase reliability compared to discrete designs. Channel frequency hopping, direct sequence spread spectrum modulation, or a combination of these two, are utilized in cordless telephone technology. The RF9904 can be used in designs using direct sequence spread spectrum modulation. The device is manufactured in a low cost, commercially available silicon bipolar process. The process features NPN transistors with an f_t of 5GHz, PNP transistors with an f_t of 1GHz, thin film resistors, Schottky diodes, and capacitors.

Product Description

A functional block diagram of the RF9904 is shown in Figure 1. The transceiver includes a transmit BPSK modulator and a receive quadrature demodulator. The LO input is split between the transmit and receive section, each section having LO buffer amplifiers. Only a single external LO source is needed, since direct modulation and demodulation at the carrier frequency are used. The RF9904 operates over the 700MHz to 1100MHz frequency range and has a separate RX and TX power control. They are supplied in an SOIC16 package and require a 4V to 6V supply.

Figure 1: RF9904 Functional Block Diagram

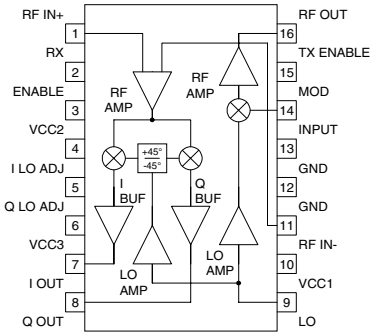


Figure 1. RF9904 Functional Block Diagram

Transmit Section

The transmit section of the RF9904 consists of a LO amplifier/buffer, BPSK modulator and an RF amplifier. The LO input, typically between -6dBm and 0dBm, is split between the transmit and the receive sections. A combination of differential amplifiers and emitter followers provide the gain and buffering required to drive the BPSK modulator. The LO signal is coupled to a set of differential pairs with their collectors cross-coupled. The modulation signal is applied to a lower differential pair and the modulation input can range from 0MHz to 15MHz with up to 0.5V peak-to-peak. The resultant phase of the carrier is shifted 0 degrees or 180 degrees depending on the modulation waveform. The output is a double sideband suppressed carrier signal with typical carrier suppression >25dBc for the maximum input level. The modulation input has an internal 6kΩ resistor to ground and should have a nominal 0V offset. The DC offset sets the carrier suppression and can be between +1V and -1V.

A final stage of RF amplification follows the modulator and has an open collector output. This pin requires an external inductor to V_{CC} for biasing. The inductor can be incorporated into an output-matching network. The maximum output from the chip is -7dBm to -12dBm and in the transmit mode the part draws 12mA.

Receive Section

This section describes the quadrature demodulation function in the receive section. The LO input is first amplified, and then in order to achieve quadrature demodulation, the LO signals to each mixer must be in phase quadrature. A simple, yet accurate method of phase shifting on-chip is to use an R-C network. The network combines a low- and high-pass filter. Each of the networks provides a 45 degree phase shift to the LO signal but in opposite directions, hence the required 90 degrees is obtained. The accuracy of the 90 degree phasing is more dependent on the matching of the R and C rather than their absolute tolerance, while the amplitude balance is exact at only one frequency. Differential amplifier limiters are placed between the phase shifters and mixer LO ports so that the quadrature signals are amplified until they are clipping, removing an amplitude imbalance in the LO drive to the mixers.

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The quadrature LO signals are coupled to the top transistors in a modified Gilbert Cell configuration used for the I and Q mixers. The RF input signal is amplified by differential amplifiers, which form the lower part of the modified I and Q mixers. The RF input is single-ended and requires an external DC blocking capacitor.

The I and Q outputs are amplified by differential amplifiers which drive a push-pull output configuration to provide a 50Ω single-ended output. The amplitude error is <0.5dB and the phase error is <1 degree at the nominal operating point of V_{CC} = 5V and an LO input level of -3dBm. There are two external resistors to ground that can be used to adjust the bias on the I and Q LO amplifiers. Typical values for these resistors are between 0Ω and 200Ω. These can be used to adjust the amplitude balance and phase error for non-optimum values of V_{CC} and LO input level. Figures 2 and 3 show amplitude and phase error versus LO input level. These results were taken on an evaluation board that had been optimized for amplitude error across a range of different LO input levels. The same board could have been optimized for phase error with a resulting degradation in the amplitude error. The noise figure is between 10dB and 15dB depending on the RF input network. This means that some form of front-end low noise amplification is required. The current consumption in the receive mode is typically 27mA at 5V.

Figure 2: RF9904 Amplitude Error versus LO Input Level

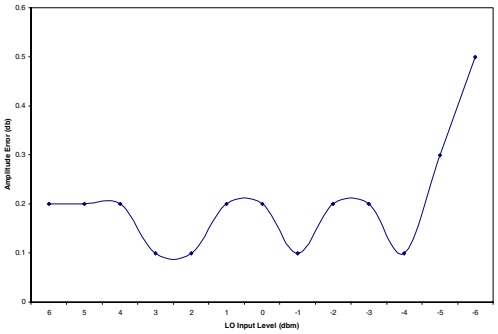
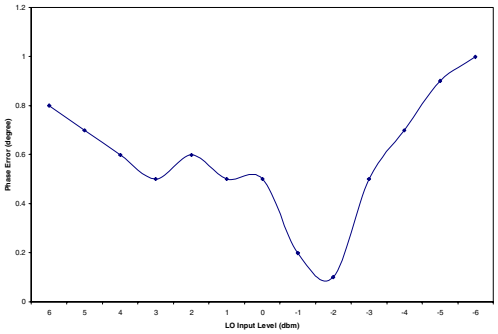


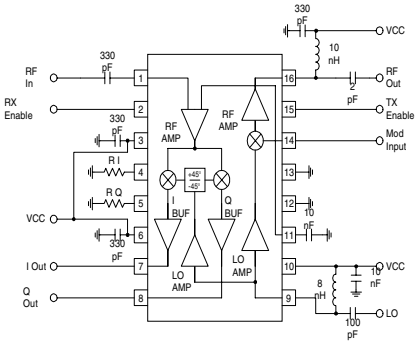
Figure 3: RF9904 Phase Error versus LO Input Level



Application Circuit

The circuit shown in Figure 4 was used to demonstrate typical performance of the RF9904. The RF and LO inputs are DC blocked while a DC block should be used on the modulation input if a DC level of 0V is required and also on the I and Q outputs since a DC level is present there. A pull-up inductor to V_{CC} is required on the RF output and all V_{CC} inputs should be bypassed as close as possible to the device. The switching between the transmit and receive mode is achieved by TX enable or RX enable being set high, typically to V_{CC}.

Figure 4: RF9904 916MHz Application Schematic



Conclusion

The RF9904's easily implemented transmit and receive capabilities make it suitable for many direct sequence spread spectrum applications. It has been used along with a front end IC in high volume cordless telephone manufacturing, helping to reduce system costs and increasing reliability without affecting performance.

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Low Cost, Low Voltage Power Amplifier for ISM Applications

Abstract

RF Micro Devices introduces a new low cost, low voltage power amplifier manufactured in an advanced Silicon bipolar technology. The power amplifier operates from 400MHz up to 1GHz and delivers 0.5W at 3.6V with a gain of 21dB. The analog gain control provides 40dB of range. This power amplifier is intended for cost-sensitive applications, such as the final output stage for a 900MHz ISM band cordless phone or as a driver for 400MHz mobile phones. The device operates from a single 3.6V power supply without the need for a negative voltage. The on-board gain control also doubles as Power Down control, and the device draws less than 10µA of supply current when in the power down mode, eliminating the need for a supply side switch. The part is packaged in a thermally enhanced, industry standard 16-lead SOIC with fused leads. Pricing is very competitive at less than $2.

Introduction

Cordless phone manufacturers are under constant pressure to reduce the cost of handsets, and at the same time to improve performance. Phone designs which operate with a low voltage (thus a smaller and lighter battery) and use highly integrated electronics (thus smaller and cheaper) are the most likely to succeed in this market. Spread spectrum handsets operating in the 915MHz ISM band offer a clear advantage over their VHF predecessors. The users of spread spectrum handsets are less likely to experience line interference compared with the 45MHz handsets. Electronic noise from appliances, computers and other electronic devices, along with typically poor range, are characteristic of the old 45MHz cordless phones. These problems do not exist in the 900MHz spread spectrum phones due to the digital modulation. The FCC rules Part 15 allow up to 1W of transmitted power in this band. However, battery life and talk time are reduced as the output power is increased. Cordless phone manufacturers have generally kept their output power levels around 250mW in order to get the best trade-off of talk time versus handset range. Allowing 3dB for loss for filtering and an RX/TX switch between the PA and the antenna, the output power required from the PA is 500mW. Some cordless phones also implement a power control function to maximize talk time.

Ideally suited for this 900MHz application is the RF2104, a new power amplifier from RF Micro Devices. This integrated PA is also well suited for lower frequency applications, such as a driver amplifier for 400MHz mobile phones and base stations. This Low Voltage PA amplifies a +6dBm input signal to +27dBm of output power, drawing about 350mA of current from a single 3.6V supply. With the proper output matching circuit, similar performance can be achieved at voltages as low as 2.7V. Higher power levels of up to 1W are also possible, but with less ruggedness into output load mismatches. When the power control pin is reduced to 0.5V, the PA draws less than 10µA of supply current when the input RF power is removed, eliminating the need for a supply side switch. The RF2104 is packaged in a thermally enhanced version of the standard 16-lead SOIC with fused leads. When compared to and implemented with discrete components, the RF2104 greatly reduces the component count, overall size, performance variations, and most importantly, the overall cost.

RF2104 Theory of Operation and Application Information

The block diagram for the RF2104 is shown in Figure 1. The IC is a two-stage power amplifier with

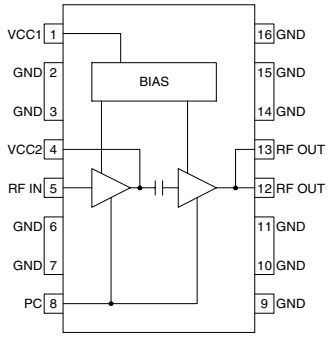


Figure 1. Block Diagram and Pinout for RF2104

26dB of small-signal gain that operates between 2.7V and 6.0V. With an input drive level of +6dBm, the PA delivers over +27dBm with an efficiency of about 40 percent from a 3.6V supply. A power down feature is implemented with a single pin interface (Pin 8); when this pin is at less than 0.5V, the PA draws less than 10µA provided the input RF power is turned off (when the RF input is still at +6dBm the device draws about

4mA due to self-biasing of the input stage). When the voltage on the power control pin is increased to a nominal value of 2.5V, the PA is set for maximum output power. This pin draws about 1mA of current when set to 2.5V. Pin 1 is connected to the battery voltage and is used to supply base current to the RF transistors.

The ground for the device is achieved through the four large pins on both sides of the device. These pins should be connected directly with vias to the PCB ground plane. The RF output is brought through Pins 12 and 13, which are used for the output signal, as well as to feed the bias current to the final stage.

The amplifier operates in Class AB mode. When the power control is set for maximum output power, the idle current is 250mA. When an RF signal is applied to the input, the output stage self-biases, and draws about 350mA of DC current.

Interstage Matching

Pin 4 is the supply voltage for the first stage. The inductance between this pin and the bypass capacitor sets the frequency of the small-signal gain peak. A short PCB trace between the pin and bypass capacitor, together with the internal bondwire inductance, conveniently realizes this inductance. Moving this capacitor away from the device shifts the gain peak to a lower frequency.

Input Matching

The input of the RF2104 is internally matched to 50Ω. The input is DC coupled and requires a blocking capacitor. A series capacitor and shunt inductor can be added to the input to improve the VSWR. Without external matching, the return loss of the input is about -10dB.

Output Matching

The optimum load impedance to the device is 5Ω. With this impedance, power levels over 1W can be achieved. However, if the device has to operate into high mismatches at the output, which is generally the case in hand-held equipment, it is recommended to reduce the maximum output power and increase the load impedance. The output pins also provide the bias for the output stage. A stripline or inductor to the V_{CC} is required. Because the impedance at the output is low, a small inductor or short stripline can be chosen. It is not necessary to use a quarter wave stripline; a line or inductor that provides an impedance of more than 50Ω is sufficient. Details of the implementation of those matching circuits can be seen in Figure 2. Note that several of the bypass capacitors are only required on the test board connected with long wires to the test equipment. In a practical phone design, capacitors (C2, C4, C6, C8) can be eliminated.

RF2104 Performance

A full data sheet can be obtained from RF Micro Devices.

The performance of the RF2104 has been characterized using a low-cost, 30mil FR-4 printed circuit board. Evaluation boards for 915MHz and 830MHz are available. The application schematic and layout drawing for the PA for 915MHz operation are included in Figures 2 and 3.

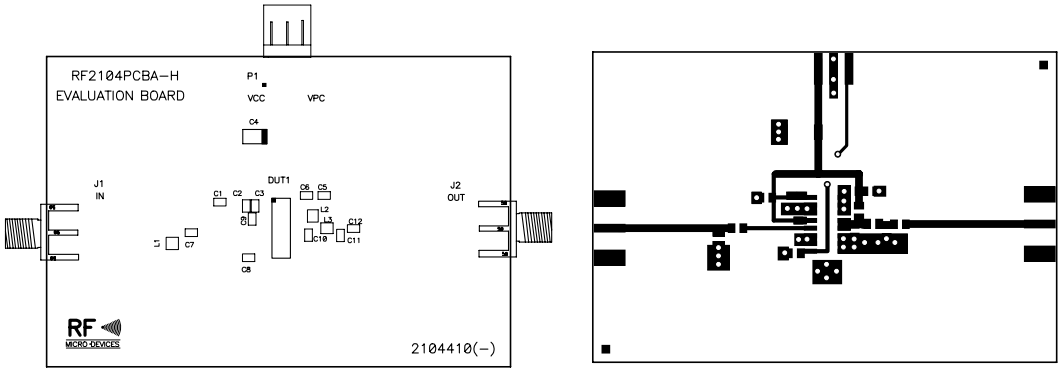
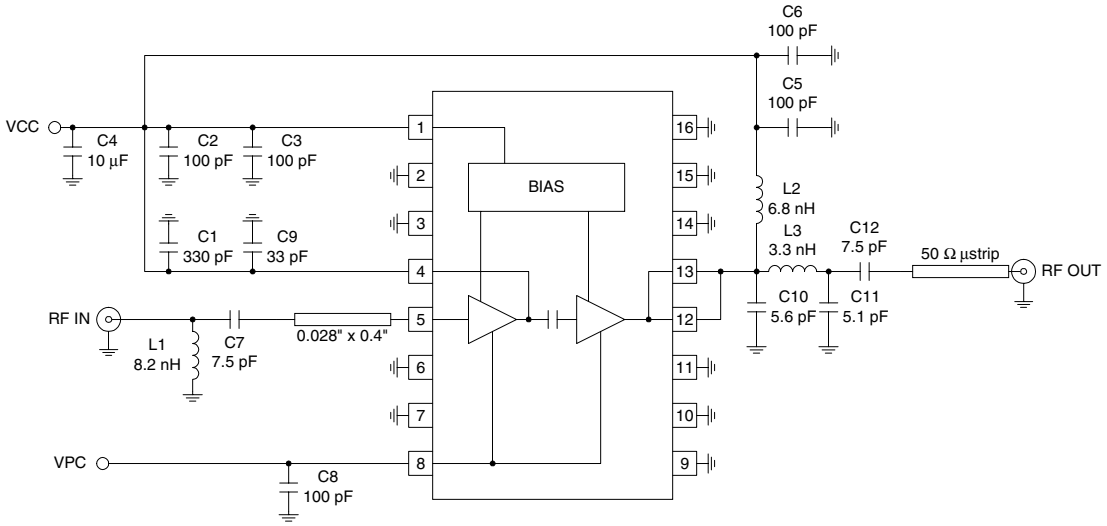


Figure 3. Test board layout for the RF2104 for 915MHz operation



Note: Efficiency is affected by actual position of C9 and C10; C9 is mounted close to DUT and C10 mounted away from DUT.

Figure 2. 915MHz test circuit of the RF2104

Some typical performance curves are shown in Figures 4 and 5.

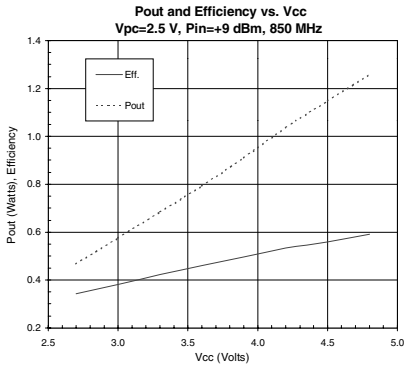


Figure 4. Typical performance of the RF2104

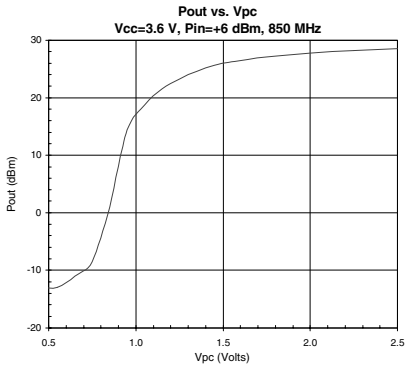


Figure 5. Typical performance of the RF2104

Conclusion

The RF2104 Power Amplifier is introduced by RF Micro Devices. With a +6dBm input level, this IC amplifier delivers 0.5W operating from a single supply from 2.7V to 5.5V. Additionally, the PA offers a convenient analog power control function. The RF2104 has applications in any analog or digital communication system that requires a low-voltage, low-cost PA. Specifically, this IC was designed for 900MHz cordless phones and 400MHz industrial radios, where the device will simplify the transmitter design, reduce overall component count, and reduce cost. Using discrete matching components, the size required for this PA is less than 0.4 square inches. The price of the RF2104 is less than $2.

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A Dynamic Current Control Scheme for RF Power Amplifiers

Abstract

A commonly applied technique to improve linearity of an RF power amplifier is to increase the quiescent current so that the transistor operates in a more linear portion of the I/V curve. This method unfortunately requires the amplifier to run at high idle current all the time even if the input is not large enough to demand the linearity. A dynamic current control scheme is demonstrated here to automatically adjust bias current on a need basis to meet linearity requirements.

Introduction

State-of-the-art RF systems demand higher linearity power amplifiers to minimize adjacent and alternate channel distortion. Portable systems have an additional challenge in meeting the tough requirements with high efficiency. It thus behooves RF designers to create new schemes to optimize efficiency and obtain the required linearity. This paper demonstrates a feed-forward circuit which senses the input power level of the signal and dynamically adjusts the bias current of the amplifier. It is shown using Spice simulations that, at low input power levels, obtain an improvement of about 50 percent in DC power consumption, while allowing about 6dB increased linear output power.

Design Requirements

There has been a general trend in the RF IC industry to optimize process technology for a particular application. RF Micro Devices uses Optimum Technology Matching™, where we apply high performance GaAs HBT and MESFET technology to Power Amplifier (PA) designs and front ends, and lower cost BiCMOS technology to RF/IF ASIC design. This partitioning allows optimum price/performance trade-off. It is easier to design temperature, power supply and process insensitive circuits in BiCMOS technology than in GaAs MESFET or HBT technology. Control and logic functions can also be easily accommodated by BiCMOS circuits at lower cost and higher performance. Thus, implementing multi-technology IC's in one chipset will improve performance, provide additional features and lower cost.

The scheme described here uses a BiCMOS control circuit to improve linearity and efficiency by dynamically controlling the amplifier bias.

Method

As shown in Figure 1, the system described here consists of a two stage, 20dB gain PA driver (operating between 1800MHz to 1900MHz) and a support chip supplying bias reference currents. Figure 2 shows the bias control circuit. For simplicity, the bias circuit shown here focuses on controlling bias with respect to the input signal with other functions stripped off.

Figure 1. Top Level Schematic

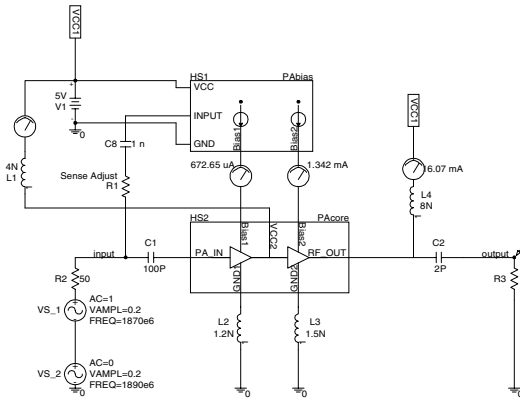
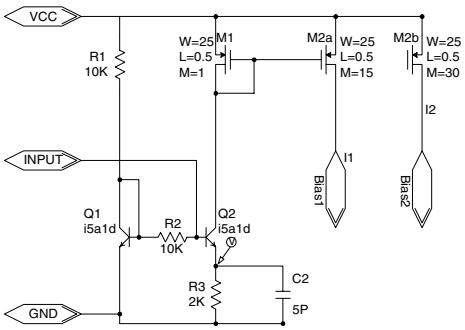


Figure 2. PaBias-Block Simplified Schematic

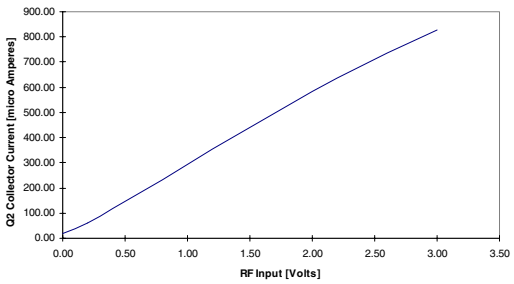


The circuit in Figure 2 senses the strength of the input signal and converts it to DC current which is then mirrored over by the PMOS transistors. Q1, Q2, R1, and R3 set up the minimum DC bias conditions when the input signal is small. In this mode, the current in Q2 is small and is used to bias the amplifier, creating a more efficient system when the input signal is small. As the input signal gets larger, Q2 amplifies and rectifies the

signal, and the components C2 and R3 filter the rectified signal. We are left with a DC current that is used to set the bias current in the PA driver. The larger the input signal, the larger the bias current (see Figure 3), allowing the amplifier to linearly amplify larger signals than before. R3 and C2 also set the time constant of the system. In the top level schematic, the input consists of a sense resistor (R1) and a DC blocking capacitor (C8). R1 is used to adjust the transconductance of the dynamic bias system.

Figure 3 shows the transfer function of the bias block. As the RF input peak voltage (at 1880MHz) is swept from 0V to 3V, the output DC current I Q2 collector changes from 18µA to 828µA. This current effectively sets the operating regions of the PA transistors. The second stage requires twice the first stage current to operate, and the two output PMOS transistors are sized accordingly. The bias control can be easily removed from the circuit by grounding the sense resistor (R1), or making it very large.

Figure 3. PABias Schematic's Q2 Collector Current versus RF Input at 1800MHz



Results and Discussions

Figure 4 shows the Spice simulation depicting the gain compression characteristic of the PA driver versus the input power for the system. The figure shows the linear operating range of the PA driver, controlled by the automatic bias control, extended about 6dB as compared to constant bias case.

Figure 4. Gain Compression of the PA Driver

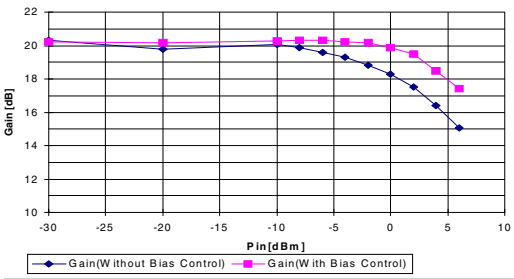
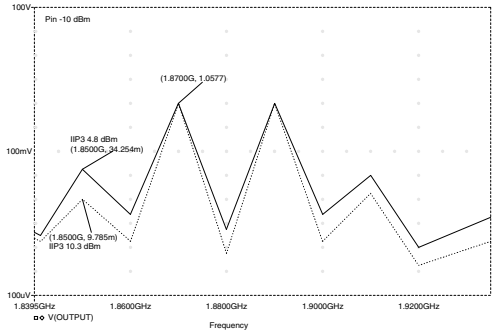


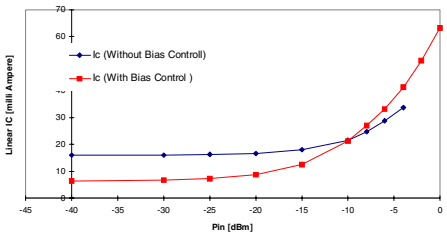
Figure 5 shows the Input IP3 Plot for the two cases. The Input IP3 is about 5.5dB higher with the automatic bias control activated.

Figure 5. Two-Tone Input IP3 of the PA Driver With and Without Automatic Bias Control



Finally, Figure 6 shows the efficiency (in terms of linear output collector currents) of the system operating with and without bias control. In order to demonstrate this over a wide dynamic range, the external sense resistor (R1) of the top level schematic, and R1 of the PABias schematic, were increased to 3kΩ and 100KΩ, respectively. It can be seen that under small signal conditions, the quiescent currents are much lower for the circuit with automatic bias control. At the same time, the automatic bias control extends the linear operating range under large signal conditions. Thus, efficiency is dynamically adjusted as the PA driver input power varies.

Figure 6. Linear Final Stage RMS Collector Currents for the Two Cases as the Input Signal is Varied



Conclusions

A new dynamic bias technique for use with RF Power Amps is presented. This circuit adjusts the bias current in the PA depending on the input power level sensed. At low input power levels, about half the DC current is used, thereby doubling the amplifier efficiency. At higher input power levels, the bias current is increased, allowing about 6dB more output power before linearity is compromised.

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Low Cost Family of 3V Silicon Gain Blocks

Abstract

RF Micro Devices introduces a family of low cost silicon gain blocks designed for 3V supply operation. Part numbers RF2321, RF2322, RF2323, RF2325, and RF2326, comprise the family. The parts are packaged in SOT23-5 lead packages and are available on evaluation boards from RF Micro Devices. Applications include broadband gain stages, final PA for ISM band applications, driver amps, oscillator loop amplifiers, and buffer amplifiers.

Introduction

Two different circuit topologies are used in the 3V gain block family. The first is a dual common emitter (CE-CE) topology (RF2321/2322/2323), and the second is a Darlington topology (RF2325/2326). Figure 1 shows the amplifier schematics, and Figure 2 shows the applications schematics for the two topologies. In both designs, series and shunt feedback are used to simultaneously set the gain and the impedance match.

Figure 1: Amplifier Schematics

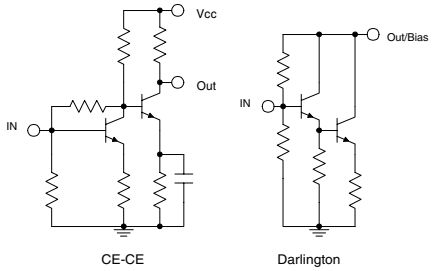
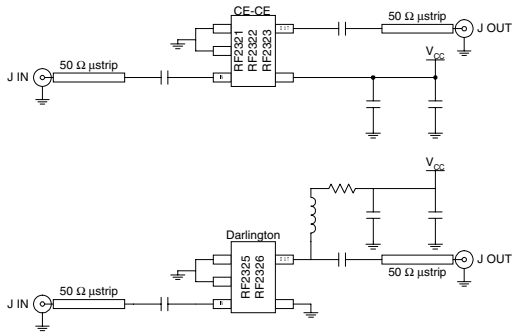
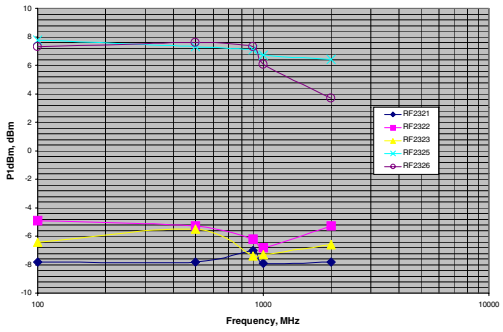


Figure 2: Applications Schematics



The use of the two circuit topologies results in varied circuit performance. The CE-CE designs require no external bias components and have lower noise figures; however, they are limited in output power to approximately -5dBm to -8dBm P1dBm (see Figure 3). They are biased at approximately 7mA. The Darlington designs require external bias components and have higher noise figures, but have a P1dBm of 6dBm to 7dBm. They are biased at approximately 25mA.

Figure 3: Output Power (P1dBm)



Design Descriptions

The CE-CE amplifiers have two stages of gain to cascade for the overall gain. Putting more gain in the first stage as well as optimizing the input transistor allows the lower noise figures to be achieved. The collector resistor in the second stage sets the output impedance as well as affecting the gain of the second stage. The fixed resistor between the collector and supply causes the amplifier to compress at lower input levels than the Darlington due to limiting on the positive half cycle of the output. In the Darlington topology, the limiting occurs on the negative half cycle when the collector base junction voltage of the second transistor approaches zero. The Darlington's first stage is essentially an emitter follower with unity voltage gain which tracks the input. In the Darlington there is no intermediate stage of amplification whose voltage swing must be accommodated to remain linear. This results in larger available output swings.

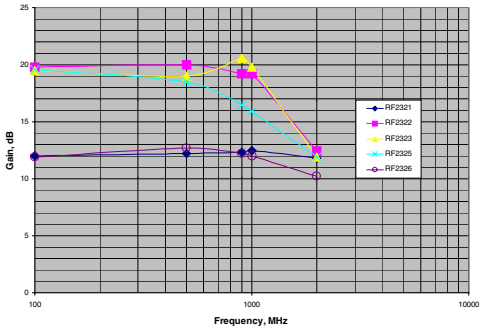
The evaluation board for the CE-CE designs requires only bypass and blocking capacitors. The values should be optimized for the desired frequency of oper-

ation. Typically a low and a high frequency bypass capacitor will be chosen to ensure that a broad range of noise will be filtered. All test data was taken using 100pF blocking and a 1nF bypass capacitor.

The Darlington amplifiers required the same capacitors as the dual CE designs, as well as some bias components. A series resistor and choke are used to bias the Darlington topology. The resistor is used to establish a bias current into the amplifier. It also serves to stabilize the current over temperature through negative feedback. The choke is chosen to have an impedance of at least 10Zo or 500Ω to prevent the network from loading the output.

The CE-CE designs incorporate capacitive compensation in the emitter circuit of the second stage. This boosts the gain at high frequencies, thus extending the bandwidth of the device. The value is chosen to extend the bandwidth as much as possible while avoiding excessive gain peaking at the 3dB point. Figure 4 shows a plot of the gain of the five parts in the family.

Figure 4: Gain Figures

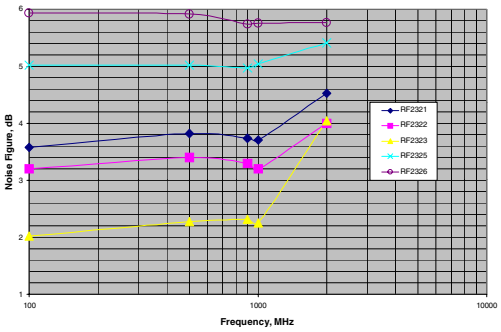


Performance Data

The RF2321 and RF2326 have a nominal gain of 12dB. The nominal gain of the RF2322, RF2323 and RF2325 is 19dBm to 20dBm. As can be seen, all parts have 10dB or more usable gain at 2GHz.

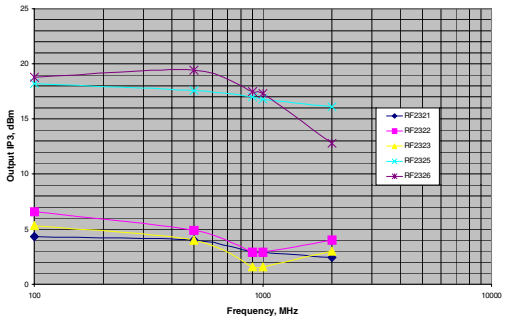
Figure 5 shows the noise figures for the five parts. The RF2323 has a noise figure of 2.3dB at 900MHz making it suitable for some LNA applications.

Figure 5: Noise Figures



IP3 values are shown in Figure 6. Note that these values are 10dBm to 12dBm above the P1dBm in Figure 3. The Darlington amplifiers have an IP3 of 17dBm at 900MHz.

Figure 6: IP3 Values



Input and output return loss is shown in Figures 7 and 8. The input match of the RF2323 is worse than the other parts due to its very high first stage gain. This gave it the low noise figure discussed earlier. Note that all the data shown is from evaluation boards assembled as in Figure 2. No reactive tuning elements were used to match the devices. The output match of the RF2321, RF2322 and RF2323 is set by the output collector resistor, whereas the output match of the RF2325 and RF2326 is set by series and shunt feedback closer to 50Ω.

Figure 7: Input Return Loss

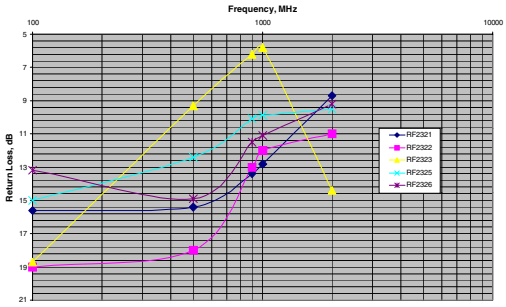


Figure 8: Output Return Loss

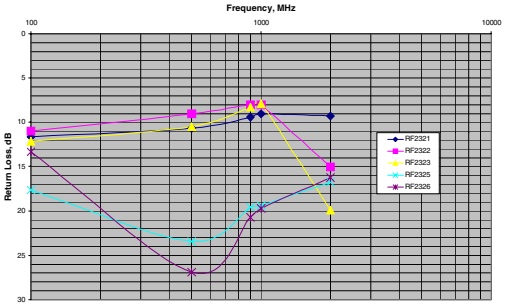
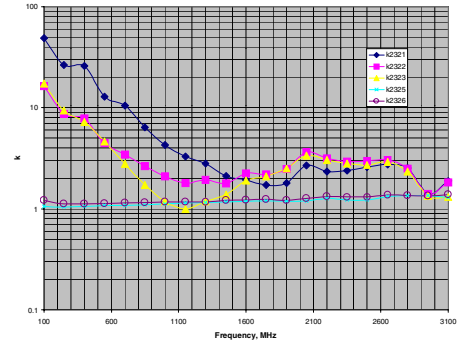


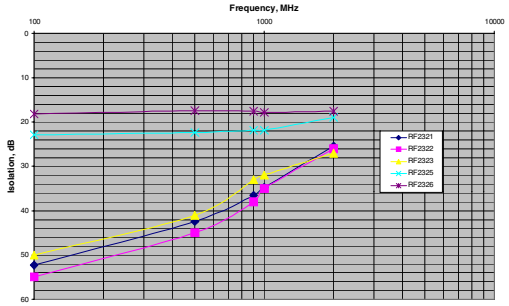
Figure 9 shows calculated values of k, indicating unconditional stability for all five parts. The parasitics of the package contribute heavily to the stability of the amplifier, particularly in the ground circuit(s) of the amplifiers. Unintentional feedback between stages can lead to degraded input match and potential instability.

Figure 9: Stability Analysis



The final parameter to be measured was reverse isolation. Figure 10 compares the five parts. As can be seen, the dual CE topology offers superior isolation due to its dual stage design, however the Darlington configuration results in at least 17dB of broadband isolation.

Figure 10: Isolation



The 3V Silicon Gain block family has been characterized from 2.7V to 3.3V supply and over a temperature range of -40°C to +85°C. The parts are rated at 4V maximum supply voltage.

Conclusion

RF Micro Devices has introduced a family of 3V Silicon Gain Blocks. They are packaged in an industry standard SOT23-5 lead package for low cost and small size. The five parts range in gain from 12dB to 19dB and are designed to be unconditionally stable. Potential applications include broadband gain stages, final PA for ISM band applications, driver amps, oscillator loop amplifiers, and buffer amplifiers. The use of resistive feedback for gain setting and impedance matching results in very compact and broadband designs. This also translates to very low cost and manufacturable designs, eliminating costly tuning associated with narrowband and/or discrete designs.

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The Role of Silicon Germanium in Optimum Technology Matching®

Introduction

RF Micro Devices (RFMD) has added Silicon Germanium (SiGe) to the list of technologies used in its RFIC designs. While much has been written concerning the future of SiGe technology, and its impending takeover of the RFIC industry, the importance of other process technologies cannot be immediately dismissed. As new technologies become available, they must be continually evaluated against the changing demands of new applications, particularly in the areas of price and performance. With SiGe components just becoming available, this process is beginning in earnest. All technologies have their advantages and disadvantages and none are perfect for every application. RFMD uses its exclusive methodology, Optimum Technology Matching® (OTM), to determine which of the available process technologies will maximize performance and minimize cost. This paper will examine the process of OTM, and discuss the role of SiGe within that framework.

Optimum Technology Matching®

Whether designing a custom or standard RFIC, the designer is faced with many choices including: the package; the circuit topology; and, the process technology. RFMD uses it's OTM methodology to determine which of four cutting-edge process technologies will maximize performance and minimize cost. This decision is made on a case-by-case basis, and is enhanced by a large experience base coupled with an in-depth knowledge of the application and the limits of technology. Currently, the available choices include: Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT); Gallium Arsenide Metal Semiconductor Field Effect Transistor (GaAs MESFET); Silicon Bipolar Complementary Metal Oxide Semiconductor (Si BiCMOS) and Silicon Bipolar Junction Transmitter (Si BJT); and, SiGe. The relative strengths and weaknesses of each technology determine the applications where each technology will be best utilized. New technologies having demonstrable advantages will be added to this list as they become available. The following sections present these technologies in more detail and discuss typical applications for each.

GaAs HBT

GaAs HBT technology has found wide acceptance in the marketplace, particularly for handset applications. This acceptance is based on the technology characteristics of high linearity and efficiencies, low phase noise, thermal ruggedness, and low cost. HBTs have a breakdown voltage greater than 20V, which eliminates possible problems with overvoltage, making them ideal for battery-operated applications. Their bipolar structure allows these devices to operate from a single positive supply. This means, that unlike MESFET technology, HBTs do not require a charge pump that either adds current to the IC or cost to the application. HBTs also have an advantage in power control circuitry. The HBT can be completely powered down using a control voltage, eliminating the need for a drain supply switch used in MESFET designs. The MESFET approach requires an additional component and adversely impacts system efficiency. An example of an HBT design for use as a power amplifier is the RF2152, which was developed for 3V handheld systems. This device may be used as the final RF amplifier in dual-mode 3V CDMA/FM handheld digital cellular equipment and other applications in the 800MHz to 900MHz band. The RF2152 delivers 28dBm linear output power and 30dB linear gain, while operating at 35 percent linear efficiency. Power amplifiers are not the only uses for HBT technology. Recently, RFMD announced a series of extremely small low-noise PA driver amplifiers using HBT technology. Included is the RF2324, which features low noise, a high intercept point, and operates over the 150MHz to 2500MHz range. This device is packaged in an 8-lead plastic MSOP package and is priced at $1.53 per unit (in quantities exceeding 10,000 units). Similarly, RFMD has also announced a line of HBT process technology general-purpose broadband amplifiers that provides the power required in many wireless applications at a low cost and in a small package. These devices sell for as low as $0.90 per unit (in quantities of 1,000 or more), while providing +34dBm output IP3 at 1GHz, and operate up to 6GHz (RF2333). The combination of high power capability, high efficiency, and low cost make the GaAs HBT an optimal choice for many handheld wireless applications.

GaAs MESFET

GaAs MESFET technology is widely used in high frequency applications. In addition to their high frequency capability, GaAs MESFETs combine low noise characteristics with excellent switching capabilities. These characteristics make the devices suitable for a variety of high-performance small-signal and moderate power amplifier applications, as well as for control applications. RFMD has developed a variety of components exploiting these characteristics. For example, the RF2320 is a general purpose, low-cost, high-linearity amplifier. This power amplifier (+22dBm output power) has a low noise figure (1.6dB) and operates over a large bandwidth (5MHz to 2500MHz) making it an ideal choice for cable TV applications. Other examples include the RF2420 programmable attenuator. This device is a typical example of the control applications for GaAs MESFET technology and exploits the switching characteristics of the devices for digital control components. The RF2420, for example, provides 5 bits of digitally-controlled attenuation over the DC to 950MHz frequency range. Although GaAs HBT technology has won many of the power amplifier slots from the GaAs MESFET, the MESFET remains a useful device for some applications.

Si BiCMOS and Si BJT

Si BiCMOS and Si BJT are widely used process technologies for RFICs. There are several compelling reasons to consider using silicon process technologies when designing a new RFIC. Perhaps the most compelling reason is cost. Because of the large wafer size (8 inches) and the large volume of devices using this technology, these are the most cost effective (per square mm) technologies in common use for RFICs. In addition to the low cost, the available bipolar devices are capable of high frequency operation and the process is able to integrate complex digital circuits using CMOS devices (Si BiCMOS). This combination of analog performance, digital capability, and low cost is powerful. RFMD has developed a large variety of components using these technologies including amplifiers, mixers, modulators and demodulators, front-ends, and highly integrated transceivers. This technology is effective for single functional blocks such as mixers (RF2456), as well as for complex, highly integrated components such as transceivers (RF2905). The RF2456 is a receiver dual downconverter designed for the receive section of dual-mode CDMA/FM cellular applications. The RF2905 is a monolithic integrated circuit intended for use as a low cost transceiver in linear (AM, FM) or digital (ASK, FSK, OOK) applications in the North American (915MHz) and European (433MHz and 868MHz) ISM bands. The CMOS capabilities are exploited by the RF2908, 915MHz spread spectrum receiver with PLL frequency synthesizer. This device couples a direct conversion receiver with a complete on-chip 86-channel frequency synthesizer and on-chip selectable IF bandwidths. The range of applications for these technologies is broad and growing rapidly.

SiGe

SiGe technology is only beginning to be commercially exploited. This technology is highly anticipated because of its promise of high linearity, low noise, and low power consumption, along with the ability for high levels of integration. RFMD is currently designing RFICs using SiGe and plans to use SiGe for a broad range of custom and standard RFICs.

Conclusion

Just as there is a broad spectrum of RFIC applications, there are a variety of process technologies that can be utilized. No single process technology can be optimized for every application. RFMD has developed a unique methodology of Optimum Technology Matching® (OTM) for choosing the best technology to optimize performance and minimize cost for a given application. The emergence of SiGe, or any other new technology, does not obviate the need for this approach, but makes this methodology even more important. Just as GaAs HBT has found wide acceptance as a key technology for power amplification in handheld devices, GaAs MESFET has found acceptance as a key technology for high performance small signal and control applications, and Si BiCMOS and Si BJT have found acceptance as key technologies for lower power/performance/cost applications, SiGe will find acceptance as a key technology for some applications. RFMD will aggressively pursue this and other new technologies in order to further position ourselves as a “one-stop” solution for our customers’ RFIC needs. RFMD’s silicon products are the fastest growing segment of our business and we expect that the addition of SiGe technology will enable us to accelerate the growth of our silicon product portfolio.

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DC Accurate FSK Modulator

A typical, low cost, FSK modulator is implemented by injecting the modulation voltage into the phase lock loop of the carrier synthesizer. This is done in two ways, by summing the modulation voltage and the loop error voltage together and applying that to a VCO tuning port. Or, by using a separate tuning port usually having lower sensitivity to voltage changes. The modulating data would change the carrier frequency by a predetermined amount (deviation). This, however, causes a frequency error within the PLL that the loop begins to correct for. The effect of the loop correcting for the frequency errors caused by the modulation is analogous to passing the modulating signal through a high pass filter. Lower frequency components of the modulation signal get filtered off (or even eliminated). This results in unreliable communications for random data streams, especially for long strings of non-changing bits.

There have been several solutions developed and implemented that address this problem. One approach is to predistort the modulation signal to compensate for the effects of the PLL. This has limited results and a finite frequency range. Another commonly used method is to encode the data stream with such techniques as Manchester coding or split phase coding. The basis of this coding is to send two complementary symbols for every data bit, thus a transition is guaranteed for every data bit. This is very effective in that it fixes the lowest frequency component of the modulation signal so that a loop bandwidth can be designed to have a minimal effect on the coded data. Unfortunately, this means that the effective data rate of the radio is doubled, increasing channel bandwidth. The encoding procedure is rather simple (exclusive OR the data and clock together). The decoding is much more complicated requiring some synchronization to guarantee the correct two symbols are used to decode the data bit.

Other approaches avoid the problem altogether by modulating outside of the PLL loop. Modulating the reference crystal, for example, can do this. A varactor can be used with a crystal to pull the center frequency to the mark and space frequencies. Since the modulation occurs outside the loop, the PLL does not effect the modulation signal, it simply tracks the changes in the reference frequency. The pullability of the crystal will limit the achievable frequency deviation and thus the maximum data rate using this method. Given the variances in crystals and varactors, this would require tuning to set the desired deviation. Another method would be to generate the reference frequency with a Direct Digital Synthesizer and modulate within this synthesizer. This works very well and accurately but cost is considerably higher.

Another type of approach is to program the mark and space frequencies in the PLL. There are several ways to do this depending on the programmability of the PLL divider registers. A new technique takes advantage of low cost ICs that contain an integrated, simple PLL and the VCO functions. These devices are typically designed to be multipliers of a reference crystal to generate a local oscillator frequency or they can be modulated for FSK transmitters. One component of the PLL is the prescaler. This divides the VCO frequency down to the reference crystal frequency. The prescaler usually has 2 divide-by rates (N and N+1) and is referred to as dual modulus. By controlling the ratio of the 2 rates, the VCO frequency can be set to a desired frequency. Using one ratio for logic 1 and another ratio for logic 0 can effectively generate FSK modulation that is not affected by the PLL and therefore can be used for signals that contain near DC components.

One way to generate this ratio is to use a pulse width modulator. This is similar to how a typical PLL would work. The prescaler would divide by N for part of a cycle and then divide by N+1 for the remainder. This would synthesize a frequency that is N+(duty cycle) times the reference frequency. The step size between two frequencies is set by the resolution of the counter used to set the duty cycle. Another way to generate a ratio is to start with a clock pattern and periodically inject an extra bit. The ratio is then tied to the period of the injected bit. By changing the period of the injected bit, a new ratio is formed and thus a new synthesized frequency.

An example of this approach is as follows using a 4-bit programmable counter. By loading one set of bits into the counter with the carry-out, the counter can be programmed to divide the clock by s, (Fclk/s), resulting in a cycle rate of s/Fclk second. The first divider output, Qa, normally looks like Fclk divided by 2. If the programmed value s is chosen such that a “1” is loaded into the “a” divider (an odd number), then the Qa output stays a “1” from the previous state. This puts one more “1” in the Qa output than “0” for every cycle of the counter. This unequal number of 1s and 0s will define a

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fractional number over the cycle rate of the programmed bits. Different programmed bits can generate different fractional numbers and thus different synthesized frequencies. If b is the number of bits in the counter and s is the programmed word, then the fractional number generated is:

# of Qa states per cycle = 2^b-s

# of 0s per cycle = 2^b-s-1

Then fractional n = 2^b-s-1

The synthesized frequency can then be calculated as $F(ref)*(N+n)$. If s and $n(s)$ represent the space frequency and m and n(m) represent the mark frequency, then the peak to peak frequency deviation can be calculated as $F(ref)*(n(s)-n(m))$. This method can produce smaller deviations with fewer dividers than the previous method but offers fewer selections from which to chose.

A simple form of this technique is described in Figure 1. It is implemented with a 4-bit counter and the values of s and m are chosen such that only 1 of the 4 bits is different. Therefore, the data to be modulated onto the carrier is used to set or clear that divider every cycle. An infinite numbers of cycles can occur at either the mark of space frequency without correction by the PLL therefore making this modulator accurate down to DC.

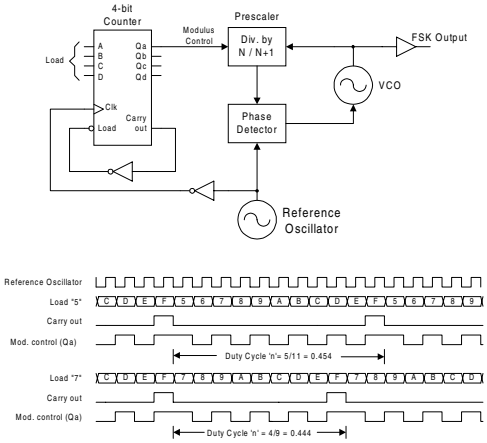


Figure 1. DC Accurate FSK Modulator

In the example of Figure 1, a 4-bit counter is used to control the divider ratio of the prescaler in a PLL synthesizer. The Qa output toggles high and low except when the carry out is asserted. Then the Qa output stays high with the correct load value. For a loaded value of '5', the Qa output will be low for 5 out of the 11 states of the counter, (16-5-1)/2. This sets up a ratio or duty cycle of n = .454. The 'B' bit of the counter can be changed from a 0 to a 1 to change the load value from 5 to 7. In this case the Qa output is low for 4 out of 9 states, ((16-7-1)/2) for a duty cycle of n = .444. The ratios modify the prescaler to produce an output frequency with a fractional divide by ratio, that is 128.454 or 128.444. Therefore the output frequencies differ by (128.454 - 128.444) times the reference oscillator. The rate of change on the modulus control pin is very high relative to the PLL loop bandwidth so the changes are averaged or smoothed out over time.

A simple hardware implementation of a radio link using this method is described here. A family of transmitter or transceiver ICs from RF Micro Devices offer the internal PLL and dual modulus prescaler which can be used in this design. The RF2513 was chosen to demonstrate a simple low cost transmitter for USA ISM band applications. The RF2513 contains all the active circuitry necessary to implement a single IC FSK transmitter; a reference crystal oscillator, PLL, dual modulus prescaler, VCO, TX buffer amp, and PA. The RF2513 also has an internal varactor for tuning the VCO. By using printed inductors for the resonators, the external component count is minimized. A 74HC161 4-bit counter is used to implement the counter and a 74HC04 is used for the necessary inversion to load the counter and to buffer the reference oscillator used for the clock. The schematic of the final circuit is shown in Figure 2.

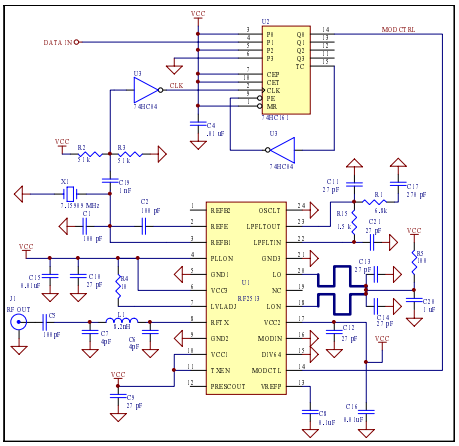


Figure 2. Example Schematic of DC Accurate Modulator

The reference crystal which is supplied with the RF2513 eval board is 7.15909MHz,. This normally produces a transmit frequency of 916.4MHz for a divide by 128 setting. Other values could easily be substituted. Since the divider ratios are 128.454 and 128.444, the output frequencies are 919.6137MHz for a logic “0” and 919.5421MHz for a logic “1” input. Thus, peak to peak deviation is fixed at 71.6kHz. Since the deviation is derived by numerical means as a fraction of the crystal frequency, it is very accurate and repeatable without the tuning. This deviation allows for a wide range of data rates, from 1bps to 100kbps by using different modulation indices. The upper limit is actually limited by the loop bandwidth of the PLL, up to the point where the modulation index becomes too small. In Figure 3, a pseudo random data pattern clocked at a 100bps bit rate is shown as an example of the low data rate capability. The recovered data maintains its DC level through several consecutive data bits providing evidence of the DC accuracy of this modulator. In Figure 4, the same pseudo random data pattern at 72kbps is shown. In each instance, a RF2917 evaluation board tuned for 919.578MHz was used to demodulate the data.

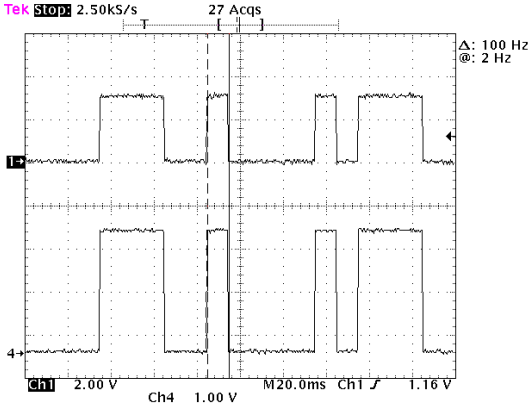


Figure 3. Transmitted Data (top) and Recovered Data (bottom) at 100Bps

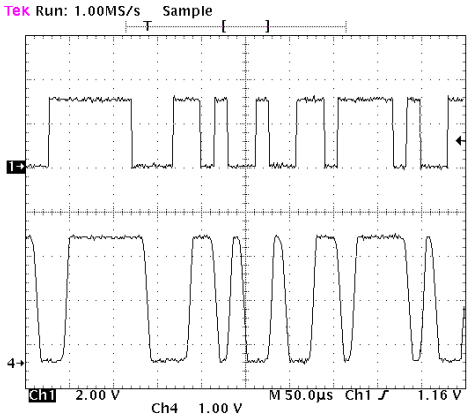


Figure 4. Transmitted Data (top) and Recovered Data (bottom) at 72Kbps

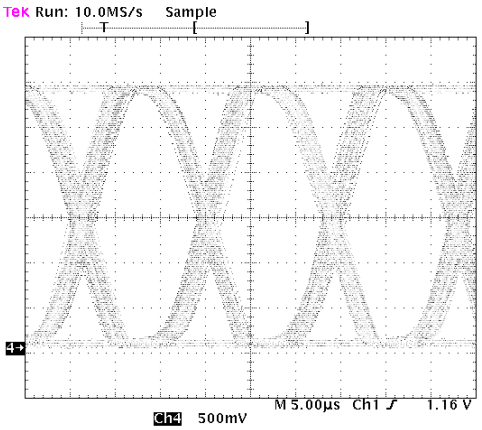


Figure 5. Kbps Eye Pattern

The PLL loop bandwidth is designed to be reasonably wide and yet still provide reasonable spurious rejection. The loop bandwidth is one of the factors that determine the rate at which the VCO changes from one frequency to the other and, thus, the upper data rates. As data rates exceed the loop bandwidth, the modulation waveform becomes band-limited and takes on the appearance of inter-symbol interference. Figure 5 shows the eye pattern of this modulator as seen at the RF2917 receiver output. The flatness of the eye pattern attests to immunity of this modulator to random

data patterns. The slew rate due to the PLL loop bandwidth is also evident here. the high loop bandwidth offers a couple of advantages. First, the close-in phase noise of the VCO is corrected for by the PLL, at best to that of the crystal. More importantly, though, is that the PLL synthesizer will have a faster lock time because of the higher bandwidth. This is useful for systems that occasionally burst a packet of data and then shut down to conserve battery life. Burst type systems are also affected by load pulling when the PA is turned on. The faster loop response can minimize or eliminate out of band spurs due to turn on transients that would be problematic for low data rate systems that use lower loop bandwidths.

For this design, the loop bandwidth is set at 50kHz and a type II, 3rd order loop is used to help with suppression of the crystal reference spurs. Please refer to technical article TA0031 in the 1999 RFMD catalog for more information on designing the loop filters. Figure 6 demonstrates the close in phase noise and Figure 7 shows the spurious output. Also seen in Figure 7 are the modulation spurs that result from the counter cycles. The primary source for these modulation spurs are voltage spikes caused by the gates and flip-flops changing states during the carry over which then get coupled into the VCO. Careful isolation and decoupling are needing to the best suppression of these spurs. The modulated signal, shown in Figure 8, shows an occupied bandwidth (99%) of 150kHz for the 72kbps data rate. The loop filter acts as a smoothing filter and helps shape the frequency spectrum even though the input signal is digital. This bandwidth works well with a receiver using low cost 180kHz ceramic IF filters.

The RF2513 transmitter IC has a companion single IC receiver, the RF2917, for low cost FM or FSK simplex links. The RF2917 incorporates the reference oscillator, PLL, VCO, LNA, downconverting mixer, 94dB limiting IF amps, frequency discriminating demodulator, and data slicer in a single chip. With the addition of a few external, discrete components, a complete FSK receiver can be built. One of the features of this part is the differential connection of the demodulator to the data slicer. A DC averaging circuit is not needed, therefore, the response to receiver data is 1 or 2 bit times and a lengthy preamble is not required. This approach is also immune to the low frequency components in the data pattern that plague the DC averaging circuits. This makes it a perfect receiver to complement the DC-accurate modulator. A fully assembled evaluation board for the RF2917 is available with 180kHz IF filters. By using this bandwidth for low data rates, sensitivity is lost due to the increased noise power over the signal power resulting in less than optimum range. The higher bandwidth and larger deviations do not reduce the frequency accuracy needed, thereby allowing lower-cost crystals to be used.

There are a variety of applications that can benefit from this type of modulation. Computer peripherals, for example, tend to send data in bursts with indeterminate pauses in-between. Wireless keyboards, mice and joysticks are migrating from infra-red to RF, but the immunity to random data patterns and pauses is necessary to guarantee reliable operation. It is generally preferred that remote controls for satellite receivers be RF as opposed to infra-red so that the TV does not have to be co-located with the receiver. The range of infra-red remote controls can be augmented by RF repeaters. An IR receiver data output can be used to modulate this RF2513 circuit and an RF2917 receiver data output can be buffered to drive the IR LEDs. Telemetry sensor outputs such as temperature or fluid level can be transmitted directly from the A/D output with this transmitter without concern for the data pattern. This modulator can also be implemented with the RF2905 transceiver IC to create a low cost half duplex two way radio link.

Conclusions

In conclusion, the enticements of low cost single chip solutions get many people entangled by the problems that random data patterns can cause when modulating VCOs. Veteran radio designers are aware of the problem and several methods for working with it. With so many new applications that need low to moderate data rates at a low cost, this modulator provides a low cost, easy to implement alternative to existing schemes. This modulation scheme is being patented and will be incorporated into new IC which can reduce the overall cost of the transmitter even lower.

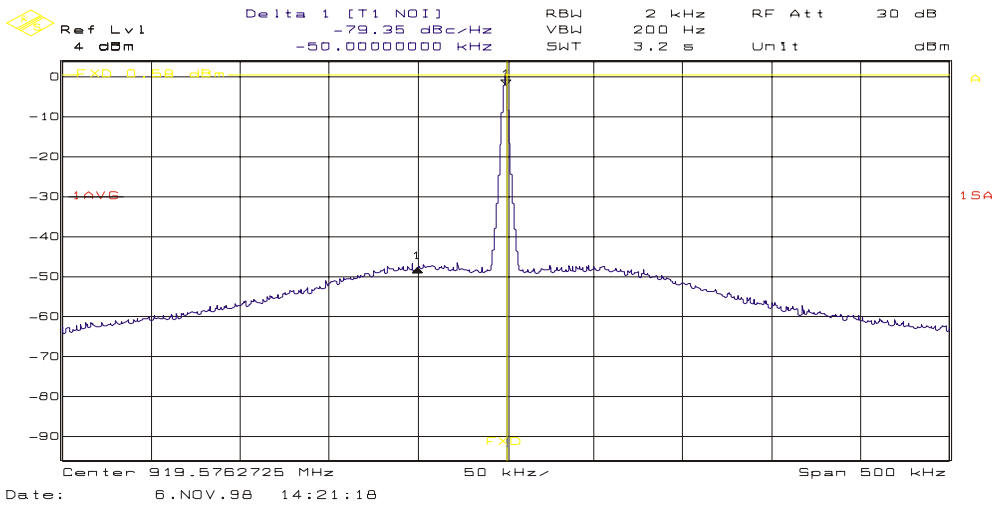


Figure 6. Linear Final Stage RMS Collector Currents for the Two Cases as the Input Signal is Varied

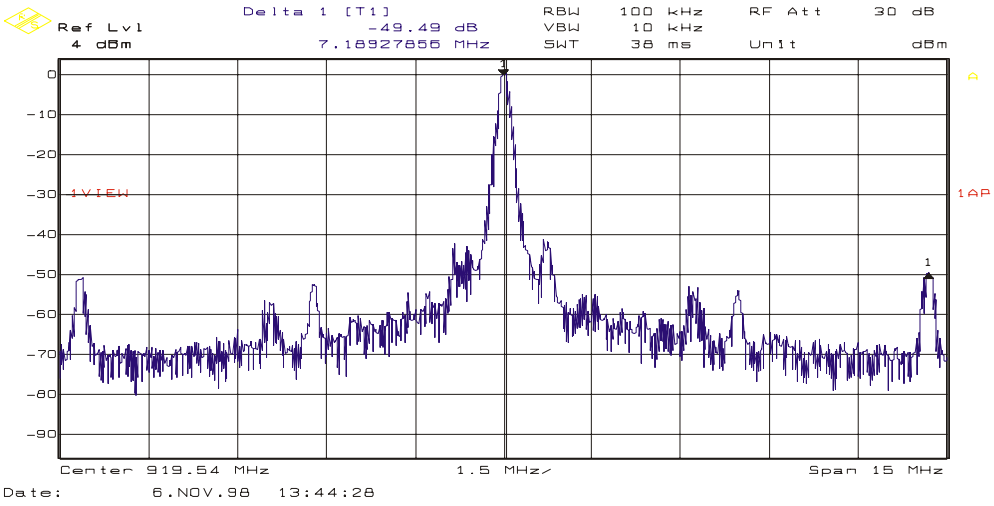


Figure 7. RF2510 Spurious Output with Modulation

13 TECHNICAL NOTES AND ARTICLES

TA0038

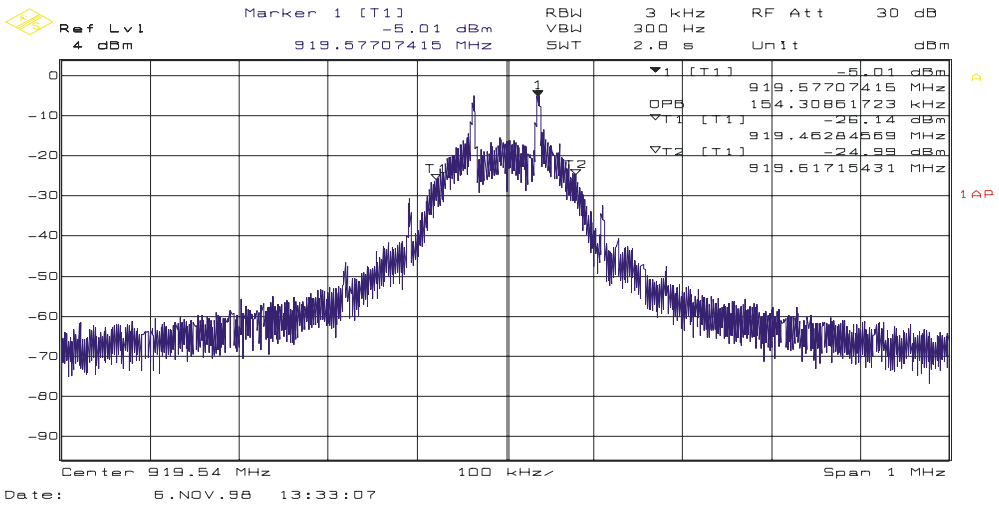


Figure 8. Modulated Spectrum with 72 Kbps Pseudo Random Data

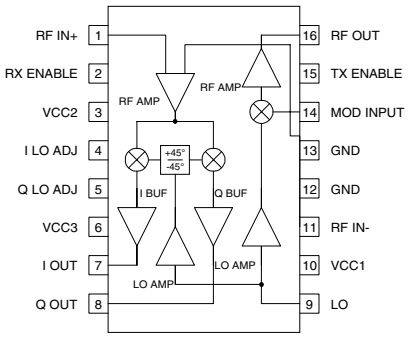
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Integrated Solution Targets 900MHz Cordless Phones

Abstract
Cordless technology has evolved greatly over the past two years. The move to 900MHz and to spread-spectrum systems has forced phone developers and component manufacturers to face strict cost issues (*see Wireless* Systems *Design*, October 1996, p. 18). In order to drive prices down, system-level designers are challenging wireless manufacturers to develop more highly-integrated products. One answer to these problems is using two-chip solutions for the RF portion of the phone, such as the integrated two-chip RF front-end solution developed by RF Micro Devices.

Design Requirements
The two integrated circuits (ICs) that make up the front-end product include the RF9904 transceiver and the RF2403 transceiver front end. Geared for direct-sequence, spread-spectrum (DSSS) 900MHz cordless systems, the combined solution supports direct down-conversion from RF to baseband frequencies. By doing this, the solution eliminates a first RF image filter and an intermediate-frequency (IF) channel filter, thus reducing size and cost. Both ICs are packaged in a 16-pin SOIC plastic package.

Operating across the 700MHz to 1100MHz frequency range, the RF9904 (see Figure 1) transceiver IC includes a transmit binary phase-shift-keying (BPSK) modulator, a receiver quadrature demodulator, a splitter for the local-oscillator (LO) signal, and separate transmit and receive LO buffer amplifiers. The IC contains all of the circuits required for quadrature demodulation, using an integrated LO phase-shift network. It also includes all circuits for biphase modulation.



Meeting the needs of system designers, the transceiver IC is engineered to run from a single +3VDC to +6VDC supply. At +5VDC, the chip consumes 20mA to 35mA current in the receive path and 7mA to 20mA current in the transmit path.

The RF9904 comes equipped with a separate transmit and receive power-down control and a 0MHz to 3MHz in-phase/quadrature (I/Q) frequency. When powered-down, the IC offers a 0.5V off voltage while consuming 100ΩA current. The chip also supports a 100ns maximum switching time when going from power-down to operational mode.

On the receive side, the RF9904 supports a 1.40:1 input VSWR, 10-dB noise figure, a 3MHz baseband frequency, a 1dB compression point of 2dBm, and a +8-dBm third-order-intercept (TOI) point. In this section, the unit also offers a 5mV DC offset between I and Q as well as a 1V peak-to-peak maximum I/Q output level. The transceiver's transmit section features 6kμ modulation input impedance, 0.5V peak-to-peak modulation voltage, -10dBm typical RF output power, and -26dBc carrier suppression.

The RF2403 transceiver front end integrates a single-stage low-noise amplifier (LNA), a two-stage power amplifier, and a low-loss transmit/receive (T/R) switch in a single package. Although designed for cordless phones operating across the 915MHz range, the device can be used in applications within an octave of 915MHz since the IC has little on-chip tuning circuitry.

This front-end device offers independent transmit and receive lines which enable it to be driven be complementary-metal-oxide-semiconductor (CMOS) logic. It also features single +5VDC operation. When working from this supply, the unit consumes 1mA to 2mA quiescent current in receive mode, and 70mA to 115mA current in transmit mode. The unit's T/R switch provides 0.8dB insertion loss and 17dB isolation.

On the transmit side, the unit offers a +15dBm to +20dBm two-tone output-power level through the T/R switch. In this mode, it also features 22dB transmit large-signal gain, 1mA to 1.5mA transmit enable-line consumption, and -27dBc to 25dBc third-order intermodulation suppression. In receive mode, the front-end IC supports a 2.9dB antenna-port noise figure, 12dB to 20dB gain, and 0.1mA to 0.5mA receive enable-line current.

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A Study of Device Input Impedance in PSpice

When coupled with accurate nonlinear models, Spice allows observation and manipulation of circuit behavior that is impossible in the lab using test equipment. The procedures outlined have been developed using PSpice [1], although the principles apply to Spice programs in general.

One aspect of a circuit's behavior that is of interest to amplifier designers, and power amplifier designers in particular, is the input impedance of a device under large-signal drive. In the past, this quantity has been approximated by the small-signal value, determined from S-parameters or small-signal analysis. However, as the signal levels increase and nonlinear currents begin to flow, the impedance shifts.

There a number of ways to determine the nonlinear input impedance, but the most straightforward is the introduction of a sensing resistor (0.001Ω) into that circuit branch to monitor the voltage and current. This works fine for AC analysis (i.e., small-signal) but for large-signal transient analysis, V(t)/I(t) is not the device input impedance. The impedance can be determined by applying a fast Fourier transform (FFT) to V(t) and I(t) to generate magnitude and phase of the fundamental before the division. This approach is not a familiar technique to RF designers where the foundation for impedance measurement and transformation is based upon s-parameters. Standard Spice s-parameter techniques have been adapted for large-signal applications.

S-parameter measurements are conducted by applying energy to a system port. All the remaining ports are terminated with a convenient impedance. Energy is reflected back toward the source, and some energy comes out the remaining ports. The excitation is at a known amplitude and frequency, and the amplitude and phase of the transmitted and reflected signals may be determined. For small-signal measurements, harmonic generation is not a problem. Large-signal waveforms in a nonlinear system will be distorted. In this case, the reflected signal contains the fundamental tone plus varying amounts of harmonics. Is S11 all the reflected energy or just the energy contained in the fundamental? A simplifying assumption is to only consider the fundamental frequency. In this case, the goal is to determine the input impedance for matching purposes, and the impedance at the input frequency is the desired result.

In determining the input impedance in the final circuit of a device under bias conditions, the primary focus will be S11. If desired, the output signal at the load can be easily determined, allowing a computation of S21. The amplifier may then be turned around within the test set-up to provide S22 and S12.

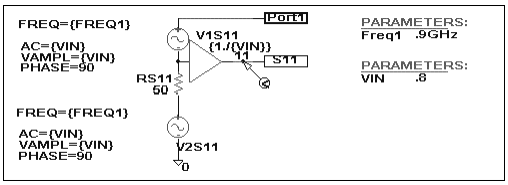


Figure 1. Single Port S-Parameter Test Set (modified for large signal TRANsient analysis)

S-Parameter test set

The S-parameter test set is shown in Figure 1. This is an extension of the standard test set with the following features:

1. A large-signal sine wave generator (a PSpice VSIN element) has been used in place of the small-signal AC source.
2. The large-signal frequency is set by the parameter FREQ1 so both generators track. During AC analysis, the source frequency for both generators is swept in the normal fashion.
3. The peak signal amplitude is set by the parameter VIN for both the AC and the transient case.
4. The S11 output is normalized by the (1/VIN) gain block.
5. The phase of the large signal source is offset by 90^{o} to provide the correct phase after the FFT.
6. A global symbol for Port1 is used to allow the signal generator to reside on a different page of the schematic.

The addition of the amplitude parameter VIN and the output signal scaling allows this test set to be used as a variable amplitude signal source. Electrical energy is applied to the circuit input port. Impedance mismatches between the generator and the circuit cause reflections and phase shifts in the reflected signal. The reflected signal at S11 of the test set contains the desired impedance information according to [1]:

$$\frac{Z}{Zo} = \frac{1 + S11}{1 - S11} \qquad [1]$$

where S11 is a complex number (normally presented as τ in this type of expression) and Zo is the reference impedance of the system RS11 of 50Ω in Figure 1.

This brings up an interesting issue concerning what source impedance should be used. Actually, it doesn't matter, because the reflected energy is related to the impedance ratio. However, the power delivered into the port is reduced by the reflected energy, and the drive level may need to be modified to provide a given input power. The accuracy for the computed impedance will be improved if the value of S11 is toward the center of the Smith chart. For example, a power device may have an input impedance close to 10Ω. If RS11 is changed to 10Ω, better efficiency will be obtained in coupling energy into the device, the reflected energy represented by S11 will be smaller, and the resultant device impedance will be obtained with improved accuracy.

The circuit to be investigated is shown in Figure 2. C1 and C2 provide DC blocks for the device input and output. Actually, C1 will become part of the interstage matching network. The two transmission lines have a time delay that is 90° at 900MHz. T1 provides a quarterwave stub for collector bias, and T2 transforms the 50-Ω load into 1Ω at the device collector.

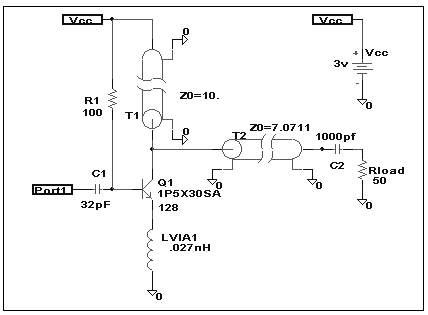


Figure 2. Test Transistor with Bias and Output Transformer

Before starting the nonlinear study, a linear (i.e. AC) analysis of the circuit is beneficial. The test set is connected and swept from 800-1,000MHz. RS11 was set at 10Ω and is the basis for the measurements. The output can be displayed in a familiar presentation by plotting the imaginary part of S11, i.e. IMG(V(S11)) on the y-axis and the real part of the S11, i.e. R(V(S11)) on the x-axis. The scale on both axes ranges from -1 to +1. This polar form (shown in Figure 3) is one of the normal presentations of S-parameters. In this case the Smith chart grid system is missing.

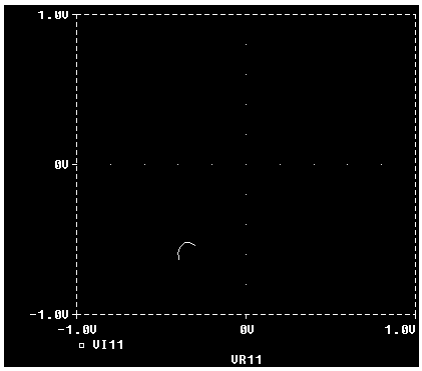


Figure 3. Small Signal S11 Displayed in Polar Format

Equation 1 may be rewritten in polar coordinates by expressing S11 as:

$$S11 = M\cos\phi + jM\sin\phi \quad [2]$$

where M is the magnitude and ϕ is the angle of S11.

$$\frac{Z}{Zo} = \frac{1 - M \times M + j2M\sin\phi}{1 + M \times M - 2M\cos\phi} \quad [3]$$

At 900 MHz the value of S11 from the figure is 0.659 at -125.3°. Using these values in Equation 3 along with 10μ for the reference impedance is Zo, the small-signal input impedance is computed at Z=2.57-j4.90.

Large-signal excitation

Three factors must be taken into account when a large-signal transient analysis is performed for S-parameter analysis. To avoid introducing errors in the FFT, the initial transient response of the circuit must have decayed, the section of waveform selected for analysis must contain an integer number of cycles, and the waveform must start at an integer number of periods after t=0. Figure 4 shows the voltage waveform at the circuit input, output and the reflected input signal. This was generated with VIN = 0.6V and RS11 at 10Ω. Even at this level, the circuit is starting to generate obvious non-linearities. Notice that the signals do not reach a steady state until almost 15nsec into the simulation. If a section of the waveform from 20-40nsec is used for analysis, 18 complete cycles will be starting exactly 18 cycles after t=0. This is important because any shifting along the time axis is a phase shift after

the FFT. Anything other than an integer number of cycles will directly affect the results.

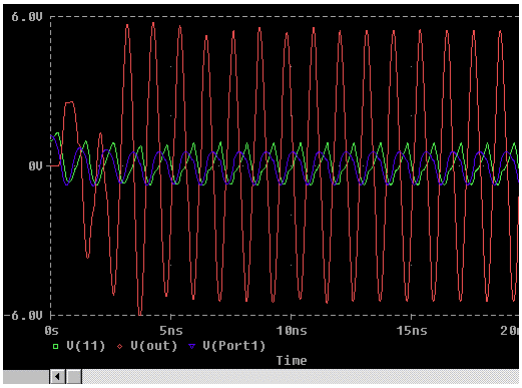


Figure 4. Circuit Response Waveforms Showing the Initial Start-Up Transients

A simulation that swept the VIN parameter from 0.05-1 V at 900MHz was set up and a transient analysis was generated for 40nsec at each VIN value. The output data was restricted to a range from 20-40nsec for the subsequent processing. An FFT of V(S11) was performed and the magnitude and phase data were copied into a spread sheet. The data at 900MHz was selected and processed according to Equation 3. Figure 5 shows the results of that calculation. As can be seen, the driving point impedance of this device changes radically with drive level.

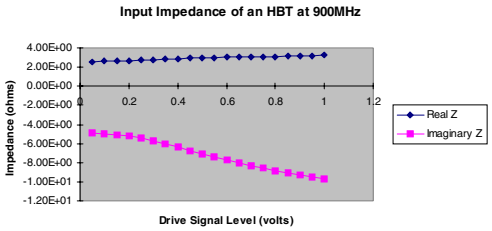


Figure 5. Variation in Input Impedance with Drive Level

Now suppose that VIN = 0.6V was a desired input signal amplitude. This level may provide the optimum efficiency or minimum distortion. At VIN = 0.6V, the input impedance is (from the data used in the plot) Z = 3.02 - 7.75j. This is the impedance needed for the interstage matching network design that will implement the desired features. However, one more interesting experiment sheds light on the dynamics of the problem.

The magnitude of S11 at this drive level was 0.688. The power delivered into the device is:

$$Pin = (1 - S11 \times S11) \times Vin \times \frac{Vin}{(4 \times RS11 \times 2)}$$

$$= (1 - 0.688 \times 0.688) \times 0.6 \times \frac{0.6}{(4 \times 10 \times 2)} \quad [4]$$

$$= 2.37mW$$

(the factor of 2 is to convert peak to RMS and Zo is 10Ω). Now the test set can be matched to the device. A 1.37nH inductor has an impedance of 7.75jΩ at 900 MHz. An inductor is added in series with the test set to cancel out the capacitive component in the device, and the base impedance RS11 is changed to 3.02Ω.

Re-sweeping the VIN parameter from 0.05V to 1V and plotting the magnitude of V(S11) (see Figure 6) shows that, at about the 0.225V input drive level, there is an excellent power match to the test set. The source impedance is a conjugate of the device impedance previously determined. The power delivered to the device at the fundamental frequency and new drive level approaches 2.07mW. This is close to the previous value. VIN is lower because the system impedance has been reduced, and most of the energy is now coupled into the device. Also, the power reflected at the second harmonic has increased. The key point illustrated by this exercise is that the optimum matching network designs for large-signal applications will depend on the signal level.

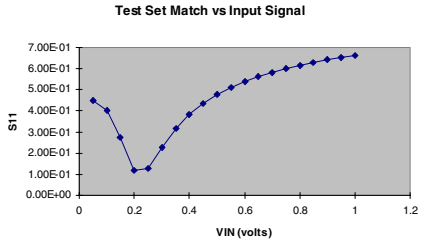


Figure 6. Test Set Match versus Input Level for Z=3.02+7.75j

Linear impedance sniffer

Are the results valid? Can these results be obtained in some other fashion that allows verification of the calculations? In the case of a linear analysis or transient analysis with a small input signal, the answer is yes. An

impedance sniffer shown in Figure 7 can be used to directly present the real and imaginary impedance at any point in a circuit. The 10-megohm resister is there to keep PSpice happy (i.e., converging) when the "test" port is open circuited.

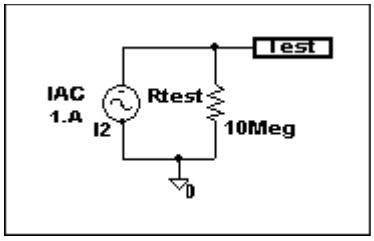


Figure 7. Impedance Sniffer for AC Analysis

The test point is connected to the desired circuit node, and 1 A of AC current is injected. Ohm's law is considerably simplified in this case. The real and imaginary voltage at the test port is the real and imaginary impedance. But you can't inject an ampere of AC current just anywhere. In the AC analysis, everything is linearized. The current source could be set for a mega-amp, but it's easier to divide by one. Running the simulation (Figure 2 with PORT1 replaced by TEST) and taking the real R(V(test)) and imaginary IMG(V(test)) at 900 MHz produces the linearized input impedance of 2.571 - j4.897. This value agrees well with the previous calculations.

Conclusions

A method of determining the large signal input impedance of a circuit has been presented that is useful within PSpice. The procedure is straightfoward to implement and self-consistent. As the source signal level is reduced, the impedance converges to the values determined from small signal analysis. These same tools can also be used to determine how a large signal match varies with signal level. One important question remains. Are the impedances believable? The decision to believe the results is based on the trust in the device models. How do you gain trust in the model? One way is to design circuits using the models and then see if they perform according to those predictions when they are fabricated. And, to that end, large signal S-parameter techniques can improve the design process.

References

1.PSpice is a registered trademark of MicroSim Corp.

2.Vendelin, George, *Design of Amplifiers and Oscillators by the S-Parameter Method*, John Wiley, 1982.

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14 Quality And Reliability

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"Total Customer Satisfaction By Providing Products With Exceptional Quality, Reliability and Performance Standards"

Introduction

RF Micro Devices, an ISO9001 company, is committed to providing products of world class design, performance, reliability and quality. Our quality program includes conservative design techniques, extensive subcontractor and supply line management, comprehensive statistical process control, and 100 percent RF and DC test. Whether manufactured at our own GaAs HBT foundry, or one of our foundry partners, RF Micro Devices' rigorous attention to quality has resulted in a high level or customer satisfaction. Because of this, RF Micro Devices has become one of the world's fastest growing RF integrated circuit manufacturers.

ISO 9001

RF Micro Devices is ISO9001 certified. ISO9001 breaks a quality system down into 20 key areas, or sections. These sections form the framework for RF Micro Devices' successful quality system. ISO9001 offers something many other quality systems do not: stringent requirements on the key elements of quality program framework, combined with the flexibility to decide how to best implement that framework. For a copy of our Corporate Quality Manual, please contact your RF Micro Devices sales representative.

Designed-in Reliability

Our products are designed and developed using conservative design rules and cutting edge commercial and proprietary design tools. In order to assure strict compliance to foundry specifications, all designs are scrutinized using computerized, proprietary Design Rule Checks (DRC's). These checks help ensure high reliability and significant manufacturing margin. In addition, simulation tools evaluate circuit performance under worst-case conditions of temperature and process variation. In all cases, the designs are centered on standard foundry processes and tolerances, and do not require any product-specific process control or screening.

Sub-Contract

RF Micro Devices supplements its in-house capabilities by using qualified foundries and off-shore packaging and assembly operations. All outside suppliers are well established, certified facilities with exceptional quality programs. After the facilities pass RF Micro Devices' initial qualification process, the compliance of our vendors to performance and quality requirements is strictly monitored. Our compliance assurance program includes incoming inspection operations, as well as regular audits.

Production Test

High speed, automated IC handlers and test equipment are used to ensure consistent lot-to-lot product uniformity. All products are 100 percent tested at RF Micro Devices for critical RF and DC parameters. The goal for all products is to maintain a Cpk>1.5 relative to each critical product specification (corresponding to a 4.5 sigma distribution). All production test data is evaluated using standard SPC techniques and then archived for future use. Any control limit violations will alert our Production Test and Quality departments that corrective action is required.

Process Control Monitors

Process control monitors (PCMs) are used throughout the production process, including critical areas of fabrication, assembly, and electrical test. The table below shows electrical, mechanical, reliability, and environment stress control monitors used to monitor final packaged products. These and other monitors are used to ensure the quality of all products, to guide our quality improvement efforts, and to focus our energy on areas which can further enhance our process capabilities.

Process Control Monitor Testing

(these tests are subject to change without notice)

Thermal Shock Test, Liquid-to-Liquid

- 30 Cycles @ T = -45°C to +125°C, Dwell 5 Minutes @ Each Temperature
- MIL-STD-883, Method 1011, Condition B (M)
- Quarterly Per Package Family, Process Technology and Assembly Location

Pressure Pot Test

- Temperature = +121°C @ 2 ATM & 100% Relative Humidity For 96 Hours
- Quarterly Per Package Family, Process Technology and Assembly Location

Operating Lifetest

- Ambient Temperature = +150°C For 185 Hours(min) to 1000 Hours(max)
- Bi-Quarterly Per Assembly Location and Process Technology

Solderability
- MIL-STD-883 Method 2003
- Quarterly Per Package Family and Assembly Location

Resistance to Solvents
- MIL-STD-883 Method 2015
- Quarterly Per Package Family and Assembly Location

Lead Integrity
- MIL-STD-883 Method 2004
- Performed Bi-Quarterly Per Package Family and Assembly Location

Bond Strength
- MIL-STD-883 Method 2011
- Bi-Quarterly Per Package Family, Assembly Location, and Process Technology

ESD
- MIL-STD-883 Method 3015
- Yearly Per Process Technology and Foundry

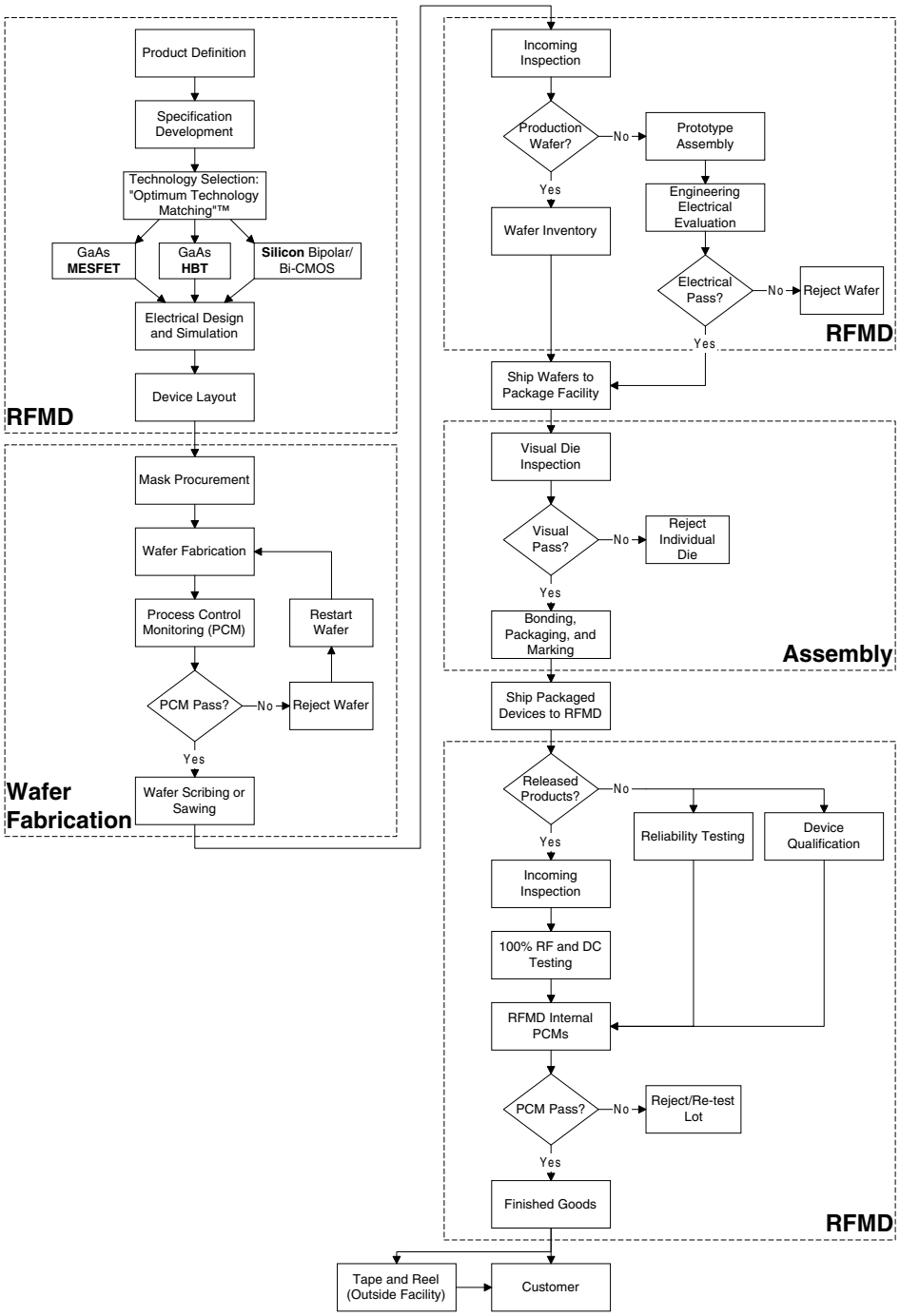
ESD

As with all high-performance integrated circuits, caution must be used when handling RF Micro Devices products. Without proper precautions, electrostatic discharge can be a major contributor to device failures.

Electrostatic discharge sensitivity (ESDS) is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESDS classification testing, and is used as the basis for assigning an ESDS class. RF Micro Devices continually evaluates devices to determine the ESD sensitivity level. RF Micro Device's standard method of ESD testing is Human Body Model (HBM), although Charged Device Model (CDM) or Machine Model (MM) testing can be performed as well. Knowing the ESD sensitivity will enable the end user to asses the adequacy of work areas, shipping materials, storage materials, and production equipment used while handling RF Micro Devices parts. We recommend that all personnel wear conductive smocks, heel straps on both feet or conductive shoes, wrist straps (RF Micro Devices recommends the use of 3M 722 continuous monitor wrist straps), and antistatic hand lotion. Production facilities should have ESD safe floors, and all benches, chairs, and production equipment should be grounded. ESD generating materials (paper, glass, plastic, Scotch tape, styrofoam, etc.) should be kept out of ESD safe areas at all times. All employees should be soft grounded via a 1Mohm resistor, and all equipment should be hard grounded.

Continuous process improvement and the relentless drive to exceed customer quality and reliability needs is a critical part of our success. Please contact RF Micro Devices for more detailed information on our Quality Program.

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15 Sales and Ordering Information

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Ordering Information
To order any product, obtain pricing information, or for additional applications information, please contact your local factory sales representative *or RFMD customer service*. Listings of both domestic and international sales representatives are provided in the Sales Information section of this catalog.

Purchase orders may be faxed to RF Micro Devices at (336) 664-0454, or may be sent to your local representative. In either case, the original copy of the purchase order should be sent to the factory as confirmation. If you are a new customer, we ask that you include a copy of your credit references when initially placing your order.

Standard terms are net 30. Payment may be made by check payable to RF Micro Devices, Inc. We also accept VISA, MasterCard, American Express, Discover, bank draft and money orders.

Delivery is FOB Greensboro, North Carolina.

Availability
To support pre-production, off-the-shelf delivery is available on all standard products. Evaluation boards with matching components and SMA connectors are available for a nominal fee. Samples of all products are also available for immediate evaluation. Prototype parts are sometimes not available as samples or for orders; please contact your local factory sales representative or RFMD customer service to ascertain availability.

Sample Requests
Requests for samples and evaluation boards should be placed through the Customer Service Department.

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Warranty

RF Micro Devices warrants its products to be free from defects in materials and workmanship under proper use in normal conditions for a period of one year from the date of shipment. Return of product in question should be made prepaid to RF Micro Devices for evaluation. If product is found to be defective, RF Micro Devices will repair or replace, at its option, said defective product. This warranty does not apply to products which have been disassembled, modified, or subjected to conditions exceeding the application specifications.

Disclaimer

RF Micro Devices reserves the right to change circuit designs or specifications at any time without notice. It is the user's responsibility to verify that the information in this publication is current at the time of placing orders. The applications information included herein is intended solely for general guidance and information. Use of these devices in a user's specific application is at the user's own risk.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s). These products should not be used in critical life support devices or systems.

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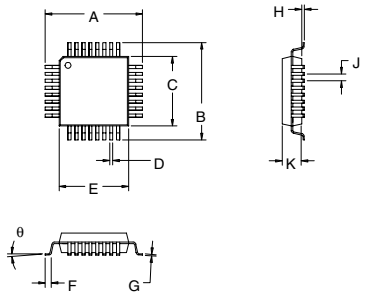
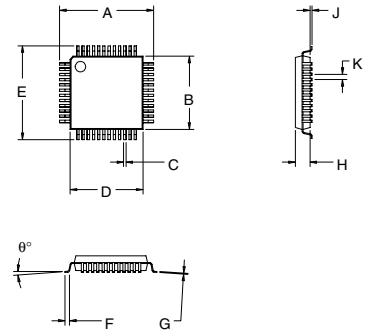
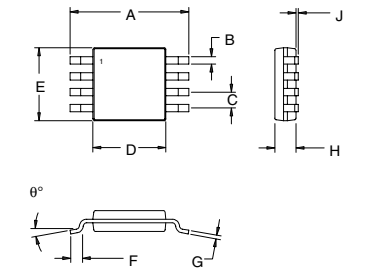
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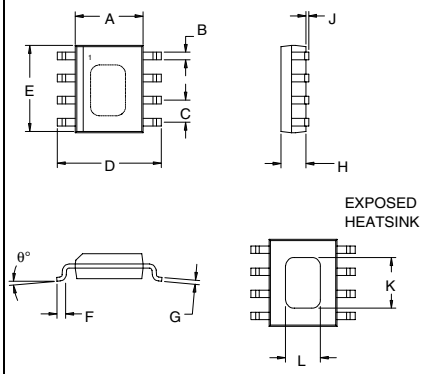
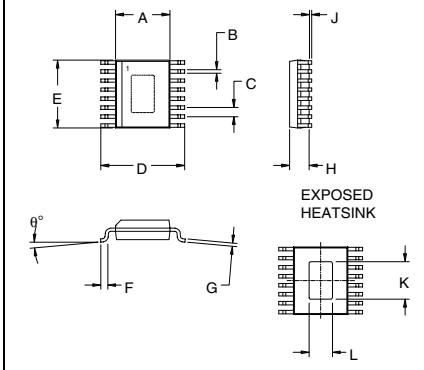
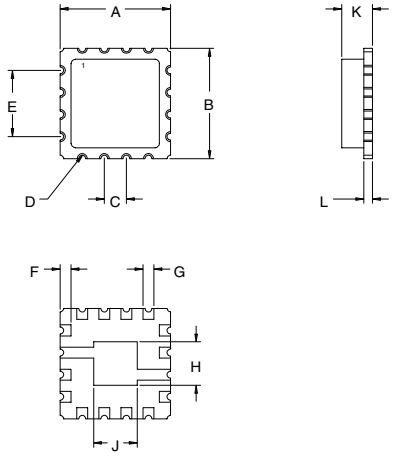
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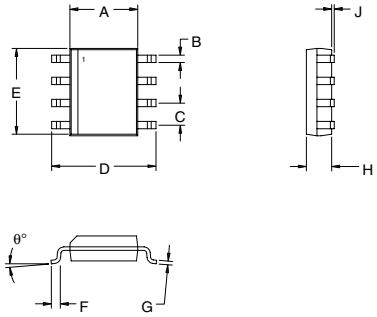
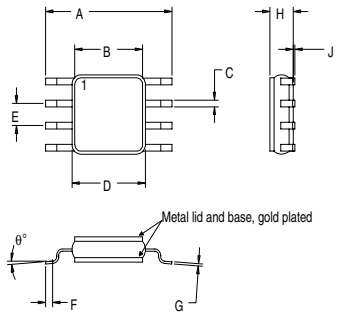
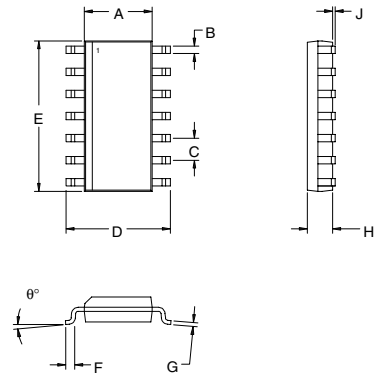
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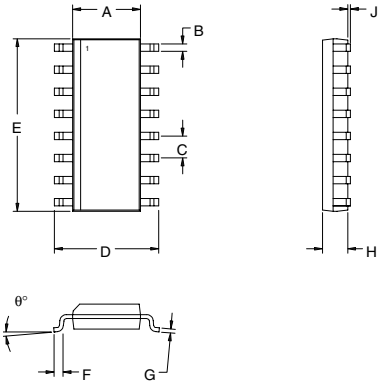
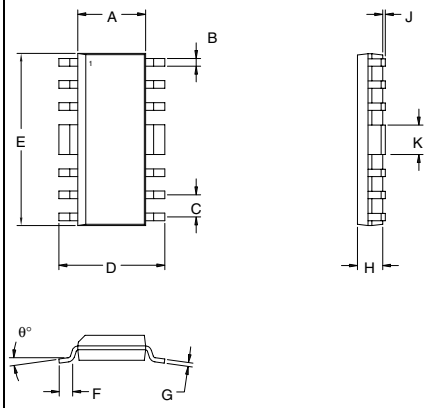
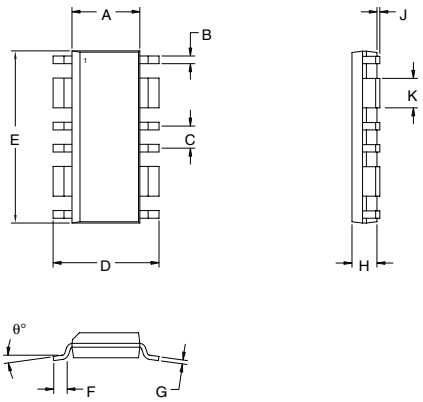
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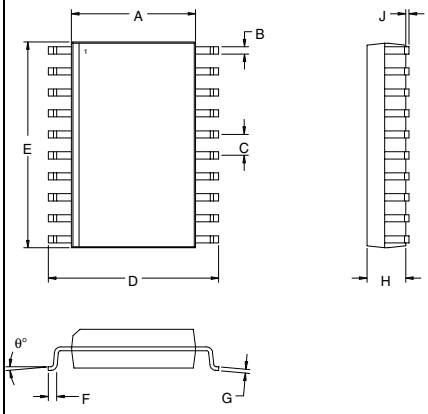
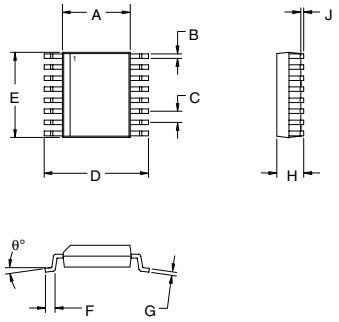
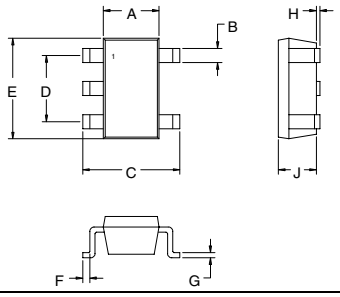
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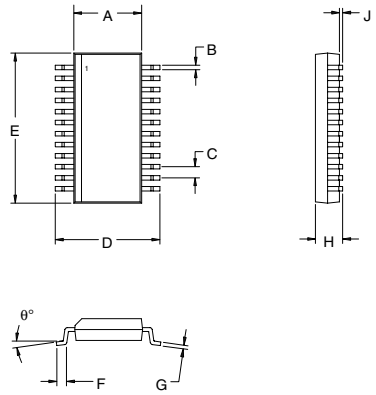
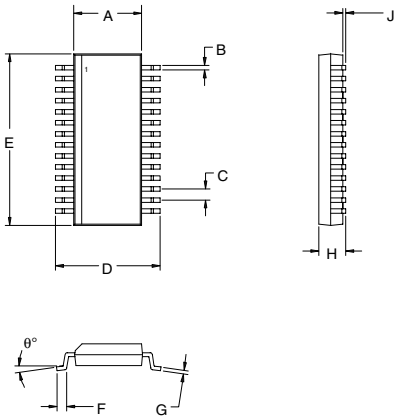
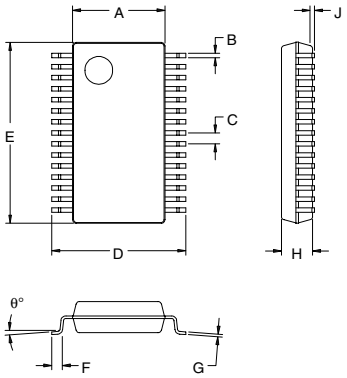
Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
LQFP-32 	A	7.00	±0.20	0.276	±0.008
	B	7.00	±0.20	0.276	±0.008
	C	5.00	±0.10	0.197	±0.004
	D	0.22	±0.05	0.009	±0.002
	E	5.00	±0.10	0.197	±0.004
	F	0.60	+0.15, -0.10	0.024	+0.006, -0.004
	G	0.127		0.005	
	H	0.05 to 0.15		0.002 to 0.006	
	J	0.50		0.020	
	K	1.40	±0.05	0.055	±0.002
	θ	0° to 7°		0° to 7°	
LQFP-48 	A	9.00	±0.20	0.354	±0.008
	B	7.00	±0.10	0.276	±0.004
	C	0.22	±0.05	0.009	±0.002
	D	7.00	±0.10	0.276	±0.004
	E	9.00	±0.20	0.354	±0.008
	F	0.60	+0.15, -0.10	0.025	+0.006, -0.004
	G	0.17 Max		0.007 Max	
	H	1.40	±0.05	0.055	±0.002
	J	0.05 to 0.15		0.002 to 0.006	
	K	0.50		0.020	
	θ	0° to 7°		0° to 7°	
MSOP-8 	A	4.90	±0.08	0.193	±0.003
	B	0.33	±0.08	0.013	±0.003
	C	0.65		0.026	
	D	3.00	±0.05	0.118	±0.002
	E	3.00	±0.05	0.118	±0.002
	F	0.56	±0.13	0.022	±0.005
	G	0.18	±0.05	0.007	±0.002
	H	0.86	±0.05	0.034	±0.002
	J	0.10	±0.05	0.004	±0.002
	θ	0° to 6°		0° to 6°	

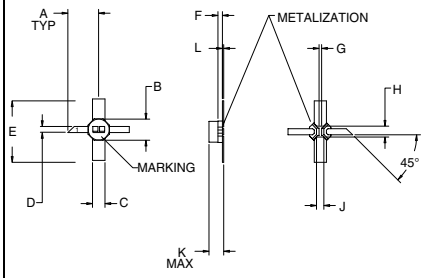
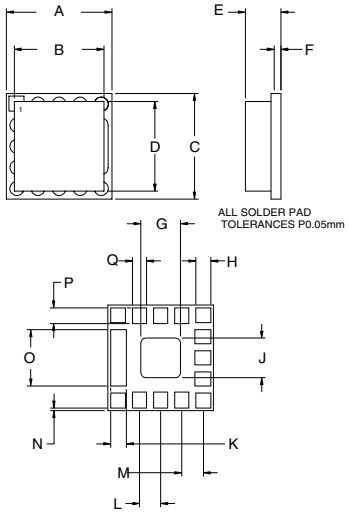
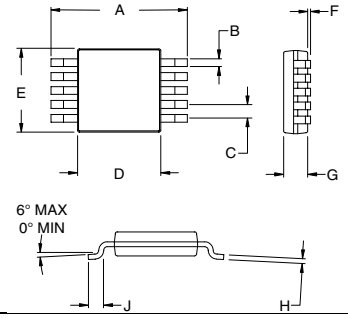
Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
PSOP-8	A	3.91	+0.08, -0.10	0.154	+0.003, -0.004
	B	0.41	±0.08	0.016	±0.003
	C	1.27		0.050	
	D	6.02	±0.18	0.237	±0.007
	E	4.90	+0.08, -0.10	0.193	+0.003, -0.004
	F	0.64	+0.25, -0.23	0.025	+0.010, -0.009
	G	0.23	+0.03, -0.05	0.009	+0.001, -0.002
	H	1.47	±0.08	0.058	±0.003
	J	0.05	±0.025	0.002	±0.001
	K	2.92	±0.20	0.115	±0.008
	L	2.00	±0.20	0.079	±0.008
	θ	0° to 8°		0° to 8°	
PSSOP-16	A	3.90	±0.10	0.154	+0.003, -0.004
	B	0.25	±0.05	0.010	±0.002
	C	0.65		0.026	
	D	6.00	±0.20	0.236	±0.008
	E	4.90	±0.10	0.193	±0.004
	F	0.60	±0.15	0.024	±0.006
	G	0.20 to 0.24		0.008 to 0.009	
	H	1.40	±0.10	0.055	±0.004
	J	0.05	±0.025	0.002	±0.001
	K	2.69	±0.10	0.106	±0.004
	L	1.68	±0.10	0.066	±0.004
	θ	0° to 8°		0° to 8°	
QLCC-16	A	6.35	±0.20	0.250	±0.008
	B	6.35	±0.20	0.250	±0.008
	C	1.27		0.050	
	D	Radius 0.20		Radius 0.008	
	E	3.81		0.150	
	F	0.64	±0.20	0.025	±0.008
	G	0.64		0.025	
	H	2.49		0.098	
	J	2.49		0.098	
	K	1.78	±0.13	0.070	±0.005
	L	0.51	±0.05	0.020	±0.002

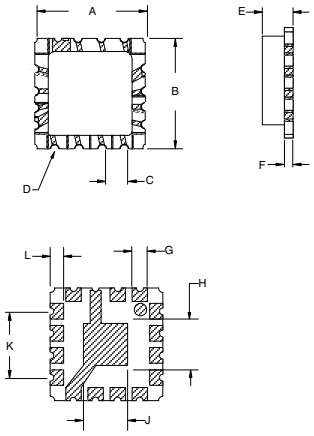
Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
SOP-8 	A	3.90	±0.05	0.154	±0.002
	B	0.43		0.017	
	C	1.27		0.050	
	D	6.00	±0.10	0.236	±0.004
	E	4.90	±0.20	0.193	±0.008
	F	0.50	±0.05	0.020	±0.002
	G	0.20		0.008	
	H	1.37	±0.05	0.054	±0.002
	J	0.10 Min		0.004 Min	
	θ	5°		5°	
SOP-8-C 	A	7.87	±0.13	0.310	±0.005
	B	4.22 Square		0.166 Square	
	C	0.38	±0.05	0.015	±0.002
	D	4.57 Max		0.180 Max	
	E	1.27		0.050	
	F	0.38	±0.05	0.015	±0.002
	G	0.13	±0.03	0.005	±0.001
	H	1.45 Max		0.057 Max	
	J	0 to 0.10		0 to 0.004	
	θ	0° to 4°		0° to 4°	
SOP-14 	A	3.90	±0.09	0.154	±0.004
	B	0.41	±0.05	0.016	±0.002
	C	1.27		0.050	
	D	6.00	±0.20	0.236	±0.008
	E	8.65	±0.09	0.340	±0.003
	F	0.84	±0.43	0.033	±0.017
	G	0.22	±0.03	0.009	+0.001, -0.002
	H	1.61	±0.09	0.063	+0.004, -0.003
	J	0.18	+0.07, -0.08	0.007	±0.003
	θ	0° to 8°		0° to 8°	

Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
SOP-16 	A	3.90	±0.09	0.154	±0.004
	B	0.41	±0.05	0.016	±0.002
	C	1.27		0.050	
	D	6.00	±0.20	0.236	±0.008
	E	9.89	±0.09	0.390	+0.003, -0.004
	F	0.84	±0.43	0.033	±0.017
	G	0.22	±0.03	0.009	+0.001, -0.002
	H	1.41	±0.09	0.063	+0.004, -0.003
	J	0.18	+0.07, -0.08	0.007	±0.003
	θ	0° to 8°		0° to 8°	
SOP-16 BW 	A	3.91	±0.10	0.154	±0.004
	B	0.43	±0.08	0.017	±0.003
	C	1.27		0.050	
	D	6.02	±0.18	0.237	±0.007
	E	9.88	±0.08	0.389	±0.003
	F	0.64	+0.25, -0.23	0.025	+0.010, -0.009
	G	0.23	±0.03	0.009	±0.001
	H	1.45	+0.05, -0.08	0.057	+0.002, -0.003
	J	0.17	+0.06, -0.08	0.007	+0.002, -0.003
	K	1.69	+0.06, -0.07	0.067	+0.002, -0.003
	θ	0° to 8°		0° to 8°	
SOP-16 QBW1 	A	3.91	±0.10	0.154	±0.004
	B	0.43	±0.08	0.017	±0.003
	C	1.27		0.050	
	D	6.02	±0.18	0.237	±0.007
	E	9.88	±0.08	0.389	±0.003
	F	0.64	+0.25, -0.23	0.025	+0.010, -0.009
	G	0.23	±0.03	0.009	±0.001
	H	1.45	+0.05, -0.08	0.057	+0.002, -0.003
	J	0.17	+0.06, -0.08	0.007	+0.002, -0.003
	K	1.69	+0.06, -0.07	0.067	+0.002, -0.003
	θ	0° to 8°		0° to 8°	

Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
SOP-20 	A	7.50	±0.10	0.295	±0.004
	B	0.41	±0.05	0.016	±0.002
	C	1.27		0.050	
	D	10.31	±0.20	0.406	±0.008
	E	12.75	±0.10	0.502	±0.004
	F	0.76	±0.25	0.030	±0.010
	G	0.27	±0.05	0.011	±0.002
	H	2.34		0.092	
	J	0.20	±0.10	0.008	±0.004
	θ	0° to 8°		0° to 8°	
SSOP-16 	A	3.90	±0.09	0.154	±0.003
	B	0.26	±0.05	0.010	±0.002
	C	0.64		0.025	
	D	6.00	±0.20	0.236	±0.008
	E	4.89	±0.09	0.192	±0.003
	F	0.84	±0.43	0.033	±0.017
	G	0.22	±0.03	0.009	+0.001, -0.002
	H	1.55	±0.20	0.061	+0.007, -0.008
	J	0.18	+0.07, -0.08	0.007	±0.003
	θ	0° to 8°		0° to 8°	
SOT-23-5 	A	1.60	+0.20, -0.10	0.063	+0.008, -0.004
	B	0.40	+0.10, -0.05	0.016	+0.004, -0.002
	C	2.80	±0.20	0.110	±0.008
	D	1.90	+0.30, -0.20	0.075	±0.008
	E	2.90	±0.20	0.114	±0.008
	F	0.20 Min		0.008 Min	
	G	0.15	+0.10, -0.05	0.006	+0.004, -0.002
	H	0.00 to 0.10		0.00 to 0.004	
	J	1.10	+0.20, -0.10	0.043	+0.008, -0.004

Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
SSOP-24 	A	3.90	±0.09	0.154	±0.003
	B	0.26	±0.05	0.010	±0.002
	C	0.64		0.025	
	D	6.00	±0.20	0.236	±0.008
	E	8.60	±0.09	0.340	±0.003
	F	0.84	±0.43	0.033	±0.017
	G	0.22	±0.03	0.009	+0.001, -0.002
	H	1.55	±0.20	0.061	+0.007, -0.008
	J	0.18	+0.07, -0.08	0.007	±0.003
	θ	0° to 8°		0° to 8°	
SSOP-28 	A	3.90	±0.09	0.154	±0.003
	B	0.26	±0.05	0.010	±0.002
	C	0.64		0.025	
	D	6.00	±0.20	0.236	±0.008
	E	10.00	+0.21, -0.20	0.394	±0.008
	F	0.84	±0.43	0.033	±0.017
	G	0.22	±0.03	0.009	+0.001, -0.002
	H	1.55	±0.20	0.061	+0.007, -0.008
	J	0.18	+0.07, -0.08	0.007	±0.003
	θ	0° to 8°		0° to 8°	
SSOP-30 	A	5.30	+0.00, -0.10	0.209	+0.000, -0.004
	B	0.30	±0.10	0.012	±0.004
	C	0.65	±0.12	0.026	±0.005
	D	7.70	±0.20	0.303	±0.008
	E	10.40 Max		0.409 Max	
	F	0.60	±0.15	0.024	±0.006
	G	0.15	±0.05	0.006	±0.002
	H	1.80	±0.05	0.071	±0.002
	J	0.10	+0.05, -0.10	0.004	+0.002, -0.004
	θ	1° to 7°		1° to 7°	

Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
Micro-X-CF	A	2.54	±0.38	0.100	±0.015
	B	1.78	±0.08	0.070	±0.003
	C	1.02	±0.13	0.040	±0.005
	D	0.51	±0.13	0.020	±0.005
	E	5.10	±0.38	0.200	±0.015
	F	0.30	±0.05	0.012	±0.002
	G	0.20	±0.05	0.008	±0.002
	H	0.89	±0.08	0.035	±0.003
	J	0.61	±0.05	0.024	±0.002
	K	1.45 Max		0.57 Max	
	L	0.13	±0.05	0.005	±0.002
	θ	45°		45°	
MP16K01A	A	4.08	+0.12, -0.13	0.161	+0.004, -0.005
	B	3.43	+0.07, -0.08	0.135	+0.002, -0.003
	C	4.08	+0.12, -0.13	0.161	+0.004, -0.005
	D	3.43	+0.07, -0.08	0.135	+0.002, -0.003
	E	1.35	±0.15	0.053	±0.005
	F	0.25		0.009	
	G	1.50		0.059	
	H	0.57 Square		0.022 Square	
	J	1.50		0.059	
	K	0.60		0.023	
	L	0.80		0.031	
	M	0.82		0.032	
	N	0.11	+0.07, -0.08	0.004	+0.002, -0.003
	O	2.13		0.083	
	P	0.60		0.023	
	Q	0.52		0.020	
	θ				
MSOP-10	A	4.90	±0.20	0.193	±0.008
	B	0.28	±0.15	0.011	±0.006
	C	0.50		0.0197	
	D	3.00	±0.15	0.118	±0.006
	E	3.00	±0.15	0.118	±0.006
	F	0.10	±0.05	0.004	±0.002
	G	0.86	±0.10	0.034	±0.004
	H	0.18	±0.10	0.007	±0.004
	J	0.55	±0.20	0.0215	±0.008
	θ	0° to 6°		0° to 6°	

Package Drawing	Dimension	Measurement (mm)		Measurement (inches)	
		Typical	Tolerance	Typical	Tolerance
QLCC-16ALN	A	6.35	±0.20	0.250	±0.008
	B	6.35	±0.20	0.250	±0.008
	C	1.27		0.050	
	D	Radius 0.20		Radius 0.008	
	E	1.78	±1.27	0.070	±0.005
	F	0.56	±0.05	0.022	±0.002
	G	0.64		0.025	
	H	3.04		0.120	
	J	3.04		0.120	
	K	3.81	±0.13	0.150	±0.005
	L	0.64	±0.20	0.025	±0.008
	θ				

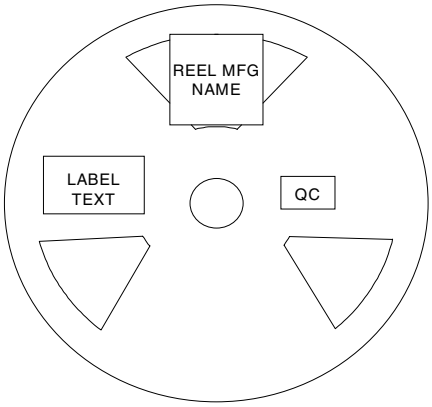
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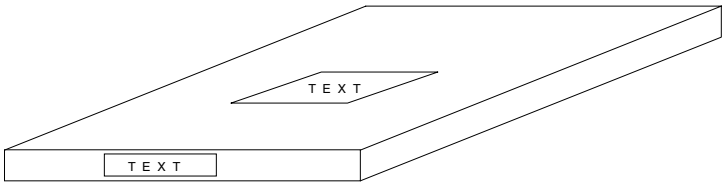
Tape and Reel Packaging

All parts will be packaged for shipment in industry-standard 13" and 7" tape-and-reel packaging compatible with automatic tape dispensing and parts handling equipment per EIA-481-2 standards. Best commercial practice shall be employed in protecting the devices from electrostatic discharge (ESD) and mechanical damage in shipment.

Marking for Reel and Delivery Box

ESD attention labels will be placed on reel and antistatic bag.





Contents of Marking Label

RF MICRO-DEVICES	
CPN: ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦	
MPN: ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦ ¦	
D/C: ¦ ¦ ¦ ¦ ¦	**QTY:** ¦ ¦ ¦ ¦ ¦
LOT: ¦ ¦ ¦ ¦ ¦	**R/D:** ¦ ¦ ¦ ¦ ¦
PO#: ¦ ¦ ¦ ¦ ¦	**TYPE:** ¦ ¦ ¦ ¦ ¦

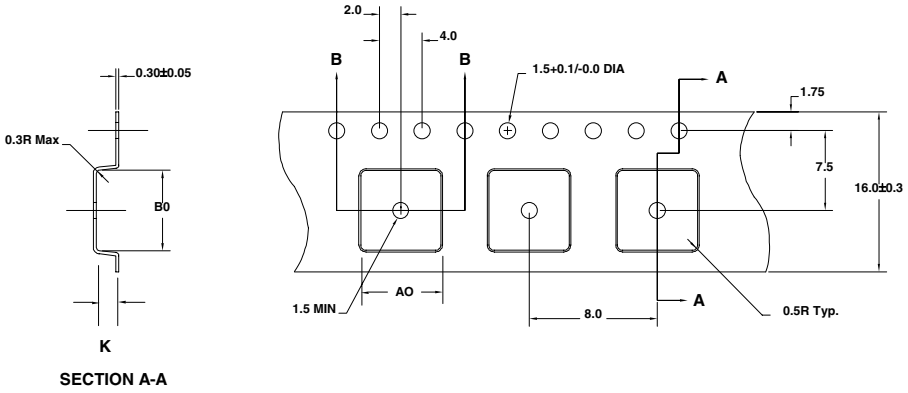
Number of Parts per Reel

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Package Type	7" Reel	13" Reel
SOP-8/14/16	750	2500
SOP-20	N/A	1000
PSOP-8	750	2500
SSOP-16/24/28	750	2500
QLCC-16	N/A	2500

Configuration of Tape

All dimensions in mm.



A0 = 6.5mm
B0 =10.3mm
K0 = 2.1mm

Dimensions

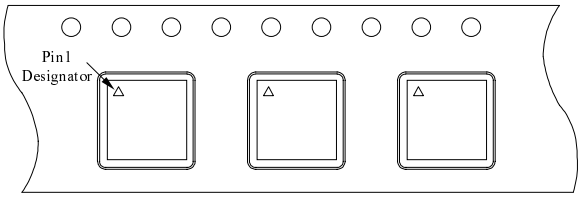
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Package Type	A0	B0	K0
MP16K01A (4x4)	4.35	4.35	1.6

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Advantek Polystyrene.
4. AO and BO measured on a plane 0.3mm above the bottom of the pocket.
5. KO measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Configuration of Parts in Tape



Leader and Trailer Specification

The leader and trailer will be minimum 15".

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The following specifications apply to all RF Micro Devices products.

Solderable Surface Finish
The following solderable surface finishes are used:

Package Style	Plating Material	Thickness
SOP-8-C	Au on Ni	Au max 1µm Ni 2-6µm
All plastic packages	SnPb (60/40) on Ni	SnPb min 6µm typ 12µm

Minimum Requirements for Shipping and Storing in Order to Preserve Reliability and Solderability
Minimum protection required: Cardboard box
Maximum shelf life with specified protection: 1 year

Expected Shipping and Storing Conditions:
Relative humidity 15% to 70%
Temperature -5°C to 40°C
Sulphur dioxide average 0.3mg/m^3
Sulphuretted hydrogen average 0.1mg/m^3

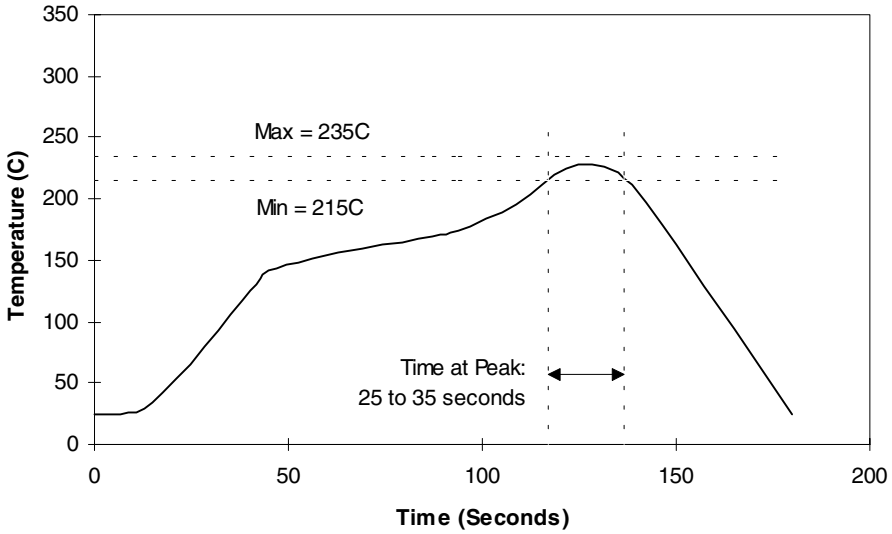
Component Coplanarity
Determination of coplanarity: solderable lead deviation from the reference plane formed by three lowest contact points when component lies on flat surface by its own weight.

Coplanarity specification: max 0.004 inches

Solderability
Test equipment: wetting balance analyzer Multicore MUST System II

Specification: wetting speed 1.0 s to 2/3 F_{max}

Recommended Reflow Soldering Profile



Maximum temperature slope: 5°C/second
Product can withstand this profile two times.

Manual Hot Gas Soldering
Maximum air temperature: 300°C
Maximum air velocity: 10m/s
Maximum exposure time: 30s

Manual Soldering Using Soldering Iron
Tip Diameter: Selected to fit application
Maximum tip temperature: 370°C
Antistatic protection: Required
Maximum exposure time: 3s

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Special Handling Information for Power Small Outline Package (PSOP) and Power Shrunk Small Outline Package (PSSOP) Products

RF Micro Devices is pleased to introduce a new high volume low cost packaging technology for our GaAs HBT power amplifiers. These packages are considered ***JEDEC level 5 for moisture sensitivity*** and require special handling to assure reliable performance.

The Power Small Outline Package (PSOP) and Power Shrunk Small Outline Package (PSSOP) packages are beginning to see common usage within the industry and offer significant advantages for power amplifier applications. The exposed copper slug on the bottom of the package improves both thermal and electrical performance. Since the RFIC is mounted directly on the thermal slug, and the slug is soldered directly to the PCB, the thermal resistance to the PCB is minimized. Also, the RF ground for the power amplifier is established through this copper slug as it is soldered to the ground plane on the PCB. This offers the least inductance ground path available.

Care must be taken when soldering these packages to the PCB. They are currently considered JEDEC Level 5 for moisture sensitivity. Therefore the parts must be handled in a dry environment prior to soldering, as is specified in the JEDEC Specification. Specifically, RFMD recommends the following procedure prior to assembly:

1. Dry-bake the parts at 125°C for 24 hours, minimum. Note: the shipping tubes can not withstand 125°C baking temperature.
2. Parts delivered on Tape and Reel are already dry baked and dry packed. These can be stored up to one year, but must be assembled within 48 hours within opening the bag.
3. Assemble the dry-baked parts within 2 (two) days of removal from the oven.
4. During this 2-day period, the parts must be stored in humidity less than 60%.

IMPORTANT! If the 2-day period is exceeded, then this procedure must be repeated prior to assembly.

If there are any questions or concerns, please feel free to contact us at RF Micro Devices. We look forward to supporting your power amplifier requirements.

For more information about the JEDEC standard, please refer to: http://www.eia.org/jedec/download/std020.pdf

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