

RFIC Components for Cordless Phones

Introduction

The commercial market for RF Integrated Circuits (RFICs) is expanding rapidly. Many commercial applications are appearing which need small, efficient components which provide higher levels of integration. Some examples include Point-of-Sale (POS) Terminals, cordless and cellular telephones, wireless meter reading equipment, wireless security systems, and many others. This increased integration level provides very low component counts on the PC board, and reduces the burden placed on the system manufacturer, ultimately allowing much lower system cost. This progression is analogous to that seen with digital circuits and micro-processors, whereby increasing levels of technology was placed upon the IC, and taken off the circuit board.

One application which requires high-volume, low-cost RFICs is the digital cordless telephone. Several 900 MHz phones have appeared on the market recently, requiring a low-cost RF section. Some of these RF sections are all discrete, others use a number of individual ICs, while still others use highly integrated ICs. Also, some of the entries utilize channel frequency hopping, others use direct-sequence spread-spectrum (DS-SS), and others use a combination of DS-SS and frequency hopping. A highly integrated RF chipset for a 915 MHz spread-spectrum cordless phone has been developed and will be described. The specific chipset as described here was developed under contract, and as such it is not generally available for sale. It does, however, demonstrate capability and the functionality presented here is available through RFMD standard components.

RF Chipset Requirements

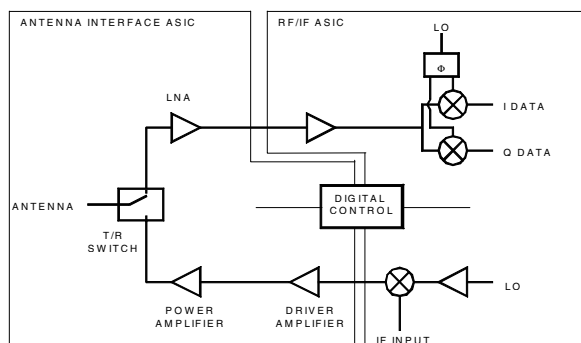


Figure 1. Block diagram of the RF section

The RF section such as that shown in Fig. 1 performs

the following functions:

- Modulates the baseband spread-spectrum encoded data signals directly onto an RF carrier at 915 MHz,
- Amplifies the modulated signal with a power amplifier to 100 mW for transmission,
- Provides for switching between transmit and receive paths, using a T/R switch with digital control,
- Receives the incoming signal and amplifies with a low-noise amplifier,
- Demodulates the signal directly to baseband In-phase and Quadrature-phase components.

The chipset consists of two chips; an Antenna Interface ASIC and a RF/IF ASIC, as shown in Fig. 2 and 3. RF Micro Devices, Inc. utilized **Optimum Technology Matching™**, choosing high-performance GaAs MESFET technology for the Antenna Interface ASIC, and low-cost Silicon bipolar technology for the RF/IF ASIC. This partitioning of technologies allows the optimum price/performance trade-off.

Antenna Interface ASIC

The Antenna Interface ASIC is a GaAs MESFET circuit, including a T/R switch, high-gain power amplifier, and a low-noise amplifier. The chip, supplied in a plastic SOIC-16 package, operates from a single 5V power supply. The overall specifications for the circuit require gain of 23 dB in transmit mode with 100 mW transmitted power, and 13 dB gain with less than 3 dB noise figure in receive mode. The T/R switch is controlled by digital translators, so a standard CMOS or TTL level input can be applied to control transmit or receive. Power down features are incorporated on all circuits and are tied to the T/R control.

The power amplifier is a self-biased, 3-stage GaAs MESFET design, with a total gate width on the final stage of 1.2mm. The final stage is biased slightly Class-AB, and consists of depletion-mode FETs with pinch-off voltage of $\sim 0.9V$. Total current consumption in transmit mode is ~ 60 mA. Enhancement-mode FETs are used for part of the driver amplifiers as well as in the power down circuitry. The EFETs allow the amplifier to be shut off completely when not in use, using only the positive voltages available from the translators. The entire amplifier operates from a single 5V

supply, with no need for an external negative voltage.

The LNA is a 12 dB gain block with ~2 dB noise figure. The input and output are matched to 50Ω; the output interfaces directly to the RF IN port on the RF/IF ASIC.

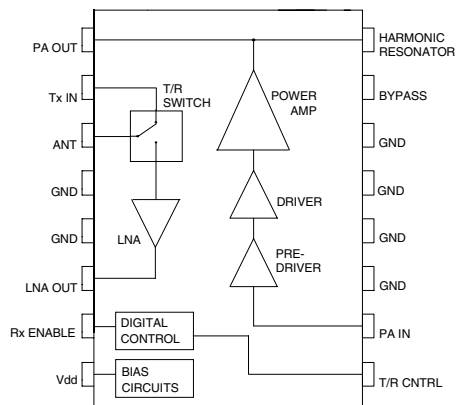


Figure 2. Antenna Interface ASIC.

RF/IF ASIC

The RF/IF ASIC is a Silicon bipolar circuit, and includes a bi-phase modulator for transmit, and a quadrature demodulator for receive. The LO input power is -10 dBm, which is amplified by the LO buffers to 0 dBm, and is distributed to both the up- and down-converter. Direct bi-phase modulation and direct quadrature demodulation is used, so a single external synthesizer is all that is required for the transceiver function. The 90° phase shifter for the quadrature demodulator is included on-chip to simplify the interface requirements.

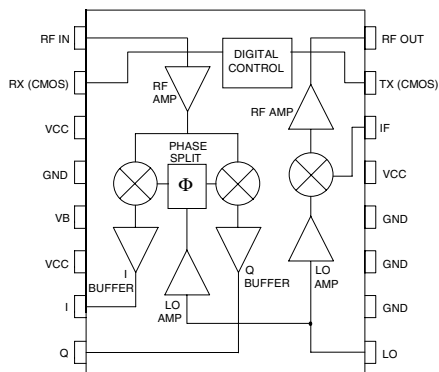


Figure 3. RF/IF ASIC.

The bi-phase modulator accepts inputs from 0 to >3 MHz with up to 0.5V_{p-p}. Carrier suppression is >25 dBc for the maximum input level. Maximum output from the chip is -10 to -15 dBm. This provides an easily achievable level from the bipolar process, placing the

majority of the gain and power output onto the GaAs circuit, where gain/stage and power are much higher.

The quadrature demodulator operates directly at 915 MHz. Input signals can range from 900-930 MHz, and the I/Q output bandwidth is 0 to 3 MHz minimum. Amplitude and phase balance specs are <1 dB and ±5°, respectively. I/Q output level can be as high as 1.4V_{p-p} at 1dB gain compression.

This chip also operates from a single 5V power supply and is supplied in an SOIC-16 package.

Summary

A highly integrated 2 chip set has been designed for cordless phones operating in the 915 MHz ISM-band using direct-sequence spread-spectrum modulation. This chipset allows the phone to be produced with much lower manufacturing costs and greater reliability than do the discrete components.

This paper was originally presented during the 1994 Wireless Symposium, Santa Clara, California.