An FSK Transmit and Receive Chip Set

The RF9901 and RF9902 are low cost monolithic integrated circuits which can be used separately or together as a two-chip set that provides all the functions necessary to implement a binary FSK transceiver for such applications as 915MHz ISM-band handheld terminals for POS meter reading, bar-coding reading, as well as other digital applications such as SMR.

The parts are provided in 16-lead plastic SOIC packaging, operate from a 3V to 5V supply with no negative voltage required and cover the 400MHz to 950MHz frequency range. They are implemented using a low cost silicon bipolar process which features NPN transistors with an f_t of 5GHz, PNP transistors with an f_t of 1GHz, thin film resistors, Schottky diodes and capacitors.

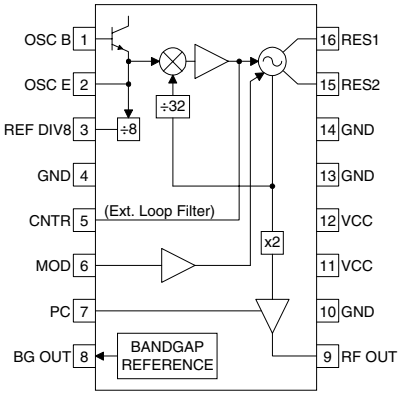

Figure 1. RF9901 Functional Block Diagram

THE RF9901 TRANSMITTER

The RF9901 operates as an FSK transmitter with all the functions required to form a fully integrated PLL system. A functional block diagram of the device is shown in Figure 1 and a typical application circuit for operation at 916MHz is shown in Figure 2. The PLL section consists of an integrated phase-frequency detector, VCO, divide-by-32 prescaler and reference frequency oscillator amplifier. The VCO runs at one half of the output frequency, f_o, since a doubler circuit is used after the VCO to provide the output signal.

Bandgap Reference

The bandgap reference voltage is used internally for biasing to achieve constant performance over varying temperature and power supply voltages. On-chip circuitry provides a bandgap voltage of 1.15V. The bandgap is brought out through a pin and can be used as an external reference for circuitry that has less than 1mA current draw and can provide a constant load. A series resistor should be used to prevent any oscillations in the case of a long lead being connected to this pin.

Crystal Reference Oscillator

The crystal reference oscillator is a common emitter Colpitts design which uses a parallel resonant crystal operating in the fundamental mode. The crystal is calibrated with a 50pF load. The values of the external

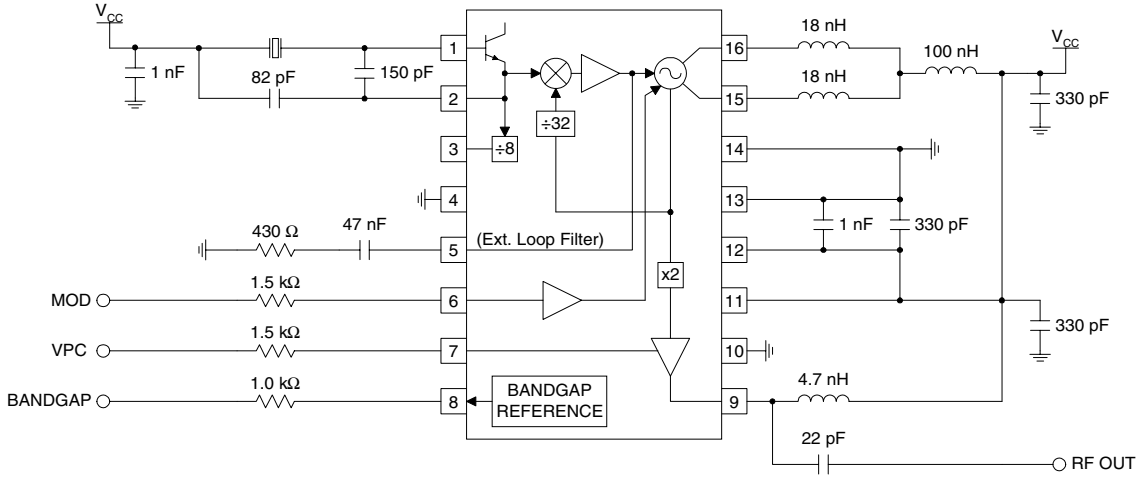

Figure 2. RF9901 916MHz Application Schematic

feedback capacitors can be adjusted for optimal performance at different frequencies. The crystal can be replaced by an external source. The signal should be AC coupled using a capacitor and the level should be about 500mV_{p-p}.

VCO and Output Amplifier

The VCO design is based on a balanced configuration which utilizes cross-coupling between the bases and collectors of a transistor pair. The tank resonator circuits are formed by a pair of external inductors and on-chip varactor diodes which are driven by the phase/frequency detector to form part of the PLL.

A balanced configuration was used instead of a single ended design since it can provide differential drive to the prescaler section and has better rejection of unwanted modulation signals although it does require two tuning elements instead of one. The VCO resonators must have a DC path to VCC on these pins. The value of the inductors required for an f_o=916MHz is 18nH with the values required for other frequencies being approximated by the following empirically derived formula

$$L = \frac{12.6 \cdot 10^6}{f^2}$$

where L is the inductor value in nH and f is the frequency in MHz.

The transmitter uses a VCO/doubler approach for f_o although a fundamental VCO was the first consideration for the original design. The trade-off between the two approaches were that the doubler design has a higher output level, better noise characteristics and greater temperature stability than the fundamental design while the main advantage in the fundamental design is that the f_o/2 harmonic level is much lower. The f_o/2 level in the doubler design is only 25dB below the fundamental.

Typical harmonic levels for an fo = 916MHz at 0dBm into a 50Ω load with V_{CC}=4V and the power control voltage on pin 7, V_{PC}=2.5V, are as follows:

Harmonic	Level Below Fundamental (dBc)
2fo	20
3fo	min 30
fo/2	25
Reference Frequency	min 55

The typical current draw at V_{CC}=4V, V_{PC}=2.5V is 26mA. The power control pin when set to 0V disables the output amplifier and the device draws about 20mA so it does not function as a complete power down control. At positive voltages above 1V the output amplifier turns on. The higher the voltage, the higher the power although a series resistor of 1.5kΩ should be placed on pin 7 if V_{PC} is taken directly from V_{CC}.

The amplifier output must have a DC connection to V_{CC} through an RF choke. The RF choke can be part of the matching network. An extra one or two components at the most can be added to the output network to reduce the f_o/2 level since the network is a high pass structure.

PLL Parameters and Frequency Modulation

The fixed divide by 32 prescaler is implemented using a master/slave flip-flop divider architecture while the phase/frequency detector essentially uses D type flip-flops and charge pumps to provide the control signal to the VCO.

The application circuit, Figure 2, indicates a series RC to ground on pin 5 for the loop filter. The values will give a lock time of less than 3ms, smaller capacitor values will increase the loop bandwidth and decrease the lock time. The lock time is also a function of the VCO resonator setting since the fastest lock time results when the VCO resonator is set to resonate at just above f_o with the loop control voltage set at V_{CC}/2. The VCO sensitivity is about 25MHz/V and the phase detector sensitivity is about 0.4μA/degree.

The modulation input is designed to be driven by a logic level, 0V or V_{CC}. The maximum modulation frequency is 500kHz and a series resistor can be used to reduce the frequency deviation. The modulation is applied to an internal varactor in the VCO, therefore the PLL will correct the frequency offsets caused by the modulation unless the loop bandwidth is narrow enough.

THE RF9902 RECEIVER

This part contains the input amplifier, mixer, IF limiting amplifier, phase detector, and an output Schmitt trigger to generate the FSK digital signal as shown in Figure 3. There are two sections to the chip; one section performs the downconversion from the RF to IF frequency while the second amplifies and demodulates the IF signal. A typical application circuit for use at an

IF=20MHz is shown in Figure 4.

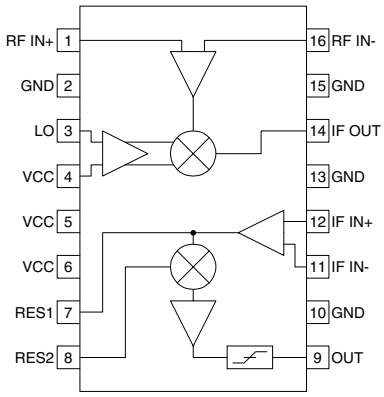

Figure 3. RF9902 Functional Block Diagram

RF Amplifier and Mixer

A differential RF amplifier and Gilbert cell mixer form the basis of the downconversion section. The RF input requires a DC blocking capacitor and can be brought in on pin 1 or pin 16. The unused pin should be AC grounded at the package. This front-end section has typically 18dB of gain and a noise figure of around 7dB. The 1dB input compression point is -22dBm and the input IP3 is -10dBm. The RF input VSWR is less than 1.5:1 across the operating frequency. The IF output impedance is 500Ω and the pin has to be loaded with a coupling capacitor or a filter with a high DC resistance.

IF Section

This section has an IF amplifier, limiting amplifier, FM demodulation circuitry, and a Schmitt trigger. The IF signal from the mixer is filtered externally and amplified to provide the required drive level to the limiter. The differential IF amplifiers have about 90dB of gain. The function of the limiter is to remove amplitude variations from the IF frequency since the FM detection circuitry will attempt to demodulate any amplitude variations in addition to the required frequency variations. This would decrease sensitivity and increase the distortion in data signal output.

The IF input impedance is 500Ω and pin 11 is the complementary input. Pin 11 should be bypassed to ground with a capacitor as close to the package as possible. There should be no DC path between the mixer output and IF input.

FM Demodulation

The FM demodulation is accomplished by a quadrature detector consisting of an analog multiplier and an external quadrature tank circuit. The multiplier can be easily implemented on chip and discrete components can be used for the quadrature tank.

The limiter signal is split into two and applied differentially to the lower transistors in the multiplier and also to the upper transistors via the external phase shift capacitor as shown in Figure 4. The two signals are at the same frequency but have a 90° phase difference at the carrier frequency and the multiplier acts as the phase detector.

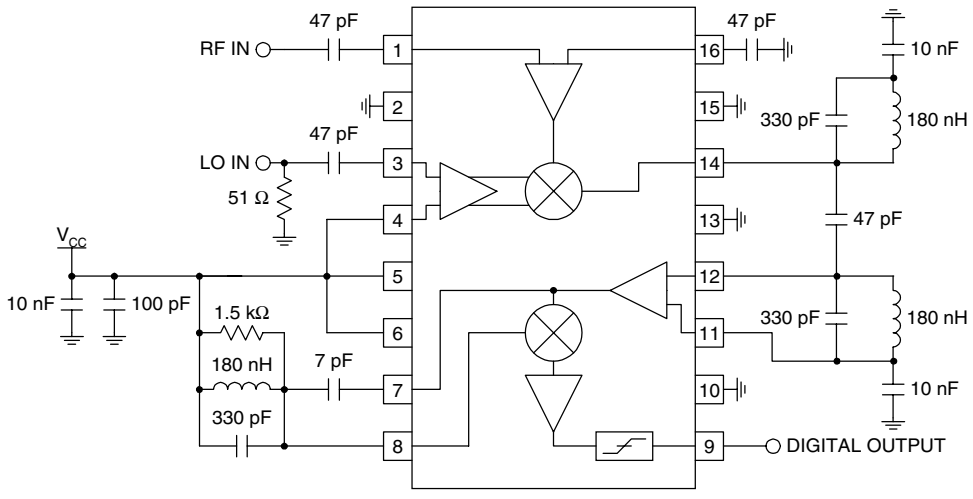

Figure 4. RF9902 Application Schematic

The external quadrature tank circuit should have a connection to V_{CC} for internal biasing purposes. The tank circuit provides the 90° phase shift at the carrier frequency and a linear phase shift on either side of the carrier. It is the relative phase shift versus frequency which determines the modulation state of the signal. The Q of the tank circuit should be such that the 3dB bandwidth is approximately equal to the modulated frequency shift of the carrier. Wider bandwidths are possible provided that the peak-to-peak phase shift is at least 45°. High Q components should be used since the shunt resistor can always be adjusted to lower the Q.

The digital output indicates the modulation state of the carrier input. It is a logic signal which when low is equal to 0V and when high is equal to V_{CC} indicating positive modulation. The Schmitt trigger helps in restoring the shape of the demodulated digital output.

The RF9902 draws 25mA at a V_{CC}=4V and has an RF sensitivity of at least -80dBm for an IF=30MHz. Higher IF frequencies may lead to a degradation in sensitivity. An external LNA, or gain block such as the RF2304, with at least 10dB of gain and an image noise filter between the LNA and RF9902 input should be used for maximum sensitivity applications.

Circuit Board Layout for the RF9901 and RF9902

The ground pins should be connected directly to the PCB ground plane as close to the package as possible. The V_{CC} pins should be bypassed to ground directly at the package and any decoupling capacitors on the board should have a direct return to ground.

The RF9902 receiver requires some extra care in the board layout to achieve sensitivity and maximize stability. The VCC must be bypassed with quality RF capacitors and the circuitry around the IF output and inputs must be bypassed close to the package. The PCB board must have a good double sided ground plane which runs directly under the part on both sides. This isolates one side of the part from the other. Although the functionality of pins 1 and 16 can be interchanged, it is recommended that pin 1 is used for the input signal. This will minimize any potential coupling between the RF and IF sections.