A Highly Integrated Receiver IC for Spread Spectrum Applications

Introduction

An integrated receiver has been developed which includes most of the circuitry needed for reception of a digitally modulated signal. The device is manufactured using a low-cost high-performance Silicon Bipolar process, and contains a RF front-end, IF amplifier with gain control and Received Signal Strength Indicator (RSSI), and a quadrature demodulator. The circuit can be used for 915MHz ISM band systems, or as a dual IF section in higher frequency and super-heterodyne systems. Since the intended applications are usually under size and cost pressure, the device is packaged in a small low-cost plastic SSOP-24 package.

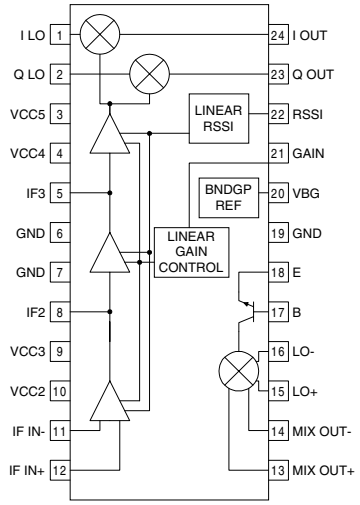

Figure 2. RF2903 Functional Block Diagram

Direct Sequence Spread Spectrum (DSSS) generally uses Phase Shift Keying (PSK) to modulate the carrier. The two most common forms are Quadrature PSK QPSK and biphase PSK (BPSK). BPSK modulates one bit at a time on the carrier, by setting the carrier phase to either 0 or to 180 degrees. QPSK modulates two bits at a time, one bit on the In-phase (I) channel, and the other bit on the Quadrature (Q) channel. This results in phase modulation in 90 degrees increments. Though the modulator for BPSK is simpler than for QPSK, the receiver needs to have a quadrature demodulator in both cases to resolve frequency offset and channel distortion between the transmitter and receiver. Amplifiers in those systems need to be linear to handle interfering signals without deteriorating the system performance (measured by the Bit Error Rate).

Because of the flexibility chosen in the chip architecture the device can also be used as a FM or ASK receiver.

Architecture

A block diagram for a basic Spread Spectrum receiver is shown in Figure 3. The RF2903 contains the RF front-end with RF Amplifier and Downconverter, three IF amplifier stages with linear gain control and RSSI, and a quadrature demodulator. Each of those functions will be described in more detail below. Components that are not included on-chip are the filters, the Local Oscillators, and the Base Band processing. The Gain Control is set by the Base Band Processor to such a level that the system is operating linearly, and no jamming by interferers can occur. The RSSI output of the RF2903 can be used as a "signal present" indicator, or as a coarse input for the gain control loop. In case there is no in-band interference expected the gain control may be fixed at the maximum level.

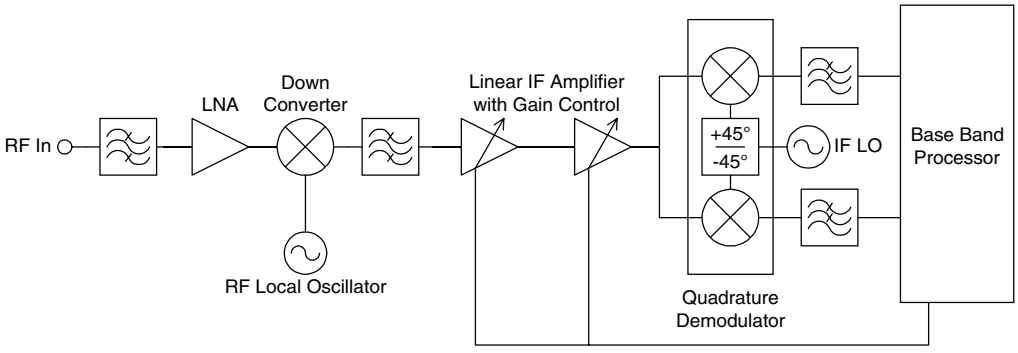

Figure 3. Typical Direct Sequence Spread Spectrum Receiver Architecture

Front End With RF Amplifier And Downconverter

The RF Amplifier and mixer are implemented as a differential amplifier with the RF signal modulating the current source in the common leg, see Figure 4. The current source also serves as the LNA. One of the differential inputs is normally terminated or connected to V_{CC} when a single ended input signal is used. The current through the current source is set by the base voltage that is externally provided (usually using the internal bandgap reference) and the value of the emitter resistor. The typical current in the current source is 5mA.

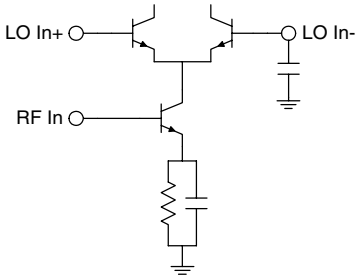

Figure 4. The Front End Circuit

RF2903 Pre-Amp/Mixer Power Gain vs. Frequency (Load=1k)

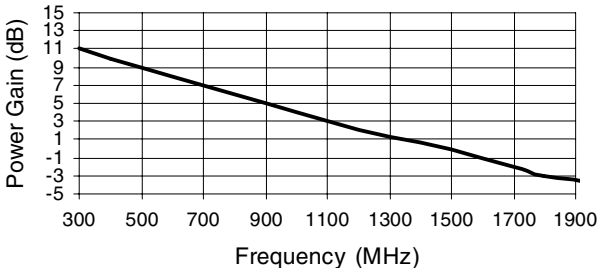

Figure 5. Front-End Gain

To obtain maximum flexibility in the system design the front-end can be configured in different ways. In case the RF input is directly at the RF2903 the LNA/Mixer should be configured for maximum gain and lowest noise figure. This is achieved by a common emitter configuration as shown in Figure 7. To increase system sensitivity one may choose to use an external LNA, and improve the overall noise figure. In this case, it is more important to obtain a high IP_3 in the LNA/Mixer. The common base configuration of Figure 6 achieves this, with the IP_3 being about 10dB higher than in the common emitter configuration but with higher noise figure and lower gain.

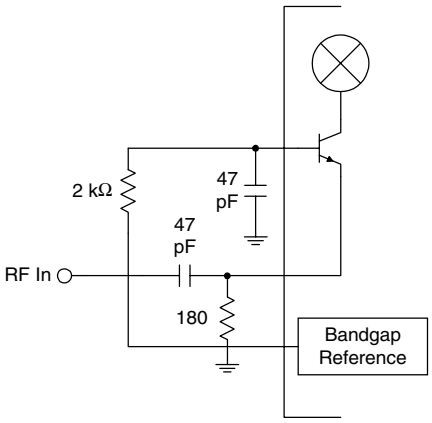

Figure 6. LNA in Common Base Configuration

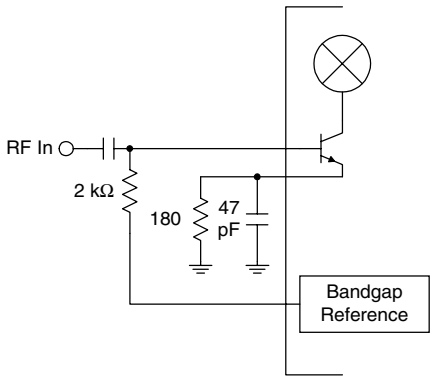

Figure 7. LNA in Common Emitter Configuration

IF Amplifier With Linear Gain Control And RSSI

The IF section consists of three identical gain stages, each with gain control and a Received Signal Strength Indicator (RSSI) detector. One of the goals in the IF section design was a linear gain control (measured in dB/V). This was achieved by putting gain control in all stages, being controlled by a segmentation amplifier. When the RF2903 is used in a linear system, for example a Direct Sequence Spread Spectrum receiver, the gain control will be used to keep the signal levels throughout the system such that no clipping occurs, even when a strong in-band interfering signal is present. When this device is used in a system where no linearity is required, for example a FM or Frequency Hopping receiver, the gain can be set to the maximum value at all times. The RSSI is than an indicator for the received signal strength.

To avoid amplification of DC offsets throughout the device, the output each of each stage is normalized at

VCC through an external inductor to VCC. With this approach the external LC resonator also serves as a bandwidth limiting filter, to avoid that the amplifier gets saturated by wide band noise in the high gain region.

Amplifier Stages

Each of the IF stages is made up of two differential pairs put in parallel, see Figure 8. One differential pair has high gain, while the other has low gain because of the emitter resistors. The gain control of each stage is achieved by gradually turning on one pair, while the other pair is gradually turned off. The actual gain of each stage is depending on the Q factor of the external resonator. A lower Q results in a lower equivalent parallel resistor, and hence in lower gain. The output of each stage is internally connected to the input of the next stage, and one pin is used for the power supply and bandwidth limiting for each stage.

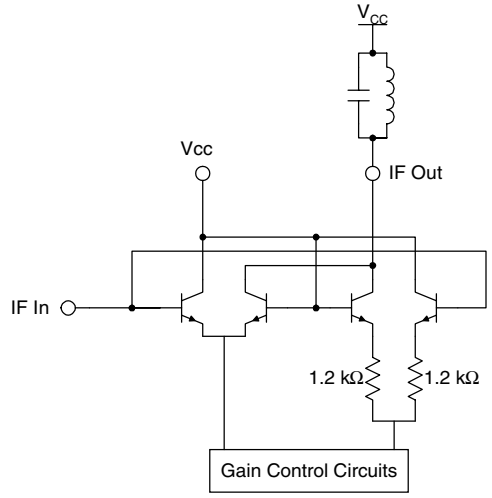

Figure 8. A single IF Amplifier Stage

The first and last stage have slightly different interconnections. The first stage has a balanced input, hence the complementary input is not connected to VCC as shown, but has a separate pin instead. The output stage has a balanced output, which goes through a buffer amplifier to the mixers.

The maximum gain in each amplifier stage is about 23dB, with an additional 25dB in the buffer amplifier and demodulator.

Gain Control

The gain control is achieved by turning on one pair, while turning off the other pair of the IF amplifier stage described above. Because the outputs of the pairs are open collectors, hence current sources, current adding occurs at the output. This means that the gain control can be done by putting more current into one pair while reducing the current in the other pair. Another differential amplifier as shown in Figure 9 is used for controlling the current into each differential pair. There are three of those amplifiers, one for each stage. The VBG' voltage determines at which control voltage that stage comes into action. In this way sequencing of the gain stages is achieved to optimize the dynamic range of the IF section. When the voltage is slowly increased, the first stage is turned on first, then the second stage, and as last the third stage. Because there are no capacitors besides parasitics in the circuit, the response time is very fast. The gain can be changed over the full range within 100ns, while no ringing or overshoot occurs.

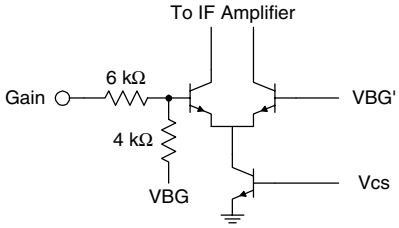

Figure 9. The Gain Control Circuits

VCS is derived from the bandgap voltage to set the current into each amplifier. The bandgap reference is used to obtain maximum temperature stability and minimize the effects of manufacturing process variations.

RSSI

The RSSI signal is obtained by rectifying the signal at the output of each stage, then summing those signals. Because the signal level is measured at the output of each stage, the RSSI vs. input power response changes when the gain control voltage is changed. This needs to be taken into account when designing a feedback loop that uses the RSSI signal to set the gain control voltage to maintain a constant output signal. The RSSI output is an open-collector PNP transistor, and an external resistor of 3kΩ is recommended. A capacitor to suppress IF signal should also be connected to the RSSI output and determines the actual response bandwidth, which potentially can be as high as the IF frequency itself.

Quadrature Demodulator

The quadrature demodulator consists of two Gilbert Cell mixers which are both driven differentially by the IF amplifier output, see Figure 11. The LO signals to the mixers need to be provided externally and should be 90 degrees out of phase. A phase splitter for this purpose is shown in Figure 12. This circuit achieves an accurate 90 degrees phase difference over a wide fre-

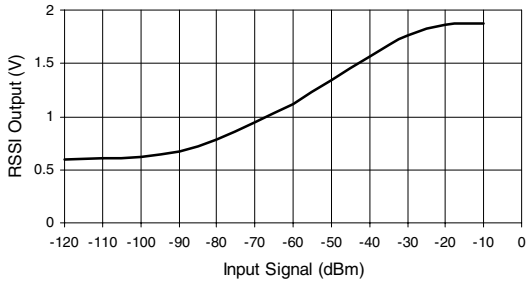

Figure 10. RSSI Characteristic at Maximum Gain

quency range, but introduces also an amplitude difference. This is no problem, however, because the LO inputs drive the mixers into saturation, taking out any amplitude difference between the I and Q LO signals. The only requirement is that the RC networks are matched to obtain an accurate phase shifting. The LO inputs are connected directly to the base of the input transistor, hence an external pull-up resistor is needed. The complementary LO inputs of the Gilbert Cells are internally connected to V_{CC}, hence the external DC voltage should be very close to V_{CC}. A 470Ω resistor to V_{CC} is small enough to achieve this, because the current into the inputs is very low.

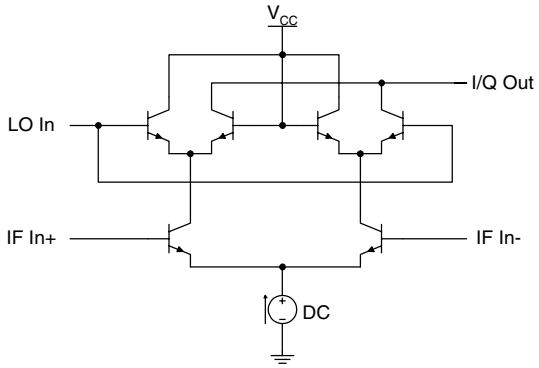

Figure 11. A Simplified Gilbert Cell Mixer

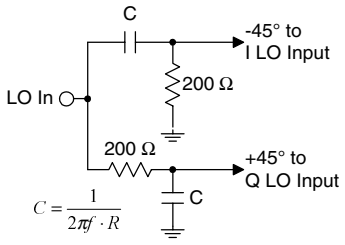

Figure 12. The Phase Splitter Circuit

The outputs of the Gilbert Cell mixers are buffered by an emitter follower such that the device can drive low impedance base band filters directly.

An on-chip bandgap reference is used for biasing all circuits. By doing this the performance of the chip is not sensitive for temperature and power supply voltage variations, and very consistent performance is achieved over the 2.7V to 5.5V range. The bandgap voltage is made available externally through a pin, and can be used for biasing the front-end as shown in Figure 6 and Figure 7, or for any other circuit in the system. The bandgap voltage is 1.63V and capable of driving up to 1mA.

Using The Device

Because of the high flexibility in the use of the device, many different circuits can be built using this chip. We will describe the three main configurations: the standard quadrature demodulator, an FM demodulator, and a configuration where the demodulator is bypassed.

Basic Application Schematic

The schematic for using the RF2903 with a quadrature demodulator is shown in Figure 15. The resonators are tuned for 50MHz, but may be scaled for any frequency up to 200MHz. Note that the biasing of the first amplifier stage is done through a resistor rather than through a resonator. A resistor can be used here because the bias is only for the base of the input transistor, it is not feeding the collector of an output. Hence the current is only a fraction of a milli-amp, and the voltage drop across the resistor is insignificant. The advantage of using an resistor instead of a resonator is to avoid inductive coupling between the stages, which could result in instability at higher gain settings.

Also worth mentioning is the choice of the mixer output and IF input pin. A single ended filter is used, thus the balanced mixer output and balanced IF section input can not be used. Only one output and one input is used, while the other is terminated. Pin 14 is used as the mixer output, and pin 11 as the IF input. It is also possible to use pin 13 and pin 12, but because the leads of those two pins run parallel inside the package a strong coupling exists between those pins. Since a filter is inserted between the mixer output and the IF input, it is crucial not to degrade the isolation. Measured isolation between pin 12 and 13 is 40dB, and between pin 11 and 14 better than 60dB. When high isolation is required it is recommended to use pin 11 and 14, rather than pin 12 and 13. The overall gain of this circuit is shown in Figure 14. The sensitivity in Figure 13 is measured with a signal bandwidth of 1MHz, based on a 0dB signal-to-noise ratio. This means that

if an actual system would have a signal bandwidth of 100kHz, the sensitivity would be 10dB better, while if a detection margin of 20dB is needed, the sensitivity would be 20dB less.

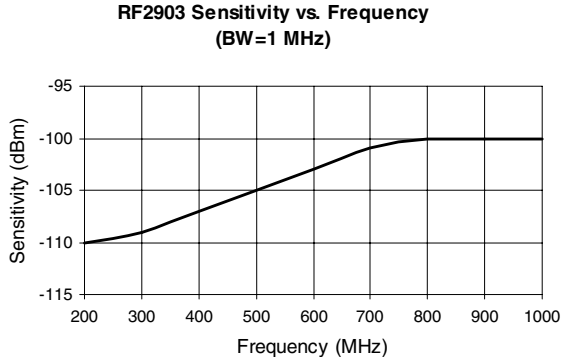

Figure 13. Receiver Sensitivity vs. Frequency

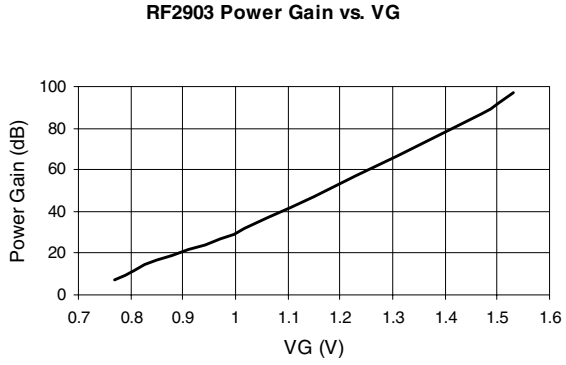

Figure 14. Overall Gain vs. Gain Control Voltage

FM Demodulation Circuit

The RF2903 can also be used as an FM or FSK receiver. The schematic for this configuration is mostly the same as shown before in Figure 15, but with a few changes in the configuration of the demodulator, see Figure 15.

The gain control can be set to maximum since no linearity in the IF section is needed. The I mixer is configured as straight-through by applying a DC signal to its LO input. This means that the IF signal from the IF section is multiplied by a DC signal (hence amplified), and the IF signal is available at the mixer output, see Figure 11. The IF signal is then phase shifted through an FM discriminator and applied to the Q mixer. Here the phase shifted IF signal is mixed with the IF signal, giving a DC output signal which is proportional to the phase difference between the two. Since the phase shifting in the quadrature tank is proportional with the frequency offset from the tank's center frequency, the demodulated output signal is a function of the instantaneous IF frequency.

Direct-Through Configuration

When no demodulation is needed at all, the mixers can be configured as regular amplifiers by applying a DC voltage to the LO inputs. When the DC voltage at the LO input in Figure 11 is less than V_{CC}, only one half of the differential pairs will be active and hence the IF signal is amplified and available at the I/Q output. The implementation of this circuit is shown in Figure 17.

When used in this configuration all the gain is accomplished at the IF frequency. Especially when the maximum possible gain of over 90dB is needed, attention needs to be paid to the layout and shielding of the circuit to avoid oscillations.

Board Layout

When designing a board layout for this device, some of

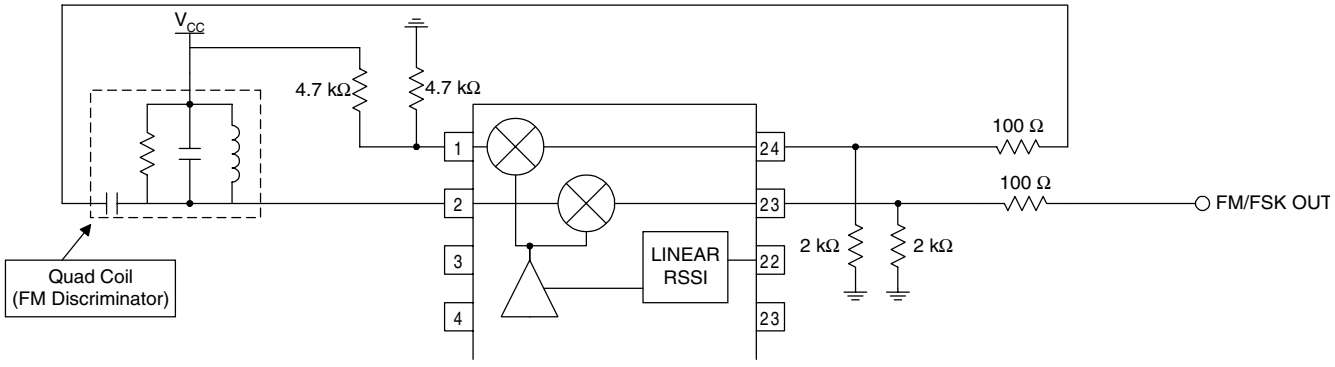

Figure 16. Detector Circuit for a FM or FSK Receiver

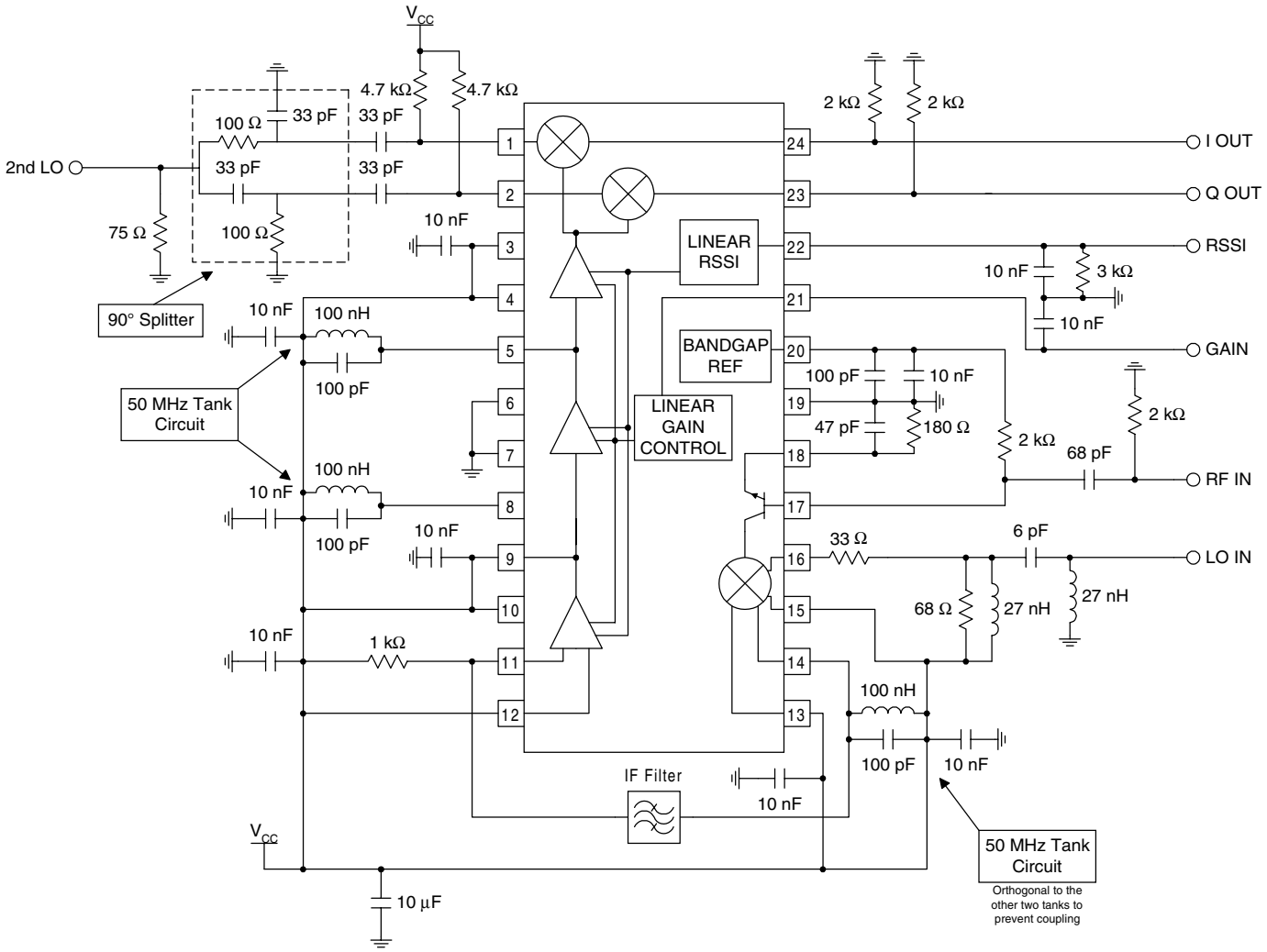

Figure 15. Basic Application Schematic for Quadrature Demodulation

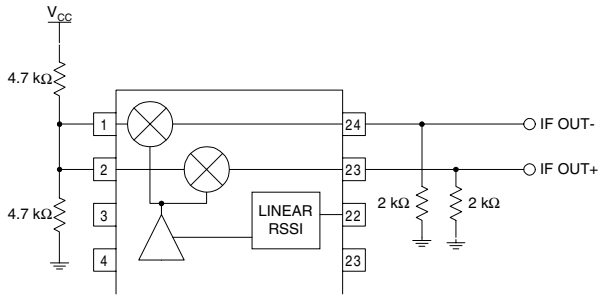

Figure 17. Used With IF Direct Through

the external circuits need special attention. To obtain maximum stability it is important that there is minimal feedback from the (interstage) outputs to the input. To achieve this the resonator tank circuits need to be orthogonal to minimize inductive coupling. Also, the spacing between the tanks should be as large as layout restrictions permit. The decoupling on the power supply pins should be done with a capacitor that has a series resonance frequency close to the IF frequency, and the capacitors should be mounted as close to the pins as physically possible.

When isolation between the mixer output and IF input is critical for e.g. image and spurious suppression, a slot in the ground plane of the PCB helps to minimize coupling due to ground currents. The slot should be at least 1mm wide and run lengthwise under the RF2903 such that the ground currents in the mixer circuit and the IF input pins are isolated. A proposed layout for the circuit is shown in Figure 18

Frequency Tuning

The device can be used over an IF frequency range of less than 100kHz to 200MHz. The low end of the fre-

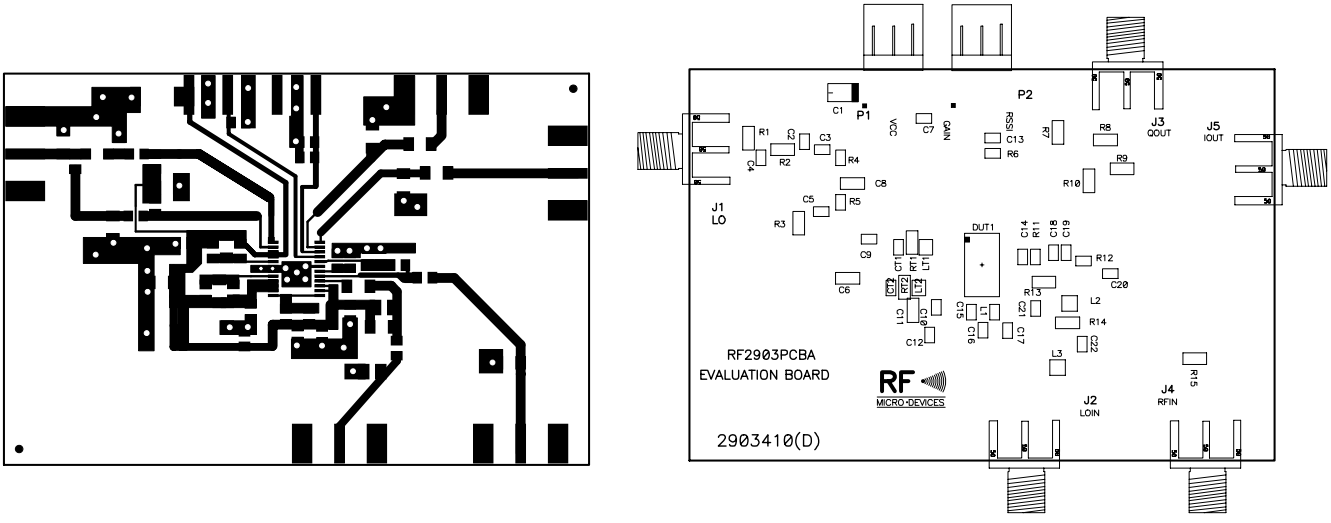

Figure 18. Layout of the Test Board

quency range is limited by the practicability of inductors for the tank circuits, while the high frequency limit is set by gain roll-off and increasing coupling on the board resulting in instability. Even though the device can operate over a wide frequency range, it is intended for narrow bandwidth operation. The bandwidth is limited by the tank circuits, and a wider bandwidth can be obtained with lower Q resonators, at the expense of maximum gain. The wider bandwidth also results in more noise power, which eventually will saturate the amplifier at higher gains, thus limiting the usable bandwidth depending on signal-to-noise ratio requirements. On the other hand, the bandwidth of the resonators should not be too narrow to avoid reduced gain caused by different frequency responses in the stages due to component tolerances. Too narrow band resonators will also result in very high gain, causing instability. This can addressed by damping the resonators by adding a parallel resistor to the tank circuits.

Conclusion

A highly integrated, very low cost receiver chip for DSSS and FM has been demonstrated. The device operates over a wide frequency range, and from a low battery voltage. The part is designed to be used in many different systems, and the flexibility in configurations makes the part suitable for several radio designs and architectures.

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