Frequency Synthesis Using the RF2510

Introduction

Narrow band receivers utilizing crystal referenced phase locked loops (PLL) allow for cost effective transmitters, receivers, and transceivers to be constructed with receiver sensitivities in the -97dBm range for frequency shift keying (FSK) with bit error rates (BER) of 10^{-4} (-94dBm for amplitude shift keying (ASK)). This is possible because of the availability of low cost crystals, which provide the required frequency accuracy to use narrow band IF filters. These 10.7MHz ceramic filters come in bandwidths of 110kHz to 360kHz and are available (in volume) for less than 40 cents each. SAW solutions are accompanied by frequency tolerances and drift on the order of 200kHz as compared to 50kHz for a crystal available (in volume) for less than 50 cents. In applications such as the European 868MHz to 870MHz ISM band, the majority of the allocated bandwidth must be used to accommodate the SAW center frequency drift (Subband A 600kHz, Subband B 500kHz), leaving little room for modulation sidebands. Noise bandwidth for the SAW approaches is typically 800kHz. Sensitivities of the SAW solutions are in the -80dBm range due to the increased noise bandwidth as well as receiver noise figure. The PLL approach offers approximately 7dB of sensitivity improvement due to decreased noise bandwidth and 7dB due to receiver noise figure.

The RF2510 is a Frequency Synthesizer Integrated Circuit designed for use in ISM Band Transmitter Products, including the European 433.05MHz to 434.79MHz and 868MHz to 870MHz Bands, as well as the United States 902MHz to 928MHz Band. In general, the RF2510 can be used over the 300MHz to 1000MHz range. The RF2510 integrates PLL components such as a voltage controlled oscillator (VCO), prescaler, crystal oscillator (RefOsc), phase detector, charge pump, and power down circuitry. A modulation pin is also provided for FM or FSK applications using on-chip diodes. The RF2510 is available in 16 pin plastic surface mount packaging (SSOP-16). With a 9mA typical current draw at 3Volts and 10.5mA at 3.6Volts, the RF2510 is well suited for battery powered applications.

This article discusses the design and measurement of a frequency synthesizer to be used in ISM band applications. The formulas used for calculation of key parameters are presented and measurement results are shown. Particular emphasis is given to the tradeoffs between loop bandwidth and phase noise, two key parameters of any frequency synthesizer design. All measurements were performed with a spectrum analyzer, and the data presented is typical of a standard product evaluation board routinely assembled for customer sampling.

Design Features

Figure 1 shows a functional block diagram for the RF2510. The crystal oscillator topology is a modified Colpitts type which requires two external capacitors as well as the crystal to be connected to Pins 1 and 2 as shown. In addition, an external reference oscillator can be injected at Pin 1 when one is already available, eliminating the need for the Colpitts circuitry discussed above.

Pin 4 is the output of the transmitter. An output attenuator can be used to decrease sensitivity to output VSWR and a harmonic filter is used to meet the ISM band specifications.

The power down pin (Pin 7) is used to disable the onboard voltage reference. It is active low so that a DC voltage less than 1Volt powers down the RF2510. Current consumption in power down mode is less than 1microamp.

The division ratio N of the prescaler is controlled by the logic levels at Pins 9 and 10. Depending on the combination shown in Figure 1, divisors of 64, 65, 128, or 129 can be achieved.

Pins 11 through 13 are associated with the VCO. MODIN (Pin 12) is connected to the smaller tuning diodes used to FM or FSK the VCO. An external varactor circuit is connected between Pins 11 and 13 for locking the VCO to the required center frequency as well as flexibility in tuning range and/or sensitivity. The VCO inductors are connected to Pins 11 and 13 and they serve to set the center frequency as well as provide bias current to the oscillator.

The outputs of the on-chip charge pumps are connected to the loop filter pin (Pin 14). A common loop filter for low cost synthesizers is a one port three element passive filter, however higher performance two port passive or active filter topologies could also be used. The voltage on the loop filter pin tunes the varac-

tor of the VCO.

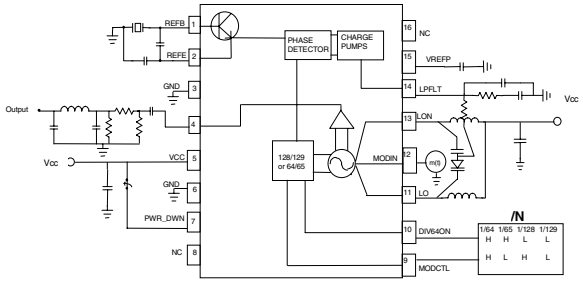
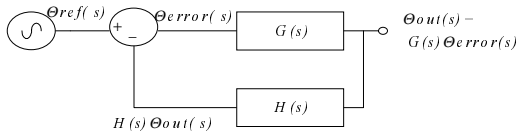


Figure 1. RF2510 Functional Block Diagram

Charge Pump PLL Design

Figure 2 shows a block diagram of a generalized PLL showing the feedforward function G(s) and feedback function H(s). The transfer functions of the PLL can be expressed in terms of these functions as shown.



$\Theta out(s) = G(s)\Theta error(s)$

$G(s)[\Theta ref(s) - H(s)\Theta out(s)]$

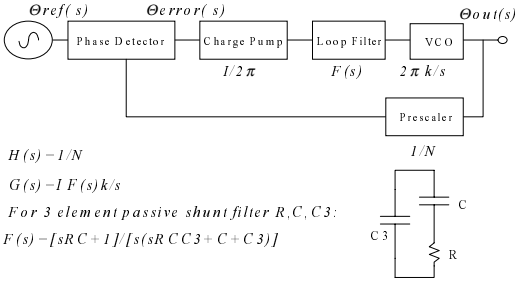
$G(s)\Theta ref(s) - G(s)H(s)\Theta out(s)$

$Acl = \Theta out(s)/\Theta ref(s) = G(s)/[1 + G(s)H(s)]$ *Closed loop gain*

$Aol = G(s)H(s)$ *Open loop gain*

Figure 2. General PLL Transfer Functions

Figure 3 shows the design of a third order type 2 charge pump based PLL. The loop filter for this design is a one port, three element passive filter. All the design equations needed for the loop design are shown in Figure 3. Phase margins of 45 degrees to 60 degrees are typically used to guarantee loop stability.



$H(s) = 1/N$

$G(s) = I\,F(s)\,k/s$

For 3 element passive shunt filter R, C, C3:

$F(s) = [sRC + 1]/[s(sRCC3 + C + C3)]$

$$Aol = G(s)H(s) = I\,F(s)\,Kv/Ns$$

$$\frac{I\,Kv(sRC + 1)}{Ns^2(sRCC3 + C + C3)}$$

Type 2 since two poles at origin. Will lock to step change in phase or frequency. Constant phase error for ramping frequency shift(acceleration)

$Acl = G(s)/[1 + G(s)H(s)]$ *Third Order C.E. in denominator*

ϕm = *phase margin, deg*
fo = loop BW, Hz
wo = loop BW, rad/sec
k = VCO tuning sensitivity, Hz/V
I = Charge pump current, Amps
N = Prescaler Divisor

$$t1 = \frac{\tan(\phi m) + \sec(\phi m)}{wo} \qquad K = \frac{kI}{N}$$

$$t2 = \frac{1}{wo^2 t1} \qquad Co = \frac{K}{wo^2}\sqrt{\frac{1 + wo^2 t1}{1 + wo^2 t2}}$$

$$C3 = t2\frac{Co}{t1} \qquad C = Co - C3 \qquad R = \frac{t1}{C}$$

$$tlock = 4/fo$$

Figure 3. Charge Pump PLL Design Equations

Figures 4 and 5 show the open loop gain and phase for a sample PLL. As can be seen, the loop BW is 5kHz and the phase margin is 60 degrees. The loop BW is defined as the frequency where the open loop transfer function reaches unity gain and the phase margin is the difference between the phase at unity gain and 180 degrees.

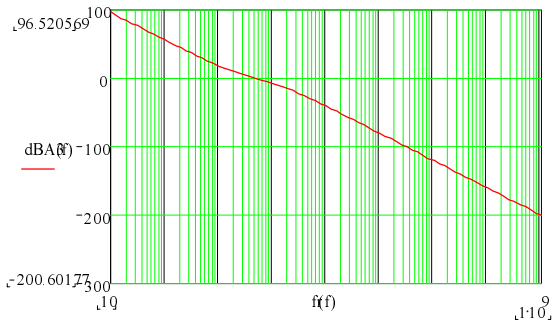


Figure 4. Open Loop Gain

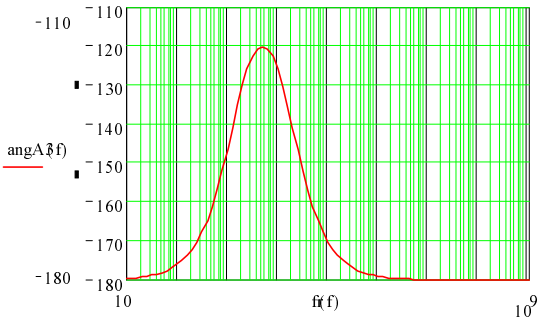


Figure 5. Open Loop Phase

Noise Analysis

Oscillator phase noise is usually characterized with Leeson's model (as shown in Equation 1). The oscillator active device has a 1/f phase noise corner frequency. This is approximately 5kHz for Silicon NPN and 5MHz for GaAs MESFET at 900MHz. When placed in a feedback loop to form an oscillator this 1/f phase noise is scaled by the circuit group delay $\tau=2Q_L/\omega_0$ into frequency noise. Since phase is the integral of frequency, the resulting frequency noise spectral density is divided by the offset frequency to convert or integrate to phase noise. The term in Equation 1 is squared because L(f) is a noise power ratio. The noise floor of the oscillator is determined by the amplifier compressed gain, noise figure, output power, and thermal noise (kT). When the 1/f model terms drop below the noise floor, Equation 1 is approximately equal to the noise floor.

$$L(f) = 10\log[((1+(fo/(2fQl))^2)(1+fc/f))10^{(G+NF+kT-Po)/10}]$$

fo = oscillator center frequency, Hz
f = offset frequency, Hz
Ql = loaded resonator Q
fc = active device 1/f corner frequency, Hz
G = compressed Gain of active device, dB
NF = noise figure of active device, dB
kT = -174 dBm Thermal noise
Po = oscillator output power, dBm

Equation 1. Leeson's Formula for Phase Noise

Figure 6 shows phase noise calculated for a reference oscillator at 7.15MHz and a VCO at 915.2MHz. The floors of the two oscillators are approximately the same, while the very large Q of the crystal oscillator results in much lower 1/f noise.

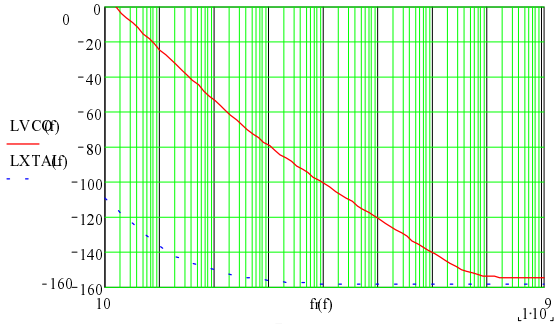


Figure 6. Oscillator Phase Noise

Figure 7 shows several PLL noise transfer functions of interest to estimate PLL phase noise. The reference oscillator and divider noise will be multiplied by the closed loop PLL transfer function. Inside the loop bandwidth, this is equivalent to adding 20logN to the phase noise of both the reference oscillator and the divider.

Outside the loop bandwidth, contributions by the reference oscillator and divider to the phase noise characteristic are attenuated due to the lowpass characteristic of the closed loop transfer function. The VCO noise is multiplied by a highpass function which is inversely proportional to the open loop gain. It is unity for offsets much greater than the loop bandwidth and rolls for offsets less than the loop bandwidth.

The third noise transfer function is that due to noise on the VCO tune line coming from the phase detector. This noise voltage will modulate the VCO and impact the overall phase noise. Since it is injected at a point between previously defined transfer functions, it can be scaled by the phase detector gain Kpd and then multiplied by the closed loop gain to get its contribution to

the output. This equation is shown in Figure 7 and Figure 8 shows the noise characteristic of the VCO, the Reference Oscillator + 20logN, the Divider noise +20logN, and a noise voltage on the tune line multiplied by the phase detector noise gain. Note that this noise voltage could arise from a number of sources, including varactors in the VCO, loop filter components, or from the phase detector/charge pump circuitry.

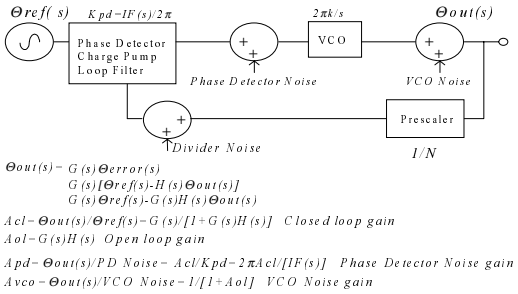


Figure 7. PLL Noise Transfer Functions

For an optimal phase noise design, loop bandwidth is normally chosen as the intersection of the VCO curve and the multiplied reference or divider curve, whichever occurs at the lower frequency. In the case of Figure 8, this would be approximately 20kHz. In other instances lock time may be of prime concern and bandwidth is set to approximately 4 divided by the locktime. Also, when direct modulation of the VCO is required, the loop BW must be set lower than the modulation frequency in order to keep the PLL from canceling the modulation. Manchester encoding can be used to keep long strings of 1's or 0's from being cancelled by the PLL, due to their low apparent frequency despite the higher data rate.

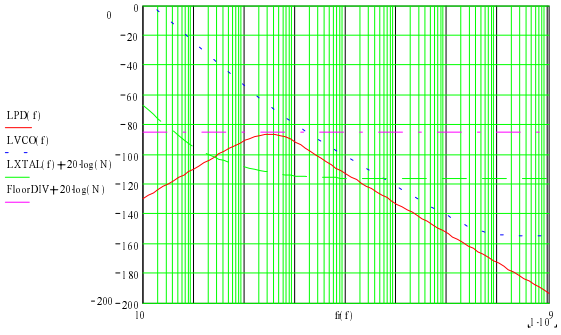


Figure 8. PLL Phase Noise Contributors for BW=5kHz

Figure 9 shows the results of multiplying the noise sources by their respective transfer functions and Figure 10a shows the composite noise curve generated by the RMS sum of the four noise curves. Note the peaking in the noise characteristic due to the loop bandwidth being set below the crossover frequency shown in Figure 8. Figure 10b shows the result if the loop BW is set to 100kHz. In this case, the result is a pedestal in the noise response caused by the divider noise.

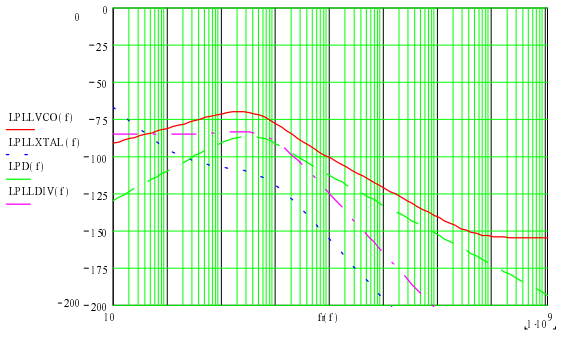


Figure 9. PLL Noise Contributors for BS=5kHz (modified by PLL)

Figure 10a. Overall PLL Phase Noise (BW=5kHz)

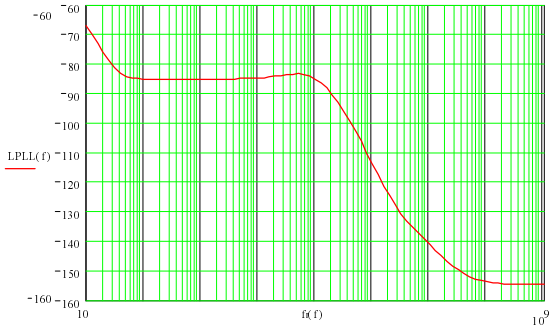


Figure 10b. Overall PLL Phase Noise (BW=100kHz)

Figure 11 shows measured PLL phase noise for bandwidths of 5kHz and 100kHz. Figure 11a indicates a phase noise at 10kHz offsets of -49-31=-80 dBc/Hz, taking into account the 1kHz resolution BW. Figure 11b indicates a phase noise of approximately -65-35=-100 dBc/Hz at 100kHz offsets. Figure 11c shows the phase noise for 100kHz BW, which has the same noise pedestal shown in Figure 10b. Figure 12 shows measured phase noise data at 10kHz and 100kHz as loop BW is varied. From this plot the optimum loop BW for phase noise can be seen to be in the 10 to 20kHz range. Due to modulation at 9600 baud, the RF2510 evaluation boards are typically configured for 5kHz loop BW.

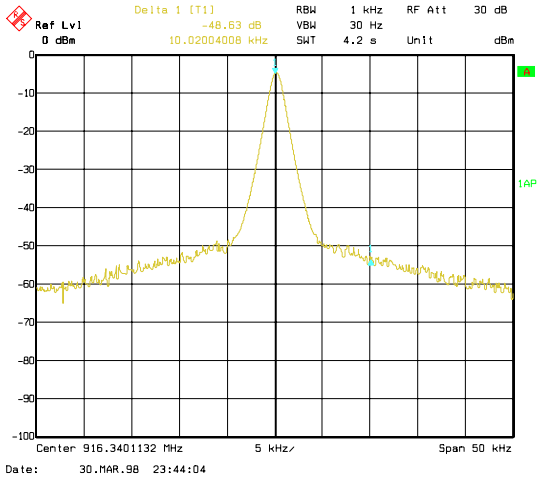


Figure 11a. Measured Phase Noise (BW=5kHz)

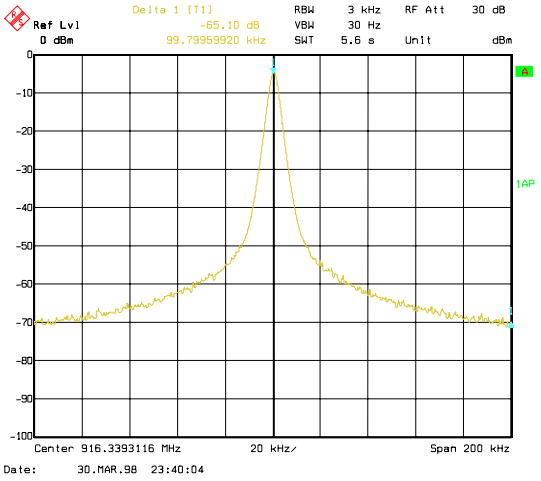


Figure 11b. Measured Phase Noise (BW=5kHz)

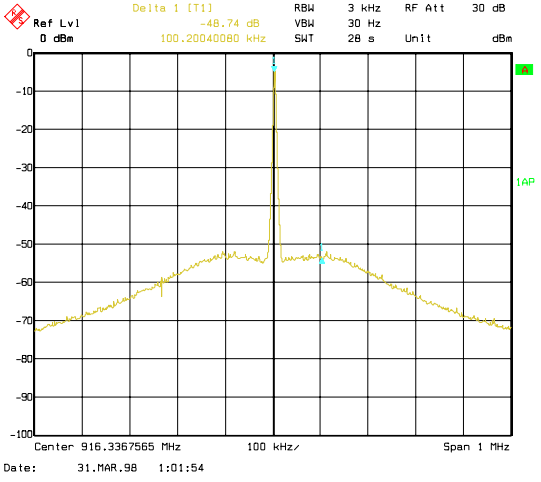


Figure 11c. Measured Phase Noise (BW=100kHz)

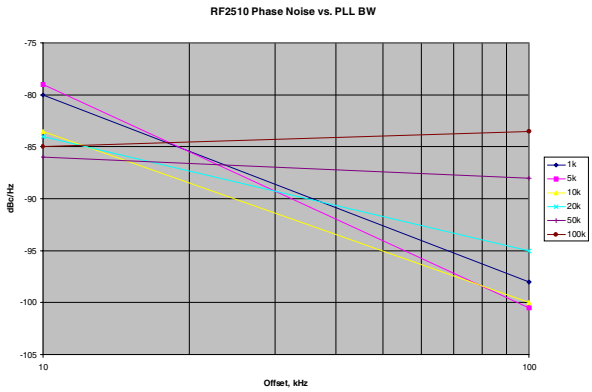
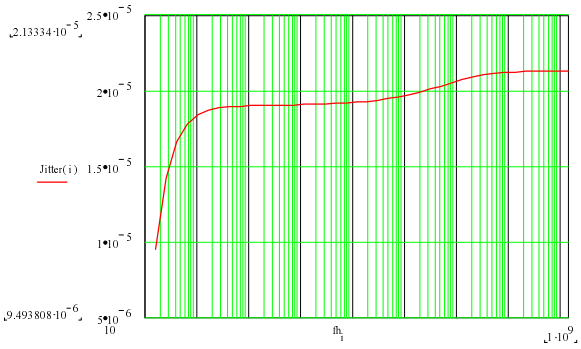


Figure 12. Measured Phase Noise as a Function of Loop BW

Once the phase noise characteristic is obtained, information such as Jitter, RMS Phase Deviation, and RMS Frequency Deviation or Residual FM can be determined. Jitter is obtained by integrating the phase noise over a specified bandwidth. Figure 13 shows results of this integration for different bandwidths using 10Hz as the lower limit. For upper limits of 100Hz and above, the Jitter is approximately $2x10^{-5}rad^2$. RMS Phase Deviation is the square root of the Jitter. Figure 14 shows the RMS Phase Deviation in degrees. For upper limits of 100Hz and above, the RMS Phase Deviation is approximately .25degrees. RMS Frequency Deviation or Residual FM is obtained by multiplying the phase noise by a frequency term and then integrating over a specified bandwidth. Figure 15 shows the RMS Frequency Deviation or Residual FM which is approximately 1Hz for an upper limit of integration of 3MHz. In practice, this upper limit is determined by filters which limit the noise bandwidth. Figure 16 shows the equations for calculating the above parameters from phase noise plots and Table1 shows some data sheet parameters for the RF2510.



.Figure 13. Jitter in rad^2 for BW=10Hz-fhHz

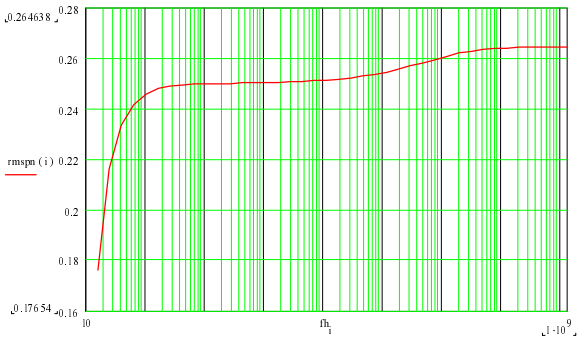


Figure 14. RMS Phase Deviation in deg for BW= 10Hz-fhHz

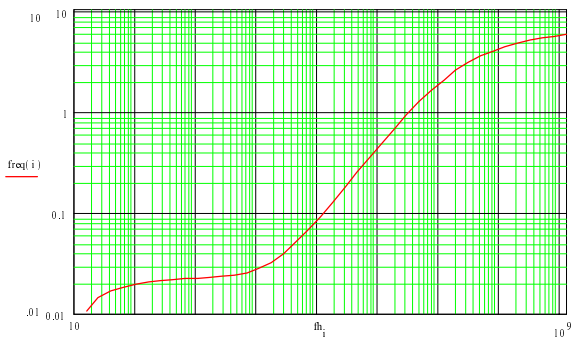


Figure 15. RMS Frequency Deviation or Residual FM in Hz for BW= 10Hz-fhHz

$$Jitter := \int_{fl}^{fh} 2 \cdot L(f)\, df \quad rad^2$$

$$RMSPhase := \sqrt{Jitter} \cdot \frac{180}{\pi} \quad deg$$

$$RMSFrequency := \sqrt{\int_{fl}^{fh} 2 \cdot L(f) \cdot f^2\, df} \quad Hz$$

Figure 16. Parameters Calculated from L(f)

Table 1. RF2510 Data Sheet Parameters

Parameter:	Specification			Units
	Min	Typ	Max	
General Characteristics				
Frequency Range	300	433, 868, 915	1000	MHz
Modulation Options		FM/FSK		
Transmitter RF Characteristics				
Output Power (50 ohm load)		-5.5		dBm
Modulation Rate			2	MHz
Max. FM Deviation	200			kHz
PLL/Prescaler Characteristics				
Prescaler Divide Ratio		64/65/128/129		
PLL Lock Time		4/Loop BW		ms
PLL Phase Noise (100kHz offset, 5kHz Loop BW)		-98		dBc/Hz
Crystal Startup		2	4	ms
Max. Crystal Rs		50		Ω
Charge Pump Output Current		+/-40		uA
Harmonics (with three element lowpass filter on board)		-50	-41.25	dBm
Spurious		-62	-49.2	dBm
VCO Gain, K_{VCO} (dependant upon external components)		70		MHz/V
Power Supply				
Operating Voltage	2.4	3.6	5.0	V
Tx Mode Current Consumption (3.6V)	7.5	10.5	13.5	mA
Sleep Mode Current Consumption			1	uA
Temperature Range	-40		+85	°C
Package		16 pin QSOP, plastic		

Note 1: The PLL Lock time is externally programmable through appropriate selection of an external resistor and capacitor (see application circuit)

Conclusion

The RF2510 is a Frequency Synthesizer Integrated Circuit designed for ISM Band transmitter applications. Its features have been discussed, and trade-offs between PLL parameters and phase noise have been presented. The RF2510 integrates PLL components such as a VCO, prescaler, RefOsc, phase detector, charge pump, and power down circuitry. The IC is available in industry standard SSOP-16 packaging and can be used to construct low cost transmitters.

Bibliography

4. Leeson, D.B. “A Simple Model of Feedback Oscillator Noise Spectrum”, Proceedings of the IEEE, Vol. 54, Feb. 1966, pp. 329-330.
5. Scherer, Dieter. “Today’s Lesson - Learn About Low Noise Design”, Microwaves, May 1979, pp. 72-77.
6. Hock, Terrence. “Synthesizer Design With Detailed Noise Analysis”, RF Design, July 1993, pp. 37-48.

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