A Dynamic Current Control Scheme for RF Power Amplifiers

Abstract

A commonly applied technique to improve linearity of an RF power amplifier is to increase the quiescent current so that the transistor operates in a more linear portion of the I/V curve. This method unfortunately requires the amplifier to run at high idle current all the time even if the input is not large enough to demand the linearity. A dynamic current control scheme is demonstrated here to automatically adjust bias current on a need basis to meet linearity requirements.

Introduction

State-of-the-art RF systems demand higher linearity power amplifiers to minimize adjacent and alternate channel distortion. Portable systems have an additional challenge in meeting the tough requirements with high efficiency. It thus behooves RF designers to create new schemes to optimize efficiency and obtain the required linearity. This paper demonstrates a feed-forward circuit which senses the input power level of the signal and dynamically adjusts the bias current of the amplifier. It is shown using Spice simulations that, at low input power levels, obtain an improvement of about 50 percent in DC power consumption, while allowing about 6dB increased linear output power.

Design Requirements

There has been a general trend in the RF IC industry to optimize process technology for a particular application. RF Micro Devices uses Optimum Technology Matching™, where we apply high performance GaAs HBT and MESFET technology to Power Amplifier (PA) designs and front ends, and lower cost BiCMOS technology to RF/IF ASIC design. This partitioning allows optimum price/performance trade-off. It is easier to design temperature, power supply and process insensitive circuits in BiCMOS technology than in GaAs MESFET or HBT technology. Control and logic functions can also be easily accommodated by BiCMOS circuits at lower cost and higher performance. Thus, implementing multi-technology IC's in one chipset will improve performance, provide additional features and lower cost.

The scheme described here uses a BiCMOS control circuit to improve linearity and efficiency by dynamically controlling the amplifier bias.

Method

As shown in Figure 1, the system described here consists of a two stage, 20dB gain PA driver (operating between 1800MHz to 1900MHz) and a support chip supplying bias reference currents. Figure 2 shows the bias control circuit. For simplicity, the bias circuit shown here focuses on controlling bias with respect to the input signal with other functions stripped off.

Figure 1. Top Level Schematic

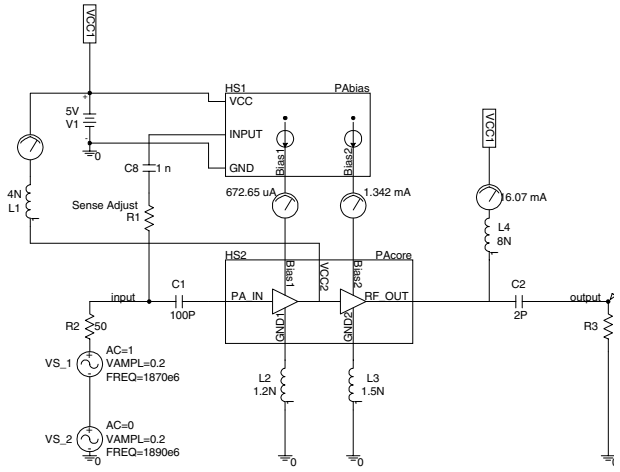
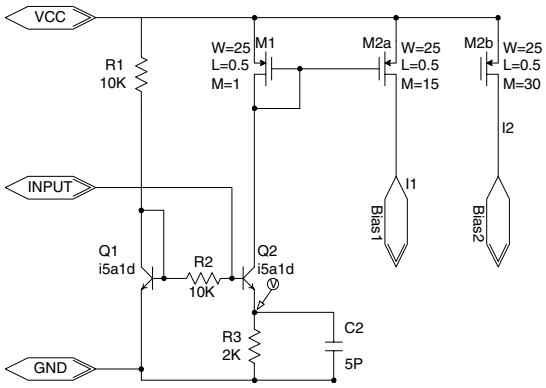


Figure 2. PaBias-Block Simplified Schematic

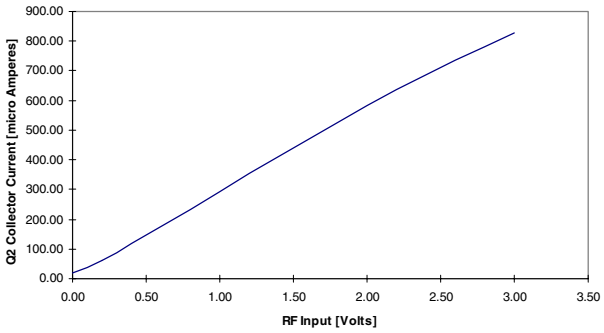


The circuit in Figure 2 senses the strength of the input signal and converts it to DC current which is then mirrored over by the PMOS transistors. Q1, Q2, R1, and R3 set up the minimum DC bias conditions when the input signal is small. In this mode, the current in Q2 is small and is used to bias the amplifier, creating a more efficient system when the input signal is small. As the input signal gets larger, Q2 amplifies and rectifies the

signal, and the components C2 and R3 filter the rectified signal. We are left with a DC current that is used to set the bias current in the PA driver. The larger the input signal, the larger the bias current (see Figure 3), allowing the amplifier to linearly amplify larger signals than before. R3 and C2 also set the time constant of the system. In the top level schematic, the input consists of a sense resistor (R1) and a DC blocking capacitor (C8). R1 is used to adjust the transconductance of the dynamic bias system.

Figure 3 shows the transfer function of the bias block. As the RF input peak voltage (at 1880MHz) is swept from 0V to 3V, the output DC current I Q2 collector changes from 18µA to 828µA. This current effectively sets the operating regions of the PA transistors. The second stage requires twice the first stage current to operate, and the two output PMOS transistors are sized accordingly. The bias control can be easily removed from the circuit by grounding the sense resistor (R1), or making it very large.

Figure 3. PABias Schematic's Q2 Collector Current versus RF Input at 1800MHz



Results and Discussions

Figure 4 shows the Spice simulation depicting the gain compression characteristic of the PA driver versus the input power for the system. The figure shows the linear operating range of the PA driver, controlled by the automatic bias control, extended about 6dB as compared to constant bias case.

Figure 4. Gain Compression of the PA Driver

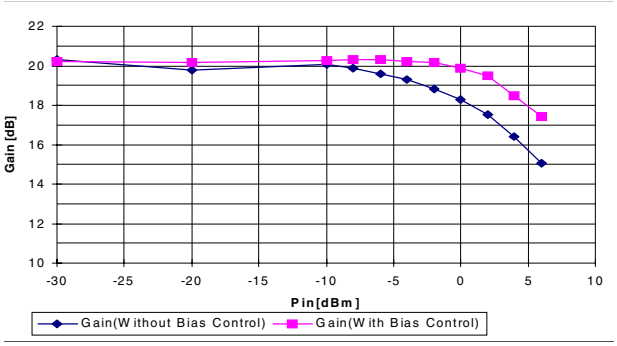
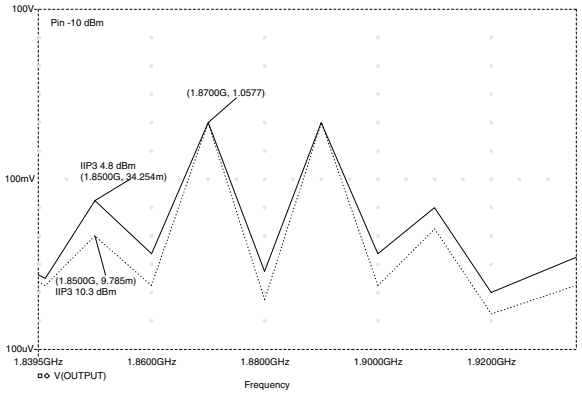


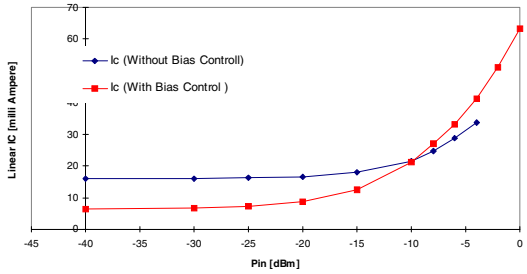
Figure 5 shows the Input IP3 Plot for the two cases. The Input IP3 is about 5.5dB higher with the automatic bias control activated.

Figure 5. Two-Tone Input IP3 of the PA Driver With and Without Automatic Bias Control



Finally, Figure 6 shows the efficiency (in terms of linear output collector currents) of the system operating with and without bias control. In order to demonstrate this over a wide dynamic range, the external sense resistor (R1) of the top level schematic, and R1 of the PABias schematic, were increased to 3kΩ and 100KΩ, respectively. It can be seen that under small signal conditions, the quiescent currents are much lower for the circuit with automatic bias control. At the same time, the automatic bias control extends the linear operating range under large signal conditions. Thus, efficiency is dynamically adjusted as the PA driver input power varies.

Figure 6. Linear Final Stage RMS Collector Currents for the Two Cases as the Input Signal is Varied



Conclusions

A new dynamic bias technique for use with RF Power Amps is presented. This circuit adjusts the bias current in the PA depending on the input power level sensed. At low input power levels, about half the DC current is used, thereby doubling the amplifier efficiency. At higher input power levels, the bias current is increased, allowing about 6dB more output power before linearity is compromised.