Low Cost Family of 3V Silicon Gain Blocks

Abstract

RF Micro Devices introduces a family of low cost silicon gain blocks designed for 3V supply operation. Part numbers RF2321, RF2322, RF2323, RF2325, and RF2326, comprise the family. The parts are packaged in SOT23-5 lead packages and are available on evaluation boards from RF Micro Devices. Applications include broadband gain stages, final PA for ISM band applications, driver amps, oscillator loop amplifiers, and buffer amplifiers.

Introduction

Two different circuit topologies are used in the 3V gain block family. The first is a dual common emitter (CE-CE) topology (RF2321/2322/2323), and the second is a Darlington topology (RF2325/2326). Figure 1 shows the amplifier schematics, and Figure 2 shows the applications schematics for the two topologies. In both designs, series and shunt feedback are used to simultaneously set the gain and the impedance match.

Figure 1: Amplifier Schematics

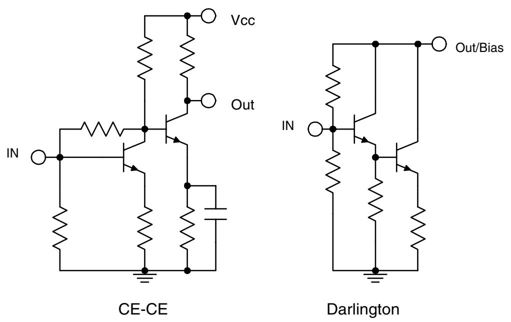
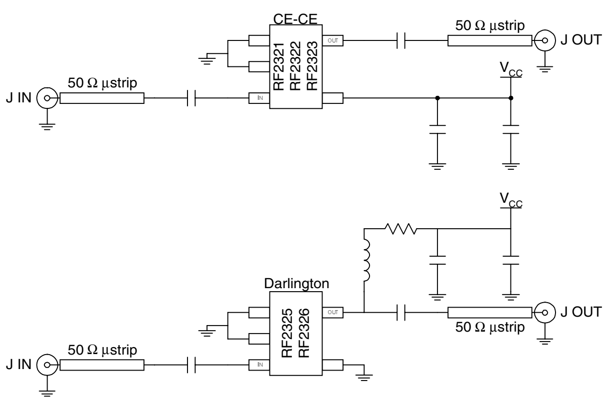
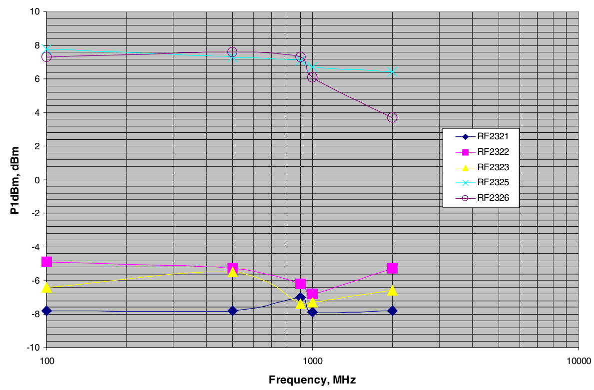


Figure 2: Applications Schematics



The use of the two circuit topologies results in varied circuit performance. The CE-CE designs require no external bias components and have lower noise figures; however, they are limited in output power to approximately -5dBm to -8dBm P1dBm (see Figure 3). They are biased at approximately 7mA. The Darlington designs require external bias components and have higher noise figures, but have a P1dBm of 6dBm to 7dBm. They are biased at approximately 25mA.

Figure 3: Output Power (P1dBm)



Design Descriptions

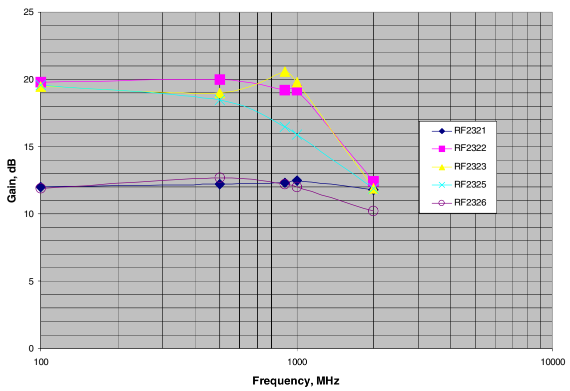
The CE-CE amplifiers have two stages of gain to cascade for the overall gain. Putting more gain in the first stage as well as optimizing the input transistor allows the lower noise figures to be achieved. The collector resistor in the second stage sets the output impedance as well as affecting the gain of the second stage. The fixed resistor between the collector and supply causes the amplifier to compress at lower input levels than the Darlington due to limiting on the positive half cycle of the output. In the Darlington topology, the limiting occurs on the negative half cycle when the collector base junction voltage of the second transistor approaches zero. The Darlington's first stage is essentially an emitter follower with unity voltage gain which tracks the input. In the Darlington there is no intermediate stage of amplification whose voltage swing must be accommodated to remain linear. This results in larger available output swings.

The evaluation board for the CE-CE designs requires only bypass and blocking capacitors. The values should be optimized for the desired frequency of operation. Typically a low and a high frequency bypass capacitor will be chosen to ensure that a broad range of noise will be filtered. All test data was taken using 100pF blocking and a 1nF bypass capacitor.

The Darlington amplifiers required the same capacitors as the dual CE designs, as well as some bias components. A series resistor and choke are used to bias the Darlington topology. The resistor is used to establish a bias current into the amplifier. It also serves to stabilize the current over temperature through negative feedback. The choke is chosen to have an impedance of at least 10Zo or 500Ω to prevent the network from loading the output.

The CE-CE designs incorporate capacitive compensation in the emitter circuit of the second stage. This boosts the gain at high frequencies, thus extending the bandwidth of the device. The value is chosen to extend the bandwidth as much as possible while avoiding excessive gain peaking at the 3dB point. Figure 4 shows a plot of the gain of the five parts in the family.

Figure 4: Gain Figures

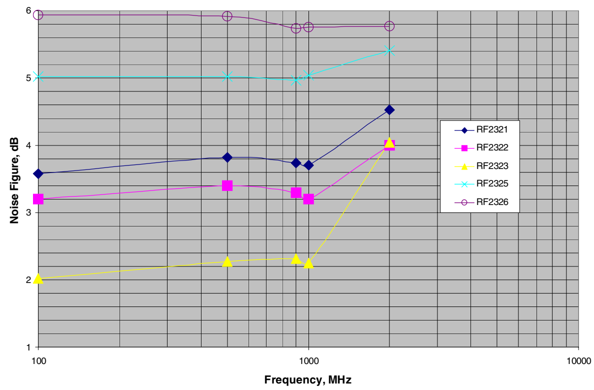


Performance Data

The RF2321 and RF2326 have a nominal gain of 12dB. The nominal gain of the RF2322, RF2323 and RF2325 is 19dBm to 20dBm. As can be seen, all parts have 10dB or more usable gain at 2GHz.

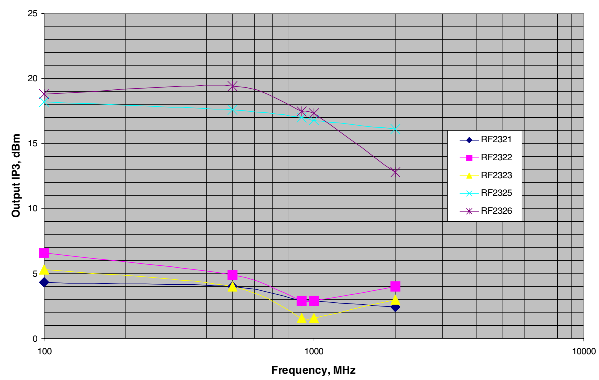
Figure 5 shows the noise figures for the five parts. The RF2323 has a noise figure of 2.3dB at 900MHz making it suitable for some LNA applications.

Figure 5: Noise Figures



IP3 values are shown in Figure 6. Note that these values are 10dBm to 12dBm above the P1dBm in Figure 3. The Darlington amplifiers have an IP3 of 17dBm at 900MHz.

Figure 6: IP3 Values



Input and output return loss is shown in Figures 7 and 8. The input match of the RF2323 is worse than the other parts due to its very high first stage gain. This gave it the low noise figure discussed earlier. Note that all the data shown is from evaluation boards assembled as in Figure 2. No reactive tuning elements were used to match the devices. The output match of the RF2321, RF2322 and RF2323 is set by the output collector resistor, whereas the output match of the RF2325 and RF2326 is set by series and shunt feedback closer to 50Ω.

Figure 7: Input Return Loss

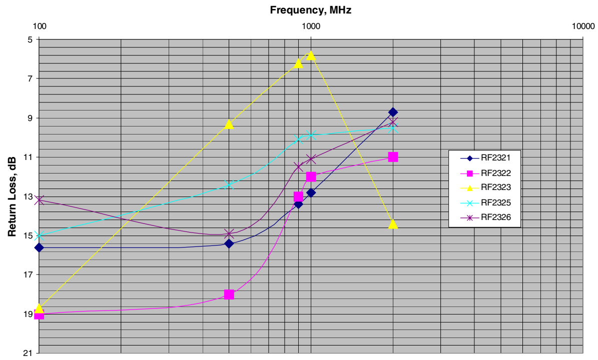


Figure 8: Output Return Loss

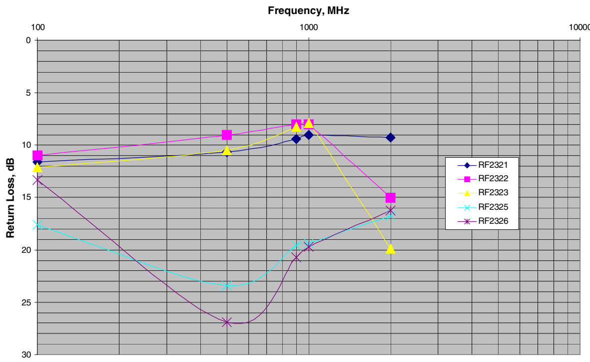
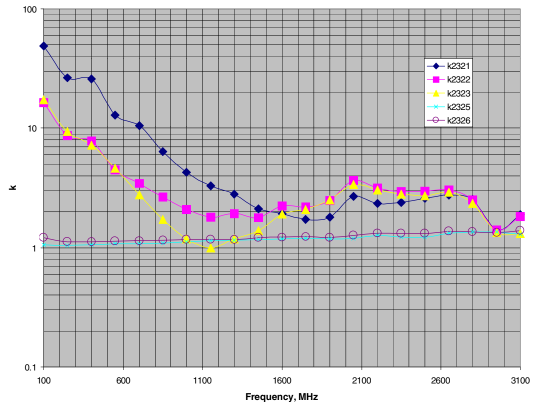


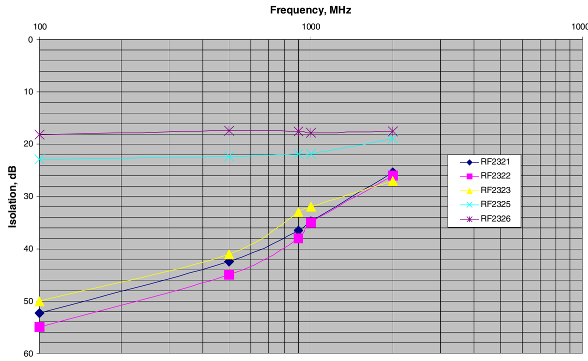
Figure 9 shows calculated values of k, indicating unconditional stability for all five parts. The parasitics of the package contribute heavily to the stability of the amplifier, particularly in the ground circuit(s) of the amplifiers. Unintentional feedback between stages can lead to degraded input match and potential instability.

Figure 9: Stability Analysis



The final parameter to be measured was reverse isolation. Figure 10 compares the five parts. As can be seen, the dual CE topology offers superior isolation due to its dual stage design, however the Darlington configuration results in at least 17dB of broadband isolation.

Figure 10: Isolation



The 3V Silicon Gain block family has been characterized from 2.7V to 3.3V supply and over a temperature range of -40°C to +85°C. The parts are rated at 4V maximum supply voltage.

Conclusion

RF Micro Devices has introduced a family of 3V Silicon Gain Blocks. They are packaged in an industry standard SOT23-5 lead package for low cost and small size. The five parts range in gain from 12dB to 19dB and are designed to be unconditionally stable. Potential applications include broadband gain stages, final PA for ISM band applications, driver amps, oscillator loop amplifiers, and buffer amplifiers. The use of resistive feedback for gain setting and impedance matching results in very compact and broadband designs. This also translates to very low cost and manufacturable designs, eliminating costly tuning associated with narrowband and/or discrete designs.

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