A Study of Device Input Impedance in PSpice

When coupled with accurate nonlinear models, Spice allows observation and manipulation of circuit behavior that is impossible in the lab using test equipment. The procedures outlined have been developed using PSpice [1], although the principles apply to Spice programs in general.

One aspect of a circuit's behavior that is of interest to amplifier designers, and power amplifier designers in particular, is the input impedance of a device under large-signal drive. In the past, this quantity has been approximated by the small-signal value, determined from S-parameters or small-signal analysis. However, as the signal levels increase and nonlinear currents begin to flow, the impedance shifts.

There a number of ways to determine the nonlinear input impedance, but the most straightforward is the introduction of a sensing resistor (0.001Ω) into that circuit branch to monitor the voltage and current. This works fine for AC analysis (i.e., small-signal) but for large-signal transient analysis, V(t)/I(t) is not the device input impedance. The impedance can be determined by applying a fast Fourier transform (FFT) to V(t) and I(t) to generate magnitude and phase of the fundamental before the division. This approach is not a familiar technique to RF designers where the foundation for impedance measurement and transformation is based upon s-parameters. Standard Spice s-parameter techniques have been adapted for large-signal applications.

S-parameter measurements are conducted by applying energy to a system port. All the remaining ports are terminated with a convenient impedance. Energy is reflected back toward the source, and some energy comes out the remaining ports. The excitation is at a known amplitude and frequency, and the amplitude and phase of the transmitted and reflected signals may be determined. For small-signal measurements, harmonic generation is not a problem. Large-signal waveforms in a nonlinear system will be distorted. In this case, the reflected signal contains the fundamental tone plus varying amounts of harmonics. Is S11 all the reflected energy or just the energy contained in the fundamental? A simplifying assumption is to only consider the fundamental frequency. In this case, the goal is to determine the input impedance for matching purposes, and the impedance at the input frequency is the desired result.

In determining the input impedance in the final circuit of a device under bias conditions, the primary focus will be S11. If desired, the output signal at the load can be easily determined, allowing a computation of S21. The amplifier may then be turned around within the test setup to provide S22 and S12.

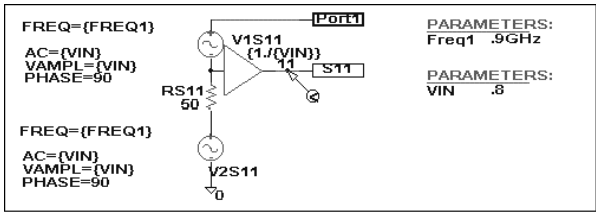

Figure 1. Single Port S-Parameter Test Set (modified for large signal TRANsient analysis)

S-Parameter test set

The S-parameter test set is shown in Figure 1. This is an extension of the standard test set with the following features:

1. A large-signal sine wave generator (a PSpice VSIN element) has been used in place of the small-signal AC source.
2. The large-signal frequency is set by the parameter FREQ1 so both generators track. During AC analysis, the source frequency for both generators is swept in the normal fashion.
3. The peak signal amplitude is set by the parameter VIN for both the AC and the transient case.
4. The S11 output is normalized by the (1/VIN) gain block.
5. The phase of the large signal source is offset by 90^{o} to provide the correct phase after the FFT.
6. A global symbol for Port1 is used to allow the signal generator to reside on a different page of the schematic.

The addition of the amplitude parameter VIN and the output signal scaling allows this test set to be used as a variable amplitude signal source. Electrical energy is applied to the circuit input port. Impedance mismatches between the generator and the circuit cause reflections and phase shifts in the reflected signal. The reflected signal at S11 of the test set contains the desired impedance information according to [1]:

$$\frac{Z}{Zo} = \frac{1+S11}{1-S11} \qquad [1]$$

where S11 is a complex number (normally presented as τ in this type of expression) and Zo is the reference impedance of the system RS11 of 50Ω in Figure 1.

This brings up an interesting issue concerning what source impedance should be used. Actually, it doesn't matter, because the reflected energy is related to the impedance ratio. However, the power delivered into the port is reduced by the reflected energy, and the drive level may need to be modified to provide a given input power. The accuracy for the computed impedance will be improved if the value of S11 is toward the center of the Smith chart. For example, a power device may have an input impedance close to 10Ω. If RS11 is changed to 10Ω, better efficiency will be obtained in coupling energy into the device, the reflected energy represented by S11 will be smaller, and the resultant device impedance will be obtained with improved accuracy.

The circuit to be investigated is shown in Figure 2. C1 and C2 provide DC blocks for the device input and output. Actually, C1 will become part of the interstage matching network. The two transmission lines have a time delay that is 90° at 900MHz. T1 provides a quarterwave stub for collector bias, and T2 transforms the 50-Ω load into 1Ω at the device collector.

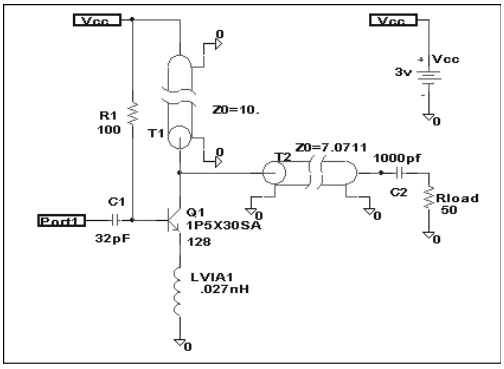

Figure 2. Test Transistor with Bias and Output Transformer

Before starting the nonlinear study, a linear (i.e. AC) analysis of the circuit is beneficial. The test set is connected and swept from 800-1,000MHz. RS11 was set at 10Ω and is the basis for the measurements. The output can be displayed in a familiar presentation by plotting the imaginary part of S11, i.e. IMG(V(S11)) on the y-axis and the real part of the S11, i.e. R(V(S11)) on the x-axis. The scale on both axes ranges from -1 to +1. This polar form (shown in Figure 3) is one of the normal presentations of S-parameters. In this case the Smith chart grid system is missing.

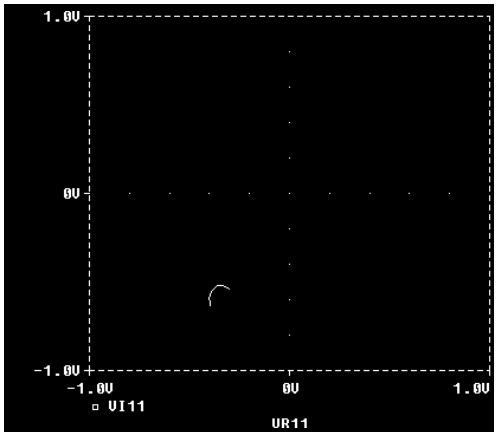

Figure 3. Small Signal S11 Displayed in Polar Format

Equation 1 may be rewritten in polar coordinates by expressing S11 as:

$$S11 = M\cos\phi + jM\sin\phi \quad [2]$$

where M is the magnitude and ϕ is the angle of S11.

$$\frac{Z}{Zo} = \frac{1 - M \times M + j2M\sin\phi}{1 + M \times M - 2M\cos\phi} \quad [3]$$

At 900 MHz the value of S11 from the figure is 0.659 at -125.3°. Using these values in Equation 3 along with 10μ for the reference impedance is Zo, the small-signal input impedance is computed at Z=2.57-j4.90.

Large-signal excitation

Three factors must be taken into account when a large-signal transient analysis is performed for S-parameter analysis. To avoid introducing errors in the FFT, the initial transient response of the circuit must have decayed, the section of waveform selected for analysis must contain an integer number of cycles, and the waveform must start at an integer number of periods after t=0. Figure 4 shows the voltage waveform at the circuit input, output and the reflected input signal. This was generated with VIN = 0.6V and RS11 at 10Ω. Even at this level, the circuit is starting to generate obvious non-linearities. Notice that the signals do not reach a steady state until almost 15nsec into the simulation. If a section of the waveform from 20-40nsec is used for analysis, 18 complete cycles will be starting exactly 18 cycles after t=0. This is important because any shifting along the time axis is a phase shift after

the FFT. Anything other than an integer number of cycles will directly affect the results.

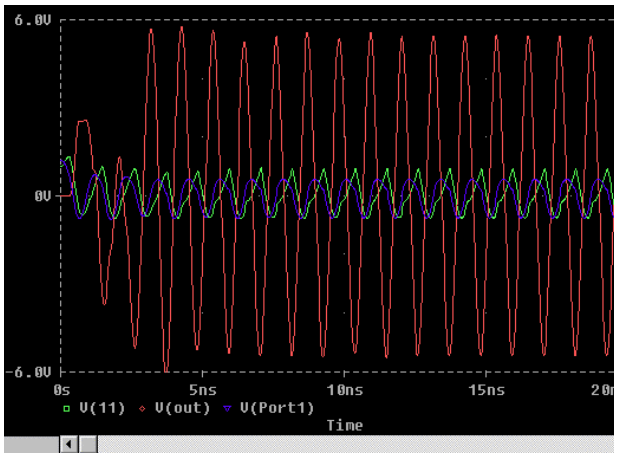

Figure 4. Circuit Response Waveforms Showing the Initial Start-Up Transients

A simulation that swept the VIN parameter from 0.05-1 V at 900MHz was set up and a transient analysis was generated for 40nsec at each VIN value. The output data was restricted to a range from 20-40nsec for the subsequent processing. An FFT of V(S11) was performed and the magnitude and phase data were copied into a spread sheet. The data at 900MHz was selected and processed according to Equation 3. Figure 5 shows the results of that calculation. As can be seen, the driving point impedance of this device changes radically with drive level.

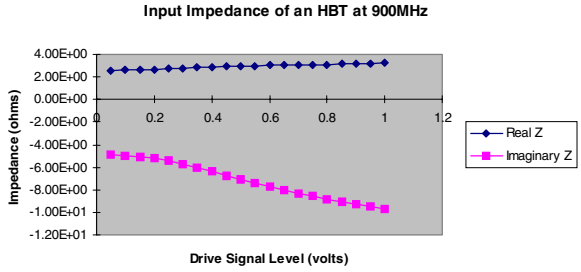

Figure 5. Variation in Input Impedance with Drive Level

Now suppose that VIN = 0.6V was a desired input signal amplitude. This level may provide the optimum efficiency or minimum distortion. At VIN = 0.6V, the input impedance is (from the data used in the plot) Z = 3.02 - 7.75j. This is the impedance needed for the interstage matching network design that will implement the desired features. However, one more interesting experiment sheds light on the dynamics of the problem.

The magnitude of S11 at this drive level was 0.688. The power delivered into the device is:

$$Pin = (1 - S11 \times S11) \times Vin \times \frac{Vin}{(4 \times RS11 \times 2)}$$

$$= (1 - 0.688 \times 0.688) \times 0.6 \times \frac{0.6}{(4 \times 10 \times 2)} \quad [4]$$

$$= 2.37mW$$

(the factor of 2 is to convert peak to RMS and Zo is 10Ω). Now the test set can be matched to the device. A 1.37nH inductor has an impedance of 7.75jΩ at 900 MHz. An inductor is added in series with the test set to cancel out the capacitive component in the device, and the base impedance RS11 is changed to 3.02Ω.

Re-sweeping the VIN parameter from 0.05V to 1V and plotting the magnitude of V(S11) (see Figure 6) shows that, at about the 0.225V input drive level, there is an excellent power match to the test set. The source impedance is a conjugate of the device impedance previously determined. The power delivered to the device at the fundamental frequency and new drive level approaches 2.07mW. This is close to the previous value. VIN is lower because the system impedance has been reduced, and most of the energy is now coupled into the device. Also, the power reflected at the second harmonic has increased. The key point illustrated by this exercise is that the optimum matching network designs for large-signal applications will depend on the signal level.

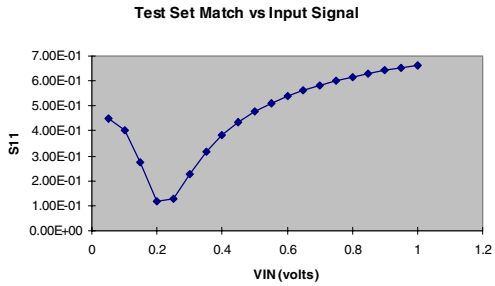

Figure 6. Test Set Match versus Input Level for Z=3.02+7.75j

Linear impedance sniffer

Are the results valid? Can these results be obtained in some other fashion that allows verification of the calculations? In the case of a linear analysis or transient analysis with a small input signal, the answer is yes. An

impedance sniffer shown in Figure 7 can be used to directly present the real and imaginary impedance at any point in a circuit. The 10-megohm resister is there to keep PSpice happy (i.e., converging) when the "test" port is open circuited.

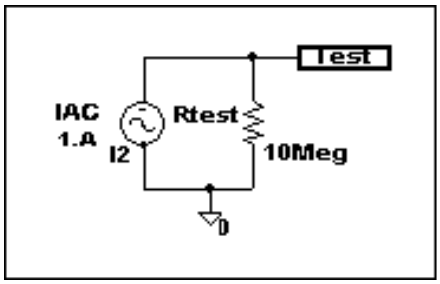

Figure 7. Impedance Sniffer for AC Analysis

The test point is connected to the desired circuit node, and 1 A of AC current is injected. Ohm's law is considerably simplified in this case. The real and imaginary voltage at the test port is the real and imaginary impedance. But you can't inject an ampere of AC current just anywhere. In the AC analysis, everything is linearized. The current source could be set for a mega-amp, but it's easier to divide by one. Running the simulation (Figure 2 with PORT1 replaced by TEST) and taking the real R(V(test)) and imaginary IMG(V(test)) at 900 MHz produces the linearized input impedance of 2.571 - j4.897. This value agrees well with the previous calculations.

Conclusions

A method of determining the large signal input impedance of a circuit has been presented that is useful within PSpice. The procedure is straightfoward to implement and self-consistent. As the source signal level is reduced, the impedance converges to the values determined from small signal analysis. These same tools can also be used to determine how a large signal match varies with signal level. One important question remains. Are the impedances believable? The decision to believe the results is based on the trust in the device models. How do you gain trust in the model? One way is to design circuits using the models and then see if they perform according to those predictions when they are fabricated. And, to that end, large signal S-parameter techniques can improve the design process.

References

1.PSpice is a registered trademark of MicroSim Corp.

2.Vendelin, George, *Design of Amplifiers and Oscillators by the S-Parameter Method*, John Wiley, 1982.