Implementing a π/4 Shift D-QPSK Baseband Modem Using the TMS320C50

Authors: J. Webber, N. Dahnoun

ESIEE, Paris

September 1996
SPRA341

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

Contents

Figures

Implementing a π/4 Shift D-QPSK Baseband Modem Using the TMS320C50

Abstract

π/4 D-QPSK ('π/4 shift Differential-Quadrature Phase Shift Keying') is a four level modulation scheme first proposed by Baker in 1962[1] and is currently the focus of intensive research. The scheme is currently implemented in the American Digital Cellular, Japanese Handy Phone and the European TETRA systems.

The aim of this undergraduate project[2] was to implement a π/4 Shift D-QPSK baseband modulator on the Texas Instruments (TI™) TMS320C50 digital signal processor (DSP). The functions included π/4 D-QPSK signal mapping using a look-up table and raised cosine filtering to reduce Inter-Symbol Interference (ISI), and spectral spreading. The report also describes the differential detection and data recovery implementations in the demodulator; and the theory behind the symbol timing recovery module is introduced.

Raised cosine filtering of the I and Q channel streams at the modulator output was implemented digitally using a twenty tap FIR filter. A technique called interpolation was used in the filtering algorithm to increase the sampling rate and relax the reconstruction filter design. The filter coefficients for use in the DSP program were derived using a Matlab program.

This document was part of the first European DSP Education and Research Conference that took place September 26 and 27, 1996 in Paris. For information on how TI encourages students from around the world to find innovative ways to use DSPs, see TI's World Wide Web site at www.ti.com.

Product Support on the World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Baseband Communications

In this class of modem the modulator and demodulator functions such as signal mapping and filtering are completed at *baseband* frequencies as opposed to directly modulating the carrier at IF. Baseband signal processing is advantageous as DSP techniques can then be applied. Baseband frequencies of up to a few hundred kHz can be processed by current DSP clock speeds.

Figure 1. Baseband Communications

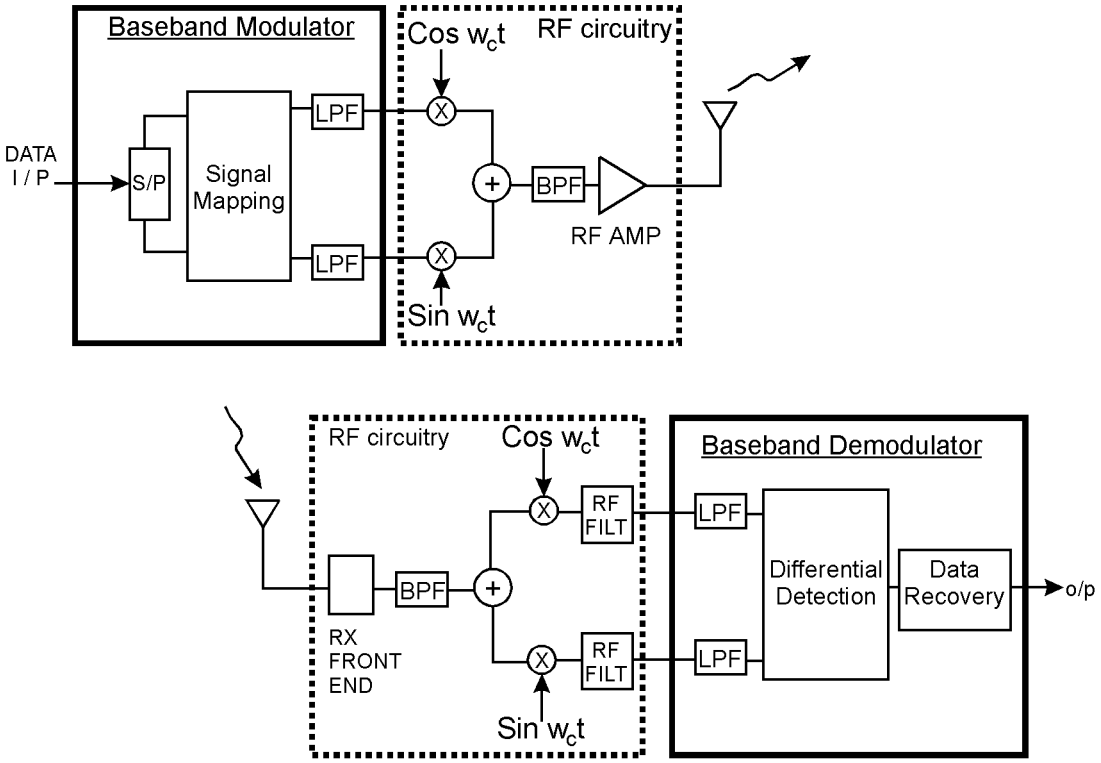


Figure 2. Modem Design in DSP

Modem Design in DSP	
Advantages	**Disadvantages**
Good noise immunity	High current drains
No insertion/matching problems	Conversion steps
Accuracy predicted & controlled	D/A Speed limitations
Wide dynamic range	Larger chip area
Linear phase filtering	Band-limit input freq.'s
Guaranteed Stability	
Software flexibility	
Adaptive filtering possible	
High Performance/cost	

Figure 1 shows the relative position of the baseband modules developed in this project in relation to the complete communications system. Principally, the output of the *baseband modulator* would be mixed with the carrier frequency, RF filtered and power amplified. The signal detected at the receiver would be demodulated by mixing it with a local carrier oscillator, RF filtered, and input to the *baseband demodulator*

Modem functions such as signal mapping and filtering require repetitive algorithms to be processed at high clock speeds. These functions are particularly suited to DSP techniques (Figure 2).

Modulation Techniques

Performance Trade-Off's

The performance of a digital cellular system in terms of the number of users per km^2 and data transmission rate depends on the modulation technique. The method determines the bandwidth efficiency in terms of the number of bits per second that can be transmitted per Hertz of channel bandwidth. The following factors must be considered when selecting a suitable cellular modulation technique:

- High power efficiency
- High bandwidth efficiency
- Low out of band radiation
- Low sensitivity to multi-path fading

- Constant envelope
- Low cost
- Ease of implementation

It is not possible to select a modulation scheme that simultaneously optimises all of the above features as each has its own practical limitations and some are interrelated. A high bandwidth efficiency, for example, requires a large signalling set and this requires an increase in signal power at the transmitter.

Classification of Modulation Techniques

There are three principal modulation groups:

- Amplitude Shift Keying (ASK)
- Frequency Shift Keying (FSK)
- Phase Shift Keying (PSK)

PSK systems represent the transmitted data signal by varying the phase of a fixed frequency carrier. All communications channels will distort the applied signal to varying degrees in phase, amplitude and or frequency. The general expression for a modulated carrier is:

$$y(t) = a(t) * \cos [w_c t + \theta(t)] \quad [1]$$

where: $a(t)$ = amplitude
$w_c t$ = angular frequency
$\theta(t)$ = phase

Figure 3 summarises the characteristics of the three modulation groups, together with APSK a hybrid of ASK and PSK.

Figure 3. Summary of Modulation Groups

ASK	PSK/FSK	A & P SK
Needs linear amp to preserve envelope	Constant or non constant envelope depends on filtering	Most spectrally & power efficient
Vulnerable to rapid channel gain fluct.s	Insensitive to channel fluctuations	Needs linear power amp
Freq./Phase error insensitive	Doppler and carrier phase error sensitive	Channel gain & phase distortion sensitive
Rarely used	Currently most popular format	Likely to dominate as amplifier tech. improves

Demodulation can be classed into techniques that use *coherent* and *non-coherent* methods. Coherent demodulators generate a local carrier, which is phase synchronised with the transmitter. Up to 70% of the demodulator circuitry can be attributed to carrier synchronisation and so classes of techniques such as differential detection that don't require coherent detection are important. However, they require 3dB more transmit power to achieve the same bit error rate (BER) performance.

Envelope Variations

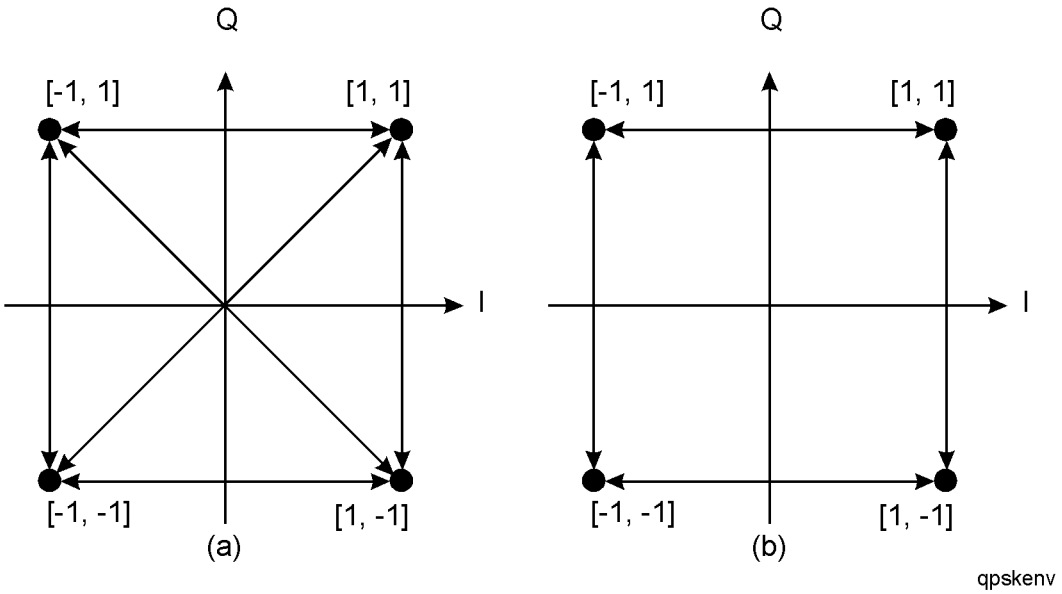
Most digital transmitters operate their high power amplifiers at or near to saturation in order to achieve maximum power efficiency. At saturation however, the signal is non-linearly amplified which generates amplitude and phase distortions. These distortions spread the transmitted signal into adjacent channels. A filter used to suppress the sideband lobes can introduce amplitude distortions when the input pulse changes abruptly. The result of these amplitude variations is to increase the bandwidth of the signal if non-linear amplification is used.[3]

In an ideal system, the transition from one constellation point to the next occurs instantaneously. However, filtering in a practical system will mean that the transition takes a finite time, resulting in a progressive phase change and hence signal envelope. The envelope variation of a signal is defined by the changes in the magnitude of the vector from the origin on the I-Q constellation diagram to the line 'traced' by the signal when changing from one constellation point to the next.

A Non-Offset QPSK

Alternate data bits are directly modulated onto the I and Q channels at the same time (Figure 4a). The 180° phase variations can cause envelope variations of up to 100%.

Figure 4. QPSK Envelope Variations (a) Non-Offset; (b) Offset



Offset QPSK

The offset refers to the fact that I and Q bit streams are delayed by half a symbol period to each other. Only two phase transients per symbol period are now possible: 90° and -90° (Figure 4b). Envelope variations are confined to 33%, reducing spectral spreading.

π/4 QPSK

One QPSK constellation is used to modulate odd symbol numbers and another offset by π/4 to modulate even symbol numbers (Figure 5). This results in a maximum phase transient of 135° (Figure 6), in between that of offset QPSK (90°) and non-offset QPSK (180°). However, π/4 D-QPSK has the advantage over offset QPSK in that it can be *differentially* detected. A stream of identical 1's or 0's will always produce a phase change.

Figure 5. π/4 QPSK

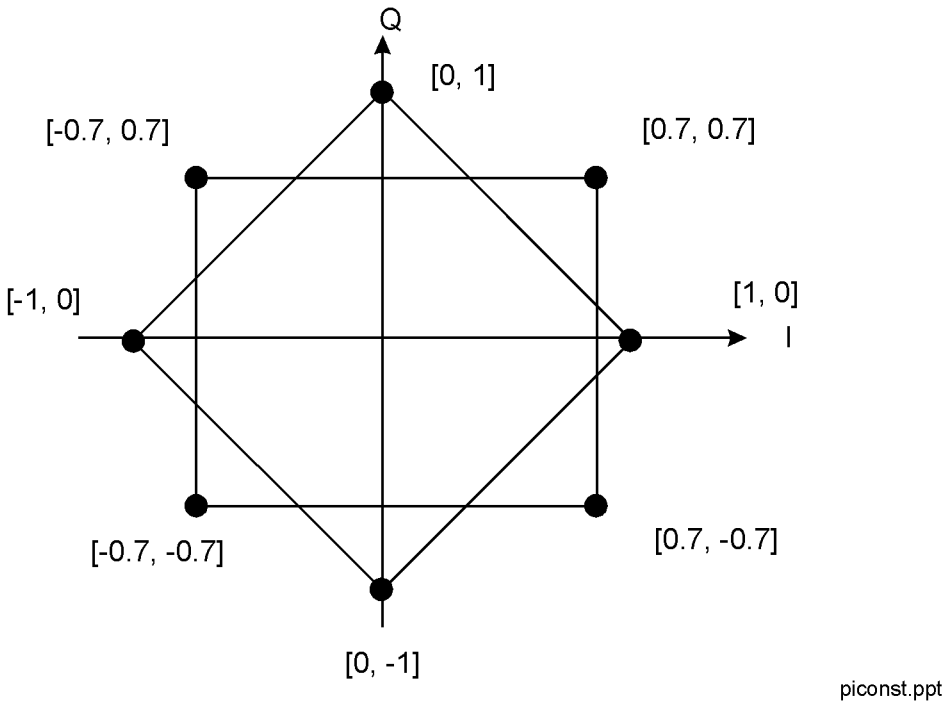
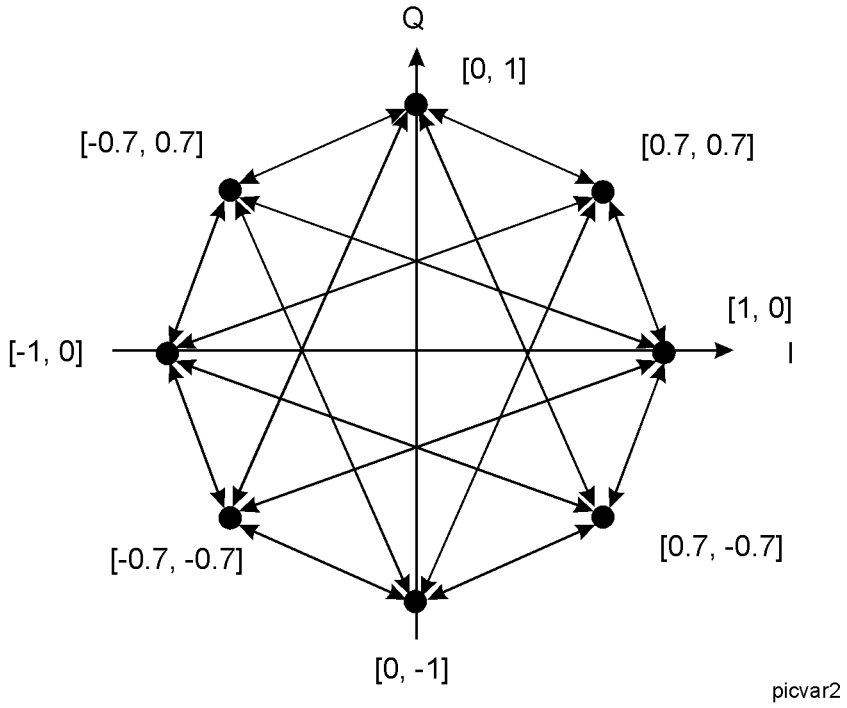


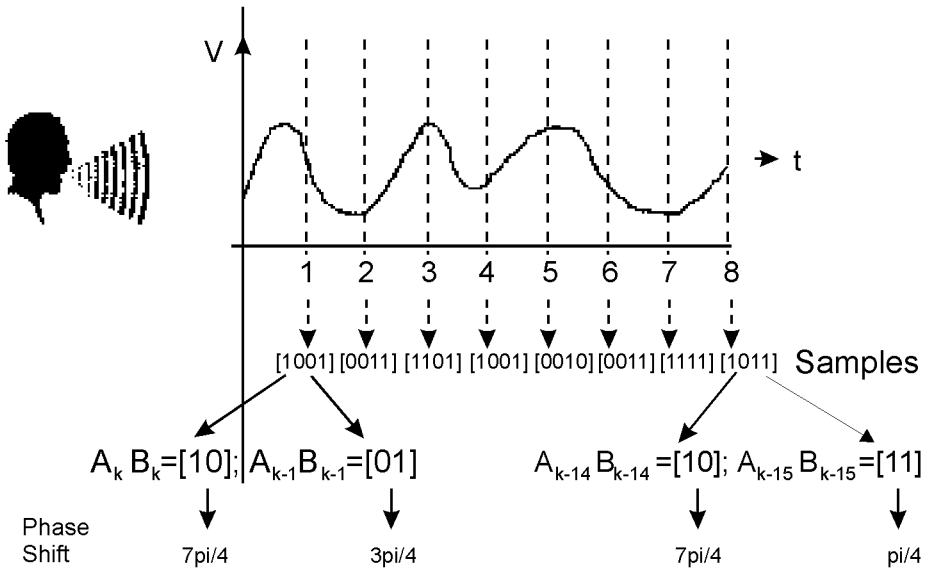
Figure 6. π/4 QPSK Envelope



Sampling the Input Signal

Input data will be either analogue or digital. Analogue waveforms need to be first sampled (Figure 7). Even bits are designated A_k and odd bits, B_k. A group of two bits, A_k B_k, is called a symbol (or 'dibit') and hence there are two symbols for every sample. Assume that each sample, S_w, consists of four bits.

Figure 7. Analogue Sampling



Let S = [A_0 B_0 A_{-1} B_{-1} A_{-2} B_{-2} A_{-3} B_{-3} A_{-4} B_{-4} ... A_{-n} B_{-n}] represents the complete waveform. Then, S_w = [A_k B_k A_{k-1} B_{k-1}] represents a particular sample of 4 bits.

Generation of π/4 D-QPSK Signals

There are four possible values for each dibit, A_k B_k. Each of the four different dibits will represent a different *phase shift, Δθ* (Figure 8). Phases are represented by points on the I-Q diagram. The phase being the angle made by the vector from the origin to the point on the I-Q diagram and the I=0 axis.

Figure 8. π/4 Phase Shift

A_kB_k	Δθ
0 0	+5π/4
0 1	+3π/4
1 1	7π/4
1 0	π/4

The present phase, θ_k, is simply equal to the previous phase, θ_{k-1}, plus the phase shift, Δθ. This can be easily obtained from knowledge of the previous phase representation [I_{k-1} Q_{k-1}] and the received dibit.

In π/4 D-QPSK the data is encoded in the change in phase of the transmitted carrier. Let S_{k-1} represent the carrier transmitted for the previous symbol and θ is equal to the absolute phase.

$$S_{k-1} = A \cos (w_c t - \theta) \quad [2]$$

Then, the carrier for the new symbol is:

$S_k = A \cos (w_c t – (\theta+\Delta\theta))$ where, $\Delta\theta$ is the phase change

$$S_k = A \cos (\theta+\Delta\theta) \cos w_c t + A \sin (\theta+\Delta\theta) \sin w_c t$$

$$S_k = I_k \cos w_c t + Q_k \sin w_c t \quad [3]$$

where, $I_k = A \cos (\theta+\Delta\theta)$

$$= A \cos\theta \cos\Delta\theta - A \sin\theta \sin\Delta\theta$$

$$= I_{k-1} \cos\Delta\theta - Q_{k-1} \sin\Delta\theta \quad [4]$$

and $Q_k = A \sin (\theta+\Delta\theta)$

$$= A \sin\theta \cos\Delta\theta + A \cos\theta \sin\Delta\theta$$

$$= Q_{k-1} \cos\Delta\theta + I_{k-1} \sin\Delta\theta \quad [5]$$

If the input data is *Gray coded* (Figure 9) then the values of ($\sin\Delta\theta$) and ($\cos\Delta\theta$) are obtained according to Figure 10. Note that a zero data bit is represented by minus one for the **A_{KG} and B_{KG}** which represents the logic values of the Gray coded data bit $A_K B_K$.

Figure 9. Gray Coded Phases

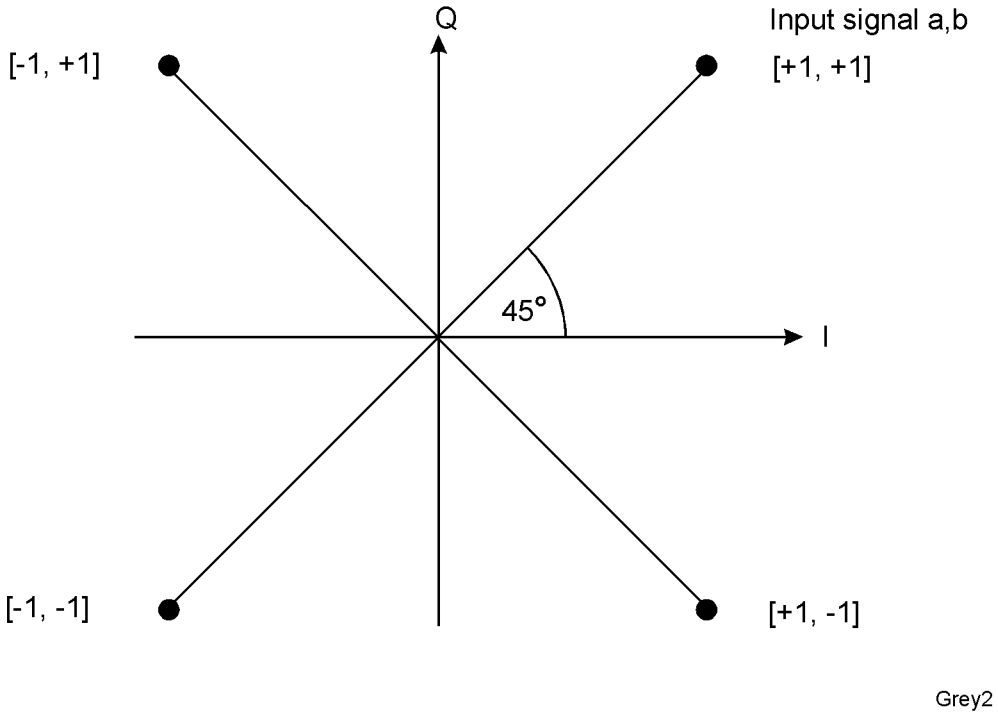


Figure 10. Relationship Between Input Data and Sin∆θ, Cos∆θ

A_k B_k	A_{kG} B_{kG}	$\Delta\theta$	**cos** $\Delta\theta$	**sin** $\Delta\theta$
0 0	-1 -1	$5\pi/4$	-0.7	-0.7
0 1	-1 +1	$3\pi/4$	-0.7	+0.7
1 0	+1 -1	$\pi/4$	+0.7	-0.7
1 1	+1 +1	$7\pi/4$	+0.7	+0.7

A_{kG} = -1 if ($\cos\Delta\theta$) < 0 and, B_{kG} = -1 if ($\sin\Delta\theta$) < 0, by inspection. Therefore equations [4] and [5] may be rewritten as:

$$I_k = (I_{k-1} * A_{KG} - Q_{k-1} * B_{kG}) * 0.707 \quad [6]$$

$$Q_k = (Q_{k-1} * A_{kG} + I_{k-1} * B_{kG}) * 0.707 \quad [7]$$

System Design and Program Structure

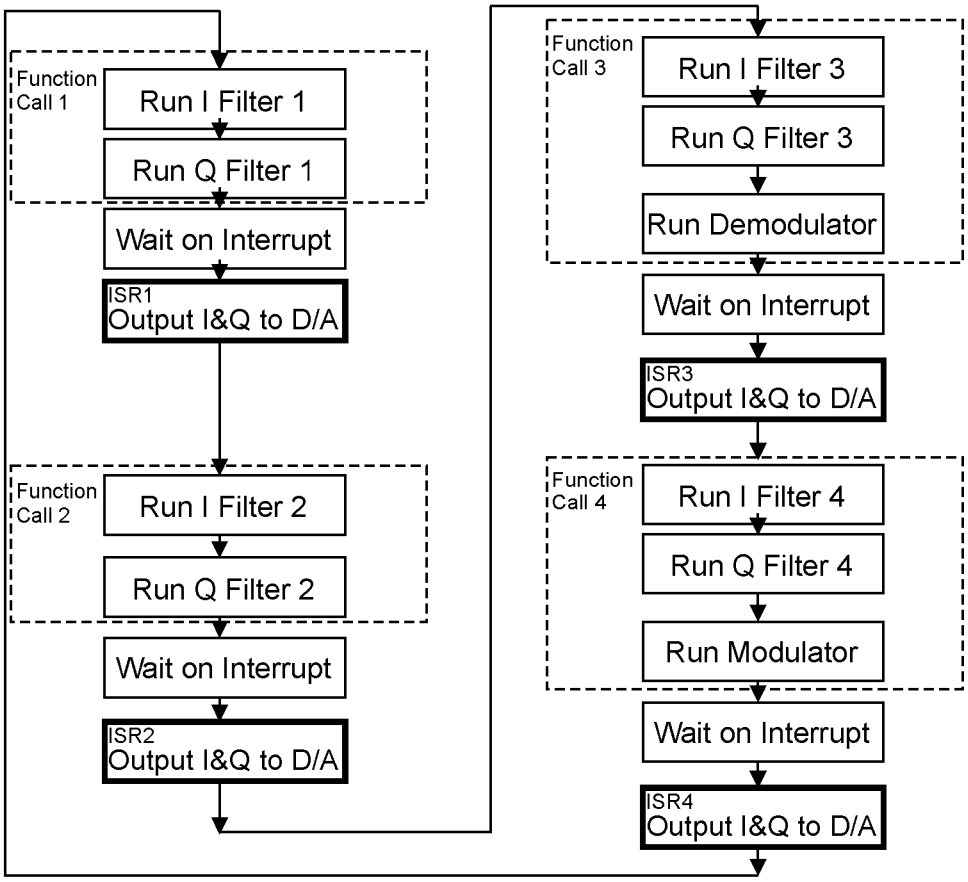
Pulse-shaping may be used to reduce Inter-Symbol Interference. In this work, the I and Q data streams were shaped by a 20 tap FIR filter and the output was sampled by the D/A converter which will also create unwanted spectral images at intervals of the sampling frequency. These images need to be removed by the reconstruction filter. The greater the distance between the first image and the first component the lower the order of the reconstruction filter. A process called interpolation is used to achieve this. (see *Interpolation*) This necessitated the use of four interrupts per program cycle to over-sample the input I & Q symbol waveform.

The program is designed around a four interrupt structure, Figure 11. The rectangular shaped pulses representing the I and Q channels at the output of the modulator are pulse shaped using raised cosine filters. A high sampling rate increases the computational requirements of the DSP. If the 'window' on the number of past and present I or Q pulses is fixed (five were used in the program) then increasing the sampling rate requires an increase in the number of filter taps and hence, again, increased computational requirements. For these reasons four interrupts are typically used in a 20 tap filter system.

The symbol timing module would indicate to the demodulator the optimum time to sample the incoming waveform. As this was part of future work the demodulator module is called consistently in function call 3 only.

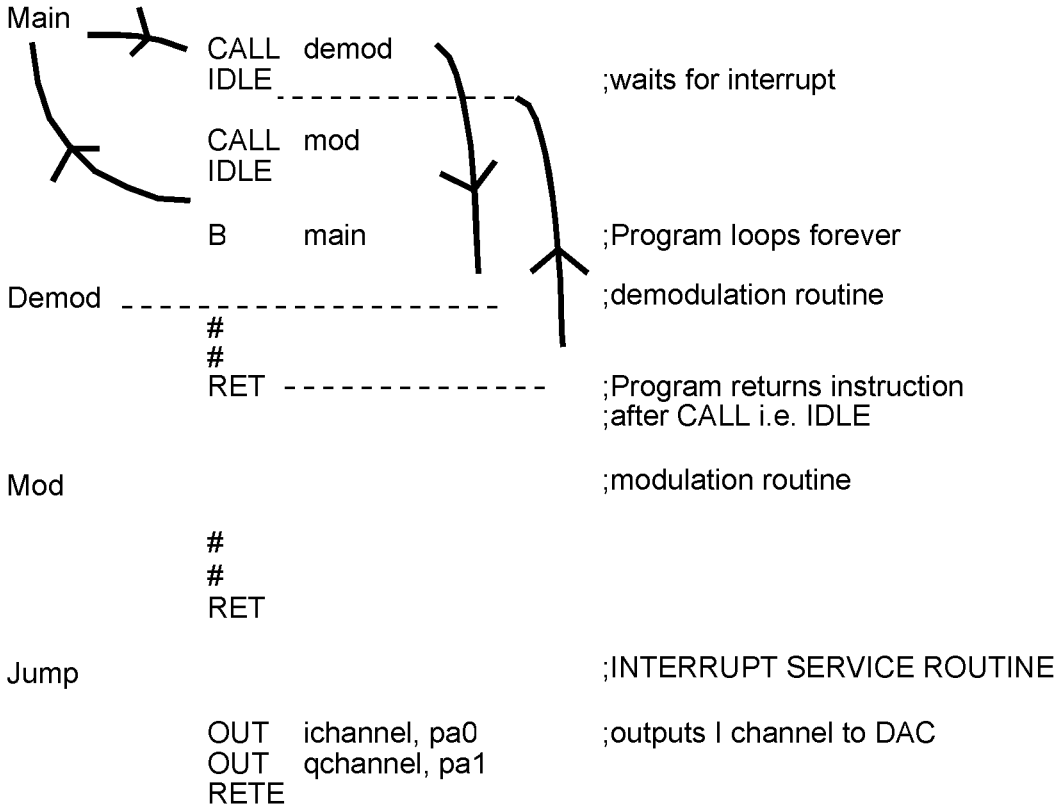
Each module in the program (i.e. filtering, modulator and demodulator) takes a different amount of time to execute. However, the I and Q outputs from the modulator must be produced at a constant time period. This is achieved by placing a wait ('IDLE') state at the end of each module and using a timer interrupt to start the interrupt service routine (ISR).

Figure 11. Program Structure



During each ISR, the output values of the I & Q filters are written onto the data bus and hence to the D/A converter. A simplified excerpt from the program code is shown in Figure 12. The filtering module process has not been shown for clarity.

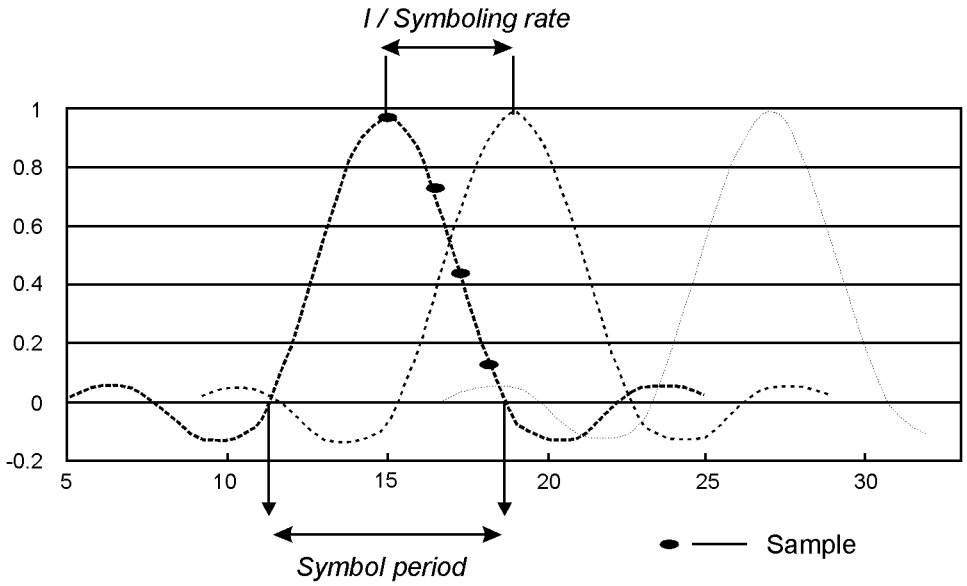
Figure 12. Program Function Calls



Data Throughput

The time between each interrupt depends on the value loaded into the PRD register. This was set for a 10 us period. There are four timer interrupts in the program and hence one complete program cycle is 40 us (25 kHz). The symboling rate in either I or Q channel is also 25 kHz (Figure 13). Two bits being modulated for each symbol gives a bit rate of 50 kHz. The baseband bandwidth occupied in each channel is given by: (1 +α) ***** Symboling rate */* 2; where α is the raised cosine filter 'roll-off' factor. The RF bandwidth required after up-conversion would be twice the baseband bandwidth.

Figure 13. Symboling Rate



Inter-Symbol Interference (ISI)

The frequency response of a rectangular pulse is a sine function containing an infinite number of frequency components. Therefore in all practical channel mediums where the bandwidth is limited the rectangular pulse will be distorted in both amplitude and phase; thus affecting the next pulse. This is called 'Inter-Symbol Interference'. The amount of ISI may be reduced by shaping the digital pulses so that the sampling instant coincides with the zero crossing of the adjacent symbols. A sine function satisfies this criteria and offers the highest possible symbol rate which can be transmitted using the minimum Nyquist baseband frequency. The sine function, (α=0), represents a 'brick-wall' filter in the frequency domain. The spectra of the raised cosine filter, ($\alpha > 0$), is smoother and hence easier to implement practically. Raised cosine filtering is usually achieved by implementing a root raised cosine filter as part of the modulator and demodulator.

In the practical situation the maximum number of taps is compromised by processor speed limitations. In the time domain, limiting the number of taps truncates the impulse response and results in undesirable side lobes generated in the frequency domain. As α approaches zero the side lobes rise up to the principal pass-band lobe attenuation level and hence the desired filtering characteristic is unachievable.[4] An α of about 0.2 is achievable by the clock speed of today's DSPs.

Interpolation

Interpolation is a powerful signal processing concept which strongly influences the hardware reconstruction filter specification and digital filter design. Interpolation involves sampling the input waveform at a greater rate than the existing samples are produced (Figure 14) by interposing extra samples in between them. This can be achieved by repeating existing samples or inserting zero impulses. The design used here uses the latter as it simplifies the filtering algorithm (Figure 15 and Figure 16).

Figure 14. (a) Existing Sampling. (b) Interpolation Sampling. (- - - = Hardware Reconstruction Filter Characteristic)

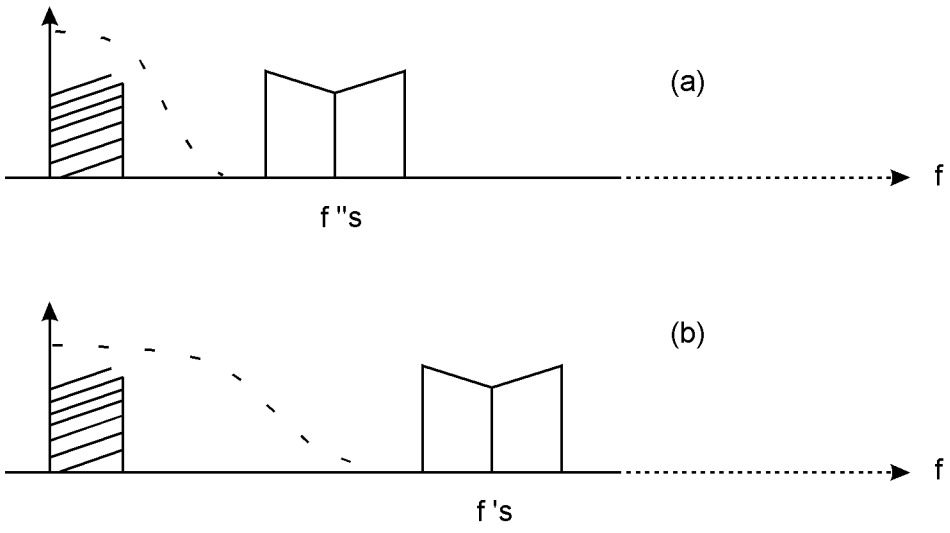


Figure 15. Insertion of Zero Pads (i)

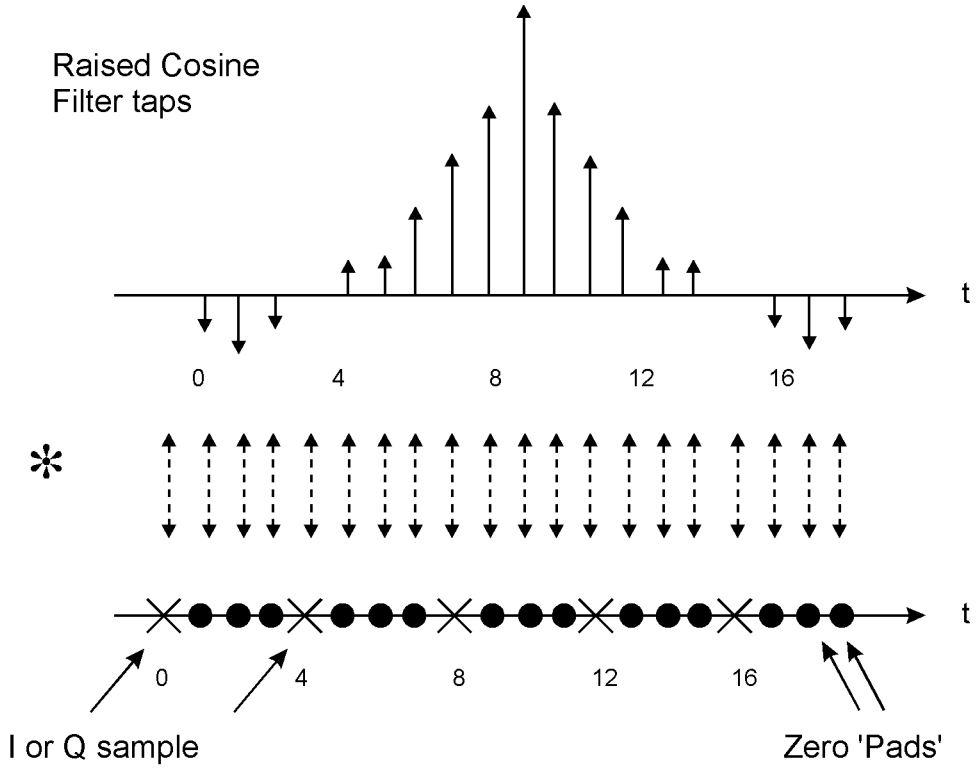
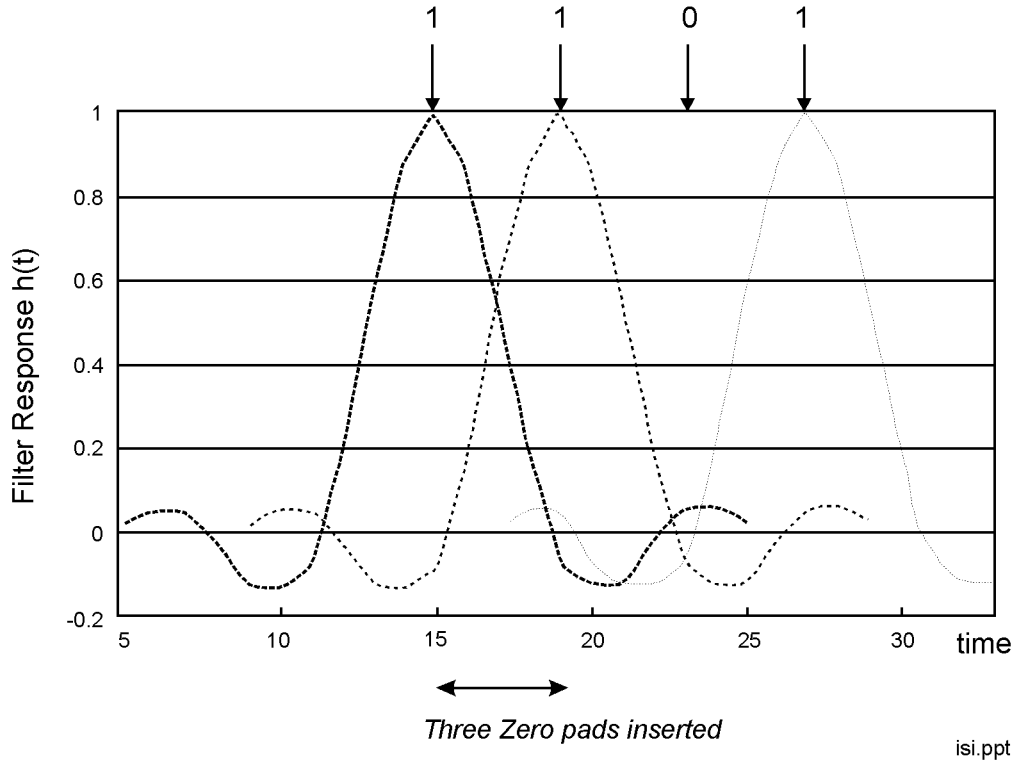


Figure 16. Insertion of Zero Pads (ii)



DSP Raised Cosine FIR Filter Implementation

To increase the sampling rate by four times, three zero pads are 'inserted' in between each of the five I channel data stream symbols. The convolution signal is thus:

$x(n) = \{I_0, 0, 0, 0, I_{-1}, 0, 0, 0, I_{-2}, 0, 0, 0, I_{-3}, 0, 0, 0, I_{-4}, 0, 0, 0\}$.

The output of the FIR filter, $y(n) = \Sigma\, h(k).x(n-k)$, is then computed. After three convolutions a new I value, I_1, will enter the equation and the oldest I value, I_{-4}, is dropped. Four samples per symbol requires the filtering to be completed within four separate interrupts.

$y[0] = h[0]x[0] + h[1]x[-1] + h[2]x[-2] + ... + h[19]x[-19]$

$y[1] = h[0]x[1] + h[1]x[0] + h[2]x[-1] + ... + h[19]x[-18]$

: : : : : :

$y[19] = h[0]x[19] + h[1]x[18] + h[2]x[17] + ... + h[19]x[0]$

Through noting that fifteen of the multiplications in each convolution are by zero, processor time can be saved by simply multiplying by the five coefficients used.

$y[0] = h[0]\, I_0 + h[4]\, I_{-1} + h[8]\, I_{-2} + h[12]\, I_{-3} + h[16]\, I_{-4}$

$y[1] = h[1]\, I_0 + h[5]\, I_{-1} + h[9]\, I_{-2} + h[13]\, I_{-3} + h[17]\, I_{-4}$

$y[2] = h[2]\, I_0 + h[6]\, I_{-1} + h[10]\, I_{-2} + h[14]\, I_{-3} + h[18]\, I_{-4}$

$y[3] = h[3]\, I_0 + h[7]\, I_{-1} + h[11]\, I_{-2} + h[15]\, I_{-3} + h[19]\, I_{-4}$

$y[4] = h[0]\, I_{+1} + h[4]\, I_0 + h[8]\, I_{-1} + h[12]\, I_{-2} + h[16]\, I_{-3}$

etc.

The **MAC** instruction is used in interrupts 1,2&4 of the modem implementation.

```
lar     ar5,#Ilocs      ;Data samples held in Ilocs
nop
nop
nop                     ;Flushes pipeline
rptz    #4              ;Repeats (MAC) 5 times
mac     IRC1,*+         ;Pipelined multiply and accumulate
                        ;with I filter coeffs.
apac                    ;Adds final product to accumulator
sach    Ifiltered,1     ;Stores accumulator result
```

The **MACD** instruction is used in the third interrupt to first compute the convolution and then to shift the data to make room for a new I or Q symbol at the next program cycle (Figure 17).

Figure 17. Contents of Memory Locations Before and After MACD Operation

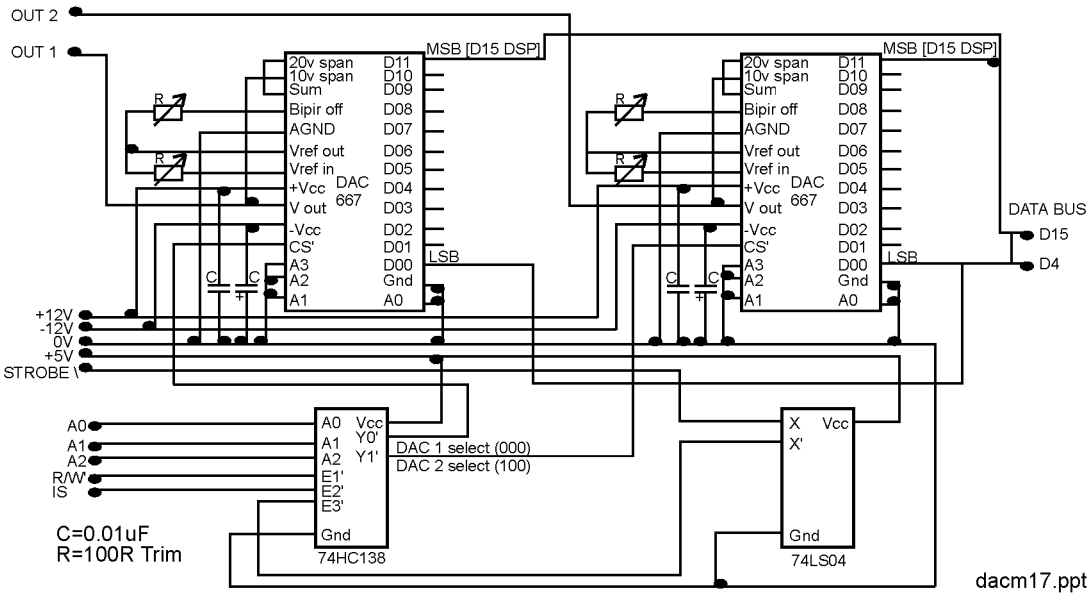
Interrupt	Consecutive Memory Locations						Comments
	d0	**d1**	**d2**	**d3**	**d4**	**Space**	
n	I_0	I_{-1}	I_{-2}	I_{-3}	I_{-4}	(I_{-5})	Before MACD operation
n+1	I_0	I_0	I_{-1}	I_{-2}	I_{-3}	I_{-4}	After MACD data shift
n+1	I_{+1}	I_0	I_{-1}	I_{-2}	I_{-3}	I_{-4}	New Value I_{+1} overwrites I_0

Digital to Analogue Converter Circuit

The aim of the DAC circuit is to convert the data output from the DSP into an analogue signal which could be transmitted via a two wire transmission line. Although the DSK kit has an inbuilt DAC (and ADC) circuit, there is only one channel available. Also, the maximum sampling frequency of the DSK DAC circuit is 19.2 kHz, which is below the required modem sampling frequency.

In the bipolar mode the maximum output voltage is obtained when all the data bits are high [FFFh]. A conversion is therefore required to map the maximum positive DSP value of 7FFh to FFFh of the DAC. This is realised in the program by the addition of 800h to both I and Q channel words prior to the output write operation. Note that the 12 MSBs of the 16 bit DSP data bus are connected to the 12 bit DAC data bus (Figure 18).

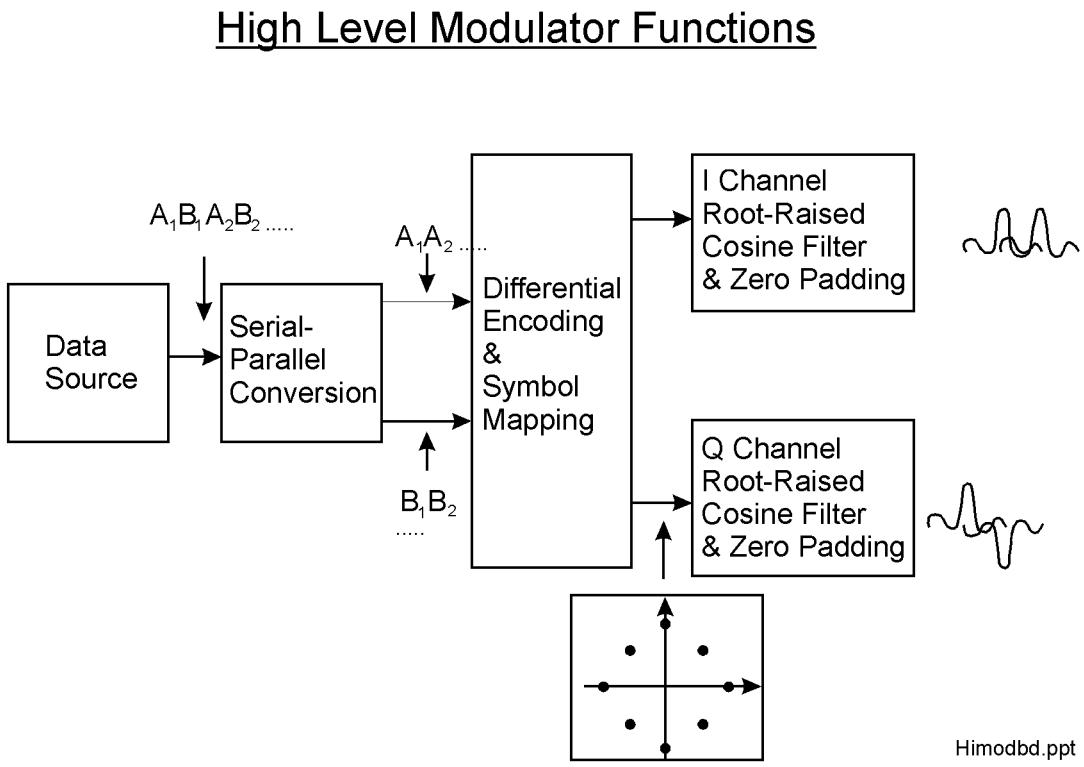
Figure 18. Two Channel DAC Circuit Diagram



Modulator Implementation

The aim of the baseband modulator is to map data bits onto a π/4 shift D-QPSK constellation and spectrally shape the baseband I and Q pulses (Figure 19). Four different designs for the symbol mapping were researched. This report describes the look-up table design using circular buffers.

Figure 19. High Level Modulator Functions



Signal Mapping

The pair of equations to calculate the I and Q streams were derived in the section, *Generation of π/4 D-QPSK Signals*:

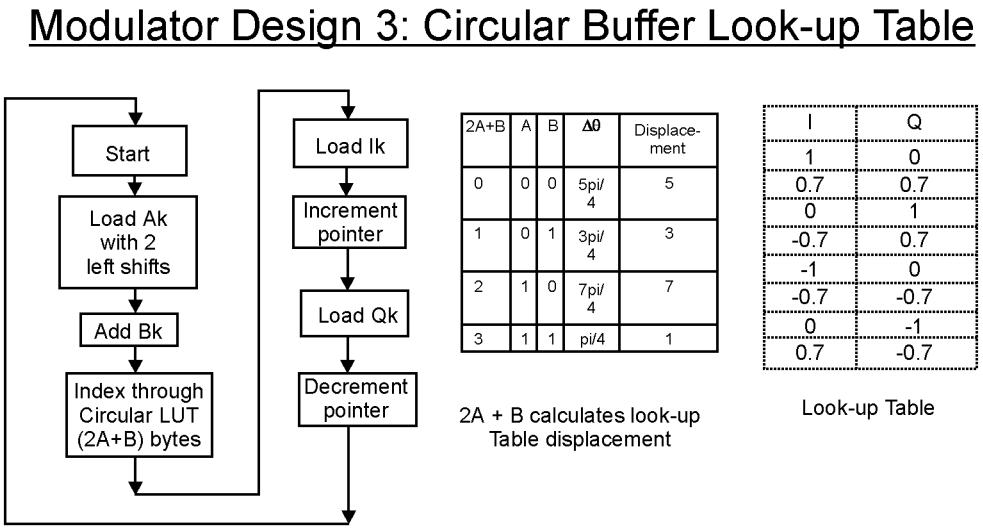
$$I_k = (I_{k-1} * A_{KG} - Q_{k-1} * B_{kG}) * 0.707 \quad [8]$$

$$Q_k = (Q_{k-1} * A_{kG} + I_{k-1} * B_{kG}) * 0.707 \quad [9]$$

Two key aims when implementing the signal mapping equation are speed and accuracy. Techniques that avoid the direct calculation of the formula are desirable. This is achieved by considering the π/4 D-QPSK constellation and searching for a relationship between the input signals A_k B_k and the value of the absolute phase, θ. Circular addressing is an important feature of DSPs. A start address and end address are loaded into the corresponding buffer registers and a delegated auxiliary register acts as a pointer to the buffer. A value is loaded into the index register, INDX, to specify the step size for increments through the array. Once the end of the array is met, the pointer returns to the beginning of the buffer.

The eight points of the π/4 QPSK constellation form the look-up table in Figure 20. Gray Coding of the input data results in a displacement through the look-up table, as shown in the left table of Figure 20.

Figure 20. Circular Buffer Look-Up Table



As an example, if the present constellation point is $[I_k, Q_k] = [0, -1]$ (row 7 of the right table) and the input data is $[A_k, B_k] = [0, 0]$ a displacement of five rows (i.e. content of position 2*0 + 0 of the left table) is implied in the left look-up table. As the left look-up table is contained in a circular buffer, after two displacements the pointer loops to the beginning of the table. Three further row displacements are made and the data in row four is recovered: [I, Q] = [-0.7, 0.7].

Problems Encountered

[i] If the displacement causes the register to point to the points of the last row in the look-up table.

In this situation the I_k value would be loaded; the pointer incremented; the Q_k value loaded and then the pointer would *ideally* decrement in preparation to load the consecutive value of I_{k+1} in the next signal mapping cycle. The problem is caused, however, by not being able to decrement the pointer (or any index operation) if the auxiliary register pointer is currently at the circular buffer end register.

Solution: A 'dummy' column containing zeros after the I and Q columns, which whilst never being used would prevent the last Q address in row eight being situated at the circular buffer end address. A minor variation on this technique is to insert an additional column of zeros which would result in each row containing four elements. Four elements, being a power of two means that once the displacement has been calculated in the accumulator, a shift left of two places could be achieved at no additional execution time overhead. Three elements, however, would have required an extra calculation and hence program cycle, increasing the execution time.

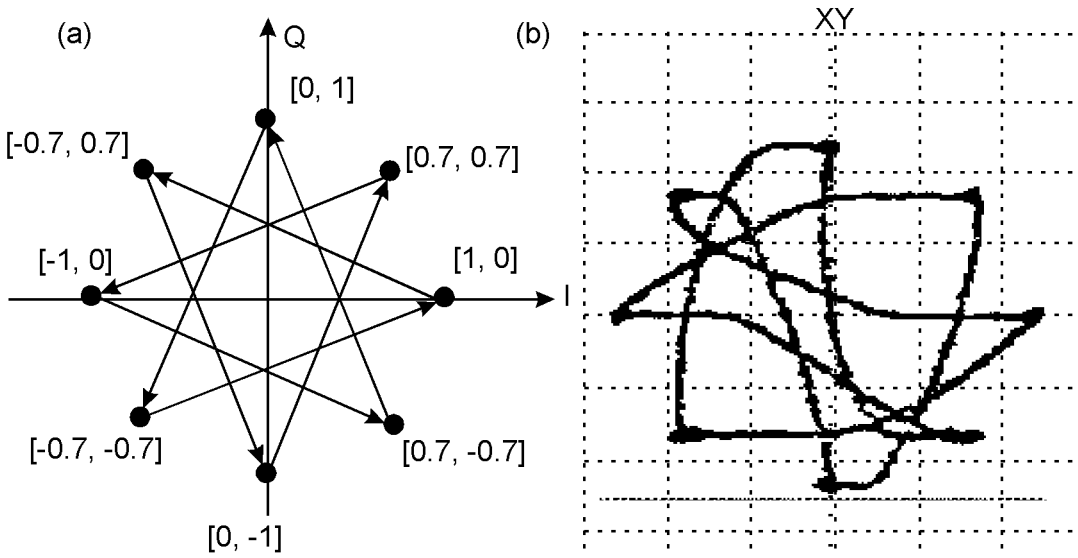
[ii] If the INDX register is not equal to one and the displacement causes the pointer to pass the circular buffer end register. In this situation the auxiliary register pointer leaves the buffer and does not return to the begin register!!

Solution: The INDX register was set to one. The RPT instruction repeated the MAR *+ instruction (increment by 1 the auxiliary register pointer) the required number of steps through the array.

Modulator Performance

The characteristic feature of *differential* π/4 QPSK is clearly shown in the test pattern Figure 21a. It shows the theoretical phase transitions (3π/4) in modulating a constant pattern of binary data: 01, 01, …, 01. Figure 21b is the plot obtained, in practice, by connecting the I-channel and the Q-channel DAC output to the X-channel and Y-channel of the oscilloscope respectively. The theoretical cyclic pattern is clearly repeated. The exact path in the transition from one point on the constellation to the next, however, is undefined. The DAC output, consisting of rectangular (time domain) pulses contains frequency domain components extended to infinity. The oscilloscope probes, however, exhibit a low-pass characteristic thus attenuating these higher order components, introducing a time delay discussed in *Modulation Techniques*. The loci was indeed observed to change when adjusting the oscilloscope probe capacitance.

Figure 21. Unfiltered I-Q Constellation. Data [01, 01, …, 01] ⇒ 3π/4 Shift; (a) Theoretical Result; (b) Practice



π/4 D-QPSK Signal Mapping

Figure 22 records the signal values of the I and Q channels for a repeated input data sequence of [01]. The eight constellation points in π/4 D-QPSK are observed and repeated after eight symbols.

Figure 22. I & Q From Data Sequence of [01]

Input	Δθ	I	Q
01	3π/4	0.7	0.7
01	3π/4	-1	0
01	3π/4	0.7	-0.7
01	3π/4	0	+1
01	3π/4	-0.7	-0.7
01	3π/4	+1	0
01	3π/4	-0.7	0.7
01	3π/4	0	-1

Raised Cosine Filtering

Figure 23 - (Top) shows the unfiltered I stream at the output of the signal mapping module. The rectangular pulses contribute harmonic components which when passed through the band limited channel result in distortion. The raised cosine filtering removes ISI at the sampling point (see *Interpolation*). In the time domain four values (one at each interrupt) for the filter output are calculated for each rectangular pulse. The time delay observed by comparing the two channels represents the latency in the FIR filter.

Figure 23. Output of Raised Cosine Filter for I Channel (Top): Unfiltered (Bottom): Filtered

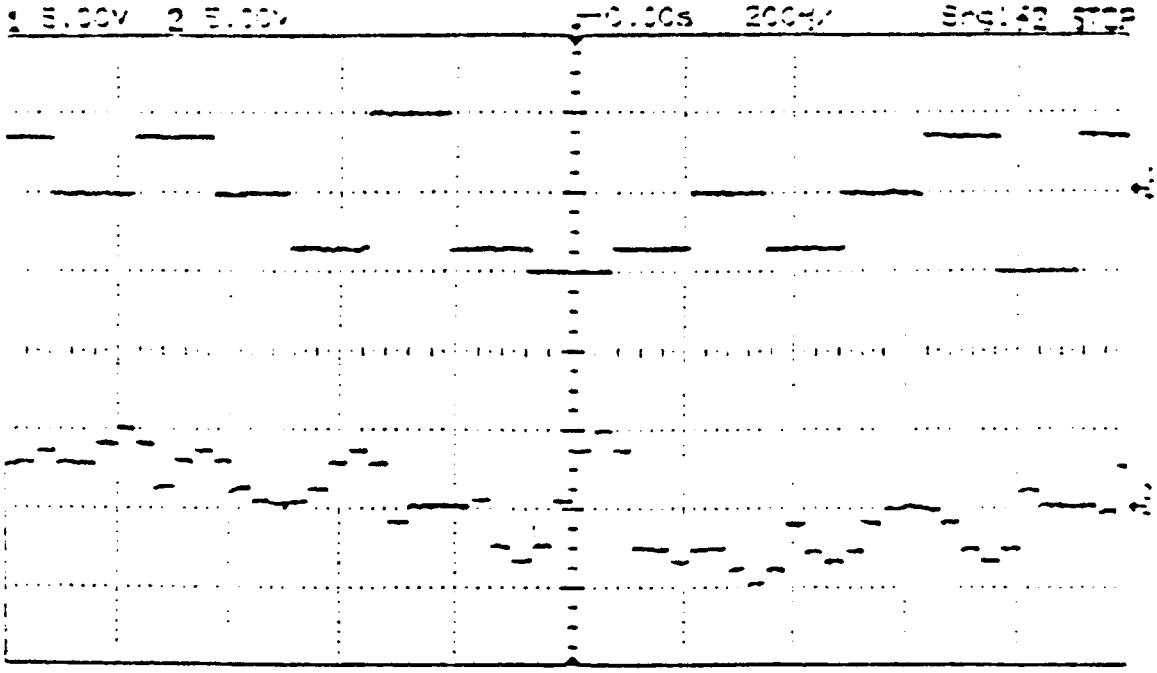
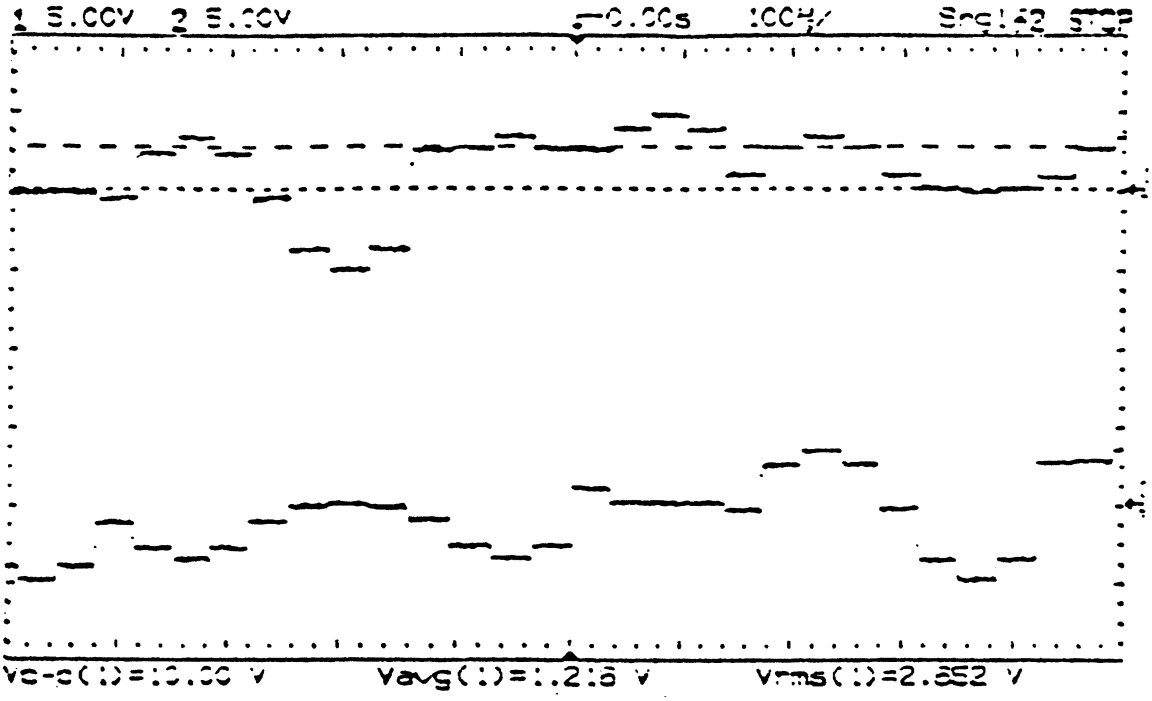


Figure 24. Output of Raised Cosine Filter for I & Q Channels: (Top) I-Channel (Bottom) Q-Channel



Reconstruction Filter

Figure 25 (Top) shows the raised cosine filtering described above. The reconstruction filter or 'Smoothing' filter produces a continuous signal (Bottom) from the discrete-sampled signal. Figure 26 shows a complete pair of I & Q reconstructed signals at the output of the finished modulator.

Figure 25. Output of Reconstruction Filter (I-Channel) for Input Data [11 10 11 00,…] (Top): Raised Cosine Filtered; (Bottom): RC & Reconstruction Filter

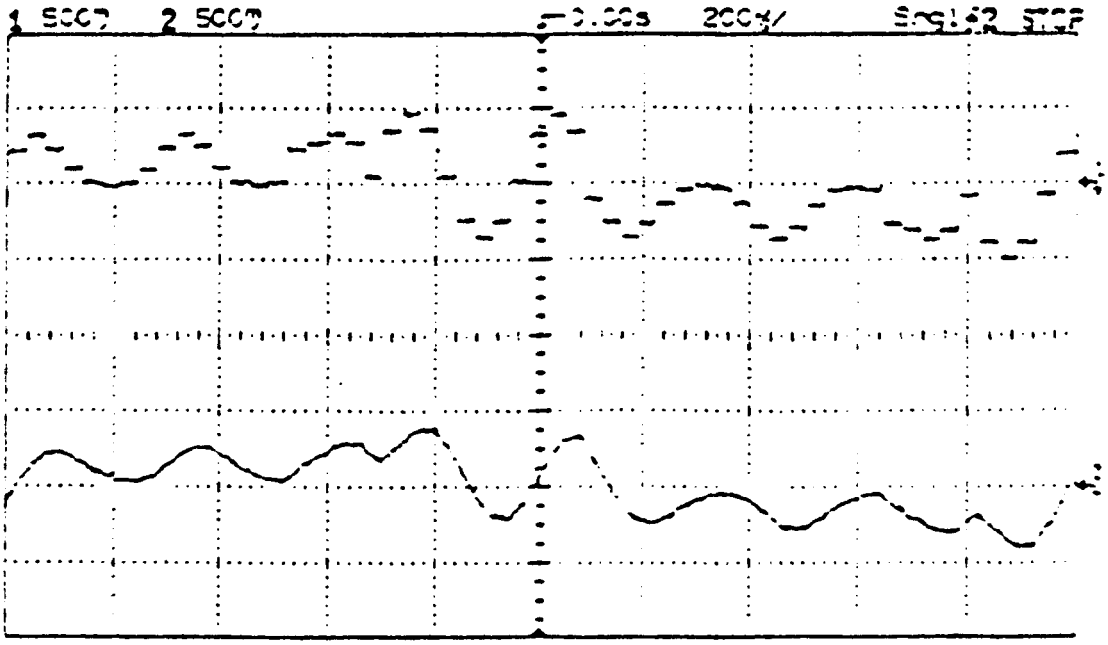
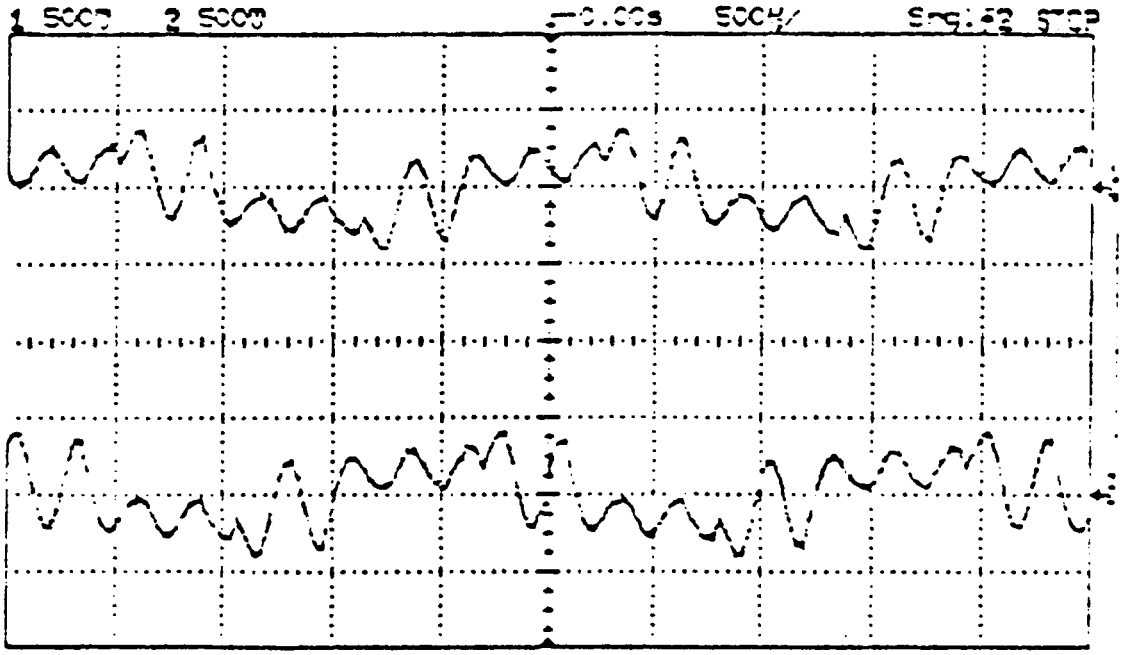


Figure 26. Output of Reconstruction Filter for Input Data [11 10 11 00,…]: (Top) I-Channel; (Bottom) Q-Channel



Demodulator Implementation

The aim of the demodulator is to recover the data from the received baseband phase signals, I and Q. A block diagram showing the principal modules is shown in Figure 27. A flowchart (Figure 28) summarises the differential detection and data recovery algorithms.

Figure 27. Baseband Demodulator

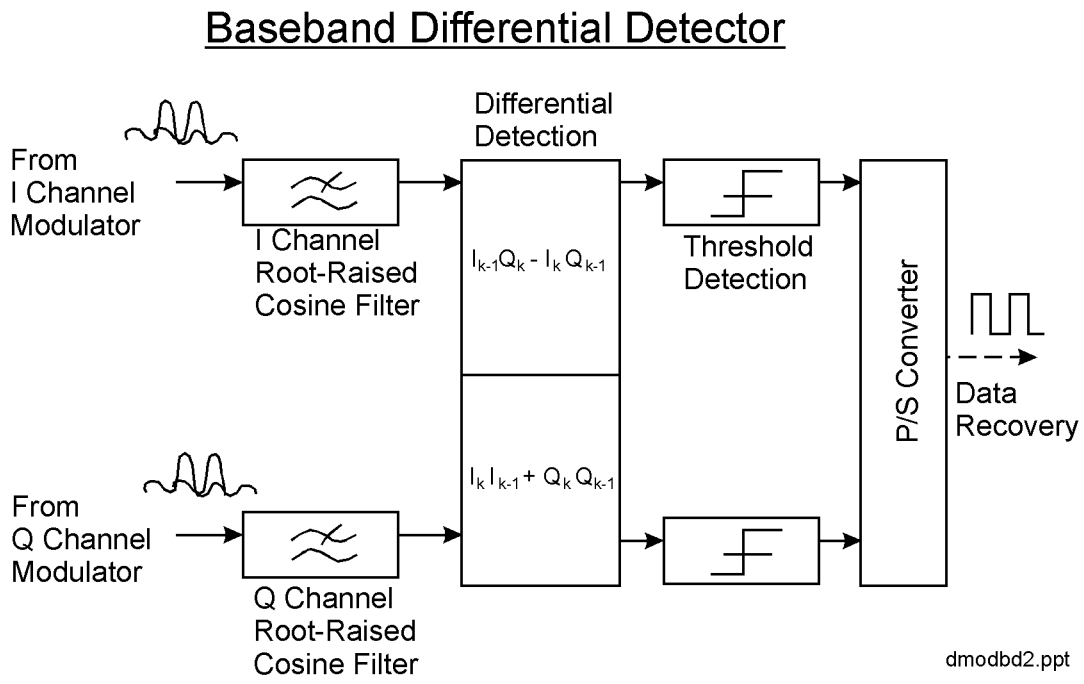
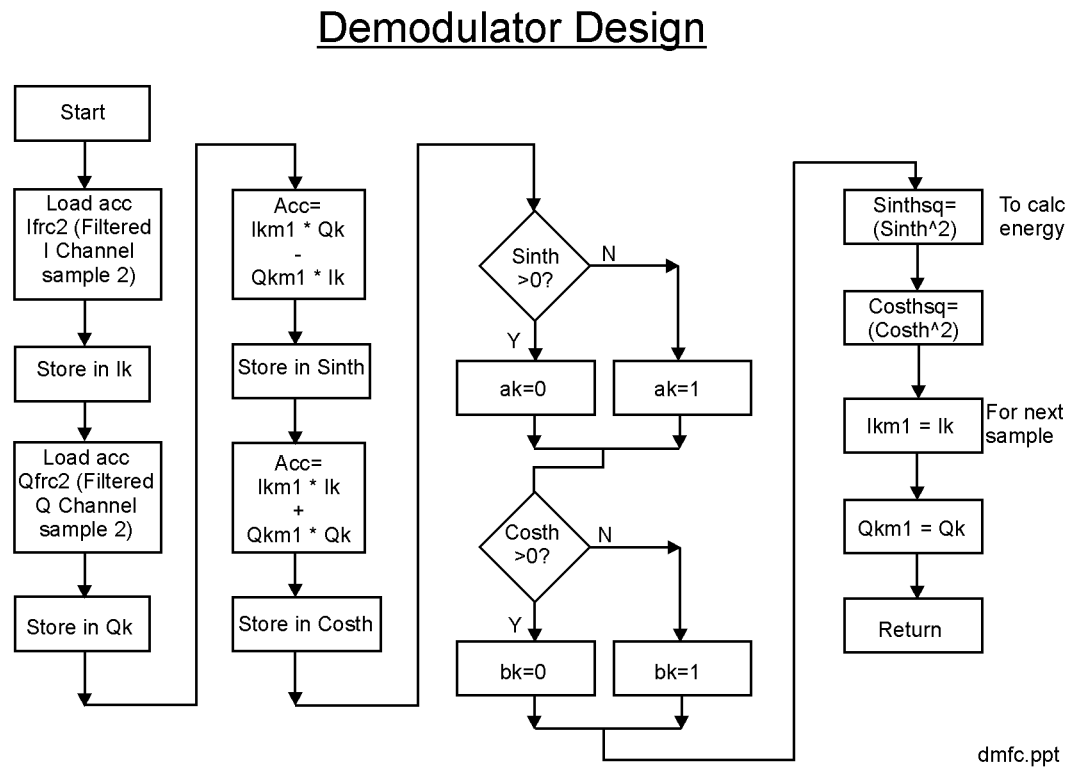


Figure 28. Demodulator Flowchart



Differential Detection of π/4 D-QPSK Signals

The aim is to recover the data symbols, A_k and B_k, from the four received phase signals, [I_k, Q_k, I_{k-1}, Q_{k-1}]. Equations [10] to [15] and Figure 29 show that A_k and B_k, can be determined from the sign of cosθ and sinθ respectively.

Figure 29. Data Recovery Using Sinθ and Cosθ

cosθ	**sin**θ	Δθ	A_{kG}	B_{kG}	A_k	B_k
+0.707	+0.707	1π/4	+1	+1	1	1
+0.707	-0.707	7π/4	+1	-1	1	0
-0.707	+0.707	3π/4	-1	+1	0	1
-0.707	-0.707	5π/4	-1	-1	0	0

Solving the two equations for the π/4 D-QPSK, equation [10] and [11], $\cos\theta_k$ and $\sin\theta_k$ may be derived.

$$I_k = I_{k-1} * \cos\theta_k - Q_{k-1} * \sin\theta_k \quad [10]$$

$$Q_k = Q_{k-1} * \cos\theta_k + I_{k-1} * \sin\theta_k \quad [11]$$

$$\cos\theta_k = \frac{Q_k * Q_{k-1} + I_k * I_{k-1}}{Q_{k-1}^2 + I_{k-1}^2} \quad [12]$$

And,

$$\sin\theta_k = \frac{I_{k-1} * Q_k - I_k Q_{k-1}}{Q_{k-1}^2 + I_{k-1}^2} \quad [13]$$

To calculate $\cos\theta_k$ and $\sin\theta_k$ using equation [12] and [13] is time consuming. However, if we look at Figure 29, we notice that:

1) If ($\cos\theta_k$ >0) then A_k = 1, otherwise A_k = 0

2) If ($\sin\theta_k$ >0) then B_k = 1, otherwise B_k = 0

Therefore we need only to calculate the sign of $\cos\theta_k$ and the sign $\sin\theta_k$ to determine A_k and B_k. Finally to calculate A_k and B_k we need to calculate equation [14] and [15] which are:

$$\text{Sign}(\cos\theta_k) = \text{sign}(Q_k * Q_{k-1} + I_k * I_{k-1}) \quad [14]$$

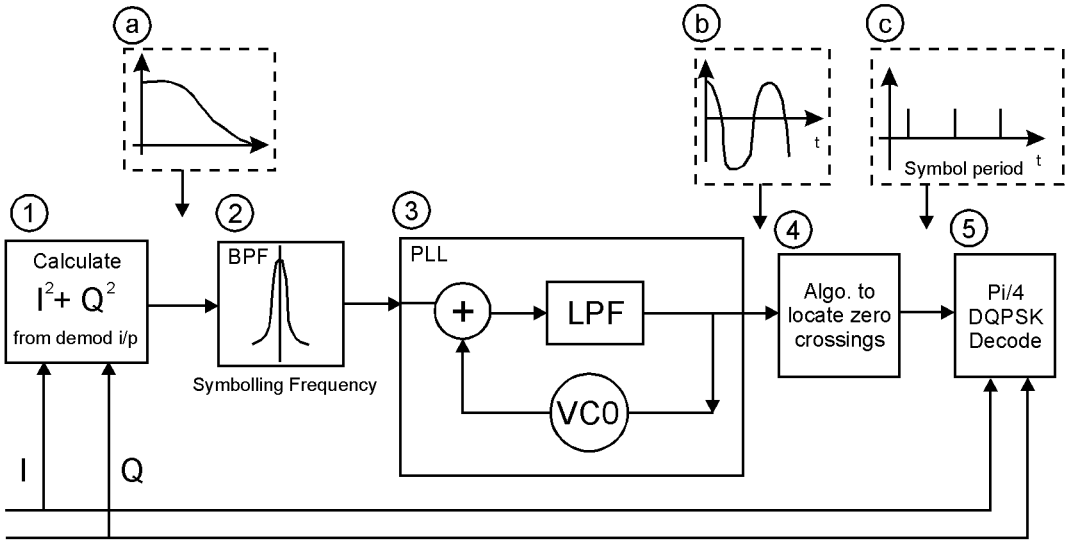
And,

$$\text{Sign}(\sin\theta_k) = \text{sign}(I_{k-1} * Q_k - I_k * Q_{k-1}) \quad [15]$$

Symbol Timing Recovery

At every interrupt, k, the instantaneous energy in both channels is calculated by $I_k^2 + Q_k^2$ (Figure 30) (1). A frequency domain plot (a) shows that an elevated tone appears at the symboling frequency. This signal is passed through a bandpass filter (2) centred at the symbol frequency. A phase locked loop (3) locks on to the centre frequency producing a single frequency sinusoid (b). The alternate crossings indicate the optimum time to sample the I and Q data stream. The zero crossing point is determined by an algorithm (4) which looks at successive samples to see if they are of opposite sign. A time delay may have to be inserted to compensate for BPF and PLL lines and the I and Q lines entering the pi/4 D-QPSK decoder (5).

Figure 30. Timing Recovery Process Using Energy Squaring Principle



Demodulator Performance

Figure 31 shows the output of the demodulator together with the data signal input to the modulator. The demodulated data stream is identical to the input data stream to the modulator albeit delayed by two samples. This samples representing the demodulator outputs produced at the end of interrupt four and the modulator output produced at the end of interrupt two. Figure 32 -top shows the output of the demodulator for even bits A_k and the bottom figure shows the demodulator output for the odd bit B_k. The plots are read together to show the output at any point in time. The input to the modulator can be seen at the output [1110 etc.].

Figure 31. Demodulator Output Showing Mod-Demod Latency. (Top) Modulator Input: Even stream, A_k; (Bottom) Demodulator Output A_k

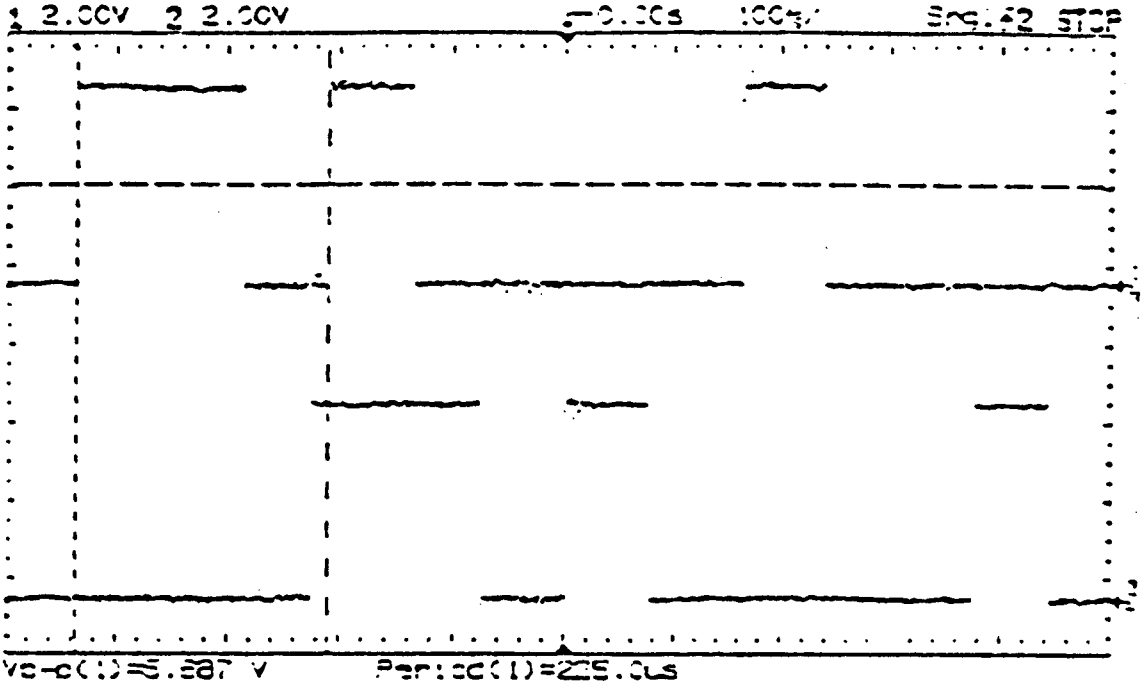
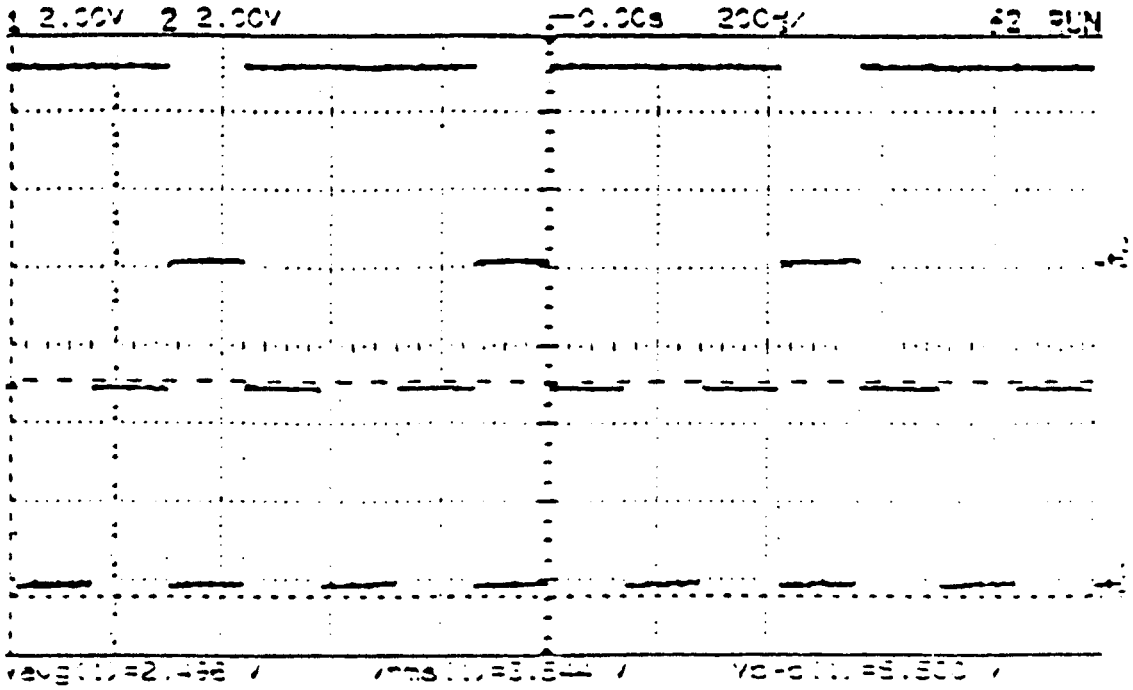


Figure 32. Demodulator Output for Input [11 10 11.00..] (a) Even Stream Output, A_k ; (b) Odd Stream Output, B_k



References

[1] Baker, P.A., Phase-modulation data sets for serial transmission at 2000 and 2400 bits per second, Part 1, AIEE Trans. on Communications Electronics. July 1962

[2] Webber. J.L., Desion & Construction of a Pi/4 D-QPSK Baseband Modem using the TM5320C50 DSP
Final year undergraduate thesis, University of Bristol, UK, 1996

[3] Aghvami, A., Digital Modulation Techniques for Mobile and Personal Communications Systems.
Electronics and Communications Journal
lEE, June 1993

[4] Nix A. R., A Fundamental Investigation into Short Range High capacity Mobile Data Transmission.PhD Thesis, University of Bristol, UK, 1994.