Symmetricom

DATA SHEET

SCi 2000 SoftClock

Embedded Software Clock Solution

Key Features

- Best in class clock recovery algorithm for IEEE 1588-2008 (PTP v2)
- Carrier-class embedded software based clock solution
- Multiple synchronization inputs including IEEE 1588, SyncE, E1/T1 and GPS
- Industry-leading frequency and phase performance
- Three configurable Sync service tiers for targeted performance under various network conditions
- Support for digital synthesis and varactor-steered architectures
- Extensive user control for sync input channel selection
- Advanced sync performance metric reporting
- Fast convergence time
- Support for multiple PTP packet Rates
- Architected for redundancy support

Key Benefits

- Single clock solution supporting multiple network applications simplifies design effort
- Targeted performance can be achieved even in the presence of high PDV
- Reduces total cost of ownership
- Operates with a wide range of oscillators including OCXO or miniOCXO
- End-to-end delay mechanism for on-path transparent clock enables network scalability
- Enables sync performance visibility through advanced metric reporting

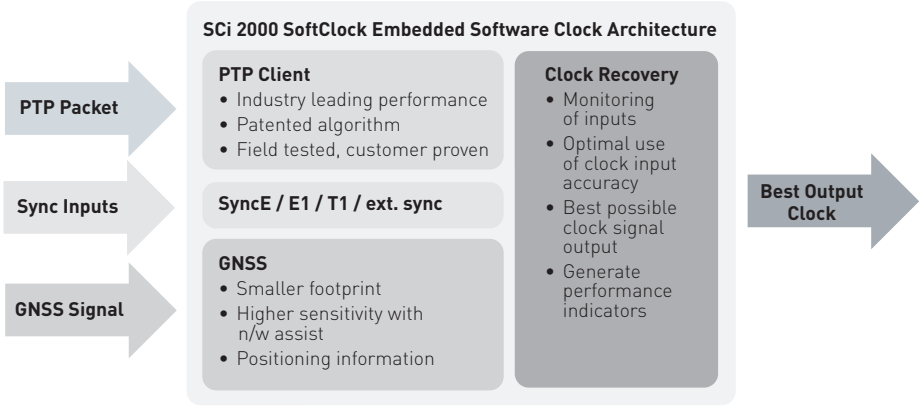
Product Overview

The Symmetricom® SCi 2000 SoftClock is an embedded software clock necessary for telecom network equipments migrating to packet networks from legacy TDM networks. SCi 2000 SoftClock implements a PTP ordinary slave-clock as defined in IEEE 1588. The clock supports other sync reference inputs, including SyncE, GPS, E1/T1, and redundant inputs from a peer clock. SCi 2000 SoftClock runs on a customers target hardware platform delivering high precision frequency and phase synchronization using Symmetricom's patented servo algorithm. The SCi 2000 SoftClock is designed to be hardware agnostic and provides a full-featured API set and sample FPGA functional blocks for easy and rapid development. The clock solution enables Network Equipment Manufacturers (NEMs) to leverage their choice of processor and other hardware blocks within their design to achieve superior performance. Fully verified reference design and development tools are available to shorten the developer's time to market.

Product Applications

Most network equipment today uses dedicated timing hardware to deliver synchronization. This design model faces severe challenges in next generation networks which require small form factor, high performance and low operational cost. Operators are competing to offer better services with lower fees. NEMs are pressured to deliver solutions with minimum total cost of ownership. Using

Figure 1: SCi 2000 SoftClock Embedded Software Clock Architecture



SCi 2000 SoftClock

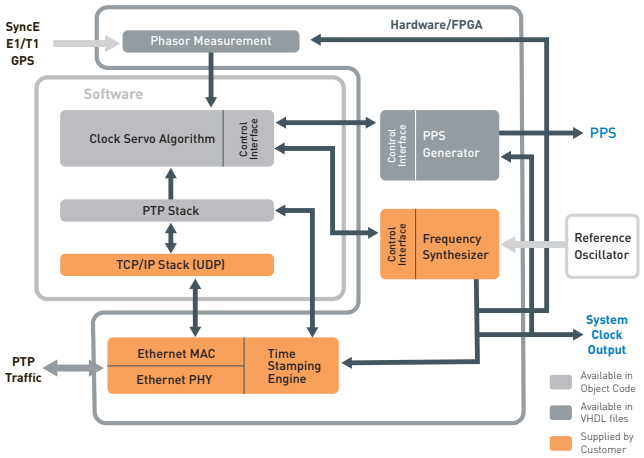


Figure 2: The SCi 2000 SoftClock operates in synthesizer mode

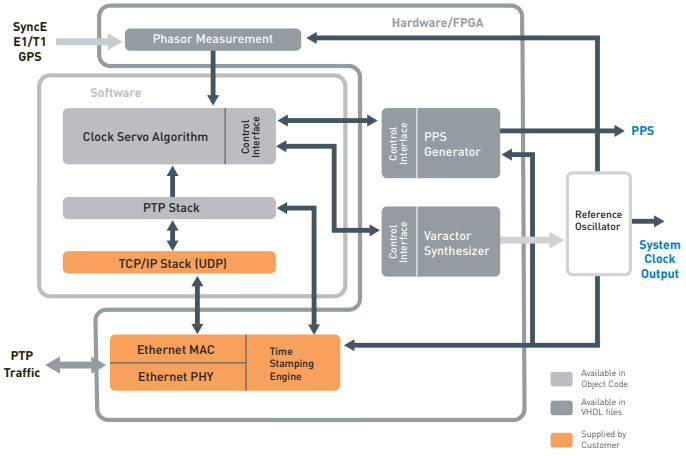


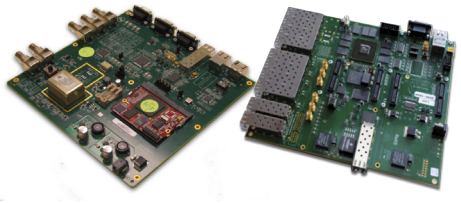
Figure 3: The SCi 2000 SoftClock operates in analog loop mode

a complete synchronization solution will eliminate dedicated timing blocks, resulting in a smaller footprint, lower power consumption, simpler operation, and a highly integrated cost effective solution. Devices that can take advantage of the SCi 2000 SoftClock include base stations, cell site aggregation switches, access routers, and mobile backhaul devices.

Product Functions

SCi 2000 SoftClock is an embedded software clock solution designed to be architecture and hardware-platform agnostic. This flexibility allows the SoftClock to operate in Synthesizer and Analog Loop Modes, to work with different types of reference oscillators, to interact with internal and external time stamping units and have the capability to be integrated into a target hardware platform regardless of the desired output frequencies. The SCi 2000 SoftClock configuration interface allows users to specify the transport mode, signal quality level (use of synchronization status messaging), input priority (as an input channel selection method) and oscillator quality that is possible with OCXO and mini-OCXO. Since SCi 2000 SoftClock supports multiple inputs simultaneously, it can use any of the input sync channels when a preferred input is not available or unusable. For PTP inputs, SCi 2000 SoftClock also provides fractional frequency and time accuracy estimation based on packet availability, packet stability, and network jitter. These estimators and statistics are available to network operators, who can monitor the performance of the devices effectively and take corrective action when needed.

SCi 2000 SoftClock provides three configurable Sync service tiers that define network performance expectations for PTP services. Each service tier identifies a performance target for a given set of network conditions. Upon configuring the required tier, the impact of Packet Delay Variation (PDV) in the transport network can be taken into consideration and target frequency and time output performance can be achieved.



Demonstration Platform Design

The image above show two examples of fully proven and validated designs based on Freescale MPC8313 PowerQUICC II Pro, Altera Stratix FPGA and PMC Sierra WinPath3, respectively. These demo designs can be easily adapted into the customer target platform to minimize design effort and reduce time to market.

SCi 2000 SoftClock Developer's Kit

- Documentation
  - User's Guide
  - API Reference
  - Developer's Guide
  - Evaluation board schematics and BOMs
- Software Release Note (SRN)
- SCi 2000 SoftClock library in binary form
- SCi 2000 SoftClock FPGA VHDL source

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